MAINTENANCE MANUAL

VOLUME I

LINC-8

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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VOLUME I

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(PROGram OF OPeration)

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CHAPTER 1
INTRODUCTION

1.1 SCOPE

LINC-8 is a high-speed, dual-computer system manufactured by Digital Equipment Corporation (DEC), Maynard, Massachusetts. The two major subsystems of the LINC-8 are the LINC (Laboratory INstrument Computer), and the PDP-8 (Programmed Data Processor 8). This maintenance manual describes the LINC subsystem, the interface between the PDP-8 and the LINC, and PDP-8 modifications necessary for LINC operation.

The LINC-8 Maintenance Manual is divided into two volumes. Volume I consists of five chapters organized in the following manner. Chapter 1 is a general introduction to the maintenance manual. Chapter 2 summarizes the functions of PROGOFOP (PROGram OF OPeration for the LINC-8). The system logic is described in Chapter 3, while Chapter 4 presents timing diagram descriptions for each LINC instruction. Maintenance and checkout procedures for the system are found in Chapter 5. In addition, Volume II of the LINC-8 Maintenance Manual contains engineering drawings for the basic LINC-8 system; included are logic schematics, instruction timing-flow diagrams, mechanical drawings, and module schematics not found in other related documents.

A complete set of engineering drawings is delivered with each LINC-8. In some cases of custom-design or design improvements, certain descriptions in this manual may conflict with information shown on drawings for a particular system. The drawings reflect the system as delivered and are therefore of greater validity than the basic system discussions.

1.2 PURPOSE

The LINC-8 Maintenance Manual is one of several documents related to the LINC-8 Computer. The level of discussion in this manual assumes that the reader understands the basic functional operation of single-address, fixed-word length, parallel computers using 1s and 2s complement binary arithmetic. This manual also references information contained in other LINC-8 literature. Refer to Table 1-1 for a complete list of related documents for use with this manual.

Table 1-1
Related Documentation

Document Number	Title	Description
C-800	Digital Small Computer Handbook	Both the LINC-8 and PDP-8 Users Handbooks are contained in this document. The LINC-8 section includes an introduction to the LINC-8 Computer, its basic organization, and its operation. The PDP-8 section contains similar information for the PDP-8 Computer.
F87	PDP-8 Maintenance Manual	This manual contains maintenance information for the PDP-8 Computer. With minor differences explained in the LINC-8 Maintenance Manual, the F-87 provides information for the PDP-8 subsection of the LINC-8 Computer.
I-L85 (A)	LINC-8 Programming Manual	LINC-8 programming information appears in this document.
DEC-L8-DSS0-D (Volume I) DEC-L8-DSS1-D (Volume II)	SUDSY (SUper Diagnostic SYstem)	SUDSY (Volumes I and II) describes the major diagnostic maintenance program for the LINC subsection. It is a collection of subprograms, each of which tests a particular LINC section function.
DEC-L8-SFA0-D	PROGOFOP	This programming document describes the current version of PROGOFOP in detail. Chapter 2 of the LINC-8 Maintenance Manual summarizes the functions of PROGOFOP.
	LINC-8 Software Package	This software package is supplied with each system and contains updated programming and operating information for the LINC-8.
561	Tektronix Type 561 Oscilloscope Maintenance Manual	The LINC-8 display oscilloscope is described in this document.

1.3 REFERENCE CONVENTIONS

Reference conventions used throughout this manual are similar to those in the PDP-8 Maintenance Manual, F-87. Certain reference conventions are explained below to aid in effective text presentation and readability.

1.3.1 Engineering Drawings

The majority of LINC-8 engineering drawings are referenced in text by the number of letter-number combination appearing at the end of the complete drawing number. For example, drawing BS-D-LINC8-0-2 is referenced as drawing 2. Drawing BS-D-LINC8-0-L2 is referenced as drawing L2. Certain drawings, such as MAGtape transport drawing AD-D-7404150-00, are referenced by their complete number. LINC-8 drawings use standard DEC symbology as described in Chapter 10 of the PDP-8 Maintenance Manual.

1.3.1.1 Signal Origins - Each engineering drawing for the LINC subsystem shows certain signals which originate on other engineering drawings. A table at the bottom of each drawing lists these signals and their drawing origin. For brevity, the origins are referenced only by the number or letter-number combination appearing at the end of the complete drawing number.

1.3.2 Illustrations

References to in-text illustrations and tables include the chapter prefix number such as Figure 3-3, or Table 5-1.

1.3.3 Signal Mnemonics

Uncommon signal mnemonics are explained parenthetically the first time they are mentioned in the discussion, e.g., GNI (get next instruction).

1.4 PHYSICAL DESCRIPTION

Chapter 9 of the LINC-8 Users Handbook describes physical characteristics, installation requirements, and interfacing capabilities of the LINC-8 Computer. As a supplement to that chapter, this section details the physical location of modules within the computer. Figure 1-1 shows the wiring pin side of module connectors within each of the three main sections of the LINC-8 Computer. Each section contains eight vertical rows of connectors identified by the letters A, B, C, D, E, F, H, and J, from right to left. The prefix M (memory), L (LINC), or P (processor) further specifies one of three major logic segments (top, middle, bottom).

Each vertical row within a section contains 40 module connectors numbered 1 through 40 from top to bottom. Modules are referenced in this manual by using a letter-number code to specify the section, row, and slot in which that module is located. As an example, the designation MH12 specifies a memory section module located in slot 12 or row H. The designation LD04 refers to a module in slot 4, row D, of the LINC section.

Module connector locations within the data terminal panel are also specified through use of a similar coordinate system. Figure 1-2 shows the wiring pin side of module connectors located behind the panel. Vertical row A is on the right and row B is on the left. Module connectors are numbered from 1 through 36, top to bottom in each row. The designation B29, for example, specifies a module located in slot 29 of row B.

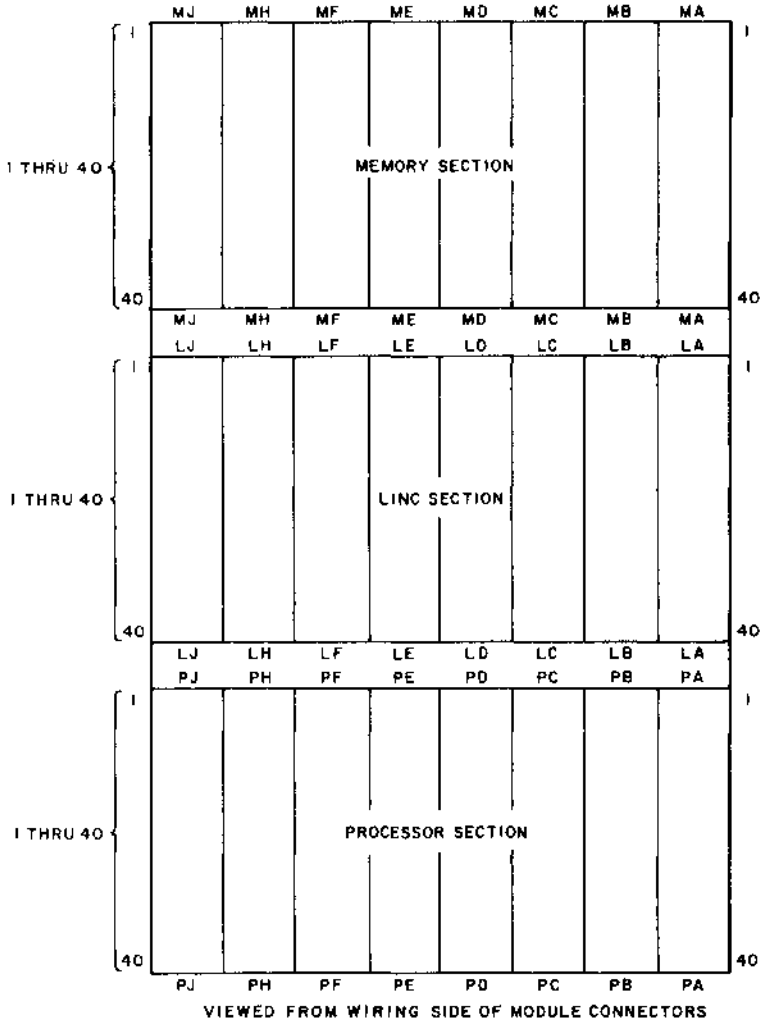


Figure 1-1 Linc-8 Module Connector Designations

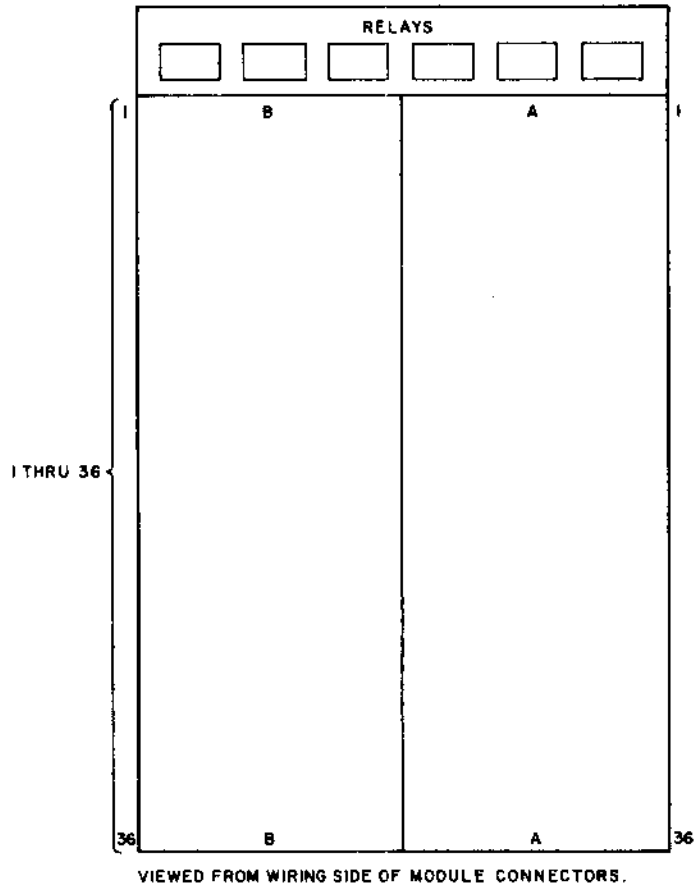


Figure 1-2 Data Terminal Panel Module Connector Designations

1.5 PACKING AND MOVING

The LINC-8 system is a carefully designed piece of high quality electronic equipment. It is rugged and capable of being moved; however, certain procedures should be observed to insure the maximum safety of the system.

When the system is delivered there are several shipping brackets that should be saved for future use. The nylon wedge, which supports the bottom corner of the logic panel, should be replaced any time the system is moved a substantial distance. The two brackets that bolt the logic panel to the LINC-8 frame should be installed when moving. The tape transport electronics section should be supported by placing a block between the tape and the top of the scope. Any shipping bolts in additional cabinets, or peripheral items, should be replaced.

If the above cautions are observed, and reasonable care is exercised, no substantial problems should be encountered when moving the LINC-8.

CHAPTER 2

PROGOFOP
(PROGram OF OPeration)

2.1 INTRODUCTION

The following description applies to PROGOFOP Version II, as supplied through August 1967. Subsequent versions of PROGOFOP may be altered in some detail; therefore, the reader should refer to descriptive material supplied with the current version of the program for specific programming details.

PROGOFOP is a program which occupies the bottom quarter of LINC-8 memory. It serves the function of executing commands generated by the operation of LINC console switches (left side of the console), execution of LINC operate class (500) instructions, LINC execute class instructions (740), and LINC MAGtape (MTP, 700) instructions. In addition, PROGOFOP handles the defined PDP-8 program interrupt devices which include the teletype keyboard and printer as well as any specially defined interrupt devices unique to a particular LINC-8 system. PROGOFOP starts the LINC processor, answers any system interrupt requests, and handles any of the above defined LINC instructions which are not executed by the LINC processor itself. The program consists of a number of subroutines which handle various devices and/or functions. For a complete description of PROGOFOP and its details of operations, the user is referred to DEC document number DEC-L8-SFA0-D. A brief description of some subroutines and features of PROGOFOP follows.

2.2 INTERRUPTS SERVICE AND OPERATIONS PRIORITIES

The key to determining PROGOFOP priorities of operation is contained in its basic interrupt service programming. Whenever any external interrupt device or request to execute a PDP-8 program, or request for action from a console switch occurs, control is transferred to PROGOFOP through the PROCESS routine.

The first action initiated is that of checking the LINC interrupt flip-flops to see if a console switch interrupt occurred. If this is the case, then a check is made to determine if the STOP switch was depressed. Operation of the STOP switch initiates the PRESET condition. This means that all previous information in PROGOFOP is to be preset and a PWR CLR pulse is generated in the LINC section, thereby clearing the state of the LINC section to a preset condition.

If a console switch other than the STOP switch was operated, a further check is made to be sure that neither a MAGtape request nor a LINC program execution request (OPR, EXC, MTP) was made. If none of these conditions exist, the status of the E STOP, F STOP, and EXAMINE STEP switches is checked. If any of these switches are pressed, the appropriate execution is carried out. At this point, the PROGOFOP internal flags are checked to see if the LINC is in either a MAGTAPE or OPERATE

PAUSE (waiting for either more information from the tape control, or for a key to be pressed on the keyboard). If PROGOFOP is currently in a MAGTAPE or OPERATE PAUSE, no further console switches are checked and the requesting console switch is ignored. This means that any other switch function are of a lower priority than a MAGTAPE or OPERATE PAUSE. If the program is not in a MAGTAPE or an OPERATE PAUSE, the request for the console switch operation is carried out.

Assuming that no console switch function has been requested, the interrupt service routine then proceeds to check for a MAGtape interrupt; a request for the PDP-8 execution of a LINC instruction; the state of the match, or instruction by instruction interrupt flip-flop; and then a check of the auto restart delay. Each of these functions is checked in turn, and the appropriate action taken if it is found. After the above items are checked, the user-defined interrupts are checked. There are provisions in the program for the user to insert a special interrupt service routine to check for interrupts that are particular to a given LINC-8 system, or to a given set of either hardware or software conditions. On returning from the special user-defined interrupts, the teletype keyboard and printer flags are checked. After PROGOFOP has taken the appropriate action, the program then either starts the LINC or merely turns the interrupt system back on, depending on the requirement. There are several entry points to this restarting. The entry point RESTART will start the LINC running again if it had been running when it was called to handle the interrupt just processed. The entry point GO will start the LINC regardless of whether or not it had been running previously. RENINT is an entry point to re-enable the interrupt and not start the LINC at all. The entry point AUTO checks the state of AUTO-RESTART flip-flop, and if it is in the 1-state, triggers the restart delay and waits for the timing out of the restart delay. The entry point DELRST is where the program restarts the LINC upon completion of the timing out of the restart delay.

2.3 EXECUTING A LINC INSTRUCTION (THE DO FUNCTION)

The DO switch utilizes a considerable amount of PROGOFOP and illustrates some of its functions. Assuming that the LINC is stopped and the DO switch is lifted, the contents of LINC locations 20 and 21 are saved in PROGOFOP internal registers. The contents of the left and right switches are then placed in LINC locations 20 and 21, respectively. The contents of the LINC program counter are stored and the number 20 is placed in the LINC P-register. The program indicator TOGIN (toggle function indicator) is set to 7777; the LINC IBI (instruction-by-instruction) flip-flop is set; and the LINC is started (at LINC location 20). If the function specified by the switches is a LINC processor instruction, the LINC starts and executes one instruction, and then control is transferred back to PROGOFOP. At this time, PROGOFOP resets the contents of the LINC program counter; resets LINC location 20 and 21; clears the IBI flip-flop and returns to await another program interrupt request.

Alternatively, if the instruction requested calls for PROGOFOP execution, the appropriate actions in PROGOFOP take place. When this is the case, the TOGIND (toggle function indicator) register serves as a program flag to PROGOFOP to indicate that this was a function executed by the DO switch. This means that if the instruction is a MAGtape instruction, PROGOFOP resets the contents of LINC location 20 and 21 before actually carrying out the MAGtape transfer which could be a write tape instruction.

2.4 LINC ADDRESS USAGE

PROGOFOP utilizes the contents of the LINC Memory Bank Selection Registers to determine where in memory it must go to find the contents of selected LINC addresses. The subroutine RMEXT (reset memory extension indicators) sets up the necessary address pointers for PROGOFOP. The subroutines READ and WRITE then go to these addresses and either read or write information to or from the LINC portion of memory.

2.5 LINC FLIP-FLOP REGISTER

There are a number of flip-flops in the LINC subsystem under direct control of PROGOFOP including the IBI, E STOP, F STOP, AUTO RESTART, extended tape units, MARK flip-flop, and so forth. These flip-flops are controlled by two subroutines; SETFF and CLFF which, respectively, set and clear appropriate bits of the flip-flop register. To set a particular bit of the flip-flop register without clearing whatever other bits may be set, a 1 is put in the appropriate bit of the PDP-8 accumulator and a JMS to the SETFF subroutine is given. To clear a desired bit of the flip-flop register without affecting the other bits, a 1 is placed in the desired bit of the PDP-8 accumulator, and a JMS to the CLFF subroutine is given.

2.6 TELETYPE OPERATION

PROGOFOP uses the teletype keyboard as an input to the LINC-8 System. The keyboard is read-in and the ASCII code converted to the appropriate LINC code by a table look-up procedure. The character equivalence table is given in the LINC-8 Users Handbook. For selection of upper case LINC characters, PROGOFOP gives both the upper case code and then the actual character code to the LINC. When a character is typed into the LINC system, it is read-in by PROGOFOP and the keyboard flag is cleared; however, the ASCII equivalent is not typed back until the LINC processor has completely accepted the code. This means acceptance of both the upper case code and the character code for upper case LINC characters.

PROGOFOP communicates the existence of a keyboard character by setting the KST flip-flop in the LINC section. When characters are typed out from the LINC processor by the instruction TYP (514), PROGOFOP first checks to see that a character is not currently being typed on the teleprinter. If the teleprinter is free, the character is placed in the teleprinter buffer and the PROGOFOP register PRINT is set to a non-zero value to indicate that the character is currently being printed by the teleprinter. Control is then transferred to the LINC section. If the teleprinter is busy, PROGOFOP waits with the interrupt off until the teleprinter is free. The program then prints the character and returns to the LINC section, again with the interrupt on.

2.7 MAGTAPE ROUTINES

The MAGtape instruction is one of the EXC (execute) class instructions; it is trapped by the LINC-8 hardware with control transferred to PROGOFOP. At EXCGO, PROGOFOP saves the value of the current LINC instruction being executed by reading this instruction from the LINC B-Register and storing it in PROGOFOP register LINSTR. After performing functions which depend on whether or not the LINC processor is in the instruction-by-instruction mode, control is transferred to the routine MTPGO.

Here, PROGOFOP goes to the address designated by the LINC P-register and gets the second word of the MAGtape instruction. This is then stored in location QNBN (quarter number, block number). The LINC program counter is advanced by 1 and various PROGOFOP program flags are preset. A check is then made to ascertain whether this tape instruction is the result of a programming sequence from the LINC, or is the result of a DO toggle operation from the console. In the latter case, certain LINC memory locations must be reset.

The next segment of programming is the SEARCH routine. Here, the MAGtape control is placed in the SEARCH mode, and the status of the tape motion is checked. If the tape is currently in motion, it is left in motion. If the tape is not in motion, it is set in the forward direction. At location CKTYPE, the MAGtape instruction is used to dispatch to the various tape routines. The routines GROUP and NONGRP are the group and non-group set-up routines, respectively. These set the LINC addresses for the tape transfers.

Finally, the tape dispatch will take the flow of operation to one of three routines, RDTAPE, WTAPE, or MTBOPR. RDTAPE is the routine which reads a block of tape. The block may be read either into memory (during the RDC, RCG, and RDE instructions) or may be read for the purpose of computing a checksum (during the WRC, WRG, and CHK instructions). The WTAPE routine transfers data from some segment of memory to a block on tape, and it is entered by either a WRC or WRG instruction. The MTBOPR routine is entered only during the MAGtape instruction MTB (move toward block).

2.7.1 RDTAPE (Read Tape Routine)

The TPWAIT subroutine transfers control back to the interrupt enable routine and leaves the LINC with the interrupt on. This routine is used to wait for the next interrupt in the MAGtape control. At the beginning of the RDTAPE routine, the tape is in search mode, and the interrupts occur once during every block (approximately 40 milliseconds). The interrupt wait routine also has a built-in time delay check. If a MAGtape instruction is in progress (MTOPIN contains 4000) and if no tape interrupt occurs within one second, then control is transferred back to the beginning of the tape instruction to reexecute the entire instruction. The assumption here is that, for some reason, tape motion was stopped and the instruction was not executed correctly.

On reentering the read tape routine from TPWAIT, the current block number where the tape is located will be contained in the LINC A-register. The routine BLKCK (block check) checks for the correct block number (contained in the location DESIRED) and for the correct motion. If the correct block number and a FWD motion are not found, control is transferred to the routine SETMTN (set motion) which resets the tape motion as specified by the block number, direction, and desired block. If the correct block number and motion are found, the tape control is put in the block mode.

The next tape wait passes over the guard word. A check is then made to determine whether the tape reading is for the purpose of storing in memory, or simply for forming a checksum. If data is to go to memory, 7777 is put in the register DOMEM, otherwise, DOMEM is cleared. Control is transferred to TPWAIT to wait for the first data word. Then, the first data word is read from the A-register and stored in memory, if DOMEM equals 7777. The data word is added to the checksum and the word counter decremented. Control then transfers to TPWAIT to wait for the next word. After all words are read in, then one more TPWAIT gets the checksum word. This checksum word is added to DATASUM and this checksum is put in the register DATASUM. The block mode is turned off and additional checks are made to determine whether or not the checksum is correct (7777), and whether this is a group instruction or an individual block instruction. Depending upon the above conditions, control is either transferred back to the beginning of the tape routines (in the case of checksum error), the beginning of the read routine (in the case of group instructions requiring more data), or the checksum is placed in the LINC A-register and control is transferred to FINMTN (final motion).

In the routine FINMTN, the i bit of the LINC tape instruction determines whether the tape is to be left in its current motion, or whether it is to be placed in the turn-around state. If the i bit = 1, tape is left in its current motion. Control is then transferred back to the LINC mode, or the interrupt wait loop of PROGOFOP, depending upon whether the instruction was part of a LINC coding sequence or the result of a DO switch function.

2.7.2 WTAPE (Write Tape Routine)

The write tape routine is similar to the read tape routine except that, in the case of writing, the data word must be placed in the LINC B-register prior to the disassembly of that word onto tape. Therefore, the transfers occur one word ahead of where they would during a read routine. The same TPWAIT, BLKCK, and SETMTN routines are used during the writing of tape. At the end of the WTAPE routine, control is transferred either to the RDTAPE (read tape) routine in the case of WRC, to the beginning of the tape instruction in the case of the end of a WRG instruction, to the WTAPE routine in the case of an incompleted WRG instruction, or returned to the LINC in the case of a WRI instruction.

2.7.3 MTBOPR (Move Toward Block Routine)

The move toward block routine is entered with the tape in the search mode, and in motion. One block number is read, the search mode is turned off, and motion is set according to where the desired block is with respect to the current block. Transfer is then returned to the LINC through the FINMTN routine.

CHAPTER 3
FUNCTIONAL LOGIC DESCRIPTION

3.1 GENERAL INFORMATION

This chapter contains detailed functional descriptions of each logic element comprising the LINC subsystem of the LINC-8 computer. Also described are modifications to the PDP-8 which are necessary for LINC operation. For ease of reference, certain section headings in this chapter also include the related engineering drawing number. Standard PDP-8 operations and functional descriptions are found in the PDP-8 Maintenance Manual, F-87. Since the majority of LINC logic operations relate to specific LINC instructions, the reader should refer to the appropriate instruction timing diagram descriptions in Chapter 4 when these instructions are called out in this chapter.

3.2 LINC/PDP-8 INTERFACE

The LINC/PDP-8 interface consists of logic circuits which transfer control and provide the necessary synchronization between the LINC processor and the PDP-8 processor. The LINC subsystem can be considered an I/O device of the PDP-8 computer. The PDP-8 is held in its break cycle mode and continuously generates time pulses T1 and MD (memory done) which control LINC functions. A special group of PDP-8 IOT instructions are provided for direct control of the LINC subsystem. Once PROGOFOP is in PDP-8 memory and the PDP-8 relinquishes control to the LINC through IOT instructions, the LINC-8 is capable of executing LINC programs. Upon completion of these programs, the LINC subsystem can return control to the PDP-8 through use of the OPR (operate), EXC (execute), or MTP (magnetic tape) class of instructions; the HLT (halt) instruction; or through an external program interrupt request or a data break request. A detailed explanation of LINC/PDP-8 intercommunication is presented in Chapter 7 of the LINC-8 Users Handbook.

3.2.1 IOT Decoding and Control (L17)

The circuits that decode PDP-8 IOT instructions for the LINC are shown on drawing L17. Basically, IOP1 is received from the PDP-8 to generate LINC control pulses 8L1, 8L2, and 8L3. Time pulse 8L1 is designated 0 ⟶ B(A) and is generated by the R603 Pulse Amplifier in location LJ06 if bit BMB07 is 1. Buffered MB and AC bits are shown on the left of drawing L17. BAC and BMB bits, along with time pulse 8L2 enable the instruction decoders shown on the upper right of drawing L17. Additional functions controlled by 8L2 and 8L3 are shown on the lower right drawing L20.

A tabular summary of PDP-8 IOT instructions for the LINC subsystem is presented on the lower right of drawing L17. The larger table to the left summarizes all of the PDP-8 IOT instructions

for the LINC, while the smaller table on the right is concerned only with IOT 141. As an example of table usage, consider IOT instruction 141. The complete designation of this IOT is 6141 (ICON). When ICON is executed, the number 6 is decoded by the PDP-8 instruction register to specify an IOT instruction. The remainder of the IOT instruction (141) is contained in PDP-8 MB bits 3 through 11. The configuration of these bits is shown alongside 141 in the larger table. Since BMB07 is 0, the pulse 0 ⟶ B(A) is not generated; therefore, no action occurs at 8L1 time.

At 8L2, the LINC-8 is instructed to perform the LINC function specified by the rightmost four bits of the PDP-8 AC register. The particular action occurring at 8L2 is indicated by the right-hand table. For example, if AC bits 8, 9, 10, and 11 contain 0000 when ICON is issued, the pulse 0 ⟶ MOTN is generated. If they contain 0010, SELECTL is produced. BAC bits are decoded by the circuits shown on the upper right to produce the various functions. Nothing of significance occurs at 8L3 during an ICON instruction.

As a second example of table usage, assume that the PDP-8 IOT instruction 6163 (IACS) is issued. Looking at the IOT CODE column of the table, it can be seen that 163 appears in MB bits 3 through 11 as 001 110 011. At 8L1, since BMB07 is 1, the signal 0 ⟶ B(A) is generated clearing the B-register. At 8L2, the contents of the PDP-8 AC go into the B-register. At 8L3, the contents of the B-register are jam-transferred into the S-register and then B is cleared. IOT 163 has the overall effect of placing the contents of the AC into the S-register and clearing the B-register.

3.2.2 LINC Inputs to PDP-8 Accumulator (L7)

A total of twelve R141 modules transfer information from the LINC processor into the PDP-8 accumulator. Each R141 contains seven 2-input AND gates and the twelve modules produce ground-level output signals (input mixer bits IM00 through IM11) which set specific PDP-8 accumulator bits. All seven 2-input AND gates on each R141 are used to transfer the following information into the PDP-8 accumulator: contents of the B-register; settings of the left switches; interrupt status; settings of console switches 1 and 2; the status of the upper and lower memory bank selectors; and special tape-mark-window and decoding information used for maintenance purposes.

To further explain PDP-8 input gate operation, consider the third gate in from the left on drawing L7 as an example. The output of this gate is designated IM02 (generated at terminal LC31D) and is used to set PDP-8 accumulator bit AC2. One pair of input conditions that produce IM02 is the coincidence of B02(1) and B ⟶ AC. B02(1) comes in to terminal LC31E and B ⟶ AC arrives at terminal LC31F. The F-terminals of all R141 Diode Gates are connected in common and receive the PDP-8 IOT signal B ⟶ AC. Another set of conditions that produce IM02 is the coincidence of UMB00(1) and MEMBK ⟶ AC. IOT signal MEMBK ⟶ AC is applied to terminal T of each R141 gate. Terminals F, J, L, N, R, T, and V are connected in common to all R141 Diode Gates.

3.2.3 LINC Interface Control (L16)

Drawing L16 shows most of the flip-flops used to communicate status between the LINC and the PDP-8, the synchronization for starting and stopping the LINC processor, data break, and program interrupt requests. This drawing also shows the address selection between LINC and PDP-8 address registers, LINC synchronization for external data break requests and interrupts from both the LINC section and external devices.

The flip-flops CLEAR, IBI, FSTOP, ESTOP, AUTO, and KST (drawing L16) as well as MARK, UNIT 1, and UNIT 2 (drawings M10 and M13) are set by PDP-8 program control and in some cases control the LINC processor's operation. In addition, the flip-flops TAPE INT, IBI OR MATCH INT, 8 EXC INT, LCONSL INT, LINC INT, EXT INT, and RUN INT are used to signal various status conditions to the PDP-8 so that PROGOFOP can control the LINC properly.

The LSEL flip-flop allows the LINC section to be disconnected from the I/O interface. The LBRK flip-flop requests a PDP-8 data break cycle. The LRUN flip-flop indicates that the LINC is running. The flip-flop MEM WRITE specifies the direction of data being written into or read out of the LINC-8 memory. The EXT BRK flip-flop is used to synchronize the LINC with requests for data breaks from external devices.

The R303 Delay (AUTO-RESTART DLY) is used to time out the delay for automatic restarting after either a stop in the instruction-by-instruction mode or because of an address match in either the F-stop or E-stop mode. The LINC console switches are ORed together and brought into the input of a W501 Schmitt Trigger in LB37. The output of this Schmitt trigger sets the LCONSL INT flip-flop. In addition, if the switch being pressed is the load switch, the output of the W501 will also cause a LOAD PLS to be generated.

The level INTL in the lower right of drawing L16 sets the LINC INT flip-flop to request a program interrupt from the PDP-8. The HOLD level stops the LINC during an EXC class instruction, an external LINC interrupt (such as console switches), or an external program interrupt request and signals PROGOFOP. It is gated against the pulse GNI (get next instruction) to zero the LBRK flip-flop, thus stopping the LINC. The GO pulse generated in the bottom center of drawing L16 starts the LINC processor. The PWR CLR pulse shown in the top center of drawing L16 is generated by the PDP-8 IOT instruction DESELECT L, or by a PDP-8 PWR CLR pulse which inturn is generated by either power turnon, or a PDP-8 Key start. The PWR CLR pulse clears various states and flip-flops in the LINC section and sets the LINC processor to a known PRESET state.

3.2.4 Memory Addressing (M8)

The PDP-8 memory is shared by both the PDP-8 and LINC and can be addressed by either of two registers in the LINC-8 computer. In the PDP-8 mode of operation, core memory is addressed by

the MA register as described in the PDP-8 Maintenance Manual. In the LINC mode, memory is addressed by the LINC S-register. Address gating for both registers is shown on drawing M8. The particular register selected is determined by the signals 8 ADDRESS and LINC ADDRESS which are the outputs of the ADDRESS SELECT flip-flop shown on drawing L16.

In the LINC mode of operation, the 4096-word memory is subdivided into four memory banks (0, 1, 2, and 3) of 1024_{10} words each ($0\text{-}1777_8$). Therefore, only 10 bits are required to address any location within one of these banks. S-register bits S02 through S11 perform this addressing function. These bits produce addressing signals GMA02 through GMA11 (drawing M8) which go to the PDP-8 memory. Address bits GMA00 and GMA01 select bank 1, 2, or 3. Memory bank 0 is not available in LINC mode, since it stores PROGOFOP. GMA00 and GMA01 are developed by circuits shown on drawing L26 according to the contents of S-register bit S01 and the contents of the LINC LMB and UMB registers.

3.2.4.1 Memory Extension (L26) - Drawing L26 shows the UMB (upper memory bank) and LMB (lower memory bank) selectors which specify where in the potential 32,768 words of memory the upper and lower 1024 words addressed by the LINC order code are pointing. Signals GMA00 and GMA01, shown at the top, combine with GMA02 through GMA11 (drawing M8) to address any location in the standard 4096-word PDP-8 memory. The EXTEND ADDRESS signals at the upper left of drawing L26 allow addressing of extended memory up to the maximum 32,768 words subdivided into 32 banks of 1024 words each. Some modules are not installed unless the system contains extended memory.

In the LINC mode of operation, the particular memory bank selected is determined by the contents of the LMB register, UMB register, and S-register bit S01. If S01 is 0, the LMB register selects the memory bank. If S01 is 1, the UMB register specifies the memory bank. In normal operation using a 4096-word memory, memory bank 2 is selected as the LMB and bank 3 is the UMB. When the LINC-8 Computer is turned on, a PWR CLR pulse from the PDP-8 enables RESET MEMORY (lower right, drawing L26) which sets the LMB register to 00010, to designate memory bank 2 as the lower memory bank, and also sets the UMB register to 00011, thereby selecting memory bank 3 as the upper memory bank.

LINC instructions LMB and UMB allow the user to change the contents of the LMB and UMB registers. In this way, any two 1024-word banks can be selected as the lower and upper memory banks. The upper memory bank is loaded directly from the C-register. The lower memory bank is loaded from the 5-bit LMB setup register, which in turn is loaded during the LMB instruction. Its contents are then transferred to the LMB register at time pulse T2 of the next JMP instruction. Gating is shown for extended addresses and for the two most-significant bits of the memory address. The level DISABLE MEM CHANGE provides for the non-operation of either LMB or UMB instructions if a memory bank is requested that does not exist in the machine, or if memory bank 0 is requested (this is the memory area used by PROGOFOP).

3.2.5 External Data Break (P23)

The external connections to the data break system for use by external devices, such as IBM compatible tape systems or user's special interfaces, are functionally identical to those connections provided for the PDP-8. A detailed description concerning the functional and timing characteristics of the data break system is found in the PDP-8 section of the Small Computer Handbook. The actual pin locations which connect to the data break system are described in the Interface and Installation chapter of the LINC-8 section of the Small Computer Handbook, C-800.

When an external device requests a data break cycle (either single- or three-cycle) from the LINC-8 system, that data break cycle will be granted either at the end of the currently executed instruction, or at the end of the next instruction. The external data break cycle will be at the end of the current instruction, unless the data break request comes up after the last BT1 pulse of the currently executed instruction. This means that a data break cycle will be granted during the execution of either PDP-8 or LINC mode programming. The considerations of executing a data break cycle from a LINC mode instruction as opposed to a PDP-8 mode instruction are identical. The only point worth noting is that some of the LINC instructions (DSC and MUL) are quite long. Therefore, it could take as long as 150 μs to answer a data break request if the LINC were doing a DSC instruction.

Because the LINC section of the LINC-8 system also uses the data break, the system is provided with the equivalent of a two-channel data break multiplexer. This allows either the LINC section or some external device to request data breaks from the basic PDP-8 system. The LINC section is of the lower priority, and therefore any external data break requests will take precedence over the LINC sections operations.

The logic associated with answering external data breaks is shown on drawings P23 and L16. An external data break request comes in to the LINC-8 through connector PJ04K. This request is then transferred to the LINC section where it sets the EXT BRK (external break) flip-flop shown in the upper left-hand corner of drawing L16. This indicates that an external break request is present and should be serviced. The EXT BRK flip-flop prevents the next LINC instruction from occurring by disabling the ENABLE GO level (bottom center, drawing L16). In addition, the fact that the external break request is on and the LINC is not running, generates the ENABLE PDP-8 signal, and disables the ENABLE LINC signal. These signals are used in conjunction with the ENABLE 8 ADDRESS signal to switch the address selection back to the PDP-8 and to connect the external data bits input lines to the PDP-8 MB data-bits input gates (drawing P23). The R123 gates shown on drawing P23 allow either the LINC B-register bits or the external data-bits inputs to be connected to the PDP-8 data-bits signal lines.

To provide adequate synchronization for external data break requests, several other signals are modified in the PDP-8. The ADDRESS ACCEPTED signal is gated with ENABLE PDP-8 to generate GATED ADDRESS ACCEPTED (drawing P23). This signal goes to the input/output system and will only

be generated when an external data-break request is being answered. Similarly, the BREAK OUTPUT, and CYCLE SELECT signals are disabled in the PDP-8 to prevent LINC-requested data break cycles from interfering with external devices. BREAK OUTPUT and CYCLE SELECT are disabled whenever the LINC is enabled. The R302 Delay (pin PH05M, drawing P25) is used to extend the B (break) signal of the input/output interface (drawing P110) for the entire break cycle as the ENABLE LINC signal is again true at T1 of the last external break cycle. Finally, the DATA IN signal from external devices is gated with ENABLE PDP-8 to prevent external data-direction signals from interfering with the correct operation of the LINC section.

3.2.6 MB Register Modifications (P25)

Since data indexing and address modification computations are carried on simultaneously in both the LINC B-register and the PDP-8 MB register, certain modifications to the MB register are necessary to enable it to function as a 10-bit counter, compatible with the characteristics of LINC mode indexing. These modifications, which are shown both on LINC drawing P25 and on MB Register Control, Drawing P105, allow the MB register to count during certain LINC instructions (iβ class, hβ class, DIS, and XSK instructions).

The first change is the signal MB11 COMP-ENABLE. This signal comes from the LINC section and allows the least-significant bit of the MB register to be complemented whenever the COUNT MB pulse is generated, except conditionally during half-word address indexing calculations. The logic for the signal MB11 COMP ENABLE is shown on drawing L18. The signal LOW ORDER MB COUNT ENABLE (drawing P25) which enables the S181 DC Carry Gate (location PD19) functions in a similar manner as MB11 COMP ENABLE, and conditionally disables counting functions during half-word indexing. When the LINC is running, the high order S181 DC Carry Gate (PC19) is disabled by the inverter in PH10 (pins J and K) shown on drawing P105. With this high-order DC carry gate disabled, the carry-gate functions necessary for complementing MB0, MB2, and MB3 are provided by the R121 located in PH11 (drawing P105) when the LINC processor is running.

3.3 LINC LOGIC DESCRIPTION

This section describes the various LINC registers, register control circuits, timing functions, and other functions which synchronize LINC operations. As stated previously, the user will gain a more thorough understanding of the LINC-8 computer if he relates these logic descriptions to the specific LINC instructions explained in Chapter 4 when these instructions are referenced in this section.

3.3.1 Timing and Control (L15)

LINC subsystem timing pulses are generated by the time pulse distributor shown on drawing L15. Distributor operation is controlled by PDP-8 timing pulses BT1 (buffered T1) and MEM DONE. BT1 is inverted (BTP1) and gated with LRUN(1) to initiate RTP (run time pulse). MEM DONE is also gated with LRUN(1) to initiate RTP. In addition to the gating functions, MEM DONE generates B MEM DONE to produce TLAST if the LAST TIME flip-flop is in the 1-state. LRUN(1) indicates that the LINC subsystem of the LINC-8 computer is in operation.

Flip-flops T00, T01, T02, and T03 form a 4-bit counter, initially set to 0001 by the GO pulse. In the LINC mode, LRUN(1) conditions the enable level inputs of the DCD gates of these flip-flops. The counter is advanced by RTP at the DCD complement gates of T03. During certain instructions, the flip-flops are jammed to either a count of 1000 (10_8) or 0100 (04_8) through collector triggering by the R001 and R002 gates shown above the 4-bit counter.

Outputs of T00 through T03 are delayed through two stages of inversion (upper left, drawing L15) and then go to the R151 Binary-To-Octal Decoders at LH26 and LH27. Capacitors connected to the output of these inverters slow down the output fall so that the signals on the inputs to the R151 decoders do not change when a pulse appears at input terminal D. The pulses applied to input terminal D are very critical in width; they should be adjusted to 170 ns (± 30 ns) for reliable operation with wide marginal capabilities. Positive time pulses T1 through T15 are inverted by S107 inverters since both positive and negative pulses are required throughout the LINC processor to control various functions. Time pulses T11 and T12 are used extensively, and are therefore buffered through R603 Pulse Amplifiers in location LH31 shown in the bottom left of drawing L15.

3.3.2 Control Pulse Gating (L20)

LINC control functions that occur during specific time pulses are shown on drawing L20. Each of the time pulses T1 through T17 is applied as an enabling level to a group of NAND gates which generate the required control signals depending on the particular instruction being executed. Additional gating for the functions occurring at time pulses T2 and T3 of the MSC class of instructions is shown on the upper right. Time pulses 8L2 and 8L3 (lower right) provide control during PDP-8 IOT instructions used to communicate between the PDP-8 and LINC processors.

3.3.3 Instruction Control (C) Register (L14)

The 12-bit C-register holds the instruction currently being executed by the LINC-8. At the start of a particular instruction, the GO pulse directly clears flip-flops C00 through C07 and produces the pulse 0⟶N which clears flip-flops C08 through C11. GO also sets the MEM⟶C ENABLE

flip-flop shown above C00 and C01. The 1-state output at terminal T of this flip-flop conditions the level-input terminals of the DCD gates for C06 through C11 while the 1-state output at terminal S is inverted to enable C00 through C05.

Following these operations, the instruction is read out of PDP-8 memory into the B-register and into the C-register by the pulses 1 ⟶ B00 to 1 ⟶ B11 through gates previously conditioned by the MEM ⟶ C ENABLE flip-flop outputs. The C-register now contains the instruction to be executed and at time pulse T1, the MEM ⟶ C ENABLE flip-flop is cleared. The 0-state outputs disable any data from entering the C-register until the next GO pulse signifies the start of the next instruction.

3.3.3.1 C-Register Decoding - The decoders and gates shown on drawing L14 decode the binary outputs of the C-register and produce corresponding signals to indicate the particular instruction being executed. In the upper left-hand corner of the drawing, bits C00 and C01 are decoded to select either the full-address class instructions (ADD, JMP, STC) or subgroup (SBGRP). Bits C02 and C03 then combine with SBGRP to select either subgroup 0, 1, 2, or 3. Each subgroup, along with bits C02 through C06, is further decoded by R151 decoders for the remaining 32 LINC instructions. In many cases a negative level is also required for these LINC instructions. The S107 inverters shown on the drawing provide these levels.

3.3.3.2 N-Counter - During the instructions DIS, DSC, MUL, and SAM, bits C08 through C11 function as a 4-bit down counter (N-counter) to tally certain repetitive loop operations occurring within each of these instructions. When the N-counter indicates that the specified number of operations has taken place, the LINC-8 is directed to execute the next instruction in its program sequence. In the execution of instructions ROL, ROR, and SCR, the right four bits of the C-register function as a step counter. The contents of these four flip-flops are designated N. For each shift operation, the value N is decremented by 1 until N is equal to 0000, at which point the instruction is completed.

At the start of either DIS, DSC, or MUL, the C-register contains addressing information. It also specifies channel selection for the instruction SAM. When this information is no longer required, the N-counter is cleared by the pulse 0 ⟶ N (drawing L20). Following this clearing operation, the N-counter is set up for operation by the N COUNT ENABLE level starting at T10 and remaining enabled throughout the remainder of the instruction. Each time a repeat operation takes place, the pulse N-1 ⟶ N causes the N-counter to decrement by 1. Following the signal 0 ⟶ N, the first N-1 ⟶ N pulse sets the N-counter to 17_8 (1111_2). Succeeding N-1 ⟶ N pulses set N to 16_8 (1110_2), 15, 14, etc., until the correct number of repeat operations have occurred. Outputs of the N-counter are decoded by the R151 Binary-To-Octal Decoders shown above flip-flops C08 through C11 on drawing L14.

3.3.4 Control Functions (L18)

The majority of control functions for the LINC subsystem are shown on this drawing. Instructions are gated with various levels and signals to generate additional control functions. These will then be gated with time pulses to provide the necessary control for the LINC processor.

Control functions presented on drawing L18 can be typified by the R121 NAND gate shown at the upper left. This module contains four gates. Terminals LE30E, LE30F, and LE30D are associated with the top gate which is not presently used. The second gate produces the −3V output signal LDA V LDH whenever the LINC is executing the instruction LDA or LDH. The −3V HB signal comes up whenever the half-word instruction STH, SHD, or LDH is being performed. Finally, the −3V control signal SSSS is generated as an OR function initiated by either SRO, STA, STH, or SET.

3.3.5 Memory Address (S) Register (L3)

The LINC S-register operates in conjunction with the memory addressing gates and memory extension circuits to select specific 12-bit locations in the PDP-8 core memory. As stated in Section 3.2.4, S-register bits S02 through S11 directly produce memory addressing bits GMA02 through GMA11. S01 determines the state of bits GMA00 and GMA01 while S00 is not used for addressing, although it is used during half-word instructions and during MUL, DIS, and DSC for special operations. The S-register is shown on drawing L3 and the S-register control is on L21.

Flip-flops S00 through S07 are directly cleared by the signal 0 ⟶ S0-7 which is generated whenever the contents of the B-register are jam-transferred into the P-register. It is also generated when the LINC is not performing the ADD or STC instructions and β is read into S-register bits S08, S09, S10, and S11 from flip-flops C08, C09, C10, and C11, respectively. At T2 of the JMP instruction, the signal P ⤑ B directly clears S08 through S11 and also generates 0 ⟶ S0-7 to effectively clear all 12 bits of the S-register.

S11 is set to 1 and S00 through S10 are cleared by the signal 1 ⟶ S which is generated during the DSC instruction to locate the horizontal coordinate of the character to be displayed on the oscilloscope. All twelve P-register bits are jam-transferred into the S-register by P ⤑ S, and since P00 and P01 are permanently held in the 0-state, S00 and S01 are cleared. In the case of B ⤑ S, all twelve B-register bits are jam-transferred into corresponding S-register bits.

When executing the full-address instructions ADD or STC, the signal X ⤑ S jam-transfers C-register bits C02 through C11 into S02 through S11, respectively. These 10 bits specify the address of the operand. S00 and S01 remain cleared. During iβ- or hβ-class instructions, the signal BETA ⤑ S jam-transfers C-register bits C08 through C11 into S08 through S11. Beta ⤑ S also initiates the signal 0 ⟶ S0-7 to clear S00 through S07.

3.3.6 Buffer (B) Register (L2)

The 12-bit B-register is comprised of double-height R211 modules and is primarily used to buffer information from the memory sense amplifiers into the LINC subsystem. Control for the B-register is shown on drawing L22. Many B-register functions are similar to those of the PDP-8 MB register described in the PDP-8 Maintenance Manual, F-87. B-register functions are described below.

3.3.6.1 B-Register to Memory Transfer - Information in the LINC B-register is written into memory through the PDP-8 MB register (drawing P105) and the data break input gates (drawing P23). In the LINC mode of operation, the signal ENABLE LINC from interface drawing L16 allows B-register bits B00(1) through B11(1) to generate the signals DATA BIT 00 through DATA BIT 11. These signals go directly into the PDP-8 MB register through DATA BIT connector PE04 (drawing P105). LINC B-register information is therefore written into memory through the PDP-8 MB register.

3.3.6.2 Memory to B-Register Transfer - Information read out of the memory sense amplifiers into the B-register is controlled by the two flip-flops shown on the lower right of drawing L22. The 1-state output of the SA ⟶ BLENABLE flip-flop allows sense amplifier data bits SA00 through SA05 to enter B-register flip-flops B00 through B05 respectively, while SA ⟶ BRENABLE gates SA06 through SA11 into B06 through B11. Together, the 1-state outputs of both flip-flops effect the transfer of an entire 12-bit word from memory into the B-register. Output signals from the R603 Pulse Amplifiers which set the B-register flip-flops are designated 1 ⟶ B00 through 1 ⟶ B11 and are also used to set the C-register flip-flops (see drawing L14).

During time pulse T10 of the half-word instruction STH, only one of the SA ⟶ B flip-flops will remain in the 1-state. Thus either the right or the left six bits will be read into the corresponding half of the B-register. The half selected depends on the state of flip-flop B00 which holds the H-bit during the STH instruction.

3.3.6.3 AC to B Transfer - The AC ⟶ B pulse effects a 1s transfer of PDP-8 AC bits A01 through A11 into B-register bits B00 through B11, respectively.

3.3.6.4 A to B Transfer - Half-word transfers between the A- and B-registers are affected by the pulses AL ⟶ BL and AR ⟶ BR. When the AL ⟶ BL pulse is generated, the left six bits of the A-register (A00 through A05) are 1s transferred into the left six bits (B00 through B05) of the B-register. In a similar manner, the AR ⟶ BR pulse effects a 1s transfer of A06 through A11 into B06 through B11. Combined, these pulses transfer an entire 12-bit word from the A-register into the B-register.

3.3.6.5 P →B IOT Function - During time pulse 8L3 of certain IOT instructions, the level 8L3BEXP jam-transfers P-register bits P00 and P01 into B-register bits B00 and B01, respectively. Since P-register bits P00 and P01 are permanently in the 0-state, the signal 8L3BEXP merely clears B-register bits B00 and B01. 8L3BEXP also generates the signal P →B which jam-transfers P-register bits P02 through P11 into B02 through B11. Therefore, the overall effect of 8L3BEXP is to clear B00 and B01, jam-transfer P02 through P11 into B02 through B11, and also jam-transfer B00 through B11 into P00 through P11.

3.3.6.6 Rotate Function - Each bit of the B-register can be rotated right one place by the ground-level ROTB signal. ROTB is applied to the pulse input terminal of jam-transfer gates associated with each flip-flop. The level-input to each gate is received from the same side (0 or 1) of the previous flip-flop; thus, B00 is rotated into B01, B06 goes into B07, and B11 is rotated into B00.

3.3.6.7 B-Register Complementing and Counting - The 200-ns DCD complement gates (pins FH and FJ) provide the ability to complement specific B-register bits. The B COMP ENABLE level conditions all 12 complement gates so that pulse COMP B will complement the entire B-register (used during the MUL and BCL instructions).

The same complement gates allow the B-register to function as a counter. A DC carry chain similar to that used with the PDP-8 MB register provides enable levels which allow the B-register to be used as a 10-bit counter for address computations during the iβ-class instructions and for DIS and XSK counting operations.

For half-word address computations, the level hB connects the B-register as an 11-bit counter with B00 being the least-significant bit, B11 as the next least-significant bit, B10, and so forth, up to B02. B01 does not function in this counting operation. The contents of B00 following this counting (if i=1) is the h-bit and specifies which half of a word is selected for a half-word instruction. At T10 of a half-word instruction, the h-bit is transferred to the S-register and is contained in S00 after T10.

During the DSC instruction, the B-register is used to increment the horizontal coordinate of the character displayed. In this function, the complement gates are enabled to make the B-register a counter which counts by four every time the COMP B pulse is enabled. Bits B02 through B09 are used in this application.

3.3.6.8 SAM Instruction A-D Setup - When the LINC is executing the SAM instruction, the B-register is first cleared and then bit B03 is set to 1. The 1 in B03 selects A-register bit A03 for evaluation. After A03 is evaluated, the 1 in B03 is rotated into B04 which selects A04 for evaluation. The 1 originally in B03 is rotated into locations B04 through B11, thus selecting all A-register bits from A03 through A11 for evaluation in a successive approximation manner.

3.3.7 LINC A-Register (L4 and L5)

These two drawings show the left and right half of the LINC A-register. The A-register is the main arithmetic register of the LINC processor. It is comprised of R210 modules and functions in essentially the same fashion as the PDP-8 AC register. The control for the A-register is shown in drawing L22. The link bit, and each bit of the A-register consists of an R210 double height module. This module contains a single flip-flop and the various gates used to set, clear, and complement the particular bit.

The A-register is cleared by the signals A CLEAR 0-6 and A CLEAR 7-11. The A-register is set up to rotate to the right or to the left. In either case, the link bit may or may not be included. The gating to include or exclude the link from the rotating is shown on the left of drawing L4. The A-register is rotated or scaled to the right during the MUL, SCR or ROR instructions. Bit A11 is shifted into bit 0 of the Z-register and the Z-register is simultaneously shifted to the right. During the ZTA instruction, the A-register is shifted right after the Z⊣→A function. The Z-register may be directly loaded into the A-register by jam-transfer gates Z⊣→A.

A-register bits may also be cleared by the pulses BCLA 1-11 and BCLA 0. These functions clear a bit of the A-register if the corresponding bit of the B-register is 0. The relay register is loaded into the right 6-bits of the A-register by the pulse R ⟶A. A special set of gates is used for the A to D conversion. This consists of pins DP, CK, DV and DU. The DCD gate associated with pins DP and DU is used to set a bit of the A-register if the B-register bit one place to the left is on 1. The gates DP, CK and DV are used then to clear an A-register bit, if the corresponding B-register bit is 1 and the output of the A-D system comparator is negative. For a detailed discussion of the A to D conversion process, see the SAM instruction description in Chapter 4.

Input pin CM is a direct complement input; a negative pulse on this input will complement the associated A-register bit. The half-add and carry gating is used to add a number from the B-register to the number currently in the A-register. For a detailed description of this gating, see the PDP-8 Maintenance Manual.

During a DSC instruction, the ACARRY pulse and the DCD complement gate of flip-flop A09 allow the A-register to count by four. The level-input terminal of this DCD gate is held at ground by the output of the S107 Inverter shown on the lower left of drawing L5. Each time ACARRY is generated, bit A09 is complemented thereby incrementing the A-register contents by four.

The link bit is set during a LAM instruction by the pulse L CARRY and the signal A0 COUT (A00 carry out). The link bit may be cleared, complemented, and rotated to the right or left. Bit A00 can also be read into the link. The remaining gates on the link bit are not used.

During an ADD instruction, the carry-out of the A00 is connected around to the carry input of A11 as the signal END CARRY. This means that the sum of 7776 plus 0002 will equal 0001. This END AROUND CARRY is connected at all times except during the LAM and MUL instructions.

The FLOW flip-flop indicates an overflow during any of the four LINC add instructions. The FLOW flip-flop is set to 1 at ACARRY time if overflow occurs. Overflow occurs if the sum of two numbers, which are of identical sign, is of a different sign than that of the addends. This test is accomplished by the inequality of A0 COUT and A0 CIN at ACARRY time. An R613 generates the pulse which sets the FLOW flip-flop. The R613 is used because it has a fast (300 ns) DCD gate.

3.3.8 Program Counter (P) Register (L3)

In the LINC mode, the P-register specifies the lower memory bank address from which the next LINC instruction, data word, or address will be taken. A total of 12 flip-flops are shown comprising the P-register; however, P00 and P01 are not used. They are permanently held in the 0-state by the ground connection to their direct-clear terminals. Therefore, only ten P-register bits specify the location of the memory register containing the data to be operated on. These 10 bits are sufficient to address any location within the selected 1024_{10}-word lower memory bank. P-register counting is controlled by an R181 module (LH12) and two R121 modules (LD04 and LH11) all of which constitute a dc carry chain. Each carry chain output is applied to the level-input terminal of the DCD gate for a P-register flip-flop. The output level is enabled (ground) if all of the preceding P-register flip-flops are in the 1-state. The P+1 ⟶ P pulse will complement a flip-flop, if its associated DCD gate is enabled. Since the DCD gate of flip-flop P11 is permanently grounded, this flip-flop is complemented with each P+1 ⟶ P pulse. Thus, the value in the P-register is incremented by 1 each time the P+1 ⟶ P pulse is generated.

Two other P-register functions are shown on drawing L3. P02 through P11 are directly cleared by the pulse 0 ⟶ P, which clears all 12 P-register bits since P00 and P01 are permanently cleared. B-register bits B00 through B11 are jam-transferred into respective P-register flip-flops by the B ⤏ P pulse.

3.3.9 Relay (R) Register (L6)

The LINC-8 contains six DPDT relays that are available to control various external devices during a particular experiment. Each relay is energized or deenergized under program control by an associated R-register flip-flop. The 1-state outputs of the R-register flip-flops are inverted by R107 inverters to produce the −3V signals BR06(1) through BR11(1), each of which drives an associated relay as shown on drawing 2. Since the relays are DPDT, the user may select the energized state of the winding to either open or close two sets of relay contacts.

All six R-register flip-flops are cleared by the signal 0 ⟶ R which is generated at time pulse T2 of an ATR instruction. 0 ⟶ R is also produced by a G906 Power Up module during initial power turn-on. At T3 of the ATR instruction, A-register bits A06(1) through A11(1) are 1s transferred into flip-flops R06 through R11 by the signal A ⟶ R to energize particular relay windings on the data terminal panel. At T3 of an RTA instruction, the signal R ⟶ A initiates a 1s transfer of bits R06 through R11 into A06 through A11.

3.3.10 Z-Register (L6)

The 12-bit Z-register serves as an extension of the A-register during the MUL, ROR, or SCR instructions. The Z-register also buffers and assembles or disassembles words read from or written onto tape during MAGtape instructions. During the DSC instruction, the Z-register holds the 12-bit intensification matrix word. Functions initiated by the ICON instruction include clearing (0 ⟶ Z) and receiving information from the B-register (B ⟶ Z).

3.3.10.1 Shift Right Operation - During the MUL instruction, the Z- and A-registers combine to produce a 24-bit register. When executing MUL, ROR, or SCR, bits are shifted to the right. Bit A00 goes into A01, A01 goes into A02, etc., and A11 goes into Z00 through jam-transfer gates. Z-register bits are also shifted right. Bit Z00 goes into Z01, Z10 goes into Z11, and Z11 is lost. When performing the DSC instruction, bits of the intensification matrix word are shifted right in the Z-register.

3.3.10.2 Shift Left Operation - The Z-register assembles a 12-bit word from information stored on the three data tracks of the MAGtape. Three read/write heads read information from the tape and send it to the Z-register, via the 0- and 1-states of three data readers DR01, DR02, and DR03. The 0 and 1 outputs of the data readers are jam-transferred into Z-register flip-flops Z11, Z07, and Z03, respectively. When the first three bits of data are read, Z11, Z07, and Z03 are either set or cleared by the ZSHL pulse. Three more bits of data are read from tape into the data reader flip-flops and the next ZSHL pulse shifts the first three bits to the left in the Z-register.

The first three bits of data are now in Z10, Z06, and Z02. Two more readin and shift operations fill the Z-register with a 12-bit word compiled from four 3-bit tape lines. During MAGtape write operations, data is transferred from the B-register into the Z-register, and then out of bits Z00, Z04, and Z08 into the data writers. Here again, ZSHL is used to disassemble data words onto tape. The tape writers are shown on drawing M09.

3.3.10.3 Display Character Function - During a DSC instruction, the Z-register holds a 12-bit intensification word which is shifted to the right. While each bit of the word is in location Z11, it is evaluated to determine whether an ONINT (on intensity) or OFFINT (off intensity) pulse is generated (see drawing L21). If Z11 = 0 at time pulse T15 of a DSC instruction, the OFFINT pulse is produced; therefore, the particular grid coordinate selected is not intensified. If Z11 = 1, DSCN is generated to intensify the grid coordinate and to clear bit Z11. Bit Z11 is now evaluated again. Since it is 0, the OFFINT pulse is produced to turn off the intensity for the selected grid coordinate. At this point the contents of the Z-register are shifted right one place. Bit Z11 is lost and bit Z10 (now in location Z11) is evaluated, in the same manner as Z11 was previously.

3.3.11 Skip Network (L19)

The internal sense conditions are shown in the top left of the drawing L19. Type R141 Diode Gates are used to OR together the various possible internal-skip conditions to generate the level I SENSE. The external sense conditions are generated by R141 Diode Gates in LB32 and LB33. Again, the N value of an SXL instruction is gated against a condition (external sense line) to generate the X SENSE level. Levels are generated on this drawing when the left and right halves of the A-register are equal to 0, and when the A-register is equal to 7777. The level XSKCMET is generated by the B171 Diode Gate in LB35. This signals the skip condition during an XSK instruction. The inputs for the sense lines, the sense switches, and the left switches are shown on this drawing.

The MATCH V IBI level is generated in the lower left of drawing L19. This level is set up by the coincidence of the right 11-bits of the LINC S-register (address) and the left switches during the fetch or execute portion of an instruction. In addition, this level will be set up by the 1-state output of the IBI flip-flop.

3.3.12 PDP-8 Switches and Indicators (P27)

This drawing shows the cables that transfer switch-setting information into the PDP-8 processor section and the indicator drivers which enable the lights on the PDP-8 portion of LINC-8 control panel. Also shown are the cable connections which transfer the indicator signal information out to the LINC-8 console.

3.3.13 LINC Switches and Indicators (L28)

This drawing shows the indicator drivers used to control the lights on the LINC half of the LINC-8 control console. The cable connections for the control console lights and the control console switches are also shown, as are the drivers for the LINC speaker and the LINC RUN light.

3.4 MAGTAPE CONTROL

The MAGtape control is a standard subsystem of the LINC-8 Computer. It operates in conjunction with a dual tape transport to provide data storage and retrieval capabilities. Refer to the LINC-8 User Handbook section of the Digital Small Computer Handbook (C-800) for an introduction to the LINC MAGtape System.

3.4.1 MAGtape Format

3.4.1.1 MAGtape Track Placement - MAGtape utilizes a 5-channel format. To materially reduce bit dropout and minimize the effect of skew, each channel is redundantly recorded on two nonadjacent tracks of the 10-track MAGtape (Figure 3-1). The five MAGtape channels include: a timing channel (simultaneously recorded on tracks 1 and 10); a mark channel (tracks 2 and 9); data channel 1 (tracks 3 and 6); data channel 2 (tracks 4 and 7); and data channel 3 (tracks 5 and 8).

Information is transferred between MAGtape and the MAGtape control through a 10-track read/write head. Series connection of corresponding track heads within each channel and the use of Manchester phase recording techniques, rather than amplitude sensing techniques, virtually eliminate dropouts.

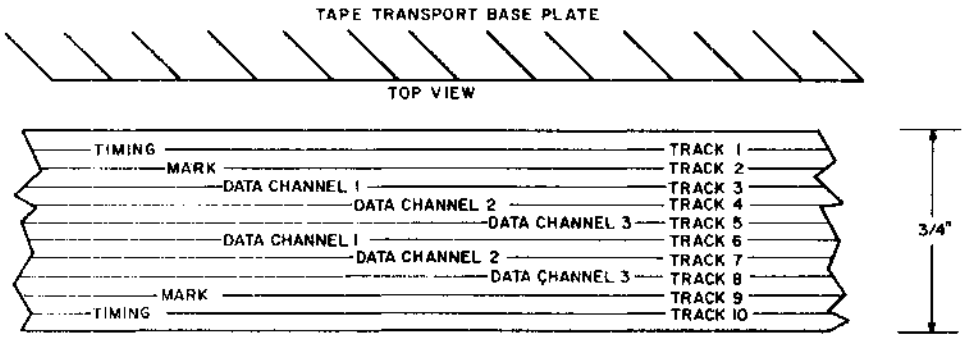


Figure 3-1 Track Allocation Showing Redundantly Paired Tracks

3.4.1.2 Word Assembly and Disassembly - During normal data reading, the LINC Z-register assembles 12-bit computer length words from four consecutive 3-bit lines read from the data channel tracks of tape (Figure 3-2). At the same time, the mark track is decoded to specify whether that 12-bit word represents a data word, a block number, or other information stored on tape. Timing signals from the timing track are used by the MAGtape control to provide synchronization for reading the mark track and reading from or writing on the data tracks. During normal data writing, the tape control disassembles

12-bit words and distributes the bits so that they are recorded on four successive data channel lines. Checksums are recorded with the data and used during subsequent reading operation to verify the correctness of the data transfers.

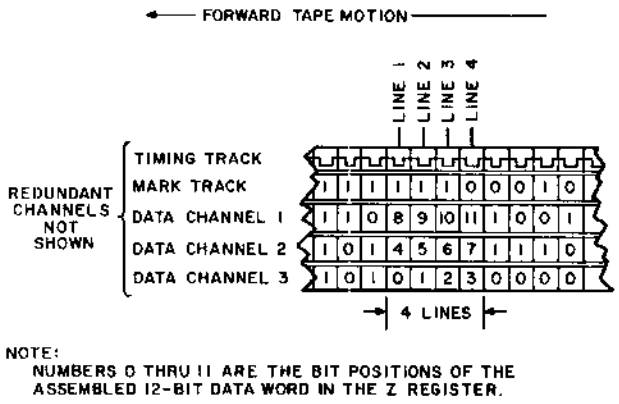


Figure 3-2 Structure of 12-Bit Data Word (4 Tape Lines)

3.4.1.3 Overall MAGtape Format - Figure 3-3 shows the overall block format for a standard MAGtape. The front and back end zones provide physical protection for tape. In normal computer programmed tape operations, the detection of an end zone either reverses the tape motion or brings both tape reels to a complete stop.

MAGtape blocks are numbered in octal. Blocks -10_8 to -0_8 are not used for data storage and are disregarded by the MAGtape control; however, these blocks provide a buffer area necessary for correct turnaround and search operations. Blocks 0 through 777_8 provide the user with 1000_8 (512_{10}) data storage areas. Each block contains 256_{10} 12-bit computer length words.

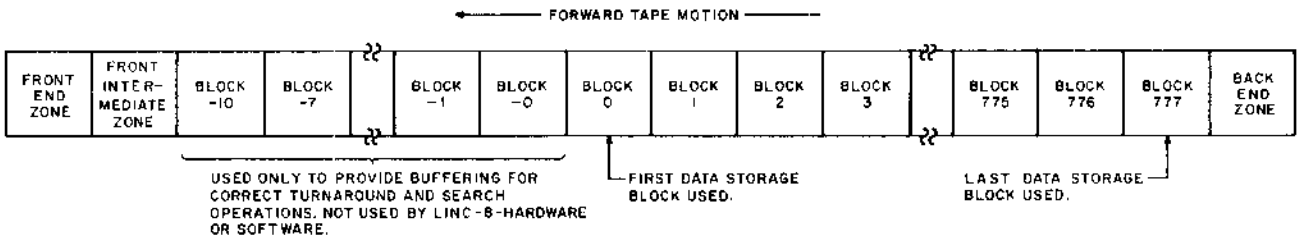
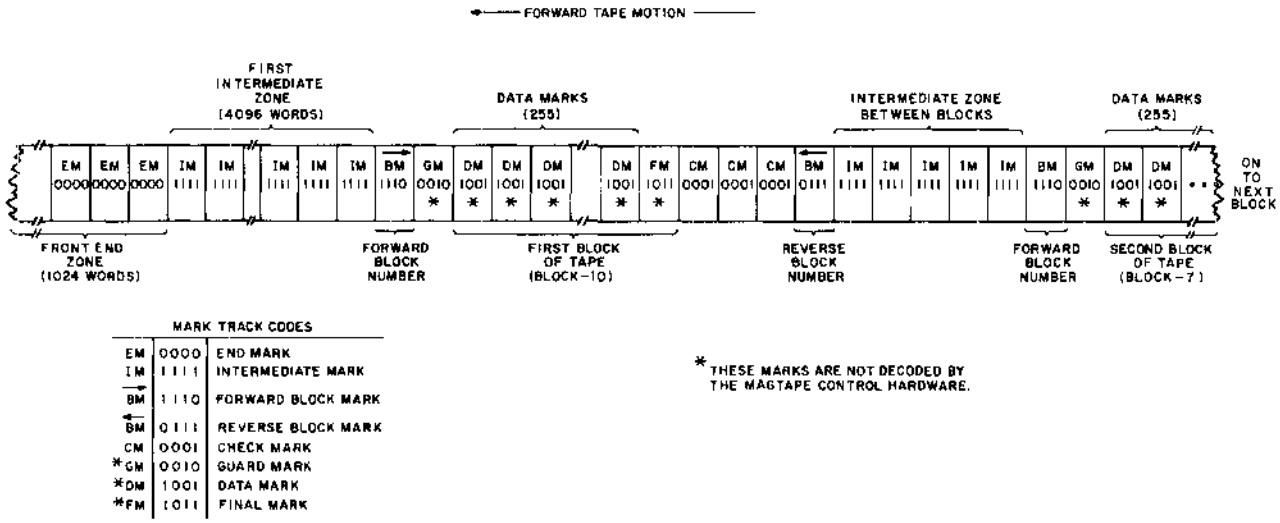


Figure 3-3 Overall LINC-8 MAGtape Format

3.4.1.4 Detailed MAGtape Block Format - Figure 3-4 illustrates the detailed MAGtape block format. Each area of tape, along with its associated mark track code, is shown. Starting at the left is the front end area (EM) consisting of 1024_{10} 12-bit words. This area, the front intermediate mark (IM) area and the negatively numbered front blocks provide buffering for tape turnaround and search operations. The front of the first data block of tape is indicated by the forward block mark (BM) of 1110. When the mark track decoder contains this value, the A- and the Z-registers contain the number of that particular data block (block -10 in this case). The value contained in the LINC A- and Z-register at a block mark is the complement of the number of the block, i.e., A and Z will contain 7701_8 at block 76_8. Although tape blocks -10 through -0 are not used for data storage by the LINC, their format is identical to that of blocks 0 through 777, which are used for data storage.

A block consists of a front block word ($\overrightarrow{BM}$), a guard word (GM), and the data words (DM). The last data word is the final word (FM) and then there is a check word (CM). The first check word contains the checksum (complement of the sum of data). The check mark (CM) also guarantees that the data writers will be turned off. Therefore, the two additional check marks (CM) are insurance to protect the backward block word ($\overleftarrow{BM}$). The final segments of a tape block are the five intermediate zone words (IM). These 20 lines of tape are sensed with a LINC skip instruction for special types of programmed searching.



MARK TRACK CODES		
EM	0000	END MARK
IM	1111	INTERMEDIATE MARK
$\overrightarrow{BM}$	1110	FORWARD BLOCK MARK
$\overleftarrow{BM}$	0111	REVERSE BLOCK MARK
CM	0001	CHECK MARK
*GM	0010	GUARD MARK
*DM	1001	DATA MARK
*FM	1011	FINAL MARK

* THESE MARKS ARE NOT DECODED BY THE MAGTAPE CONTROL HARDWARE.

Figure 3-4 Detailed MAGtape Block Format

3.4.1.5 MAGtape Format Summary - Table 3-1 presents a summary of MAGtape format; listed are the various zones of MAGtape, the number of words in each zone, and the function of each zone.

Table 3-1
MAGtape Format Summary

Mark		Number of Words	Function
EM		1024	Front End Zone
IM		4096	First Intermediate Zone
BM	Repeated 520 Times For All Blocks	1	Forward Block Zone Number
GM*		1	Guard Word
DM*		255	First 255 Data Words
FM*		1	Final Data Word
CM		3	Check Marks
BM		1	Backward Block Number
IM		5	Second Intermediate Zone
EM		1024	Back End Zone

*These marks are not decoded by the MAGtape control hardware.

3.4.2 Block Diagram Description

Figure 3-5 shows a block diagram of the MAGtape control. Basic timing pulses for tape operations are provided by the timing track, which is read by the timing track reader/writer. This functional element sends the signals BTR(0) and BTR(1) to the timing generator to produce timing signals TT0, TT1, and TT2 which control the majority of MAGtape operations.

Mark track data is used to locate specific control marks on the tape. These marks identify block zones, intermediate zones, check zones, and beginning- and end-of-tape areas. Mark track decoding is accomplished by the window register and decoder. Outputs of the decoder go to the motion control and the mode control. The motion and unit control selects a particular tape transport and determines the direction or reel rotation for the selected transport. The tape instruction, through the interface bus, initiates the operation of the motion control.

Data bits are read from and written onto three data channels of tape. The data is assembled and disassembled in the Z-register. One line of tape is read by the three data readers to produce three corresponding bits in the Z-register. The data in the Z-register is shifted left one place and three more bits are read from tape. After four read-and-shift operations, the Z-register contains a 12-bit word

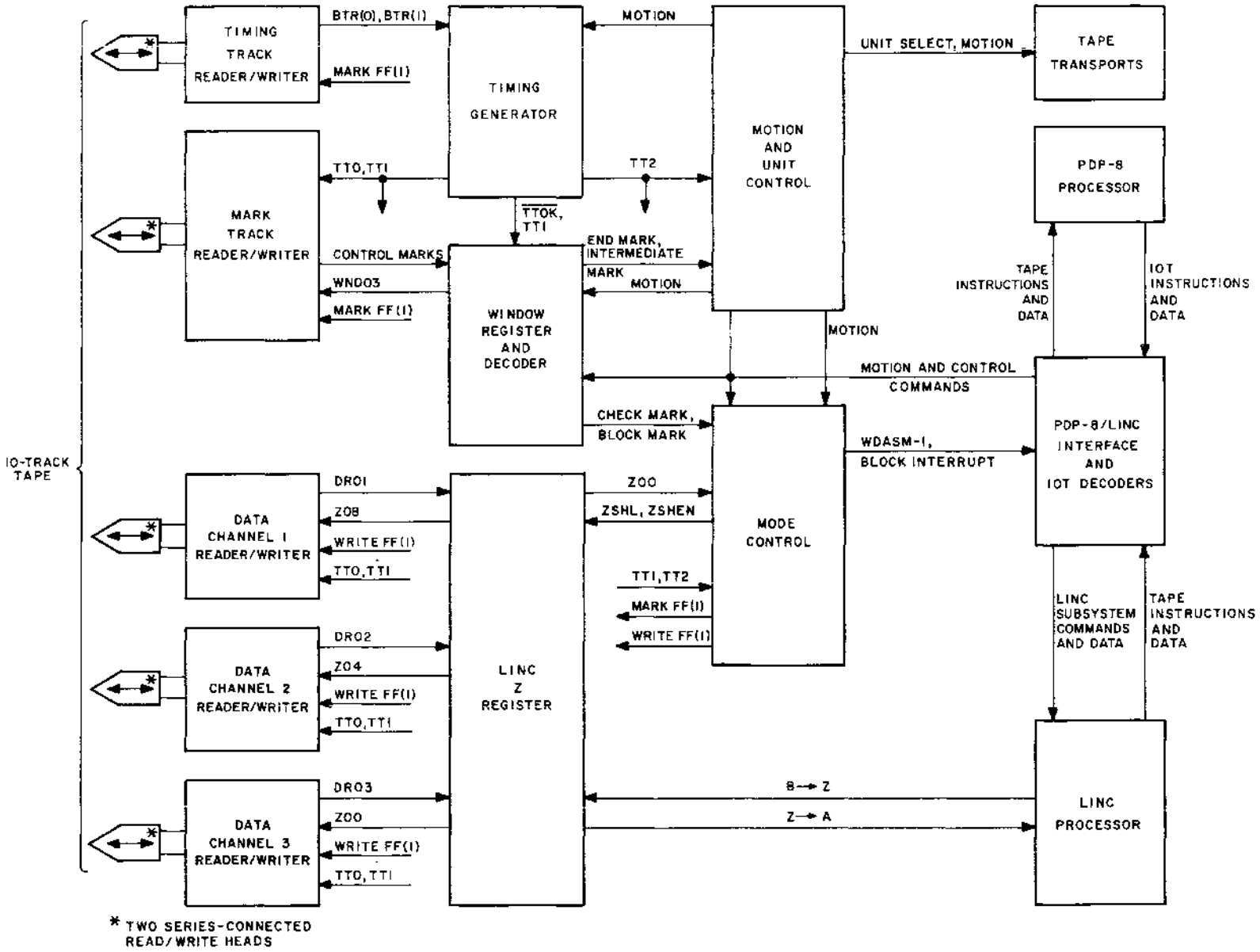


Figure 3-5 MAGtape Control Block Diagram

read from four lines of tape. Data is also written onto tape three bits at a time from the Z-register, in a similar manner as the reading operation. The Z-register sends tape information to the LINC A-register and receives data for writing from the B-register.

Reading and writing of tape data is determined by the mode control, through PDP-8 commands. Using outputs of the MARK, WRITE, LOAD, SEARCH, and BLOCK flip-flops, the mode control directs operation of all five reader/writer circuits. It initiates Z-register shift operations and also flags the PDP-8/LINC interface that assembly and disassembly of data is complete, through the WDASM-1 and BLOCK INTERRUPT signals.

3.4.3 Reader/Writer Circuits (M9)

Drawing M9 shows the reader/writer circuits associated with the five tape channels. These circuits consist of G882 modules which are high gain differential amplifiers connected directly to the read/write heads through a W072 Connector. The reader-half of the G882 receives outputs from the read/write head to produce complementary outputs at terminals V and U. The writer-half of the G882 produces complementary outputs at terminals J and K which go into the read/write head for writing on tape.

A −3V level at terminal R of each writer allows data to be written on tape while a ground level disables the writers from producing a flux change on tape. Writing on the timing and mark tracks is controlled by the 1-state output of the MARK flip-flop, while three data channels are controlled by the 1-state output of the WRITE flip-flop. Both of these flip-flops are shown on drawing M12.

3.4.3.1 Timing Track Reader/Writer - Basic timing pulses for tape operation are generated by the timing track reader/writer shown on the left of drawing M9. The timing track read/write head (two heads connected in series) is connected to terminals BD and BE of the W072 Connector. The signal read by this head is essentially a sinusoid with a period of 40 μs; each time the sinusoid crosses the zero reference (20 μs), the TR READER output changes. Outputs from the TR READER go through buffers to generate BTR(0) and BTR(1), which in turn generate TT0 and TT1, the two basic timing pulses for tape operations.

During the marking of tape, the 1-state output of the MARK flip-flop allows the T CHAN flip-flop to write timing data on tape. MARK flip-flop (1) also turns on the 10 μs clock shown on the lower left of drawing M9. Pulses from this clock complement the TC00 flip-flop every 10 μs while TC01 is complemented every 20 μs. The T CHAN flip-flop follows the output of TC01 to write a sinusoid on tape which crosses the zero reference every 20 μs.

3.4.3.2 Mark Track Reader/Writer - Control marks, defining specific areas of tape, are contained on the mark track. This data is read by the MR READER and sent to the window register (drawing M13)

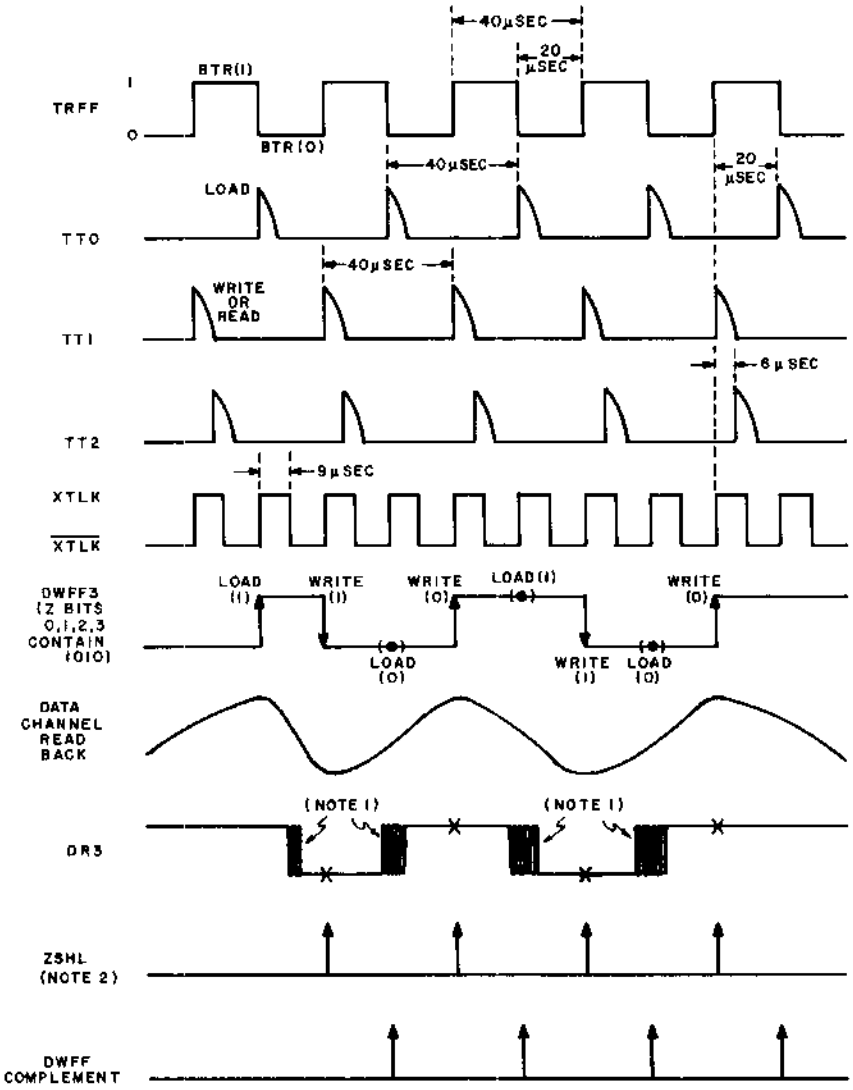
for decoding. During the marking of tape, MARK flip-flop (1) allows data to enter the M CHAN WRITER from the MWFF flip-flop. This data is the output of window register flip-flop WND03. Data from this flip-flop is read into the MWFF flip-flop at TT0. The MWFF flip-flop is then complemented at TT1. Therefore, the flux written on tape is changed from 0 to 1, or from 1 to 0, in synchronization with TT1 (corresponding to the time that the three data writer flip-flops are complemented). This process insures that the tape head signal as read-back will be maximum at TT1, which means that the read amplifier will be fully saturated with either a 0 or a 1 at TT1 time when data is read back.

3.4.3.3 Data Channel Reader/Writer Circuits - Three tracks on tape are available for data storage. Data is stored on tape serially, in groups of four 3-bit lines which correspond to one 12-bit data word. The Z-register disassembles data to be written on tape or receives (assembles) data from the three data tracks during reading. Writing of data from the Z-register is accomplished by data writer flip-flops DWFF03, DWFF02, and DWFF01. During a write operation, the Z-register holds a 12-bit word. At TT0, bits Z00, Z04, and Z08, are jam-transferred into DWFF03, DWFF02, and DWFF01, respectively, by the pulse TT0. From the DW flip-flops, the data is written on tape. Approximately 20 μs later, the DW flip-flops are complemented by time pulse TT1 which writes a complement of the data on tape. It is this flux change that saturates the reader on read-back when data is strobed in at TT1. TT1 also initiates a ZSHL (Z-register contents shift left one place) operation which places bits Z01, Z05, and Z09 into Z-register flip-flops Z00, Z04, and Z08, respectively. TT0 now jam-transfers these bits into DWFF03, DWFF02, and DWFF01, respectively. From the data writers, the data is now written on tape and the complement of the data is written on tape at TT1. In this way, the 12-bit word is written onto four lines of tape from the Z-register.

Data is read from the three data channels using reader outputs DR03, DR02, and DR01. These bits go into Z-register flip-flops Z03, Z07, and Z11, respectively. The ZSHL pulse is generated to shift the data to the left. A 12-bit word is read from four lines of tape and assembled in the Z-register in a similar manner to the disassembly for writing. Figure 3-6 shows the relationship between the flux changes mentioned above and the timing signals discussed below.

3.4.4 Timing Generator (M11)

The MAGtape timing generator is shown on drawing M11. It produces the timing pulses necessary for correct operation when the tape reaches a certain speed in either the forward or backward direction. The timing generator also inhibits the timing and control pulses if the tape is not up to speed or if a command is issued to stop the tape.



NOTE:
1. SHOWS NONSYMMETRY OF DATA TRACK ZERO CROSSINGS. DATA IS STROBED AT THE TIME OF MAXIMUM FLUX CHANGE.
2. DATA STROBED INTO Z REGISTER DURING READ. DATA DISASSEMBLED FROM Z REGISTER DURING WRITE.

Figure 3-6 MAGtape Read-Write Timing Diagram

The zero crossings of the tape timing-track data come into the timing generator as transitions of the signals BTR(0) and BTR(1). When tape is initially set into motion, the XTLK (cross talk) delay is in the 0-state which allows BTR(0) or BTR(1) to trigger the R602 Pulse Amplifier in location MH21. The output of this pulse amplifier sets the TTOK (tape timing OK) delay and also triggers the XTLK one-shot multivibrator (R302 module in location MH10). Once triggered, the R302 remains in the 1-state for 9 μs, thus inhibiting $\overline{\text{XTLK}}$. This ensures that there will be only one TT0 or TT1 for a given zero crossing on tape including times when the data writers are on. The TTOK delay is an integrating one-shot multivibrator which, when triggered, times out for 34 μs. Therefore, as long as zero crossings on the tape timing channel (nominal 20 μs) occur every 34 μs, the TTOK delay will always be in progress. This delay ensures that tape speed is approximately 50 percent of maximum, which is the minimum speed necessary for correct operation. The function of signals $\overline{\text{XTLK}}$ and TTOK in the generation of time pulses TT0, TT1, and TT2 is described below.

To further reduce the possibility of erroneous tape operation, the tape control timing pulses (TT0, TT1, and TT2) are inhibited during the time that a tape is accelerating up to speed. Acceleration occurs whenever a tape is started from a complete stop or when it has changed direction from forward to reverse or reverse to forward. Tape motion is defined by the states of the MOTN (motion) flip-flops shown on drawing M10. Acceleration or change of direction is indicated whenever one or both of these flip-flops go from the 0- to the 1-state. If either signal MOTN00 or MOTN01 goes to the 1-state, the R602 Pulse Amplifier (location MJ19) is enabled by the −3V to ground output transition of the respective motion flip-flop. The pulse amplifier is also triggered by the LOAD PLS (drawing L16) which prevents any spurious tape information from being picked up at the beginning of the load operation.

The R602 Pulse Amplifier triggers the R303 Delay, which produces ACIP, to indicate that acceleration is in progress. The R303 times out for 120 ms, which is sufficient time for the tape to come up to speed. At the end of this period, $\overline{\text{ACIP}}$ indicates that acceleration is not in progress and that the tape should be up to correct operating speed.

The circuits producing TT0, TT1, and TT2 are shown on the bottom of drawing M11. BTR(0) and BTR(1) are received at the pulse input terminals of the DCD gates which trigger the R602 Pulse Amplifiers. The level-input terminals of these DCD gates are enabled by the output of the gate shown on the lower left of drawing M11. The output of this gate goes to ground under the following conditions: tape timing is correct; acceleration is not in progress; cross-talk delay is not in progress; tape is not being marked; and tape is in motion. When the DCD gates are enabled, the zero crossings of BTR(0) and BTR(1) produce TT0 and TT1, respectively. TT2 occurs 6 μs following TT1. During the process of marking tape, TT0 and TT1 are generated by outputs from the TC00 and TC01 flip-flops described previously in the MAGtape Reader/Writer Section.

3.4.5 Mark Window Register and Decoder (M13)

In the MAGtape system, the mark track contains coded information which specifies definite areas of tape including block zones, intermediate zones, check zones, and beginning- and end-of-tape zones. Mark track data is read by the mark track reader and sent to the mark window register and decoders (drawing M13) as signals MR(0) and MR(1). The window register is a shift register comprised of five flip-flops which accumulate information from the mark track of tape. Gates shown on drawings M13 and M12 decode the outputs of the mark window register to produce control signals sent to other elements of the tape system. During initial tape operation, the CLOSE pulse sets the window register to 01110. CLOSE is initiated by the PWR CLR pulse, LOAD pulse, AC⟶MOTN command, or a combination of $\overline{\text{TTOK}}$ (tape not yet up to speed) and MARK flip-flop (0). The value 01110 in the window register is not one of the decoded Marks and therefore produces no significant tape operation. The close pulse generator output is 100 ns in duration; however, the R302 Delay (MH10V) increases the pulse duration to 0.5 μs. Since the WSHD flip-flop is in the 0-state, the window register output decoders are disabled from sending commands to other elements of the tape control system. Once the tape is up to speed, the WSHD flip-flop goes into the 1-state to permit window register output decoding.

If tape is moving in the forward direction, information from MR(1) is gated into WND00 through the R111 Gate (MJ23) and the R001 Gate (MJ22), shown on the lower center of drawing M13. At TT1, data is shifted in the window register from right to left. In the backward tape direction, the R121 Gate (MJ32) gates MR(0) into WND00. Because of this input inversion, the window register will contain a value for EM (end mark) which will be the same regardless of the direction in which tape is moving at the time. The forward EM code of 0000 will be read as 1111 in the reverse direction since, on tape, a 0 (forward) is read as a 1 (backward). However, since opposite sides of the mark track reader are gated into the window register, depending on the direction of tape motion, the window register ends up with the same value for EM. The same conditions are true for IM (intermediate mark) since the IM code 1111 (forward) is read as 0000 (reverse). In the case of BM (block mark), two codes are used because block numbers are read in either forward or reverse. The forward BM code is 1110 and the backward BM code is 0111. The CM (check mark) code is valid only in the forward direction of tape motion.

The CM decoder is shown on the right center of drawing M12. In this decoder, the four bits of the window register are ANDed with an output from the WDASM-2 (word assemble 2) delay to directly clear the WRITE SYNC flip-flop. The check mark occurs at the very end of the checksum word which appears at the end of a data block on tape.

During the marking of tape, the 1-state output of the MARK flip-flop holds the WSHD flip-flop in the 0-state to disable the window register output decoders from decoding the mark track information. The window register is loaded from the PDP-8 AC by bits BAC08(1), BAC09(1), BAC10(1),

and BAC11(1). These bits are 1s transferred into flip-flops WND03, WND02, WND01, and WND00 by MARK flip-flop (1) ANDed with WDASM-1. The signal WDASM-1 (drawing M12) occurs every time that four lines of data have been written on tape. Data read in from the PDP-8 AC is shifted left in the window register by TT1, and out of WND03 into the MW flip-flop (drawing M9) for writing on tape.

3.4.6 Motion Control (M10)

The basic MAGtape system is supplied with one dual-tape transport (tape unit 0 and tape unit 1). As an option, up to eight tape drives (maximum of four dual-tape transports) may be supplied with the LINC-8 Computer. Selection of a particular transport for data transfer and selection of tape motion is accomplished by the motion control shown on drawing M10.

In the basic LINC-8, unit flip-flop U0 (MH24) specifies either tape unit 0 (left) or unit 1 (right) for selection. Outputs of U0 are buffered through S107 Inverters to generate signals BU0 (buffered unit 0) and BU1 which provide enabling levels to the selection relays in the tape transports. When the LINC-8 is equipped with more than one dual-tape transport, the extended unit flip-flops U1 and U2 are added along with the unit decoder, shown above them on drawing M10. This binary-to-octal decoder provides information as to which unit is selected for operation (unit 0 through 7). The outputs of this decoder are inverted to provide the signals BU0 through BU7 (buffered unit 0 through 7). The inverters that buffer the outputs of the unit decoder now override the inverters that were previously used to generate BU0 and BU1. The extended unit flip-flops are loaded by the PDP-8 IOT instruction AC ⟶ FF (accumulator to flip-flops). The extended unit flip-flops are cleared either by the pulse 0 ⟶ FF (clear the flip-flops) or by the LOAD pulse.

3.4.6.1 Motion Flip-Flops - The motion of a selected tape unit is determined by the MOTN00 and MOTN01 flip-flops, shown on the right of drawing M10. A table relating tape motion to the states of these flip-flops is also shown on drawing M10. The STOP state provides no motion. The BKWD state causes the selected tape to go from left to right (backwards). The FWD state provides forward motion (right to left). The TURN AROUND state causes tape to go backwards and is the same as the backward state, as far as the tape transport is concerned.

Both motion flip-flops are cleared by the pulse 0 ⟶ MOTN which is an ICON instruction executed with 0000 in AC bits 8, 9, 10, and 11. The motion flip-flops will be set directly to the BKWD state when the LOAD pulse is generated during the load operation. They will be cleared by a combination of TT2 and EM when the LOAD flip-flop is in the 0-state and the tape is not in the search mode. This is done so that, if the tape is left in motion following a particular command and the end of tape is encountered, the tape will stop without winding off of the tape reel. The motion flip-flops

will also be cleared by a combination of TT2, IM, SRCH(0), MOTN00(1), and MOTN01(1). This enables the tape to be left in the TURN AROUND (backward) state and provides that the tape will automatically stop after it encounters the first intermediate mark. These conditions ensure that the tape has backed up one full block past the point at which it was turned around. This operation is advantageous to the programmer since the tape will always back up beyond the block of data last used.

The motion flip-flops will be complemented, during either of the following two conditions, by a gate associated with the complement terminals of the DCD gates of these flip-flops. The first condition occurs during the search mode and is triggered by the following signals: SRCH(1), EM, and TT2. During the search mode, these signals guarantee that the tape will turn around and return to the marked area when it reaches the end of a tape. The second condition for automatically complementing the motion flip-flops occurs when the tape is going backwards and the LOAD flip-flop is in the 1-state. These two conditions combined with EM and TT2 complement the motion flip-flops. During the load operation, the tape will turn around at the front end zone, thereby causing the tape to proceed toward block 0. The motion flip-flops may also be set depending on the contents of PDP-8 AC bit 0. If AC0 = 0, the AC⟶MOTN pulse will set MOTN00 to 1. AC⟶MOTN is generated during an ICON instruction when the right four bits of the PDP-8 AC contain 0001. If AC0 = 1, the same instruction will set MOTN01 to the 1-state.

3.4.7 Mode Control (M12)

The MAGtape mode control is shown on drawing M12 and consists of the MARK, BLOCK, SRCH, LOAD, and WRITE flip-flops. The state of a particular flip-flop or a combination of flip-flop states defines the various tape control modes of operation. Table 3-2 lists the various tape control modes and also shows how these modes are selected and cleared.

Table 3-2
Tape Control Modes

Mode	Instruction	PDP-8 AC
SEARCH	Set by: ICON: SET SEARCH	2
	Cleared by: ICON: OFF SEARCH	4
	Cleared by: ICON: ON BLOCK	3
	Cleared by: POWER CLEAR	
BLOCK	Set by: ICON: ON BLOCK	3
	Cleared by: ICON: OFF WRITE	6
	Cleared by: ICON: SET SEARCH	2
	Cleared by: POWER CLEAR	

Table 3-2 (cont.)
Tape Control Modes

Mode	Instruction	PDP-8 AC
WRITE	Set by: ICON: ON WRITE	5
	Cleared by: ICON: OFF WRITE	6
	Cleared by: 0 to MOTION	0
	Cleared by: ICON: SET SEARCH	2
	Cleared by: POWER CLEAR	
	Cleared by: CHECK MARK (after checksum word on tape)	
	Cleared by: TAPE TIME NO GOOD (Such as change of tape motion causing tape timing to go out of limit)	

3.4.7.1 Search Mode - The tape control is in search mode when the SRCH flip-flop is in the 1-state. In this mode, data from tape is continuously assembled in the Z-register and at the occurrence of each BM (block mark), block number data will be transferred from the Z- to the A-register and the LINC TAPE INT flip-flop (drawing L16) will be set to 1. The SRCH flip-flop is set by the IOT signal SET SEARCH and is cleared through IOT instructions ON BLOCK or OFF SEARCH. The LINC PWR CLR pulse also clears the SRCH flip-flop.

3.4.7.2 Block Mode - The block mode is selected when the BLOCK flip-flop is set to 1. In the block mode, data is assembled continuously in the Z-register. When four lines of data have been read into the Z-register, its contents are transferred into both the A- and B-registers and the Z-register is cleared.

3.4.7.3 Write Mode - The write mode is selected when both the BLOCK and WRITE flip-flops are set. This allows data to be transferred from the B- to the Z-register, for disassembly onto tape.

3.4.7.4 Mark Mode - When the BLOCK, WRITE, and MARK flip-flops are set, the mark mode is selected. The IOT command AC⟶FF is ANDed with the ground level produced when the MARK switch is lifted to set the MARK flip-flop. In this mode, the tape timing and mark tracks are written on tape under control of tape timing pulses TT0, TT1, and TT2 which at this time, are derived from the mark clock shown on drawing M9. Since the BLOCK and WRITE flip-flops are on, the mark mode functions essentially the same as the write mode, with one exception. In addition to writing information on the data channels from the Z-register (as transferred from the B-register), the mark channel is written from information shifted out of the window register. This information is transferred from bits 8 through 11 of the PDP-8 AC register under control of the Mark Program.

3.4.7.5 Line Counter - The line counter is a 2-bit register (LC00 and LC01) which is cleared by the signal BM·TT2 (block mark and tape timing 2) and counts on every TT1. The line counter is used in conjunction with the block mode of operation to generate WDASM pulses which signal the assembly of the four lines of data (one 12-bit word).

3.4.7.6 WDASM 1 and WDASM 2 - These two pulses occur shortly after TT1 (tape timing 1) to transfer data between various registers after a 12-bit word has been assembled (read) or disassembled (write) in the Z-register. In addition, WDASM-1 is used to set the TAPE INT flip-flop.

3.4.7.7 LOAD SYNC Flip-Flops - The LOAD SYNC flip-flops synchronize the tape operation with the memory timing when in the load mode. These flip-flops are discussed in detail in Section 3.4.8.

3.4.8 Load Operation (30)

The load operation enables the LINC-8 to transfer PROGOFOP from the basic system tape mounted on tape unit 0 (left-hand transport) into memory bank 0. The PDP-8 RIM and BIN Loaders are also loaded into the upper portion of memory bank 3. The load operation then starts PROGOFOP and the LINC-8 is set up to function in the LINC mode.

The following load description will refer to drawing 30 (Load Flow Diagram) and to the LINC-8 block schematic drawings which show the functions indicated on the flow diagram. The LOAD pulse (drawing L16) sets the LBRK and the LSEL flip-flops to initiate LINC LOAD operation. In the tape control section, the LOAD pulse clears the BLOCK flip-flop, sets the LOAD flip-flop, and forces the motion bits (M00 and M01) to the backward state. If the tape WRITE flip-flop was in the 1-state tape motion would be forward. The fact that motion was reversed would generate $\overline{\text{TTOK}}$ (tape timing not OK) and therefore generate the CLOSE pulse. The CLOSE pulse clears the WRITE flip-flop. If the SRCH flip-flop was in the 1 state, it will remain on. The LOAD pulse also sets the LCONSL INT (LINC console interrupt) flip-flop to indicate that a LINC console switch function has been initiated.

In addition, the LOAD pulse also generates the signal RESET MEMORY, shown on drawing L26. This sets the LMB to 2, and the UMB to 3. The LOAD flip-flop which has now been set by the LOAD pulse clears flip-flop LMB03 through an inverter which guarantees that the lower memory bank selector register will then equal zero. This means that all future LINC addressing will point to the first 2000_8 words of PDP-8 memory. On drawing P25, the LOAD flip-flop generates INT ENABLE to turn on the PDP-8 interrupt enable flip-flop. LOAD FF (1) also holds the PDP-8 timing signal CP ON in the ON state. The INT ENABLE function guarantees that when the LOAD process is complete, the PDP-8 will immediately answer a program interrupt request set up by the load process. CP ON ensures that the PDP-8 timing chain is running; therefore, memory can be referenced and data stored in memory under control of the LOAD hardware.

The ADDRESS SELECT flip-flop (drawing L16), is set to the LINC state at the next occurrence of B MEM DONE (buffered memory done) after the LOAD flip-flop has come on. If the LINC processor is running, it will continue to run until the next GNI (get next instruction) occurs, at which time the L RUN (LINC RUN) flip-flop will be cleared. The tape mark track is sensed and when an end mark occurs, the motion bits are complemented, thereby forcing the tape to the forward state. This logic is shown on drawing M10. When the tape turns around, the LINC P-register is zeroed as shown on drawing L21. Gates shown on drawing M12 set the BLOCK flip-flop to 1 at the occurrence of the block mark with the Z00 flip-flop in the 1-state. This indicates that the first positive block number has been found and the tape is moving in the forward direction (this is block 0).

WDASM (word assemble) pulses are generated when the tape control is in both the load mode and in the block mode with tape going forward. These pulses, as with other tape operations, transfer Z into A and B. The LOAD SYNC 1 FF is set to 1 by WDASM 2. This flip-flop then sets the LOAD SYNC 2 FF at the next BT2 (PDP-8 buffer time 2). These two synchronizing flip-flops provide synchronization between the tape operation and the operation of PDP-8 memory. The first time LOAD SYNC 2 is set to 1, the LINC MEM WRITE flip-flop is set to 1. This means that all subsequent memory operations occur with the data direction into the PDP-8 memory and, therefore, information will be written from the LINC B-register into the PDP-8 memory.

At MD (memory done) time when LOAD SYNC is set to 1, the signal P⊣▶S is generated. The first time through, this signal transfers the 0 from the P-register into the S-register and continues to write the contents of the B-register into memory. When the second word comes along, that word will be in the B-register for one memory cycle before the next P⊣▶S occurred. Therefore, the first word which is read (guard word) is written into memory for a number of memory cycles. Then the second word read (first word of the block) is written into the first location (address 0) for one memory cycle and then the address is changed to address 1 and so forth on through the entire data.

The above process continues until bit 3 of the LINC P-register changes from 0 to 1. This indicates that 376_8 data words have been written into memory. The change of P03 from 0 to 1 generates the pulse END LOAD (drawing L21). The END LOAD pulse clears the LBRK flip-flop, the BLOCK flip-flop, and the LOAD flip-flop. With the LOAD flip-flop in the 0-state, the ADDRESS SELECT flip-flop changes back to PDP-8 address at the next buffered memory done time, and the fact that END LOAD cleared the LBRK flip-flop guarantees that no further LINC processor operations are requested. The fact that the program interrupt is on means that if the PDP-8 was running, a program interrupt request is answered and the PDP-8 starts operating at location 1. If the PDP-8 was not running, then the END LOAD pulse will generate the KEY START level as shown on drawing P25 which starts the PDP-8 running. In addition, END LOAD clears the PDP-8 PC register by generating a 0 ⟶ PC 5-11 pulse (0 to PC05 to 11) as shown on drawing P25.

The above operations read the first block of tape into memory locations 0000 through 0376_8, and program control is transferred to the PDP-8. The PDP-8 then proceeds to execute the LOAD program which was also read-in from block 0 of tape. The standard LOAD program starts the LINC processor for at least two instructions which change the lower memory bank from 0 back to the standard setting of 2, and then proceeds to read in PROGOFOP and the PDP-8 RIM and BIN Loaders. For a more detailed description of the Load Program, the user is referred to the detailed write-up of the Load Program which is in the DEC Software Library.

3.5 LINC-8 TAPE TRANSPORT

This section of the LINC-8 Maintenance Manual contains both a mechanical and an electrical description of the LINC-8 Tape Transport. Operation of the tape transport through front panel pushbuttons, and automatic tape operation through computer commands, is described. It is recommended that the maintenance technician read and understand the information describing the tape transport and control before performing any maintenance checks or adjustments.

3.5.1 Mechanical Description

The MAGtape transport shown in Figure 3-7 consists of two complete tape transport systems designated unit 0 (left) and unit 1 (right). Each transport contains a pair of tape reel hubs, each of which is driven by an induction motor through a geared nylon belt. The tape motors are relatively high torque, low inertia motors which allow the tape to be started and stopped quickly. Correct operation of the tape system requires that the tape be rapidly started and stopped, without lifting the tape off the heads. Tape lifting can be one of the biggest sources of problems for the MAGtape system, and it can also be one of the most subtle.

Each motor and hub combination includes several parts with critical adjustments for correct tape system operation. Each motor has a pair of ball bearings, one at the front of the shaft and one at the back. Motor shaft end play is controlled by adding or removing shims from the adjusting port at the back end of the motor. The end play of the motor shaft should be between 0.001 and 0.004 in. The motor shaft end play is adjusted so that the bearings operate quietly while allowing the rotor to move very freely. Too tight an adjustment will result in drag, which will slow down the tape turn around and speed characteristics. Too loose an adjustment on the motor bearings will result in noisy motor operation. On some later transports the motors are equipped with a spring-loaded bearing assembly; in this case, the end-play tolerance is 0.005 in. to 0.025 in.

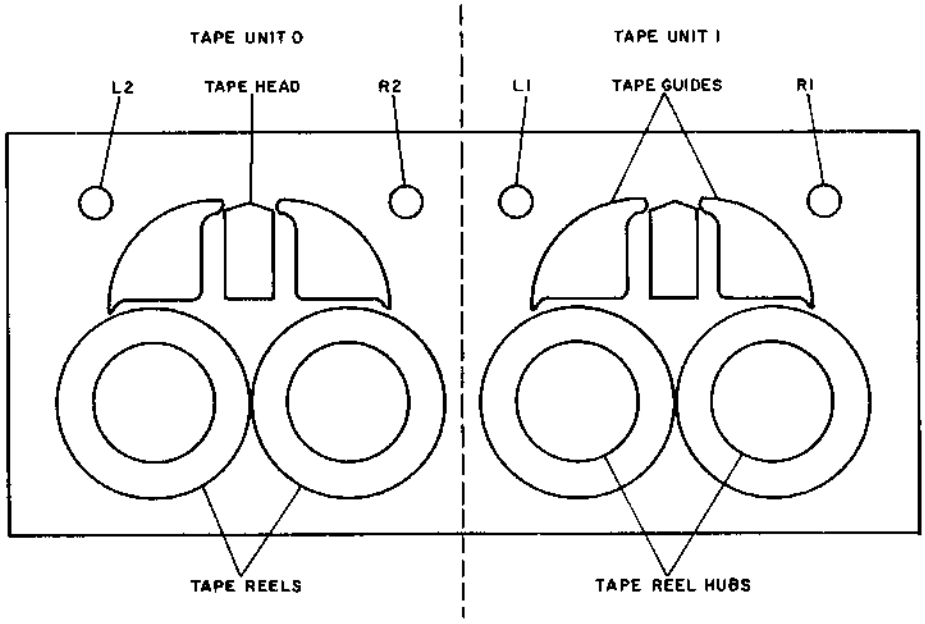


Figure 3-7 LINC-8 Tape Transport

Associated with the hub shaft are two more ball bearing assemblies. These are mounted at each end of the shaft, and are preloaded by a spring washer located between the front plate of the tape assembly and a collar which holds the spring washer against the front plate. Adjustment of this spring washer should allow approximately 0.01 in. of end play on the hub shaft. Again, the spring washer provides preloading to keep the operation of the bearings quiet. The final element in the drive is the belt that connects between the motor shaft and the hub assembly. This geared nylon belt does not stretch or change characteristics appreciably with time. It should run freely and, although it will tend to work its way to either the front or back of the pulleys on which it rides, it should never ride towards either the front or the back with such force that it binds against the edge of the pulleys. A belt that is binding against the pulleys usually indicates one of two things: either, the motor and hub shafts are not parallel, or the sides of the nylon belt are not parallel and have some high spot which will rub against the pulleys. Belt tensioning is controlled by the two screws which mount the motor assembly to its mounting plate. The belt is adjusted so that when it is pushed from the side, between the two pulleys, it moves approximately 3/16 in. If the belt is adjusted too tightly, there is too much friction in the system and the hubs and motor cannot spin freely; if the belt is adjusted too loosely, it will sometimes appear to be noisy, and it can ride up on the pulleys, thereby causing it to bind.

In conclusion, the motor and hub shaft assembly should be assembled so that they spin freely, do not bind, there is no appreciable amount of friction, and that they are mechanically quiet. If the above guidelines are followed, the motor hub assembly can be considered to be correctly adjusted.

3.5.1.1 Tape Travel Path - As shown in Figure 3-7, the tape travel path includes the feed hub, takeup hub, the feed and takeup reels mounted on these hubs, the two guides, and the tape head. Correct alignment of the tape travel path is extremely important for reliable operation of the tape system with good marginal characteristics. The tape hub is mounted on the hub shaft with two set screws. The distance the hub is mounted from the base plate of the tape system is a very important parameter. This is set at the factory and typically would not need to be changed, unless the hub was removed. The criterion for the correct placement of the hub is that when the tape feeds onto and off of the guides, it goes on to the middle of the tape reel and doesn't bind against either edge of the reel. From a practical standpoint, the distance from the base plate to the back edge of the hub is measured as the thickness of the back flange of a tape hub itself. However, the correct setting is ultimately determined by the tape going on to and off of the guides evenly.

A tape reel is held on the hub by the spring which goes around a groove in the hub. This spring is backed by two or three small rubber bands which provide the correct pressure to hold the reels against the hubs. If a reel is too loose it will slip when the tape is started or stopped. If it is too tight, it will take excessive pressure to mount a reel on a hub. Rubber bands are either removed or added to correct this condition.

To ensure compatibility between tapes, some rather rigid specifications are enforced for the alignment of the tape head and the guides with respect to the base plate. The base plate material is a very carefully finished jig plate which has very tightly controlled tolerances on its flatness. In addition, the perpendicularity between the back of the tape head and the positioning of the gaps on the various channels of the head guarantee that when the base plate and head are assembled together, the line of tape gaps will be perfectly perpendicular to the base plate (within 0.0005 in.). In addition, the tape guides are made from a single piece of lathe-turned aluminum. This guarantees that the thickness of the back flange of the tape guide will be essentially the same for the tape guide at either side of the head. Therefore, when tape is drawn across the head, the guides ensure that the tape comes at precise right angles to the gaps of the head. If, for some reason, the tape transport has been disassembled and the guides and/or head removed, extreme care must be taken when reassembling these components. Dirt cannot be allowed to accumulate behind the tape guides or tape head as this tends to skew the tape with respect to the head. The tape base plate and the tape head are critical mechanical components which should not be subjected to any undue stress.

Normally, no shimming is necessary or required in the mounting of the tape heads to the tape-transport base plate; the same is true of the tape guides. Under normal circumstances, skew is not observed on MAGtape transports. If skew is observed, it is usually caused by either damage to the tape head or to the tape base plate. If this condition is observed, it is strongly recommended that the tape transport be returned to DEC for a complete inspection and overhaul.

CAUTION

When making any adjustments, or when assembling or disassembling the tape transport, extreme care must be taken not to damage the heads, over-tighten the screws into the heads or the guides, or in any way damage the base plate.

The holes in the base plate which are used to mount the heads and guides are somewhat larger than the mounting screws. To ensure correct relative placement of the heads and guides, the guides should be gently pushed down as far as possible at the head and up at the outside edge (see Figure 3-8). The head should be pushed gently as far up as possible. This places the tape head well into the tape travel path.

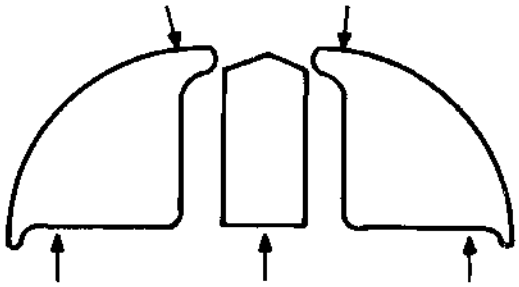


Figure 3-8 Tape Travel Path Adjustments

3.5.2 Functional Description

Both MAGtape transports are shown on drawing BS-D-7404146-0-1. Tape transport 1 is shown on the left and tape transport 0 appears on the right. Control signals between each transport and the LINC-8 Computer are interfaced through the MA connector shown at the bottom of the drawing. The two transports are operated independently of each other and never operate simultaneously. They share common ac and dc power lines, data lines, and signal lines, with the exception of the signals BU^0 and BU^1. These signals, which come from the motion control shown on drawing M10, are the buffered outputs of an S151 Decoder (MJ12). This binary-to-octal decoder receives inputs from the unit flip-flops. In normal operation, only one decoder line can be selected; hence, only one transport can be selected for operation at one time.

Both transports receive motion control commands in the form of signals $BMOTN_0^1$ and $BMOTN_1^1$ which are the 1-state outputs of the MOTN flip-flops, buffered through S107 Inverters (drawing M10).

However, only one transport will respond to these commands depending on whether BU^0 or BU^1 is at −3V (enabled condition). Unless otherwise indicated, the remainder of the tape-transport functional description will be directed toward unit 1 (shown on the left of drawing BS-D-7404146-0-1), but will also apply to unit 0.

Data is written on and read from the unit 1 tape while it is moving in the forward direction. Looking at the front of unit 1, the forward direction of motion finds both reels rotating counter-clockwise and the tape moving from right to left across the 10-track read/write head. The motor driving the left tape reel is called the left reel motor and is shown as M2 on the drawing. The right tape reel is associated with motor M1 which is defined as the right reel motor.

The tape unit has no capstan to maintain a constant tape speed; however, the maximum and minimum diameters of the tape reels are so close that tape speed remains relatively constant. Although reading and writing of data is always performed with the tape moving in the forward direction, block searching can be accomplished with the tape moving in either the forward or reverse direction. When bit packing density increases on a slower moving portion of tape (during write), that portion of tape is read at precisely the same tape speed as it was written, thus providing the effect of constant tape speed.

In the process of reading or writing data, approximately the full line voltage is supplied to motor M2 (left reel motor) while motor M1 (right reel motor) receives a small voltage which creates a small amount of torque in the reverse direction. This reverse torque ensures that tape is held against the head during tape motion operations. When the tape is stopped, the line voltage is divided across M1 and M2 connected in series. This produces a torque in opposite directions, thereby holding the tape tight against the head. Both motors M1 and M2 may be energized by pressing buttons located on the front panel next to each tape guide, or, remotely through signals received at connector MA.

3.5.2.1 Motors - M1 and M2 are unidirectional, single-phase, ac induction motors. The motors for 60 Hz systems operate at 117V and rotate at approximately 1600 rpm while 50 Hz motors require 117V and turn at approximately 1330 rpm. Each motor in the 60 Hz system drives a tape hub through a nylon gear belt at a 4:1 speed reduction and 50 Hz units utilize a speed reduction of 3.33:1.

The circuitry appearing above connectors PL_1 and PL_2 is the same for motors M1 and M2. For example, capacitor C1 in the right reel motor circuit functions as a phase shifting as does capacitor C2 of the left reel motor to provide the necessary motor torque. Thyractor Z1, in parallel with the series-connected 0.1 mF capacitor and 39 ohm resistor, functions to suppress noise generating transients when M1 is turned off. Similar functions for M2 are provided by Z2 and its associated capacitor and resistor. The remaining control circuitry for both M1 and M2 is described in relation to the various manual modes of operation and later as it applies to computer-controlled modes of operation.

3.5.3 Manual Tape Operation

Manual operation of tape unit 1 is initiated by the two pushbuttons located at the top of the tape unit 1 mounting plate. For certain modes, a button is merely pressed and then released; while for other modes, it must be pushed and held. The upper left pushbutton is designated L1 (Figure 3-7) and the upper right pushbutton is identified as R1. The four manual modes of operation are forward, reverse, static stop, and dynamic stop.

3.5.3.1 Forward Mode - In forward mode, the left reel motor (M2) drives counter-clockwise with strong torque. The right reel motor (M1) may drive cw with a slight torque or may be stopped, depending on the adjustment of the 100 ohm wire-wound resistor R1. The forward mode is selected by pressing and holding button L1. This connects −3.3V through contacts 5, 6, and 8 of L1 to terminal 3 of relay P1. The −3.3V is developed by zener diode 1/4M3.3AZ in series with a 1K resistor across −15V. This −3.3V causes relay P1 to energize and latch itself through its own contacts, 15 and 16, and through contacts 5, 6, and 7 of relay R1. When P1 energizes, it connects motor M2 between the 117 Vac lines through contacts 6 and 7; through resistor R1; through AC contacts 1, 2, and 3 of switch R1; and then through contacts 1, 2, and 4 of switch L1. The left reel motor M2 will now drive with a maximum torque in the ccw direction. The torque is determined by the adjustment of resistor R1.

Pushbutton L1 also connects resistor R1 to the same ac line that goes to the right reel motor M1. This produces a small ac voltage across M1, depending on the setting of resistor R1, which tries to turn M1 in a cw direction with a slight torque. This reverse torque keeps the tape tight against the read/write head while motor M2 is pulling tape in the forward direction.

3.5.3.2 Reverse Mode - In reverse mode, the right reel motor (M1) drives in a cw direction with a strong torque. The left reel motor (M2) is static with a light drag apparent in either direction. The reverse mode is selected by pressing and holding button R1. This will connect motor M1 across the 117V ac lines through R1 contacts 1, 2, and 4. M1 will now drive with a maximum torque which is somewhat variable depending on the setting of resistor R1.

3.5.3.3 Static Stop Mode - In static stop mode, the left reel motor (M2) is static with a slight drag apparent in either direction; while motor M1 is stopped but free to turn, by hand, in either direction. The static stop mode is selected whenever power is first applied to the transport or when button R1 is pressed and then released. The slight drag condition of motor M2 is caused by a pulsating dc voltage developed by transformer T1, capacitor C6, and the 1N645 diode. The dc voltage is applied to motor M2 through n.c. contacts 5 and 6 of relay P1.

3.5.3.4 Dynamic Stop Mode - The dynamic stop mode causes the left reel motor (M2) to drive ccw while motor M1 drives cw, each driving with approximately equal and medium torque. This mode is selected by pressing and releasing button L1. When L1 is released, relay P1 remains energized through its own n.o. contacts 15 and 16. Since contacts 1, 2, and 4 of button L1 are open, motors M1 and M2 are connected in series between 117V. Thus both motors drive with equal torque, and if tape were loaded on the reels, the tape motion would be stopped dynamically.

3.5.4 Computer Tape Operation

Tape unit 1 can be automatically directed to read and write data through signals received from the tape control system. The signals are designated BU^1, $BMOTN_0^1$, and $BMOTN_1^1$, and enter the tape transport through the MA connector located on the back of the unit and shown on the bottom of the tape transport drawing. Tape unit 1 is selected for operation when the signal BU^1 is at −3V. This signal also energizes relay H1 to enable the read/write heads associated with tape unit 1. The status of the BMOTN signals then determine the motion of tape unit 1. The BMOTN signals also control tape unit 0 when the signal BU^0 is at −3V. Tape unit 1 is described for each of its four computer controlled modes of operation: forward, reverse, turn around, and dynamic stop.

3.5.4.1 Forward Mode - In forward mode, the left reel motor (M2) drives ccw with a strong torque. Motor M1, depending on the adjustment of resistor R1, may drive cw with a light torque or will be stopped, but free to turn by hand. This mode is selected when both the $BMOTN_1^1$ and BU^1 signals are at −3V. $BMOTN_1^1$ can be designated as a bus switching signal since it energizes relay M1. Relay M1 then switches a −3 Vdc bus at contact 15 to a control bus line at contact 16. Relay M1 also closes an ac line bus through contacts 7 and 6 thus causing the left reel motor M2 to drive with maximum torque.

3.5.4.2 Reverse Mode - In reverse mode, motor M1 drives in a cw direction with strong torque. Motor M2, depending on the adjustment of resistor R1, will drive ccw with a light torque or will be stopped but free to turn by hand. This mode is selected when $BMOTN_0^1$ and BU^1 are at −3V. The reverse mode is similar to the forward mode with the exception that relay M0 is energized instead of relay M1. This connects the opposite ac line to the control bus line through relay M0 contacts 6 and 7 placing a small ac voltage across the left reel motor M2. Motor M1 receives almost the full line voltage and therefore drives with a maximum torque.

3.5.4.3 Turn Around Mode - The turn around mode is selected by energizing both relays M0 and M1. This mode is identical to the reverse mode (described in Section 3.5.4.2 above) as far as the transport is concerned. The computer control examines the mark window and then clears the motion bits at the next occurrence of intermediate zone marks.

3.5.4.4 Dynamic Stop Mode - This mode causes the right reel motor (M1) to drive in a cw direction while M2 drives in a ccw direction, both turning with an equal and medium torque. The dynamic stop mode is selected by disabling all control signals after some other computer controlled mode was previously selected. Removal of the signal BU^1 is not pertinent during single unit (unit 1) operation. As an example, after disabling the signals that selected the forward mode of operation, relay P1 remains latched, thereby connecting both motors in a series across the ac line through P1 contacts 6 and 7. This causes each motor to drive with equal and medium torque.

3.5.5 Tape Head Selection

Each dual-tape transport is equipped with two tape heads. Each head consists of five 2-track channels. As shown on drawing BS-D-7404146-0-0 and SC-D-3404601-0-0, diodes are provided to select the head. In normal operation, only one tape head is selected. Selection is accomplished by grounding the center taps of each of the channels of a given head. Because there is a 1 mA loading to −15V at the tape connector (MA40 and MB40), the head selection diodes are forward biased for selection. The center taps of the unselected head are held to −15V, thereby back-biasing the selection diodes for that particular head.

Since the T (timing) and M (mark) channels are read while simultaneously writing on the data channels, it is very important that the ground lines for the T and M channels be isolated from the ground line for the data channels. The relays H0 and H1 select the heads for unit 0 and unit 1, respectively.

3.6 ANALOG SYSTEM (P24)

This section describes the operation of the LINC-8 analog system including A-D converter, analog-output circuits, preamps and optional multiplexer channels. The analog system (drawing P24) includes two 9-bit D-A converters, A502 Comparator, A401 Sample and Hold, A130 Multiplexer modules, A202 Preamplifiers, and associated logic (primarily the LINC A- and B-registers). The D-A converter connected to the least-significant nine bits of the LINC B-register provides the 0 to 3V signal used to drive the scope horizontal axis. The D-A converter connected to the right nine bits of the LINC A-register is used to drive the scope vertical deflection (through a W500 Follower) as well as provide the comparison voltage during A-D conversions. The W500 eliminates oscilloscope cable capacitance from affecting the accuracy of the D-A converter during the SAM instruction. Refer to the analog section of the FLIP CHIP Module Catalog for a discussion of successive approximation A-D converters, D-A converter modules, A704 Power Supply and A502 Comparator modules used in the LINC-8 analog system. Because of the accuracy and stability of the modules, it is unlikely any of the above modules will need adjustment. Basic A-D alignment procedures are included in the Maintenance Section of this manual.

The system utilizes the D-A converter associated with the A-register and also uses LINC A- and B-register logic to form a 9-bit conversion. The signal to be converted produces a voltage between 0 and −10V at the output of the sample and hold module (pin PH24P) during conversion. The sample and hold continuously samples the output of the multiplexer channel which is determined by the right four or five bits of the LINC C-register. The sample and hold goes into hold mode at T3 of the SAM instruction. This means that the desired multiplexer channel was selected for 2 μs before going into the hold state. The sample and hold can track any input which moves slower than 10V/μs. The A130 Multiplexers select one of 16 (32 with optional channels) input channels and connect the input to the sample and hold. The multiplexers provide both offset and attenuation. The inputs to the multiplexers are approximately −5V to +5V and produce corresponding outputs of −7.5V to −2.5V. Channels 0-7 are directly connected to 5K 3-turn potentiometers located on the face of the oscilloscope preamplifiers. These potentiometers have +6 and −6V across them received from the A706 Power Supply located in PJ25. This supply also provides power to the multiplexer and sample and hold circuits.

Channels 10-17 are connected to eight preamplifiers located in the terminal panel (drawing 2). These preamplifiers have both gain and offset adjustments which compensate for tolerances in both multiplexers and the sample and hold. For accuracy and stability, all eight preamplifiers are operated from the regulated A706 Reference Supply mounted in location B31. Each of the two preamplifiers comprising one A202 Module has an input impedance of 50K and receives an input signal through a phone jack mounted on the data terminal panel. This analog input can be a maximum of ±1V which produces a corresponding output change of ±5V. The outputs of all eight preamplifiers go through the W011 Connector (B32) to the W021 Connector (PH21) associated with the LINC-8 A-D System (drawing P24).

3.6.1 Display Oscilloscope

The LINC-8 uses a Tektronix Type 561 Oscilloscope for display purposes. Two D-A signals (X deflection, Y deflection) are applied across 510 ohm resistors to produce 0 to −3.3V signals with an output impedance of approximately 3000 ohms (drawing P24). These D-A signals go to the right-hand scope plug-in and are directly available on the right-hand scope plug-in front panel. Two intensify pulses are also generated, ONINT 0 and ONINT 1. The rotary switch at the lower left of the right-hand scope plug-in is used to select which one, or both, intensify pulses will trigger the intensify flip-flop located in the oscilloscope plug-in. The OFFINT pulse turns the intensify flip-flop off. See the Tektronix 561 Manual and refer to Chapter 5 in the LINC-8 Users Handbook for more information concerning the display oscilloscope. In addition, Section 5.9 of this manual contains a test procedure for the display oscilloscope.

NOTE: When working with analog aspects of the LINC-8 system one must be careful of ground loops. Both A-D inputs and D-A outputs are single ended with respect to the ground reference located on racks H and J of the Processor (P) section.

3.7 DATA TERMINAL PANEL (2)

The data terminal panel contains facilities for interfacing the LINC-8 Computer to external devices associated with a particular experiment. The facilities include: eight analog preamplifiers, six DPDT relays and relay amplifiers, and a permanent magnet speaker (see drawing 2). The data terminal panel also contains module connectors which will accept up to 50 FLIP CHIP modules. With these connectors, the user can wire his own special interface and control logic circuits for application in the experiment he is conducting.

3.7.1 Analog Preamplifiers

Four Type A202 Dual Preamplifiers are shown on the left drawing 2. These are normally used in conjunction with the LINC-8 A-D circuits but are available for other user applications (see last paragraph in Section 3.6).

3.7.2 Relays and Relay Amplifiers

Shown in the center of drawing 2 are six DPDT relays and their respective relay amplifiers. One SPDT relay (terminals 5, 6, and 7) in each DPDT combination is connected to one set of red, blue, and white binding posts on the data terminal panel. A second SPDT relay (terminals 14, 15, and 16) in each combination is operated by the same relay amplifier as the first. Connections to this relay can be made at the relay itself. A −3V level at the base of the transistor relay amplifier energizes the relay coil thus closing relay contact 6 to 7, and contact 15 to 16. A ground level at the base deenergizes the relay, thus closing contact 6 to 5, and contact 15 to 14. Base inputs to the relay amplifiers are received from the R-register, shown on drawing L6.

3.7.3 Audio Monitoring Facilities

The LINC-8 contains both a speaker circuit and a chime circuit, as shown on the lower center of drawing 2. The chime circuit is activated whenever a LINC HALT instruction is executed and the CHIME switch is on.

3.8 SPECIAL MODULES DESCRIPTION

There are several modules that are special to the LINC-8 computer and are not described elsewhere. These modules are briefly described below. Block schematics of these modules are shown in Volume II of this manual.

3.8.1 W072 LINC-8 Scope Connector

This is a double-height module which is used to connect the LINC-8 scope to the display logic. In addition to providing one-to-one connections, between split lugs for the cable and the logic pins, several load resistors are provided. Between pins AE and AF, and between pins AH and AJ there are 560 ohm quarter-watt resistors. These resistors provide loading for the analog output signals.

Across each of the pairs AK-AL, AM-AN, and AP-AR, there is an 100 ohm resistor. These resistors provide termination for the intensity pulses (coming from the W640 module).

3.8.2 W073 LINC-8 Tape Cable Connector

This connector provides for the connection of the LINC-8 tape transport to the tape control logic. It is essentially one to one connections between split lugs and the logic terminals. In addition, 15K resistors are connected between each of the head cable lines and -15V which is brought to pin BK. These resistors provide 1 mA of current from the -15V supply. This provides forward bias for the head selection diodes in the tape transports.

3.8.3 G906 LINC-8 Capacitor and Power Up Modules

This module consists of two sections; the first section is made up of 12 each 220 PF capacitors. These capacitors are used to slow down the outputs of the delayed timing inverters shown on drawing LI5. The second section of this module consists of a special power inverter which is connected through isolation diodes to pins T, U, and V. This power inverter is so designed that it will prevent pins T, U, and V from going more negative than -0.8V until such time as the -15V supply is more negative than -7V. The combined load on pins T, U and V must be less than the equivalent of a 200 ohm resistor to the -15V supply.

This power inverter section of the module is used to hold the internal LINC power clear lines and other lines in the 0 (ground) state during the time that the power is being turned on in the machine. This prevents any spurious writing on the tape which may be located over the tape heads, and also ensures that the LINC-8 relays will come up in a 0 state.

3.8.4 A202 Preamplifier

The A202 preamplifier consists of two non-inverting operational amplifiers. These amplifiers are identical and, therefore, this discussion will only include one amplifier (pins J & K). The amplifier is provided with a nominal gain of 5, and a nominal input range of ±1V. The nominal offset is 0 ± 0.2V.

Diodes D1 and D2 provide input range limiting to prevent the amplifier from saturating when large input signals are applied to the amplifier. R2, in conjunction with the diodes D1 and D2, provides maximum current limiting on the input in case of extremely large input signals. If several hundred volts are applied to the input, R2 will be burned out. The input is capable of handling up to 50V input for periods of several seconds. R1, in conjunction with the base loading of Q1 provides the input impedance of approximately 50K.

Q1 is connected as a differential amplifier which compares the input signal with 1/5 of the output signal as developed across the potentiometer R12. The voltage references for the offset adjustments are provided from an A706 Power Supply module which also supplies the -10V reference for the amplifier.

3.8.5 A130 Multiplexer Module

The A130 module is a 4-channel multiplex module used in the LINC-8 system to select one of up to 32 possible channels of analog input. The 4 channels are virtually identical and so the following discussion will only be for the first channel pins J, L, K, and the output H. A channel is selected if the diode input consisting of D1, D2, D3, D4 and Q2 is enabled by providing a positive signal on both pins J and L. The analog input for channel 0 is brought into pin K. The voltage divider, consisting of R3 and R4 provides attenuation and offset. The channel 0 signal then goes through the emitter followers Q1 and Q3. If the given channel is selected, this means that Q2 is in the cutoff state. Therefore, the emitter of Q3 will be following the offset attenuated analog-input signal. The output terminal pin H will then track the emitter of Q3 by the forward biased diode, D6. If channel 0 is to be cut off, then Q2 will be placed in a conducting state thereby back biasing D6 when another channel is selected.

The multiplexer has an input range of ±5V and provides an output signal of -2.5 to -7.5V.

3.8.6 A401 Sample and Hold

The A401 Sample and Hold module consists of an input buffering amplifier, a holding capacitor and output buffering amplifier. Q1 provides the internal switching signals and buffers the digital input, hold signal (pin L). When pin L is negative the sample and hold is said to be in the sampling state. The analog-input signal is buffered through the dual emitter configuration of Q2 and Q3.

Q8, Q9 and Q10 constitute an operational amplifier used to buffer the output of the charging capacitor and provide for a holding accuracy of at least 0.2 V/ms. The input signal to the sample and hold is -2.5 to -7.5V, and the output signal is 0 to -10V.

3.8.7 A706 Power Supply Module

The A706 Power Supply is used to provide regulated power for the A202 Preamplifiers in the data terminal panel. One A706 is required for each four A202 modules. In addition, another A706 is used to provide the reference voltages for the potentiometers connected to A-D channels 0-7 and the offset reference for the A401 Sample and Hold.

This module consists of three short-circuit protected, series regulating supplies. The supply voltages are +6 ± 0.3, -6 ± 0.3, and 10 ± 0.5V. The outputs should change less than ±0.020V with the following input power: 10 ± 1V, and 15 ± 2V. The nominal maximum loading on the supplies is: 50 mA for the two 6V supplies, and 25 mA for the 10V supply. The dynamic output impedance of the power supplies, when operating in the regulating range, is less than 1 ohm.

CHAPTER 4
INSTRUCTION TIMING DIAGRAM DESCRIPTIONS

4.1 GENERAL INFORMATION

This chapter contains timing-flow diagram descriptions for each instruction performed by the LINC section of the LINC-8 computer. The first part of the chapter is a general introduction to the format of the instruction flow diagrams. Following that is a description of each instruction to be used with the flow diagram for that particular instruction. Timing-flow diagrams are presented in alphabetical order in Volume II of this Maintenance Manual. The instruction description coupled with a detailed description of the logic functions and registers affected during that instruction provide the user with comprehensive information about LINC operation. Descriptions of LINC logic elements are contained in Chapter 3. In particular, refer to Section 3.2.1 for a description of the PDP-8 IOT instructions which perform specific functions within the LINC subsystem. Supplementary information concerning each LINC instruction is found in the LINC-8 section of the Digital Small Computer Handbook (C-800) and in the LINC-8 Programming Manual, I-L85 (A).

4.2 INSTRUCTION TIMING DIAGRAM FORMAT

LINC-8 operations during the execution of each instruction are shown on the timing-flow diagram for that particular instruction. As an example, look at the LDA diagram in Volume II; the dashed line across the upper section of the drawing separates PDP-8 processor functions (shown above the line) from LINC processor functions (shown below the line). PDP-8 timing pulses T1 and MD are shown at the top while LINC timing pulses (GNI, GO, T1, T2, TLAST, etc.,) appear at the bottom.

PDP-8 and LINC registers affected during an instruction execution are listed along the left side of the drawing. PDP-8 functions shown include the status of the MB register, sense amplifiers, and in some cases, the DATA DIRECTION. When DATA DIRECTION is shown up, data is written into memory from the LINC B-register. LINC registers include the S-, P-, B-, A-, and C-registers, and the MEM ⟶ B flip-flops which allow stored information from the PDP-8 memory to enter the LINC B-register. Additional functions are also shown when they affect a particular instruction.

A break in the horizontal line (—┤) associated with a particular register or flip-flop indicates a clearing operation such as that which clears the MEM ⟶ B flip-flops at GNI time. A vertical arrow (↓ or ↑) indicates that information from one register goes into another register. An example of this is shown at GO time when the contents of the P-register go into the S-register. Previous to GO, the P-register contained some value (designated by P); following GO, the P-register contains P+1.

A circle and dot (⊙) like the one shown for the PDP-8 sense amplifiers between GO and T1, indicate that information read out of the sense amplifiers goes into the MB, B-, and C-registers, all of which were previously cleared at GO time.

When the format of the LDA iβ instruction is changed, due to the configuration of the i and β bits (i=0, i=1; β=0, β≠0), the table and information appearing at the bottom of the drawing indicate the sequence of events that occur during that particular configuration. The curved, dashed line shown following T1, on the LINC timing pulse scale, indicates that the LINC-8 will jump from time pulse T1 directly to T10 for the condition where i=1 and β=0. T2 through T7 are skipped during this particular format. This is also indicated in the table shown at the bottom of the drawing. At T1, the signal 10 ⟶ T is produced if i=1 and β=0.

At T2, information from either the C-register or the P-register goes into the S-register as shown by the dashed line. The particular condition is determined by following the line down from time pulse T2 to the table. If i=0 and β=0, P+1 goes into S and P+2 goes into P. P+1 is shown in parentheses following T2 on the P-register line. The tabular designation P+2 ⟶ P indicates that the P-register has been incremented twice since the start of the LDA instruction. At T2 if i=0 and β≠0, bits 8 through 11 (Beta information) of the C-register go into bits S08 through S11 and S00 through S07 go to 0. If i=1 and β=0, T2 is skipped. Finally, if i=1 and β≠0, a β ⟶ S transfer occurs. The lowercase letter a on the A-register line represents the contents of the A-register.

Indexing operations that take place within certain registers are indicated by parentheses and a dot ((⊙)) such as is shown for the MB and B-registers at T3. The indexing is conditional depending on the state of the i and β bits. If i=1 and β≠0, the contents of the MB and B-registers are indexed by 1 at T3. If i=1 and β=0, T3 is skipped. No indexing occurs for the other two conditions of i and β.

The value read out of the memory sense amplifiers following T2 into the MB and B-registers is designated Y. The designations Y* and P* specify the contents of the S- and P-registers, respectively, at T10. These designations also appear as headings for the table shown on the bottom of the drawing. The symbols indicate that following T10, the P-register will contain p+2 and the S-register will contain Y, if i=0 and β=0. P will contain p+1 and S will contain Y when i=0 and β≠0. If i=1 and β=0, the P-register contains p+2 and S contains p+1. Finally, if i=1, and β≠0, S will contain Y+1 and P will contain p+1.

The right-most column of the table specifies functions that occur at T10 depending on the i and β configuration. When i=1 and β=0, the contents of the P-register go into the S-register and the P-register is incremented by 1. For all other conditions of i and β, the contents of the B-register are transferred into the S-register. The A-register is cleared at T10.

Following T10, the operand "r" is transferred from memory (sense amplifiers) into the B-register. At T11, the contents of the B-register (r) are transferred to the A-register by the half-add function

designated BCOA (B-register bits complement corresponding A-register bits). The A-register now contains the operand "r". GNI (get next instruction) will be generated at T11 in anticipation of the next instruction. TLAST is generated 0.5 μs after GNI. If the LINC-8 is to continue operation in the LINC mode, GO will be generated to start the next instruction. Assuming that this is the case, then +1 is added to the contents of the P-register and P* (determined at T10) goes into the S-register. Thus the LINC is executing the next instruction. This GO pulse is the same as the one shown at the beginning of the timing diagram for the next sequential LINC instruction.

If the LDA i β instruction described in the preceding paragraphs is the first LINC instruction to be executed, then the GNI pulse shown at the start of the timing diagram is not generated. In this particular case, the instruction would commence with the GO pulse. GNI would be generated, however, for all succeeding LINC instructions since the first GNI pulse is not generated until the completion of the first LINC instruction. As explained previously, this GNI pulse is the same one shown at the beginning of the flow diagram for the next sequential LINC instruction.

4.3 FULL-ADDRESS INSTRUCTIONS

4.3.1 ADD X

At GO time, the C, B, and MB registers are cleared while the MEM ⟶ B flip-flops are set. The contents of P go into the S-register and p+1 goes into the P-register. The A-register still contains the value a. The S-register now contains p, which specifies the memory location containing the ADD instruction and its associated operand address (X).

Following GO time, the MEM ⟶ B flip-flops allow data to come from the memory location specified by S through the sense amplifiers into the MB register, the B-register and the C-register since the PDP-8 is in a read operation. This 12-bit word is the ADD instruction where bits 0 and 1 specify the operation code (ADD) and bits 2 through 11 specify the address (X).

At T1 time, the B-register is cleared. The PDP-8 at this time writes the instruction back into location p from the MB register.

At T2 time, the address portion of the ADD instruction (bits 2 through 11) is jam-transferred from the C-register into the S-register (bits 2 through 11) to specify the memory location containing r. S0 and S1 remain cleared. The PDP-8 is in a read cycle and the operand "r" is read from the specified memory location into the MB register and into the B-register.

At T3, a BCOA (B-bits complement corresponding A-bits) takes place between the A- and B-registers. This operation is commonly referred to as half-add or exclusive OR. For each bit of B that is 1, complement the corresponding A-bit. For any B-bit that is 0, leave the corresponding A-bit

unchanged. The previous contents of A are lost. The operand "r" is rewritten back into its memory location from the MB register. GNI is produced during T3 and the MEM ⟶ B flip-flops are cleared.

The final operation of the ADD instruction is a carry function between A and B following the BCOA. At TLAST, for any bit of A which is 0 and whose corresponding B-bit is 1, leave that A-bit unchanged and complement the next most-significant (left) bit of A. If the B-bit is 0, leave the corresponding A-bit unchanged and do not complement the next most-significant bit of A. At this point, for any A-bit that changes from 1 to 0 as a result of the carry function, complement the next most-significant bit of A. In the process, if there is a carry out of bit A00, an end-around-carry is produced which causes bit A11 to be complemented, A now contains a+r.

TLAST is generated 0.5 μs after GNI. If the LINC is to continue on, GO will be generated, starting the next instruction. If this is the case, a P ⟶| S occurs, placing p+1 in the S-register. The jam causes p+2 to be left in the P-register, and clears the B-register. The C and MB registers are also cleared at this time.

4.3.2 STC X

At GNI, the A-register contains the value designated "a" and the P-register contains "p." The MEM ⟶ B (SA ⟶ BL ENABLE and SA ⟶ BR ENABLE) flip-flops are cleared. At GO, the pulse P ⟶| S jam-transfers bits P00-P11 (p) into S-register bits S00-S11. Because P-register bits P00 and P01 are permanently cleared, the jam transfer clears S-register bits S00 and S01. The value P+1 is left in the P-register, since a P ⟶| S causes a P+1 ⟶ P. P ⟶| S also clears the B-register. Both MEM ⟶ B flip-flops are set at this time and the C-register is cleared. GO also sets the MEM ⟶ C ENABLE flip-flop, thereby permitting data to be 1s transferred into the C-register from the B-register.

Following GO, the contents (12-bit word) of the memory location specified by the S-register are read from PDP-8 memory into the MB, B-, and C-registers. At T1, the contents of the MB register are written back into the PDP-8 memory location from which they were read. The B-register and MEM ⟶ B flip-flops are cleared.

At T2, the address part of the instruction (bits 2-11) is jam-transferred from C-register bits C02-C11 into S-register bits S02-S11. S00 and S01 are cleared. The contents of the A-register are 1s transferred into the previously cleared B-register. At T3, GNI is produced while the contents of the B-register go into the MB register. From the MB register, this value is written into the PDP-8 memory location specified by the S-register.

TLAST is generated 0.5 μs after GNI. If the LINC is to continue on, GO will be generated, starting the next instruction. If this is the case, a P ⟶| S occurs, placing P+1 in the S-register. The jam transfer causes P+2 to be left in the P-register, and clears the B-register. The C and MB registers are also cleared at this time.

4.3.3 JMP X

At GNI, the P-register contains the value (p). The MEM ⟶ B (SA ⟶ BL ENABLE and SA ⟶ BR ENABLE) flip-flops are cleared. At GO, a P ⟶ S occurs, placing p in the S-register and p+1 in the P-register. The jam transfer clears the B-register. The MEM ⟶ B flip-flops are set at this time and the C-register is cleared. GO sets the MEM ⟶ C ENABLE flip-flop, thereby permitting data to be placed in the C-register.

4.3.3.1 X≠0 - Following GO, the contents of the memory location specified by the S-register are read into the MB, B-, and C-registers. At T1, the MEM ⟶ B flip-flops are cleared. The contents of the MB register are written into the memory location from which they were read. At T2, a B ⟶ P pulse is generated placing X, (bits 2-11 of the JMP instruction) in the P-register, and clearing bits 0-7 of the S-register. A P ⟶ B pulse is also generated at T2 and clears bits 8-11 of the S-register. The MB register is also cleared at this time.

GNI is produced at T3. The contents of the B-register (JMP P+1) are transferred into the MB register and written into memory location 0. TLAST is generated 0.5 μs after GNI. If the LINC is to continue on, GO will be generated, starting the next instruction. If this is the case, a P ⟶ S pulse is generated, thus placing X in the S-register. The jam transfer causes X+1 to be left in the P-register, and clears the B-register. The C and MB registers are also cleared at this time.

4.3.3.2 X=0 - At T1, GNI is produced. The MEM ⟶ B flip-flops and the P-register are cleared. TLAST is generated 0.5 μs after GNI. If the LINC is to continue, GO will occur at TLAST. The contents of the P-register (0) are jam-transferred into the S-register. This operation causes 1 to be left in the P-register, and the next instruction is taken from LINC location 0.

4.4 INDEX-CLASS INSTRUCTIONS

4.4.1 Instruction Format

The iβ class of LINC-8 instructions is organized as follows: bits 0 and 1 are 0 and bit 2 is 1 to specify the iβ instruction class. Bits 3 through 6 select the particular function to be performed such as LDA (load contents of a memory location into the A-register), ADM (add contents of A-register to contents of specified memory location), and STA (store contents of A-register in specified memory location) etc. Bit 7 (i bit) and bits 8 through 11 (β-register bits) of an iβ instruction specify the location of the operand (number to be stored, loaded, added, etc.) according to the sequence described below. The reader should also refer to the LDA instruction description for a complete understanding of the iβ setup.

4.4.1.1 i=0, β=0 - When both i and β are equal to 0, the operand address is taken as the contents of p+1. As an example, if the program counter (P) is at a count of 0020 and if location 0020 contains the instruction LDA, the LINC will interpret the contents of location 0021 as the address of the operand to be loaded into the A-register. Assuming location 0021 contains the address 1234 and location 1234 contains the operand 5555, the A-register will contain 5555 after completion of the instruction LDA.

4.4.1.2 i=1, β=0 - When i=1 and β=0, the operand itself is taken from the memory location immediately following the instruction. Assuming location 0063 contains the instruction LDA i and 0064 contains 3333, the A-register will contain 3333 following the LDA i instruction.

4.4.1.3 i=0, β≠0 - There are 17_8 12-bit β-registers in the LINC. These occupy memory locations 1_8 (0001_2) to 17_8 (1111_2). When i=0 and β equals any number from 1_8 through 17_8, the contents of that β-register specify the address of the operand. Assuming β=13, location 13 contains the address 2122, and location 2122 contains 4444, the A-register will contain 4444 after the completion of LDA 13.

4.4.1.4 i=1, β≠0 - In the case where i=1 and β specifies one of the 17_8 memory locations between 1_8 and 17_8, the LINC will go to the β-register to obtain an address. The address is then incremented by 1 and rewritten into the β location. This incremented address is now taken as the location of the operand. If the same instruction is executed again, the LINC will take the previously incremented address, increment it again by 1, rewrite it into β, and then take the contents of the newly incremented address as the location of the operand. This operation is similar to the autoindexing function of the PDP-8.

The following example illustrates the LINC autoindexing operation. The instruction LDA i 16 is used. In location 16 is the address 3333. Register 3334 contains 5050, register 3335 contains 6060, and register 3336 contains 7070. The first time the LINC encounters LDA i 16, it takes the addresses 3333 and increments it to 3334. The number 3334 is now written into β location 16. The operand 5050 contained in register 3334 is then loaded into the A-register. If the same LDA i 16 instruction is executed again, the LINC again goes to β-register 16 for the address of an operand. This second time the LINC finds the number 3334 in β-register 16. This number is incremented to 3335 and the new number 3335 is written into location 16. The LINC now takes the content of location 3335 (operand 6060) and loads it into the A-register. The A-register now contains 6060 after the second execution of LDA i 16.

If LDA i 16 is repeated for the third time in the same program, the LINC goes to β-register 16, and finds the address 3335. This is incremented to 3336 and 3336 is written into location 16. The contents of address 3336 (operand 7070) are loaded into the A-register.

4.4.2 LDA iβ

4.4.2.1 LDA (i=0, β=0) - Prior to T1, standard operations place the LDA instruction in the MB, B-, and C-registers. The remaining operations depend upon the value of i and β.

At T2, the contents of the P-register (P+1), are jam transferred into the S-register for addressing memory. The P ⊣▶ S pulse adds 1 to the contents of the P-register incrementing it to P+2, and the B-register is cleared. The MB register is also cleared. Following T2, the PDP-8 memory location specified by the S-register is read into the MB and B-registers as the value Y.

At T3, the data held in the MB register is written back into the memory location from which it was obtained. The B-register contains the address of the operand. The timing generator is advanced to T10.

At T10, the A and MB registers are cleared. The value Y, held in the B-register, is jam transferred into the S-register. The B-register is cleared. Following T10, the operand is transferred from memory location Y into the previously cleared MB and B-registers.

At T11, r is written back into memory from the MB register. A BCOA operation occurs between the A- and B-registers. Since A was previously cleared, r is simply 1s transferred into the A-register. The GNI pulse is now produced.

TLAST is the next timing pulse. If the LINC is to continue on, GO will be produced to clear the C-register, set the MEM ⟶ B flip-flops and start the next instruction. If this is the case, the P ⊣▶ S pulse is generated thus placing (P+1) in the P-register. The jam transfer increments the P-register to P+2, and clears the B-register. The C and MB registers are also cleared at this time.

4.4.2.2 LDA (i=0, β≠0) - LDA β is in the C-register at T1. At T2, the β portion of the instruction is jam-transferred from C-register bits C08 through C11 into S-register bits S08 through S11 by the β ⊣▶ S pulse which also clears the B-register. S00 through S07 are cleared. Following T2, the contents of the memory location specified by the value in the S-register are read into the MB and B-registers.

The contents of the β-register are read into the MB and B-registers. The contents of the MB register are then written back into the memory location from which they were obtained. At T3, the time pulse distributor is advanced to T10. The A-register is cleared. A B ⊣▶ S operation takes place which, in turn, clears the B-register. After T10, r is read from memory into the MB and B-registers.

GNI is produced at T11. A BCOA operation between the B-register and the cleared A-register places r into the A-register. At TLAST, if the LINC is to continue on, GO is produced. A P ⊣▶ S pulse is also generated to place p+1 into the S-register. The jam transfer produces a P+1 ⟶ P with the result that P+2 is now in the P-register, and also clears the B-register. GO sets the MEM ⟶ B flip-flops and clears the C-register.

4.4.2.3 LDA (i=1, β=0) - With the i bit set to 1 and β equal to 0, the timing generator jumps from T1 to T10, bypassing T2 through T7. At T10, a P→S occurs, placing P+1 in the S-register, incrementing the P-register by 1, and clearing the B-register.

The operand r is ls transferred from the memory location specified by the S-register into the previously cleared MB and B-registers.

At T11, GNI is produced. A BCOA operation occurs between the A- and B-registers, and, since the A-register was previously cleared, the contents of the B-register are simply placed in the A-register.

GO is produced at TLAST if the LINC is to continue on. Assuming such is the case, standard end-of-instruction operations take place.

4.4.2.4 LDA (i=1, β≠0) - As with previous forms of LDA, the instruction is in the C-register at T1. At T2, since β≠0, the β-portion of the instruction is jam-transferred into S-register flip-flops S08 through S11. The jam transfer clears the B-register, and also clears S00 through S07.

Following T2, the memory location specified by the S-register is read into the MB and B-registers. At T3, the contents of both the MB and B-registers are incremented by 1. This is accomplished by complementing the least-significant flip-flops of each register (B11 and MB11). Any carries out of B11 and MB11 will be propagated to B10 and MB10, and so forth, down the line to B02 and MB02.

At T10, the incremented contents of the B-register go into the S-register to address memory, and both the A- and B-registers are cleared. Following T10, the operand contained in the memory location specified by the S-register is read into the B-register. The operand is then written back into the PDP-8 memory location from which it was obtained. At T11, the MEM→B flip-flops are cleared and a BCOA operation places operand "r" into the A-register. Standard operations occur at TLAST if the LINC is to continue. GO is also generated at this time.

4.4.3 STA iβ

Standard operations that occur prior to T1 read the STA instruction into the MB, B-, and C-registers. The operations that take place at T2 are dependent on the value of β. If β=0, the contents of the P-register are jam-transferred into the S-register and the P-register is incremented by 1. If β≠0, the β portion of the instruction, held in C-register bits C08 through C11, is jam-transferred in S08 through S11. S00 through S07 are cleared. PDP-8 memory is addressed by the S-register following T2. The address (Y) selected to receive the operand (a) is read into the MB and B-registers from the address specified by the S-register. At T3 if i=1, Y is incremented by 1. After T3, the contents of the MB register are written into the memory location specified by the S-register.

The time pulse distributor is advanced to T10. The functions that take place at T10 are dependent on the iβ configuration. If i=1 and β=0, the P-register jam-transferred into the S-register, the P-register is incremented by 1, and the B-register is cleared. For all other conditions of i and β, the B-register is jam-transferred into the S-register and then the B-register is cleared.

At T11, the contents (a) of the A-register are 1s transferred into the previously cleared B-register. At T12, the PDP-8 memory is in a write cycle. GNI is generated at T13. The value "a" is written into the MB register and into the memory location specified by the S-register. If the LINC is to continue on, GO will be produced at TLAST. At this time, the contents of the P-register are jam-transferred into the S-register, the P-register is incremented by 1, the B- and C-registers are cleared, and the MEM ⟶ B flip-flops are set.

4.4.4 ADA iβ

Standard operations that occur prior to T1 read the ADA instruction into the C-register. No operations occur at T1 unless i=1 and β=0, in which case the time pulse distributor is advanced to T10. At T2, if β=0 the contents of the P-register are jam-transferred into the S-register, the P-register is incremented by 1, and the B-register is cleared. If β≠0, the β portion of the instruction is jam-transferred into the S-register. Following T2, the memory location specified by the S-register is read into the MB and B-registers.

At T3, if i=1, the MB and B-registers are indexed. The contents of the MB registers are written back into the memory location from which they were obtained. The time pulse distributor is advanced to T10. The functions that take place at T10 are dependent on the iβ configuration. If i=1 and β=0, the P-register is jam-transferred into the S-register, the P-register is incremented by 1, and the B-register is cleared. For all other conditions of i and β, the B-register is jam-transferred into the S-register and then the B-register is cleared.

Following T10, the memory location specified by the S-register is read into the B and MB registers. At T11, GNI is produced. The MB register writes its contents back into the memory location from which they were obtained. The remaining functions of the ADA instruction include a BCOA operation and carry function as presented in the ADD instruction description in Section 4.3.1. BCOA occurs at T11 and CARRY occurs at TLAST.

4.4.5 ADM iβ

Standard operations that occur prior to T1 read the ADM instruction into the C-register. No operations occur at T1, unless i=1 and β=0, in which case the time pulse distributor is advanced to T10. At T2, if β=0, the contents of the P-register are jam-transferred into the S-register, the P-register is

incremented by 1, and the B-register is cleared. If $\beta \neq 0$, the β portion of the instruction is jam-transferred into the S-register. Following T2, the memory location specified by the S-register is read into the MB and B-registers.

At T3, if i=1, the MB and B-registers are indexed. The contents of the MB register are written back into the memory location from which they were obtained.

The time pulse distributor is advanced to T10. The functions that take place at T10 are dependent on the iβ configuration. If i=1 and β=0, the P-register jam-transferred into the S-register, the P-register is incremented by 1, and the B-register cleared. For all other conditions of i and β, the B-register is jam-transferred into the S-register and then the B-register is cleared.

Following T10, the contents of the memory location specified by the S-register are read into the MB and B-registers. The value is designated as "r". The contents of the MB register are written into the memory location from which they were obtained. At T11, a BCOA (see Section 4.3.1) operation occurs between the A-register which contains a, and the B-register which contains r. At T12 a CARRY pulse is generated which completes the addition of the A- and B-registers into the A-register (a + r).

The result, a+r, is left in the A-register. Both the B and MB registers are cleared at T12. At T13, the contents of A (a + r) is 1s transferred into the previously cleared B-register. The A-register also maintains this value. At T12, the MB register is cleared. The WRITE flip-flop is set at T13. This requests the next memory cycle to be a WRITE cycle.

At T15, the value a+r is read from B into the MB register and then written into the memory location from which r was obtained. a+r also resides in memory and in both the A- and B-registers. The next time pulse, TLAST, will produce GO if the LINC is to continue on.

4.4.6 LAM iβ

Addition using the LAM instruction involves the A- and B-registers, and the Link flip-flop. With LAM, a carry-out of bit A00 is saved in the Link bit; it is not added to bit 11 of the A-register.

When LAM is executed and the Link is 0, the A-register and the memory operand register will contain A + B + 0 (content of Link). If an end carry results from the addition of A + B + 0, the LINK is set to 1; otherwise it remains in the 0-state.

If the Link is in the 1-state when LAM is executed, the A-register and the memory operand register will contain A + B + 1 (content of Link). In the case where an end carry results from the addition of A + B + C (L), the Link flip-flop is set; otherwise it will be cleared.

Functionally, the operation of LAM is identical to that of the ADM instruction with the exception of the Link flip-flop and end-carry functions.

At T12, the content of the Link (1 or 0) is added to bit 11 of the A-register as described above. If an end carry is produced as a result of the addition, the Link is set at T12, at which time the B-register is also cleared.

At T13, the contents of A are 1s transferred into the B-register. Data from the MB register is inhibited from entering the B-register, since the MEM ⟶ B flip-flops were cleared at T11. At T14, nothing of significance occurs; however, at T15, the value a + r + Link is written into the memory location from which r was originally obtained. GNI and GO start operation of the following instruction at T15 and TLAST.

4.4.7 MUL iβ

MUL iβ directs the LINC to multiply the contents of the A-register (multiplicand) by the contents of a specified memory register (multiplier). The address of the memory register containing the multiplier is obtained through the standard iβ instruction setup. Bit 0 of this address is defined as the h-bit and indicates the following: if h=0, both the multiplicand and multiplier are taken as integers with their binary points placed to the right of bit 11. If h=1, both numbers are considered fractions with their binary points assumed to be between bit 0 and bit 1. In the special case where i=1 and β=0, the location immediately following the MUL i instruction is the operand. There is no h-bit in this case since there is no operand address involved; therefore, the LINC assumes that h is equal to 0 and treats both the multiplicand and multiplier as integers. Bit 0 of both the multiplicand and multiplier specify the sign of that particular number. A positive number is indicated by bit 0=0, while bit 0=1 indicates a negative value.

Standard iβ functions occur during GNI, GO, T1, T2, and T3. At T4, the S-register receives address information from either the P- or B-register according to the iβ setup. Also at T4, the binary 0 or 1 residing in bit 0 of the multiplicand (A) goes into the LINK flip-flop. This bit specifies the sign of the multiplicand in the A-register. The Z, B, and MB registers are cleared and, following T4, the 11-bit multiplier (r) and sign bit is transferred from memory into the B-register.

At T5, bits 8 through 11 of the C-register are cleared by the command 0 ⟶ N. Also, if bit 0 of the A-register is 0, specifying a positive multiplicand, the value in A is unchanged. If bit 0 is 1, a negative number is indicated, therefore, the A-register is complemented to designate the absolute value. The same process is used for the multiplier in the B-register. If bit 0=0, the values in B and the link flip-flop are unchanged, while bit 0=1 complements the value in B and in the LINK flip-flop. Thus the LINK holds the sign of the product. Finally, at T5 the MEM ⟶ B flip-flops are cleared

to gate off any additional information from entering the B-register from memory. Following T5, the B-register contains the absolute value of the multiplier ($|r|$) and the A-register contains the absolute value of the multiplicand ($|a|$).

When T6 is generated, the multiplier $|r|$ is 1s transferred from the B-register into the Z-register, B is cleared at T7, and the multiplicand $|a|$ is 1s transferred from A to B. At T10 when N is still equal to 0, bit location 11 of the Z-register is examined. If Z11=0, nothing of significance occurs at T10 or T11. If Z11=1, a BCOA takes place between the B- and A-registers (see BCOA description in Section 4.3.1), and at T11, the CARRY function is generated. The above operations add the contents of B to the A-register.

The contents of both the A- and Z-registers are shifted right 1 place at T12. Bit A11 goes into Z0; Z11 is lost and is replaced by bit Z10. N is decremented by 1 to the value 17 and the time pulse distributor is set to 10. With N equal to 17, bit position Z11 (now containing Z10) is again examined. If Z11=0, the previous contents of A are not affected. If Z11=1, another BCOA and CARRY operation takes place thus adding the value in B to the current value in A. At T12, A and Z are shifted right one place, N-1⟶N sets N equal to 16, and the time pulse distributor goes back to T10. Bit Z9 is now evaluated by the LINC-8. The above process continues until N=6.

With N=6, 11 shift operations have resulted in the evaluation of all bits of Z. At T12 with N=6, N is decremented to 5 and now the h-bit is examined to determine whether integer or fractional multiplication is being executed. If integers are specified (h=0), the signal Z⟶A is produced which transfers the contents of Z- into the A-register. At T11 with h=0, the contents of A are shifted right one place thus placing the 11 least-significant bits of the product in A1 through A11. At T12, N is decremented to 4, while the time pulse distributor is set back to T10. If fractional multiplication is indicated (h=1), the A-register is left as it was with the 11 most-significant bits of the product in bits A1 through A11.

At T10 with N=4, the state of the LINK flip-flop is examined. If it is 0, nothing of significance occurs; however, if the link bit is 1, the value in the A-register is complemented. This operation assigns the correct sign to the resultant answer in the A-register. GNI is generated at T11 to start execution of the following instruction.

4.4.8 SAE iβ

Standard operations that occur prior to T1 place the SAE instruction into the C-register. No operations occur at T1 unless i=1 and β=0, in which case the time pulse distributor is advanced to T10. At T2, if β=0, the contents of the P-register are jam-transferred into the S-register, causing the P-register to be incremented by 1 and clearing the B-register. If $\beta \neq 0$, the β portion of the instruction is jam transferred into the S-register. Following T2, the memory location specified by the S-register is read into the MB and B-registers.

At T3, if i=1, the MB and B-registers are indexed. The contents of the MB register are written back into the memory location from which they were obtained.

The time pulse distributor is advanced to T10. The functions that take place at T10 are dependent on the iβ configuration. If i=1 and β=0, the P-register jam-transferred into the S-register, the P-register is incremented by 1, and the B-register is cleared. For all other conditions of i and β, the B-register is jam-transferred into the S-register and then the B-register is cleared.

Following T10, the memory location specified by the S-register is read into the B- and MB registers.

At T11, the contents of the MB register are written back into the memory location from which they were obtained. At T12, a BCOA operation occurs between the A- and B-registers, the result being left in the A-register. This resultant will be 0 if the initial contents of the A- and B-registers were equal.

Following T12, the same memory location is again read into the B and MB registers. At T13, the contents of the MB register are written back into the memory location from which they were obtained. Also at T13, if the contents of the A-register are 0 following the BCOA at T12, the P-register is incremented by 1. The P-register is not incremented if the contents of the A-register do not equal 0. A second BCOA at T13 leaves the A-register as it was before T12.

TLAST is generated 0.5 μs after GNI. If the LINC is to continue on, GO will be generated, starting the next instruction. Assuming this is the case, a P ⊣▸ S pulse is generated, placing P+1 in the S-register and leaving P+2 in the P-register. The B, C, and MB registers are also cleared at this time. If the P-register was incremented at T13, then the P ⊣▸ S function causes the LINC to skip the next sequential instruction.

4.4.9 SRO iβ

Standard operations that occur prior to T1 place the SRO instruction into the C-register. No operations occur at T1 unless i=1 and β=0, in which case the time pulse distributor is advanced to T10. At T2, if β=0, P ⊣▸ S, causing the P-register to be incremented by 1 and clearing the B-register. If β≠0, the β portion of the instruction is jammed into the S-register. Following T2, the memory location specified by the S-register is read into the MB and B-registers.

At T3, if i=1, the MB and B-registers are indexed. The contents of the MB register are written back into the memory location from which they were obtained.

The time pulse distributor is advanced to T10. The functions that take place at T10 are dependent on the iβ configuration. If i=1 and β=0, the P-register jam-transferred into the S-register, the P-register is incremented by 1, and the B-register is cleared. For all other conditions of i and β, the B-register is jam-transferred into the S-register and then the B-register is cleared.

Following T10, the memory location specified by the S-register is read into the B-register and MB registers.

At T11, the contents of the MB register are written back into the memory location from which they were obtained. At T12, if bit B11 contains 0, the P-register is incremented by 1 and the B-register is rotated one place to the right. If B11 = 1 at T12, the B-register is rotated one place to the right but the P-register is not incremented. At T13, the contents of the B-register are written into the memory location specified by the S-register. The MEM ⟶ B flip-flops are cleared at this time.

TLAST is the next time pulse. If the LINC is to continue on, the GO pulse will be produced in coincidence with TLAST. GO generates a P ⟶ S pulse which in turn produces a p+1 pulse that increments the P-register by 1. The C, B, and MB registers are cleared and the MEM ⟶ B flip-flops are set.

4.4.10 BCL iβ

Standard operations that occur prior to T1 place the BCL instruction into the C-register. No operations occur at T1 unless i=1 and β=0, in which case the time pulse distributor is advanced to T10. At T2, if β=0, the contents of the P-register are jam-transferred into the S-register, causing the P-register to be incremented by 1 and clearing the B-register. If β≠0, the β portion of the instruction is jam-transferred into the S-register. Following T2, the memory location specified by the S-register is read into the MB and B-registers.

At T3, if i=1, the MB and B-registers are indexed. The contents of the MB register are written back into the memory location from which they were obtained.

The time pulse distributor is advanced to T10. The functions that take place at T10 are dependent on the iβ configuration. If i=1 and β=0, the P-register jam-transferred into the S-register, the P-register is incremented by 1, and the B-register is cleared. For all other conditions of i and β, the B-register is jam-transferred into the S-register and then the B-register is cleared.

Following T10, the memory location specified by the S-register is read, placing r in the B and MB registers. At T11, the contents of the MB register are written back into the memory location from which they were obtained. The B-register is complemented, yielding $\bar{r}$. The GNI pulse clears the MEM ⟶ B flip-flops.

AT TLAST, a BCLA (AND with 0s) operation occurs between the A- and B-registers. For each bit of the B-register that contains 1, corresponding A-register bit is cleared. If the B-register bit is 0, the corresponding A-register bit is not changed. Assuming the LINC is to continue on, standard end of instruction operations take place.

4.4.11 BSE iβ

Standard operations that occur prior to T1 read the BSE instruction into the C-register. No operations occur at T1 unless i=1 and β=0, in which case the time pulse distributor is advanced to T10. At T2, if β=0, the contents of the P-register are jam-transferred into the S-register, causing the P-register to be incremented by 1 and clearing the B-register. If β≠0, the β portion of the instruction is jammed into the S-register. Following T2, the memory location specified by the S-register is read into the MB and B-registers.

At T3, if i=1, the MB and B-registers are indexed. The contents of the MB register are written back into the memory location from which they were obtained.

The time pulse distributor is advanced to T10. The functions that take place at T10 are dependent on the iβ configuration. If i=1 and β=0, the P-register jam-transferred into the S-register, the P-register is incremented by 1, and the B-register is cleared. For all other conditions of i and β, the B-register is jam-transferred into the S-register and then the B-register is cleared.

Following T10, the memory location specified by the S-register is read into the B and MB registers. This places r in the MB and B-registers. Prior to this, the A-register contained a. At T11, GNI is produced, clearing the MEM ⟶ B flip-flops. An inclusive OR operation occurs between the A- and B-registers. For each bit of A that is 1, set the corresponding bit of the B-register to 1. Otherwise keep the value of the B-bit. The result of the operation is placed in the B-register. The A-register is cleared.

At TLAST, a BCOA operation occurs between the A- and B-registers. Because the A-register was cleared at T11, the contents of the B-register are simply read into the A-register. If the LINC is to go on, GO will be produced which causes a P⟶J⟶S, sets the MEM ⟶ B flip-flops, and clears the C-register. The P⟶J⟶S adds 1 to the P-register and clears the B-register. The MB register is also cleared.

4.4.12 BCO iβ

Standard operations that occur prior to T1 read the BCO instruction into the C-register. No operations occur at T1 unless i=1 and β=0, in which case the time pulse distributor is advanced to T10. At T2, if β=0, the contents of the P-register are jam-transferred into the S-register, causing the P-register to be incremented by 1 and clearing the B-register. If β≠0, the β portion of the instruction is jam-transferred into the S-register. Following T2, the memory location specified by the S-register is read into the MB and B-registers.

At T3, if i=1, the MB and B-registers are indexed. The contents of the MB register are written back into the memory location from which they were obtained.

The time pulse distributor is advanced to T10. The functions that take place at T10 are dependent on the iβ configuration. If i=1 and β=0, the P-register jam-transferred into the S-register, the P-register is incremented by 1, and the B-register is cleared. For all other conditions of i and β, the B-register is jam-transferred into the S-register and then the B-register is cleared.

Following T10, the memory location specified by the S-register is read into the B and BM registers.

The memory read places the value r in the B and MB registers. At T11, GNI is produced. A BCOA (exclusive OR) operation occurs between the A- and B-registers. For each bit of B that is 1, complement the corresponding A-bit. For any B-bit that is 0, leave the corresponding A-bit unchanged. The GNI pulse clears the MEM ⟶ B flip-flops.

GO will be produced with TLAST if the LINC is to continue on. If such is the case, standard end-of-instruction operations take place.

4.4.13 DSC iβ

The DSC iβ instruction intensifies points within a 2 (horizontal) by 6 (vertical) grid on the display oscilloscope according to the bit configuration of a selected 12-bit operand. The location of this operand is determined through the standard iβ instruction format. Once the operand is obtained, each bit controls one of the 12 specific locations within the intensification grid. If a particular bit is 0, the corresponding grid point is not intensified; conversely, if a bit is 1, the associated point is intensified. The relationship between grid points and operand bits is shown in Figure 4-1.

POINT 6 (BIT 6)	POINT 12 (BIT 0)
POINT 5 (BIT 7)	POINT 11 (BIT 1)
POINT 4 (BIT 8)	POINT 10 (BIT 2)
POINT 3 (BIT 9)	POINT 9 (BIT 3)
POINT 2 (BIT 10)	POINT 8 (BIT 4)
POINT 1 (BIT 11)	POINT 7 (BIT 5)

Figure 4-1 Bit Positions of DSC Instruction

Assuming bits 0 through 5 of the operand are 0, and bits 6 through 11 are 1, the entire vertical column of points 1 through 6 would be intensified, thereby producing a small straight vertical line on the display oscilloscope. If bits 5 and 11 are 1 and the remaining bits (0 through 4 and 6 through 10) are 0, display points 1 and 7 would be intensified. By programming two consecutive DSC instructions, a second 2 by 6 grid can be displayed to the right of the first, thus producing a 4 by 6 overall grid. Through proper selection of operands, the combined grids can display letters of the alphabet, numbers, and symbols meaningful to users of the LINC-8. Additional information concerning the use of the DSC instruction can be found in Programming The LINC-8.

In the DSC instruction, the horizontal coordinate of display point 1 (Figure 4-1) and the horizontal movement of points is controlled by the B-register. The vertical coordinate of each display point is determined by bits 3 through 11 of the A-register with bits 7 through 11 set to 0. The intensification of each operand bit (on or off) is controlled by the Z-register. The intensification word is the operand obtained through the standard iβ instruction format. The major difference in the way this instruction obtains the operand is that the time pulse distributor does not jump from T1 or T3 to T10 as in other iβ instructions. It will skip from T1 to T4 when i=1 and β=0. The horizontal coordinate of the display character is stored in memory location 0001. In addition, bit 0 (h-bit) of register 001 specifies one of two display channels: if h=0; display channel 0 is selected; if h=1, channel 1 is selected. In the case where i=1 and β=0, display channel 0 is used only.

This description will commence with pulse T4, at which time the Z-register is cleared, address information is being jam-transferred into S from either P or B, and the MB and B-registers are cleared. Following T4, the sense amplifiers read out of the memory location specified by S into the B-register. This 12-bit word (r) will control the intensification (on or off) of each point in the 2 by 6 display grid. At T5, r is rewritten back into memory while bits 8 through 11 of the C-register are cleared by the signal $0 \longrightarrow N$. At T5, the pulse $10 \longrightarrow T$ causes T_6 and T_7 to be skipped. C-register flip-flops C08 through C11 comprise a 4-bit down counter. Output levels of the counter are decoded into the signals N=0 through N-17 which control various functions associated with the DSC instruction. The counter is initially cleared at T5 by the signal $0 \longrightarrow N$ and is decremented by 1 each time the signal $N-1 \longrightarrow N$ is generated. Functions that occur during each value of N are shown in tabular form on the DSC instruction timing diagram.

At T10, the operand in the B-register (the intensification word) is ls transferred into the Z-register and B is cleared. The S-register is set to 0001. Following T10, the sense amplifiers read out of memory location 0001 into the B-register. The contents of location 0001 plus 4 will be the horizontal starting location of grid point 1. The A-register contains the vertical starting location (bits A0 through A2 are not decoded; bits A3 through A6 specify the vertical coordinate; bits A7 through A11 will be cleared at T15), and the Z-register contains the intensification operand. Finally the $MEM \longrightarrow B$ flip-flops are cleared at T11.

The horizontal, vertical, and intensification levels remain in their respective registers at T12, T13, and T14 to allow settling time for the D-A circuits associated with the display oscilloscope. At T15, the following occur: with N=0, the time pulse distributor is reset to T10; N is decremented to 17; bits A7 through A11 are cleared; and the number in the B-register (horizontal coordinate minus 4) is incremented by 4. The A- and B-registers now specify the exact location of display point 1.

The time pulse distributor is now recycling from T10 to T15, with N equal to 17, the distributor again goes back to T10 and the pulse N-1 ⟶ N decrements N to 16. As the distributor reaches T15 with N=16, the distributor is again set back to T10 while the following occurs as indicated by the symbol ② on the timing diagram: bit Z11 is examined to determine if it is 1 or 0. If Z11 is 1, an ONINT (on intensity) pulse turns on the display oscilloscope for either channel 0 or channel 1, depending on the h-bit, and grid point 1 is intensified. Bit Z11 is now cleared. The pulse 10 ⟶ T causes the time pulse distributor to recycle from T10 to T15 with N still equal to 16. Grid point 1 remains displayed.

At T15, with bit Z11 now cleared, or in the event that Z11 was initially a 0, the following events occur. The OFFINT (off intensity) pulse is generated which disables the intensification level at the oscilloscope, thus grid point 1 is turned off or not intensified. The value in the A-register is incremented by 4, N is decremented to 15, and the contents of the Z-register are shifted right 1 place. Bit Z11 is lost and Z10 now occupies the location previously held by Z11.

When the distributor reaches T15 with N equal to 15, the operations specified by ② are repeated. Bit location Z11, which now contains Z10 due to the previous shift right of the Z-register is examined. If a 1 is found, the ONINT level intensifies grid point 2 for channel 0 or 1. The A-register was previously incremented by four, thus selecting point 2. Again, bit location Z11 (containing the previous Z10) is cleared. If the bit in location Z11 is 0, OFFINT is produced and grid point 2 is not intensified. The A-register is again incremented by 4 to select grid point 9; N is decremented to 14; and the contents of Z are shifted right 1 place. Bit Z10 is lost and Z9 now occupies the position originally held by Z11 (right-most position).

The shifting of Z-bits to the right and the incrementing of the A-register by four will continue until bit Z6 has been evaluated for either an ONINT or OFFINT level. N is now equal to 11, and the functions indicated by ③ on the timing diagram occur: Z6 is cleared following its evaluation; bits A7 through A11 are cleared; and the horizontal coordinate value in B is incremented by four. Grid point 5 is now selected by the A- and B-registers for evaluation. The time pulse distributor is set to T10.

A second column of display points (point 7 through point 12) is plotted in the same manner as the first. The time pulse distributor continues to recycle from T10 to T15 and the Z-register bits associated with specific grid points are shifted right for evaluation while occupying position Z11. When the value N is decremented to 0001, SETWR (set write) and GNI (get next instruction) are generated

in preparation for the following instruction. SETWR causes the value in the B-register (horizontal coordinate of grid points 0 through 5) to be stored into memory at T15 when N=01. In the event that the next instruction is a DSC to display another 2 by 6 matrix alongside the first, the combined instructions produce a 4 by 6 matrix. Bits A5 through A11 are cleared so that grid point 1 of the second 2 by 6 matrix is displayed alongside the first.

4.5 ALPHA CLASS INSTRUCTIONS

4.5.1 SET iα

Standard operations that occur prior to T1 read the SET instruction into the C-register. No operations occur at T1 unless i=1, in which case the time pulse distributor is set to T10.

Assuming i=0, T2 is the next time pulse. At this time, the contents of the P-register are jam-transferred into the S-register, placing p+1 in the S-register, p+2 in the P-register, and clearing the B-register. After T2, the contents of the memory location specified by the S-register are read into the MB and B-registers. At T3, the contents are written back into the memory location from which they were obtained. The time pulse distributor is advanced to T10.

At T10, if i=1, the contents of the P-register are jam-transferred into the S-register, placing P+2 into the S-register. The P-register is incremented by 1, and the B-register is cleared. If i=0, the contents of B are jam-transferred to S and the B-register is cleared. Following T10, the contents of the memory location specified by the S-register are read into the MB and B-registers. At T11, the contents of this location are written back into memory and the WRITE flip-flop is set.

At T12, the contents of C08 through C11 (α) are jam-transferred into bits S08 through S11, thereby writing the contents of B into the location specified by S.

At T13, GNI is produced. The value held in the B-register goes into the MB register and memory. At TLAST, GO will be produced if the LINC is to continue, in which case a P→→S occurs, placing p+2 in the S-register. P+3 goes into the P-register and the B- and C-registers are cleared.

4.5.2 DIS iα

This instruction displays a point on the oscilloscope whose vertical coordinate is specified by the right-most nine bits of the A-register. The horizontal coordinate is specified by the right-most nine bits of the contents of the register selected by α ($0 \leq \alpha \leq 17$). The left-most bit of the contents of register α specifies one of two display channels (further selected by a switch on the display scope). The left-most horizontal coordinate is 000; the right-most, 777_8. The lowest vertical coordinate is -377_8; the highest, $+377_8$. The contents of bits 0 through 2 of the A-register and of the contents of the α-register do not affect the position of the point.

Standard LINC-8 register functions during GNI, GO, and T1 place the DIS instruction into the C-register. At T2, the MB and B-registers are cleared at the right-most four bits (α) of the instruction are jam-transferred into the S-register. The value α can be used to select any LINC-8 register from 0 through 17_8. Following T2, the sense amplifiers read out of the memory location specified by α into the MB and B-registers. The A-register still contains the value y, which specifies the vertical position of the display point.

At T3 the MEM ⟶ B flip-flops are cleared. If bit 7 (i bit) of the instruction is a 1, the contents of the MB and B-registers specified by α are indexed by 1. This incremented value is rewritten into the memory location specified by α. If i=0, the contents are not indexed before being written back into memory. At T3 and T4, the B-register contains a value which specifies the horizontal position of the display point, while the vertical position is specified by the contents of the A-register. The MB register is cleared at T4. Following T4, the sense amplifiers read out of the α-register into the MB register. The information is then written back into the α-register. The information does not enter the B-register, however, since the MEM ⟶ B flip-flops were cleared at T3.

Bits 8 through 11 of the C-register are cleared at T5 by the signal 0 ⟶ N. During T6 through T17, the D-to-A converters in the LINC-8 Display System settle. At T17 since N=0, the following occur: bits 8 through 11 (N bits) are decremented to 1111_2 (17_8) by the pulse N-1 ⟶ N. An on intensity pulse (ONINT0 or ONINT1) is generated, thus intensifying the point on the oscilloscope screen, and the time pulse distributor is set to 10. ONINT0 will be produced if the h-bit (bit 0 of the word currently in the B-register) is 0, ONINT1 will be produced if h=1.

As the time pulse distributor continues to cycle from T10 through T17, the intensification level determined by the intensification flip-flop in the LINC Scope PLUG IN remains on. At T17, since N is now equal to 17, the OFF INT pulse is generated. This turns off the intensification. The LINC continues to TLAST and GO which initiate the next instruction if the LINC section is to continue. By writing the DIS iα instruction with the i bit = 1 in a repeated program loop, a horizontal line will be displayed on the oscilloscope. The line is actually comprised of a series of points which are generated in the horizontal direction each time the contents of the B-register are incremented by 1 at T3.

4.5.3 XSK iα

If the contents of the right-most 10-bits of the α-register ($0 \leq \alpha \leq 17$) equals 1777, skip the next register in the instruction sequence; otherwise, execute the next instruction in sequence. If i=1, the address part of the α-register is first indexed by 1, using 10-bit binary addition without end carry. The left-most two bits are unchanged. Thus, 1777 is indexed to 0000; 3777 to 2000; 5777 to 4000; and 7777 to 6000.

The standard sequence of events during GNI, GO, and T1 place the XSK instruction into the C-register. At T2, the MB and B-register are cleared, and bits C08 through C11 (α) of the instruction are jam-transferred into the S-register to select the contents of an address for reading into the MB and B-registers. At T3, this number in the MB and B-registers is left unchanged if i=0, and is incremented by 1 in both registers, if i=1. Following T4, the PDP-8 reads out of memory into the MB register but not into the B-register, since the MEM ⟶ B flip-flops were cleared at T3.

At T5, if bits B02 through B11 contain 1777, the P-register is incremented by 1 and the LINC-8 skips the next instruction in the program. If the count is not equal to 1777, the P-register is not incremented and the next instruction in the sequence is executed. Assuming that i=1, the value in the B-register will be incremented by 1 each time the instruction is repeated.

4.5.4 SAM iα

One feature of the LINC-8 Analog-to-Digital system (Section 3.6) is a sample-and-hold operation which allows adequate statistical representation of high frequency analog data. The SAM instruction samples 1 of 16 input channels and converts the analog voltage on this channel to a binary number in the A-register by using the successive approximation technique. Bit A3 specifies the sign (+ or -), while bits A4 through A11 specify the magnitude (000 through 377_8) of the analog input. Bits A0, A1, and A2 assume the same value as bit A3 (sign bit).

The standard LINC-8 is supplied with 16 analog input channels. In the standard configuration, bit 7 (i bit) of the SAM instruction has no affect; bits 8 through 11 select 1 of 16 inputs. When a LINC-8 is equipped with 32 analog input channels (16 standard, 16 optional), the i bit selects the particular group of 16 channels in which the desired channel is located. Bits 8 through 11 then specify one of the 16 analog channels in the group selected by the i bit.

Many of the functions shown on the SAM instruction timing diagram should be familiar through comparison with other LINC instructions. One exception, however, is the HOLD SAMPLE level which starts out positive (ground), goes negative (-3V) for the time following MEM STROBE until T3, goes positive again at T3, and remains positive throughout the duration of the SAM instruction. The time that the HOLD SAMPLE level remains at -3V is defined as the "aperture time" and its duration is approximately 2 μs. During GNI and GO times, standard LINC-8 register operations occur and the HOLD SAMPLE level is at ground. Following GO, the SAM instruction is read out of PDP-8 memory into the LINC-8 register and the C-register. Bits 8 through 11 and the i-bit (32 channel operation) are decoded to turn on a particular analog input channel. At this time, the HOLD SAMPLE level goes to -3V, thus allowing the analog input signal to start charging the hold capacitor in the sample-and-hold circuit.

At T3, the sample time is completed thus closing the aperture and the sample and hold starts holding. The MEM ⟶B flip-flops are cleared at T3 to disable memory data from entering the B-register. At T4, the MB, B-, and A-registers are cleared. Of special importance is the clearing of the A-register which causes the A-to-D comparison circuit to select a mid-scale value of 0V (+1 to -1). At this point, the comparison between the analog input and the reference voltage has already started. When this first comparison is complete, the A-to-D circuit will establish whether the analog input is positive (0 to +1V) or negative 0 to -1V). At T5, bits 8 through 11 of the C-register (N down counter) are cleared to 0000.

At T6, bit B03 is set to 1 by the signal 1 ⟶B3. The B-register serves as a pointer to select one A-register bit at a time for evaluation. Nothing of significance occurs at T7 and T10; however, at T11, the value in the A-register (midscale) and the output of the sample circuit are compared by the CVTPLS pulse. If the analog sample voltage is more positive than the A-to-D reference, bit A03 is left in the 0-state. If the analog voltage is more negative than 0V, bit A03 is set to 1. Thus, the first successive approximation starting with bit A03 is complete. The 1 in bit B03 is now rotated into B04 by the ROTB pulse to establish the evaluation of bit A04; A04 is set to 1. Finally, at T11, the time pulse distributor is set back to T10 and N is decremented to 17 (1111). Nothing of significance occurs at T10 this second time. At T11, with B04 set, bit A04 is evaluated in a manner similar to that used to evaluate A03. If the analog-sample voltage is more positive than the reference-ladder output voltage, bit A04 is left in the 1-state. If the analog voltage is more negative, A04 is cleared. During this second comparison, CVTPLS sets bits A00, A01, and A02 if bit A03 is set to 1. The 1 in bit B04 is now rotated into B05, and N is decremented to 16 (1110) to evaluate A04, and A05 may be set to 1. The time counter is set to T10.

The cycle at T10 and T11 will continue until N is equal to 10 (1000). At this point, bit A11 is being evaluated to complete the A to D conversion of the analog voltage. GNI is generated to start the next instruction and the A-register now contains a 12-bit digital word corresponding to the analog input converted to an accuracy of 9 bits.

4.6 SHIFT INSTRUCTIONS

4.6.1 ROL i N

ROL i N is a shift class instruction containing two variables, i and N. The i bit specifies whether or not the Link bit is to be included in the rotation while N, tells how many places to the left the A-register is to be rotated.

At GNI, the P-register contains the address of the ROL instruction. GNI clears the MEM ⟶B flip-flops and at GO, the contents of the P-register are jam-transferred into the S-register.

This function increments the P-register by 1 and clears the B-register. The GO pulse also clears the C-register and sets the MEM ⟶ B flip-flops. Following GO, the memory location specified by the S-register is read into the MB and B-registers and the C-register.

C-register bits C08 through C11 now contain the value N which specifies the number of times that the contents of the A-register will be rotated to the left. These four bits function as a step counter which is decremented by 1 for each rotate operation. When the specified number of rotations have been completed, C08 through C11 contain 0000 and the instruction is complete except for the standard end-of-instruction operations. Additional information concerning the N step-counter function is presented in Section 3.3.3.2.

At T1, the time pulse distributor is advanced to T10, at which time the MB register is cleared. If N≠0 at T10, the contents of the A-register are rotated one place to the left by the AROL pulse. If N=0 at T11, then GNI is produced and the specified number of rotations have been completed, in this case, one rotation. If N≠0 at T11, a second AROL pulse is produced and the time pulse distributor is brought back to T10. If N is now equal to 0 then nothing of significance occurs at T10 and GNI is generated at T11. The rotate functions continue until N=0, signifying that the correct number of rotations have taken place.

Assuming the LINC is to continue on, GO will be produced in coincidence with TLAST. At this time the contents of the P-register are jam-transferred into the S-register, the P-register is incremented by 1, the B- and C-registers are cleared, and the MEM ⟶ B flip-flops are set.

4.6.2 ROR i N

ROR i N is a shift class instruction containing two variables, i and N. The i bit specifies whether or not the Link bit is included in the rotation, while N tells how many places to the right the A-register is to be rotated. The Z-register is also shifted to the right. A11 goes into Z00 and Z11 is lost.

Functionally, the operation of ROR is the same as that for ROL, with the exception that the A-register is rotated to the right and the Z-register receives bits from A11 and shifts them to the right. Each time a rotate operation occurs, the Z-register is shifted one place to the right.

4.6.3 SCR i N

SCR i N is a shift class instruction containing two variables, i and N. The i bit specifies whether or not the link bit is to be included in the scaling, while N tells how many places to the right the A-register is to be scaled. The Z-register is also shifted right. Bit A11 goes into Z00 and Z11 is lost. A11 also goes into the link bit if i=1.

Functionally, the operation of SCR is the same as that for ROR with the following exceptions. Bit A00 is never changed and is shifted into A01 on each shift. When i=1, bit A11 goes into the Link bit and the previous contents of the Link bit are lost. Bit A11 also goes into Z00 and the Z-register is shifted right. When i=0, the Link bit is excluded altogether from the scaling. Bit A11 goes into Z00 only and the Z-register is shifted right.

4.7 SKIP INSTRUCTIONS

4.7.1 SXL i N

SXL i N is a skip instruction. At GNI, the P-register contains the value p. At GO, this value is jam-transferred into the S-register. The jam transfer adds 1 to the P-register (p+1) and clears the B-register. The GO pulse also clears the C-register and sets the MEM ⟶ B flip-flops.

Following GO, the contents of the memory location specified by the S-register is read into the MB, B- and C-registers. No operations occur at T1 and only the MB register is cleared at T2. Following T2, the same memory location read after GO is read into the MB and B-registers.

At T3, GNI is produced, clearing the MEM ⟶ B flip-flops. The P-register will be incremented by 1 if i=0 and the signal on external level line N is -3V, or i=1 and the external level line is at 0V. Otherwise, the P-register is not changed.

At TLAST, GO will be produced if the LINC is to continue. A P ⇢ S occurs. The jam-transfer increments the P-register by 1 and clears the B-register. GO also sets the MEM ⟶ B flip-flops and clears the C-register.

4.7.2 SKP i N

SKP i N is a skip instruction. At GNI, the P-register contains the value p. At GO, this value is transferred into the S-register. The jam transfer adds 1 to the P-register (p+1) and clears the B-register. The GO pulse also clears the C-register and sets the MEM ⟶ B flip-flops.

Following GO, the memory location specified by the S-register is read into the MB, B-, and C-registers. No operations occur at T1 and only the MB register is cleared at T2. Following T2, the same memory location read after GO is read into the MB and B-registers.

At T3, GNI is produced, clearing the MEM ⟶ B flip-flops. The P-register will be incremented by 1 if i=0 and the internal condition is met or if i=1 and the internal condition is not met. Otherwise, the P-register is not changed.

At TLAST, operations identical with those that occur with SXL take place.

4.8 MISCELLANEOUS CLASS INSTRUCTIONS

4.8.1 MSC N

At GNI, the P-register contains the address of the instruction. The MEM ⟶ B flip-flops are cleared. The GO pulse initiates a P ⟶ S which causes the P-register to be incremented by 1 and clears the B-register. GO also sets the MEM ⟶ B flip-flops and clears the C-register. Next, the contents of the memory location specified by the S-register are read into the C, B, and MB registers. At T1, the contents of the MB register are written into the memory location which they were obtained. The particular MSC class instruction to be executed depends on the value of N (right-most 4 bits of MSC N instruction).

4.8.1.1 N=0 (HLT) - At T2, the RUN INT, AUTO, and LBRK flip-flops are cleared. At T3, the CHIME flip-flop is set. During T2 and T3, no operations occur in the registers shown.

4.8.1.2 N=5 (ZTA) - At T2, the contents of bits 0-11 of the Z-register, replace the contents of bits 0-11 of the A-register. The contents of the Z-register are unchanged.

At T3, the ASHRPLS (A shift right pulse) is produced, shifting the contents of the A-register one place to the right. ASHRPLS also generates BCLA0 which clears bit A00 since B00 is 0 at this time. Bit A11 is lost.

4.8.1.3 N=11 (CLR) - At T2, the A-register and the Link bit are cleared. The MB register is cleared at this time. At T3, the Z-register is cleared.

4.8.1.4 N=14 (ATR) - At T2, the six flip-flops of the R-register are cleared as is the MB reigster. At T3, bits 6-11 of the A-register are 1s transferred into the R-register. The contents of the A-register are left unchanged.

4.8.1.5 N=15 (RTA) - At T2, the A and MB registers are cleared. At T3, the contents of the R-register are 1s transferred into the right half of the A-register. The contents of the R-register are left unchanged.

4.8.1.6 N=16 (NOP) - At T2, the MB register is cleared. No operations occur at T3.

4.8.1.7 N=17 (COM) - At T2, the A-register is complemented and the MB register is cleared. No operations occur at T3.

4.9 HALF-WORD INSTRUCTIONS

This section contains timing-flow diagram descriptions of the half-word instructions LDH, STH, and SHD. Of special importance is an understanding of the h-bit function during a half-word instruction. The h bit is defined as the most-significant bit (bit 00) of the register containing the address of the operand of a half-word instruction. If h=0, the left-half of the 12-bit operand is selected; while, if h=1 the right half is used. The actual selection of either the right- or left-half of the operand does not occur until T10, at which time the contents of the B-register are jam-transferred into the S-register for all instruction formats except i=1 and B=0. S00 contains the h-bit after T10 and B00 contains the h-bit just prior to T10. In the case where i=1 and B=0, the operand is located in the memory register immediately following the half-word instruction itself. For this particular situation, the left-half of the operand is specified and the right-half is never used.

A second important function during half-word instructions is the MB and B-register indexing which takes place at time pulse T3 if the i bit is 1 and B≠0. This indexing involves B-register bit B02 (most-significant bit) through B11, which function as a binary counter. Bit B00 (h bit) functions as the least-significant bit of this counter, thus making it an 11-bit counter. B01 is not used at all in this operation. Each time an index operation takes place at T3 of a half-word instruction, B00 is complemented. A carry out of B00 is brought around to complement B11. A carry out of B11 complements B10, and so forth all the way down to B02.

The above operations come into effect during the condition where i=1 and B≠0 of a half-word instruction. Assume that the h-bit = 0 the first time this instruction is executed. This 0 specifies a function involving the left 6-bits (0 through 5) of the operand. At T3 of this instruction, the h bit is complemented. If the instruction is immediately repeated through a program loop operation with the h bit set to 1, then the right 6-bits (6 through 11) of the same 12-bit operand are selected. During a third execution of the same instruction, the h bit is again complemented to the 0-state. This produces a carry out of B00 which is brought around to complement B11, thereby indexing the contents of the B-register by 1. In this repetition of the instruction, the left-half of the operand in the next sequential memory location is selected. The indexing of the B-register and complementing of B00 allow the user to select alternate left and right halves of consecutive memory locations by repeating the half-word instruction with i=1 and B≠0. Similar indexing operations as described above for the B-register also take place in the PDP-8 MB register.

4.9.1 LDH iβ

Standard operations that occur prior to T1 read the LDH instruction into the C-register. No operations occur at T1 unless i=1 and β=0, in which case the time pulse distributor is advanced to T10.

Assuming this is not the case, the next time pulse is T2. If $\beta=0$, the contents of the P-register are jam-transferred into the S-register, causing the P-register to be incremented by 1 and clearing the B-register. If $\beta\neq0$, the β portion of the instruction (bits 8 through 11) is jam-transferred into corresponding S-register bits. Following T2, the PDP-8 memory location specified by the S-register is read into the MB and B-registers.

At T3, if i=1, the MB and B-registers are indexed as described in the introduction to half-word intructions (Section 4.9). The time pulse distributor is advanced to T10. Following T3, the contents of the MB register are written back into the memory location from which they were obtained.

The time pulse distributor is advanced to T10. The functions that take place at T10 are dependent on the iβ configuration. If i=1 and $\beta=0$; the P-register is jam-transferred into the S-register, the P-register is incremented by 1, and the B-register is cleared. For all other conditions of i and β, the B-register is jam-transferred into the S-register and then the B-register is cleared. The A-register is also cleared at T10. Following T10, the contents of the memory location specified by the S-register are read into the MB and B-registers.

4.9.1.1 hBit=0 - At T10, for all conditions of iβ except when i=1 and $\beta=0$, the B ⊣► S transfer places the h bit into S00. At T11, S00 (now containing the h bit) is evaluated for either a 0 or a 1. If h=0, the left-half of the B-register is 1s transferred into the left-half of the A-register, while the right-half of the A-register remains cleared. At TLAST, the left and right halves of the A-register are interchanged (designated by ↻), placing the half-word just read out of memory into the right-half of the A-register.

4.9.1.2 h Bit=1 - At T11 if h=1, the right-half of the B-register is 1s transferred into the right-half of the A-register. Regardless of the value of h, GNI will be generated at T11 and the GO pulse will be generated at TLAST if the LINC is to continue in the LINC mode of operation.

4.9.2 STH iβ

The A-register contains a 12-bit word, the right 6-bits of which will be stored into the designated half of a memory location. Standard operations occur from GNI to T3. At T3, if i=1, the MB and B-registers are indexed as in LDH. The time pulse distributor is advanced to T10.

4.9.2.1 h Bit=0 - At T10, the left six bits of the PDP-8 memory location specified by the contents of the S-register are inhibited by clearing the SA ⟶ BL ENABLE flip-flop. Following T10, a 12-bit operand is read out of memory into the MB register. Since the left six input gates to the B-register are inhibited, only the right six bits of the operand go into the right-half of the B-register.

At T11, the left and right halves of the A-register are interchanged and the WRITE flip-flop is set. At T12, the left 6-bits of the A-register are 1s transferred into the left 6-bits of the B-register. After this operation, the B-register will contain a 12-bit word, the left 6-bits containing what was originally in the right 6-bits of the A-register, and the right 6-bits containing what was read from memory.

At T13, the contents of the B-register are read into the MB register and into memory. GNI is produced. Again the left and right halves of the A-register are interchanged, leaving the A-register as it was before T11.

4.9.2.2 h Bit=1 - At T10, the right-half of the memory location specified by the contents of the S-register is inhibited by clearing the SA ⟶ BR ENABLE flip-flop. Following T10, the 12-bit operand is read into the MB register. Only the left-half enters the B-register (bits B00-B05).

At T11, all registers maintain their status and the WRITE flip-flop is set. At T12, the right-half of the A-register is read into the right-half of the B-register. The B-register now contains a 12-bit word. The left 6-bits are the left 6-bits of the operand. The right 6-bits are from the right-half of the A-register.

At T13, the contents of the B-register are read into the MB register and into memory since the WRITE flip-flop was enabled. TLAST is the next LINC-8 timing pulse. If the LINC is to continue on, GO will be generated, starting the next instruction.

4.9.3 SHD iβ

If the contents of the right-half of the A-register do not match the contents of the designated half of operand in memory, skip the next instruction in sequence; otherwise, execute the next instruction. The contents of the A-register and the selected memory register are unchanged.

Standard operations which occur prior to T1 read the SHD instruction into the C-register. No operations occur at T1 unless i=1 and β=0, in which case the time pulse distributor is advanced to T10. Assuming this is not the case, T2 is the next timing pulse. At T2, if β=0, the contents of the P-register are jam-transferred into the S-register, causing the P-register to be incremented by 1 and clearing the B-register. If β≠0, the β portion of the instruction is jam-transferred into the S-register. Following T2, the PDP-8 memory location specified by the S-register is read into the MB and B-registers.

At T3, if i=1, the MB and B-registers are indexed as described in the introduction to half-word instructions. The contents of the MB register are written back into memory. The time pulse distributor is advanced to T10, at which time operations occur depending upon the value of i and β. Either the contents of the B-register are jam-transferred to the S-register; or, the P-register is jam-transferred into the S-register and the P-register is incremented by 1. The B-register is cleared.

Following T10, the contents of the memory location specified by the S-register, which is the operand, is read into the MB and B-registers.

4.9.3.1 h Bit=0 - At T11, the two halves of the A-register are interchanged. At T12, a BCOA operation occurs between the A- and B-registers, the result of which is left in the A-register. Following T12, the contents of the memory location specified by the S-register are again read into the MB and B-registers. Since the operand is already in the B-register this has no effect; memory has merely been left running.

GNI is produced at T13. The contents of the MB register are written back into the memory location from which they were obtained. If AL≠0, that is if the original right-half of the A-register is not equal to the left-half of the B-register, the P-register is incremented by 1. If it is equal, the P-register is not incremented. At T13 another BCOA takes place, restoring the A-register to its original form as before T12.

At TLAST, the two halves of the A-register are again interchanged. This operation leaves the register as it was before T11. The GO pulse causes a P→S which increments the P-register by 1 and clears the B-register. The GO pulse also sets the MEM→B flip-flops and clears the C-register. If the P-register was incremented at T13, then the P→S function causes the LINC to skip the next sequential instruction.

4.9.3.2 h Bit=1 - No important operations occur at T11. At T12, a BCOA operation occurs between the A- and B-registers. Following T12, the contents of the memory location specified by the S-register are again read into the MB and B-registers.

At T13, GNI is produced. If, following the BCOA at T12 the right-half of the A-register is not 0 (indicating the original right-half of A was not equal to the right-half of B) the P-register is incremented by 1. The P-register is not incremented if the right half of the A-register is 0. Another BCOA occurs between the A- and B-registers, leaving the A-register as it was prior to T11. The contents of the B-register remain the same.

At TLAST, GO is generated if the LINC is to continue on. GO initiates a P→S pulse which increments the P-register by 1 and clears the B-register. The next instruction is skipped if the P-register was incremented at T13. The GO pulse also sets the MEM→B flip-flops and clears the B-register. The MB register is also cleared at this time.

4.10 CHANGE MEMORY BANK INSTRUCTIONS

4.10.1 UMB N

The function of this instruction is to change the Upper Memory Bank Selector. The Upper Memory Bank Selector is the register which points to the 2000_8 word segment of memory that will be used when the LINC refers to an address between 2000_8 and 3777_8. The majority of the logic is associated with this instruction as shown on drawing L26.

After the usual operations at T1 and strobe time, the contents of C-register bits 7-11 are transferred into the UMB register (Upper Memory Bank Selector Register) at T2. This transfer is accomplished by the SET UMB pulse shown in the lower right-hand corner of drawing L26. This pulse is generated by the signal UMB·T2 when the signal ENABLE MEM CHANGE is true. The signal ENABLE MEM CHANGE will be present if a legal and existing memory bank is being selected. The R151 decoder and associated diode gating, shown on drawing L26, generate the signal ENABLE MEM CHANGE. The signal will be true if memory bank 0 is not being selected, and if the memory bank which is being selected does exist (unless the system was equipped with extended memory, references to memory banks greater than three would be illegal). The SET UMB pulse therefore changes the state of the Upper Memory Bank Selector registers at T2 of the UMB instruction. Hence, all further references to the upper half of LINC memory (2000_8-3777_8) will be made to the 2000_8 word segment of memory now pointed at the Upper Memory Bank Selector Register.

4.10.2 LMB N

The instruction LMB changes the Lower Memory Bank Selector Register. The lower Memory Bank Selector Register shows which 2000_8 word segment of memory LINC instructions will be taken from. All LINC addresses between 0000_8 and 1777 will go to that 2000_8 word segment of memory pointed to by the Lower Memory Bank Selection Register. The LMB instruction does not immediately change the Lower Memory Bank Register itself. Rather, the instruction LMB sets an intermediate register called LMB SETUP which is then jam-transferred into the Lower Memory Bank Selector at the occurrence of the next jump instruction (which does not jump to location 0).

The logic associated with this instruction is shown on drawing L26. The 0⟶LMB SETUP pulse is generated at T2 of the LMB instruction. This clears out the LMB SETUP register. At T3, the pulse LOAD LMB SETUP transfers the contents of control register (bits C07 to C11) into the LMB SETUP register. The pulse LOAD LMB SETUP also sets the SET LMB SYNC flip-flop if the level ENABLE MEM CHANGE is true. The level ENABLE MEM CHANGE means that the newly selected LMB location is legal (non-zero and for memory which exists on the machine).

When the above conditions have taken place, the LMB SETUP register holds the new Lower Memory Bank contents, and this will be strobed into the Lower Memory Bank Selection Registers at the next non-zero jump instruction. At time T1 of the next non-zero jump instruction, the pulse CHANGE MEMORY EXT will strobe the LMB SETUP bits 0, 1, and 2 into the LMB registers, bit 0, 1, and 2. This is done at T1 of the jump instruction so that adequate set-up time is allowed for the extended address bits. At T2 of the jump instruction, the SET LMB pulse will be generated which will transfer LMB SETUP bits 3 and 4 into the Lower Memory Bank Selection Register bits LMB03 and LMB04. In addition, the SET LMB pulse also clears the SET LMB SYNC flip-flop.

The above operations mean that the instruction JMP (not JMP 0) will be fetched from a location in the old Lower Memory Bank, and the return address for the JMP instruction will be stored at location zero of the newly selected Lower Memory Bank location.

Note that there is no programming restriction on when the JMP must occur. After the LMB instruction, there may be any number of instructions between the LMB instruction and the JMP instruction which causes the completion of the change of Lower Memory Bank Selection Registers.

4.11 8 EXECUTE CLASS INSTRUCTIONS (MTP, OPR, EXC)

The 8 EXECUTE CLASS LINC instructions (MTP, OPR, and EXC) are used to turn off the LINC subsystem and signal PROGOFOP with the program interrupt request.

GNI clears the MEM ⟶ B flip-flops. The P-register contains the value p. At GO, a P ⟶ S occurs, placing p in the S-register, P+1 in the P-register, and clearing the B-register. The GO pulse also clears the C-register and sets the MEM ⟶ B flip-flops. Following GO, the contents of the memory location specified by the S-register are read into the MB, B and C-registers. No operations occur at T1. At T2, the MEM ⟶ B flip-flops are cleared.

GNI is produced at T3. Any 8 EXECUTE CLASS instruction-MTP, OPR, or EXC-generates a level called EXCL which sets the 8 EXEC flip-flop (drawing L16). This flip-flop signals PROGOFOP that an instruction is to be interpreted. EXCL also produces the HOLD level which causes the LBRK flip-flop to be cleared at GNI time, thus stopping the LINC subsystem and taking the PDP-8 out of the break cycle.

At TLAST, the MB register is cleared. The ADDRESS SELECT flip-flop is cleared, thereby addressing is returned to PDP-8 MA register.

CHAPTER 5
MAINTENANCE

5.1 MAINTENANCE PHILOSOPHY

This section contains maintenance information for the LINC-8 computer. From a maintenance standpoint, the LINC-8 is considered as three functional subsystems: the PDP-8 processor, the LINC processor, and the interface circuits between these two processors. The recommended method of troubleshooting the LINC-8 is to first determine whether or not the PDP-8 processor is functioning properly. Once this is verified, the PDP-8 can be used to run the diagnostic programs which exercise various functions of the LINC processor and the LINC/PDP-8 interface circuits. Maintenance procedures for the PDP-8 are found in Chapter 9 of the PDP-8 Maintenance Manual, F-87. The most important step in maintenance is to determine where and how a particular instruction sequence is not operating correctly. Then the problem is isolated, and it remains only to correct the known malfunction.

5.1.1 Scheduled Maintenance

The LINC-8 should receive certain routine maintenance attention to assure maximum life and reliability of the system.

5.1.1.1 Teletype - The Teletype should be given regular attention as outlines in the Teletype manual.

5.1.1.2 MAGtape Heads and Guides - The tape heads and guides should be cleaned whenever they are dirty. Typically, this should be once a day, although in very clean environments, where the tape system is not heavily used, it may be performed weekly.

5.1.1.3 Air Filters - The air filters should be cleaned whenever dirty. This is typically once a month, under usual conditions.

5.2 TOOLS AND TEST EQUIPMENT

Table 9-1 in the PDP-8 Maintenance Manual lists the maintenance equipment required for the PDP-8 Processor. In addition to these items, the maintenance technician will also require the items listed in Table 5-1 of this manual. The single most important tool is a thorough understanding of the operation of the entire system.

Table 5-1
Maintenance Equipment

Equipment		Manufacturer	Designation
LINC-8 Maintenance Library MAGtape, associated write-ups, and backup paper tapes*		DEC	
Precision voltage source (-1V to +1V, 0.1%	(for A-D) System	Electronic Development Corporation	VS-11
Allen wrench set	(for Tape) System		
Small open-end wrench set	(for Tape) System		

*Supplied with the LINC-8

5.3 DIAGNOSTIC PROGRAMS

The LINC subsystem of the LINC-8 Computer is checked using a special diagnostic program called SUDSY (LINC-8 SUper Diagnostic SYstem). SUDSY is a series of PDP-8 programs, each of which tests one or more parts of the LINC processor logic, LINC/PDP-8 interface, LINC processor operating mode and interrupt functions, and LINC console functions. A complete description for loading, executing, and interpreting the results of SUDSY is contained in a separate document. As stated previously, the PDP-8 processor must be functioning properly before SUDSY can be used to check the LINC subsystem.

5.4 POWER SUPPLY TEST

Power for the LINC-8 system is identical to that for the PDP-8 with the exception that an additional Type 783 Power Supply is connected in parallel with the +10V and -15V outputs of the Type 708 Power Supply used in the PDP-8. This effectively increases the system power capability to 23A at -15V. The range and ripple characteristics remain essentially the same as defined in Chapter 9 of the PDP-8 Maintenance Manual.

5.5 MARGINAL CHECKS

The LINC-8 is equipped with facilities to check individual sections of the logic by applying variable power from the marginal check section of the Type 708 Power Supply in place of the normal logic power. Access to the controls of the 708 is gained by removing the cover located below the table at the front of the LINC-8 cabinet.

There are 12 switches associated with each of the three normal logic sections of the LINC-8: memory (M), LINC (L), and processor (P). One of these switch banks is shown in Figure 5-1. Each switch has two positions. The FIXED position allows application of the normal logic operating power while the MC position selects variable power from the marginal-check power supply. The fuses located alongside each marginal check switch provide overload protection in the event that excessive current is drawn on that power line (fuses are 3A).

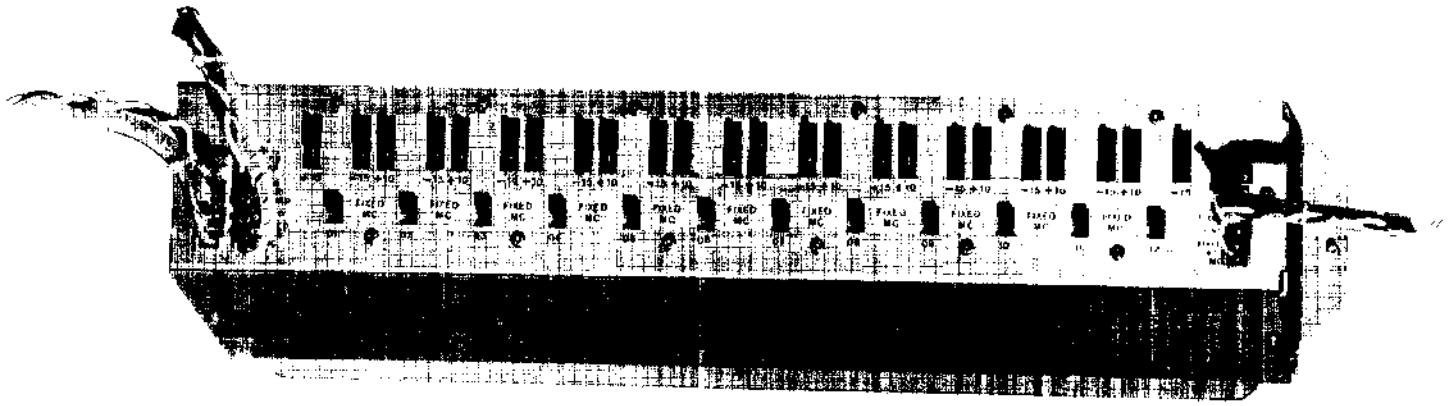


Figure 5-1 Marginal Check Switch Bank

5.5.1 Marginal Check Schedule

The LINC-8 marginal-check schedule for a particular installation is dependent upon the type of experimentation and analysis being performed. In applications requiring high reliability of operation, where a computer failure could be costly, it is recommended that marginal checking be performed at least once a month. The user should schedule approximately eight hours for the complete marginal-check procedure. In other applications, where an occasional computer malfunction can be tolerated (once or twice a year), the LINC-8 can be operated on a continuous basis until a problem is detected.

5.5.2 Marginal Check Sheet

For record keeping and evaluation, a marginal-check log sheet should be filled out each time the LINC-8 is marginal checked. Figure 5-2 shows a sample of this sheet. Nominal margins are indicated on the sheet while actual margins obtained should be filled in along with the marginal check program used to obtain them.

5.5.3 Diagnostic Marginal Check Procedure

During production, the LINC-8 system is checked to ensure that all diagnostics operate with the −15V marginal supply between −12 and −18V, and the +10V marginal supply between +5 and +15V. This applies to all switches except the following:

a. Switches 1, 2, 3 of the memory section which relate to the sense amplifiers (refer to PDP-8 Maintenance Manual).

b. LINC switch 10, because of special modules, uses supply voltages of −13V to −17V, +6V, and +14V.

For the purposes of general maintenance, the switches designated in Table 5-2 are used with certain diagnostic programs. In some unusual circumstances, it may be desirable to use other switches during maintenance. Any subsection or group of logical subsections may be margined together as long as their total current drain from the marginal checking supply does not exceed 2A.

CAUTION

When operating a system on margins, there is always a possibility that the MAGtape control will either fail or be given incorrect commands, thereby damaging the data on the tape mounted over the heads. The technician should margin the system with a tape he can afford to have destroyed. This is especially true for the following margin switches: M8-M11, and L1-L4.

Table 5-2
Marginal Check Switch Functions for Diagnostic Programs

Test		Switches
PDP-8 TEST PROGRAMS		
MAINDEC	ADDRESS TEST	M1-M5, M12
	CHECKERBOARD	M1-M5, M12
	TELETYPE TEST	M6-M7, P1, P2
	INST.TEST 1	P1-P6
	2A	P1-P6
	2B	P1-P6
	2C	P1-P6
	3A	P1-P6
	3B	P1-P6
LINC TEST PROGRAMS		
	DECTST (SUDSY)	M8-M12, L1-L12, P7, P10
	TSTINS (OPTIONAL) (ST. LOUIS TEST)	M8-M12, L1-L12, P7, P10

LINC-8 MARGINAL CHECK SHEET

If checking is done at room temp just record program name. Place "T" after program name if at elevated temperature (110°F intake). Initial entry if OK, note actual voltage if not to specification.

TECH _____

PROC _____ MEM _____ LINC _____

DATE _____

PROGRAM NAME

Switch	Nominal											
		+5/-18	+15/-12	+5/-18	+15/-12	+5/-18	+15/-12	+5/-18	+15/-12	+5/-18	+15/-12
M1	+10										
	-15										
M2	+10										
	-15										
M3	+10										
	-15										
M4	+10										
	-15										
M5	+10										
	-15										
M6	+10										
	-15										
M7	+10										
	-15										
M8	+10										
	-15										
M9	+10										
	-15										
M10	+10										
	-15										
M11	+10										
	-15										
M12	+10										
	-15										

Comments:

Figure 5-2 Marginal Check Sheet Sample

PROGRAM NAME

Switch	Nominal										
		+5/-18	+15/-12	+5/-18	+15/-12	+5/-18	+15/-12	+5/-18	+15/-12	+5/-18	+15/-12
P1	+10										
	-15										
P2	+10										
	-15										
P3	+10										
	-15										
P4	+10										
	-15										
P5	+10										
	-15										
P6	+10										
	-15										
P7	+10										
	-15										
P8	+10										
	-15										
P9	+10										
	-15										
P10	+10										
	-15										
P11	+10										
	-15										
P12	+10										
	-15										
L1	+10										
	-15										
L2	+10										
	-15										
L3	+10										
	-15										
L4	+10										
	-15										
L5	+10										
	-15										
L6	+10										
	-15										
L7	+10										
	-15										
L8	+10										
	-15										
L9	+10										
	-15										
L10	+10										
	-15										
L11	+10										
	-15										
L12	+10										
	-15										

Figure 5-2 Marginal Check Sheet Sample (Cont.)

5.5.4 Detailed Marginal Check Switch Functions

Table 5-3 lists the logic functions controlled by specific marginal-check switches for the memory, processor, and LINC sections of the LINC-8 computer. The physical location of these sections is shown in Figure 1-1.

Table 5-3
Detailed Marginal Check Switch Functions

Switch	Function
Memory Section	
SW 1	Sense Amplifiers, +10V only (slice) PIN D MA25-MA31, MB25-MB30
SW 2	Sense Amps Power MA25-MA34
SW 3	Sense Amps Power MB25-MB35
SW 4	Memory Selectors MC01-MC35
SW 5	Memory Selectors MD01-MD34
SW 6	PDP-8 Memory Rack E ME01-ME29
SW 7	PDP-8 Memory Rack F MF01-MF30
SW 8	Tape Control, Part 1 and Spares MH04-MH12, MJ01-MJ12
SW 9	Tape Control, Part 2 MH18-MH32
SW 10	Tape Control, Part 3 MJ18-MJ36
SW 11	Tape Reader-Writers and Transport MA40, MB37-MB40, MC37-MC40
SW 12	Address Selector Gates MD37-MD39, ME37-ME39, MF37-MF39
Processor Section	
SW 1	AC Register PA06-PA18
SW 2	AC Register Control and Miscellaneous PA19-PA36, PB19-PB36

Table 5-3 (Cont)
Detailed Marginal Check Switch Functions

Switch	Function
Processor Section (cont)	
SW 3	MB, PC, MA Register LC02-LC18
SW 4	MB, PC, MA Register Control and Miscellaneous PB02, PC19-PC36, PD03-PD06, PD19-PD36
SW 5	PDP-8 Processor Rack E PE05-PE36
SW 6	PDP-8 Processor Rack F PF05-PF36
SW 7	A-D and Display PH18-PH32, PJ18-PJ33
SW 8	Spares PH33-PH40, PJ34-PJ40
SW 9	Indicator Drivers PE37-PE40, PF37-PF40
SW 10	Data Break Multiplexing PH05-PH12, PJ05-PJ12
SW 11	Spare
SW 12	Indicator Drivers PA37-PA40, PB37-PB40, PC38-PC40, PD37-PD40
LINC Section	
SW 1	B-, S-, P-Register and Control Sense Amps --- B pulses LB01-LB05, LE08-LE24, LF08-LF24, LH07-LH12
SW 2	A-Register and Control LC05-LC22, LD05-LD22
SW 3	IOT Pulses and Memory Extension LC01-LC04, LD02-LD04, LE03-LE07, LF02-LF07, LH03-LH06, LJ05-LJ12
SW 4	Z-Register, Match A = 0 LA04-LA12, LB06-LB20
SW 5	Timing LH18-LH37
SW 6	C-Register and Instruction Decoders LJ18-LJ37
SW 7	Control Gates and Control Pulses LB25-LB29, LC23-LC27, LD23-LD28, LE25-LE35, LF25-LF36

Table 5-3 (Cont)
Detailed Marginal Check Switch Functions

Switch	Function
LINC Section (Cont)	
SW 8	PDP-8 AC Input Gates and Control and Interface Logic LC28-LC40, LD35-LD40, LE36-LE40, LF37-LF40
SW 9	Console Switches, I Sense, X Sense and Control LA32-LA39, LB30-LB36, LB38-LB40
SW 10	Control Functions and Console Switch Detector (R122's and W501) LA40, LD29-LD34
SW 11	Data Terminal Panel Power LA28-LA31
SW 12	Indicator Driver Power LA14-LA27, LB21-LB24

5.6 TIMING TESTS

The LINC-8 is designed to be relatively unaffected by module and parts variations. There are several delays which must be set to particular values if stable operation and wide margins are to be expected. These specific items are listed below and their adjustment is called out. Once set up, there is no reason for them to drift, because neither the modules nor the components are critical. The delay adjustments are considered in two groups: LINC processor delays, and MAGtape, system delays. These adjustments should only be made by a technician thoroughly familiar with the LINC-8.

NOTE: The PDP-8 IOT delays must be correctly set.
See PDP-8 Maintenance Manual.

5.6.1 LINC Processor Delay Adjustments

5.6.1.1 IOT Delays 8L2 and 8L3 - These delays are shown on drawing L17, and are located in LJ08 (R302). The 8L2 delay (pin M) should be 1.2 μs (±0.1 μs). The delay 8L3 (pin V) should be 0.8 μs (±0.1 μs).

The following PDP-8 program can be used to set the two above delays.

```
4000    7200    /CLA
4001    6161    /IACB
4002    7000    /NOP
4003    7000
4005    7000
4006    7000
4007    5200    /JMP 4000
```

5.6.1.2 Time Pulse Generator Pulse Amplifiers - The output width of the pulses from pin K of LH19 and LH20 (drawing L15) is rather important. These pulses should be 170 ns (±30 ns). They can be observed by either running a LINC-8 program or by grounding LH19T and setting the right switches to 5200 and pressing PDP-8 LOAD ADD, DEP, LOAD ADD, and START, in that order.

If the pulse is not of the correct width, change the value of the capacitor connected to pins D and M of the offending pulse amplifier (nominal value 220 PF).

WARNING

Remove ground from LH19T when through.

5.6.1.3 Time Pulse Generator Delay Inverters - The capacitors on the output of inverters LH24 and LH25 (drawing L15) are used to slow the output fall of the inverter. The waveform should be as shown in Figure 5-3. If the fall time is incorrect, check the modules to be sure the capacitors are the correct value (220 PF) and the R107 has 2 mA clamped loads. Check pins LH24D, F, J, L, N, R and LH25D, F, J, L, N, R. Start timing chain as in Section 5.6.1.2 above.

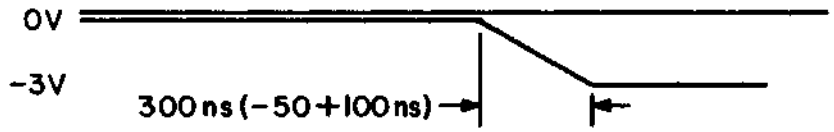


Figure 5-3 Time Pulse Delay Waveform

5.6.1.4 10 ⟶T Pulse - This pulse is generated by an R601 Pulse Generator located in LH36 (drawing L21). This pulse is used to set the timing flip-flops to the 1000-state. The pulse must be long enough so that carries from one flip-flop to the next are overridden, and short enough so that the next time pulse (500 ns later) will give proper counting. This pulse should be between 320 ns and 370 ns (LH36D). The pulse width is changed by varying the capacitor on pins LH36E to LH36F (nominal value 680 PF). This pulse can be generated by grounding pins LH19T (drawing L15) and LH36H (drawing L21). Now set right switches to 5200. Press PDP-8 LOAD ADD, DEP, LOAD ADD and START, in that order.

WARNING

Remove the above ground leads when finished.

5.6.1.5 4⟶T Pulse - This is essentially the same situation as the 10⟶T pulse. The pulse at LF24K (drawing L21) should be between 320 and 370 ns. The pulse can be generated by grounding

LH19T (drawing L15) and connecting LD03F (drawing L15) to LF24L (drawing L21). Now set the right switches to 5200, and press PDP-8 LOAD ADD, DEP, LOAD ADD, and START, in that order.

WARNING

Remove the above leads when finished.

5.6.1.6 B (Break) Disable Delay - The delay output pulse at pin PH05V (drawing P23) is used to extend the B (break) signal to the full break cycle during external data-break requests. The pulse should be set to 750 ns (±50 ns). It can be adjusted by grounding pin PH05P, setting 5200 in the right switches and then pressing PDP-8 LOAD ADD, DEP, LOAD ADD, and then START, in that order.

WARNING

Remove the ground from PH05P when finished.

5.6.1.7 LOAD Key Start Delay - The delay output pulse at pin PH05M (drawing P25) should be set to 10 ms. It can be set by removing all MAGtapes from the tape transports, lifting the PDP-8 SING INST switch, and repeatedly lifting the LOAD switch

5.6.2 MAGtape Delay Adjustments

5.6.2.1 TTOK (Tape Timing OK) Delay - The output at pin MH11D (drawing M11) should be set to 34 μs (39 μs for 50 Hz systems). This delay is an integrating one-shot which is triggered by the change in output state of the timing channel tape-track reader. The reader output will oscillate even without an input signal. If this has a period longer than 34 μs (39 μs for 50 Hz systems), it is possible to directly set the delay by observing the output at pin MH11D. If the delay is always set, manually move a marked tape across the tape head unit that is selected for operation. This will provide enough slow input to the tape reader to allow adjustment of TTOK to 34 μs (39 μs for 50 Hz systems).

5.6.2.2 XTLK (Cross Talk) Delay - This delay output at pin MH10M (drawing M11) can usually be set directly without moving tape. It should be adjusted to 9 μs.

5.6.2.3 TT2 Delay - This delay output at pin MJ10M (drawing M11) can be adjusted without moving tape by simply grounding MJ24J and setting the delay to 6 μs.

WARNING

Remove ground from MJ24J when finished.

5.6.2.4 WDASM-2 Delay - This delay output at pin MJ10V (drawing M12) can be adjusted without tape motion. Grounding MJ24J and MJ30L, will allow TT2 to be generated. TT2 will trigger the WDASM-2 delay. The delay can now be adjusted to 1 μs.

WARNING

Remove ground from MJ24J and MJ30L when finished.

5.6.2.5 Mark Clock - This is a gated clock that is set to 10 μs. The following procedure can be used to set the delay. All tapes must be removed from both transports since the Mark Tape Writers are enabled

a. Ground MJ33E (drawing M12). This will set the MARK flip-flop.

b. Set the clock (MH27) to 10 μs.

c. Turn the LINC-8 Computer OFF. This will generate power-clear pulses that clear the MARK flip-flop during power turn-on.

d. Remove ground from MJ33E.

5.6.2.6 CLOSE Pulse Delay - The delay output at pin MH10V (drawing M13) is used to lengthen the CLOSE pulse to 0.5 μs. It may be adjusted by either operating the MAGtape (if functional) or by executing the following PDP-8 program which starts at PDP-8 location 100.

```
100   7201   CLA IAC    /1 to PDP-8 AC
101   6141   ICON       /ICON (AC to MOTION)
102   5100   JMP 100    /Jump to beginning
```

5.6.2.7 ACIP Delay - Location MH7D - This delay is used to prevent the tape control from looking at the signals coming from tape any time that a new motion has been selected. This delay must be long enough to carry out beyond the 0 signal coming off the tape head during turnaround operations. (See Figure 5-4); and, it must be short enough so that when the tape turns around it is ready to read the next block. The delay is normally set to 120 ms, but with some tape transports, under some conditions, it may vary anywhere between 100 and 150 ms. This delay can be set up by operating the MAGtape System in such a way as to change the tape direction. The following LINC program is useful.

```
20     723    /move toward
21     0100   /block 100
22     6020   /jump back to 20
```

If the tape system is not functional, the following PDP-8 program will change the motion flip-flops and thereby trigger ACIP (drawings M10 and M11).

Start 4001 with 4001 in the right switches.

```
4001  7604  LAS                  4010  5207  JMP 4007
4002  6141  ICON (AC to MOTN)    4011  2215  ISZ 4015
4003  7200  CLA                  4012  5207  JMP 4007
4004  6141  ICON (0 to MOTN)     4013  5201  JMP 4001
4005  1214  TAD                  4014  7740  CONSTANT
4006  3215  DCA                  4015  0000  COUNTER
4007  2200  ISZ 4000
```

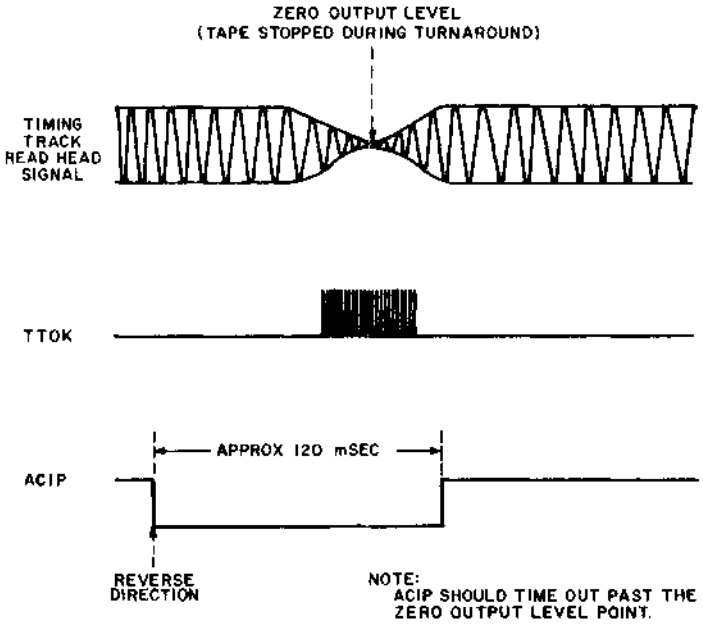


Figure 5-4 ACIP Delay Waveform

5.7 MAGTAPE TRANSPORT MECHANICAL ADJUSTMENTS

All pertinent mechanical adjustments for the MAGtape transport are described in Section 3.5.1 of this manual. The user should fully understand the operation of the transport and MAGtape control before performing any adjustments to these systems.

5.7.1 Relay Adjustment

The gap between contacts of relay M0 (back right relay when viewed from the front of the transport) is a very important adjustment. The essential function of relay M0 is shown in Figure 5-5.

Since the contacts are across the line, the contact gap should be between 0.018 to 0.025 in. Care must be taken to ensure that the contacts actually do make (i.e., armature travel is at least 0.010 in. greater than gap).

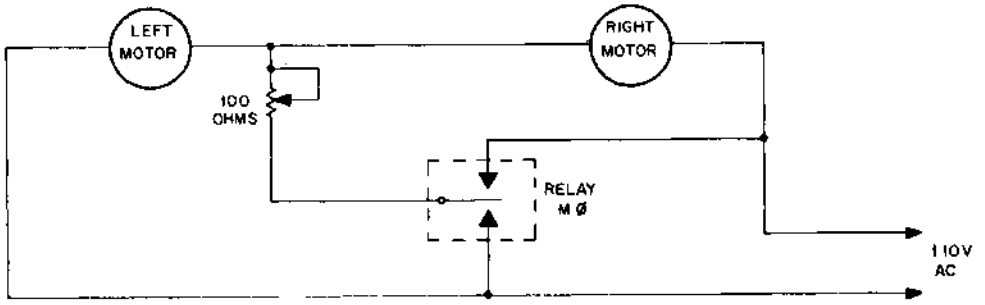


Figure 5-5 Relay M0 Function

5.8 A-D CONVERTER TEST

An EDC Voltage Source, Model VS-11 or equivalent is required for this test.

a. Execute the program ADTST from the Library System. All sense switches should be down. A display of digits representing the A-D conversion of 16 analog channels and an accompanying channel number is displayed for each channel. Press the carriage return key on the teletypewriter to get back to the Library System.

b. Channels 0-7 are controlled by the knobs. Adjust the knobs up and down to see that they all reach ±377. If not, adjustment or replacement of the sample and hold module may be necessary. The value of +376 should appear when a potentiometer is approximately 1/4 turn down from the clockwise stop. If there is considerable deviation, set the potentiometer there and adjust the A401 offset control (Figure 5-6) until a value of +376 appears. The value of -376 should occur when the knob is about 1/4 turn from the counterclockwise stop. If not, then adjust the A401 gain control. Repeat the above procedure until both end conditions are met.

NOTE: Offset is a fairly coarse control.

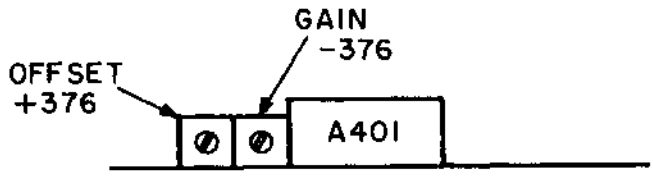


Figure 5-6 A401 Offset and Gain Adjustments

c. Channels 10-17 are associated with the preamplifiers, located on the data terminal panel. They must be precisely adjusted for gain and offset. Preamplifier adjustment controls are shown in Figure 5-7.

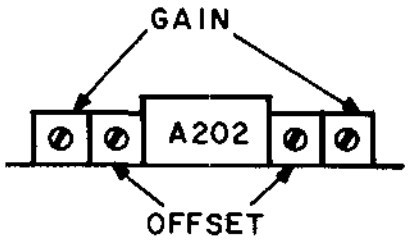


Figure 5-7 A202 Preamplifier Adjustments

With no input connected, each preamplifier can be trimmed for offset. Each offset potentiometer can be adjusted to give +000 on the scope display.

d. Set the EDC source to +.9960V and connect it to a channel input. The preamplifier gain potentiometer can be adjusted to give +376 on the display. Switch the source back to 0V and check the offset. Readjust the offset trim if necessary, and recheck the gain. Continue the procedure until both gain and offset are correct. Do this for each channel.

NOTE: If a precision voltage source is not available, any dc source can be used and the preamplifier gain adjusted to the accuracy of that source.

5.8.1 A-D Multiplex Extension Test

Lifting sense switch 0 will change the display to channels 20-37. If preamplifiers are used, they can be adjusted using the regular preamplifier procedure.

NOTE: This is only done on systems with optional A-D channels.

5.9 DISPLAY OSCILLOSCOPE TEST

a. Execute the program MARTINI from the Library System. The oscilloscope channel switch is on the lower left of the right-hand plug-in (see Figure 5-8 for oscilloscope adjustment locations).

(1) Set switch fully counterclockwise. Only the martini should be displayed.

(2) Set switch to center position. Both martini and olive should be displayed.

(3) Set switch fully clockwise. Only the olive should be displayed.

b. Execute the program SCOPCL from the Library System.

(1) Adjust oscilloscope preamplifier gain and position controls (screwdriver adjustments on the front of each plug-in) so the calibrate pattern fills the screen and is centered.

(2) Adjust the Trace Alignment Control, so the display is not tilted.

c. Return to the Library System. Execute the program LAPGO. The number 0001 will appear on the oscilloscope.

(1) Adjust Focus and Intensity so that the dots comprising the character display are round and in focus.

(2) Adjust the intensity so the display is quite bright, but not bright enough to cause degradation of the spot size. The phosphor may be burned if a very bright, fast, and small display is set up.

(3) Type GU Line Feed. The Library System will be restarted.

(4) Execute the program INDIS and press the F key twice.

(5) Push the Intensity Button. The display should intensify noticeably, but the characters should not become excessively bright or blurred. If this intensity differential adjustment needs to be changed, the oscilloscope must be removed from the LINC-8. The bottom cover of the oscilloscope is then removed. The intensity differential adjustment potentiometer is mounted on a bracket located inside the oscilloscope near the intensity button.

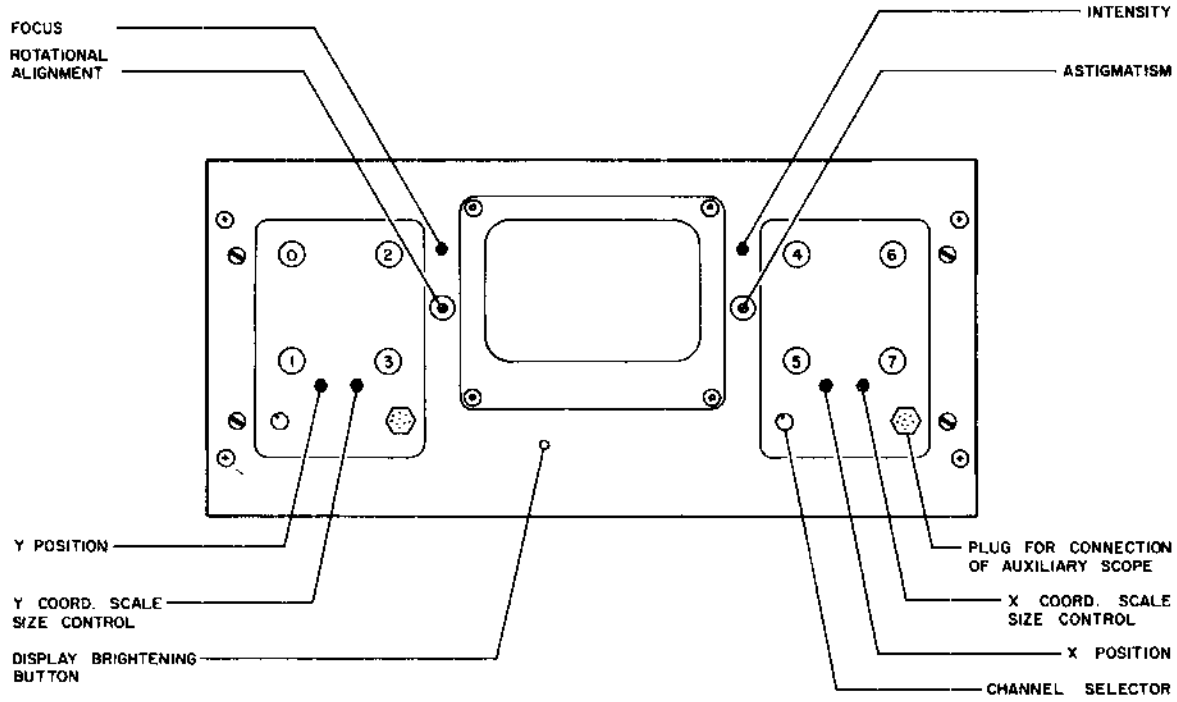


Figure 5-8 Display Oscilloscope Adjustments

5.10 DATA TERMINAL PANEL TEST

The following tests require that the computer be fully operational and able to execute programs from GUIDE.

5.10.1 Chime Test

The chime can be tested by executing the following procedure.

a. Turn the CHIME switch on.

b. Press the CLEAR lever.

c. Do 0011 (CLR).

d. Start 20. The LINC-8 will halt. The chime should ring on the start 20.

e. Turn the CHIME switch off, and then back to on. The chime should ring as the switch is turned on.

5.10.2 Speaker Test

The first step in checking the speaker is to load and start the GUIDE program. The display of EXECUTE THE PROGRAM should be accompanied by an audio tone from the speaker. By varying the audio control (concentric with the CHIME switch), sound intensity should vary from 0 to maximum with clockwise rotation.

5.10.3 Relay Test

The relay contacts can carry 1A resistive loads at 110V ac.

The user will require a dc voltage source for this test.

a. Execute the program RELTS8 from the Library System.

b. Connect the voltage source in series with the normally open contacts of relay 0 and the channel 10 analog input as shown in Figure 5-9.

c. Press the 0 (zero) key on the Teletype.

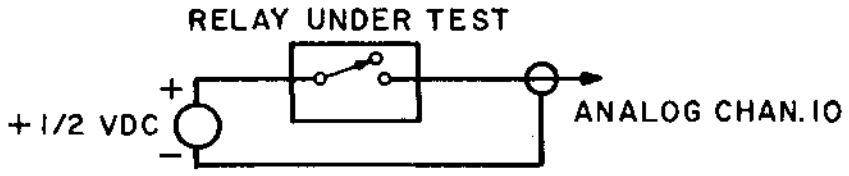


Figure 5-9 Relay Test Setup for N.O. Contacts

d. Set the scope channel selection switch to the central (both) position. The oscilloscope should display the patterns shown in Figure 5-10. The two steps indicate proper relay operation.

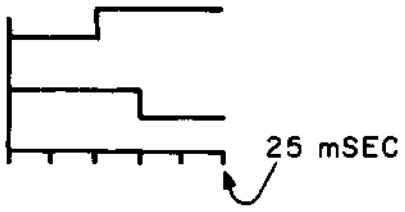


Figure 5-10 Waveform for N.O. Contacts

e. Repeat the procedure for all realy normally open contacts. Hit 0 on the keyboard to test relay 0, hit 1 for relay 1, etc.

f. Connect the relay normally closed contacts in place of the normally open contacts (Figure 5-11).

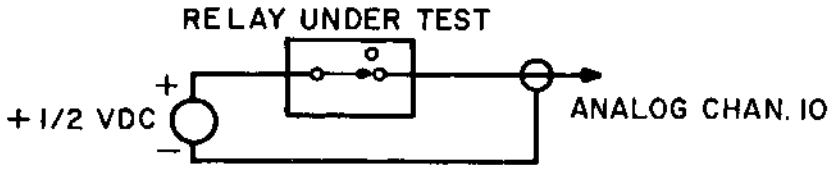


Figure 5-11 Relay Test Setup for N.C. Contacts

g. Hitting a key will test a relay, as before. The display will appear as shown in Figure 5-12. Again, the steps indicate proper contact operation.

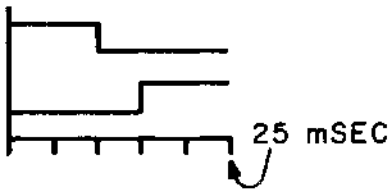


Figure 5-12 Waveform for N.C. Contacts

h. Repeat steps a through g to test all relay normally closed contacts.

5.10.4 External Levels Test

The user should execute the program XLTST from GUIDE for this test. Grounding an external level line will extinguish the corresponding bit in the LINC A-Register.

a. Ground the following pins in the Data Terminal Panel, and check that the corresponding A-register bit becomes 0.

Pin Location		LINC A-Register Bit
B34	D	00
	E	01
	H	02
	K	03
	M	04
	P	05
	S	06
	T	07
	V	08
B35	S	09
	T	10
	V	11

5.11 E-STOP AND F-STOP TEST

a. Place the following program into LINC memory.

Program			E-Stop Locations	F-Stop Locations
Location	Instruction	Mnemonic		
1	6002	JMP 2	0, 21, 2077	1, 2, 4, 10, 20, 22, 40, 100, 200, 400, 1000
2	6004	JMP 4		
4	6010	JMP 10		
10	6020	JMP 20		
20	1100	ADA		
21	2077	2077		
22	6040	JMP 40		
40	6100	JMP 100		
100	6200	JMP 200		
200	6400	JMP 400		
400	7000	JMP 1000		
1000	6001	JMP 1		
2077	4001	CONSTANT (1)		

b. Restart the LINC at location 20.

c. Place the LINC in the E-stop mode by lifting the E STOP/F STOP switch. The LINC should stop at all of the indicated addresses (to be set in the left switches) and no others.

d. Place the LINC in the F-stop mode by pressing the E STOP/F STOP switch. The LINC should stop at all indicated addresses (to be set in the left switches) and no others.

5.12 IBI FUNCTION TEST

Using the program given in Section 5.11 or using any other LINC program, press the LINC IBI switch while the program is running. The program should stop and the IBI indicator should light. Lifting the RESUME switch should cause the program to continue on.

5.13 AUTO-RESTART FUNCTION TEST

After loading the program given in Section 5.11, press the IBI switch and then lift the AUTO RESTART switch. Both the IBI and AUTO RESTART indicators should be lit with the program operating in the auto restart mode. Program speed may be varied by the auto restart DELAY controls. The incrementing of the LINC A-register by the program provides a method of observing program speed both visually and by listening to the speaker (volume adjusted by the audio control).

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