8266-B,F,W • 8267-B,F,W

DESCRIPTION

The 8266/8267 2-Input, 4-Bit Digital Multiplexer is a monolithic array utilizing familiar TTL circuit structures. The 8267 features a bare-collector output to allow expansion with other devices.

The multiplexer is intended for use at the inputs to adders, registers and in other parallel data handling applications.

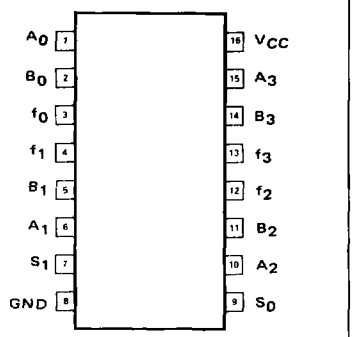
SPEED/PACKING AVAILABILITY

8266,67—B,F,W

82S66,S67—B,F

PIN CONFIGURATION

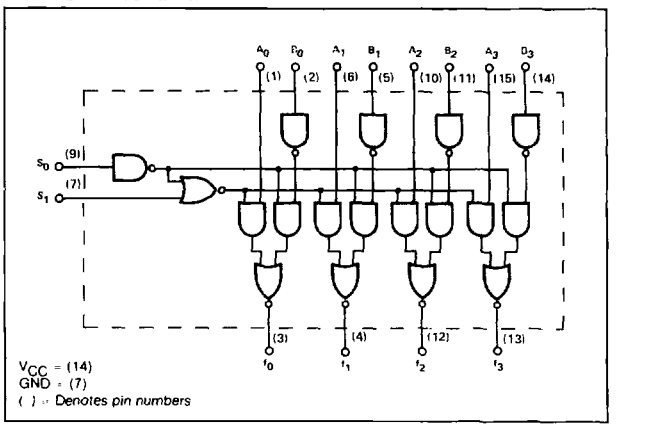
B,F,W PACKAGE



The multiplexer is able to choose from two different input sources, each containing 4 bits: A = (A_0, A_1, A_2, A_3), B = (B_0, B_1, B_2, B_3). The selection is controlled by the input S_0, while the second control input, S_1, is held at zero.

For conditional complementing, the two inputs (A_n, B_n) are tied together to form the function TRUE/COMPLEMENT, which is needed in conjunction with added elements to perform ADDITION/SUBTRACTION. Further, the inhibit state S_0 = S_1 = 1 can be used to facilitate transfer operations in an arithmetic section.

LOGIC DIAGRAM



TRUTH TABLE

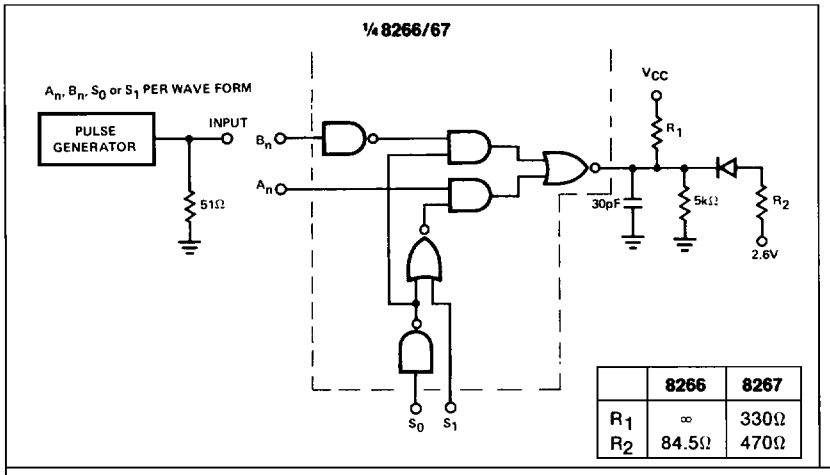
SELECT LINES		OUTPUTS
S_0	S_1	f_n (0, 1, 2, 3)
0	0	B_n
0	1	B_n
1	0	$\overline{A}_n$
1	1	1

SWITCHING CHARACTERISTICS T_A = 25°C, V_{CC} = 5V

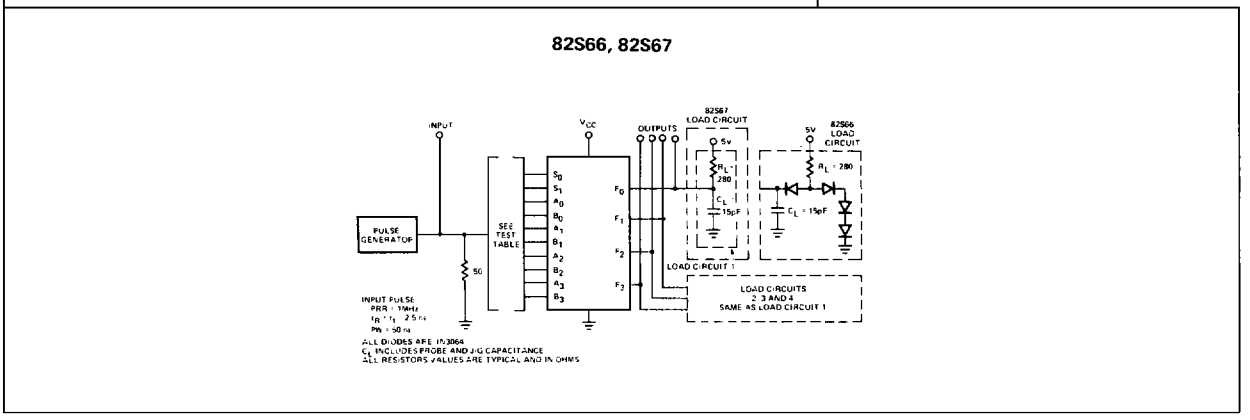
	LIMITS								
	8266		8267		82S66		82S67		
PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNIT
Propagation delay									
S_0 to f_n (short path)	18	28	18	28	12	18	15	20	ns
S_0 to f_n (long path)	20	30	27	36	—	—	—	—	
A_n to f_n	13	20	15	20	5	10	8	12	
B_n, S_1 to f_n	14	25	21	28	—	—	—	—	
S1 to fn					10	15	13	18	
Bn to fn					8	12	10	15	

LOGIC

AC TEST FIGURE



	8266	8267
R_1	∞	330Ω
R_2	84.5Ω	470Ω



AC TEST TABLE—82S66,82S67

TEST NO.	INPUTS										OUTPUTS			
	S_0	S_1	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3
1	1	PG	1	1	1	1	1	1	1	1	T			
2	1	PG	1	1	1	1	1	1	1	1	T	T	T	T
3	PG	0	1	1	1	1	1	1	1	1	T	T		T
4	0	0	0	0	0	PG	0	0	0	0		T		
5	0	0	0	0	0	0	0	PG	0	0			T	
6	1	0	PG	1	0	1	0	1	0	1	T			
7	1	0	0	1	0	1	0	1	PG	1				T

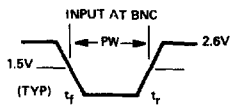
"1" = 2.7V "0" = Output

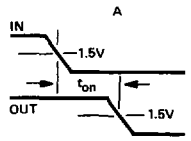
NOTES:
1. AC Test Jigs Must Not Have Any Switches.
2. AC Test Jigs Must Have Less Than ⅛ Inch Lead Length From Package Pins.

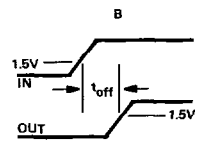
VOLTAGE WAVEFORMS

8266, 8267

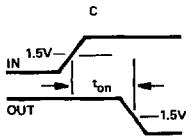
NON-INVERTING PATHS

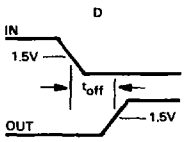






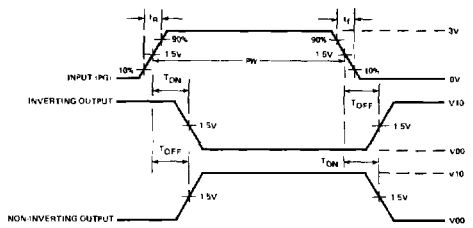
INVERTING PATHS



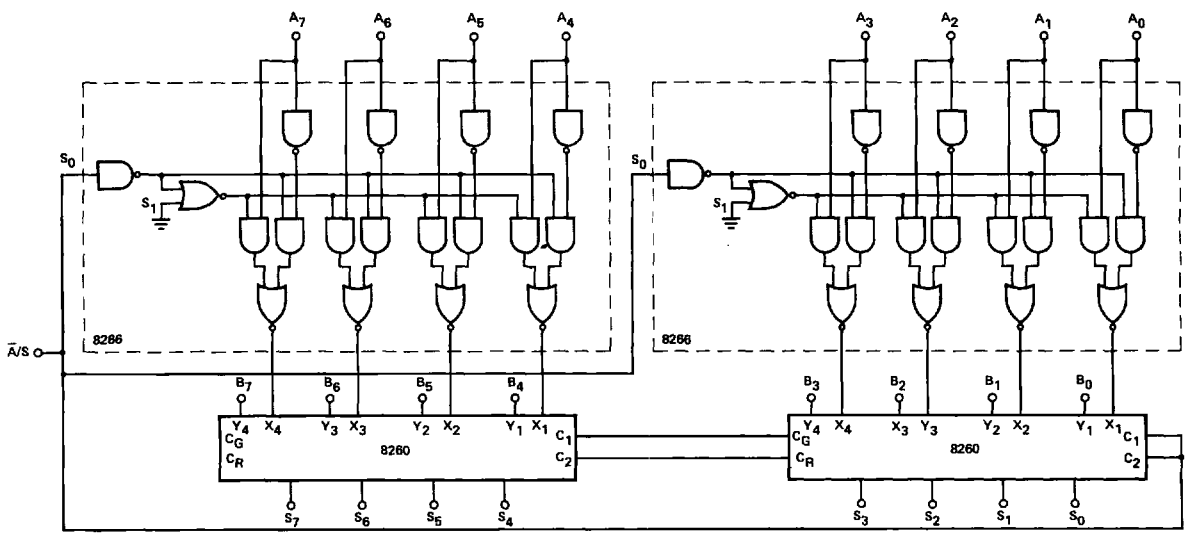


$t_r = t_f \leq 5ns$
Amplitude = 2.6V
PW = 200ns
PRR < 1MHz

82S66, 82S67



TYPICAL APPLICATIONS



The 8266 can be used in conjunction with the 8260 (Look-Ahead Carry Adder) to form an adder-subtractor.

LOGIC