

digital

RX01

Engineering Drawings

Digital Equipment Corporation

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CUSTOMER PRINT SET INDEX

THIS IS PRINT SET

RX01 FLOPPY DISK DRIVE
FLOPPY DISK CONTROL BOARD
RX01 FIRMWARE LISTING
READ/WRITE CONTROL BOARD
H771 POWER SUPPLY

SEQUENCE 77

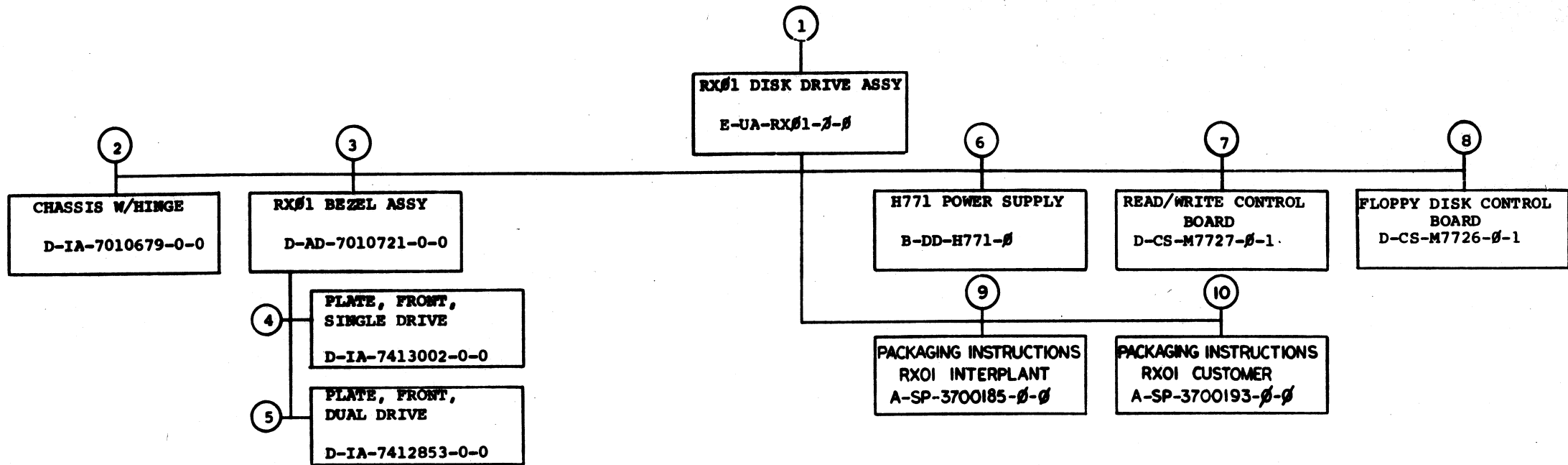
B-DD-RX01-0
D-CS-M7726-d-1
K-SP-RX01-0-2
D-CS-M7727-0-1
B-DD-H771-0

SEQUENCE 77

VAR	UNIT VARIATIONS TITLE	PRINT SET			
RX01-AA	SINGLE FLOPPY DISK, 115V, 60 HZ	X			
RX01-AC	SINGLE FLOPPY DISK, LOW V, 50HZ	X			
RX01-AD	SINGLE FLOPPY DISK, HIGH V, 50HZ	X			
RX01-BA	DUAL FLOPPY DISK, 115V, 60 HZ	X			
RX01-BC	DUAL FLOPPY DISK, LOW V, 50HZ	X			
RX01-BD	DUAL FLOPPY DISK, HIGH V, 50HZ	X			
RX01-CA	ONE REPLACE DRIVE, 60 HZ	X			
RX01-CC	ONE REPLACE DRIVE, 50 HZ	X			
RX01-DA	RX01-BA W/O BEZEL ASSY	X			
RX01-DC	RX01-BC W/O BEZEL ASSY	X			
RX01-DD	RX01-BD W/O BEZEL ASSY	X			

DEC 16-1981-1602-1A-0022

REVISIONS REV A B CHG. NO. RX01-2 RX01-3 DATE 6-76 7-76				USED ON OPTION/MODEL RX8 RX11		DRN. W. McCarthy CHK'D. McCarthy PROJ ENG. McCarthy PROJ. Miller FIELD/SERV. Miller		DATE 2/3/75 DATE 5/29/75 DATE 6/3/75 DATE 11/1/75		TITLE RX01 FLOPPY DISK DRIVE		
SIZE B DD		CODE DD			NUMBER RX01-0		REV B					
SHEET 1 OF 3				DIST								

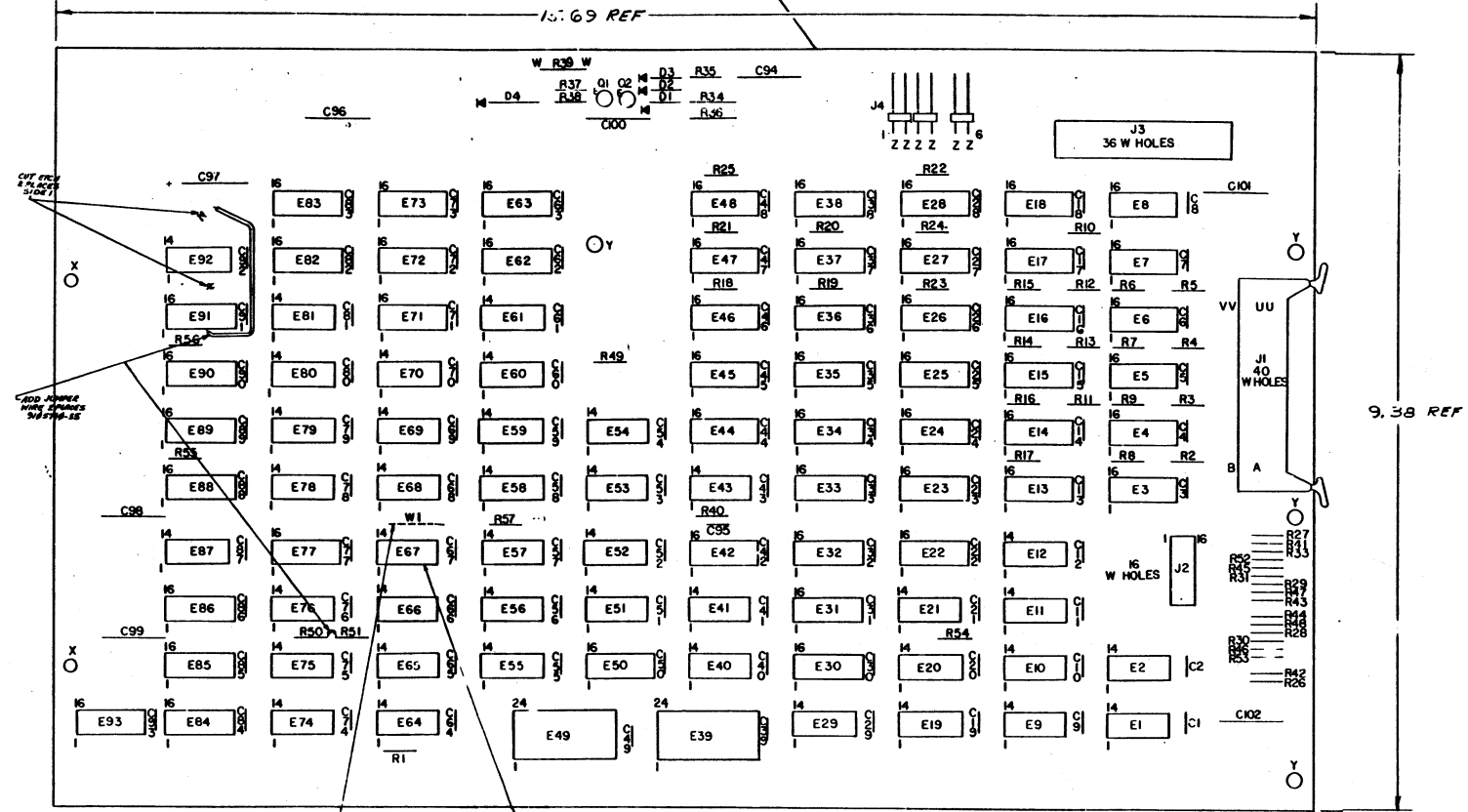


TITLE	SHEET	OF	SIZE	CODE	NUMBER	REV
RX01 FLOPPY DISK DRIVE	2	3	B	DD	RX01-0	B

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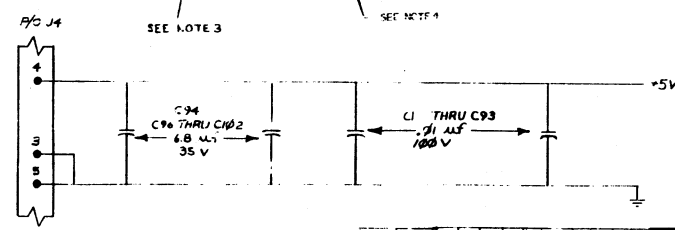
NOTES:

- REPRESENTS A 1/8 DIA PAD LOCATED ON SIDE 2 UNLESS OTHERWISE SPECIFIED
- A. ALL RESISTORS ARE 1/4 W, ± 5%
B. ALL UNUSED PINS FOR J1 ARE TIED TO GND
- INSTALL JUMPER W1 AFTER MODULE TEST
- MOUNT E67 1/8" ABOVE SURFACE OF MODULE



23-11A2	7	16
202	9	10
3040		8
74155	5	16
74174	5	16
74161	8	10
74174	8	16
74123	5	16
4-103	11	4
74H106	13	5
7489	8	16
74150	12	24
7442	8	16
8866	8	16
74193	8	16
74154	12	24
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPT WHERE STATED ABOVE
IC PIN LOCATIONS



DATE	11/29/75
DESIGNER	CHARLES YOUSE
DATE	12-15-75
DESIGNER	John Carter
DATE	12-15-75
DESIGNER	P. KOTSCHENTHER
DATE	12-15-75
DESIGNER	P. KOTSCHENTHER
DATE	12-15-75
DESIGNER	P. KOTSCHENTHER
DATE	12-15-75
DESIGNER	P. KOTSCHENTHER

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST				
FIRST USED ON OPTION MODEL				
ETCH BOARD REV. B				
DATE 11/29/75				
DRAWN BY [Signature]				
CHECKED BY [Signature]				
APPROVED BY [Signature]				
TITLE FLOPPY DISK CONTROLLER				
DCS M7726-0-1				
SCALE				
SHEET 7 OF 9				

SEMICONDUCTOR CONVERSION CHART

DCS M7726-0-1

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PARTS LIST

QTY	REF	DESIGNATION	DESCRIPTION	PART NO.	ITEM
	REF		X-Y COORDINATE HOLE LOCATION	KCO-M7726-B-4	1
	REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M7726-B-5	2
	REF		MODULE ECO HISTORY	B-MH-M7726-B-6	3
1			ETCHED CIRCUIT BOARD	5011390	4
1	J3		RECEP 36 PIN (BENOEK)	8-MD-559 07-1	5
1	J2		I/C SOCKET, 16 PIN BOLD, LOW PROFILE	1211813-02	6
1	A37		RES 10K 1/4W 5% CC	1300479-00	7
3	C 99, C96 - C102		CAP 6.8 uF 35V 10% S.TANT	1005306-00	8
93	C1 - C93		CAP .01 uF 50V AXIAL CER	1001610-00	9
1	C95		CAP 12PF 100V 5% CC	1002087-00	10
3	D1 - D3		DIODE 1N4004	1105796-00	11
1	D4		DIODE 1N746A 3.8V 5% CC	1104860-00	12
1	E 39		RES 100 1/2W 5% CC	1300228-00	13
3	J4		HEADBR. 2PIN (MALE)	1212204-00	14
8	E2, E4, E6, E8, E10 E12, E14, E16		RES 470 1/4W 5% CC	1300316-00	15
6	E27, E29, E31, E47, E52 E43, E41, E45		RES 390 1/4W 5% CC	1300309-00	16
5	E1, E49 - E51, E57		RES 3K 1/4W 5% CC	1300432-00	17
3	E70, E28, E30, E38 E42, E48, E46, E44, E53		RES 180 1/2W 5% CC	1301322-00	18
8	E3, E5, E7, E9, E11 E13, E15, E17		RES 820 1/4W 5% CC	1301775-00	19
1	E35		RES 300 1/4W 5% CC	1301425-00	20
3	E18 - E25		RES 2K 1/4W 5% CC	1302388-00	21
1	E34		RES 261 1/4W 1% MF	1302873-00	22
1	E33		RES 287 1/4W 1% MF	1305124-00	23
1	E44		RES 32K 1/2W 5% CC	1303179-00	24
3	E54 - E56		RES 1K 1/2W 5% CC	1300345-00	25
1	E42		TRANS 1N4148	1507205-00	26
1	E41		TRANS 1N4148	1507206-00	27
1	E45		TRANS 1N4148	1905597-00	28
5	E43		I.C. 74121	1905575-00	29
2	E42, E64		I.C. 74122	1905576-00	30
1	E73		I.C. 74123	1905580-00	31
1	E55		I.C. 74124	1905635-00	32
1	E54		I.C. 74125	1909004-00	33
3	E68, E70		I.C. 74126	1909056-00	34
3	E50, E72		I.C. 74127	1909267-00	35
5	E9, E69, E78, E79, E92		I.C. 74128	1909667-00	36
2	E39, E76		I.C. 74129	1909586-00	37
1	E 5		I.C. 74130	1909701-00	38
2	E1, E7		I.C. 8251	1909705-00	39
1	E61		I.C. 74134	1909931-00	40
3	E74, E92		I.C. 74135	1910011-00	41
4	E88, E85, E90, E9		I.C. 74136	1910015-00	42
2	E27, E37		I.C. 8254	1909934-00	43
1	E22		I.C. 74137	1910546-00	44
1	E65		I.C. 74137	1910591-00	45
1	E49		I.C. 74138	1910153-00	46
2	E11, E12		I.C. 74139	1910155-00	47
2	E97, E98		I.C. 74139	1910394-00	48
1	E58		I.C. 74140	1910408-00	49
3	E80, E81, E87		I.C. 74143	1910409-00	50
1	E42		I.C. 74122	1910432-00	51

REVISIONS		
CHK	CHANGE NO	REV

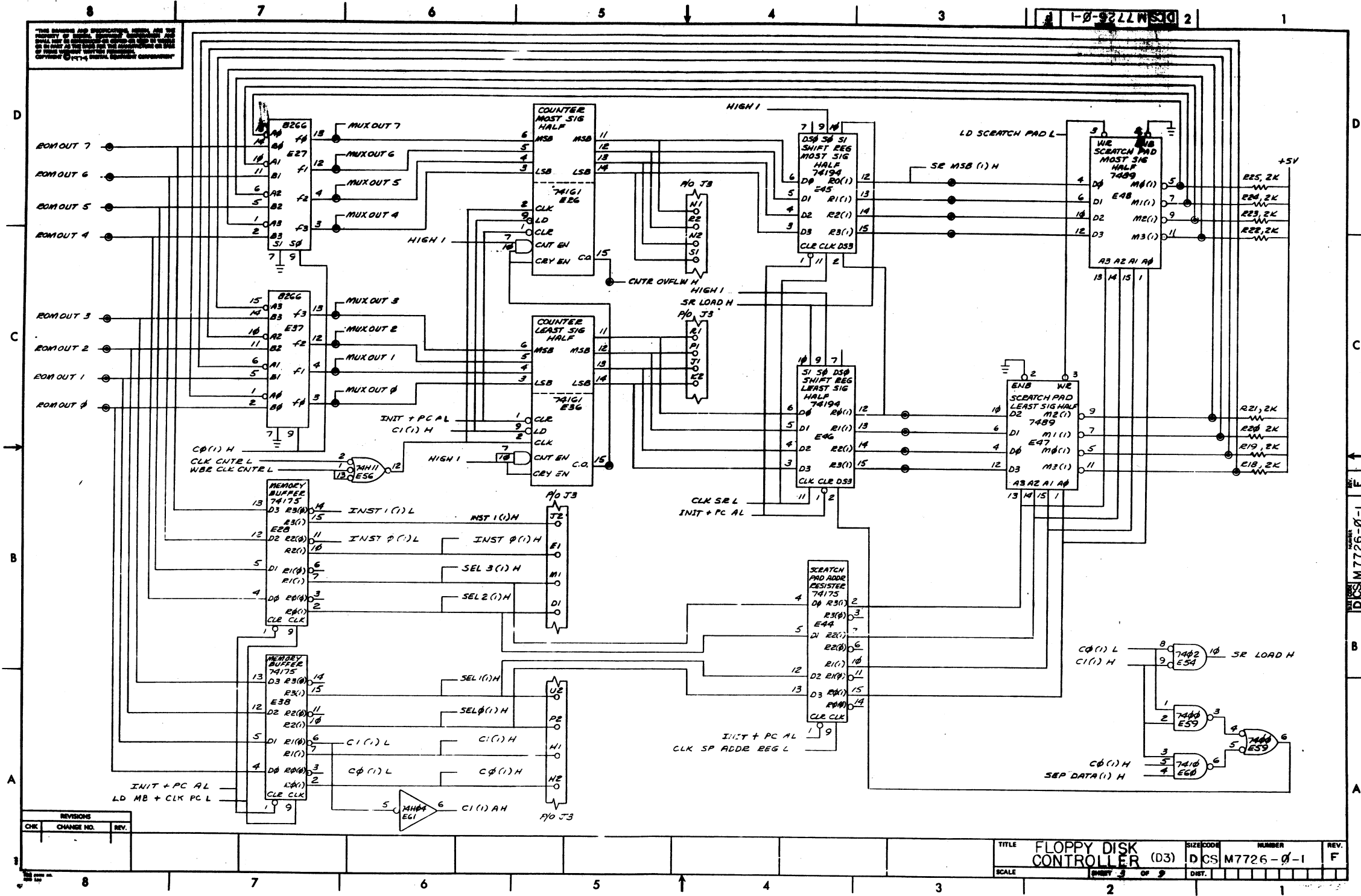
PARTS LIST

QTY	REF	DESIGNATION	DESCRIPTION	PART NO.	ITEM
2	E45, E46		I.C. 74194	1910623-00	52
8	E23, E24, E25, E26 E30, E31, E32, E36		I.C. 74161	1910650-00	53
3	E84, E85, E86		I.C. 74174	1910652-00	54
7	E53		I.C. 74227	1910878-00	55
3	E28, E38, E44		I.C. 74175	1910651-00	56
2	E10, EGG		I.C. 8240	1911469-00	57
1	E33		I.C. 2102 680 NS	2111318-02	58
					59
6	E35, E39, E62, E63 E73, E83		8PINS IC SPACER		60
1	E67		CRYSTAL OSCILLATOR 20MHZ	1811660-00	61
7	E41, E71, E93, E52		I.C. 74137	1910544-00	62
1	E51		I.C. 74140	1909057-00	63
1	E77		I.C. 74140	1909058-00	64
					65
NR			750 ANG BOLD WIRE (VCL)	310290-55	66
1	J1		CONN 40 PIN ET ANG. HDG	1209941-02	67
1	(J1)		LATCH, LEFT FOR ET ANG. HDG	1209941-03	68
1	(J1)		LATCH, RIGHT FOR ET ANG. HDG	1209941-04	69
1	E13		I.C. 256 X 4 ROM FLD0L	2311A2	70
1	E3		I.C. 256 X 4 ROM FLD0H	2311A2	71
1	E14		I.C. 256 X 4 ROM FLD1C	23257A2	72
1	E4		I.C. 256 X 4 ROM FLD1H	23258A2	73
1	E15		I.C. 256 X 4 ROM FLD1L	23115A2	74
1	E5		I.C. 256 X 4 ROM FLD2H	23116A2	75
1	E16		I.C. 256 X 4 ROM FLD3L	23117A2	76
1	E6		I.C. 256 X 4 ROM FLD3H	23118A2	77
1	E17		I.C. 256 X 4 ROM FLD4L	23259A2	78
1	E7		I.C. 256 X 4 ROM FLD4H	23260A2	79
1	E18		I.C. 256 X 4 ROM FLD5L	23121A2	80
1	E8		I.C. 256 X 4 ROM FLD5H	23122A2	81
1	R33		RES 150 1/4W 5% CC	1300250-00	82

SPARE I.C. GATES			
TYPE	LOCATION	PINS	DESCRIPTION
74004	E61	1,2	INVERTER
7404	E64	12,13	INVERTER
7404	E76	12,13	INVERTER
7408	E11	1,2,3,8,9,18	2 INPUT AND
7408	E72	1,2,3,9,5,6,8,18	2 INPUT NAND
7437	E65	8,9,18	2 INPUT NAND BUFFER
8881	E2	8,9,18	2 INPUT NAND G.C.
7408	E51	3,4,5,6	3 INPUT NAND
7404	E77	1,2,4,5,6	4 INPUT NAND BUFFER
7402	E64	4,5,6	2 INPUT NOR
8640	E66	2,6,7,11,12,13,3,5,6	2 INPUT NOR RCVR
7427	E53	1,2,12,13	3 INPUT NOR
7406	E92	4,5,6	2 INPUT XOR
7406	E74	1,2,3,4,5,6	2 INPUT XOR
74574	E73	1,2,3,4,5,6	DTYPE FLIP FLOP
74016	E58	1,2,3,4,14,15,16	J K FLIP FLOP
74123	E42	1,2,3,4,13,14,15	ONE SHOT

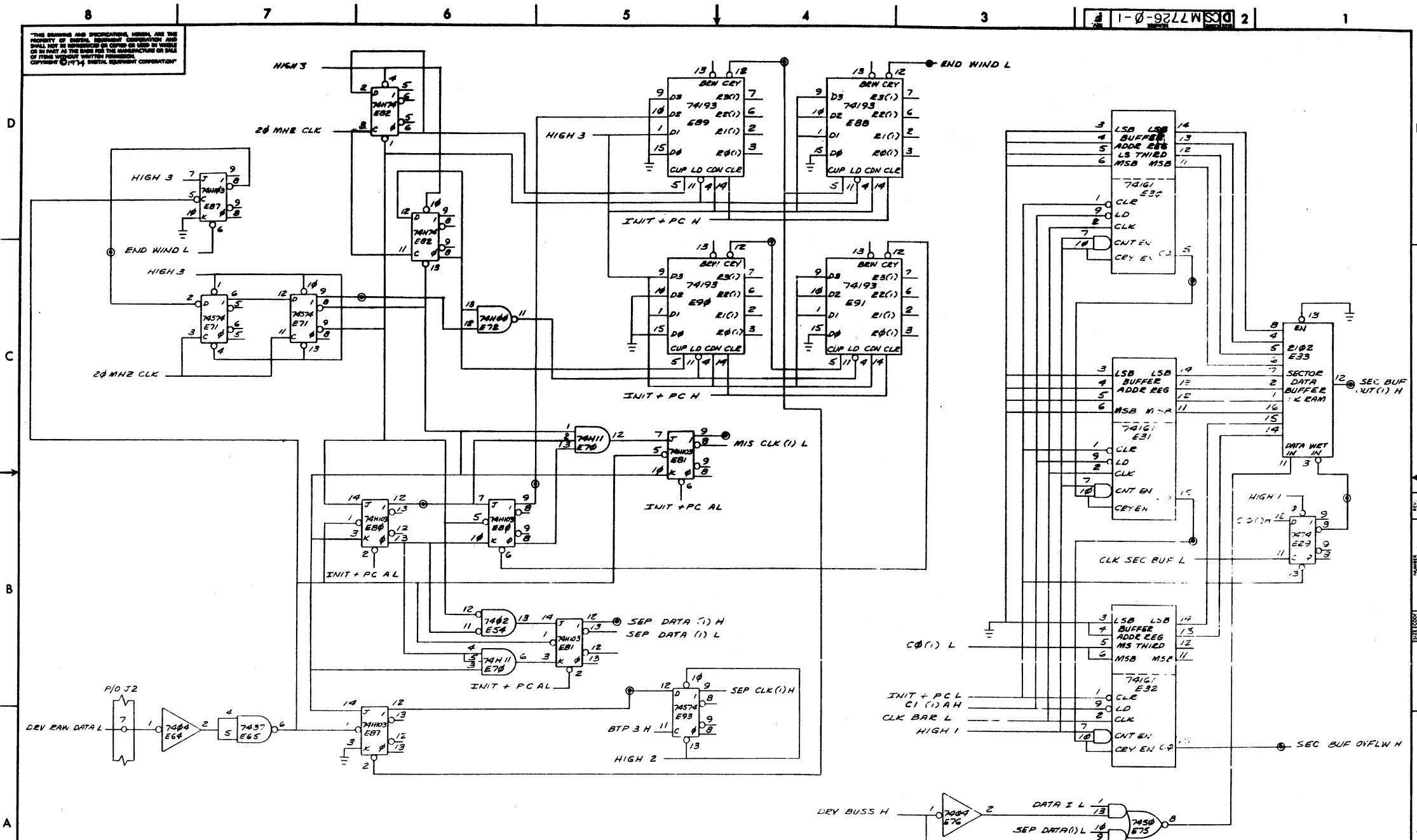
ALLOWABLE SUBSTITUTIONS					
PREFERRED			REPLACEMENT		
TYPE	ITEM #	P.N.	TYPE	ITEM #	P.N.
7481	48	1910376-00	3101A	1910653-00	
7421	48	1910376-00	8725	1911162-00	

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CHK	CHANGE NO.	REV.

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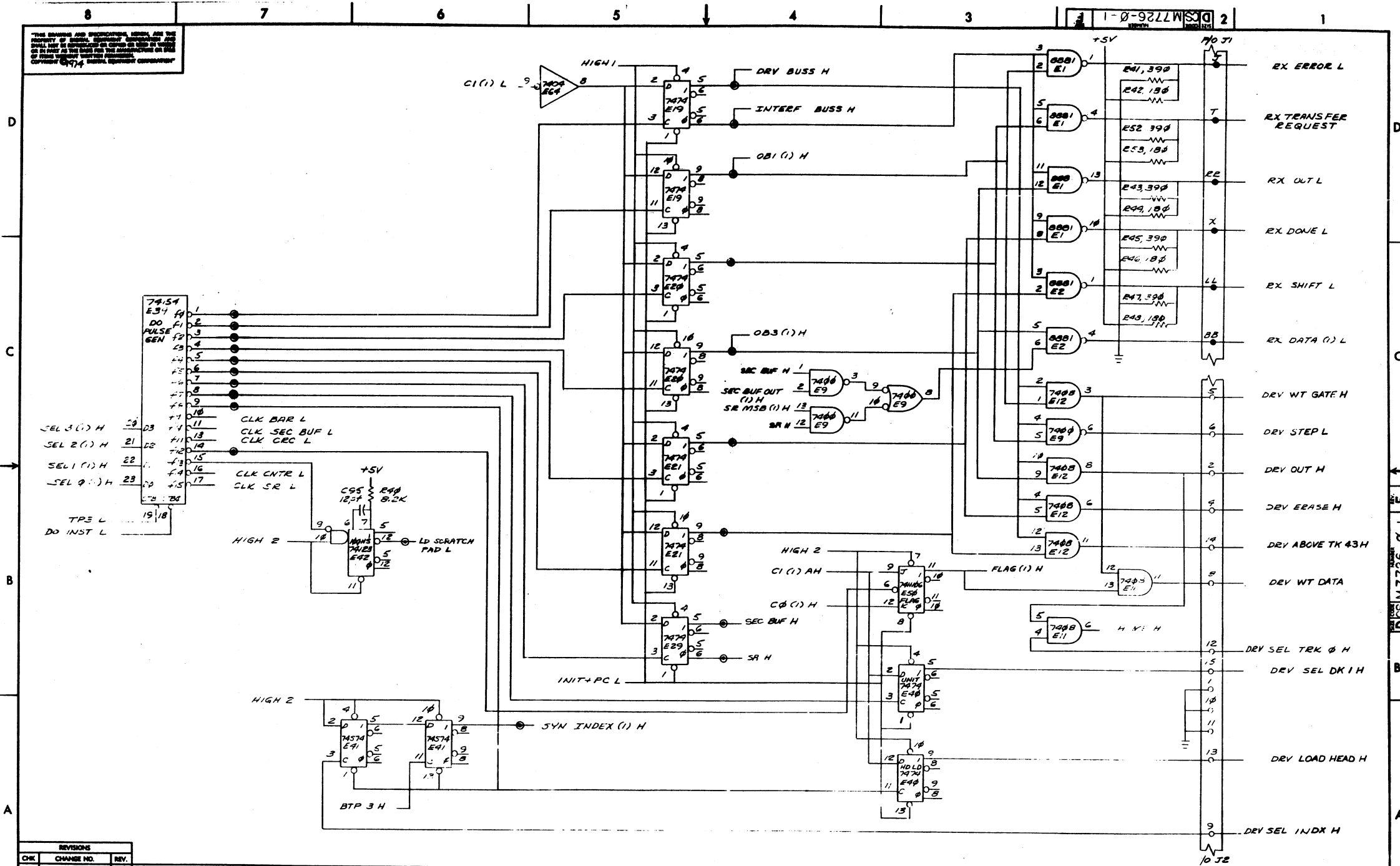
REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	FLOPPY DISK CONTROLLER (D4)	SIZE CODE	NUMBER	REV.
SCALE	1:1	SHEET	4 OF 9	DIST.

DCS M7726-0-1

1-0-922LWS02

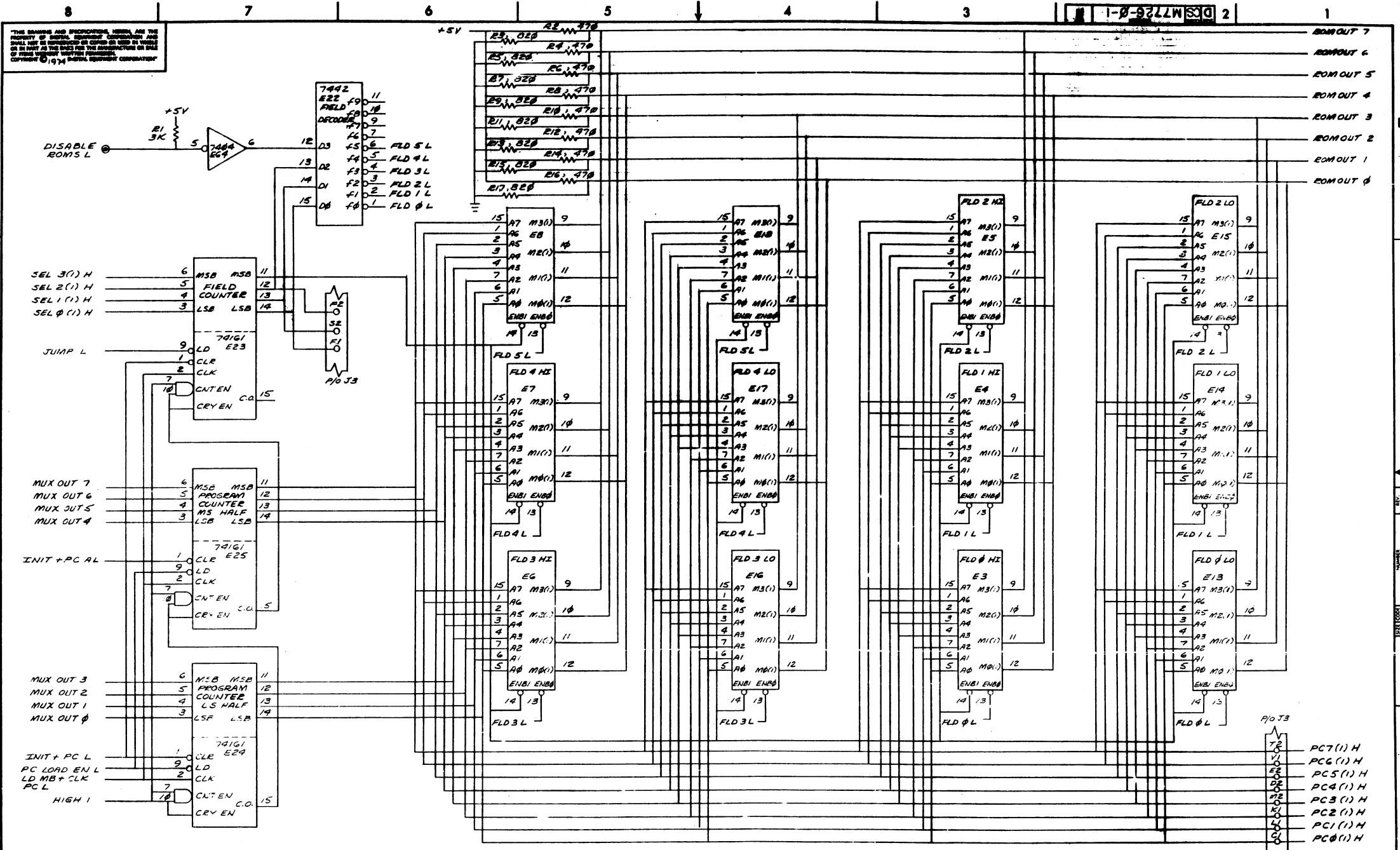
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DCS M 7726-0-1

MS 80



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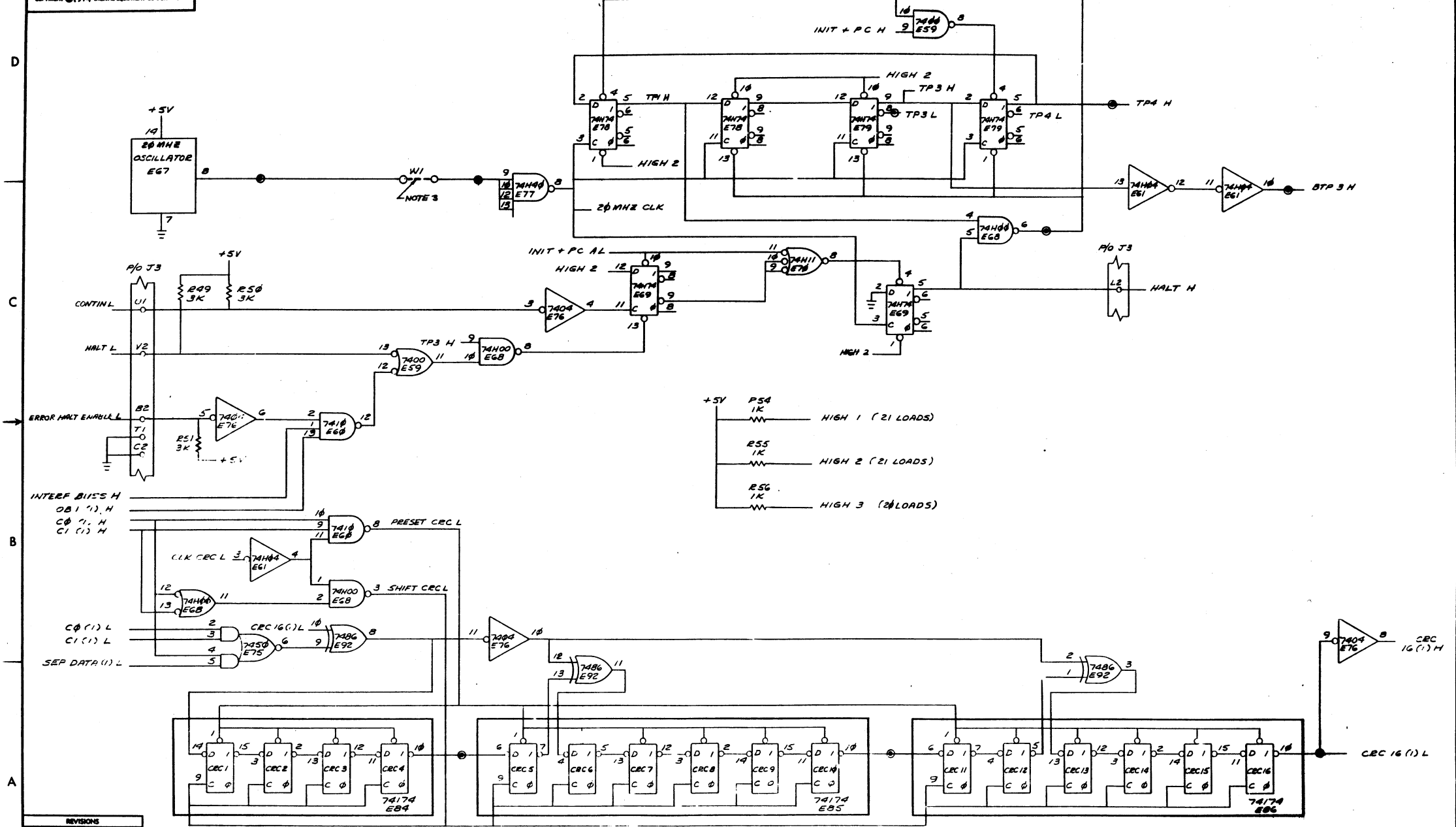
1-0-9211W SCD 2

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE FLOPPY DISK CONTROLLER (D6) SIZE CODE DCS M7726-0-1 NUMBER 7 REV. F
SCALE 1:1 SHEET 2 OF 3 DWT.

DCS M7726-0-1

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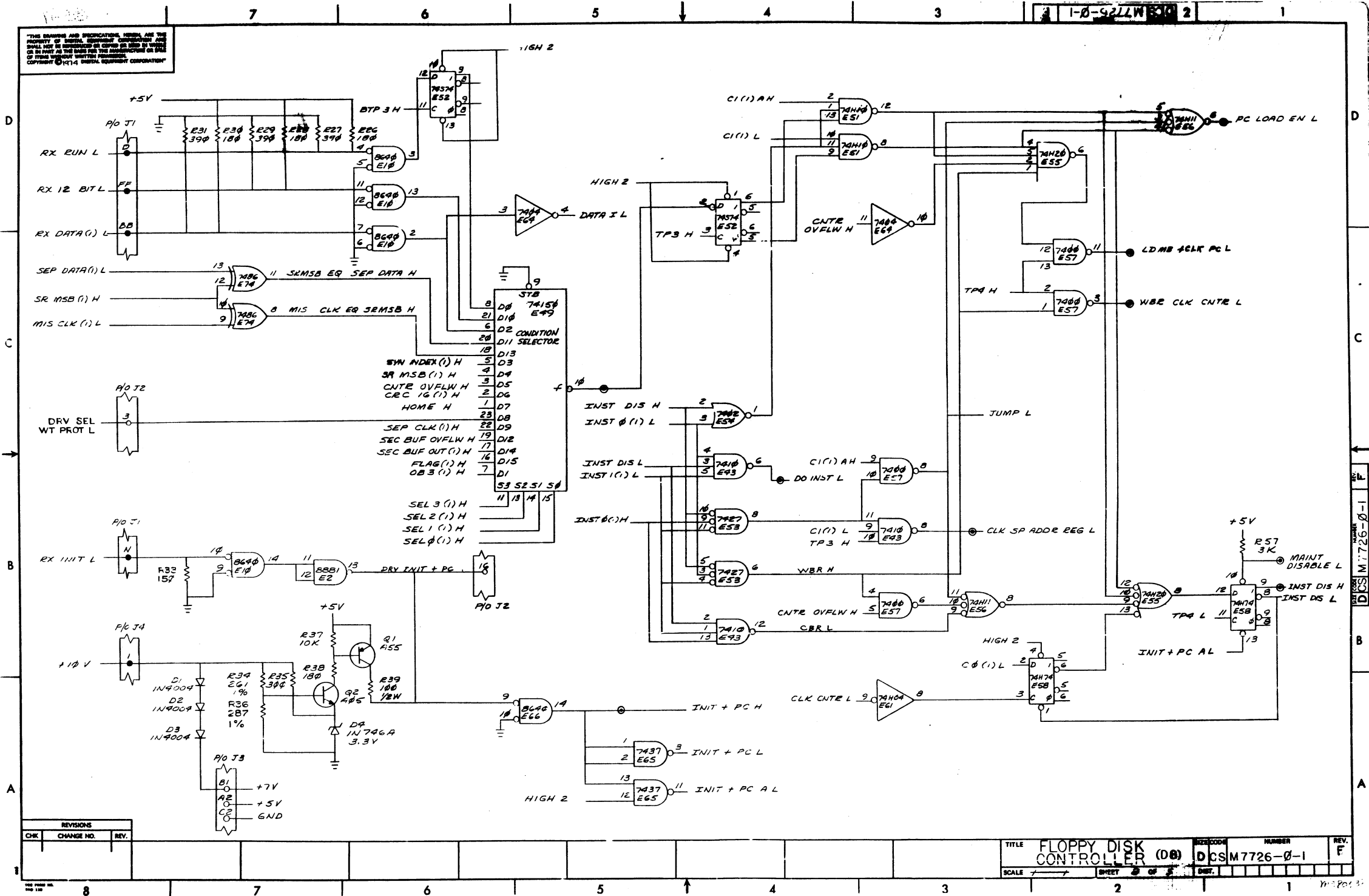


REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	FLOPPY DISK CONTROLLER (DT)	NUMBER	DCSM7726-0-1	REV.	F
SCALE		SHEET	7 OF 8		

DCSM7726-0-1

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INTERFACE REFERS TO SIGNALS ON THE INTERFACE BUSES
 DRIVE REFERS TO SIGNALS ON THE DRIVE BUSES
 POWER SUPPLY REFERS TO VOLTAGES FROM THE POWER SUPPLY
 KN11 REFERS TO SIGNALS ON J3 THE MAINTENANCE CONNECTOR

SIGNAL NAME	ORIGIN	DESTINATION			
BTP J H	D7-C1	D4-A5, D5-A6, D6-D6	OB1 (1) H	D5-D4	D7-B8
CLK BAR L	D5-C7	D4-A3	OB3 (1) H	D5-C4	D8-B6
CLK CNTR L	D5-B7	D3-B7, D8-A4	PC 0 (1) H	D6-A1	KN11
CLK CRC L	D5-C7	D7-B7	PC 1 (1) H	D6-A1	KN11
CRTP OVFLW H	D3-C5	D6-D4, D8-C6, D8-B4	PC 2 (1) H	D6-A1	KN11
CLK SEC BUS L	D5-C7	D4-B2	PC 3 (1) H	D6-A1	KN11
CLK SP ADDR REG L	D4-B3	D3-A4	PC 4 (1) H	D6-A1	KN11
CLK SR L	D5-B7	D3-B4	PC 5 (1) H	D6-A1	KN11
CUNTR L	KN11	D7-C7	PC 6 (1) H	D6-A1	KN11
CMC10 (1) H	D7-H1	DN-C6	PC 7 (1) H	D6-A1	KN11
CMC10 (1) L	D7-A1	D7-B7	PC LOAD KN L	D6-D1	D6-A8
C1 (1) AN	D3-A6	D4-B3, D5-B4, D8-D4, D8-C4	ROM OUT 0	D6-D1	D3-C8
C1 (1) L	D3-A6	D3-C5, D3-B7, D7-B8	ROM OUT 1	D6-D1	D3-C8
C0 (1) H	D3-A6	D5-D6, D7-B8, D8-D4, D8-B4	ROM OUT 2	D6-D1	D3-C8
C0 (1) L	D3-A6	D3-C7, D3-A2, D4-B1, D5-B4, D7-B8	ROM OUT 3	D6-D1	D3-C8
		D3-B2, D4-B3, D7-B8, D8-B3	ROM OUT 4	D6-D1	D3-C8
DATA I L	D8-D5	D4-A2	ROM OUT 5	D6-D1	D3-C8
DISABLE ROMS L	TEST PAD	D6-D8	ROM OUT 6	D6-D1	D3-C8
DO INET L	D8-B4	D5-B8	ROM OUT 7	D6-D1	D3-C8
DRV BUSS H	D5-D4	D4-A4	RX DATA (1) L	D5-C1, INTERFACE	INTERFACE, D8-D8
DRV ERASE H	D5-B1	DRIVE	RX DONE L	D5-D1	INTERFACE
DRV OUT H	D5-C1	DRIVE	RX ERROR L	D5-D1	INTERFACE
DRV LOAD HEAD H	D5-A1	DRIVE	RX INIT L	INTERFACE	D8-B8
DRV STEP L	D5-C1	DRIVE	RX OUT L	D5-D1	INTERFACE
DRV INIT + PC	D8-B6	DRIVE	RX RUM L	INTERFACE	D8-D8
DRV ABOVE TK 43 H	D5-B1	DRIVE	RX SHIFT L	D5-C1	INTERFACE
DRV RAW DATA L	DRIVE	D4-A8	RX TRANSFER REQUEST	D5-D1	INTERFACE
DRV SEL CLK 1 H	DRIVE	D5-B1	RX 12 HIT L	INTERFACE	D8-D8
DRV SEL INDX H	DRIVE	D5-A1			
DRV SKL TRK 0 H	DRIVE	D5-B1	SKC BUF OVFLW H	D4-A1	D8-C6
DRV WT DATA	DRIVE	D5-B1	SKC NUF OUT (1) H	D4-C1	D5-C4, D8-B6
DRV V/T GATE H	DRIVE	D5-C1	SKC NUF H	D5-B8	D5-C4
DRV CEL WT PROT L	DRIVE	D8-C8	SFL 0 (1) H	D3-A6	D5-C8, D6-C8, D8-B6, KN11
			SEL 1 (1) H	D3-A6	D5-C8, D6-C8, D8-B6, KN11
			SEL 2 (1) H	D3-B6	D5-C8, D6-C8, D8-B6, KN11
			SEL J (1) H	D3-B6	D5-C8, D6-C8, D8-B6, KN11
			SEP CLK (1) H	D4-B4	D8-C6
			SEP DATA (1) H	D4-B5	D3-A2
			SN H	D4-B5	D4-A2, D7-A8, D8-C8
			SR LOAD H	D5-B4	D5-C4
			SR NDB (1) H	D3-B3	D3-C4
			SYN INDEX (1) H	D3-D3	D5-C4, D6-C8, D8-C6
				D5-A5	D8-C6
FLAG (1) H	D5-B3	D8-B6	TP3 H	D7-D3	D7-C6, D8-B4, D8-C5
FLD 0 L	D6-D6	D6-A3, D6-A2	TP3 L	D7-D3	D5-B8
FLD 1 L	D6-D6	D6-B1, D6-B2	TP4 H	D7-D2	D8-C3
FLD 2 L	D6-D6	D6-C3, D6-C2	TP4 L	D7-D3	D8-B2
FLD 3 L	D6-D6	D6-A6, D6-A4			
FLD 4 L	D6-D6	D6-B6, D6-B4	WRK CLK CNTR L	D8-C2	D3-B7
FLD 5 L	D6-D6	D6-C6, D6-C4	20 MHZ CLK	D7-C5	D4-C8, D4-D7
HALT H	D7-C3	KN11			
HALT L	KN11	D7-C7			
HIGH 1	D7-C4	D3-D6, D3-D4, D3-C6, D3-C4, D4-A3	GND	POWER SUPPLY	D1-A4
		D4-B1, D5-D5, D6-A8	+5V	POWER SUPPLY	D1-A4, D8-A7
HIGH 2	D7-B4	D4-A5, D5-B7, D5-A7, D5-B4, D7-D5	+7V	POWER SUPPLY	KN11
		D7-D4, D7-C4, D7-C5, D8-D5, D8-B3	+10V	POWER SUPPLY	D8-B8
HIGH 3	D7-B4	DR-A5			
HOME H	D5-H2	D4-D8, D4-C8, D4-D7, D4-D5, D8-C6			
INIT + PC A L	D8-A4	D3-C5, D3-B4, D3-A4, D3-A7, D4-B6			
INIT + PC H	D8-A4	D4-B5, D4-B8, D7-C5, D8-B2			
INIT + PC L	D8-A4	D4-D5, D4-C5, D7-D4			
INST 0 (1) H	D3-B6	D4-B3, D5-A5, D6-A8			
INST 0 (1) L	D3-B6	KN11, D8-B5			
INST 1 (1) H	D3-B6	DR-C5			
INST 1 (1) L	D3-B6	KN11			
INST DIS H	D8-B1	D8-B5			
INST DIS L	DR-H1	DR-C5			
INTERF BUSS H	D5-D4	DR-H5			
JUMP L	DR-C3	D7-B8			
I.D. RM + CLK PC L	DR-C1	DR-AH, D1-AH			
I.D. SCATCH PAD L	DR-H6	D1-D1			
MAINT DIS L	TEST PAD	D8-B1			
MIS CLK (1) L	D4-C4	D8-C8			
MUX OUT 0	D3-C7	D8-A8			
MUX OUT 1	D3-C7	D6-A8			
MUX OUT 2	D3-C7	D6-A8			
MUX OUT 3	D3-C7	D6-B8			
MUX OUT 4	D3-C7	D6-B8			
MUX OUT 5	D3-D7	D6-B8			
MUX OUT 6	D3-D7	D6-B8			
MUX OUT 7	D3-D7	D6-B8			

REVISIONS		
CHK	CHANGE NO.	REV.

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FIRST USED ON OPTION MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
RXØ1				

DRN <i>W. Henin</i>	DATE 18 FEB 76
CHK'D <i>W. Henin</i>	DATE 19 FEB 76
ENG <i>P. K. ...</i>	DATE 2/19/76
PROJ. ENG. <i>Charles ...</i>	DATE 2/23/76
PROD. <i>Jack Miller</i>	DATE 2/23/76

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE
FLOPPY CONTROLLER
FIRMWARE

SCALE	SIZE CODE K SP	NUMBER RXØ1-Ø-2	REV.
SHEET 1 OF 1	DIST.		

REVISIONS	REV.
CHANGE NO.	
CHK	

/RX01 FLOPPY CONTROLLER FIRMWARE

/THIS SYMBOL TABLE REPLACES THE NORMAL PAL SYMBOL TABLE AND DEFINES
/THE INSTRUCTIONS POSSIBLE BY THE RX01 CONTROLLER

/DO INSTRUCTIONS

0002	SET=2	
0000	CLR=0	
0072	ONE=2	
0000	ZERO=0	
0000	I0B0=0	/INTERFACE=DISK BUSS OUTPUT BUFFER
0004	I0B1=4	
0010	I0B2=10	
0014	I0B3=14	
0020	I0B4=20	
0024	I0B5=24	
0030	I0B6=30	
0000	INTERF=CLR I0B0	/I0B0 SELECTS EITHER INTERFACE OR DISK BUSS. CLR= INTERFACE
0002	DISK=SET I0B0	/SET=DISK
0004	ERR=I0B1	/INTERFACE BUFFER DEFINITIONS
0010	XREQ=I0B2	/SET TO INDICATE THAT AN RX01 ERROR HAS OCCURED
0014	I0OUT=I0B3	/SET TO REQUEST AN RX01 WORD TRANSFER
0020	DONE=I0B4	/DIRECTION FOR DATA LINE. SET=TO INTERFACE
0024	SHIFT=I0B5	/SET TO INDICATE RX01 READYNSS TO ACCEPT A COMMAND
0030	SECDAT=I0B6	/SHIFT FOR DATA LINE
		/SELECTS SOURCE FOR DATA OUT OF CONTROLLER ON DATA LINE
		/SET=SECTOR BUFFER CLR=SHIFT REGISTER MOST SIG BIT
0004	WGATE=I0B1	/DISK BUFFER DEFINITIONS
0010	STPHDS=I0B2	/WRITE CURRET ENABLE WHEN SET
0014	HDOUT=I0B3	/HEAD STEP. TWO PULSES REQUIRED FOR EACH TRACK
0020	EGATE=I0B4	/DIRECTION OF HEAD MOTION
0024	LOWCUR=I0B5	/ERASE CURRENT ENABLE
		/SPECIFIES WRITE CURRENT LEVEL
0034	UNITS=34	/SELECTS ONE OF TWO DRIVES. UNIT (ZERO)(ONE)
0040	UNHD=40	/DEACTIVATES HEAD LOAD SOLOINOID OF SELECTED DRIVE
0042	LHD=42	/ACTIVATES HEAD LOAD SOLOINOID OF SELECTED DRIVE
0044	BAR=44	/SECTOR BUFFER ADDRESS REGISTER CONTROL
0001	LONG=1	/FORMAT: CLR BAR (SHORT)(LONG)
0000	SHORT=0	/SHORT PRESETS FOR COUNT OF 1024
0002	INCR=2	/LONG PRESETS FOR COUNT OF 4096
		/FORMAT: INCR BAR INCREMENT THE BUFFER ADDRESS REG.

0050	WRBUF=50	/SECTOR BUFFER WRITE CLOCK
0003	START=3	/FORMAT: (STPAT)(PIN) WRBUF
0000	FINE=0	/A 750NS MINIMUM PULSE IS REQUIRED
0054	CRC=54	/CRC REGISTER CONTROL
0057	PRECRC=57	/FORMAT: CRC (ONE)(ZERO) SPECIFIES DATA TO
0055	DATCRC=55	/BE JAMMED INTO CRC GENERATOR/CHECKER
		/PRESETS CRC REG TO ALL ONES
		/SHIFTS SEPERATED DATA INTO CRC CIRCUIT
0000	FLAG=00	/GENERAL PURPOSE FLAG CONTROL
0002	ON=2	/FORMAT: FLAG (ON)(OFF)(TOG)
0001	OFF=1	/SET FLAG
0003	TOG=3	/CLR FLAG
		/TOGGLE FLAG
0064	LSP=64	/LOAD OPEN SCRATCHPAD REG WITH CONTENTS OF SHIFT REG
0070	LCT=70	/LOAD COUNTER WITH CONTENTS OF NEXT ROM LOCATION
0071	ESP=71	/LOAD COUNTER WITH CONTENTS OF OPEN SCRATCHPAD
0073	ICT=73	/INCREMENT COUNTER
0074	ROTATE=74	/SHIFT REGISTER CONTROL
		/FORMAT: ROTATE(ONE)(ZERO)
		/SHIFTS SHIFT REG TOWARDS MOST SIGNIFICANT BIT
		/WHILE INSERTING A ONE OR ZERO INTO THE LEAST
		/SIGNIFICANT BIT
0075	LSR=75	/LOAD SHIFT REGISTER WITH CONTENTS OF COUNTER
0077	DATSR=77	/SHIFT REG TOWARDS MSB WHILE INSERTING SEPERATED
		/DATA INTO LSR


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/BRANCH INSTRUCTIONS AND CONDITIONS

0100 BR=100
    /FORMAT: BR COND (T)(F)(ONE)(ZERO)
    /IF CONDITION IS MET, A BRANCH IS MADE WITHIN
    /THE CURRENT FIELD USING THE CONTENTS OF THE
    /NEXT ROM LOCATION AS THE BRANCH ADDRESS
    /IF THE CONDITION IS NOT MET, THE NEXT ROM LOCATION
    /IS IGNORED AND THE FOLLOWING INSTRUCTION IS EXECUTED
    /FORMAT: MBR COND (T)(ONE)
    /THE COUNTER IS INCREMENTED WITH EVERY EXECUTION OF
    /THIS INSTRUCTION, THE MBR IS REPEATEDLY
    /EXECUTED UNTILL EITHER THE COUNTER OVERFLOWS OR
    /THE CONDITION IS MET. IF THE CONDITION IS MET
    /THE BRANCH IS MADE. IF THE COUNTER OVERFLOWS
    /IS EXECUTED
    /REQUIRES THE CONDITION TO BE FALSE
    /IF APPENDED TO THE JUMP, BR OR MBR INSTRUCTION,
    /CAUSES THE BRANCH ADDRESS TO BE TAKEN FROM THE
    /OPEN SCRATCHPAD RATHER THAN FROM THE NEXT ROM LOCATION

0300 WBR=300
    /WHEN ASSERTED INDICATES THAT THE INTERFACE HAS
    /SERVICED A TRANSFER REQUEST, OR THAT A COMMAND
    /IS PENDING
    /INTER/DISK OUTPUT BUFFER BIT 3
    /BIDIRECTIONAL DATA LINE BETWEEN INTERFACE AND CONTROLLER
    /DRIVE INDEX LATCH
    /SHIFT REGISTER MOST SIGNIFICANT BIT
    /OVERFLOW (ALL ONES) OF THE COUNTER
    /BIT 16 OF CRC GENERATOR/CHECKER
    /TRACK ZERO OF SELECTED DRIVE ANDED WITH HEAD
    /DIRECTION BEING OUT
    /WRITE ENABLED STATUS OF THE SELECTED DRIVE
    /SEPERATED CLOCK FROM DISK DATA
    /ASSERTED IF INTERFACE TRANSFERS ARE TO BE AS
    /12 BIT WORDS RATHER THAN 8 BIT BYTES
    /SEPERATED DATA EQUAL TO SHIFT REG BIT 7
    /OVERFLOW CONDITION (ALL ONES) OF THE SECTOR BUFFER
    /ADDRESS REGISTER
    /MISSING CLOCK EQUAL TO SHIFT REG BIT 7
    /OUTPUT OF SECTOR BUFFER
    /STATE OF GENERAL PURPOSE FLAG

0000 F=ZERO
0002 T=ONE
0001 IND=1

0000 PUN=0

0004 IOB30T=4
0010 DATAIN=10
0014 INDX=14
0020 SR7=20
0024 COFL=24
0030 CRC16=30
0034 HOME=34
0040 WRTEN=40
0244 SECLK=44
0250 XI161T=50
0054 DECSR7=54
0060 BAROFL=60
0064 MCEGSR=64
0070 BDATAO=70
0074 FLAGO=74

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/SCRATCHPAD REGISTER SELECTION

0200 OPEL=200
    /FORMAT: OPEN X WHERE X IS ONE OF THE SCRATCHPAD REG
    /THIS INSTRUCTION MAKES THE NAMED SCRATCHPAD
    /ACCESSIBLE VIA THE LSP AND ESP COMMANDS
    /DEFINITIONS OF SCRATCHPADS BY R#

0000 R0=2
0004 R1=4
0010 R2=10
0014 R3=14
0020 R4=20
0024 R5=24
0030 R6=30
0034 R7=34
0040 R8=40
0044 R9=44
0050 R10=50
0054 R11=54
0060 R12=60
0064 R13=64
0070 R14=70
0074 R15=74

0000 CURTK=0
0004 CURTK=4
0008 CURTK=8
0010 STAT=3
0014 STAT=7
0020 TARG=0
0024 TARG=4
0030 TEMP=0
0034 TEMP=4
0040 TEMP=8
0044 TEMP=12
0050 TEMP=16
0054 TEMP=20
0060 TEMP=24
0064 TEMP=28
0070 TEMP=32
0074 TEMP=36

0000 CURTK=0
0004 CURTK=4
0008 CURTK=8
0010 STAT=3
0014 STAT=7
0020 TARG=0
0024 TARG=4
0030 TEMP=0
0034 TEMP=4
0040 TEMP=8
0044 TEMP=12
0050 TEMP=16
0054 TEMP=20
0060 TEMP=24
0064 TEMP=28
0070 TEMP=32
0074 TEMP=36

/DEFINITION OF SCRATCHPADS BY PNEUMONICS
/CURRENT TRACK ADDRESS OF DRIVE 0
/CURRENT TRACK ADDRESS OF DRIVE 1
/DEFINITIVE ERROR CODE IF ANY
/STATUS WORD OF RX01
/TARGET TRACK OF CURRENT DISK ACCESS
/TEMPORARY STORAGE
/TEMPORARY STORAGE
/TEMPORARY STORAGE
/BIT 7 IS UNIT SELECT BIT, 0 MEANS UNIT 1
/BIT 7 IS HEAD LOADED BIT, 1 MEANS HEAD LOADED
/TEMPORARY STORAGE
/RETURN ADDRESS FOR 3RD LEVEL NESTED SUBROUTINES
/RETURN ADDRESS FOR 2ND LEVEL NESTED SUBROUTINES
/RETURN ADDRESS FOR 1ST LEVEL SUBROUTINES

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175 /JUMP INSTRUCTION AND JUMP FIELD DEFINITIONS
176 JUMP#202
177
178 /ORHAT: JUMP FX (IND)
179 /CAUSES A BRANCH TO ONE OF SIX ROM FIELDS (8-5)
180 /SPECIFIED BY X, THE BRANCH ADDRESS IS TAKEN FROM
181 /THE ROM LOCATION FOLLOWING THE JUMP INSTRUCTION.
182 /IF IND IS APPENDED, THE BRANCH ADDRESS
183 /IS TAKEN FROM THE OPEN SCRATCH PAD
184
185 0000 F0#0
186 0004 F1#4
187 0010 F2#10
188 0014 F3#14
189 0020 F4#20
190 0024 F5#24

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200 /TABLE OF DEFINITIVE ERROR CODES
201 KXDRV#10 /DRIVE 0 FAILED TO SEE HOME ON INITIALIZE
202 KXDRV#20 /DRIVE 1 FAILED TO SEE HOME ON INITIALIZE. DOES NOT CAUSE ERROR
203 K#RONG#30 /FOUND HOME WHEN STEPPING IN 18 TRACKS FOR INIT
204 K#TRK#40 /TRIED TO ACCESS A TRACK GREATER THAN 76
205 K#OMER#50 /HOME WAS FOUND BEFORE DESIRED TRACK WAS REACHED
206 KSELF#60 /SELF DIAGNOSTIC ERR
207 KXHDR#70 /AT 52 HEADERS
208 K#PROT#80 /WRITE FUNCTION ATTEMPTED ON A WRITE PROTECTED DISK
209 KTIMER#110 /MORE THAN 40 MICROSECONDS AND NO SEPCLOCK SEEN
210 KXPRAM#120 /A PREAMBLE COULD NOT BE FOUND
211 KXIDAM#130 /PREAMBLE FOUND BUT NO ID MARK FOUND WITHIN ALLOWABLE TIME
212 K#CRC#140 /CRC ERROR ON WHAT APPEARED TO BE A HEADER. ERROR IS NOT ASSERTED
213 KTSKER#150 /THE TRACK ADDRESS OF A GOOD HEADER DOES NOT COMPARE
214 /WITH THE DESIRED TRACK
215 KXSTRYS#160 /TOO MANY TRIES FOR AN IDAM
216 KNDAMS#170 /DATA AM NOT FOUND IN ALLOTTED TIME
217 K#CRC#200 /CRC ERROR ON READING THE SECTOR FROM THE DISK
218 KPARER#210 /PARITY ERROR ON SOME WORD FROM THE INTERFACE
219

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/ROUTINE: INITIALIZE) IF A HOST PROCESSOR INITIALIZE OR AN
 /RX01 POWER LOW IS DETECTED, THE PC IS CLEARED AND THE RX01 TIMING
 /STOPS. UPON THE NEGATION OF INITIALIZE, TIMING RESUMES AND A SELF TEST OF
 /INTERNAL DATA PATHS IS MADE. IF AN ERROR OCCURS HERE, ERROR AND
 /DONE ARE SET, BUT ERREG IS NOT ALTERED. THEN IF NO ERROR HAS OCCURRED AN ATTEMPT
 /IS MADE TO RECALASRATE DRIVE 1 THEN DRIVE 0. IF DRIVE 0 FAILS TO RECALIBRATE,
 /THE ERROR CODE IS LOADED INTO ERREG AND ERROR IS SET. IF DRIVE
 /0 RECALIBRATES AND IS READY (DISK LOADED) SECTOR ONE OF TRACK ONE
 /IS READ INTO THE SECTOR BUFFER. IT IS POSSIBLE FOR A READ ERROR
 /TO OCCUR WHILE READING THIS SECTOR.

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220 0000 *0000
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235 0000 0210
236 0001 0064
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238 0002 0322
239 0003 2352
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241 0004 0070
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243 0005 0004
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245 0006 0075
246 0007 0214
247 0010 0064
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249 0011 0070
250 0012 2377
251 0013 0075
252 0014 0204
253 0015 0064
254 0016 0000
255 0017 0064
256 0020 0204
257 0021 0064
258
259 0022 0074
260 0023 0224
261 0024 0064
262 0025 2020
263 0026 0064
264
265 0027 0002
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267 0030 0070
268 0031 0034
269 0032 2222
270 0033 2145
271
272 0034 2936
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274 0035 0014
    
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DECIMAL
 OPEN ERREG /CLEAR ERROR REGISTER
 LSP
 JUMP F4 /GO DO THE INITIALIZE DIAGNOSTIC ROUTINE
 TEST
 TSTRTN, LCT /RETURN FROM SUCCESSFUL DIAGNOSTIC ROUTINE
 OCTAL
 0
 DECIMAL
 LSR /SET THE INIT DONE BIT OF STAT
 OPEN STAT
 LSP
 LCT /SET UP SOME SCRATCHPAD REGISTERS
 -1
 LSR
 OPEN TEMPD /UNIT 0 TO SOFT UNIT BIT
 LSP
 OPEN CURTK0 /NEG ZERO TO BOTH CURRENT TRACK ADDRESSES
 LSP
 OPEN CURTK1
 LSP
 ROTATE ZERO /NEG ONE TO TARGET SECTOR
 OPEN TARSEC
 LSP
 OPEN TARTRK /NEG ONE TO TARGET TRACK FOR INITIALIZE BOOTSTRAP
 LSP
 DISK /SELECT DISK RUNS
 LCT
 RECALL /RECALL UNIT ONE
 UNIT ONE
 RECAL0, CLR HDOUT /STEP HEAD IN 1" TRACKS TO ASSURE IT IS NOT BEHIND TRACK 0

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275 0036 0070
276 0037 0305
277 0040 0075
278 0041 0070
279 0042 0045
280 0043 0222
281 0044 2100
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283 0045 0226
284 0046 2621
285
286 0047 0010
287 0050 0070
288 0051 0257
289 0052 0075
290 0053 0070
291 0054 0060
292 0055 0040
293 0056 0222
294 0057 2100
295
296 0060 0202
297 0061 0075
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299 0062 0174
300 0063 0070
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302 0064 0070
303 0065 0010
304 0066 0226
305 0067 2610
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307 0070 0070
308 0071 0020
309 0072 0075
310 0073 0210
311 0074 0064
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313 0075 0176
314 0076 0372
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316 0077 0062
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318 0100 0034
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320 0101 0202
321 0102 0035
    
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LCT
 -10-1
 LSR
 LCT
 IN10
 JUMP F4
 STEPH0
 IN10, JUMP F5 /ERROR. HOME HAS BEEN SEEN WHILE STEPPING IN.
 WRONG
 SET HDOUT /STEP OUT AS MANY AS 60 TRACKS IN SEARCH OF HOME
 LCT
 -00-1
 LSP
 LCT
 RCALOK
 UNHD
 JUMP F4
 STEPH0
 RCALOK, JUMP F0 /HOME WAS FOUND OK
 WHCHDR
 BR FLAG0 F /IF FLAG=0 RECALIBRATE WAS ON DRIVE 1
 NXDRV1
 LCT
 KNXDV0
 JUMP F5
 GOERDN
 NXDRV1, LCT /RECAL FAILURE WAS ON DRV 1, LOG ERROR
 KNXDV1 /AND CONTINUE RECALIBRATION
 LSR
 OPEN ERREG
 LSP
 WHCHDR, BR FLAG0 T /IF FLAG=1 BOTH DRIVES HAVE BEEN RECALIBRATED
 PUNRCL
 FLAG ON /SET FLAG TO INDICATE DRV 0 IS BEING RECALIBRATED
 UNIT ZERO
 JUMP F0
 RECAL0 /GO BACK AND RECALIBRATE DRV0

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322 /SUBROUTINE: FINDTRACK]
323 /THIS SUBROUTINE IS USED TO LOCATE A SPECIFIED SECTOR. IT PICKS
324 /UP THE TRACK AND SECTOR ADDRESS FROM THE INTERFACE, CHECKS THAT
325 /THE TRACK ADDRESS IS LEGAL (NOT GREATER THAN 114 OCTAL.), MOVES THE
326 /HEAD OF THE SELECTED DRIVE TO THE SPECIFIED TRACK, VERIFIES
327 /TRACK POSITION, AND LOCATES THE CORRECT SECTOR. EXIT FROM
328 /THIS SUBROUTINE OCCURS AT WRITE TURN ON TIME OF THE SELECTED
329 /SECTOR. ENTRANCE IS MADE WITH THE RETURN ADDRESS IN THE COUNTER
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0103	0075	FINDTR, LSR	/SAVE THE RETURN ADDRESS
0104	0274	OPEN RTN	
0105	0064	LSP	
0106	0270	LCT	/CLEAR THE ERROR REGISTER
0107	0060	0	
0110	0075	LSR	
0111	0210	OPEN_ERREG	
0112	0064	LSP	
0113	0244	OPEN_TEMP0	/SOFT UNIT BIT TO SR
0114	0071	ESP	
0115	0075	LSR	
0116	0122	SR SR7 ONE	/IF SR=1 DRIVE 0 IS CURRENTLY SELECTED
0117	0127	UZERO	
0120	0174	UONE,	
0121	0141	USAME	/IF FLAG0 DRIVE 1 IS DESIRED AND ALREADY SELECTED
0122	0234	UNIT ZERO	/DRIVE 0 IS DESIRED AND DRIVE1 WAS SELECTED, SELECT 0
0123	0070	LCT	/SET UP SOFT UNIT SELECT AS DRIVE 0
		OCTAL	
		200	
		DECIMAL	
0124	0200	JUMP F0	/GO STORE SOFT UNIT BIT
		UDIF	
0125	0202	JUMP F0	
0126	0134	UDIF	
0127	0176	UZERO,	
0130	0141	USAME	/IF FLAG=1 DRIVE 0 IS DESIRED AND ALREADY SELECTED
0131	0036	UNIT ONE	/DRIVE 1 IS DESIRED BUT DRIVE0 IS SELECTED, SELECT DRIVE 1
0132	0072	LCT	/SET UP SOFT UNIT SELECT BIT AS DRIVE 1
0133	0000	0	
0134	0075	UDIF,	
0135	0064	LSP	/STORE SOFT UNIT SELECT BIT
0136	0074	ROTATE ZERO	/CLR SOFT HD LOAD BIT BECAUSE UNITS CHANGED

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0137	0250	OPEN TEMPE	
0140	0064	LSP	
0141	0070	USAME,	
0142	0145	LCT	/CALL GETWORD SUBROUTINE FOR THE SECTOR ADDRESS
0143	0222	PUTSEC	
0144	2000	JUMP F4	
		GETWRD	
0145	0070	PUTSEC,	
0146	2374	-7=1	/MAKE FIRST BIT OF COMPLIMENTED SECTOR ADDRESS A 1 REGARDLESS OF DATA
0147	0076	ROTATE ONE	
0150	0126	BR COFL T	
0151	0160	07	
0152	0073	ICT	
0153	0122	BR SR7 T	
0154	0147	05	
0155	0074	ROTATE ZERO	
0156	0202	JUMP F0	
0157	0150	07	
0162	0224	OPEN TARSEC	/PUT THE TARGET SECTOR AWAY
0161	0064	LSP	
0162	0070	LCT	
0163	0166	PUTTRK	/CALL GETWRD SUBROUTINE FOR TRACK ADDRESS
0164	0222	JUMP F4	
0165	2000	GETWRD	
0166	0220	PUTTRK,	
0167	0064	LSP	/STASH THE TRACK ADDRESS
0172	0254	OPEN TEMP0	/START SETUP FOR COMPARING THE
0171	0064	LSP	/TARGET TRACK AND TRACK 76
0172	0260	OPEN TEMP0	/FB TARGET TRACK
0173	0070	LCT	/G= 77
0174	0202	077=1	
0175	0075	LSR	
0176	0064	LSP	
0177	0070	LCT	/CALL SUBR MAGCOM TO SEE IF TARGET TRACK
0200	0206	ILTRK	/IS GREATER THAN 114 OCTAL, 76 DECIMAL.
0201	0075	LSR	
0202	0270	OPEN RTNA	
0203	0064	LSP	
0204	0226	JUMP F5	
0205	2400	MAGCOM	
0206	0202	JUMP F0	/TARGET TRACK IS 77, ILLEGAL ADDRESS
0207	0242	ERTRK	/GO, REPORT THE ERROR
0210	0202	JUMP F0	/TARGET TRACK IS GREATER THAN 77
0211	0242	ERTRK	/GO, REPORT THE ERROR

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432 0212 0294 OPEN TEMPD
433 0213 0071 ESP
434 0214 0075 LSR
435
436 0215 0200 OPEN CURTK0
437
438 0216 0002 DISK
439
440 0217 0122 BR SR7 ONE
441 0220 0222 *+2
442 0221 0204 OPEN CURTK1
443
444 0222 0071 ESP
445 0223 0075 LSR
446 0224 0200 OPEN TEMPG
447 0225 0064 LSP
448
449 0226 0220 OPEN TARTRK
450 0227 0071 ESP
451 0230 0075 LSR
452 0231 0254 OPEN TEMPF
453 0232 0064 LSP
454 0233 0070 LCT
455 0234 0246 TRKEG
456 0235 0075 LSR
457 0236 0270 OPEN RTNA
458 0237 0064 LSP
459 0240 0226 JUMP FS
460 0241 2400 MAGCOM
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481
482
483
484
485
486
0242 0070 LCT
0243 0040 KERTRK
0244 0226 JUMP FS
0245 2010 GOERDN

0246 0202 TRKEG, JUMP F0
0247 0357 NOSTPS
0250 0270 OPEN RTNA
0251 0270 OPEN RTNA
0252 0270 BOOT, OPEN RTNA
0253 0070 LCT
0254 0275 *77 STPOUT
0255 0075 LSR
0256 0064 LSP
0257 0244 OPEN TEMPD
0260 0071 ESP
0261 0075 LSR
0262 0204 OPEN CURTK1
0263 0120 BR SR7 ZERO

```

/TRIED TO ACCESS A TRACK GREATER THAN 76 DECIMAL

/TARGET EQUALS THE CURRENT TRACK, NO
/STEPS ARE REQUIRED
/NOOP; TARGET > ACTUAL RETURN
/NOOP

/TARGET IS LESS THAN ACTUAL, STEPS NEEDED ALSO START OF
/OF BOOT SUBROUTINE. SET UP RETURN FROM DIF SUBR

/SOFT UNIT SELECT BIT TO SR7

/PRESELECT UNIT 1

/SR7#0 MEANS UNIT ONE

```

487 0264 0266 *+2
488 0265 0200 OPEN CURTK0
489
490 0266 0071 LCT
491 0267 0075 LSR
492
493 0270 0220 OPEN TARTRK
494 0271 0071 ESP
495
496 0272 0016 SET MDOUT
497
498 0273 0220 JUMP F5
499 0274 2462 DIF
500
501
502
503
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539
540
541
0275 0202 STPOUT, JUMP F0
0276 0300 *+2
0277 0014 CLR MDOUT
0300 0070 LCT
0301 0305 DUNSTP
0302 0040 UNMD
0303 0222 JUMP F4
0304 2100 STEPHD

0305 0226 DUNSTP, JUMP F5
0306 2456 HOMERR
0307 0244 OPEN TEMPD
0310 0071 ESP
0311 0075 LSR
0312 0220 OPEN TARTRK
0313 0071 ESP
0314 0200 OPEN CURTK0
0315 0122 BR SR7 ONE
0316 0320 *+2
0317 0204 OPEN CURTK1
0320 0075 LSR
0321 0064 LSP

0322 0220 HDSETL, OPEN TARTRK
0323 0071 ESP
0324 0075 LSR
0325 0254 OPEN TEMPF
0326 0064 LSP
0327 0070 LCT
0328 0323 -44-1

```

/PASS SELECTED CURRENT TRACK TO DIF SUBR VIA SR

/PASS TARGET TRACK TO DIF VIA CNTR

/ASSUME A STEP OUT

/GO TO THE SUBROUTINE DIF TO CALCULATE THE STEPS NEEDED

/TARGET TRACK IS LESS THAN
/THE ACTUAL, *MOVE OUT IS NECESSARY

/TARGET IS GREATER THAN ACTUAL. STEPS IN NEEDED

/COMPLEMENT OF STEPS REQUIRED IS IN THE
/SHIFT REG. SET UP RETURN FROM STPHD SUBR

/UNLOAD HEAD BEFORE MOVING

/CALL SUBROUTINE STEPHD

/HOME FOUND BEFORE LAST STEP TAKEN

/SOFT UNIT BIT TO SR7

/GET READY TO PASS TARGET TRK TO PROPER
/CURRENT TRACK

/OPEN PROPER CURRENT TRACK REGISTER
/BIT7#0 MEANS UNIT ONE

/UPDATE THE CURRENT TRACK ADDRESS

/HEAD IS SETTLED DETERMINE IF ABOVE TRACK 43 DECIMAL
/PASS TARGET TO MAGCOM VIA TEMPF

/PASS 44 TO MAGCOM VIA TEMPG

```

542 0331 0075 LSR
543 0332 0260 OPEN TEMPG
544 0333 0004 LSP
545
546 0334 0026 /ASSUME TARGET GREATER THAN 43
547
548 0335 0070 /CALL MAGCOM SUBROUTINE
549 0336 0344 /RETURN ADDRESS
550 0337 0075 LSR
551 0340 0270 OPEN RTNA
552 0341 0064 LSP
553 0342 0226 JUMP F5
554 0343 2400 MAGCOM
555
556 0344 0202 ABV43, JUMP F0 /NOOP F06 RETURN, ABOVE TRK 43
557 0345 0346 .+1 /NOOP
558
559 0346 0202 JUMP F0 /F061 ABOVE TRACK 43
560 0347 0351 .+2
561
562 0350 0024 CLR LONCUR /F061 BELOW TRACK 43. WRITE WITH HIGH CURRENT
563
564 0351 0070 CFINSE, LCT /CALL FINDSEC SUBROUTINE TO LOCATE THE DESIRED SECTOR
565 0352 0355 RFINTH
566 0353 0200 JUMP F1
567 0354 0714 FINDSE
568
569 0355 0274 RFINTR, OPEN RTN /RETURN FROM FINDTR SUBROUTINE
570 0356 0207 JUMP F1 IND
571
572
573
574 0357 0250 NOSTPS, OPEN TEMPE /NO STEPS REQUIRED
575 0360 0071 ESP /SOFT HEAD LOAD BIT TO SR7
576 0361 0075 LSR
577
578 0362 0122 BR SR7 ONE /IS HEAD LOADED?
579 0363 0322 H0SETL /YES, GO UPDATE CURRENT CONTROL
580
581 0364 0070 LCT /NO, GO LOAD HEAD AND WAIT FOR 20MS SETTLE TIME
582 0365 0322 H0SETL /RETURN ADDR FROM DLY25 SUBROUTINE
583 0366 0222 JUMP F4
584 0367 2145 DLY25
585
586
587 0370 0212 PFUNCT, JUMP F2 /POINTER FROM GETWORD SUBROUTINE TO
588 0371 1036 FUNCT /FUNCTION DECODE
589
590 0372 0224 PDHREL, JUMP F5 /POINTER TO DRV# CHECK DONE AFTER RECALBRATE
591 0373 2025 DNRCAL
592
593 0374 0000 0 /SPARE LOCATIONS
594 0375 0000 0 /OPEN
595 0376 0000 0 /OPEN
596 0377 0000 0 /OPEN

```

```

597 /ROUTINE: WRITE SECTOR)
598 /THIS ROUTINE TURNS ON WRITE GATE AT WRITE TURN ON TIME,
599 /WRITES A PREAMBLE OF 6 BYTES OF ZEROS, A DATA OR DELETED DATA MARK,
600 /THEN TURNS ON ERASE GATE. ENTER WITH CNTR=100 IF
601 /DELETED DATA, CNTR=0 IF NORMAL DATA MARK. THE DATA MARK, DATA FIELD, CRC
602 /AND ONE BYTE POSTAMBLE ARE WRITTEN. WRITE CURRENT IS TURNED OFF.
603 /511 MICRO SECONDS LATER ERASE CURRENT IS TURNED OFF. A HEADER MUST
604 /THEN BE READ TO INSURE DISK IS STILL UP TO SPEED BEFORE THE WRITE
605 /SECTOR FUNCTION IS COMPLETE.
606
607
608
609
610 0400 0214 *RTSEC, OPEN STAT /DEL DATA BIT TO STAT6
611 0401 0075 LSR
612 0402 0264 LSP
613
614 0403 0070 LCT /CALL SUBROUTINE TO FIND DESIRED TRACK AND SECTOR
615 0404 0400 S*GATE
616 0405 0202 JUMP F0
617 0406 0103 F*J*TP
618
619 0407 0061 S*GATE, FLAG OFF /ALWAYS START WRITING WITH WRITE FLOP CLEARED
620
621 0410 0140 BR *RTEN F /GO REPORT ERROR IF NO WRITE ENABLE
622 0411 0503 PRTEMP
623
624 0412 0214 OPEN STAT /DEL DATA BIT TO SR7 AND ENABLE WRT CURRENT
625 0413 0071 ESP
626 0414 0400 SET *GATE
627 0415 0075 LSR
628 0416 0074 POTATE ZERO
629
630 0417 0234 OPEN TEMPB /USE TEMPB FOR SECOND HALF DATA AM PATTERN
631
632 0420 0057 PRECRC /JAM THE CRC GENERATOR WITH FIRST 6 BITS OF DATA AM
633 0421 0056 CRC ONE
634 0422 0056 CRC ONE
635 0423 0056 CRC ONE
636 0424 0056 CRC ONE
637 0425 0056 CRC ONE
638 0426 0054 CRC ZERO
639
640 0427 0120 BR SR7 ZERO /DELETED DATA
641 0430 0460 DAMSUP /NO, REGULAR DATA MARK
642
643 0431 0070 LCT /YES, SECOND HALF OF DELETED DATA MARK TO CNTR
644 0432 0325 OCTAL /FLUX PATTERN
645
646 0433 0054 CRC ZERO /JAM LAST 2 BITS OF DELETED DATA MARK TO CRC GEN.
647 0434 0054 CRC ZERO /NOOP
648 0435 0002 DISK /NOOP
649 0436 0002 DISK

```

```

652 0437 0063 STASH, TOG FLAG /END OF THE FIRST 0 BIT
653 0440 0075 LSR /PUT SECOND HALF OF THE DESIRED MARK IN THE TEMPB
654 0441 0064 LSP /SET UP RETURN FROM WRITE ZEROS SUBROUTINE
655 0442 0070 LCT /STALL 1.0 MICRO SECONDS
656 0443 0466 HLFOLY /SPECIFY 22 ZEROS TO BE WRITTEN BY WRT08 SUBROUTINE
657 0444 0075 LSR /NOOP
658 0445 0070 LCT /WRITE SECOND CLOCK TRANSITION
659 0446 0374 -3-1 /CALL WRITE ZEROS SUBROUTINE
660 0447 0073 ICT /LOAD SECOND HALF OF NORMAL DATA MARK
661 0450 0124 BR COFL F /JAM LAST 2 BITS OF DATA MARK TO CRC GENERATOR
662 0451 0447 -2 /GO PUT AWAY THE SECOND HALF OF THE DATA MARK
663 0452 0002 DISK /NOOP
664 0453 0070 LCT /SPECIFY 22 BITS TO BE WRITTEN BY WRT08 SUBROUTINE
665 0454 0351 -22-1 /WRITE THE 25TH CLOCK TRANSITION
666 0455 0063 TOG FLAG /CALL WRT08 SUBROUTINE
667 0456 0212 JUMP F2 /LOAD SECOND HALF OF NORMAL DATA MARK
668 0457 1322 WRT08 /JAM LAST 2 BITS OF DATA MARK TO CRC GENERATOR
669 0460 0070 DAMSUP, LCT /GO PUT AWAY THE SECOND HALF OF THE DATA MARK
670 0461 0337 OCTAL /NOOP
671 0461 0337 337 /SPECIFY 22 BITS TO BE WRITTEN BY WRT08 SUBROUTINE
672 0462 0056 CRC ONE /WRITE THE 25TH CLOCK TRANSITION
673 0463 0056 CRC ONE /CALL WRT08 SUBROUTINE
674 0464 0206 JUMP F1 /NOOP WASTE .A MICRO SECONDS
675 0465 0437 STASH /NOOP
676 0466 0062 HLFOLY, DISK /NOOP
677 0467 0070 LCT /SPECIFY 22 BITS TO BE WRITTEN BY WRT08 SUBROUTINE
678 0470 0514 WRTDAM /WRITE THE 25TH CLOCK TRANSITION
679 0471 0075 LSR /CALL WRT08 SUBROUTINE
680 0472 0070 LCT /NOOP WASTE .A MICRO SECONDS
681 0473 0351 -22-1 /NOOP
682 0474 0070 LCT /NOOP
683 0475 0351 -22-1 /NOOP
684 0476 0070 LCT /SPECIFY 22 BITS TO BE WRITTEN BY WRT08 SUBROUTINE
685 0477 0351 -22-1 /WRITE THE 25TH CLOCK TRANSITION
686 0478 0063 TOG FLAG /CALL WRT08 SUBROUTINE
687 0501 0212 JUMP F2
688 0502 1322 WRT08
689 0503 0070 PRERR, LCT
690 0504 0010 10 OCTAL
691 0505 0075 LSR /NOOP
692 0506 0214 OPEN STAT /NOOP
693 0507 0364 LSP /NOOP
694 0510 0070 LCT /ERROR CODE FOR WRT PROTECT ERROR
695 0511 0100 KAPROT /NOOP
696 0512 0226 JUMP F5 /NOOP
697 0513 0010 GOERON /NOOP
698 0514 0070 WRTDAM, LCT
699 0515 0375 -2-1 /WASTE 2.0 MICRO SECONDS
700 0516 0075 ICT /SET WRT PROTECT BIT OF STAT BECAUSE A WRITE FUNCTION WAS ATTEMPTED ON
701 0517 0075 LSR /ON A WRITE PROTECTED DISKETTE
702 0520 0075 LSR /THIS ROUTINE WILL WRITE EITHER A DATA MARK OR A
703 0520 0124 LSR /DELETED DATA MARK, THE FIRST HALF OF BOTH MARKS ARE
704 0521 0516 1-3 /IDENTICAL, THE SECOND HALF IS SPECIFIED BEFORE ENTRY BY
705 0522 0063 TOG FLAG /PUTTING THE SECOND HALF BIT PATTERN IN TEMPB
706 0523 0070 LCT
707 0524 0352 OCTAL
708 0525 0075 DECIMAL
709 0526 0070 LCT
710 0527 0370 -7-1 /NOOP
711 0530 0062 DISK /NOOP
712 0531 0120 AGAIN, BR SR7 ZERO /WHATS THE BIT?
713 0532 0502 /ZERO, NO TRANSITION
714 0533 0044 CLR BAR /ONE, RESET THE BUFFER ADDR REG TO 0
715 0534 0063 TOG FLAG /WRITE FLUX TRANSITION
716 0535 0126 BR COFL T /CHECK TRANSITION LOOP COUNT
717 0536 0503 SECHLF /GO GET SECOND HALF
718 0537 0074 ROTATE /SHIFT NEXT TRANSITION TO SR7
719 0540 0073 ICT /BUMP TRANSITION LOOP COUNTER

```

```

707 0503 0070 PRERR, LCT
708 0504 0010 10 OCTAL
709 0505 0075 LSR /NOOP
710 0506 0214 OPEN STAT /NOOP
711 0507 0364 LSP /NOOP
712 0510 0070 LCT /ERROR CODE FOR WRT PROTECT ERROR
713 0511 0100 KAPROT /NOOP
714 0512 0226 JUMP F5 /NOOP
715 0513 0010 GOERON /NOOP
716 0514 0070 WRTDAM, LCT
717 0515 0375 -2-1 /WASTE 2.0 MICRO SECONDS
718 0516 0075 ICT /SET WRT PROTECT BIT OF STAT BECAUSE A WRITE FUNCTION WAS ATTEMPTED ON
719 0517 0075 LSR /ON A WRITE PROTECTED DISKETTE
720 0520 0075 LSR /THIS ROUTINE WILL WRITE EITHER A DATA MARK OR A
721 0520 0124 LSR /DELETED DATA MARK, THE FIRST HALF OF BOTH MARKS ARE
722 0521 0516 1-3 /IDENTICAL, THE SECOND HALF IS SPECIFIED BEFORE ENTRY BY
723 0522 0063 TOG FLAG /PUTTING THE SECOND HALF BIT PATTERN IN TEMPB
724 0523 0070 LCT
725 0524 0352 OCTAL
726 0525 0075 DECIMAL
727 0526 0070 LCT
728 0527 0370 -7-1 /NOOP
729 0530 0062 DISK /NOOP
730 0531 0120 AGAIN, BR SR7 ZERO /WHATS THE BIT?
731 0532 0502 /ZERO, NO TRANSITION
732 0533 0044 CLR BAR /ONE, RESET THE BUFFER ADDR REG TO 0
733 0534 0063 TOG FLAG /WRITE FLUX TRANSITION
734 0535 0126 BR COFL T /CHECK TRANSITION LOOP COUNT
735 0536 0503 SECHLF /GO GET SECOND HALF
736 0537 0074 ROTATE /SHIFT NEXT TRANSITION TO SR7
737 0540 0073 ICT /BUMP TRANSITION LOOP COUNTER

```

```

762 0541 0206 JUMP F1
763 0542 0531 AGAIN
764
765 0543 0234 /SECOND HALF OF DATA MARK TO SR
766 0544 0071 /SR
767 0545 0075 LSR
768
769 0546 0070 LCT
770 0547 0370 -7-1
771
772
773 0550 0120 /SHALL WE WRITE A TRANSITION?
774 0551 0564 /NO
775
776 0552 0063 /YES
777 0553 0082 /NOOP
778
779 0554 0126 /DONE DATA MARKS
780 0555 0566 /YES, GO WRITE DATA
781
782 0556 0073 /NO, BUMP THE LOOP COUNTER
783
784 0557 0074 /BRING UP NEXT HALF BIT TO SR7
785
786 0560 0206 /DO ANOTHER LOOP
787 0561 0550
788
789 0562 0206 A, /WASTE 2 CYCLES TO SKIP FLUX TRANSITION
790 0563 0535 /BACK
791
792 0564 0206 B, /WASTE 2 CYCLES TO SKIP FLUX TRANSITION
793 0565 0554 /BACK
794
795
796
797
798
799
800
801 0566 0622 /THIS ROUTINE WRITES THE CONTENTS OF THE SECTOR BUFFER.
802 0567 0073 /WRTDAT, SET EGATE
803 0570 0073 /NOOP, WASTE 2 CYCLES
804
805 0571 0170 /DATA, BR %DATA0 ZERO
806 0572 0615 /WHAT'S THE DATA BIT?
807 /ZERO, GO WRITE NOTHING
808
809 0573 0056 /CRC ONE
810
811 0574 0063 /CRC ONE
812 0575 0073 /WRITE A DATA TRANSITION
813 /NOOP FOR BIT CELL TIMING
814
815 0576 0162 /DONE ENTIRE SECTOR?
816 0577 0624 /YES, GO WRITE THE CRC
817
818 0620 0046 /NO, BRING UP NEXT DATA BIT FROM SEC BUFFER

```

```

817 0601 0070 LCT
818 0602 0376 -2 /NOOP - WASTE 5 CYCLES WITH
819 0603 0073 /NOOP - A SELF TEST OF THE COUNTER
820 0604 0124 /NOOP
821 0605 0624 /NOOP
822 0605 0624 /NOOP
823
824 0606 0063 /WRITE A CLOCK TRANSITION
825
826 0607 0070 LCT
827 0610 0377 -1 /NOOP - WASTE 4 CYCLES WITH
828 0611 0124 /NOOP - A SELF TEST OF THE COUNTER
829 0612 0624 /NOOP
830 0613 0206 /GO WRITE ANOTHER DATA BIT
831 0614 0571 /DATA
832
833 0615 0054 /CRC ZERO
834 0616 0206 /JUMP F1
835 0617 0576 /BACK
836
837
838
839 0620 0070 /SELF, LCT
840 0621 0060 /SELF
841 0622 0226 /JUMP F5
842 0623 2610 /GOERDN
843
844
845
846
847
848
849
850 0624 0070 /CRC, LCT
851 0625 0357 -16-1 /PRESET BIT COUNTER FOR 16 BITS
852
853 0626 0075 /NOOP WASTE 4 CYCLES AND SELF TEST THE SR
854 0627 0082 /NOOP
855 0630 0120 /NOOP
856 0631 0620 /NOOP
857
858 0632 0063 /WRITE A CLOCK TRANSITION
859
860 0633 0076 /NOOP WASTE 6 CYCLES WITH MORE SELFTEST
861 0634 0076 /NOOP
862 0635 0076 /NOOP
863 0636 0076 /NOOP
864 0637 0120 /NOOP
865 0640 0620 /NOOP
866
867 0641 0130 /WHAT IS THE CRC BIT
868 0642 0653 /ZERO, DO NOT WRITE ANYTHING
869
870 0643 0056 /CRC ONE
871 0644 0063 /WRITE A DATA TRANSITION

```



```

072 0645 0076 ROTATE ONE /NOOP
073 0646 0073 DBACK, ICT /BUMP THE BIT COUNTER
074 0647 0126 BR COFL T /DONE CRC YET?
075 0650 0656 WRT08 /YES, GO WRITE A POSTAMBLE
076 0651 0206 JUMP F1 /NO, GO WRITE ANOTHER CRC BIT
077 0652 0627 E
078 0653 0054 CRC ZERO /BRING UP NEXT CRC BIT AND SKIP DATA TRANSITION
079 0654 0206 JUMP F1
080 0655 0646 DBACK

```

```

081 /THIS ROUTINE WRITES THE ONE BYTE POSTAMBLE, TURNS OFF
082 /WRITE CURRENT, DELAYS 511 MICRO SEC AND TURNS OFF ERASE
083 /CURRENT, IT UTILIZES THE WRITE ZEROES SUBROUTINE.

```

```

084 WRT08, LCT /SETUP TO CALL WRT08 TO WRITE 8 BITS OF ZEROES
085 CWGATE
086 LSR
087 LCT
088 -0-1

```

```

089 TOG FLAG /WRITE LAST CLOCK TRANSITION OF THE CRC FIELD
090 JUMP F2 /CALL THE SUBROUTINE WRITE ZEROES
091 WRT08

```

```

092 CWGATE, CLR WGATE /DISABLE WRITE CURRENT
093 LCT
094 CEGATE /CALL WRT08 FOR 127 BITS (511.2 MICRO SEC)
095 LSR /DELAY TO ERASE TURN OFF
096 LCT
097 -127-1
098 JUMP F2
099 WRT08

```

```

100 CEGATE, CLR EGATE /DISABLE ERASE CURRENT
101 LCT
102 READOK /CALL WRT08 FOR 25 BIT (101 MICRO SEC) DELAY
103 LSR /BEFORE TRYING TO READ
104 LCT
105 -25-1
106 JUMP F2
107 WRT08

```

```

108 REAJOK, LCT /CALL FIND HEADER ROUTINE TO INSURE

```

```

927 0707 0712 GODONE /THAT THE DISK IS STILL MOVING
928 0710 0216 JUMP F3
929 0711 1482 FINDHD

```

```

930 0712 0212 GODONE, JUMP F2 /WRITE SECTOR FUNCTION IS COMPLETE
931 0713 1486

```

```

932 /SUBROUTINE: FINDSECTOR)
933 /SUBROUTINE TO FIND A SPECIFIC SECTOR, ENTER WITH RETURN ADDRESS
934 /IN CNTR, DESIRED TRACK ADDRESS IN TRK0 AND DESIRED SECTOR ADDRESS
935 /IN TMS0. THIS SUBROUTINE ASSUMES THAT THE TARGET TRACK HAS ALREADY
936 /BEEN REACHED.

```

```

937 0714 0276 FINDSE, OPEN RTNA /SAVE RETURN ADDRESS
938 0715 0075 LSR
939 0716 0064 LSP
940 0717 0206 OPEN TEMPG /PRESET SECTOR TRY COUNT TO 52 TRIES
941 0720 0070 LCT
942 0721 0313 -52-1

```

```

943 0722 0075 AGAIN2, LSP /STORE SECTOR TRY COUNT
944 0723 0064 LSP

```

```

945 0724 0070 LCT /CALL SUBROUTINE TO FIND A HEADER
946 0725 0730 CHKSEC
947 0726 0216 JUMP F3
948 0727 1400 FINDHD

```

```

949 0730 0174 CHKSEC, BR FLAG0 ZERO /CORRECT SECTOR? FLAG=1 IF NO
950 0731 0743 WAIT /YES, GO WAIT FOR PREAMBLE

```

```

951 0732 0200 OPEN TEMPG /NO, RECALL SECTOR TRY COUNT AND INCREMENT IT
952 0733 0071 ESP
953 0734 0073 ICT

```

```

954 0735 0124 BR COFL F /52 TRIES MADE FOR SECTOR YET?
955 0736 0722 AGAIN2 /NO, TRY ANOTHER SECTOR

```

```

956 0737 0070 LCT /YES, CANN'T FIND THE SECTOR
957 0740 0070 KXHDR
958 0741 0226 JUMP F5
959 0742 2610 GOERDN

```

```

960 0743 0070 WAIT, LCT /STALL 323.2 MICRO SECONDS TO WAIT FOR DATA PREAMBLE
961 0744 0345 -26-1
962 0745 0073 ICT
963 0746 0124 BR COFL F
964 0747 0745 -2
965 0750 0073 ICT
966 0751 0124 BR COFL F
967 0752 0750 -2
968 0753 0073 ICT

```

```

902 0754 0124
903 0755 0753
904
905 0756 0270
906 0757 0283
907
908
909
910
911 /ROUTINE: READ SECTOR]
912 RDSEC, ROTATE ZERO /ZERO THE STAT
913 ROTATE ZERO
914 OPEN STAT
915 LSP
916
917 LCT
918 GOREAD
919 JUMP F0
920 FINDTR
921
922 GOREAD, JUMP F4
923 READ
924
925
926
927 0
928 0
929 0
930 0
931 0
932 0
933 0
934 0
935 0
936 0
937 0
938 0
939 0
940 0
941 0
942 0
943 0
944 0
945 0
946 0
947 0
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993 0
994 0
995 0
996 0
997 0
998 0
999 0
1000 0
1001 0
1002 0
1003 0
1004 0
1005 0
1006 0
1007 0
1008 0
1009 0
1010 0
1011 0
  
```

/CALL THE FIND TRACK SUBROUTINE TO LOCATE DESIRED SECTOR

/GO READ THE DATA FIELD

/OPEN FREE LOCATIONS
 /OPEN
 /OPEN
 /OPEN
 /OPEN

```

1012
1013
1014
1015 ERDONE, CLR DONE
1016 CLR XREG
1017
1018 INTERF /SELECT INTERFACE BUSS
1019
1020 SET ERR /ASSERT ERROR LINE
1021
1022 JUMP F2 /SKIP NEXT INSTRUCTION
1023 .+2
1024
1025 OKDONE, CLR ERR /NEGATE ERROR LTNE
1026
1027 OPEN STAT /OPEN STAT TO MOVE TO INTERFACE
1028
1029 ESP /STAT OR ERREG TO SR
1030 LSR
1031
1032 CLR SHIFT /CLEAR INTERFACE OUTPUT BUFFER
1033 CLR DONE
1034 CLR XREG
1035
1036 INTERF /SELECT INTERFACE OUTPUT BUSS
1037
1038 CLR SECDAT /SELECT SR AS DATA LINE SOURCE
1039
1040 SET IOOUT /DEFINE DATA DIRECTION AS OUT (TO INTERFACE)
1041
1042 LCT /MOVE SR TO INTERFACE SERIALLY
1043 .-8-1
1044 SET SHIFT
1045 CLR SHIFT
1046 ICT
1047 ROTATE ZERO
1048 BR COPL F
1049 .-5
1050 CLR IOOUT
1051
1052
1053
1054
1055
1056
1057
1058
1059
1060
1061
1062
1063
1064
1065
1066
  
```

/NEXT TRANSFER WILL BE FROM INTERFACE

/FUNCTION IS DONE
 /CALL GET COMMAND SUBROUTINE TO GET NEXT FUNCTION

/MOVE UNIT SELECT BIT TO SR7

/FLAG IS ALREADY SET. SAVE UNIT IN FLAG, ONCOUNT 0

/GET FIRST FUNCTION BIT TO SR7

1067			
1068	1045 0120	BR SR7 ZERO	
1069	1046 1066	FUNCT4	/FUNCTION 4 OR GREATER
1070			
1071	1047 0074	ROTATE	/GET 2ND FUNCTION BIT
1072			
1073	1050 0120	BR SR7 ZERO	
1074	1051 1057	FUNCT2	/FUNCTION CODE IS 2 OR 3
1075			
1076			
1077	1052 0074	ROTATE	/GET LAST FUNCTION BIT
1078			
1079	1053 0120	BR SR7 ZERO	
1080	1054 1107	EMPTYBUF	/FUNCTION CODE 1
1081			
1082	1055 0212	JUMP F2	/FUNCTION CODE "
1083	1056 1110	FILLBUF	
1084			
1085	1057 0074	FUNCT2, ROTATE	/GET LAST FUNCTION BIT
1086			
1087	1060 0120	BR SR7 ZERO	
1088	1061 1105	PROSEC	/FUNCTION CODE 3
1089			
1090	1062 0070	LCT	/CLR CNTR BITS TO INDICATE NORMAL DATA
1091	1063 0000	0	/FUNCTION 2
1092	1064 0206	JUMP F1	
1093	1065 0400	WRTSEC	
1094			
1095	1066 0074	FUNCT4, ROTATE	/GET 2ND FUNCTION BIT
1096			
1097	1067 0120	BR SR7 ZERO	
1098	1070 1076	FUNCT6	/FUNCTION CODE IS 6 OR GREATER
1099			
1101	1071 0074	ROTATE	/GET LAST FUNCTION BIT
1102			
1103	1072 0120	BR SR7 ZERO	
1104	1073 1224	RDRSTAT	/FUNCTION 5
1105			
1106	1074 0212	JUMP F2	/FUNCTION 4=UNUSED
1107	1075 1243	CLRID	
1108			
1109	1076 0074	FUNCT6, ROTATE	/GET LAST FUNCTION BIT
1110			
1111	1077 0120	BR SR7 ZERO	
1112	1100 1275	RDEREG	/FUNCTION 7
1113			
1114	1101 0070	LCT	/SET CNTR6 TO INDICATE DELETED DATA
1115	1122 2120	OCTAL	
1116			
1117	1103 2206	DECIMAL	
1118	1134 0400	JUMP F1	/FUNCTION 6
1119			
1120	1105 0206	PROSEC, JUMP F1	/POINTER TO READ SECTOR FUNCTION
1121	1106 0760	RDRSTAT	

1122			
1123			
1124			
1125			
1126			
1127			
1128			
1129			
1130			
1131			
1132	1107 0016	EMPTYBUF, SET IOOUT	/IOOUT IS CLEARED, SET IT TO INDICATE DATA IS /MOVING TO THE INTERFACE
1133			
1134			
1135	1110 0074	FILLBUF, ROTATE ZERO	/CLEAR STAT
1136	1111 0274	ROTATE ZERO	
1137	1112 2214	OPEN STAT	
1138	1113 0064	LSP	
1139			
1140	1114 0210	OPEN ERREG	/CLEAR ERREG
1141	1115 0264	LSP	
1142			
1143	1116 0061	FLAG OFF	/NOOP
1144			
1145	1117 0044	CLR BAR SHORT	/ADDRESS THE 1ST BIT OF SECTOR BUFFER
1146			
1147	1120 0070	LCT	
1148	1121 0177	-120-1	/SET UP BYTE COUNT TO 120 (6 BIT) OR 64 (12 BIT)
1149	1122 0152	BR XIIBIT F	
1150	1123 1126	.+3	
1151	1124 0070	LCT	
1152	1125 0277	-64-1	
1153	1126 0230	OPEN TEMPA	
1154			
1155	1127 0106	BR 10830T T	/WHICH FUNCTION IS THIS?
1156	1130 1210	EMPTY1	/EMPTYBUF
1157			
1158	1131 0012	XFRQ, SET XREQ	/REQUEST DATA TRANSFER
1159			
1160	1132 0073	ICT	/INCREMENT BYTE COUNT AND RESTORE
1161	1133 0075	LSR	
1162	1134 0064	LSP	
1163			
1164	1135 0070	LCT	/CALL WAITRUN SUBR TO WAIT FOR DATA TRANSFER
1165	1136 1141	NEWORD	
1166	1137 0222	JUMP F4	
1167	1140 2312	WAITRN	
1168			
1169	1141 0230	NEWORD, OPEN TEMPA	/REOPEN THE BYTE COUNT REGISTER BECAUSE WAITRN CLOSED IT
1170	1142 0070	LCT	/SET UP BIT COUNT IN CNTR TO 6 BITS OR 12 BITS
1171	1143 0167	-6-1	
1172	1144 0150	.+3	
1173	1145 1150	.+3	
1174	1146 0070	LCT	
1175	1147 0363	-12-1	

```

1177 1150 0104 BR JOB30T F
1178 1151 1175 FILL1
1179
1180
1181
1182
1183 0026 BYTEOUT, SET SHIFT
1184 0046 INCR BAR
1185 0024 CLR SHIFT
1186 0073 ICT
1187 0124 BR COFL F
1188 1152 BYTEOUT
1189
1190 0071 ESP
1191 0124 BR COFL F
1192 1151 XFRQ
1193
1194 0012 SET XREQ
1195 0100 BR RUN F
1196 1164 *-1
1197
1198 0010 CLR XREQ
1199
1200 0212 JUMP F2
1201 1066 OKDONE
1202
1203 0050 FIN WRTBUF
1204
1205 0046 INCR BAR
1206 0026 SET SHIFT
1207 0024 CLR SHIFT
1208
1209 0053 FILL1, START WRTBUF
1210
1211 0073 ICT
1212 0124 BR COFL F
1213 1171 *-7
1214
1215 0050 FIN WRTBUF
1216
1217 0046 INCR BAR
1218
1219 0071 ESP
1220 0124 BR COFL F
1221 1131 XFRQ
1222
1223 0212 JUMP F2
1224 1066 OKDONE
1225
1226 0032 EMPTY1, SET SECDAT
1227
1228 0073 ICT
1229 0075 LSR
1230 0064 LSP
1231

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1232 1214 0270 LCT
1233 1215 0367 *-0-1
1234 1216 2150 BR XIIBIT F
1235 1217 1152 BYTEOUT
1236 1220 0070 LCT
1237 1221 0363 *-12-1
1238
1239 0212 JUMP F2
1240 1152 BYTEOUT
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```

/ROUTINE: READ STATUS)

RDSTAT, OPEN TEMPD /SELECT THE SOFT UNIT SCRATCH PAD

UNIT ONE /PRESELECT UNIT ONE

LCT

0

BR FLAGO ZERO /WHICH UNIT? FLAG=UNIT 1

*+4 /UNIT 1, SKIP UNIT 0 SETUP

UNIT ZERO /SELECT UNIT ZERO

LCT

OCTAL

200

DECIMAL

LSR

LSP

LCT

PNTRDY

JUMP F5

CHKRDY

LSR

LSP

LCT

PNTRDY

JUMP F2

*+2

*+2

ICT

BR COFL F

1246 0061 FLAG OFF

1247 0070 LCT

1248 0372 *-5-1

1249 0122 BR SR7 T

1250 1256 *+4

1251 0074 ROTATE ZERO

1252 0212 JUMP F2

1253 1257 *+2

1254 0076 ROTATE ONE

1255 0073 ICT

1256 0124 BR COFL F

/END AROUND SHIFT OF FIRST 5 BITS

/CLEAR INIT DONE BIT OF STAT

/STATUS TO SHIFT REG

/STORE SOFT UNIT BIT

/CALL CHECKRDY SUBROUTINE, RETURN TO CLRID

```

1287 1261 1251      *0
1288 1262 0176    BR FLAG0 T      /IF FLAG IS SET THEN ROTATE IS DONE
1289 1263 1272    GODUN
1290
1291 1264 0062    FLAG ON
1292 1265 0074    ROTATE ZERO
1293 1266 0070    LCT
1294 1267 0075    *2-1
1295 1270 0212    JUMP F2
1296 1271 1251    ROT
1297
1298
1299 1272 0064    GODUN, LSP      /RESTORE STAT AND GO DONE
1300 1273 0212    JUMP F2
1301 1274 1006    OKDONE
1302
1303  /ROUTINE: READ ERROR REGISTER]
1304
1305
1306
1307 1275 0210    RDEREG, OPEN ERREG
1308 1276 0212    JUMP F2
1309 1277 1010    OKDONE*2
1310
1311
1312  /SUBROUTINE: DELAY]. THIS SUBROUTINE PROVIDES DELAYS IN MULTIPLES
1313 /OF .1MS. ENTER WITH RETURN ADDRESS IN THE SHIFT REG.
1314 /AND MULTIPLIER IN THE COUNTER
1315
1316 DELAY, OPEN RTNB      /SAVE THE RETURN ADDRESS
1317 LSP
1318
1319 1302 0075    LSR      /MULTIPLIER TO SHIFT REGISTER
1320
1321 1303 0070    LCT      /DELAY 490 CYCLES (90 MICRO SECONDS)
1322 1304 0205    *-122-1
1323 1305 0073    ICT
1324 1306 0204    OPEN RTNB
1325 1307 0124    BR COFL F
1326 1310 1305    *-3
1327
1328 1311 0071    ESP
1329 1312 0064    LSP
1330 1313 0075    LSR
1331 1314 0071    ESP
1332 1315 0064    LSP
1333
1334 1316 0073    ICT      /INCREMENT THE MULTIPLIER
1335
1336 1317 0124    BR COFL F      /ANY MORE .1MS LOOPS?
1337 1320 1301    DELAY*1      /YES, GO TO IT
1338
1339 1321 0223    JUMP F4 IND      /NO, RETURN FROM SUBROUTINE
1340
1341

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```

1342 1322 2274    *RTCS, OPEN RTN      /SAVE RETURN ADDRESS
1343 1323 0064    LSP
1344
1345 1324 0075    LSR      /PUT BIT COUNTER IN SR
1346
1347 1325 0230    OPEN TEMPA      /TEMPA IS THE PATH THROUGH THE SP
1348
1349 1326 0070    LCT      /STALL 2.6 MICRO SECONDS
1350 1327 0370    *-3-1
1351 1330 0073    ICT
1352 1331 0124    BR COFL F
1353 1332 1330    *-2
1354 1333 0064    LSP
1355 1334 0071    ESP      /NOOP
1356
1357 1335 0063    TCG FLAG      /WRITE A CLOCK TRANSITION IF WRT GATE IS SET
1358
1359 1336 0064    LSP
1360 1337 0071    ESP      /PUT BIT COUNT IN THE COUNTER
1361
1362 1340 0073    ICT      /INCREMENT BIT COUNT
1363
1364 1341 0075    LSR      /PUT UPDATED BIT COUNT BACK IN SR
1365
1366 1342 0124    BR COFL F      /DONE ALL BITS?
1367 1343 1326    LOOP      /NO
1368
1369 1344 0274    OPEN RTN      /YES, RETURN FROM SUBROUTINE
1370 1345 0207    JUMP IND F1
1371
1372
1373 1346 0222    PGOTIT, JUMP F4      /POINTER TO GETWORD FROM WAITRUM
1374 1347 2010    GOTIT
1375
1376  /ROUTINE: INITIALIZE CONT.])
1377
1378 1350 0061    TEST2, FLAG OFF      /CLEAR FLAG TO INDICATE R10 IS BEING TEST'D
1379
1380 1351 0070    TEST1, LCT      /LOOP TO TEST THAT SR IS 252 AND THAT
1381 1352 0372    *-5-1      /IT CAN BE SHIFTED,
1382 1353 0120    TOTAGN, BR SR7 ZERO      /TEST FAILURE
1383 1354 1374    INTER1      ROTATE ONE
1384 1355 0076    ROTATE ONE
1385 1356 0122    BR SR7 ONE

```

```

1397 INTER1
1398 ROTATE ZERO
1399 ICT
1400 BR COFL F
1401 TSTAGN
1402
1403 OPEN R10
1404 ESP
1405 LSR
1406
1407 ROTATE ZERO
1408
1409 BR FLAGO ONE
1410 TEST2
1411
1412 TESTDN, JUMP F0
1413 TSTRN
1414
1415 INTER1, SET ERR
1416 JUMP F2
1417 STDONE
1418
1419
1374 1374 2000
1375 1375 2000
1376 1376 2000
1377 1377 2000
    
```

/TEST FAILURE

/CONTENTS OF R10 TO SR, SHOULD BE 125

/SHIFT SR ONCF TO CHANGE 125 TO 252

/HAS R10 BEEN TESTED ALREADY?

/NO

/YES, RETURN TO REMAINING INITIALIZE ROUTINE

/SELF TEST ERROR, SET ERROR AND GO SET DONE

/OPEN

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```

/SUBROUTINE1 FINDHEADER AND FIND DATA ADDRESS MARK

/SUBROUTINE TO LOCATE A LEGAL HEADER (CORRECT CRC AND TRACK #)

/ENTER WITH THE RETURN ADDRESS IN CNTR. ALSO ROUTINE TO FIND A DATA MARK

/FOR DELETED DATA MARK.

/THIS ROUTINE LOCATES A SIX BYTE PREAMBLE OF ZEROES.

/STORE RETURN ADDRESS

/256 TO BAD START INNER COUNT

/3 TO CNTR FOR BAD START OUTER COUNT, 768 BAD STARTS ALLOWED

/RESTORE BAD START COUNT

/RESET FOR A COUNT OF 4896 AS PREAMBLE FAILURE COUNT

/24 TO CNTR AS ZERO BIT COUNT

/RESTORE ZERO BIT COUNT

/PUT 0 IN SR7 FOR DATA COMPARISONS, ALSO CONSTANT FOR 48 MICRO SEC WAIT BRANCH

/WAIT 48 MICRO SECONDS FOR SEP CLK

/ERROR, NO SEP CLK

/WHAT IS SEP DATA?

/ONE, GO CHECK PREAMBLE FAILURES

/ZERO FOUND, CHECK ZERO COUNT

/NEED MORE ZEROES FOR PREAMBLE

/FOUND PREAMBLE, CLR FLAG TO INDICATE SEARCH FOR IDAM

/START SEARCH FOR IDAM OR DATA AM, BAR IS NOSTART COUNTER

/WAIT 48 MICRO SEC FOR SEP CLK

LCT

LCT

```

1475 1443 0067 -200-1
1476 1444 0046 WBR SEPCLK T
1477 1445 1450 .+3
1478 1446 0216 JUMP F3
1479 1447 1667 TIMERR
1480
1481 1450 0156 BR DECSR7 T
1482 1451 1755 NOTYET
1483
1484 1452 0164 BR MCEGSR F
1485 1453 1673 BADSRT
1486
1487 1454 0057 PRECRC
1488 1455 0056 CRC ONE
1489 1456 0056 CRC ONE
1490
1491 1457 0070 LCT
1492 1460 0067 -200-1
1493 1461 0346 WBR SEPCLK T
1494 1462 1465 .+3
1495 1463 0216 JUMP F3
1496 1464 1667 TIMERR
1497
1498 1465 0156 BR DECSR7 T
1499 1466 1673 BADSRT
1500 1467 0166 BR MCEGSR T
1501 1470 1673 BADSRT
1502
1503 1471 0056 CRC ONE
1504 1472 0056 CRC ONE
1505 1473 0056 CRC ONE
1506
1507 1474 0070 LCT
1508 1475 0067 -200-1
1509 1476 0346 WBR SEPCLK T
1510 1477 1502 .+3
1511 1500 0216 JUMP F3
1512 1501 1667 TIMERR
1513
1514 1502 0154 BR DECSR7 F
1515 1503 1673 BADSRT
1516 1504 0164 BR MCEGSR F
1517 1505 1673 BADSRT
1518
1519 1506 0070 LCT
1520 1507 0000 0
1521 1510 0075 LSR
1522
1523 1511 0070 LCT
1524 1512 0067 -200-1
1525 1513 0346 WBR SEPCLK T
1526 1514 1517 .+3
1527 1515 0216 JUMP F3
1528 1516 1667 TIMERR
1529

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TRX01 FLOPPY CONTROLLER FIRMWARE PAL10 V142A 9-FEB-76 9:17 PAGE 10-2
1530 1517 0154 BR DECSR7 F
1531 1520 1673 BADSRT
1532 1521 0042 LDMD
1533 1522 0042 LDMD
1534 1523 0164 BR MCEGSR F
1535 1524 1673 BADSRT
1536
1537 1525 0070 LCT
1538 1526 0067 -200-1
1539 1527 0346 WBR SEPCLK T
1540 1530 1533 .+3
1541 1531 0216 JUMP F3
1542 1532 1667 TIMERR
1543
1544 1533 0156 BR DECSR7 T
1545 1534 1673 BADSRT
1546
1547 1535 0176 BR FLAGO T
1548 1536 1675 DAM
1549
1550 1537 0164 BR MCEGSR F
1551 1540 1673 BADSRT
1552
1553 1541 0056 CRC ONE
1554
1555 1542 0070 LCT
1556 1543 0067 -200-1
1557 1544 0346 WBR SEPCLK T
1558 1545 1550 .+3
1559 1546 0216 JUMP F3
1560 1547 1667 TIMERR
1561
1562 1550 0156 BR DECSR7 T
1563 1551 1673 BADSRT
1564 1552 0164 BR MCEGSR F
1565 1553 1673 BADSRT
1566
1567 1554 0042 LDMD
1568
1569 1555 0056 CRC ONE
1570
1571 1556 0070 LCT
1572 1557 0067 -200-1
1573 1560 0346 WBR SEPCLK T
1574 1561 1564 .+3
1575 1562 0216 JUMP F3
1576 1563 1667 TIMERR
1577
1578 1564 0156 BR DECSR7 T
1579 1565 1673 BADSRT
1580 1566 0166 BR MCEGSR T
1581 1567 1673 BADSRT
1582
1583 1570 0054 CRC ZERO
1584

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```

/THIS ROUTINE COMPARES THE HEADER TRACK ADDRESS TO THE
 /DESIRED TRACK ADDRESS ON THE FLY. IT IS ENTERED AFTER
 /FINDING THE IDAM, ERREG BIT IS SET IF AN ERROR IS DETECTED.

```

HDCOM, OPEN TARTRK /TARGET TRACK ADDRESS TO BR
ESP
LSR
LCT /SET BIT COUNTER TO 8
-8-1
AGAIN3, BR SEPCLK F /WAIT FOR BIT CELL
.-1
BR DEGR7 T /SEP DATA EQUAL TO BR77
.+4 /NO, TRACK COMPARE ERROR
ROTATE ZERO /YES, GET NEXT TRACK ADDRESS BIT
JUMP F3
.+4
OPEN ERREG /SET ERREG BIT 9 TO INDICATE TRACK ERROR
ROTATE ONE
LSP
DATCRC /UPDATE THE CRC
ICT /INCREMENT AND TEST THE BIT COUNTER
BR COFL F /GO DO NEXT BIT
AGAIN3
LCT /TRACK COMPARED, SET UP BIT COUNTER FOR 8 BYTE
-8-1
AGAIN4, BR SEPCLK F /WAIT FOR BIT
.-1
FLAG OFF /CLEAR FLAG FOR NEXT ROUTINE
FLAG OFF /NOOP FOR LONG SEP CLK
FLAG OFF /NOOP FOR LONG SEP CLK
FLAG OFF /NOOP FOR LONG SEP CLK
DATCRC /UPDATE CRC
ICT /INCREMENT AND TEST BIT COUNT
BR COPL F /GO DO ANOTHER BIT
AGAIN4 /CONTINUE

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/THIS ROUTINE COMPARES THE HEADER SECTOR ADDRESS WITH THE
 /TARGET SECTOR ADDRESS ON THE FLY. IT IS ENTERED FROM
 /THE TRACK COMPARE ROUTINE. A MISMATCH WILL SET THE FLAG.

```

OPEN TARSEC /TARGET SECTOR ADDRESS TO BR
ESP
LSR
LCT /SET UP BIT COUNTER FOR 8 BITS
-8-1
AGAIN5, BR SEPCLK F /WAIT FOR A BIT
.-1
BR DEGR7 T /NO- DO THEY COMPARE?
.+3 /BAD, GO SET THE FLAG
JUMP F3 /GOOD, SKIP THE ERROR FLAG.
.+2
FLAG ON /SET FLAG TO INDICATE MISMATCH
ROTATE ZERO /BRING UP NEXT BIT
DATCRC /UPDATE THE CRC
ICT /BUMP THE BIT COUNTER
BR COFL F /ALL BITS COMPARED?
AGAIN5 /NO, LOOP BACK
LCT /YES, SETUP TO WAIT FOR END OF
-24-1 /CRC
AGAIN6, BR SEPCLK F /WAIT FOR BIT
.-1
ROTATE ZERO /NOOP FOR LONG SEP CLK
ROTATE ZERO /NOOP FOR LONG SEP CLK
ROTATE ZERO /NOOP FOR LONG SEP CLK
DATCRC /UPDATE CRC
ICT /BUMP THE BIT COUNTER
AGAIN6 /ALL DONE?
AGAIN6 /NO, LOOP BACK
JUMP F5 /YES, GO CHECK IF CRC IS ALL ZEROS
CKMCR
TIMERR, LCT /80 MICROSEC PASSED AND NO SEP CLOCK HAS BEEN
KTIMERR
JUMP F5
GOERDN

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BADSR T
JUMP F5
BDSRT
DAM,
BR MCEGSR T
BDSRT
CRC ZERO
LCT
-200-1
HBR SEPCLK T
+3
JUMP F3
TIMERR
BR MCEGSR F
BDSRT
LDMD
BR DEOSR7 T
DELDAT
CRC ONE
LCT
-200-1
HBR SEPCLK T
+3
JUMP F3
TIMERR
CRC ONE
BR DEOSR7 F
ENDDM
JUMP F3
BDSRT
DELDAT, CRC ZERO
LCT
-200-1
HBR SEPCLK T
/MISSING CLK SHOULD BE T
/JAM 6TH CRC BIT OF DATA AM
/WAIT FOR SIXTH BIT CELL
/MISSING CLK SHOULD BE F
/NOOP FOR LONG SEP CLK
/IF DATA8 THEN LOOK FOR DELETED DATA AM
/JAM 7TH BIT OF DATA AM
/WAIT FOR SEVENTH BIT OF DATA AM
/JAM LAST BIT OF DATA AM
/DATA SHOULD BE 1
/FLAG IS SET TO INDICATE NORMAL DATA MARK
/LAST DATA BIT WAS BAD
/JAM 7TH CRC BIT OF DEL DATA AM
/WAIT FOR 7TH CELL OF DEL DATA AM

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1801
1802
+3
JUMP F3
TIMERR
FLAG OFF
CRC ZERO
BR DEOSR7 F
BDSRT
ENDDM, BR MCEGSR F
BDSRT
JUMP F4
DATA
NOZERO, INCR BAR
BR BAROFL F
TRYAGN+3
LCT
KNXPRAM
JUMP F5
GOERDN
MUTVET, INCR BAR
LDMD
BR BAROFL F
GETDAMY1
LCT
KNXIDAM
JUMP F5
GOERDN
PNTRDY, JUMP F2
CLRZD
P/SRDY, JUMP F2
CLRZD
PNORDY, JUMP F2
OKDONE
JUMP F5
INTRDY
0
0
0
/OPEN
/OPEN
/OPEN
/INCR AND TEST IDAM OR DATA AM START FAILURE COUNT
/NOOP FOR LONG SEP CLK
/OK, TRY AGAIN
/100 MANY ZEROS WHILE LOOKING FOR START OF
/IDAM OR DATA AM
/OK, TRY AGAIN
/POINTERS FROM CHECKRDY SUBROUTINE TO RDBSTAT ROUTINE
/POINTERS FROM CHECK RDY TO INITIALIZE ROUTINE

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1803 /SUBROUTINE GETWORD AND GETCOMMAND1
1804 /SUBROUTINE TO GET AN EIGHT BIT WORD FROM THE INTERFACE.
1805 /IF TALKING TO A PDP8 INTERFACE IN 12 BIT MODE, THERE
1806 /WILL BE FOUR MEANINGLESS BITS PRECEDING THE DESIRED EIGHT
1807 /BIT WORD. ENTER THIS SUBROUTINE WITH THE RETURN ADDRESS
1808 /IN THE COUNTER. EXIT WITH THE ONES COMPLIMENT OF THE
1809 /DESIRED WORD IN THE SHIFT REGISTER. PARITY IS COMPUTED AND
1810 /CHECKED ON ALL WORDS.
1811
1812
1813 GETWRD, SET XREQ /REQUEST A WORD FROM INTERFACE
1814
1815 GETCMD, LSR /STASH THE RETURN ADDRESS
1816 OPEN RTNA
1817 LSP
1818
1819 LCT
1820 PGOTIT /CALL SUBR WAITRN TO WAIT FOR A WORD
1821 JUMP F4
1822 WAITRN
1823
1824 GOTIT, OFF FLAG /CLEAR FLAG FOR PARITY CHECK
1825
1826 CLR ENR /IN CASE RUN HAS A RESPONSE TO DONE
1827 CLR DONE
1828
1829 LCT
1830 *-8-1 /SET UP BIT COUNT IN CNTR. 8 BIT OR 12 BIT
1831 BR XIIBIT F
1832 *-3
1833 LCT
1834 *-12-1
1835
1836 *ATDAT, BR DATAIN ONE /WHAT IS THE DATA BIT?
1837 *GOTONE /ITS A ONE, GO SAVE IT
1838
1839 BR COFL T /ITS A ZERO, WAS IT THE PARITY BIT (9TH BIT)?
1840 CHKPAR /YES, GO CHECK PARITY
1841
1842 ROTATE ONE /NO SAVE THE DATA BIT COMPLIMENTED IN SR
1843
1844 JUMP F4 /GO SHIFT UP ANOTHER BIT.
1845 NUTHER
1846
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1850
1851 GOTONE, TOG FLAG /COMPLIMENT THE PARITY GENERATOR
1852
1853 BR COFL T /WAS IT THE PARITY BIT?
1854 CHKPAR /YES, GO CHECK PARITY
1855
1856 ROTATE ZERO /NO, SAVE THE COMPLIMENTED DATA BIT IN SR
1857
1858 NUTHER, SET SHIFT /SHIFT PULSE AND INCREMENT BIT COUNT

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1858 2035 0073 ICT
1859 2036 0024 CLR SHIFT
1860
1861 2037 0222 JUMP F4
1862 2040 2021 PAYDAT
1863
1864
1865 2041 2176 CHKPAR, BR FLAGO ONE /WHERE THERE AN ODD NO. OF ONES?
1866 2042 2076 GOTWRD /YES, PARITY HAS GOOD
1867
1868 2043 0214 OPEN STAT /NO, STAT TO SR
1869 2044 0371 ESP
1870 2045 2075 LSR
1871
1872 LCT
1873 *-5-1
1874 BR SR7 T
1875 *-4
1876 ROTATE ZERO
1877 JUMP F4
1878 2054 2056 *-2
1879 2055 0076 ROTATE ONE
1880 2056 0073 ICT
1881 2057 0124 BR COFL F
1882 2060 2050 *-8
1883
1884 2061 0074 ROTATE ZERO
1885 2062 0076 ROTATE ONE
1886
1887 2063 0122 BR SR7 T
1888 2064 2070 *-4
1889 2065 0074 ROTATE ZERO
1890 2066 0222 JUMP F4
1891 2067 2071 *-2
1892 2070 0076 ROTATE ONE
1893
1894 2071 0064 LSP
1895
1896 2072 0070 LCT
1897 2073 0210 KPARER /ERRCODE FOR PARITY ERROR
1898 2074 0226 JUMP F5
1899 2075 2610 GOERON
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1901 2076 0270 GOTWRD, OPEN RTNA /WORD WAS GOOD, EXIT FROM GETWRD, GETCMD
1902 2077 0263 JUMP F0 IND

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/ISSUBROUTINE: STEPHEAD]
/THIS SUBROUTINE WILL STEP THE SPECIFIED NUMBER OF TRACKS IN THE
/SPECIFIED DIRECTION, DIRECTION IS DETERMINED BY THE HD DIR FLOP
/THE NUMBER OF STEPS IS IN THE SR, RETURN ADDRESS IS IN THE CNTR,
/EXIT IS TO THE RETURN ADDRESS IF HOMP IS DETECTED, EXIT IS TO RETURN
/PLUS 2 IF THE LAST STEP HAS BEEN TAKEN, AFTER THE LAST STEP IS TAKEN,
/THE HEAD IS LOADED AND A 25MS DELAY IS EXECUTED FOR HEAD SETTLE TIME

STEPHD, OPEN RTNA    /STORE RETURN ADDR AND MOVE STEP COUNT TO CNTR
  LSP
  LSR
  ESP
  LSP
CKHOME, BR HOME T   /IS THE HEAD HOME?
  OUT                               /YES, GO EXIT
  ICT                               /NO, INCREMENT STEP COUNT AND STORE IN TEMPA
  LSR
  OPEN TEMPA
  LSP
  LCT
  SECPLS
  LSR
  LCT
  -30-1
  SET STPHD
  CLR STPHD
  JUMP F2
  DELAY
  SECPLS, SET STPHD  /ISSUE SECOND STEP PULSE
  CLR STPHD
  LCT
  DONSTP
  LSR
  LCT
  -30-1
  JUMP F2
  DELAY
  DONSTP, OPEN TEMPA /CHECK STEP COUNT
  ESP                               /NOT DONE, GO CHECK IF HOME
  BR COFL F
  CKHOME
  
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OPEN RTNA
  ESP
  ICT
  ICT
DLY25, OPEN RTNA
  LSR
  LSP
  OUT,
  LDMD
  OPEN TEMPE
  LCT
  OCTAL
  200
  DECIMAL
  LSR
  LSP
  LCT
  DONDLY
  LSR
  LCT
  -255-1
  JUMP F2
  DELAY
DONDLY, OPEN RTNA
  JUMP F0 IND

/[ROUTINE: READ SECTOR CONT.]
READ, LCT
  -3-1
  OPEN TEMPB
  LSR
  LSP
  LCT
  -120-1
  ICT
  FLAG ON
  BR COFL F
  .-3
  ICT
  LSR
  JUMP F3
  SETDAM
  
```

/DONE STEPPING, INCREMENT RETURN ADDRESS BY 2

/STORE RETURN ADDRESS ALSO START OF 25MS DELAY SUBROUTINE

/LOAD HEAD
/SET SOFT HD LOAD BIT

/CALL DELAY SUBR FOR 25MS DELAY

/RETURN FROM STEP HEAD OR DELAY 25MS SUBROUTINE

/3 TO DATA MARK TRY COUNTER

/STALL FOR 96 MICRO SEC (3 BYTES) TO AVOID WRT TURN ON SPLASH

/SET THE FLAG TO SPECIFY DATA AM IN FIND AM ROUTINE

/CLR COUNTER AND SR

/GO TRY FIND THE ADDRESS MARK

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      DATA, CLR BAR /CLEAR THE BUFFER ADDRESS REGISTER
      BR SEPCLK F /WAIT FOR CLOCK
      .-1
      START WRTBUF /START THE WRITE PULSE FOR THIS BIT
      DATCRC /UPDATE THE CRC WITH SEP DATA
      BR BAROFL T /IS BUFFER FULL YET?
      GETCRC /YES, GO GET THE CRC
      FIN WRTBUF /NO, END THE WRITE PULSE
      INCR BAR /ADDRESS NEXT SECTOR BUFFER CELL
      JUMP F4 /LOOP BACK FOR NEXT BIT
      DATA+1
      GETCRC, FIN WRTBUF /END THE WRITE PULSE FOR THE LAST BIT
      LCT /SET BIT COUNT TO 16 FOR 2 BYTE CRC
      -16-1
      BR SEPCLK F /WAIT FOR NEXT BIT
      .-1
      LDMD /4 NOOPS FOR LONG SEP CLOCK
      LDMD
      LDMD
      LDMD
      DATCRC /PUT CRC BIT IN THE CRC GENERATOR
      ICT /INCREMENT AND TEST BIT COUNT
      BR COFL F /NOT DONE, GET ANOTHER
      .-9
      OPEN STAT /STATUS TO SHIFT REG
      ESP
      LSR
      BR SRT T /END AROUND SHIFT OF DRV RDY BIT OF STAT IN SR
      +4
      ROTATE ZERO
      JUMP F4
      +2
      ROTATE ONE
      LCT /END AROUND SHIFT OF NEXT 5 BITS OF STAT IN SR
      -5-1
      BR SRT T
      +4
      ROTATE ZERO
      JUMP F4
      +2
      ROTATE ONE
      ICT
      BR COFL F
      .-8
      LCT
      -16-1
      BR CRC16 ONE
      DCRCER
      CRC ZERO
      ICT
      BR COFL F
      .-5
      ROTATE ZERO
      LSP
      JUMP F2
      OKDONE
      DCRCER, ROTATE ONE
      LSP
      LCT
      KDCRCR
      JUMP F5
      GOERDN
  
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      +4
      ROTATE ONE
      JUMP F4
      +2
      ROTATE ZERO
      LCT
      -5-1
      BR SRT T
      +4
      ROTATE ZERO
      JUMP F4
      +2
      ROTATE ONE
      ICT
      BR COFL F
      .-8
      LCT
      -16-1
      BR CRC16 ONE
      DCRCER
      CRC ZERO
      ICT
      BR COFL F
      .-5
      ROTATE ZERO
      LSP
      JUMP F2
      OKDONE
      DCRCER, ROTATE ONE
      LSP
      LCT
      KDCRCR
      JUMP F5
      GOERDN
  
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/[SUBROUTINE: WAIT FOR RUN]
 /THIS SUBROUTINE WILL WAIT FOR RUN. IF 46MS ELAPSES, THE HEAD IS UNLOADED
 /AND THE ROUTINE CONTINUES WAITING FOR RUN. RETURN ADDRESS IS PASSED
 /VIA THE COUNTER

```

      WATRNB, OPEN RTNB      /STASH THE RETURN ADDRESS
      LSR
      LSP
      BR RUN T              /GOT RUN?
      GOTRUN
      OPEN TEMPC           /PRESET LOOP COUNTER TO 0
      LCT
      0
      LSR
      LSP                   /RESTORE LOOP COUNT
      WBR RUN T           /TIME WHILE WAITING FOR FUN
      GOTRUN
      WBR RUN T
      GOTRUN
      WBR RUN T
      GOTRUN
      WBR RUN T
      GOTRUN
      ESP
      ICT                   /INCREMENT AND TEST LOOP COUNT
      BR COFL F
      BACK
      OPEN TEMPE
      ICT
      LSR
      LSP
      UNWD
      BR RUN F
      0=1
      GOTRUN, CLR XREG     /IF RUN WAS RESPONSE TO XFREG
      OPEN RTNB
      JUMP IND F2         /RETURN FROM WATRNB SUBROUTINE
  
```

/46MS NOT ELAPSED YET
 /TIME IS EXPIRED (45.6 MS). CLEAR THE SOFT HDLD BIT AND UNLOAD THE HEAD
 /WAIT FOR RUN. FOREVER IF NECESSARY
 /IF RUN WAS RESPONSE TO XFREG
 /RETURN FROM WATRNB SUBROUTINE

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/[ROUTINE: INITIALIZE CONT.]
 /CONTINUATION OF THE INITIALIZE SELF TEST

```

      TEST, LCT
      OCTAL
      252
      DECIMAL
      LSR
      OPEN R5
      LSP
      LCT
      OCTAL
      125
      DECIMAL
      LSR
      OPEN R10
      LSP
      FLAG ON
      BR FLAGO T
      +3
      JUMP F2
      INTER1
      OPEN R5
      ESP
      LSR
      JUMP F2
      TEST1
      1351
      V
      0
  
```

/LOAD R5 WITH TEST PATTERN 252
 /LOAD R10 WITH TEST PATTERN 125
 /SET FLAG AND TEST IT
 /FLAG FAILURE
 /CONTENTS OF R5 TO SR. SHOULD BE 252
 /GO CONTINUE UNIT TEST IN FLD 2
 /OPEN
 /OPEN

2197 /SUBROUTINE: MAGNITUDE COMPARISON)
 2198 /THIS SUBROUTINE COMPARES THE EIGHT BIT NUMBERS IN REGISTERS F AND G
 2199 /EXIT IS TO THE RETURN ADDRESS IF F<G. IF F<G, RETURN IS TO RTNA+2.
 2200 /IF F>G, RETURN IS TO RTNA+4. CONTENTS OF F AND G ARE UNDEFINED AT
 2201 /THE END OF THE SUBROUTINE

```

2202 2406 0230 MAGCOM, OPEN TEMPA /FOR BIT COUNT
2203 2401 0070 LCT /BIT COUNT IS 0
2204 2402 0367 -0-1
2205 2403 0075 LSP /RESTORE BIT COUNT
2206 2404 0064 LSP
2207 2405 0254 OPEN TEMPF /F TO SR
2208 2406 0071 ESP
2209 2407 0075 LSR
2210 2410 0120 BR SR7 ZERO /TEST F
2211 2411 2443 TSTG0 /ITS 0
2212 2412 0076 ROTATE ONE /ITS 1, BRING UP NEXT BIT
2213 2413 0064 LSP /RESTORE F
2214 2414 0260 OPEN TEMPG /G TO SR
2215 2415 0071 ESP
2216 2416 0075 LSR
2217 2417 0120 BR SR7 ZERO /TEST G
2218 2420 2432 GLESSF /ITS 0, G IS LESS THAN F
2219 2421 0074 NEXTG, ROTATE ZERO /ITS 1, BRING UP NEXT G BIT
2220 2422 0064 LSP /RESTORE G
2221 2423 0230 OPEN TEMPA /INCREMENT AND TEST BIT COUNT
2222 2424 0071 ESP
2223 2425 0075 ICT
2224 2426 0124 BR COFL F
2225 2427 2403 MAGCOM+3 /GO COMPARE ANOTHER BIT
2226 2430 0270 OPEN RTNA /ALL BITS COMPARED, NO DIFFERENCE
2227 2431 0203 JUMP F0 IND
2228 2432 0270 GLESSF, OPEN RTNA /G IS LESS THAN F RETURN TO RTNA +4
2229 2433 0071 ESP
2230 2434 0073 ICT
2231 2435 0073 ICT
2232 2436 0073 ICT
2233 2437 0073 ICT
2234 2438 0075 LSR
    
```

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2252 2441 0064 LSP
2253 2442 0203 JUMP F0 IND
2254 2443 0074 TSTG0, ROTATE ZERO /F WAS 0, BRING UP NEXT BIT
2255 2444 0064 LSP /RESTORE F
2256 2445 0260 OPEN TEMPG /G TO SR
2257 2446 0071 ESP
2258 2447 0075 LSR
2259 2454 0120 BR SR7 ZERO /TEST G
2260 2451 2421 NEXTG /MATCHES F, GO BRING UP NEXT G BIT
2261 2452 0270 OPEN RTNA /G IS LESS THAN F, RETURN TO RTNA +2
2262 2453 0271 ESP
2263 2454 0226 JUMP F5
2264 2455 2436 GLESSF+4
    
```

/SUBROUTINE: FIND TRACK CONT.]

```

2456 0270 HUMERR, LCT /NONE FOUND BEFORE LAST STEP TAKEN
2457 0050 KMHERR
2460 0226 JUMP F5
2461 2610 GOERDN
    
```

/SUBROUTINE: DIFFERENCE]
 /THIS SUBROUTINE COMPUTES THE DIFFERENCE BETWEEN TWO EIGHT BIT
 /NUMBERS. ENTER WITH THE RETURN ADDRESS IN RTN, A IN THE
 /COUNTER, AND B IN THE SHIFT REGISTER. EXIT IS MADE WITH THE
 /COMPLEMENT OF THE DIFFERENCE IN THE SHIFT REGISTER.
 /EXIT IS TO RTN IF A>B. EXIT IS TO RTN+2 IF A<B

```

2462 0230 DIF, OPEN TEMPA /OPEN TEMPORARY PATH THRU THE SP
2463 0120 BR COFL T /HAS A REACHED ALL ONES YET?
2464 2501 DIFB /YES, GO GET R FOR THE DIFFERENCE
2465 0064 LSP /NO, GET B
2466 0075 LSR /A INTO SHIFT REG
2467 0071 ESP /B INTO COUNTER
2470 0126 BR COFL T /HAS B REACHED ALL ONES YET?
2471 2503 DIFA /YES, GO GET A FOR THE DIFFERENCE
2472 0073 ICT /INCREMENT B
2473 0064 LSP // BRING BACK A
2474 0075 LSR /B INTO SHIFT REG
2475 0071 ESP // A INTO COUNTER
    
```

/RX01 FLOPPY CONTROLLER FIRMWARE PAL10 V102A 9-FEB-76 9117 PAGE 1502
 2307 2476 0073 ICT /INCREMENT A
 2308 2477 0226 JUMP F5 /GO BACK TO TEST A AGAIN
 2309 2500 2463 DIF+1
 2310
 2311
 2312 2501 0270 DIFB, OPEN RTNA /B IS THE COMPLEMENT OF THE DIFFERENCE
 2313 2502 0203 JUMP F0 IND /EXIT A=BB
 2314
 2315
 2316
 2317 2503 0270 DIFA, OPEN RTNA /A IS THE COMPLEMENT OF THE DIFFERENCE
 2318 2504 0071 ESP /INCREMENT THE RETURN ADDRESS BY 2
 2319 2505 0073 ICT
 2320 2506 0073 ICT
 2321 2507 0064 LSP /RESTORE RETURN ADDRESS TO SCRATCHPAD AND A TO BR
 2322 2510 0075 LSR
 2323 2511 0071 ESP
 2324 2512 0064 LSP
 2325 2513 0075 LSR
 2326
 2327 2514 0203 JUMP F0 IND /EXIT A=BB
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/[ROUTINE1 FIND HEADER CONT.]
 /THIS ROUTINE CHECKS THE CRC, AND THE RESULTS OF THE TRACK
 /AND SECTOR COMPARISONS.

CKHCRC, LCT /PRESET BIT COUNT TO 16 FOR CRC
 -16-1
 BR CRC16 ONE /IS CRC ZERO
 HRCRCR /NO, LOG ERROR AND TRY AGAIN
 ICT /YES, CRC GOOD SO FAR, BUMP BIT CNTR
 CRC ZERO /BRING UP NEXT CRC BIT
 BR COFL F /ALL BITS TESTED?
 .-5 /NO, BRANCH BACK
 OPEN ERREG /YES, CRC WAS GOOD, CHECK TRK COMP
 ESP
 LSR
 LCT /ROTATE BIT 0 TO BIT 7
 -7-1
 ROTATE ZERO
 ICT
 BR COFL F /DONE ROTATING?
 .-3 /NO

/RX01 FLOPPY CONTROLLER FIRMWARE PAL10 V102A 9-FEB-76 9117 PAGE 1503
 2362 2536 0122 BR SRT ONE /YES, WAS THERE A BAD COMPARE
 2363 2537 2542 TKSNER /YES, GO REPORT A TRACK SEEK ERROR
 2364
 2365 2544 0264 OPEN RTNA /CORRECT TRACK, EXIT FROM FIND HDR SUBR
 2366 2541 0207 JUMP F1 IND
 2367
 2368
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 2370
 2371 2542 0070 TKSNER, LCT /HEADER CRC WAS NOT CORRECT
 2372 2543 0150 KTKSKR /ADDRESS DID NOT COMPARE, MUST
 2373 2544 0226 JUMP F5 /EXIT TO ERROR NONE
 2374 2545 2610 GOERDN
 2375
 2376
 2377 2546 0070 HRCRCR, LCT /HEADER CRC WAS NOT CORRECT
 2378 2547 0140 KRCRCR /ROTATE BIT 0 TO BIT 7
 2379 2552 0275 LSR /ROTATE ZERO
 2380 2551 0210 OPEN ERREG /LOG THE ERROR
 2381 2552 0064 LSP
 2382
 2383 2553 0226 JUMP F5 /GO TRY ANOTHER HEADER
 2384 2554 2557 RADHDR
 2385
 2386
 2387
 2388
 2389 2555 0170 BDSRT, BR FLAGO T /BAD START ON DATA AM OR IDAM?
 2390 2556 2577 RADDAM
 2391
 2392 2557 0230 BADHDR, OPEN TEMPA /IDAM, INCREMENT AND TEST BAD START INNER COUNT
 2393 2560 0071 ESP
 2394 2561 0073 ICT
 2395 2562 0275 LSR
 2396 2563 0064 LSP
 2397 2564 0124 BR COFL F /NO OVERFLOW, GO TRY ANOTHER HEADER
 2398 2565 2615 PTRYAG /INCREMENT AND TEST BAD START OUTER COUNT
 2399 2566 0234 OPEN TEMPB
 2400 2567 0071 ESP
 2401 2570 0073 ICT
 2402 2571 0124 BR COFL F /NO OVERFLOW, GO TRY AGAIN
 2403 2572 2615 PTRYAG /TOO MANY TRIES FOR A HEADER
 2404 2573 0070 LCT
 2405 2574 0160 XSTRYS, KXSTRYS
 2406 2575 0226 JUMP F5
 2407 2576 2610 GOERDN
 2408
 2409
 2410 2577 0234 BADDAM, OPEN TEMPB
 2411 2600 0071 ESP
 2412 2601 0073 ICT
 2413 2602 0075 LSR
 2414 2603 0064 LSP
 2415 2604 0124 BR COFL F
 2416 2605 2617 PGETDA /NO OVERFLOW GO TRY FOR DATA AM AGAIN

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2417 2609 0070 NODAM, LCT
2418 2607 0170 LCT
2419 2610 0210 KNODAM
2420 2611 0075 GOERDN, OPEN ERREG
2421 2612 0064 LSR
2422 2613 0212 LSR
2423 2614 1000 JUMP F2
ERDONE
2424
2425 2615 0216 PTRYAG, JUMP F3
2426 2616 1413 /POINTER TO FIND AN IDAM
2427
2428
2429 2617 0216 PGETDA, JUMP F3
2430 2620 1441 /POINTER TO FIND DATA AM
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2436 2621 0070 /ROUTINE: INITIALIZE CONT.1
2437 2622 0030 WRONG, LCT
2438 2623 0226 K-RONG /HOME WAS FOUND WHILE STEPPING OUT
2439 2624 2610 GOERDN
2440
2441 2625 0070 DNRCAL, LCT
2442 2626 1771 PNRDLY
2443 2627 0226 JUMP F5
2444 2630 2640 CHKRDY
2445
2446 2631 0070 INTRDY, LCT
2447 2632 0770 GOREAD
2448 2633 0274 OPEN RTN
2449 2634 0075 LSR
2450 2635 0064 LSR
2451 2636 0202 JUMP F0
2452 2637 0252 BOOT
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2456 2640 0274 CHKRDY, OPEN RTN /SAVE RETURN ADDRESS
2457 2641 0075 LSR
2458 2642 0064 LSR
2459 2643 0070 LCT
2460 2644 0375 -2-1 /2 TO CNTR FOR INDEX PASS COUNT
2461 2645 0230 OPEN TEMPA /FOR INDEX PASS COUNT
2462 2646 0075 NEMPAS, LSR /RESTORE INDEX PASS COUNT
2463 2647 0064 LSP
2464 2650 0061 FLAG OFF /CLOSE INDEX WINDOW
2465 2651 0042 LDHD /TO CLEAR INDEX FLOP
2466 2652 0070 LCT /FOR 15 TIMES THROUGH 10MS LOOP
2467 2653 0360 -15-1
2468 2654 0234 STDLY, OPEN TEMPB /RESTORE OUTER COUNT
2469 2655 0075 LSR
2470 2656 0064 LSP
2471 2657 0070 LCT /FOR 40 TIMES THROUGH .25MS LOOP
2472 2658 0327 -40-1
2473 2659 0240 OPEN TEMPC /RESTORE INNER COUNT
2474 2660 0075 SPBACK, LSR
2475 2661 0064 LCT
2476 2662 0070 -250-1 /WAIT .25 MS FOR INDEX
2477 2663 0005 BR INDX T /FOUND INDEX
2478 2664 0116 SAWIND
2479 2665 2714 ICT
2480 2666 0073 BR COFL F
2481 2667 0124 .-4
2482 2668 2672 2666 /INCREMENT AND TEST INNER COUNT
2483 2669 0240 OPEN TEMPC
2484 2670 0071 ESP
2485 2671 0073 ICT
2486 2672 0124 BR COFL F
2487 2673 2662 2662 SPBACK
2488 2674 2662 2662
2489 2675 0070
2490 2676 0005
2491 2677 0116
2492 2678 2714
2493 2679 0073
2494 2680 0124
2495 2681 2666
2496 2682 2666
2497 2683 0240
2498 2684 0071
2499 2685 0073
2500 2686 0124
2501 2687 2662
2502 2688 2662
2503 2689 0240
2504 2690 0071
2505 2691 0073
2506 2692 0124
2507 2693 2662
2508 2694 2662
2509 2695 0240
2510 2696 0071
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2511 2700 0234 OPEN TEMPB
2512 2701 0071 ESP
2513 2702 0073 ICT
2514 2703 0124 BR COFL F
2515 2704 2655 STDLY+1
2516 2705 0176 BR FLAGO ONE
2517 2706 2767 UNRDY
2518 2707 0062 FLAG ON
2519 2710 0070 LCT
2520 2711 0374 -3-1
2521 2712 0226 JUMP FS
2522 2713 2654 STDLY
2523 2714 0230 SAWIND, OPEN TEMPB
2524 2715 0071 ESP
2525 2716 0073 ICT
2526 2717 0124 BR COFL F
2527 2720 2646 NEMPAS
2528 2721 0174 BR FLAGO ZERO
2529 2722 2767 UNRDY
2530 2723 0274 OPEN RTN
2531 2724 0071 ESP
2532 2725 0073 ICT
2533 2726 0073 ICT
2534 2727 0075 LSR
2535 2730 0064 LSP
2536 2731 0214 OPEN STAT
2537 2732 0071 ESP
2538 2733 0075 LSR
2539 2734 0076 ROTATE ONE
2540 2735 0061 FLAG OFF
2541 2736 0070 LCT
2542 2737 0374 ROT3,
2543 2740 0122 -3-1
2544 2741 2745 BR SR7 T
2545 2742 0074 ROTATE ZERO
2546 2743 0226 JUMP FS
2547 2744 2746 +2
2548 2745 0076 ROTATE ONE
2549 2746 0073 ICT
2550 2747 0124 BR COFL F
2551 2750 2740 .-8
2552 2751 0176 BR FLAGO T

```

/INCREMENT AND TEST OUTER COUNT

/WAS INDEX WINDOW OPEN?
/YES, NO INDEX WITHIN 100MB

/NO, OPEN WINDOW

/FOR 3 TIMES THROUGH 10 MS LOOP
/THE WINDOW IS 30 MS WIDE

/GO LOOK FOR INDEX

/INCREMENT AND TEST INDEX PASS COUNT

/THIS WAS 1ST INDEX, GO LOOK FOR SECOND

/THIS WAS 2ND INDEX, WAS THE WINDOW OPEN?

/NO, INDEX OCCURRED TOO SOON

/YES, INDEX OCCURRED BETWEEN 150 AND 100 MB, INCREMENT
/RETURN ADDRESS BY 2

/SET DRV RDY BIT OF STAT IN SR

/FLAG OFF TO INDICATE FIRST PASS

/END AROUND SHIFT OF THE NEXT 3 BITS OF STAT IN SR

```

2560 2752 2764 EXCHRY
2561 2753 0140 BR WRTER F
2562 2754 2760 +4
2563 2755 0074 ROTATE ZERO
2564 2756 0226 JUMP FS
2565 2757 2761 +2
2566 2760 0076 ROTATE ONE
2567 2761 0062 FLAG ON
2568 2762 0226 JUMP FS
2569 2763 2736 ROT3
2570 2764 0064 EXCHRY, LSP
2571 2765 0274 OPEN RTN
2572 2766 0217 JUMP FS IND
2573 2767 0214 OPEN STAT
2574 2770 0071 ESP
2575 2771 0075 LSR
2576 2772 0074 ROTATE ZERO
2577 2773 0220 JUMP FS
2578 2774 2735 ROT3-1
2579 2775 0000 ?
2580 2776 0000 0
2581 2777 0000 0
2582 2778 0000 0
2583 2779 0000 0
2584 2780 0000 0
2585 2781 0000 0
2586 2782 0000 0
2587 2783 0000 0
2588 2784 0000 0
2589 2785 0000 0
2590 2786 0000 0
2591 2787 0000 0
2592 2788 0000 0
2593 2789 0000 0
2594 2790 0000 0
2595 2791 0000 0
2596 2792 0000 0
2597 2793 0000 0

```

/LAST, GO EXIT

/UPDATE WRITE PROTECT BIT OF STAT IN SR

/GO SHIFT AROUND LAST 3 BITS

/RESTORE THE STAT

/RETURN FROM CHKRDY SUBROUTINE

/CLEAR DRV READY BIT OF STAT IN SR

/GO UPDATE REST OF STAT IN SR

/OPEN

/OPEN

/OPEN

```

0000 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0100 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0200 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0300 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0400 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0500 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0600 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0700 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
1000 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
1100 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
1200 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
1300 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
1400 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
1500 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
1600 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
1700 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
2000 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
2100 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
2200 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
2300 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
2400 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
2500 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
2600 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
2700 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
3000
3100
3200
3300
3400
3500
3600
3700

```

```

4000
4100
4200
4300
4400
4500
4600
4700
5000
5100
5200
5300
5400
5500
5600
5700
6000
6100
6200
6300
6400
6500
6600
6700
7000
7100
7200
7300
7400
7500
7600
7700

```

A 0562
 ABACK 0535
 ABV43 0344
 AGAIN 0531
 AGAIN1 0550
 AGAIN2 0722
 AGAIN3 1576
 AGAIN4 1616
 AGAIN5 1635
 AGAIN6 1653
 B 0564
 BACK 2322
 BADDAM 2577
 BADHDR 2557
 BADSRT 1673
 RBACK 0554
 BDSRT 2555
 BOOT 0252
 BYTEOU 1152
 C 0615
 CBACK 0576
 CEGATE 0676
 CFINSE 0351
 CHKPAR 2041
 CHKRDY 2640
 CHKSEC 0730
 CKHCRC 2515
 CKHOME 2105
 CLRID 1243
 CNGATE 0666
 D 0653
 DAM 1675
 DAMSUP 0460
 DATA 2206
 DATAA 0571
 DBACK 0646
 DCR CER 2304
 DELAY 1300
 DELDAT 1727
 DIF 2462
 DIFA 2503
 DIFB 2501
 DLY25 2145
 DNRCAL 2625
 DONDLY 2165
 DONSTP 2135
 DUNSTP 0305
 E 0627
 EMPTY1 1210
 EMPTYB 1107
 ENDDAM 1742
 ERDONE 1000

ERTRK 0242
 EXCHRY 2764
 FILL1 1175
 FILLBU 1110
 FINDHD 1400
 FINDSE 0714
 FINDTR 0103
 FUNCT 1036
 FUNCT2 1057
 FUNCT4 1066
 FUNCT6 1076
 GETCMD 2001
 GETCRC 2221
 GETDAM 1441
 GETMRD 2000
 GLESSF 2432
 GODONE 0712
 GODUN 1272
 GOERDN 2610
 GOREAD 0770
 GOTIT 2010
 GOTONE 2030
 GOTRUN 2347
 GOTWRD 2076
 HCR CER 2546
 HDRCOM 1571
 HDSETL 0322
 HLPDLY 0466
 HMERR 2456
 ILTRK 0206
 INI0 0045
 INTER1 1374
 INTRDY 2631
 LOOP 1326
 MAGCOM 2400
 MOREOS 1421
 NEWORD 1141
 NEWPAS 2646
 NEXTG 2421
 NODAM 2606
 NOSTPS 0357
 NOTYET 1755
 NOZERO 1746
 NUTHER 2034
 NXDRV0 0064
 NXDRV1 0070
 NXHDR 0737
 NXIDAM 1761
 NAPRAM 1751
 OKDONE 1006
 OUT 2150
 PDNRCL 0372

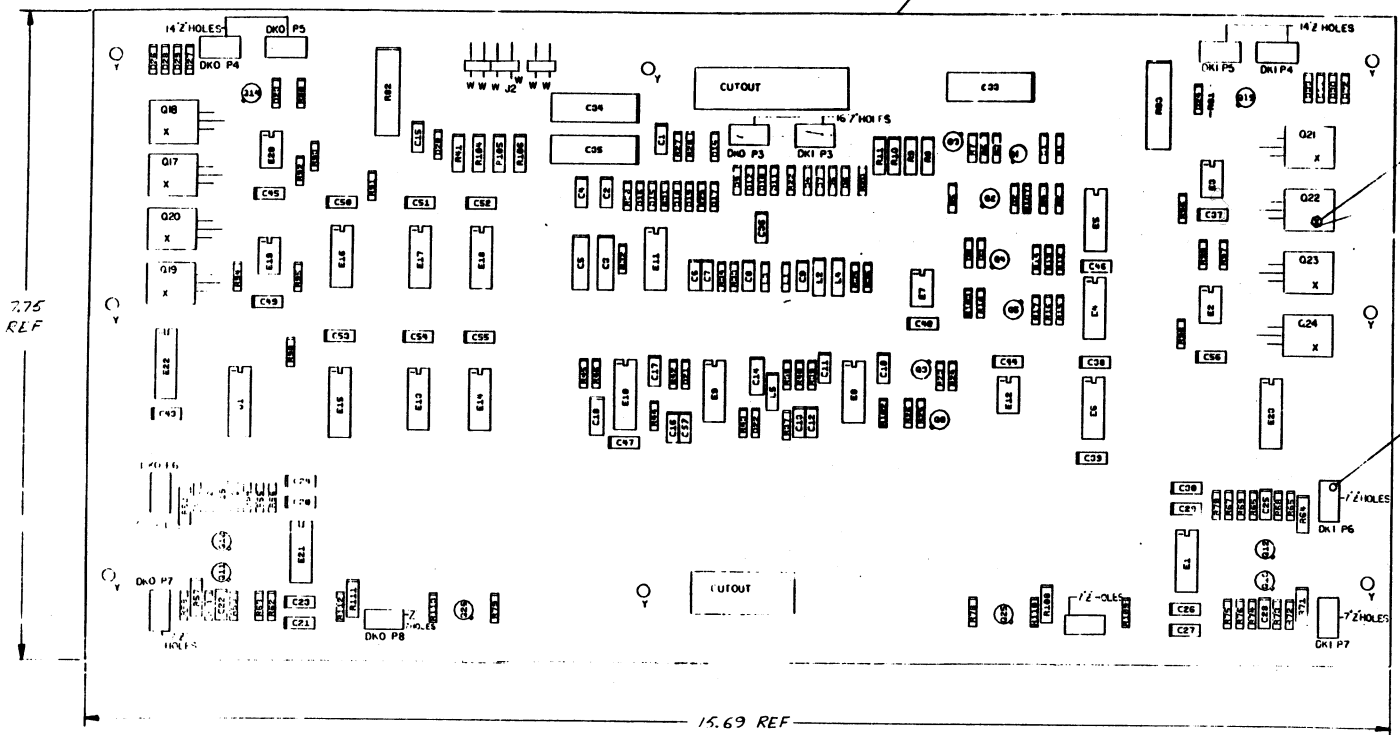
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 WRONG 2621
 WRT08 1322
 WRTCRC 0624
 WRTDAM 0514
 WRTPST 0506
 WRTSEC 0400
 XPRQ 1131
 XSTRY8 2573

PFUNCT 0370
 PGETDA 2617
 PGOIT 1346
 PNORDY 1771
 PNTRDY 1765
 PRDSEC 1105
 PRTERP 0503
 PTRYAG 2615
 PUTSEC 0145
 PUTTRY 0166
 PYSRDY 1767
 RCALOK 0060
 RDEREG 1275
 RDSEC 0760
 RDSTAT 1224
 READ 2167
 READOK 0706
 RECAL0 0035
 RECAL1 0034
 RFINTR 0355
 ROT 1251
 ROT3 2736
 SAWIND 2714
 SECHLF 0543
 SECPLS 2124
 SELFER 0620
 SPBACK 2662
 STASH 0437
 STDLY 2654
 STDONE 1031
 STEPHD 2100
 STPOUT 0275
 SWGATF 0407
 TEST 2352
 TEST1 1351
 TEST2 1350
 TESTDN 1372
 TIMERR 1667
 TKSKEP 2542
 TRKE0 0246
 TRYAGN 1413
 TSTAGN 1353
 TSTG0 2443
 TSTRT0 0004
 UDIF 0134
 UNRDY 2767
 UONE 0120
 USAME 0141
 UZERO 0127
 WAIT 0743
 WAITRN 2312
 WATDAT 2021

ERRORS DETECTED: 0
 LINKS GENERATED: 0
 RUN-TIME: 18 SECONDS
 3K CORE USED

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- NOTES:**
- UNLESS OTHERWISE SPECIFIED:
A ALL RESISTORS ARE 1/8W, ±5%
 - WASHER TO BE USED BETWEEN ITEMS 57 AND 58 WILL BE SUPPLIED WITH THE D41CB TRANSISTOR ONLY BY G.E.. THE WASHER IS ONLY REQUIRED WHEN USING THE G.E. TYPE TRANSISTOR.



57
58
SEE NOTE 2

55

IC TYPE	QTY	REF. DESIGNATION	DESCRIPTION
7475	4		
7415	4	B	
74157	4	A	
74122	4		
74123	8	E	
IC TYPE	GND	+5V	

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPT AS STATED ABOVE

IC PIN LOCATIONS

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.																
PARTS LIST																				
FIRST USED ON: M7727																				
ETCH BOARD REV: E																				
<table border="1"> <tr> <td>DATE</td> <td>12/31/74</td> </tr> <tr> <td>CHKD.</td> <td>[Signature]</td> </tr> <tr> <td>DATE</td> <td>1/10/75</td> </tr> <tr> <td>CHKD.</td> <td>[Signature]</td> </tr> <tr> <td>DATE</td> <td>1-14-75</td> </tr> <tr> <td>CHKD.</td> <td>[Signature]</td> </tr> <tr> <td>DATE</td> <td>1-14-75</td> </tr> <tr> <td>CHKD.</td> <td>[Signature]</td> </tr> </table>					DATE	12/31/74	CHKD.	[Signature]	DATE	1/10/75	CHKD.	[Signature]	DATE	1-14-75	CHKD.	[Signature]	DATE	1-14-75	CHKD.	[Signature]
DATE	12/31/74																			
CHKD.	[Signature]																			
DATE	1/10/75																			
CHKD.	[Signature]																			
DATE	1-14-75																			
CHKD.	[Signature]																			
DATE	1-14-75																			
CHKD.	[Signature]																			
TITLE: READ/WRITE CONTROL																				
NEXT HIGHER ARMY: [Signature]																				
DEC NO.	EIA NO.	DEC NO.	EIA NO.	SCALE: 1 OF 6																
SEMICONDUCTOR CONVERSION CHART																				
SHEET 1 OF 6																				
SERIAL CODE: DCSM7727-0-1																				
DIST. C																				

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1-0-222LWS 2

PARTS LIST

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	QTY
		X-Y COORDINATE HOLE LOCATION	K-00-M7727-0-4	1
		ASSY/ DRILL HOLE LAYOUT	D-M-M7727-0-5	2
		MODULE ECO HISTOY	B-M-M7727-0-6	3
1		ETCHED CIRCUIT BOARD	D-1A-501570-00	4
2	C17, C18	CAP 100 pF	1000016-00	5
1	C9	CAP 180 pF	1000020-00	6
2	C8, C14	CAP 220 pF	1000021-00	7
32	C1, C2, C4, C10, C11, C15, C16, C20, C21, C23, C24, C26, C27, C29, C30, C37, C38, C39, C40, C42, C44, C45, C46, C47, C49-C57	CAP .0.1 uF	1001610-00	8
2	C3, C5	CAP 6.8 uF 35V	1005306-00	9
2	C34, C35	CAP 190 uF	1009433-00	10
1	C38	CAP 50 uF	1000080-00	11
7	C7, C6, C12, C13	CAP .047 uF	1010978-32	12
5	C19, C25, C26, C28, C36	CAP .005 uF	1001765-00	13
10	D4, D7, D9, D12, D14, D15, D16, D17, D18, D19	DIODE D671	1103309-00	14
8	D3, D5, D8, D9, D10, D11, D21, D22	DIODE 1N472	1105275-00	15
10	D23, D24, D26, D27, D28, D29, D30, D31, D32, D33	DIODE 1N4004	1105796-00	16
1	D20	DIODE 1N4742 12V	1109502-00	17
2	D1, D2	DIODE 5.1V	110713-00	18
9	R90, R92 - E99	RES 150 1/4W 5%	1300250-00	19
1	R41, R04, R105, R06	RES 680 1/2W 5%	1300347-00	20
12	R6, R14, R17, R23, R24, R26, R26, R28, R29, R30, R34, R34	RES 1K 1/4W 5%	1300365-00	21
4	R2 - R11	RES 1.2K 1/2W 5%	1300385-00	22
6	R22, R27, R42, R42, R44, R44	RES 68 1/2W 5%	1309405-00	23
7	R12, R16, R23, R23, R25, R25, R25, R25, R102	RES 1.5K 1/4W 5%	1300391-00	24
4	R5, R26, R39, R40	RES 51 1/8W 1%	1302411-00	25
1	R5	RES 2.7K 1/8W 1%	1304868-00	26
11	R3, R4, R7, R12, R15, R18, R18, R25, R27, R42, L92	RES 3.3K 1/4W 5%	1300439-00	27
6	R1, R2, R22, R24, R45, R107	RES 1 1/2W 5%	1300479-00	28
11	R3, R37, R38, R52, R58, R62, R66, R72, R76, R109, R112	RES 1.2K 1/4W 1%	1302871-00	29
1	R32	RES 196 1/8W 1%	1302956-00	30
2	R33, R34	RES 464 1/8W 1%	1303047-00	31
2	R28, R29	RES 34.8K 1/4W 1%	1303156-00	32
4	R51, R61, R65, R73	RES 1.2K 1/8W 1%	130332-00	33
2	R82, R83	RES 100 5/8W 5%	1309094-00	34
2	R30, R31	RES 196K 1/8W 1%	1309699-00	35
6	R55, R59, R67, R74, R110, R113	RES 4.69K 1/4W 1%	1304856-00	36

PARTS LIST

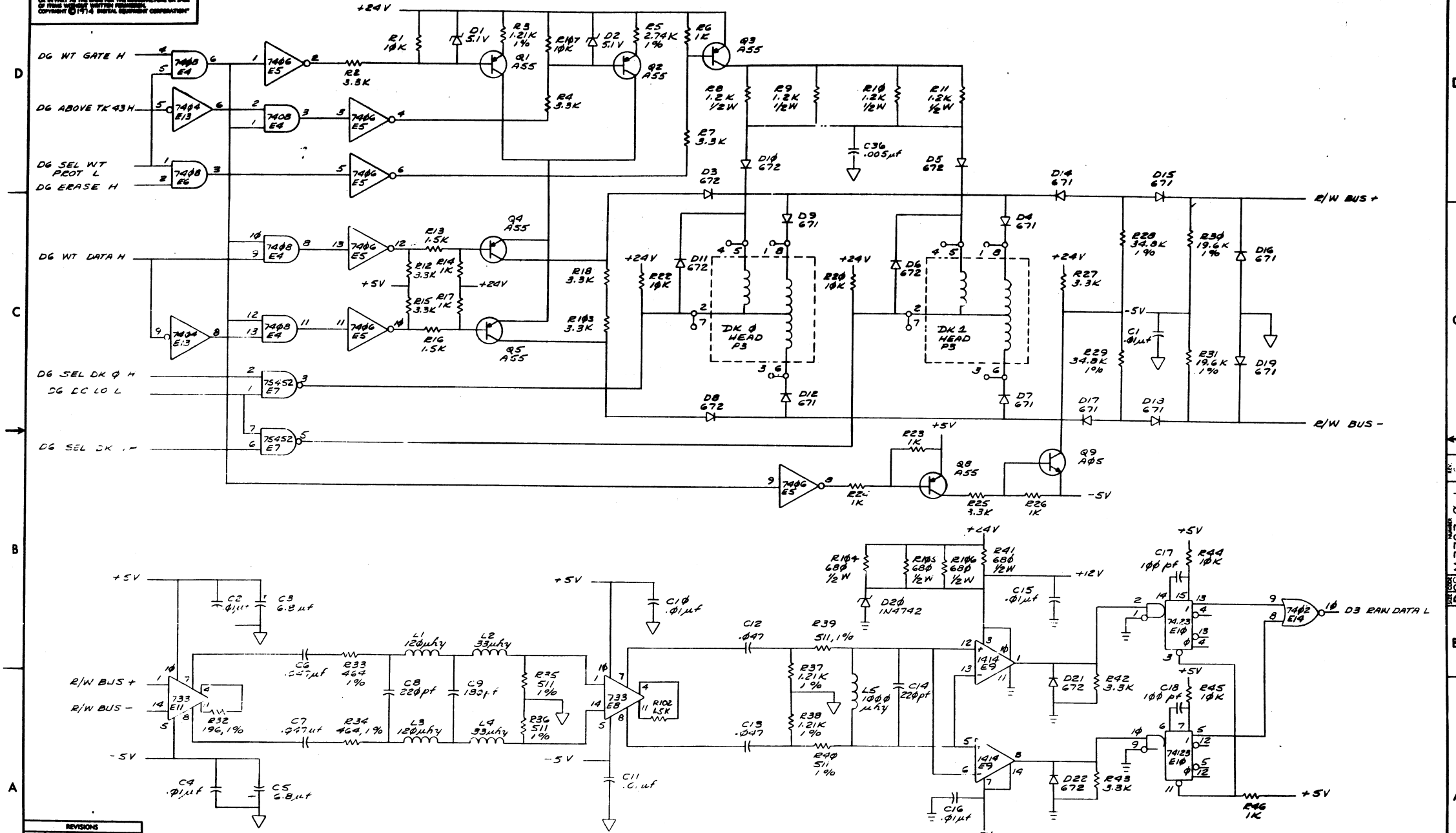
QTY	REF DESIGNATION	DESCRIPTION	PART NO.	QTY
1	L5	CHOKE 1000 MHY	1602763-00	37
2	L2, L4	CHOKE 33 MHY	1601759-00	38
2	L1, L3	CHOKE 120 MHY	1610163-00	39
1	E17	I.C. 7450	1905549-00	40
2	E16, E18	I.C. 7412	1905597-00	41
1	E14	I.C. 7402	1909039-00	42
1	E13	I.C. 7404	1909624-00	43
2	E4, E6	I.C. 7403	1909858-00	44
3	E1, E9, E21	I.C. 1414	1909858-00	45
5	E2, E3, E12, E19, E20	I.C. 74451	1910436-00	46
1	E10	I.C. 74123	1910436-00	47
2	E8, E11	I.C. 72733	1910648-00	48
1	E15	I.C. 74157	1910655-00	49
1	E5	I.C. 7412	191074-00	50
1	J1	I.C. SOCKET 16 PIN	1910858-00	51
9	Q9 THRU Q15, Q25, Q26	TRANS MIXAROS	1910105-00	52
8	Q1 - Q5, Q8	TRANS MIXAROS	1910106-00	53
8	Q17 - Q24	TRANS D44C8	1910421-00	54
86	Z HOLES	WIRE WRAP PIN	1910385-01	55
3	J2	CONN 2 POS	1912204-00	56
8	"X" HOLES	SCREW, PAN HD 4/40 X 5/16	1900610-01	57
8	"X" HOLES	NUT, KEP 4/40 X 1/4 X 3/16	1900657-00	58
1	E7	I.C. 75452	1910645-00	59
4	R54, R56, R69, R70	RES 14.7K 1/4W 1%	1902941-00	60

REVISIONS		
CHK	CHANGE NO	REV

TITLE	READ/WRITE CONTROL	SIZE CODE	D CS M7727-0-1	NUMBER		REV.	C
SCALE		SHEET	2	OF	6	DIST.	

DCS M7727-0-1 C

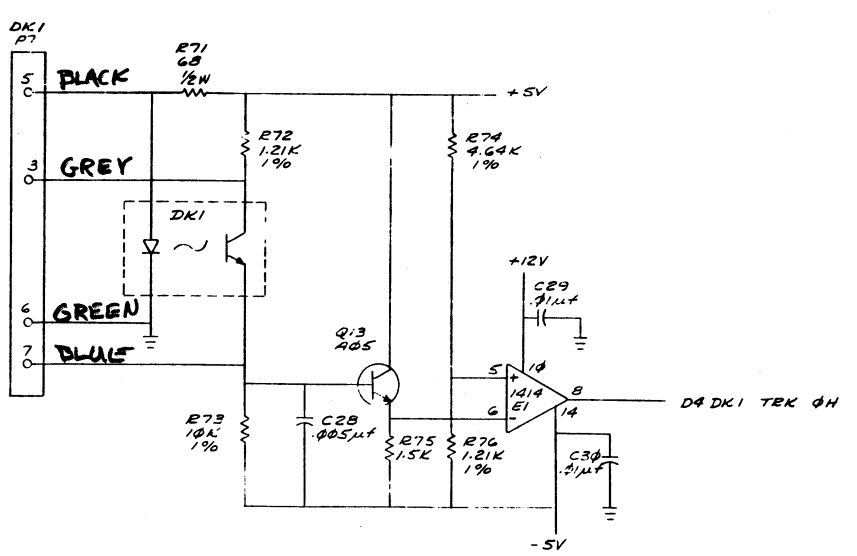
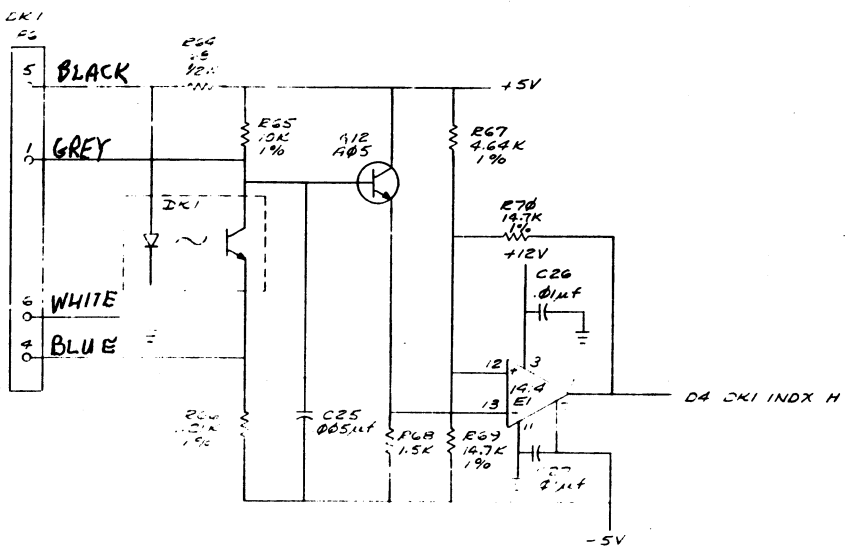
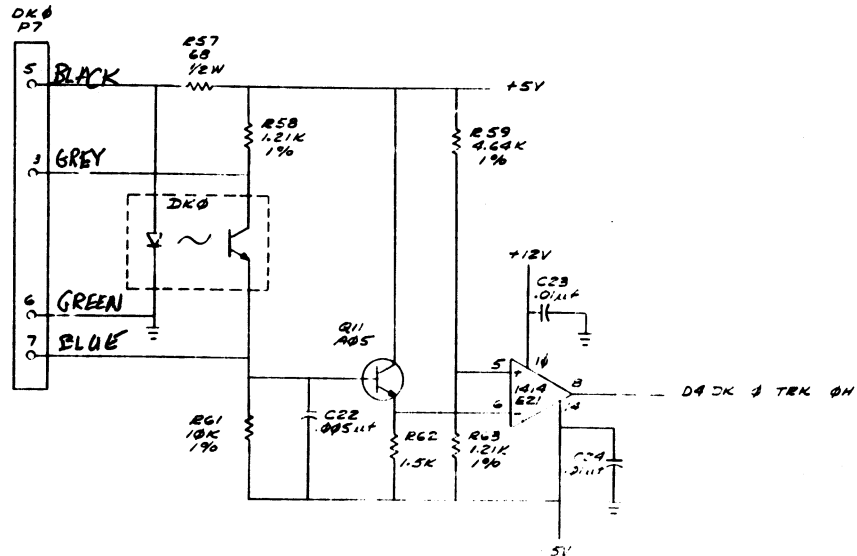
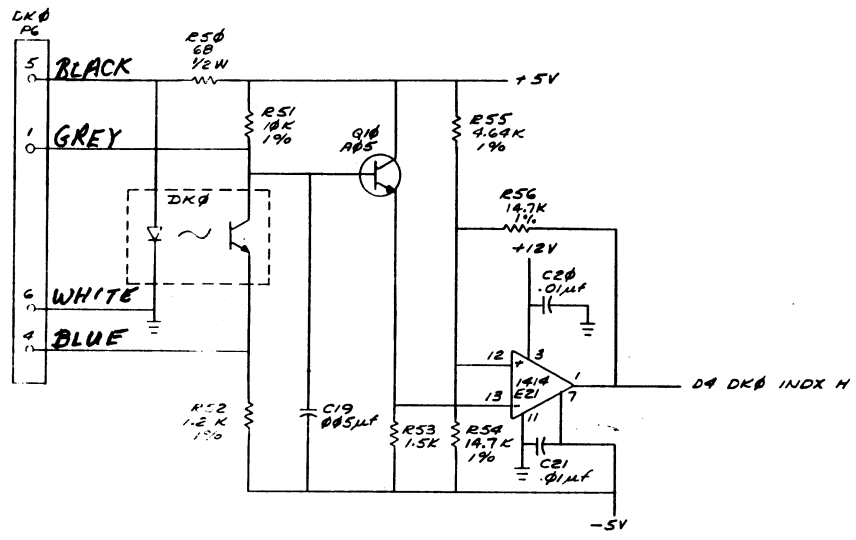
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CHK	CHANGE NO.	REV.

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DCS M7727-0-1

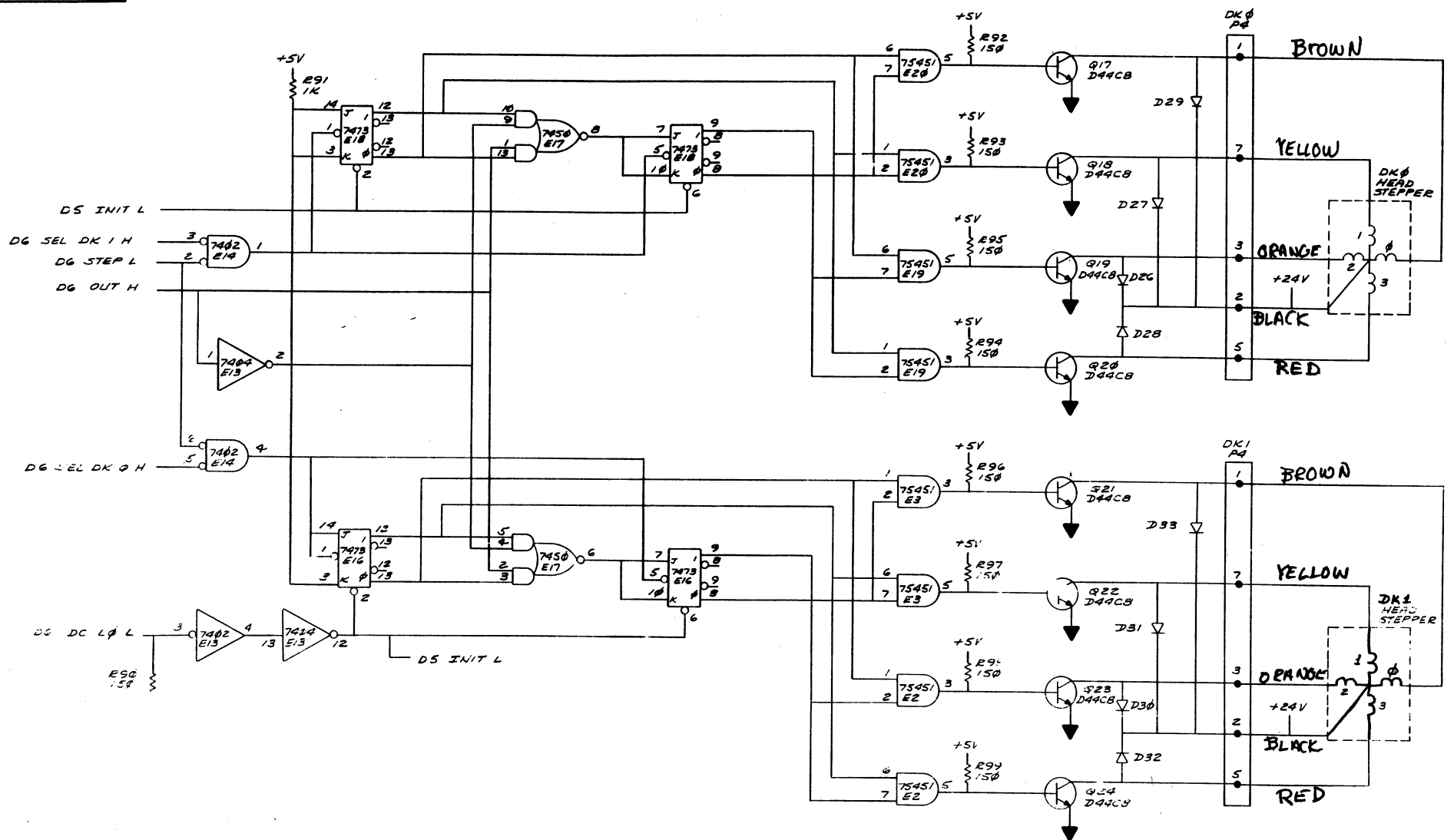


REVISIONS		
CHK	CHANGE NO.	REV.

TITLE READ / WRITE CONTROL (D4) DCS M7727-0-1
 SCALE 1:1 SHEET 4 OF 6

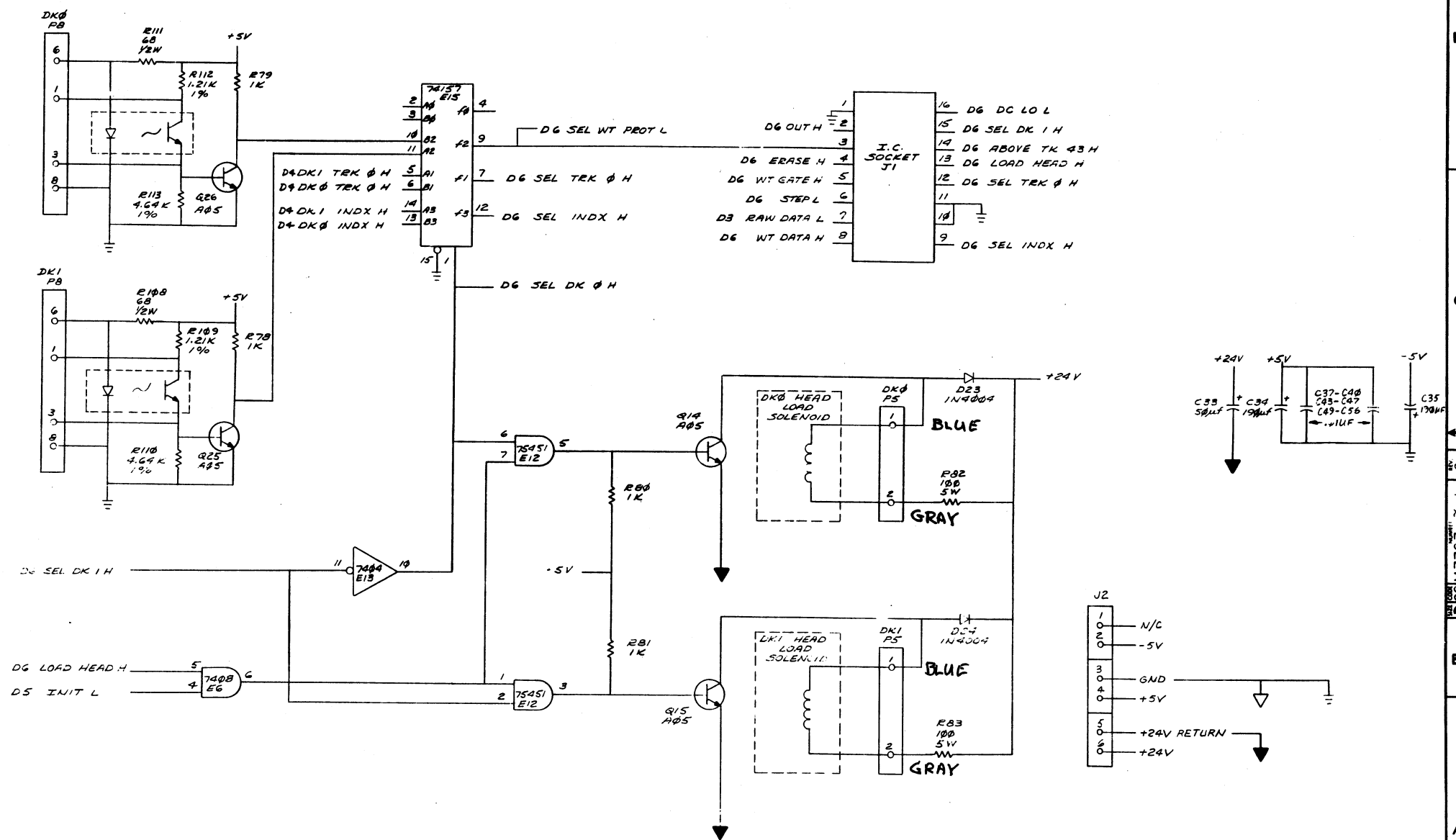
DCS M7727-0-1

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REVISIONS		
CHK	CHANGE NO.	REV.

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REVISIONS		
CHK	CHANGE NO.	REV.

DCS M7727-Ø-1 C

CUSTOMER PRINT SET INDEX

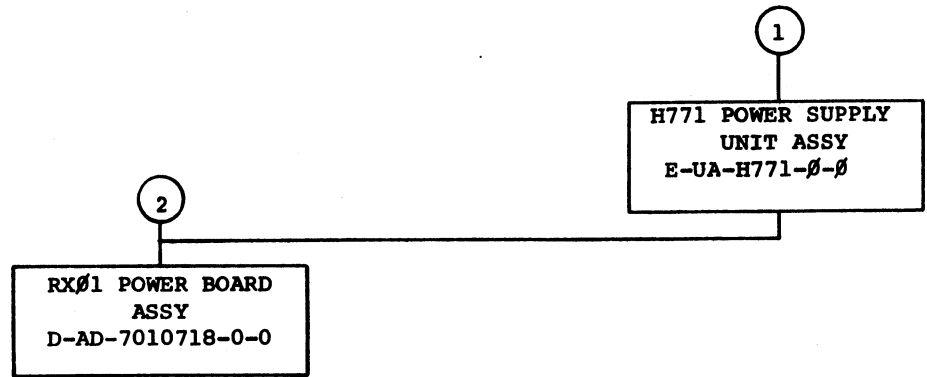
THIS IS PRINT SET

<p>H771 POWER SUPPLY H771-A CIRCUIT SCHEMATIC H771-C CIRCUIT SCHEMATIC H771-D CIRCUIT SCHEMATIC RXØ1 POWER BOARD ASSY RXØ1 POWER SUPPLY BOARD</p>	<p style="text-align: center;">SEQUENCE</p> <p>B-DD-H771-Ø D-CS-H771-A-1 D-CS-H771-C-1 D-CS-H771-D-1 D-AD-7010718-0-0 D-CS-5411398-0-1</p>
---	--

UNIT VARIATIONS		PRINT SET		
VAR	TITLE	1	2	3
H771-A	RXØ1 POWER SUPPLY, 115V, 6ØHZ	X		
H771-C	RXØ1 POWER SUPPLY, LOW VOLT, 5ØHZ	X		
H771-D	RXØ1 POWER SUPPLY, HIGH V, 5ØHZ	X		

REVISIONS		REV
DATE	CHG. NO.	
7-75	H771-1	A
10-75	H771-2	B
11-75	H771-3	C
3-76	H771-4	D

USED ON OPTION/MODEL	DRN. W. McCarthy	DATE 2/3/75	TITLE H771 POWER SUPPLY	
RXØ1	CHK'D. W.F.M. Ca. they	DATE 6/13/75		
	PROJ. ENG. G. Callahan	DATE 6/13/75		
	PROD. J. Miller	DATE 6/13/75	SIZE B	CODE DD
	FIELD SERV.	DATE 6/13/75	NUMBER H771-Ø	
SHEET 1 OF 3			REV D	



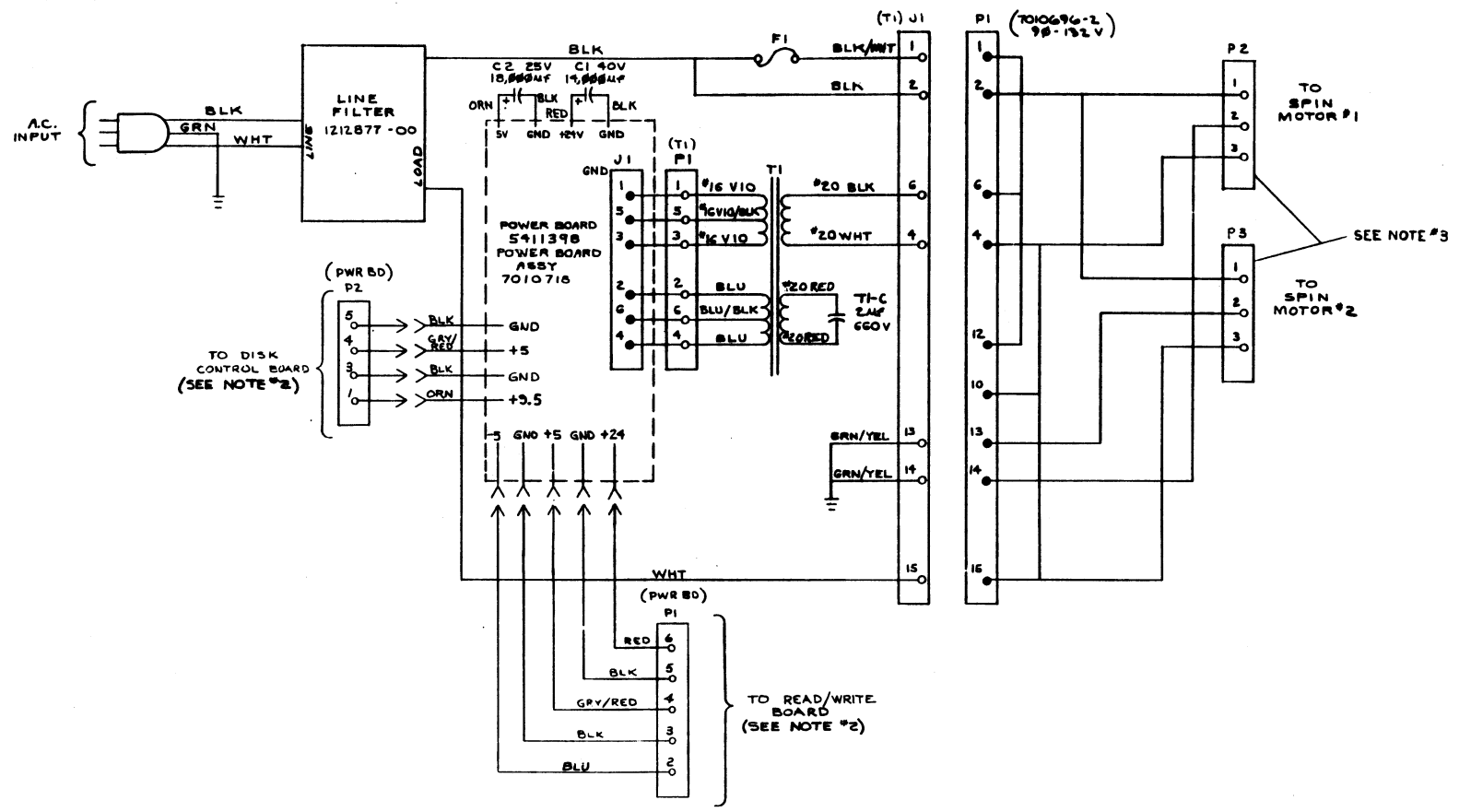
TITLE	SHEET 2 OF 3	SIZE CODE	NUMBER	REV
H771 POWER SUPPLY		B DD	H771-Ø	D

CUSTOMER PRINT SET				MECHANICAL					CUSTOMER PRINT SET				ELECTRICAL						
1	2	3	4	MFG. SET FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE	1	2	3	4	MFG. SET FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
				1	E-UA-H771- β - β	D	2	H771 POWER SUPPLY ASSY		X				1	B-DD-H771- β	D	3	H771 POWER SUPPLY	
					E-MD-7412667-0-0	D	1	CHASSIS, POWER SUPPLY		X					D-CS-H771-A-1	B	1	H771-A CIRCUIT SCHEMATIC	
					D-AD-7010680-0-0	C	1	TRANSFORMER ASSY, 60 HZ		X					D-CS-H771-C-1	C	1	H771-C CIRCUIT SCHEMATIC	
					D-AD-7010704-0-0	E	1	TRANSFORMER ASSY, 50 HZ		X					D-CS-H771-D-1	C	1	H771-D CIRCUIT SCHEMATIC	
					C-AD-7010697-0-0	B	1	POWER CORD ASSY							A-SP-H771- β -1			ENGINEERING SPECIFICATION	
					C-IA-7010972-0-0	C	1	JUMPER											
					C-MD-7413344-0-0		1	BRACKET, FUSE MOUNTING											
					A-DC-7413403-0-0		1	DECAL, H771-A											
					A-DC-7414250-0-0	A	1	DECAL, H771-C											
					A-DC-7414251-0-0	A	1	DECAL, H771-D											
				2	D-AD-7010718-0-0		1	RX01 POWER BOARD ASSY						2	D-AD-7010718-0-0	*	1	RX01 POWER BOARD ASSY	
					D-IA-7010854-0-0	C	1	READ/WRITE BOARD HARNESS		X					D-CS-5411398-0-1	*	1	RX01 POWER BOARD ASSY	
					D-IA-7010853-0-0	B	1	DISK CONTROL BOARD HARNESS		X									

CUSTOMER PRINT SET CODES	X = PRINT OF DOCUMENT INCLUDED IN PRINT SET	TITLE	SIZE	CODE	NUMBER	REV
	C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT					
	S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED					

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- NOTES:
1. ALL WIRE TO BE #18 AWG UNLESS OTHERWISE SPECIFIED.
 2. SLOT BETWEEN P1-4 + P1-5 CONTAINS A DUMMY PIN. SLOT BETWEEN P2-4 + P2-5 ALSO CONTAINS A DUMMY PIN.
 3. NO DOUBLE CRIMPS ARE ALLOWED IN MOLEX CONNECTOR(S) TO MOTOR(S).



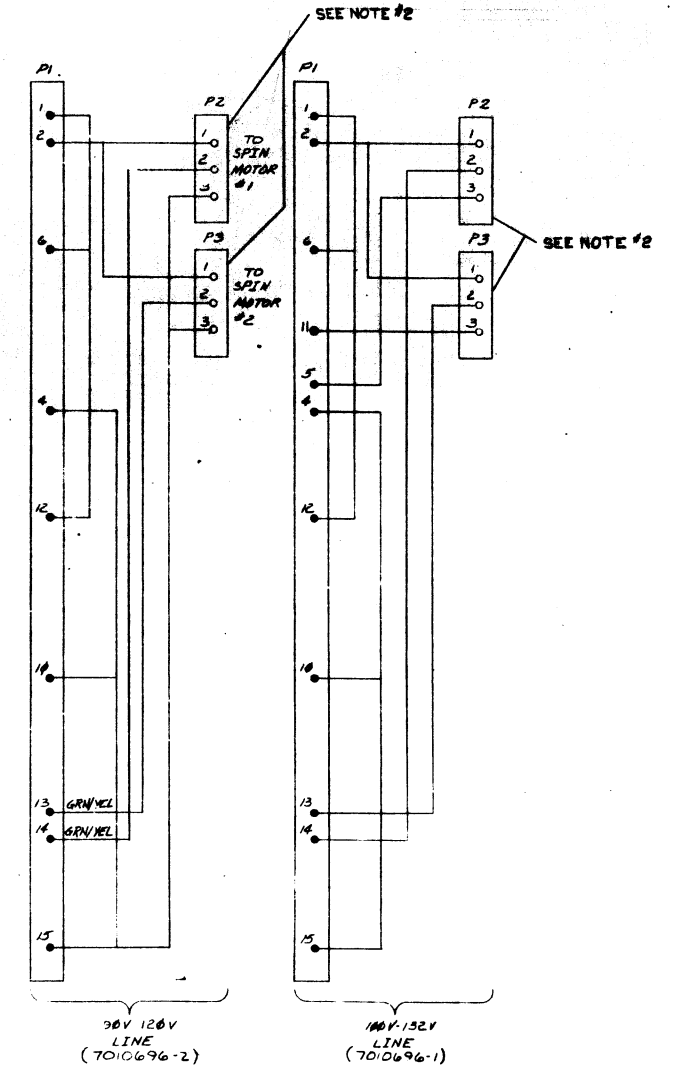
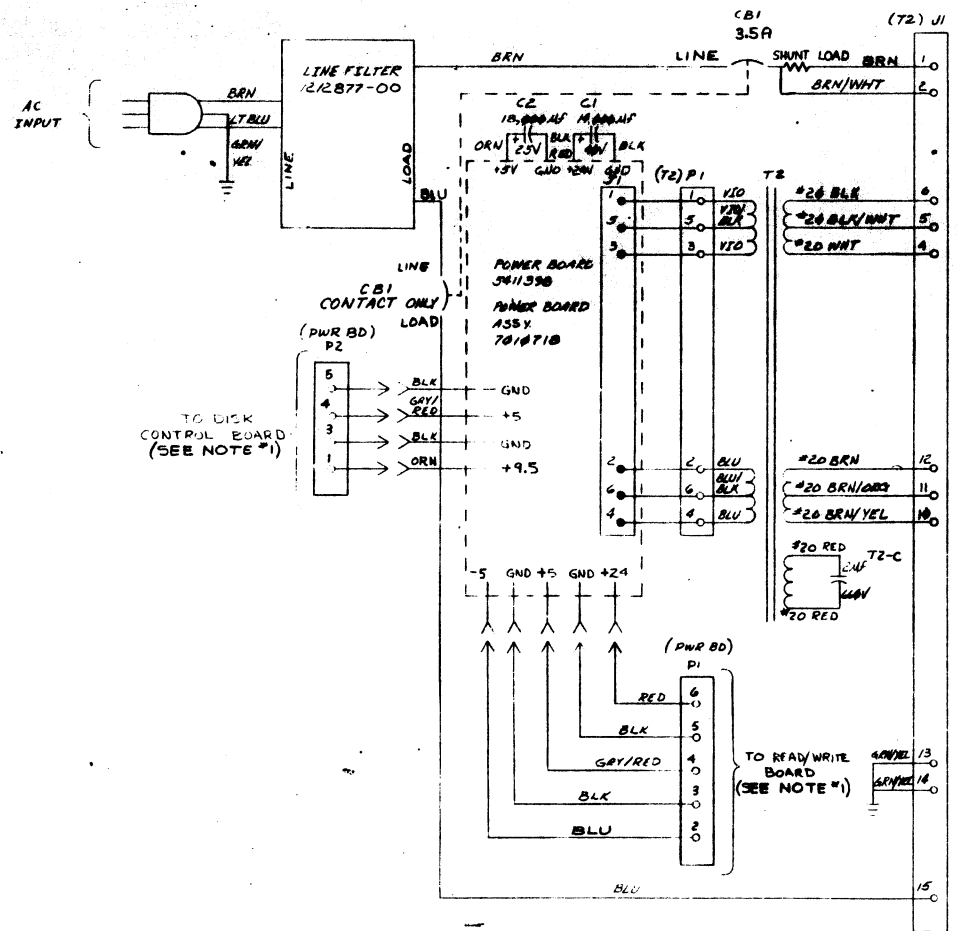
D
C
B
A

D
C
B
A

REV.	DATE	BY	CHK'D
1	11-18-75	W. HAZEN	
2	12-11-75	W. HAZEN	
3	1-14-76	W. HAZEN	
4	3-11-76	W. HAZEN	
5	3-11-76	W. HAZEN	

DRN. <i>D.E. Olson</i>	1/2/76	FIRST USED ON	RX01
CHK'D <i>W.F. Olson</i>	3/1/76	TITLE	H771A POWER CONNECTIONS
ENG. <i>D.W. Olson</i>	3-11-76	SCALE	NONE
PROD. <i>D.W. Olson</i>	3-11-76	SHEET	1 OF 1
NEXT HIGHER ASSY.		SIZE	D CS
3-DD-4771-0		NUMBER	H771-A-1
		REV.	B

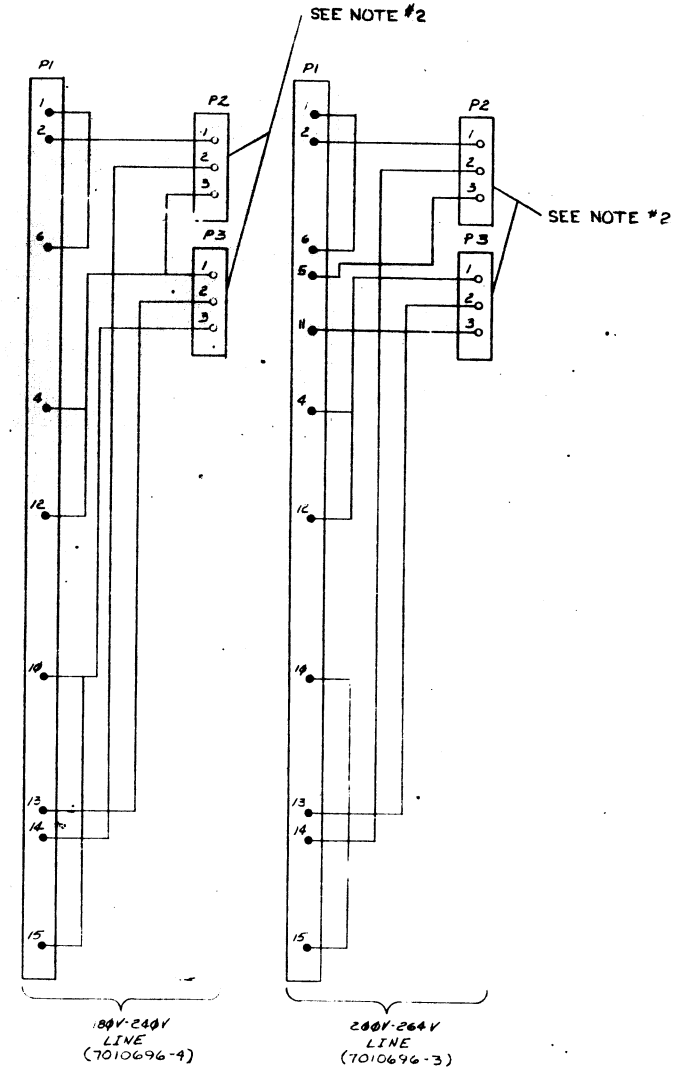
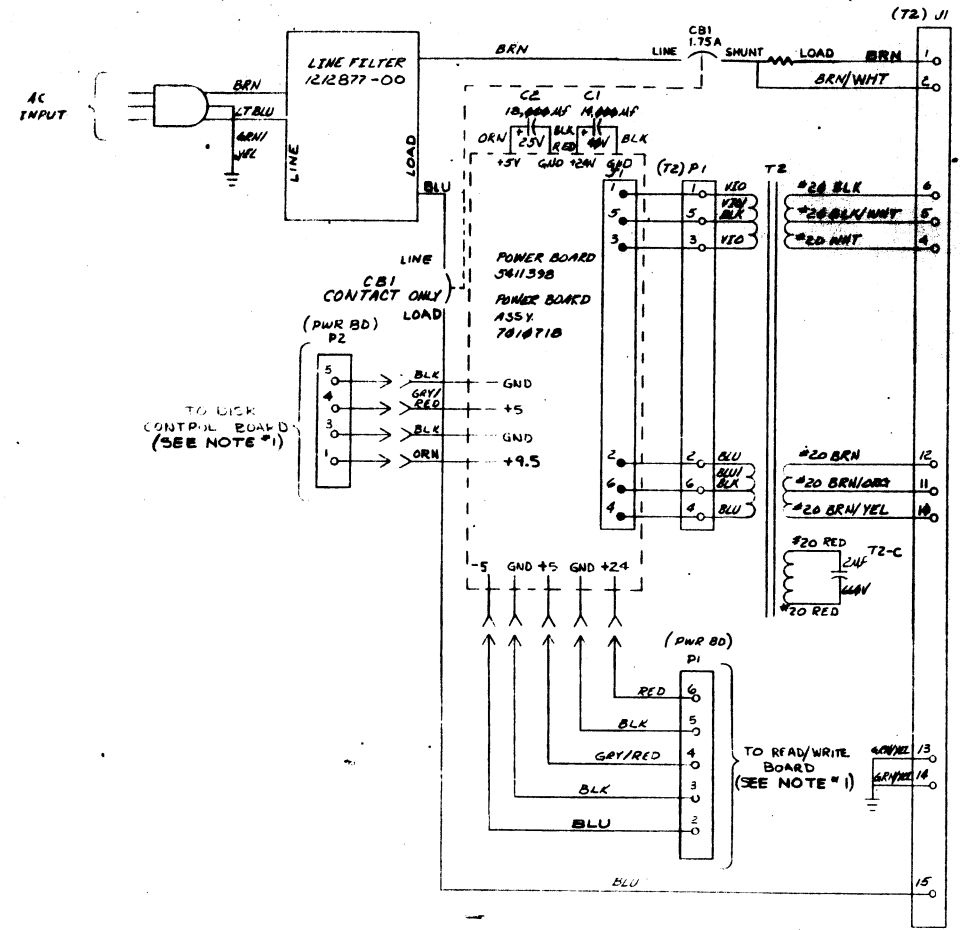
- NOTES:**
- 1. SLOT BETWEEN P1-4 AND P1-5 CONTAINS A DUMMY PIN. SLOT BETWEEN P2-4 AND P2-5 ALSO CONTAINS A DUMMY PIN.
 - 2. NO DOUBLE CRIMPS ALLOWED IN MOLEY CONNECTOR(S) TO MOTOR(S).
 - 3. ALL WIRES TO BE #18AWG UNLESS OTHERWISE SPECIFIED.



REV	1	DATE	BY
REV	2	DATE	BY
REV	3	DATE	BY
REV	4	DATE	BY
REV	5	DATE	BY
REV	6	DATE	BY
REV	7	DATE	BY
REV	8	DATE	BY
REV	9	DATE	BY
REV	10	DATE	BY

DRN	FIRST USED ON	800000
CHK	RX01	
ENG	TITLE	
PROJ ENG	H771-C POWER CONNECTIONS	
PROD		
NEXT HIGHER ASSY		
B-00	SIZE CODE	D CS
SCALE	H771-C	C
SHEET 1 OF 1	DIST.	

- NOTES:
1. SLOT BETWEEN PI-4 AND PI-5 CONTAINS A DUMMY PIN, SLOT BETWEEN P2-4 AND P2-5 ALSO CONTAINS A DUMMY PIN.
 2. NO DOUBLE CRIMPS ALLOWED IN MOLEX CONNECTOR(S) TO MOTOR(S).
 3. ALL WIRES TO BE #18AWG UNLESS OTHERWISE SPECIFIED.



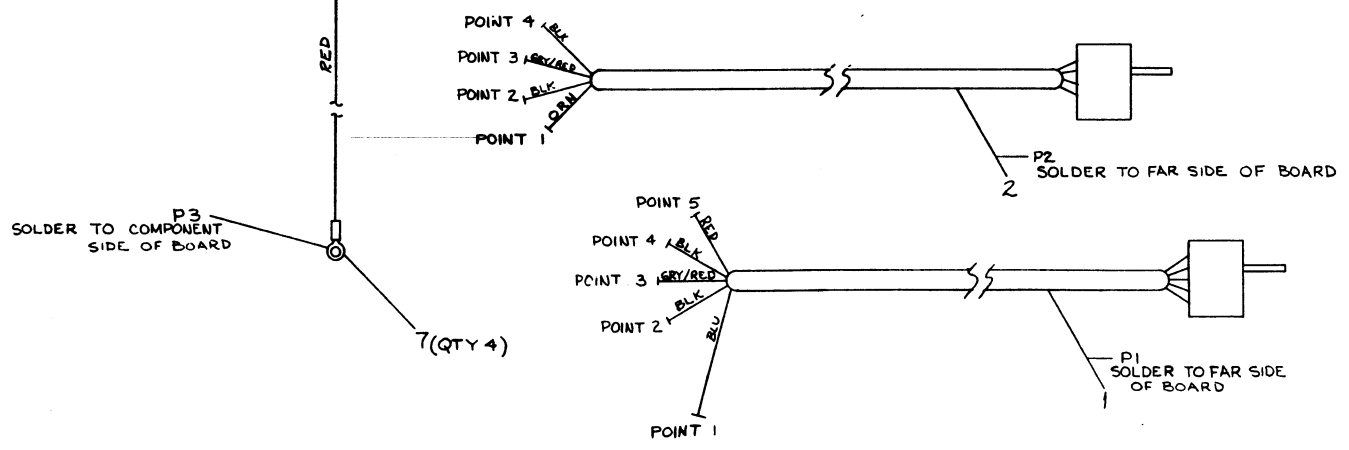
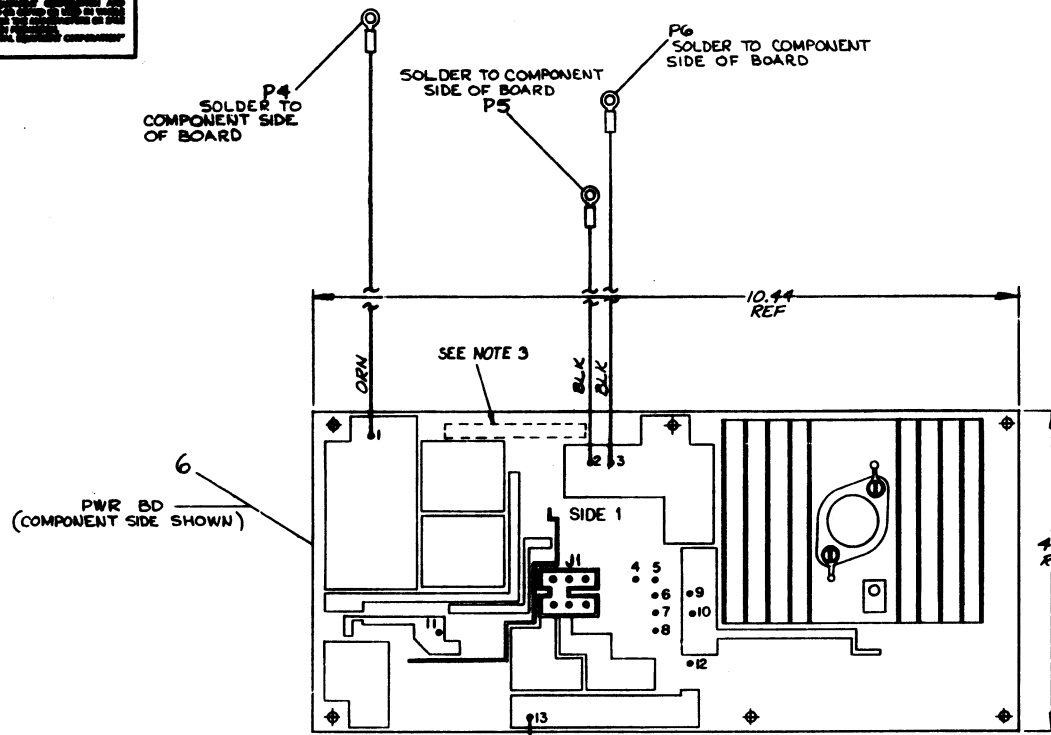
REV.	+
ENTR-00001	+
ORIGINATED	A
H771-00002	A
BY	W
DATE	11-17-73
BY	B
DATE	11-17-73
BY	C
DATE	11-17-73
BY	D
DATE	11-17-73
BY	E
DATE	11-17-73

DRN	7-31-73	FILED ON	200000
CHK'D	8-5-73	TITLE	RX01
ENG.	8-12-73	FILE	H771-D POWER CONNECTIONS
PROJ.	8-12-73	SCALE	D
NEXT HIGH# ASBY.		SHEET	1 OF 1
B-00-H771-D			

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WIRE TABLE						
ITEM NO.	AWG	COLOR	FROM		TO	
			CONN	TERM	CONN	TERM
1	18	BLU	P1	POINT 1	PWR BD #11	SOLDER
		BLK	P1	POINT 2	PWR BD #6	
		GRY/RED	P1	POINT 3	PWR BD #9	
		BLK	P1	POINT 4	PWR BD #5	
		RED	P1	POINT 5	PWR BD #12	
2		ORN	P2	POINT 1	PWR BD #4	
		BLK	P2	POINT 2	PWR BD #7	
		GRY/RED	P2	POINT 3	PWR BD #10	
	18	BLK	P2	POINT 4	PWR BD #8	
3	14	RED	P3	ITEM 7	PWR BD #13	13 IN ±.25
4	14	BLK	P5	ITEM 7	PWR BD #2	7 IN ±.25
5	14	ORN	P4	ITEM 7	PWR BD #1	11 IN ±.25
4	14	BLK	P6	ITEM 7	PWR BD #3	SOLDER 9 IN ±.25

- NOTES:
1. STRIP LENGTH FOR ITEMS 3, 4 & 5 ARE TO BE .16 LONG.
 2. THE BLACK WIRES ON P1 & P2 CAN BE INTERCHANGED BETWEEN POINTS 5, 6, 7, & 8 ON THE POWER BOARD.
 3. INK STAMP ASS'Y NO. 7010718 IN FIGURES, 13 HIGH WHERE SHOWN.



QTY	DESCRIPTION	DRAWN PART NO.	ITEM NO.
4	CONN, SOLDERLESS	9007928-00	7
1	POWER SUPPLY BOARD, RXØ1	0-05-541398-0-1	6
4	WIRE, #14 AWG, IPVC, ORANGE	9107370-33	5
4	WIRE, #14 AWG, IPVC, BLACK	9107370-00	4
4	WIRE, #14 AWG, IPVC, RED	9107370-22	3
1	HARNESS, DISK CONTROL BOARD	0-1A-7010853-0-0	2
1	HARNESS, READ/WRITE BOARD	0-1A-7010854-0-0	1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	
APPLIC. OF ACCURACY	FRAC. DEC. DIM. DIM. TOL. DIM. TOL. DIM. TOL. DIM. TOL. DIM. TOL.
SURFACE QUALITY	(CHECK ONE) <input type="checkbox"/> 1.0 <input type="checkbox"/> 2.0 <input type="checkbox"/> 3.0 <input type="checkbox"/> 4.0 <input type="checkbox"/> 5.0
QUANTITY & VARIATION	MEDIUM <input type="checkbox"/> DISPENSER <input type="checkbox"/> 1.00 2.00 3.00 4.00 5.00 10.00

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DIMS

MATERIAL SEE PARTS LIST

FINISH

DRN. *TOM* 1.2575

CHK'D. *[Signature]*

ENGR. *[Signature]*

PROJ. ENGR. *[Signature]*

PROD. *[Signature]*

FIRST USED ON: H771

TITLE: RXØ1 POWER BOARD ASS'Y

MATERIAL: E-UA-H771-0-0

SCALE: D AD 7010718-0-0

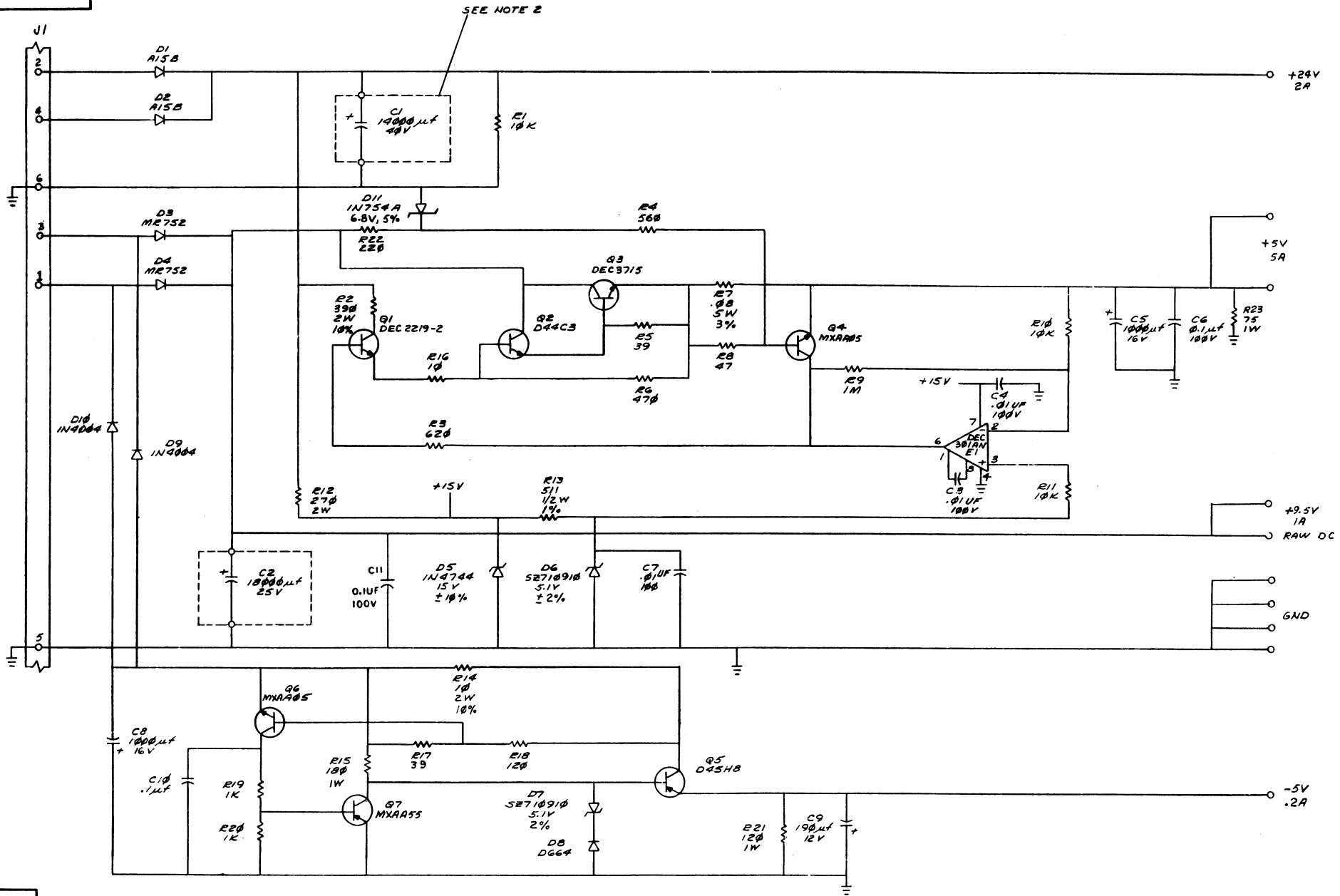
SHEET 1 OF 1

REV. B

REV.	DATE	BY	CHKD.	DESCRIPTION
A	07/12/72	[Signature]	[Signature]	ISSUED FOR PRODUCTION
B	02/07/73	[Signature]	[Signature]	REVISED TO ADD PARTS LIST

D AD 7010718-0-0

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REVISIONS		
CHK	CHANGE NO.	REV.

