CHAPTER 2
PC8-E HIGH-SPEED PAPER-TAPE READER/PUNCH

SECTION 1 INTRODUCTION

The PC8-E (or the desk-top model, PC8-EB) Reader/Punch option consists of a control module and a high-speed paper-tape reader/punch manufactured by DEC [Model PC04BL (60 Hz) or PC04BM (50 Hz)]. The control (DEC M840) plugs into the PDP-8/E OMNIBUS and connects to the external reader/punch via two signal cables that are supplied with the system.

The PC04 Reader/Punch is discussed here only to the extent necessary to fully describe control operation and present supplementary information concerning installation and checkout. Details concerning the installation, operation, troubleshooting, and maintenance of the reader/punch, itself, can be found in the *PC04/PC05 Paper-Tape Reader/Punch Maintenance Manual* [DEC-00-PC0A-D (1)]. Other publications and documents relevant to the PC8-E are:

a. *PDP-8/E & PDP-8/M Small Computer Handbook* — DEC, 1972
b. *PDP-8/E Maintenance Manual, Volume 1*
c. *Roytron Model 500 Maintenance Manual*
d. PC8-E Diagnostic, MAINDEC-8E-D2CA
e. DEC Engineering Drawing, Reader/Punch Control, E-CS-M840-0-1.

SECTION 2 INSTALLATION

The PC8-E Reader/Punch and Control is installed on site by DEC Field Service personnel. The customer should *not* attempt to unpack, inspect, install, checkout, or service the equipment.

Insert the PC8-E Control Module in the PDP-8/E OMNIBUS. Refer to Table 2-3, Volume 1, for information concerning recommended module priorities (the PC8-E is a "non-memory" option).

Connect the control to the reader/punch with the two signal cables provided. J1 of the control, a 40-pin Berg Connector, connects to reader/punch module slot B1, a DEC M955 Connector. J2 of the control connects to module slot A1 (refer to Section 5 for cable and connector pin assignments).

Refer to Chapter 2 of the *PC04 High-Speed Perforated Paper-Tape Reader/Punch Maintenance Manual* (DEC-00-HGPA-D) for additional information concerning system installation and for procedures to be followed to checkout both the control and the reader/punch.

SECTION 3 DESCRIPTION

Figure 2-1 is a block diagram of the PC8-E Control. The functions of the control can be grouped conveniently according to reader functions and punch functions, as illustrated by the block diagram. Consider the reader functions, represented by the logic blocks above the broken line.

The control logic generates signals that control the PC04 tape-feed operation. As the paper tape passes over the PC04 photoarray, signals representing the punched characters are strobed into the Control Buffer Register. The buffered information is then transferred to the PDP-8/E AC Register and operated on by subsequent program instructions.

The tape-feed operation can be initiated under program control or by activation of the Reader FEED switch on the PC04 front panel. If the switch is used, the tape feeds through the read station but data is not transferred from the Control Buffer Register. If data is to be transferred, the tape-feed operation must be program-initiated.

Two IOT instructions, 6014 (Fetch Reader Character) and 6016 (Read Buffer, Fetch Reader Character), read the information currently over the photoarray and then initiate tape feed. When either of these instructions is decoded by the IOT decoder logic, the read tape logic generates an ENABLE signal that triggers the clock logic. The first CLOCK PULSE produced enables the read tape logic to generate an RDR DATA STROBE pulse. This pulse clocks the RDR Buffer Register, loading the register with the information present on the READ HOLE 1–8 lines.

In addition to clocking the RDR Buffer Register, the RDR DATA STROBE signal sets the RDR FLAG flip-flop in the INT/skip logic and clears the RDR RUN flip-flops in the tape read logic. If the control has been logically connected to the computer interrupt system by a previous 6010 instruction, or by the INITIALIZE signal, the OMNIBUS INT RQST L signal is asserted. The computer enters the interrupt servicing routine to determine the identity of the requesting device. The 6011 instruction in the routine causes the computer to proceed to the PC8-E subroutine to service the interrupt request (refer to Table 2-1 for IOT instruction descriptions).

After producing the first CLOCK PULSE, the clock logic generates a SHIFT PULSE. This causes the motor control logic to provide stepping signals for the PC04 Reader Motor. The motor shaft turns, feeding the tape through the read station. After two steps, the next character on the tape appears over the photoarray; the current read operation is completed. If a new 6014 or 6016 instruction has been issued, another RDR DATA STROBE is generated and this character is loaded into the RDR Buffer Register. Each RDR DATA STROBE loads a character into the register. The register data is transferred to the CPU AC Register by the 6012 or 6016 instruction. If a 6014 or 6016 instruction is decoded between each RDR DATA STROBE and the next CLOCK PULSE, reader operation is continuous, at a rate of 300 characters/second. Otherwise, the character rate is limited to 25 characters/second.

The tape status logic monitors the FEED HOLE signal from the PC04. When the tape-read mechanism is out of tape, the tape status logic provides a signal that inhibits program generation of the motor stepping signals and clears the tape read logic.

Now consider the punch functions, represented by the logic blocks below the broken line in Figure 2-1. The punch motor operates continuously when power is applied to the PC04. The punch mechanism (Roytron Model 500) provides a PUNCH SYNC signal at the beginning of each punch mechanical cycle. This signal synchronizes the control timing and the rotating motor shaft. If a 6024 or 6026 instruction is decoded, the ENABLE PUNCH BUFFER L signal is generated by the IOT decoder logic. Whatever information is on the DATA 4–11 lines can now be clocked into the Punch Buffer Register. At TP3 time of the instruction the PUNCH STROBE signal clocks the register, transferring the character signals from the DATA 4–11 lines to the HOLE 1–8 lines.

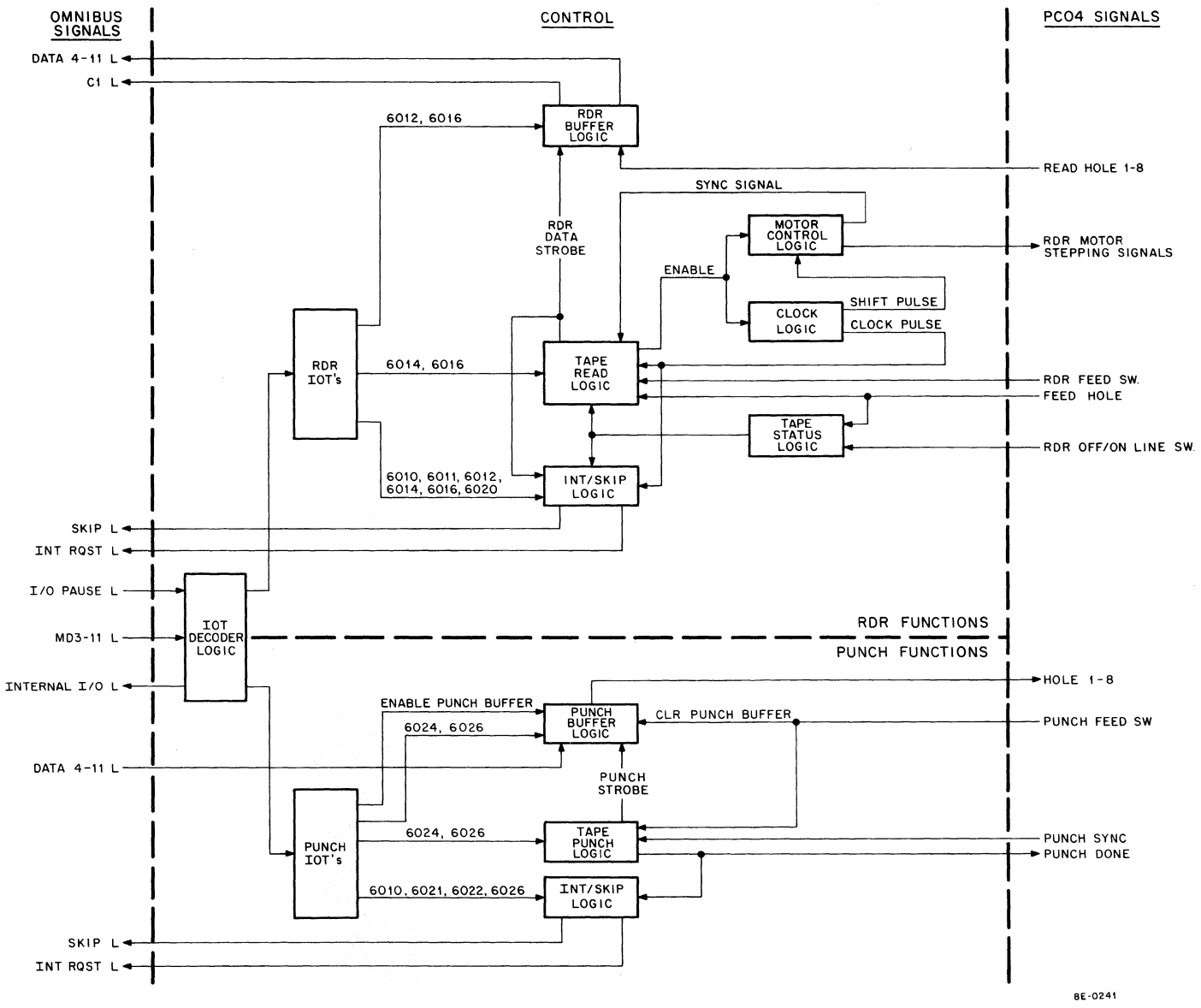

Figure 2-1 PC8-E Control, Block Diagram

Table 2-1
PC8-E IOT Instructions

Octal Code	Mnemonic	Function
6010	RPE	Set the INT ENA flip-flop. The PC8-E is logically connected to the computer interrupt system.
6011	RSF	Skip on Reader flag. Senses the state of the RDR FLAG flip-flop. If the flip-flop is set, the program counter is incremented so that the next sequential instruction is skipped.
6012	RRB	Read the RDR Buffer Register. Causes the RDR Buffer Register to be ORed into the AC Register, clears the RDR FLAG flip-flop.
6014	RFC	Fetch a character from the tape. Clears the RDR FLAG flip-flop, loads a character into the RDR Buffer Register from the tape, sets the RDR FLAG flip-flop when the RDR Buffer Register is loaded.
6016	RRB, RFC	Microprogram of 6012 and 6014. RDR Buffer Register contents are ORed into AC Register, RDR FLAG flip-flop is cleared, character is loaded into Register, and RDR FLAG flip-flop is set.
6020	PCE	Clear the INT ENA flip-flop. The PC8-E is disconnected from the computer interrupt system.
6021	PSF	Skip on Punch flag. Senses the state of the PUNCH FLAG flip-flop. If the flip-flop is set, the program counter is incremented so that the next sequential instruction is skipped.
6022	PCF	Clear the Flag. Clears the PUNCH FLAG flip-flop.
6024	PPC	Load Punch Buffer Register, punch character. Transfers the AC4–11 contents to the Punch Buffer Register, punches the character, sets the PUNCH FLAG flip-flop when done.
6026	PLS	Microprogram of 6022 and 6024. Clears the PUNCH FLAG flip-flop, transfers AC4–11 contents to the Punch Buffer Register, punches the character, sets the PUNCH FLAG flip-flop when done.

At the same TP3 time, the tape punch logic is prepared for the punch cycle. When the PUNCH SYNC signal is generated at the start of the punch cycle, the tape punch logic asserts the PUNCH DONE signal. This signal lasts for 10 ms, during which time the punch solenoid drivers are activated and the character is punched onto the tape. At the end of the PUNCH DONE signal, the PUNCH FLAG flip-flop is set. If the punch logic has previously been logically connected to the computer interrupt system, the PUNCH FLAG flip-flop asserts the OMNIBUS INT RQST L signal. The computer enters the interrupt servicing routine to determine the identity of the device. The 6021 instruction in the routine causes the computer to proceed to the PC8-E subroutine to service the interrupt request.

SECTION 4 DETAILED LOGIC

2.1 IOT DECODER LOGIC

Figure 2-2 shows the IOT decoder logic. Table 2-1 lists the PC8-E IOT instructions and a description of each. Bits MD3—8 and I/O PAUSE L are gated to produce signals 601X and 602X representing reader and punch IOTs, respectively. Both signals cause the OMNIBUS INTERNAL I/O signal to be asserted, thereby ensuring that the positive I/O bus interface ignores the IOT instruction.

The 601X signal and bits MD9—11 are applied to the BCD-to-Decimal Decoder, E31 (refer to Appendix A, Volume 1, for details); the decoder provides the reader IOT signals, as illustrated. The 602X signal and bits MD9—11 are applied to decoder E27, which provides punch IOT signals; in addition, the 602X signal causes the ENABLE PUNCH BUFFER L signal to be asserted each time a punch IOT is generated.

2.2 TAPE READ LOGIC

The tape read logic is shown in Figure 2-3. This logic generates control basic timing signals in response to an IOT instruction or a signal from the PC04 FEED switch. Assume that the PC04 Reader motor is stopped (either the reader is between blocks of characters or has just been put on-line).

When the tape is stopped, a character is always directly over the PC04 photoarray. (Refer to Paragraph 4.1 of the *PC04 High-Speed Perforated Paper-Tape Reader/Punch Maintenance Manual* for a detailed description of the tape-feed operation.) When an IOT instruction (6014, for example) is decoded, the control logic first causes the character to be loaded into the RDR Buffer Register by the RDR DATA STROBE signal. It then generates stepping signals that cause the PC04 Reader Motor to turn.

Refer to Figure 2-3. The 6014 L signal sets the RDR RUN flip-flop. Both the CLOCK PULSE L signal and the RDR MOTOR STOPPING L signal are negated at this time; thus, the RDR ENA flip-flop is set via NAND gate E5 (the clock logic is disabled until the ENABLE signal turns it on; the RDR MOTOR STOPPING L signal applies only when the stepping signals are removed). The ENABLE signal generated by the 0-output of the RDR ENA flip-flop initiates both the clock logic and the reader motor control logic. The clock logic first produces a single CLOCK PULSE that is applied to NAND gate E32 and to the C-input of the RDR ENA flip-flop. Because the flip-flop D-input is high at this time, the flip-flop remains set. The NAND gate must be enabled if an RDR DATA STROBE signal is to be generated. The second high input to this NAND gate is produced by either the (A·B) L signal or the ($\overline{A}\cdot\overline{B}$) L signal (one of these two sync signals, generated by the reader motor control logic, is high when the paper-tape holes are directly over the PC04; assume, for this discussion, that (A·B) L is asserted). The negative pulse from E32 sets the R/S flip-flop. The FEED HOLE signal, produced by the PC04 photoarray, enables the 1-output of the R/S flip-flop to activate E23. The negative-going edge of E23's output resets the R/S flip-flop after a small delay determined by the RC network. Consequently, the RDR DATA STROBE signal generated by NOR gate E35 is a narrow pulse (approximately 100-ns wide) and occurs only when the tape-feed hole is over the photoarray. The RDR DATA STROBE signal resets the RDR RUN flip-flop.

After the RDR DATA STROBE signal is generated, the clock logic produces a SHIFT PULSE that causes the reader motor control logic to generate a stepping signal. The tape holes move from over the photoarray; the FEED HOLE signal and the (A·B) L signal are negated. The D-input of the RDR ENA flip-flop is now low. If a 6014 L is not provided before the clock logic generates another CLOCK PULSE, the RDR ENA flip-flop is cleared, initiating a controlled motor-stopping operation. The clock logic is disabled and the reader motor control logic generates a final stepping signal. The reader motor stops and the tape halts with the holes directly over the photoarray. The FEED HOLE signal is again asserted and now the ($\overline{A}\cdot\overline{B}$) L signal is high. The RDR RUN flip-flop can be set by an IOT instruction any time after the RDR ENA flip-flop is cleared. However, the RDR ENA flip-flop can be set again only after a 40-ms delay (the reader motor control logic asserts RDR MOTOR STOPPING L for 40 ms after the RDR ENA flip-flop is cleared).

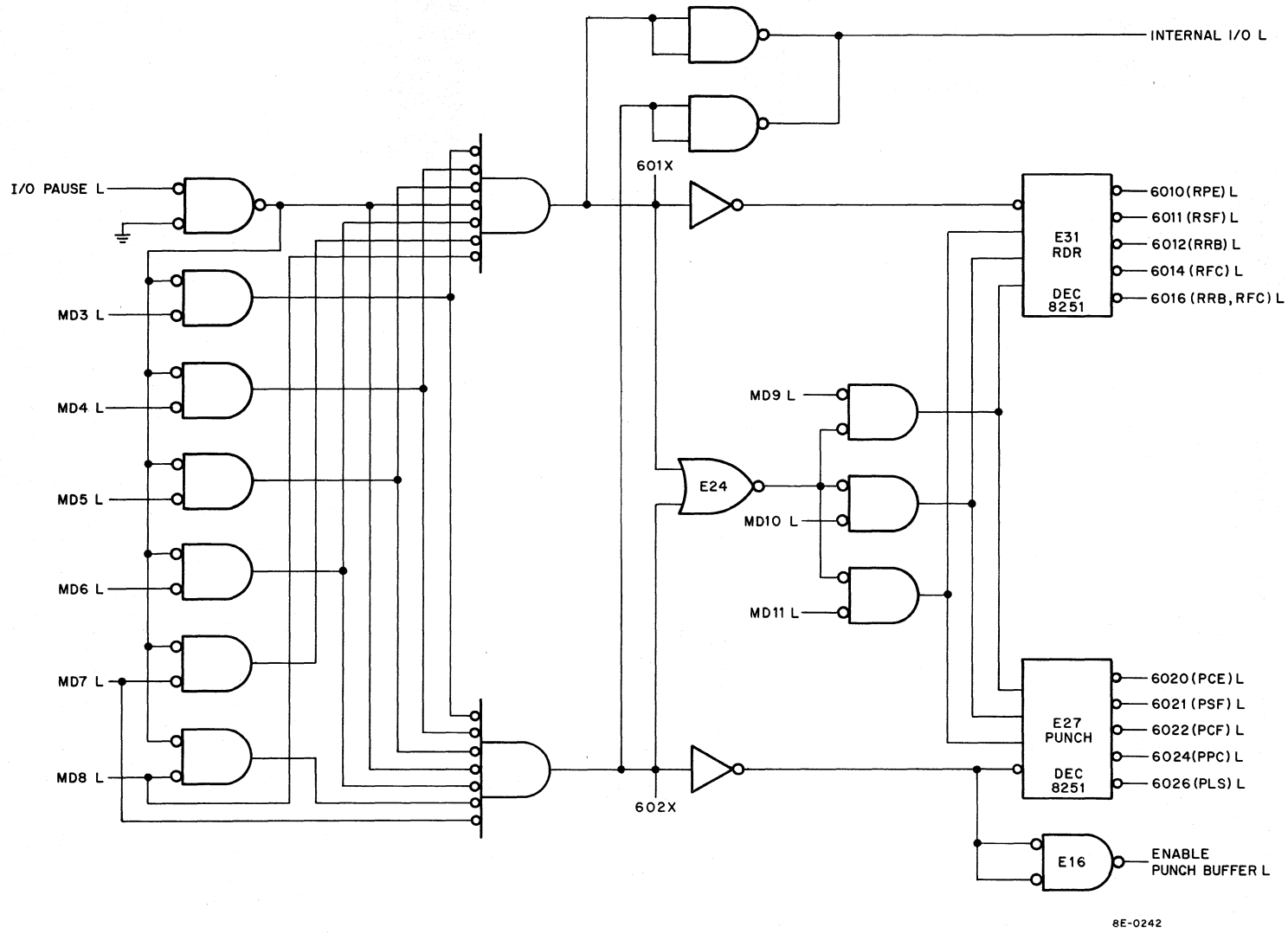

Figure 2-2 IOT Decoder Logic

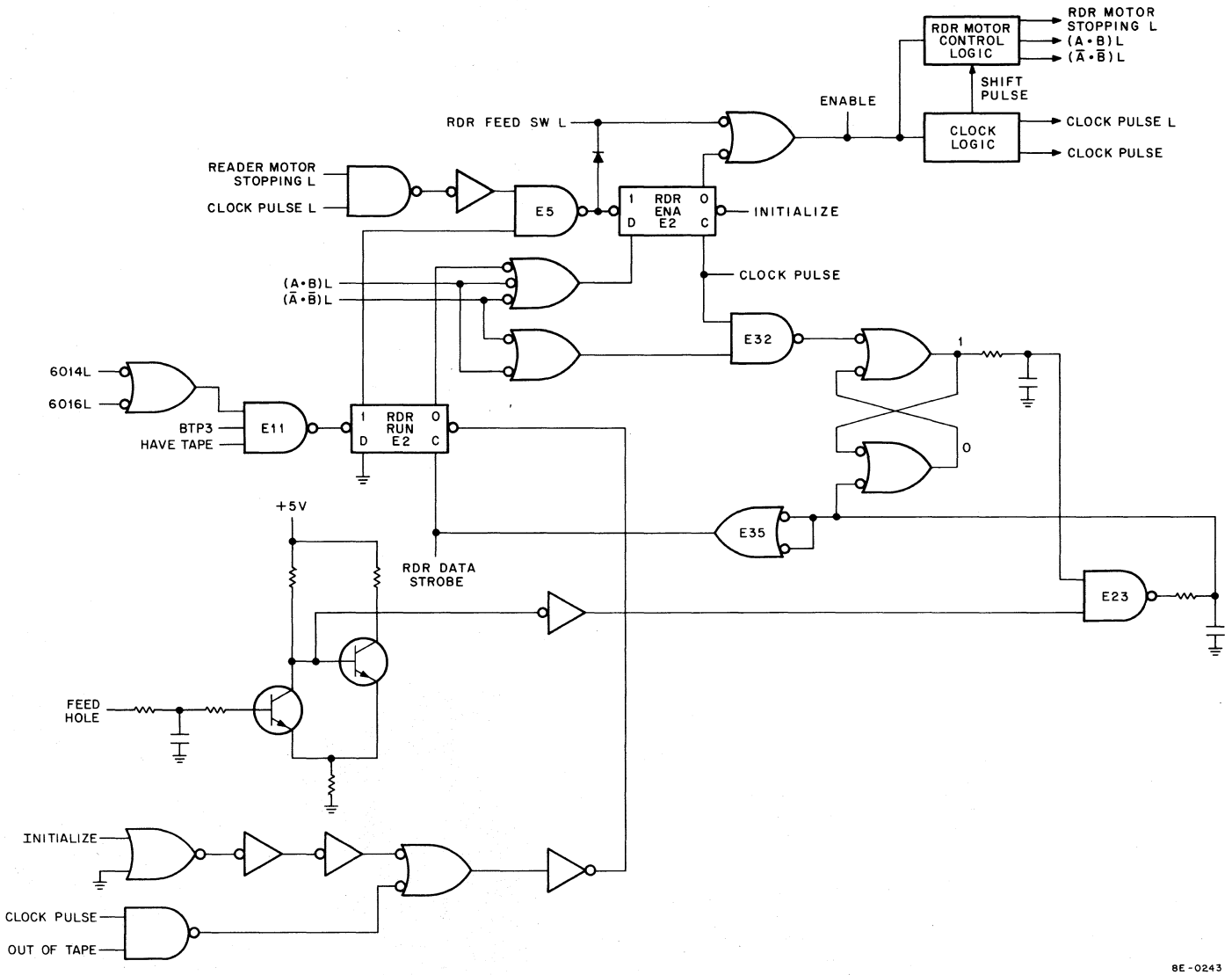

Figure 2-3 Tape Read Logic

If the RDR RUN flip-flop had been set by an IOT instruction before the second CLOCK PULSE occurred, the RDR ENA flip-flop would remain set. The second CLOCK PULSE would then be followed by the second SHIFT PULSE. At this SHIFT PULSE time the $(\overline{A} \cdot \overline{B})$ L and the FEED HOLE signals are asserted. The third CLOCK PULSE causes RDR DATA STROBE to be generated and the RDR RUN flip-flop is again cleared. Thus, a 6014 or 6016 instruction must be decoded at least once for every other clock pulse in order to maintain a 300 character/second rate of operation.

Figure 2-4 is a timing diagram that illustrates the tape read logic signals, as well as those of the reader motor control logic and the clock logic. The first clock period illustrated shows the RDR RUN flip-flop being cleared by an RDR DATA STROBE. A 6014 IOT is decoded before the next CLOCK PULSE. However, between the third and fourth CLOCK PULSES, no IOT is decoded and, therefore, the controlled motor-stopping operation is begun (this is covered fully in Paragraph 2.4).

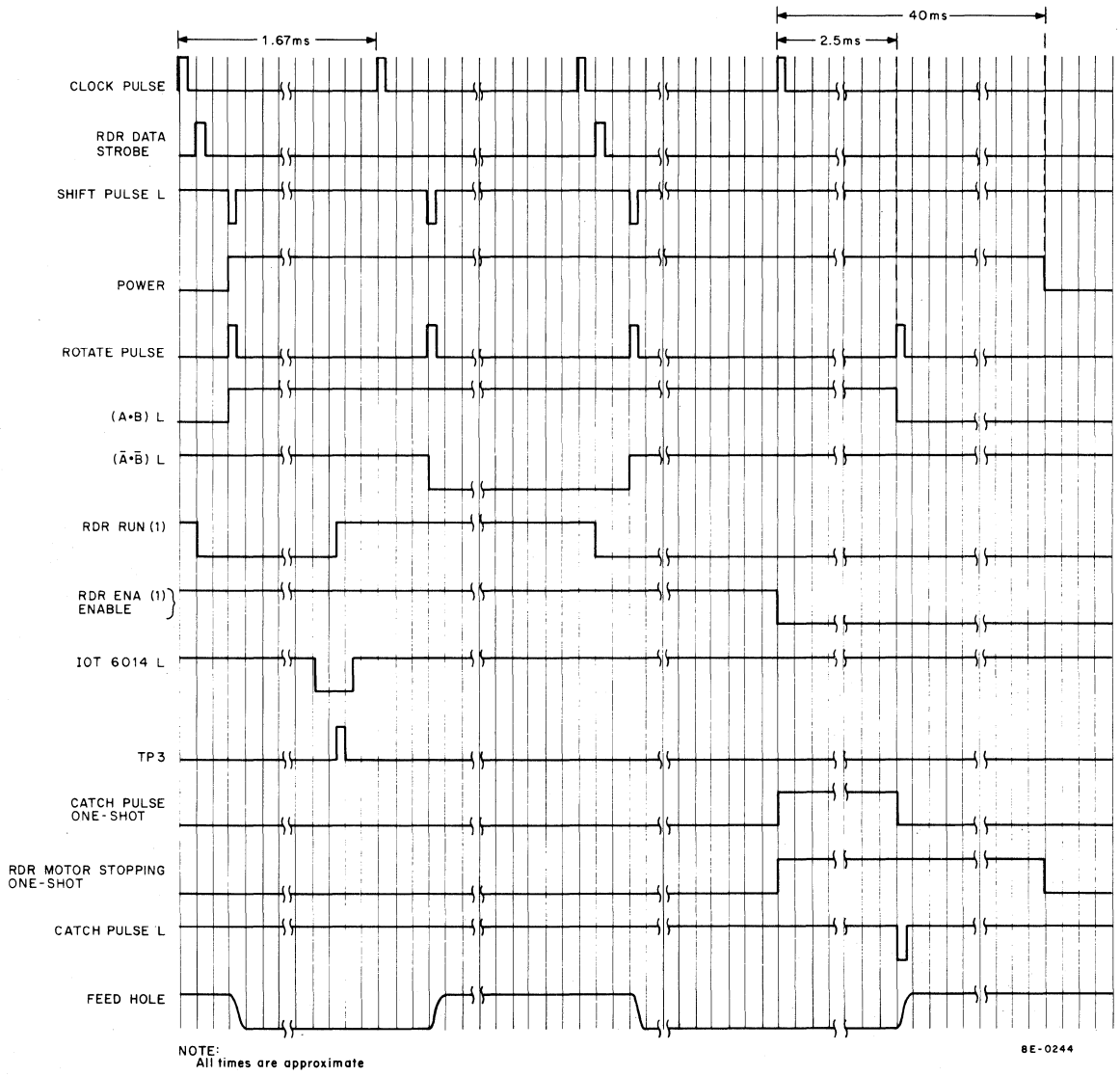

Figure 2-4 Reader Timing

2.3 CLOCK LOGIC

The clock logic is shown in Figure 2-5. The logic consists of a ramp generator, a triggered free-running multivibrator, and two pulse-forming delay networks.

During continuous operation, the reader motor is stepped once every 1.67 ms. However, when the motor must be started from a dead stop, the inertia of the motor and the tape drive wheel must be overcome. Initially, the shaft turns more slowly, and, consequently, the tape moves over the photoarray more slowly than at continuous operating speed. With each step of the motor the speed of the tape approaches continuous operating speed. In order to maintain a nearly constant ratio of tape speed to CLOCK PULSE frequency, the ramp generator, which includes transistors Q1 and Q2, is used.

When the ENABLE signal is asserted by the tape read logic, the free-running multivibrator, Q4/Q5, is triggered on via Q3. At the same time, the ramp generator is triggered. The emitter of Q2 provides the charging potential for the multivibrator. This potential is initially such that the first CLOCK PULSE period is 5 ms. The emitter potential of Q2 rises at a rate determined by the RC time constant, which can be varied by R27 (refer to Paragraph 5.3.8 of the *PC04 High-Speed Perforated Paper-Tape Reader/Punch Maintenance Manual* for adjustment procedures). As the potential rises, the capacitors in the base circuits of Q4 and Q5 take less time to charge. Thus, the on/off cycle of Q4 and Q5 decreases. Ultimately, when the ramp has ended, the CLOCK PULSE period is 1.67 ms.

The method used to generate the SHIFT PULSE L signal and the CLOCK PULSE signal is illustrated in Figure 2-6. The RC delay circuits are used extensively in the control logic. Because the circuit in Figure 2-5 is more detailed than others, it has been selected as an example of the technique. The timing diagram is mainly self-explanatory. The RC delays indicated can be roughly calculated by using the formula Delay = 0.7 RC.

2.4 READER MOTOR CONTROL LOGIC

The reader motor control logic is shown in Figure 2-7. (Refer to Paragraph 4.1.1 of the *PC04 High-Speed Perforated Paper-Tape Reader/Punch Maintenance Manual* for a detailed description of how the reader motor control logic stepping signals control the reader motor.) When the ENABLE signal is asserted by the tape read logic, the two one-shot multivibrators, E4 and E7, are readied for triggering. During continuous operation, the clock logic generates SHIFT PULSEs, the first of which sets the PWR flip-flop, thereby asserting the POWER signal. Each SHIFT PULSE L signal generates a ROTATE PULSE that clocks the A/B end-around shift register. At every other ROTATE PULSE either the $(A \cdot B)$ L signal or the $(\overline{A} \cdot \overline{B})$ L signal is asserted, indicating to the tape read logic that a character is over the photoarray.

If, as explained in Paragraph 2.2, the RDR ENA flip-flop is cleared, the ENABLE signal is negated (provided the reader FEED switch is not activated). The down-going edge of the ENABLE signal triggers E4 and E7 (Figure 2-4). After 2.6 ms, E4 times out and a CATCH PULSE L signal is generated. This pulse produces the ROTATE PULSE that steps the motor a final time. The motor stops with either $(A \cdot B)$ L or $(\overline{A} \cdot \overline{B})$ L asserted and the FEED HOLE signal high.

The E7 one-shot remains set for 40 ms before timing out. During this 40-ms period, the RDR MOTOR STOPPING L signal is asserted and prevents the RDR ENA flip-flop from being set. At the end of the period, the 0-output of E7 clears the PWR flip-flop, negating the POWER signal. Reader operation can be restarted by again setting the RDR ENA flip-flop.

The 40-ms delay provided by E7 ensures that the motor, if not pulsed for continuous operation, has sufficient time to come to a complete stop before it is activated again. If the complete stop were not allowed, undesirable oscillations in the drive motor would result, causing possible false data outputs.

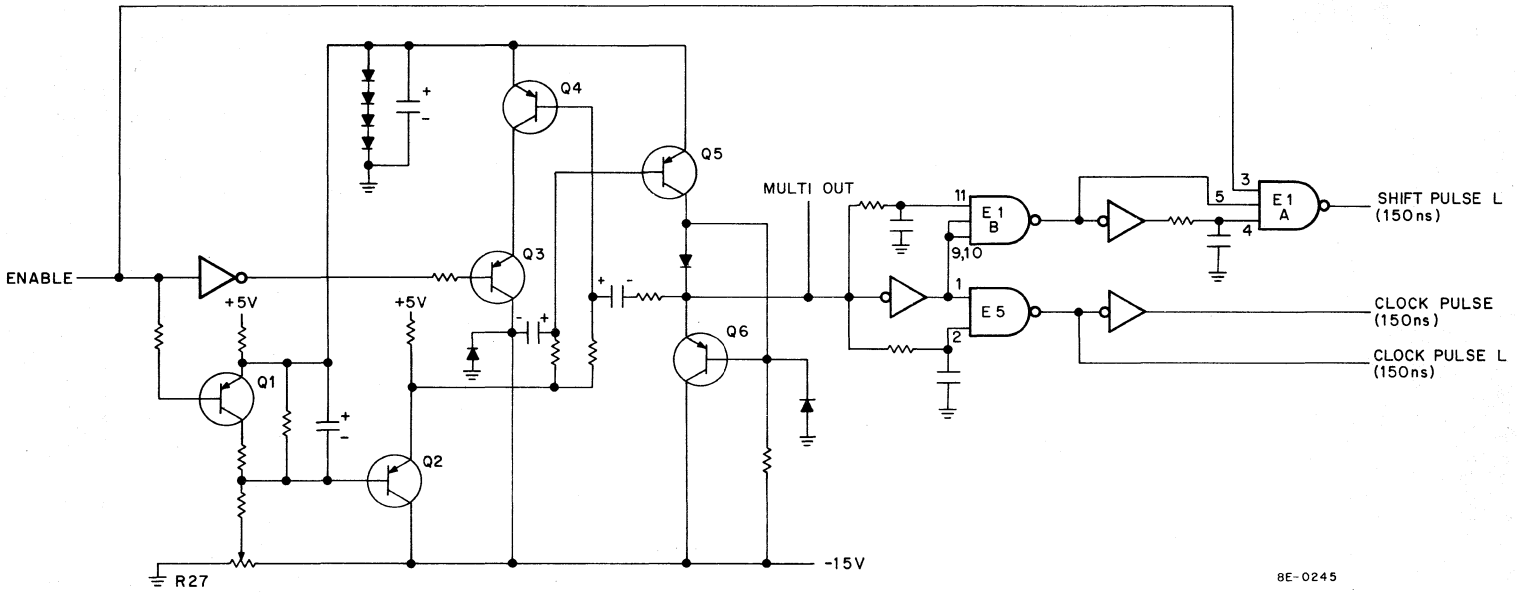

Figure 2-5 Clock Logic

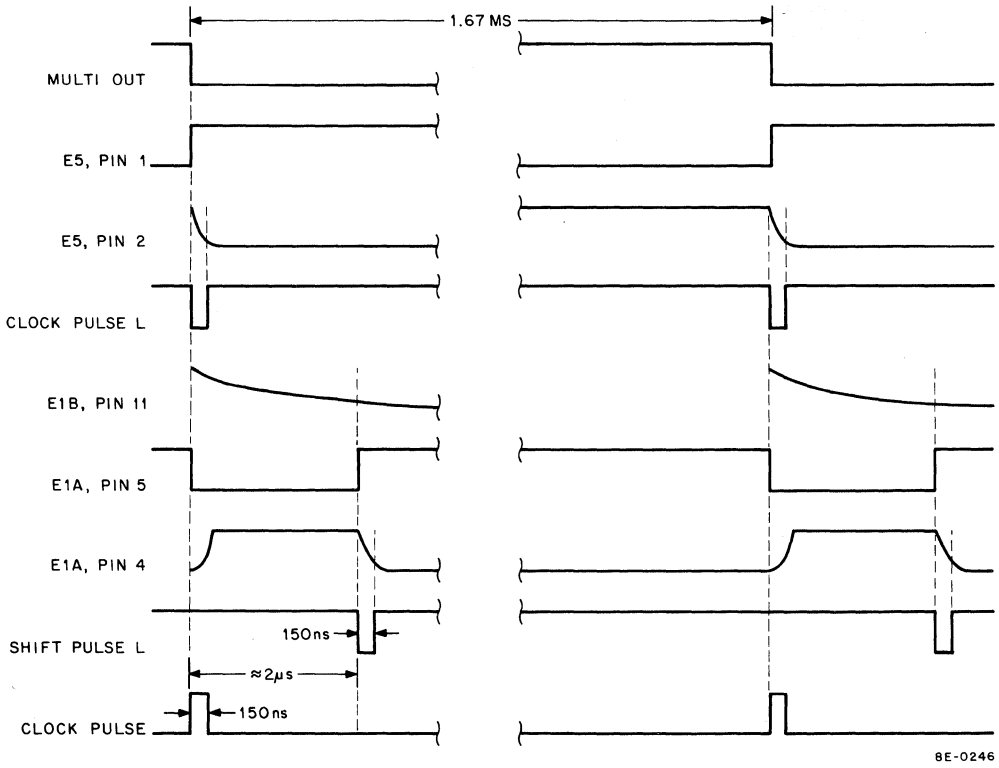

Figure 2-6 Clock/Shift Pulse Timing

2.5 RDR INT/SKIP LOGIC

The RDR INT/skip logic is shown in Figure 2-8. When an RDR DATA STROBE signal is generated it sets the RDR FLAG flip-flop (the RDR RUN flip-flop provides the necessary high at E12's D-input before being cleared, itself, by RDR DATA STROBE). Because RDR DATA STROBE also loads the RDR Buffer Register, the RDR FLAG flip-flop being set indicates that the control is ready to transfer data. If the INT ENA flip-flop has been set previously, either under program control or by INITIALIZE, the OMNIBUS INT RQST L signal is asserted. When the computer enters the PC8-E servicing subroutine, an appropriate IOT instruction reads the Buffer Register and clears the RDR FLAG flip-flop via NOR gate E1.

2.6 RDR BUFFER LOGIC

The reader buffer logic is shown in Figure 2-9. Data supplied on the READ HOLE 1–8 lines is clocked into the register by the RDR DATA STROBE signal. Either 6012 L or 6016 L gates the character onto the OMNIBUS DATA 4–11 lines. At the same time, the IOT instruction asserts the OMNIBUS C1 L signal, resulting in an ORing of the DATA 4–11 bits and the CPU AC Register contents.

2.7 TAPE STATUS LOGIC

The tape status logic is shown in Figure 2-10. The logic monitors both the FEED HOLE signal and the RDR ENA flip-flop, generating an OUT OF TAPE signal when tape is not loaded in the PC04 Tape Feeder. This signal ensures that the tape read logic cannot be triggered by a program instruction read command. The complementary signal, HAVE TAPE, is generated when tape is in the feeder, enabling the tape-feed operation to begin when program-directed.

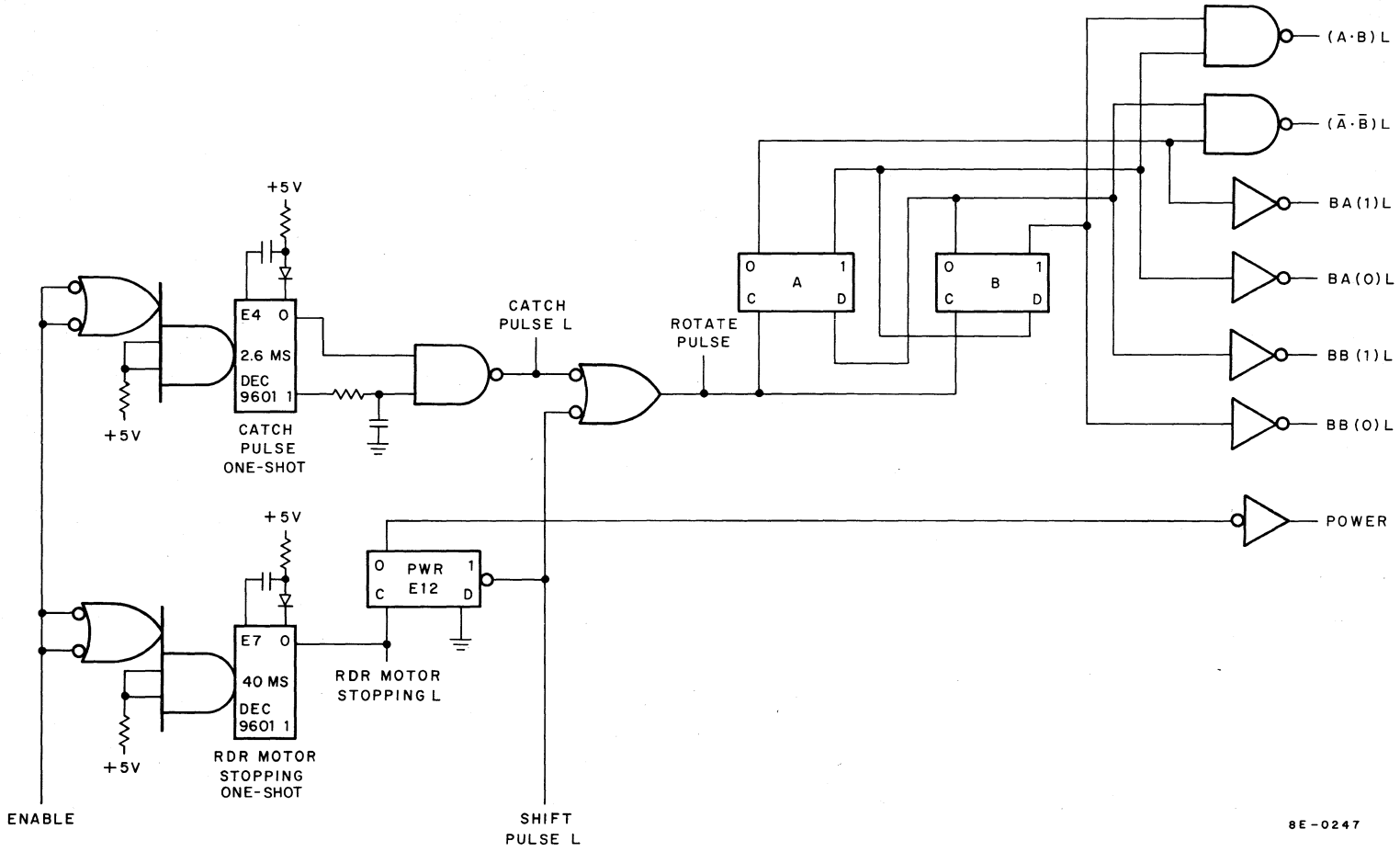

Figure 2-7 Reader Motor Control Logic

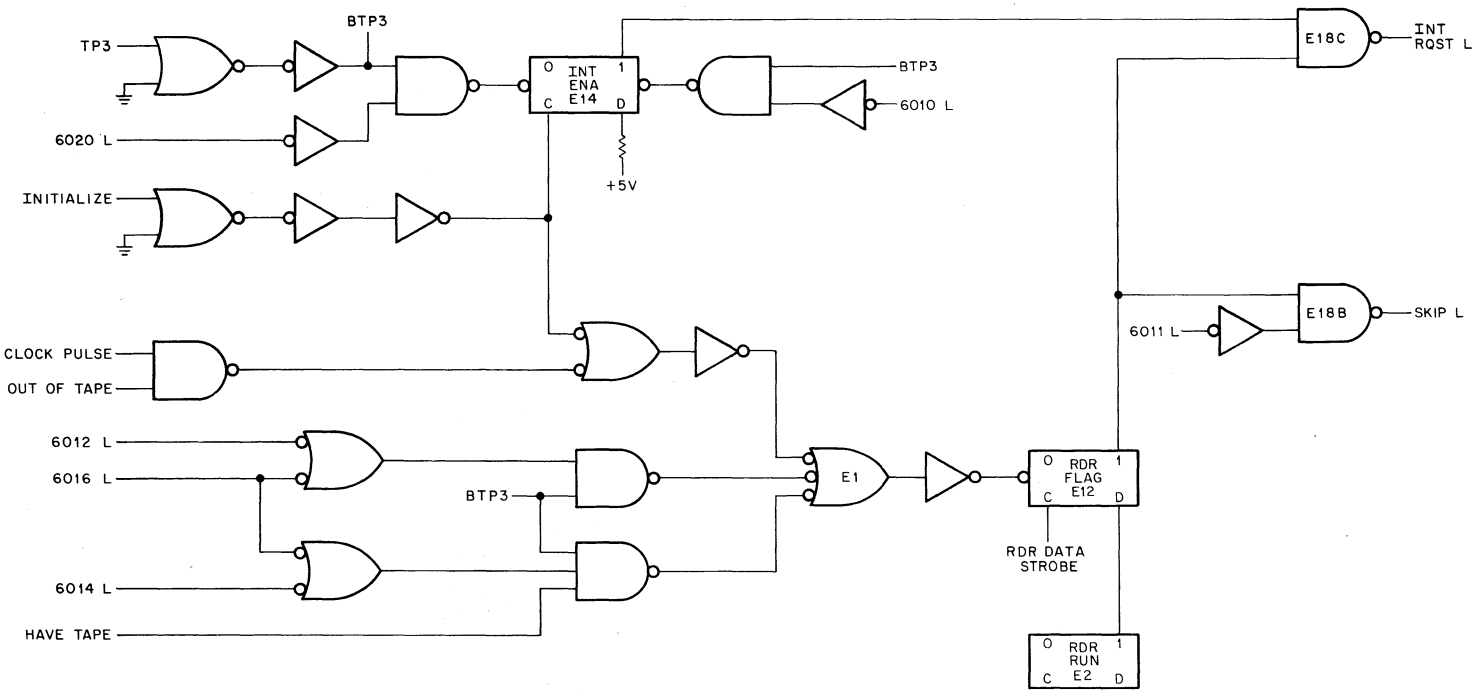

Figure 2-8 RDR INT/Skip Logic

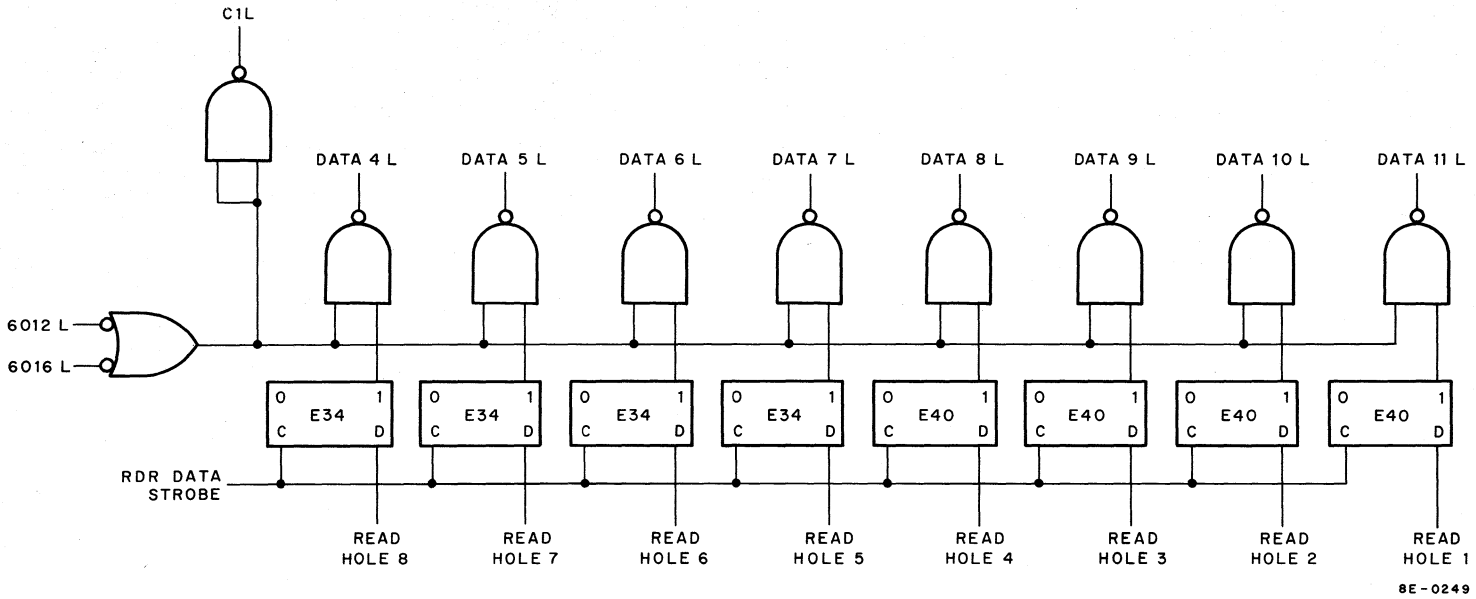

Figure 2-9 Reader Buffer Logic

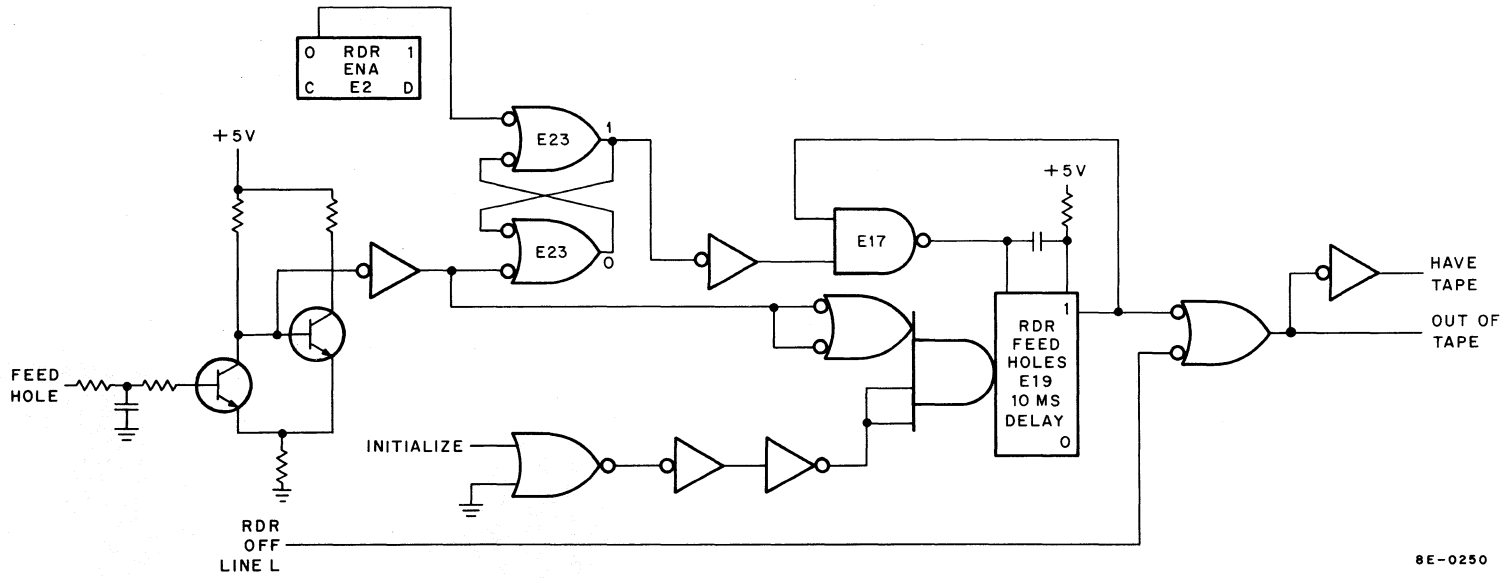

Figure 2-10 Tape Status Logic

If no tape has been inserted in the feeder, the FEED HOLE signal is high, just as it is when an actual feed hole is detected by the photoarray. The RDR FEED HOLES one-shot, E19, is in its stable state; thus, the OUT OF TAPE signal is asserted. If a read command is issued by the program, the RDR RUN flip-flop (Figure 2-3) is prevented from being set by the HAVE TAPE signal that is low at this time. Therefore, the RDR ENA flip-flop is not set and the clock logic is not triggered.

When a tape is inserted in the feeder, the photoarray light source rays are interrupted briefly by the tape web. The FEED HOLE signal goes low, and the negative-going edge causes one-shot E19 to be triggered; thus, the HAVE TAPE signal is asserted. At the same time that E19 is triggered, the flip-flop consisting of the cross-coupled NOR gates is cleared. Because the RDR ENA flip-flop is also clear, flip-flop E23 is latched in the clear state. NAND gate E17 is enabled; the resulting low at pin 11 of E19 holds the one-shot in the triggered state, i.e., the 1-output stays high. The HAVE TAPE signal remains high indefinitely, if the program does not issue a read command.

When a read command is issued, the RDR RUN flip-flop is set, causing the RDR ENA flip-flop to be set, also. The 0-output of the RDR ENA flip-flop triggers the clock logic, which generates a CLOCK PULSE, and sets flip-flop E23, which disables NAND gate E17. The one-shot enters the timeout state, during which it can be re-triggered by each trailing edge of the FEED HOLE signal. A ROTATE PULSE, generated by the clock logic approximately 2 μs after the CLOCK PULSE (Figure 2-4), causes the tape to begin feeding through the read station. The resulting negative transition of the FEED HOLE signal re-triggers the one-shot (note that flip-flop E23 is held in the set state by the 0-output of the RDR ENA flip-flop). If another trailing edge occurs within 10 ms, the one-shot is again re-triggered (a 10-ms period is necessary because the reader motor is being started from a dead stop and, consequently, the tape moves more slowly than at continuous operating speed; in continuous operation, a trailing edge occurs at 3.34-ms intervals). If the program issues read commands at such a rate that continuous operation results (at least one command between each RDR DATA STROBE and the next CLOCK PULSE), one-shot E19 is re-triggered continuously, and the HAVE TAPE signal remains asserted.

Suppose that at some point during this continuous operation a read command is not issued within approximately 3.34 ms of the preceding command. In such a situation, the motor-stopping operation is initiated. At the moment this operation begins, the RDR ENA flip-flop is cleared, and the FEED HOLE signal is low. Therefore, flip-flop E23 is again latched in the clear state, and one-shot E19 is held in its triggered state. The HAVE TAPE signal remains high while the motor is stopped.

If read commands are issued at a continuous rate and the tape runs out of the tape feeder, the OUT OF TAPE signal must be asserted. When the last portion of tape web uncovers the light source, the FEED HOLE signal goes high and remains high. One-shot E19 times out approximately 8.5-ms later, and the OUT OF TAPE signal goes high. During this 8.5-ms period, three RDR DATA STROBE pulses occur. Each of these pulses loads the Reader Buffer with 1s. Consequently, at least two transfers, possibly three, of 1s to the AC Register take place before the RDR RUN flip-flop is cleared and the clock logic is disabled.

2.8 TAPE PUNCH LOGIC

When the punch ON/OFF switch is in the ON position, the punch motor runs continuously. A tape that is loaded in the punch feeder mechanism can be punched if the FEED switch is in the FEED position, or if the program issues a punch command IOT instruction, 6024 or 6026. Either method results in the PUNCH DONE signal being generated in the tape punch logic (Figure 2-11).

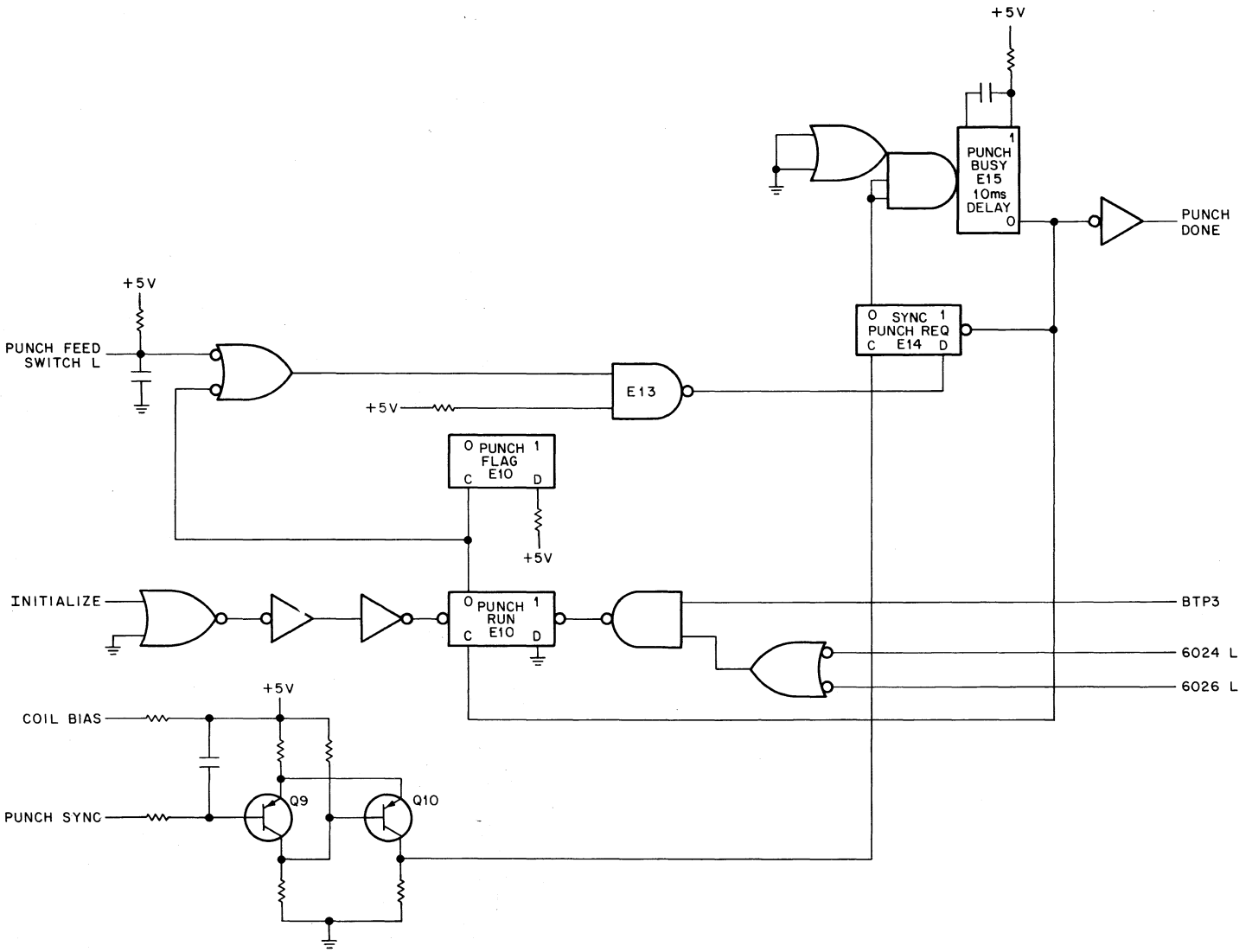

Figure 2-11 Tape Punch Logic

When the 6026 IOT instruction is issued, for example, the PUNCH RUN flip-flop, E10, is set. Setting E10 causes the D-input of the SYNC PUNCH REQ flip-flop, E14, to go low. A PUNCH SYNC signal from the tape punch mechanism can clear E14, thereby triggering the PUNCH BUSY one-shot, E15. This PUNCH SYNC signal occurs once during each punch motor revolution and signals the start of the punch mechanical cycle. The signal is applied to the Schmitt trigger, Q9 and Q10, and the output at the collector of Q10 clears E14. The resulting 10-ms PUNCH DONE signal enables the PC04 solenoid drivers to activate the punch mechanism. The tape is punched with the character that was placed on the HOLE 1–8 lines by the punch buffer logic, shown in Figure 2-12 and discussed briefly in Paragraph 2.9.

2.9 PUNCH BUFFER LOGIC

The punch buffer logic is shown in Figure 2-12. Either the 6024 L signal or the 6026 L signal enables the Buffer Register to be loaded at TP3 time with the information carried on the DATA 4–11 lines. This information is then gated to the HOLE 1–8 lines, respectively. Note that the information loaded at this time remains in the register until another punch instruction is issued or until the FEED switch is activated.

2.10 INT/SKIP LOGIC

After the tape has been punched and the punch mechanical cycle ends, the PUNCH BUSY one-shot times out. The PUNCH RUN flip-flop is cleared and the 0-output of the flip-flop sets the PUNCH FLAG flip-flop (Figure 2-13). If the INT ENA flip-flop, E14, is set at this time, the OMNIBUS INT RQST L signal is asserted. The computer enters the interrupt routine and proceeds from there to the punch subroutine.

SECTION 5 MAINTENANCE

Refer to Volume 1 and the *PC04 High-Speed Perforated Paper-Tape Reader/Punch Maintenance Manual* for PC8-E maintenance information.

Table 2-2 presents cable and connector pin assignments for the two cables that connect the control and the PC04.

SECTION 6 SPARE PARTS

Table 2-3 lists recommended spare parts for the PC8-E. These parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

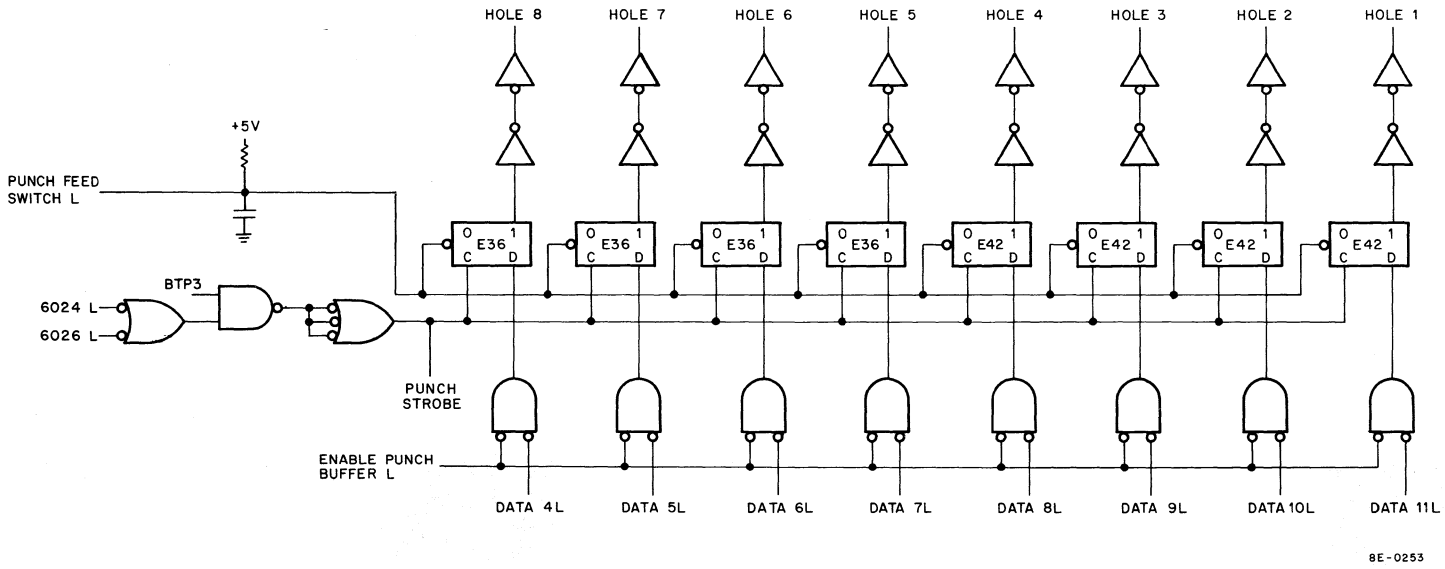

Figure 2-12 Punch Buffer Logic

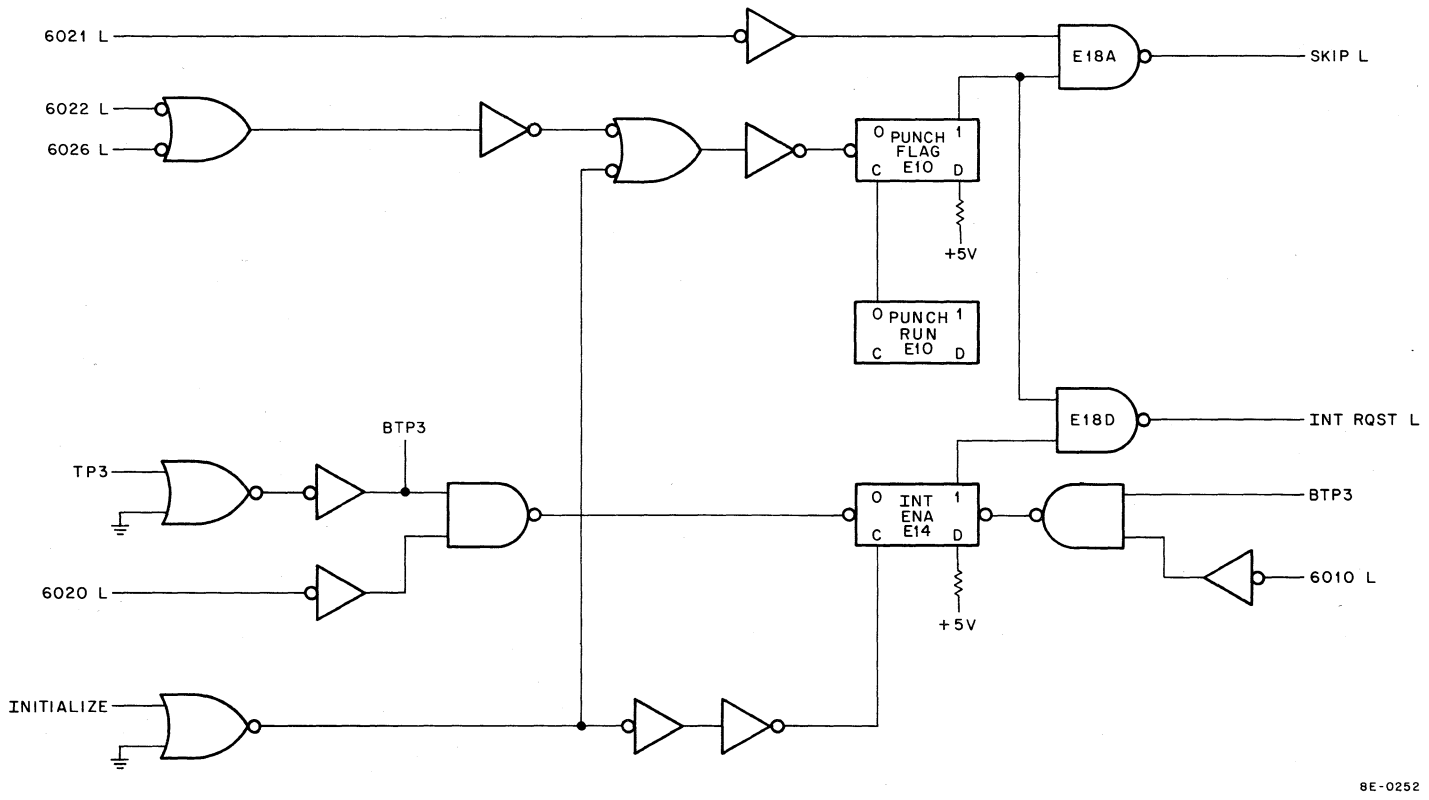

Figure 2-13 Punch INT/Skip Logic

Table 2-2
Cable/Connector Pin Assignments

Control Connector Pin	Signal Name		M955 Connector Pin
	J1 (Connects to B1)	J2 (Connects to A1)	
D	PUNCH FEED SWITCH	N/C	A
F	SCR ACTIVE	RDR ON/OFF LINE	B
J	PUNCH SYNC	GND	C
L	N/C	READ HOLE 1	D
N	PUNCH DONE	READ HOLE 2	E
R	PUNCH NOT UP TO SPEED	READ HOLE 3	F
T	HOLE 8	READ HOLE 4	H
V	HOLE 7	READ HOLE 5	J
X	HOLE 6	READ HOLE 6	K
Z	HOLE 5	READ HOLE 7	L
BB	COIL BIAS	READ HOLE 8	M
DD	HOLE 4	FEED HOLE	M
FF	HOLE 3	BA (0)	P
JJ	HOLE 2	BA (1)	R
LL	HOLE 1	BB (0)	S
NN	N/C	BB (1)	T
RR	N/C	POWER	U
TT	N/C	RDR FEED SWITCH	V
GND PINS A, B, C, E, H, K, M, P, S, U, W, Y, AA, CC, EE, HH, KK, MM, PP, SS, UU, VV			

Table 2-3
PC8-E Recommended Spare Parts

DEC Part Number	Description	Quantity
19-05547	IC DEC 7474	1
19-05575	IC DEC 7400	2
19-05576	IC DEC 7410	1
19-09486	IC DEC 384	1
19-09487	IC DEC 9601	1
19-09686	IC DEC 7404	2
19-09971	IC DEC 6380	1
19-09972	IC DEC 6314	1
19-09973	IC DEC 97401	1
19-09594	IC DEC 8251	1
19-05579	IC DEC 7440	1
19-10087	IC DEC MC4015P	1
15-03409	Transistor, 6543 D	1
15-09338	Transistor, PMS 6531	1
11-00113	Diode, D662	1
11-00114	Diode, D664	2
10-01610	Capacitor, 0.01 μF, 100V, 20%	2