CHAPTER 4
MI8-E HARDWARE BOOTSTRAP LOADER

SECTION 1 INTRODUCTION

4.1 GENERAL DESCRIPTION

The MI8-E Bootstrap Loader option uses a 32-word Read-Only Memory (ROM) with diodes that can be arranged to accommodate any program up to 32 words in length. The Bootstrap Loader option is available in the following configurations:

Option Designation	RIM Program
MI8-E	Unencoded
MI8-EA,B	Paper Tape
MI8-EC	TC08 DECtape
MI8-ED	RK8
MI8-EE	Typeset
MI8-EF	Edu System (low)
MI8-EG	Edu System (high)
MI8-EH	TD8-E DECtape

Each configuration contains a uniquely encoded ROM in the form of a specific Read-In Mode (RIM) program. Without this option, RIM would be toggled into memory by the operator at the programmer's console. The RIM loader instructs the computer to receive and store, in core, data from any of the above peripherals in RIM-coded format.

The MI8-E Bootstrap Loader is contained on one quad-size module, designated M847, that plugs directly into the OMNIBUS. All signals enter and leave the module via the OMNIBUS.

4.2 EQUIPMENT REQUIREMENTS

The following basic equipment is necessary to operate and maintain the MI8-E Bootstrap Loader:

a. PDP-8/E Computer
b. ASR-33 Teletype or Equivalent
c. Low- or High-Speed Paper-Tape Reader
d. Low- or High-Speed Paper-Tape Punch
e. MI8-E Bootstrap Diagnostic
f. Bootstrap Loader Option

4.3 COMPANION DOCUMENTS

The following documents and publications are necessary for the operation, installation, and maintenance of this option:

a. *PDP-8/E & PDP-8/M Small Computer Handbook* – DEC, 1972
b. *PDP-8/E Maintenance Manual* – Volume 1
c. *Introduction to Programming* – DEC, 1972
d. DEC engineering drawing, Bootstrap Loader Option, number M847-0-1
e. *MI8-E Bootstrap Loader Diagnostic Manual,* MAINDEC-8E-D11A-D-(D)

4.4 SOFTWARE

The MAINDEC-8E-D11A-D diagnostic is used to troubleshoot and verify the operation of the MI8-E Bootstrap Loader option in all configurations shown in Paragraph 4.1.

The diagnostic is available in a low- and high-core version. The version used to test an MI8-E Module will depend on the memory locations utilized by that particular module. The low-core version occupies and uses memory locations 0200-1777, the high-core version occupies and uses memory locations 4200-5777. Use the version that does not conflict with the memory locations of the bootstrap block for the MI8-E Module under test.

SECTION 2 INSTALLATION

The MI8-E Bootstrap Loader option is installed on-site by DEC Field Service personnel. The customer should **not** attempt to unpack, inspect, install, checkout, or service the equipment.

4.5 INSTALLATION

Perform the following procedures to install the MI8-E option:

Step	Procedure
1	Remove the module from the shipping container.
2	Inspect the module for any apparent damage.
3	Verify that the initial address, field address, and starting address jumpers are correct according to Table 4-1.
4	Verify that the diode matrix is properly cut.
5	Connect the module to a convenient OMNIBUS slot. The module should be located reasonably close to the MM8-E Modules.

4.6 CHECKOUT

Perform the following procedures to checkout the MI8-E option:

Step	Procedure
1	Perform acceptance tests provided in Paragraph 2.3, Volume 1.
2	Load MAINDEC-8E-D11A-D. This verifies the correct operation of the MI8-E Bootstrap Loader in all of its standard configurations.

(continued on next page)

Step	Procedure
3	If this verification was not performed satisfactorily, refer to Section 5 for troubleshooting procedures.
4	Make proper entry on user's log that the acceptance test for the MI8-E option was performed satisfactorily.

Table 4-1
MI8-E Bootstrap Loader Option Encoding Scheme

Option	MI8-E Unencoded	MI8-EA Paper Tape	MI8-EC TC08 DECtape	MI8-ED RK8	MI8-EE Typeset	MI8-EF Edu Sys Low	MI8-EG Edu Sys High	MI8-EH TD8-E Dectape
INITIAL	0	7737	7554	0023	7756	7737	6007	7300
ADDRESS		6014	7600	6007	7771	6007	6007	1312
Data		0776	6774	6751	6014	7604	7604	4312
		7326	1374	6745	6011	7510	7510	4312
		1337	6766	5025	5360	3343	3343	6773
		2376	6771	7200	7106	6766	6766	5303
		5340	5360	6733	7106	6771	6771	6777
		6011	7240	5031	6012	5344	5344	3726
		5356	1354	7777	7420	1376	1376	2326
		3361	3773	7777	5357	5343	5343	5303
		1361	1354	"	5756	7600	7600	5732
		3371	3772	"	4356	6603	6603	2000
		1345	1375	"	3373	6622	6622	1300
		3357	6766	"	4356	5352	5352	6774
		1345	5376	"	7777	5752	5752	6771
		3367	7754	"	"	7577	7577	5315
		6032	7755	"	"	6032	6014	6776
		6031	0600	"	"	6031	6011	0331
		5357	0220	"	"	5357	5357	1327
		6036	6771	"	"	6036	6016	7640
		7106	5376	"	"	7106	7106	5315
		7006	7777	"	"	7006	7006	2321
		7510	"	"	"	7510	7510	5712
		5374	"	"	"	5357	5374	7354
		7006	"	"	"	7006	7006	7756
		6031	"	"	"	6031	6011	7747
		5367	"	"	"	5367	5367	0077
		6034	"	"	"	6034	6016	7400
		7420	"	"	"	7420	7420	7777
		3776	"	"	"	3776	3776	"
		3376	"	"	"	3376	3376	"
		5356	"	"	"	5356	5357	"
Data	0	0	"	"	"	0220	0220	"
Starting Address		7737	7754	7703	7770	7737	7737	7300

SECTION 3 OPERATING PROCEDURES

The operating procedures for the Bootstrap Loader are as follows:

Step	Procedure
1	If the RUN lamp is on, depress the HLT key and observe that the RUN lamp is off.
2	Depress and raise the SW key.
3	Observe that the RUN lamp is again illuminated.

SECTION 4 PRINCIPLES OF OPERATION

4.7 GENERAL DESCRIPTION

The relation of the Bootstrap Loader and the CPU is similar to that of the operator's console and the CPU. Both the loader and the panel must:

a. Initialize the CPU.

b. Load Address. } to define the first address in which to deposit instructions

c. Load Extended Address. }

d. Deposit instructions in sequential locations.

e. Load starting address of the program just deposited.

f. Start the program.

Because the operation of the Bootstrap Loader is closely tied in with the operation of the processor, the reader should have a thorough understanding of the processor control signals. Detailed theory of the processor and memory is given in Chapter 3, Volume 1; the control signal description is provided in Chapter 9 of the *PDP-8/E & PDP-8/M Small Computer Handbook*.

A summary description of the control signals necessary to accomplish the six operations listed above is given in the following:

Operation	Assert	Affect on CPU
Initialize (Bootstrap)	Ground: POWER OK H (Pin BV2)	Causes the CPU's MA Control flip-flop to clear. Also causes the CPU's timing generator to generate.
Initialize (Panel)	INITIALIZE H (Pin CR1)	INITIALIZE H, clearing the AC, Link, all flags, and the Interrupt and Break systems.
Load Initial Address	Ground: LA ENABLE L (pin BM2) Place initial address onto the data lines of the OMNIBUS Pulse: PULSE LA H (Pin DR2)	Loads the address placed on the data lines into the CPMA register.

(continued on next page)

Operation	Assert	Affect On CPU
Load Extended Address	Ground: KEY CONTROL L (Pin DU2) Place extended address bits onto Data 6–8 and Data 9–11 Pulse: PULSE LA H (Pin DR2)	Loads the addresses placed on bits 6–8 and 9–11 of the DATA BUS into the IF and DF of the Memory Extension Control, Type KM8-E, if one is in the machine.
Deposit (used by panel)	Ground: KEY CONTROL L (Pin DU2) MS, IR DISABLE L (Pin CV1) Place bits to be deposited onto DATA BUS. Pulse (low): MEM START L (Pin AJ2)	Causes one memory cycle to occur. Word on DATA BUS is deposited, and PC is incremented. Machine stops at end of memory cycle.
Deposit (used by bootstrap)	Same as Deposit above, except KEY CONTROL L (Pin DU2) goes high during TS3 of computer's cycle.	Same as above, except that the machine continues to run.
Load Starting Address	Same operation as Load Initial Address except for the word placed on the DATA BUS.	
Start Program	Pulse (low): MEM START L (Pin AJ2)	Starts program.

To minimize the logic needed for the MI8-E, an extra Load Extended Address operation takes place just before starting the program. Hence the complete sequence of operations is:

a. Initialize the CPU, Bootstrap, and all system devices.

b. Load Initial Address.

c. Load Extended Address.

d. Deposit 32 words into memory.

e. Load Starting Address of the bootstrap program just deposited.

f. Load Extended Address.

g. Start the bootstrap program.

4.8 MAJOR PORTIONS OF THE MI8-E

A block diagram of the major portions of the MI8-E is shown in Figure 4-1. When power is applied to the computer, critical control flip-flops within the MI8-E are initialized so that the MI8-E is inoperative and the computer can run normally. If the switch labeled SW on the operator's console is moved to the "down" position and then to the "up" position, the MI8-E will operate.

NOTE

SW should be left in the "up" position when the MI8-E is not being used. If SW is left in the "down" position, the MI8-E will operate if the machine is stopped and the console's OFF/POWER/PANEL LOCK switch is moved to the PANEL LOCK position.

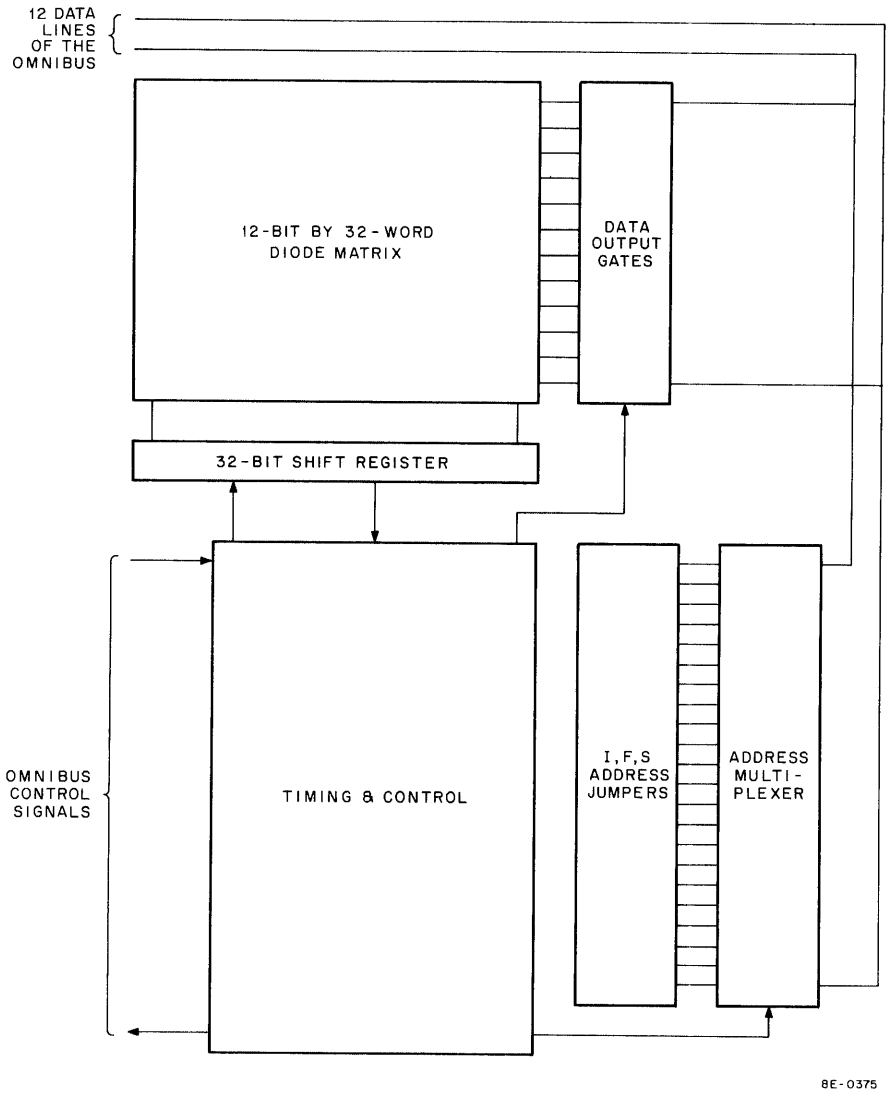


Figure 4-1 MI8-E Block Diagram

4.8.1 Address and Data Information

Address information is stored in three sets of jumpers denoted as follows:

Designation	Function
I0—I11	Initial address. I0 is the most-significant bit. The address encoded in the I jumpers is the first of 32 successive locations into which instructions will be loaded by the MI8-E.
S0—S11	Starting address. S0 is the most-significant bit. This address is the address at which the MI8-E will start the program after the bootstrap program has been stored.
F2, F1, F0	Field bits. F2 is the most-significant bit. These bits are loaded into both the IF and DF of the Memory Extension Control, Type KM8-E.

In all cases, the presence of address jumpers indicates a binary 0; the absence of a jumper indicates a binary 1. Unencoded MI8-E boards are shipped with all jumpers in place.

Data to be deposited in memory is encoded by the presence (binary 0) or absence (binary 1) of diodes in a 12-bit by 32-word matrix. The positions of words and bits within words are clearly indicated in etch on the board; the presence or absence of diodes and jumpers for standard bootstraps is shown on the engineering drawings.

4.8.2 Sequence of Operations

When SW is operated while the computer is on but not running, the MI8-E's timing and control logic is activated. The MI8-E first grounds POWER OK H to initialize the computer. Simultaneously, it clears the 32-bit shift register that drives the diode matrix. The timing and control logic then loads I and F addresses into the CPU and Extension Control, respectively, by enabling the appropriate address multiplexer and then placing signals onto the OMNIBUS. These signals have already been described in Paragraph 4.7. The MI8-E then shifts a 1 into the first bit of the 32-bit long shift register, enables the matrix data output gates, and starts the processor's timing chain. Thus, the contents of the first word in the matrix are placed on the DATA BUS. Control signal MS, IR DISABLE L, applied to the OMNIBUS, causes this word to be written into memory. The KEY CONTROL L signal causes the next sequential address to enter the CPMA, KEY CONTROL L is allowed to go high during TS3 of the processor's cycle so that the processor continues to run. At the end of each memory cycle (TP4) the single 1 is shifted down the shift register, and a 0 is shifted into the first bit of the register. This process continues until all 32 words have been deposited.

When the 1 reaches the last bit of the shift register, control circuitry causes the processor to stop. The timing of the MI8-E is restarted. After loading the "S" and "F" addresses into the CPU and Extension Control, the processor is again started and the MI8-E's job is done.

4.8.3 Bootstrap Timing (Figure 4-2)

A timing diagram illustrating the primary timing and control signals within the bootstrap, as well as the processor timing, is shown in Figure 4-2. The development of each signal is shown in the detailed logic.

4.9 DETAILED LOGIC DESCRIPTION

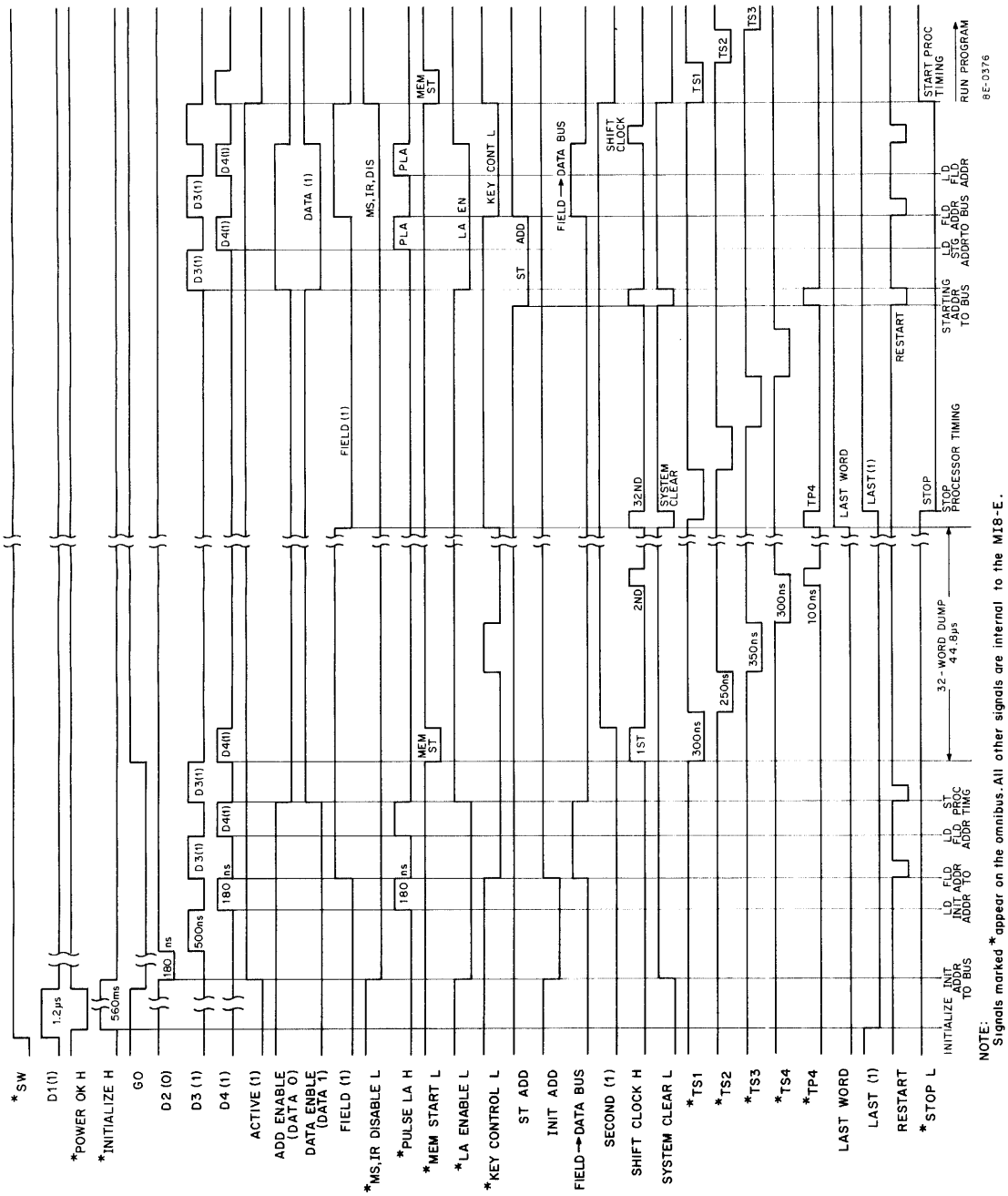
The following paragraphs present portions of the MI8-E logic. All illustrations are interrelated and, therefore, should be considered collectively. The sequential operation of each circuit is presented in the system description.

4.9.1 Bootstrap Timing Logic (Figure 4-3)

A timing chain is created in the timing logic by connecting, in series, four time-delay flip-flops designated D1 through D4. The 74123 IC has a retriggering characteristic that makes an automatic restart capability possible. However, the restart loop is concerned only with D3 and D4 and is controlled by the logical conditions of one flip-flop designated ACTIVE and a second flip-flop designated DATA.

Refer to Figure 4-4 for details about the 74123 IC. The restart operation makes use of the last line in the truth table, which states that the one-shot will initiate a timing cycle if the A and B inputs are enabled and the Master Reset input (C) is brought from low to high.

Again referring to Figure 4-3, the logic to the right of D1 is used to ground POWER OK H and serves to control the GO flip-flop. GO will set when D1 times out only if RUN L is not asserted (the machine is stopped). RUN L also prevents the bootstrap from grounding POWER OK H, which would otherwise stop the processor timing. Therefore, once the bootstrap is activated, GO remains set until processor timing begins. RUN L results and clears the GO flip-flop.



NOTE:
Signals marked * appear on the omnibus. All other signals are internal to the MI8-E.

Figure 4-2 Bootstrap Timing

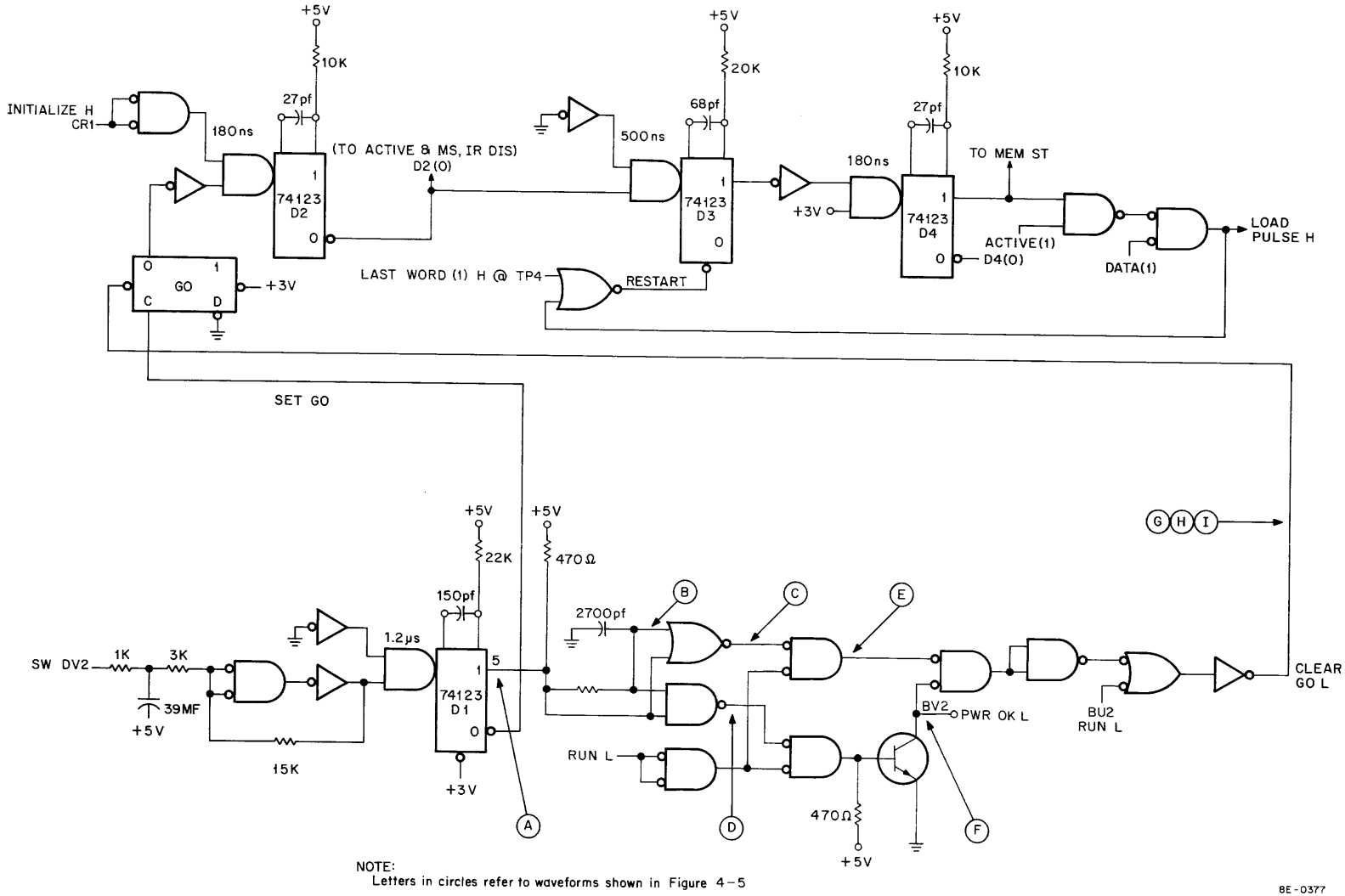
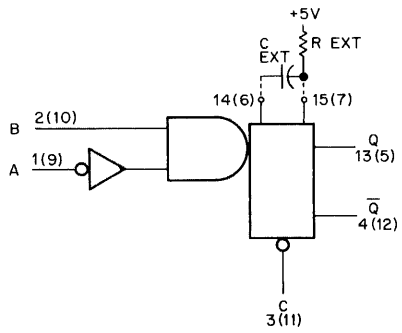


Figure 4-3 Bootstrap Timing Logic



NOTE:
Pin numbers not in parentheses are for delay 1; those within parentheses are for delay 2.

INPUTS			OUTPUTS	
A	B	C	Q	$\overline{Q}$
H	X	X	L	H
X	L	X	L	H
X	X	L	L	H
L	↑	H	⊓	⊓
↓	H	H	⊓	⊓
L	H	↑	⊓	⊓

↓ = TRANSITION FROM HIGH TO LOW

↑ = TRANSITION FROM LOW TO HIGH

⊓ = OUTPUT WAVEFORMS(DURATION DETERMINED BY THE R AND C ATTACHED TO THE ONE-SHOT)

8E-0378

Figure 4-4 74123 Logic Diagram and Truth Table

A positive-going transition on the SW line sets D1 for a period of 1.2 μs. On the input line, the RC network and feedback loop remove any switch contact bounce. On the output of D1 (1), the circuitry asserts POWER OK L (if RUN L is not asserted) and asserts CLEAR GO L when RUN L is asserted. Because CLEAR GO L is connected to the clear side of GO, the net result is:

a. If the computer is running, ignore the output of D1 (0).

b. If the computer is stopped and D1 triggers, set GO.

The conditions upon which CLEAR GO L is generated are shown graphically in Figure 4-5.

Signal POWER OK H goes low shortly after D1 (1) goes high. This causes the M8330 Timing Module to create a 560-ms INITIALIZE H pulse to clear the processor and options. In the meantime, D1 becomes reset because the 1.2-μs delay times out. This causes D1 (0) to go high; this transition clocks GO. GO (0) L half-qualifies the input to D2. At the end of the 560-ms INITIALIZE H pulse, the trailing edge sets D2 for a period of 180 ns. The D2 (0) negative-going output sets the ACTIVE flip-flop and the DEP flip-flop and the trailing edge of D2 (0) sets D3 for a period of 500 ns. At the trailing edge of D3 (1), the negative-going transition sets D4. A restart path beginning with D4 (1) H and gated by ACTIVE (1) H and DATA (1) L generates LOAD PULSE H. Signal LOAD PULSE H (trailing edge) clocks the FIELD flip-flop on the first pass and clocks the DATA flip-flop on the second pass. The trailing edge of each LOAD PULSE H causes D3 to start another timing cycle. Once the DATA flip-flop is clocked, DATA (1) H inhibits LOAD PULSE H and hence another restart operation until LAST is set (following the 32-word dump operation). The last D4 (1) H with DATA (1) H asserts MEM START L. MEM START L

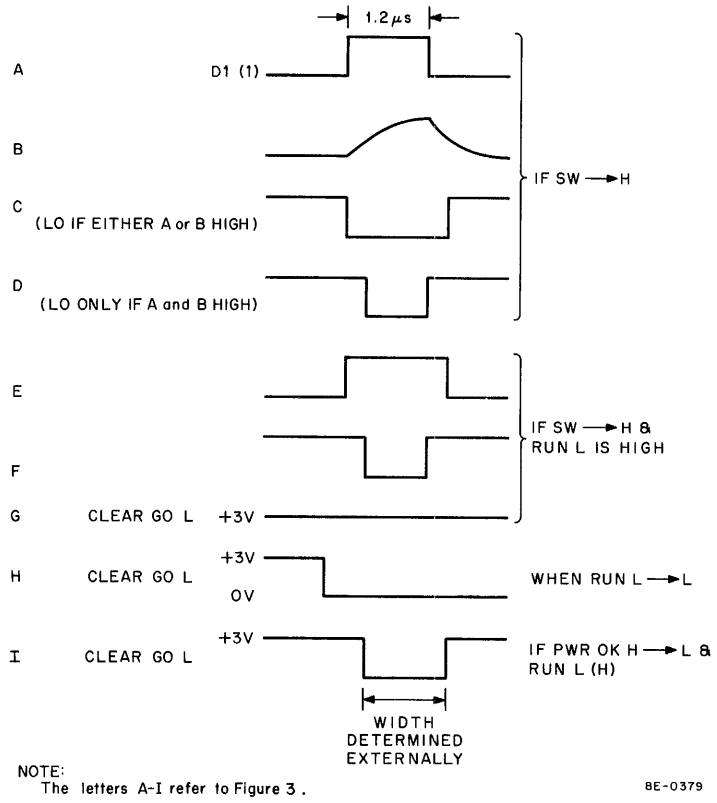


Figure 4-5 CLEAR GO Signal Waveform Analysis

asserts RUN L in the timing module and RUN L asserts CLEAR GO L, which then resets the GO flip-flop. The timing chain remains inactive until LAST WORD H sets the LAST flip-flop and with TP4 creates RESTART.

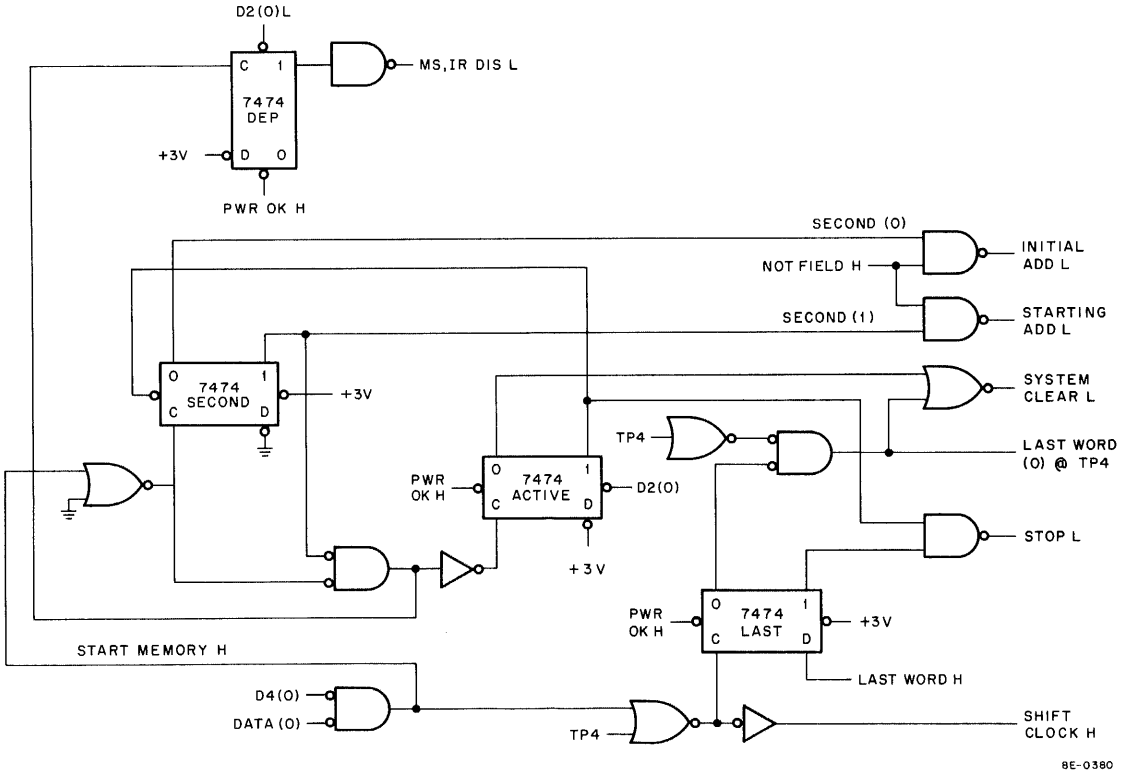
4.9.2 Bootstrap Control Logic (Figure 4-6a and b)

Four flip-flops are shown in Figure 4-6a. LAST, ACTIVE, and DEP are cleared by POWER OK H being low. ACTIVE (1) low clears SECOND. ACTIVE (0) now high generates SYSTEM CLEAR L. SYSTEM CLEAR L clears the FIELD flip-flop, the DATA flip-flop, and the 32-bit shift register.

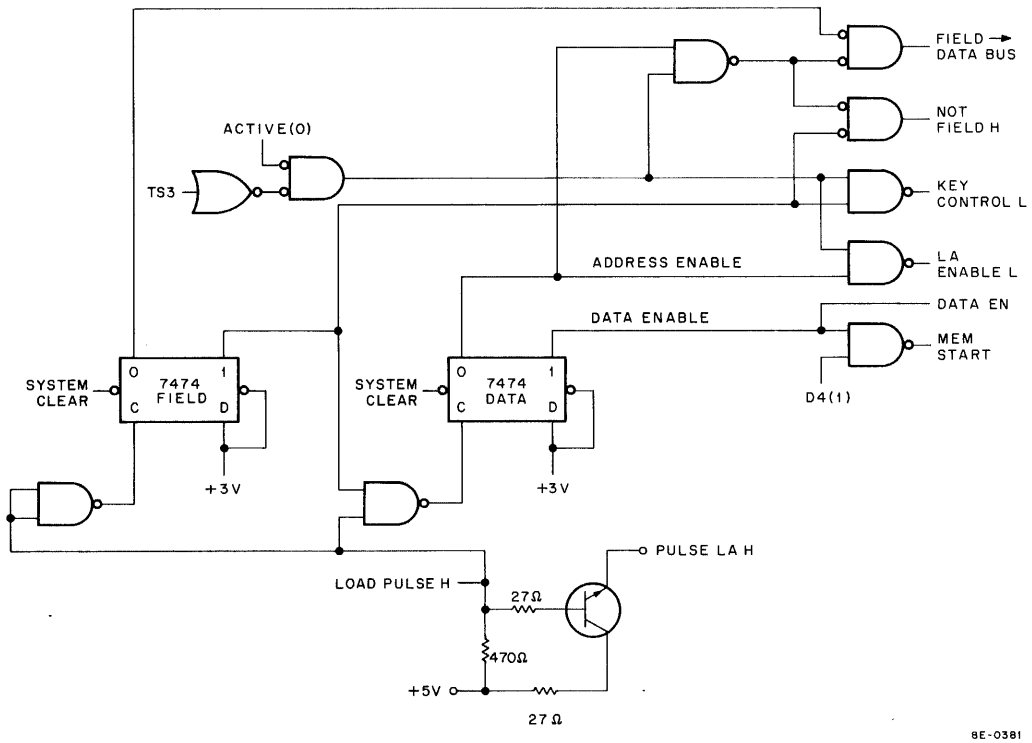
When the timing chain reaches D2, D2 (0) sets flip-flops DEP and ACTIVE. ACTIVE (1) H now half-qualifies STOP L and DEP (1) H generates MS, IR DISABLE L. FIELD (1) L and ACTIVE (0) L generate NOT FIELD H. This signal, combined with SECOND (0) H, asserts INITIAL ADD L. Signal ACTIVE (0) L, combined with DATA (0) H, asserts LA ENABLE L.

When the timing chain reaches D4 and generates LOAD PULSE H, PULSE LA H is asserted. This loads the initial address into the CPMA. When D4 times out (at the trailing edge of LOAD PULSE H), FIELD is clocked. FIELD (1) H half-qualifies the DATA flip-flop clock input and FIELD (0) L qualifies FIELD TO DATA BUS.

With FIELD set, ACTIVE set and DATA reset, FIELD TO DATA BUS, KEY CONTROL L and LA ENABLE L cause the memory field to be addressed. The trailing edge of LOAD PULSE H also asserts RESTART and the timing chain is again activated.



a.



b.

Figure 4-6 Bootstrap Control Logic

The next LOAD PULSE H at the trailing edge clocks the DATA flip-flop and again asserts RESTART. DATA (1) H now half-qualifies MEM START. When D4 is again set, D4 (1) asserts MEM START L. D4 (0) L, combined with DATA (0) L generates START MEMORY H and SHIFT CLOCK H. SECOND is clocked by the trailing edge of START MEMORY H in preparation for STARTING ADDRESS. Signal MEM START L starts the processor timing and SHIFT CLOCK H activates the 32-bit shift register. The 32-word dump operation now begins. Signal LAST WORD H is asserted when the 32nd word is reached. LAST is clocked at TP4 and LAST (1) qualifies STOP L. LAST (0) at TP4 asserts SYSTEM CLEAR L and restarts the timing chain. SYSTEM CLEAR L again clears flip-flops DATA and FIELD.

With SECOND set, the next address must be the starting address. When the starting address is loaded into the CPMA, the timing chain goes through two additional restarts for the field address and Memory Start. When MEM START L is again qualified, START MEMORY H is asserted. The trailing edge of START MEMORY H this time clocks the ACTIVE flip-flop and ACTIVE (0) asserts SYSTEM CLEAR L. This prevents a second 32-word dump and removes all bootstrap signals from the OMNIBUS.

4.9.3 Initial/Starting Address Jumper Network and Output Logic (Figure 4-7)

The initial and starting addresses, determined by jumpers I for initial address and S for starting address, provide a 12-bit word for each type of address. Removing a jumper causes a 1 of the corresponding bit to be placed onto the DATA BUS. Otherwise a 0 will be submitted. The 7235 IC multiplexer selects either the initial address or the starting address, depending upon which control line is asserted low.

4.9.4 Extended Memory Field Output Logic (Figure 4-8)

The extended memory field output logic is jumper-selectable to provide either a 1 or 0 on each corresponding bit. Signal FIELD → DATA BUS H, developed in the bootstrap control logic, is used to apply 1s and 0s to the DATA BUS.

4.9.5 12 x 32 Diode Matrix and Control Logic (Figure 4-9)

A partial illustration of the 12 x 32 diode matrix and control logic is shown in Figure 4-9. The diode matrix is arranged in 32 columns and 12 rows to accommodate 32 12-bit words. Each word is applied to the output logic gates by 8-bit parallel-out serial shift registers with the first word being applied by SHIFT CLOCK H during TS1. Four 74164 ICs, each providing 8 outputs, are used to sequentially bias the diodes corresponding to the selected row. Each time SHIFT CLOCK H is received, the 74164 IC shifts to the next sequential output line. Carry to the next IC is accomplished by the last IC output line, except for the output line labeled "31". When 31 has been reached, LAST WORD H is generated and applied to the LAST flip-flop. Signal SYSTEM CLEAR L is generated in the control logic to clear the shift registers.

SECTION 5 MAINTENANCE

The general procedures concerning preventive and corrective maintenance are given in Chapter 4, Volume 1. When corrective maintenance is required, the technician should use the maintenance program given in Section 2 of this chapter to determine the nature of the problem.

4.10 TROUBLESHOOTING

The option schematic, drawing number E-CS-M847-0-1, must be referred to for IC locations and pin numbers. Test points are provided on the module to facilitate troubleshooting.

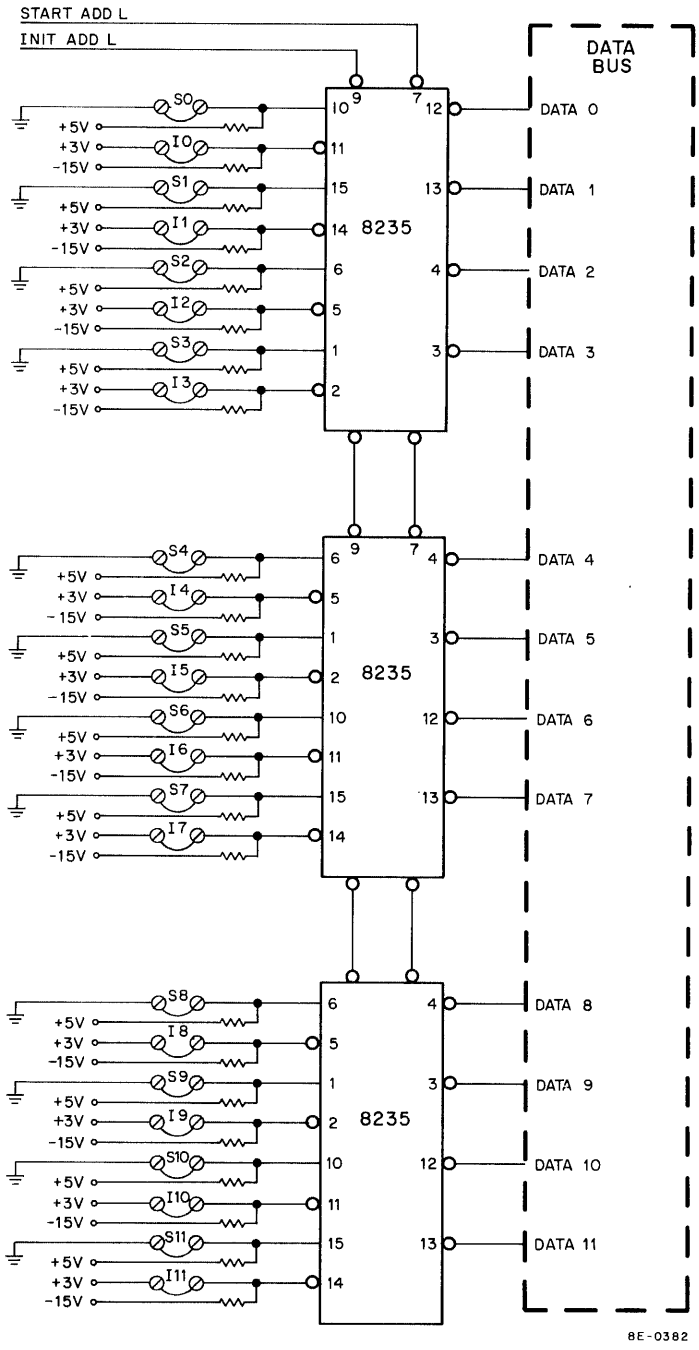


Figure 4-7 Initial/Starting Address Jumper Network

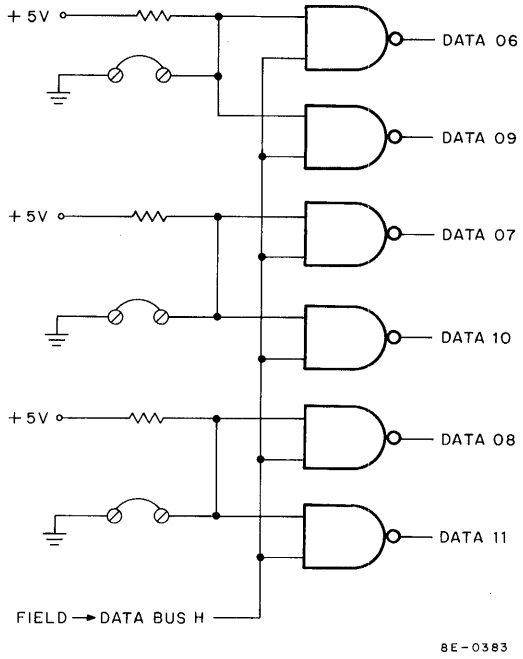


Figure 4-8 Extended Memory Field Output Logic

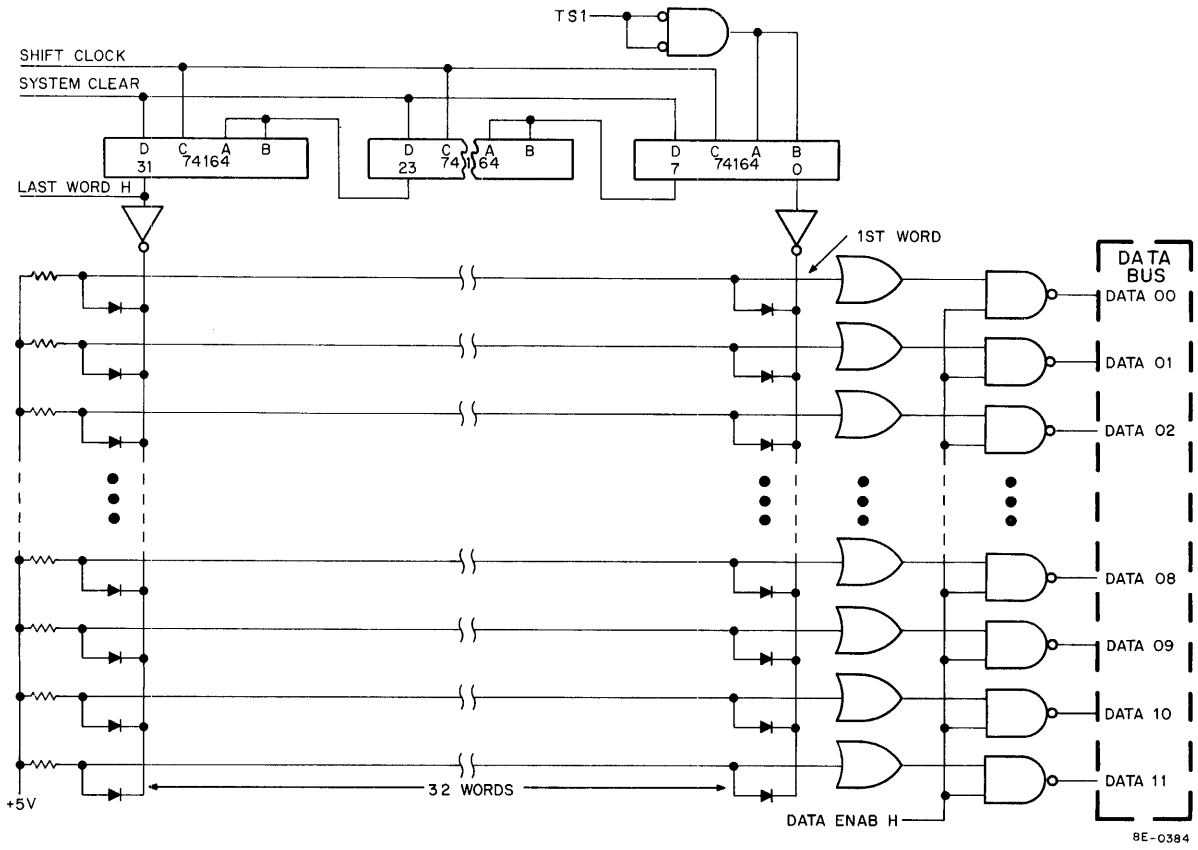


Figure 4-9 12 X 32 Diode Matrix

4.10.1 MI8-E Bootstrap Diagnostic Program

The operation of the MI8-E Bootstrap Loader should first be verified by the MI8-E Bootstrap Diagnostic Program, MAINDEC-8E-D11A-D, with corresponding MAINDEC operating procedures.

4.10.2 Direct Memory Access Control Signal Verification

Because the bootstrap loader uses direct memory access control signals in a manner similar to the operator's console (front panel), addressing memory and depositing information must be accomplished in the same manner. Proper operation of signals such as PULSE LA H, LA ENABLE L, KEY CONTROL L, MEM START L, and STOP L can be verified by performing the following procedure at the programmer's console:

Step	Procedure
1	Load Address 7777.
2	Load Address 0000.
3	Load Extended Address 7.
4	Load Extended Address 0.
5	Deposit bit 11, then 10 . . . 0 individually.
6	MA should equal 0014.
7	Load Address 0000.
8	Exam. You should see bit 11, then 10 . . . 0 until the MA = 0014.
9	Turn Rotary Switch to the state position.
10	Depress and hold LOAD ADDRESS. No major state should be lit (F,D,E).
11	Put SW up. SW indicator should be off.
12	Put SW down. SW indicator should be on.
13	Deposit in location 0/7240 1/7402.
14	Load and start location 0.
15	Turn Rotary Switch to AC position. AC should = 7777.
16	Depress CLEAR. AC should = 0000.
17	Load location 0. Deposit 5000.
18	Load and start location 0. Run light should be on.
19	Depress SINGLE STEP. Run light should be out.

If the above procedures were completed successfully, the problem is in the MI8-E Bootstrap Loader hardware. If the procedures indicate a malfunction, the MI8-E should be removed and the procedure tried again; the problem is in the programmer's console, the CPU or the Memory Extension Control.

4.11 BOOTSTRAP HARDWARE TROUBLESHOOTING ANALYSIS

A very convenient troubleshooting aid is the Programmer's Console Status Display. The mere presence or absence of any one of the addresses used in the Bootstrap Loader option can localize the problem by the process of

elimination. If the problem is that the option fails to continue after the initial address is loaded and the RUN lamp does not come on, the probable cause is the FIELD flip-flop or associated circuitry. However, if the field address is loaded but the RUN lamp does not come on, the probable cause is the ENABLE flip-flop or associated circuitry. It can be assumed that all of the logic leading up to the logic that controls MEM START functions properly.

If the RUN lamp comes on but the 32-word dump operation does not begin, it can be assumed that the DATA flip-flop functions and the problem is somewhere in the 12 x 32 diode matrix logic. No dump might indicate that the first shift register is malfunctioning.

If the RUN lamp comes on and the dump operation takes place but then fails to stop, the problem is in the Shift Register or LAST flip-flop. The problem also causes the most-significant MA lights to run at half intensity. Examination of memory shows that all locations have been cleared. The reason for the failure is that the single 1 which should shift down the 32-bit shift register has been lost, probably because of a malfunctioning 74164 IC.

A malfunction will also occur if a 74164 IC picks up a bit. In this situation, fewer than 32 words will be deposited. Some of these words will be the OR of two or more of the words encoded in the diode matrix.

When an incorrect word is deposited, the faulty diode can be located by determining which word and bit fails. This is easily accomplished by addressing the bootstrap initial address and depressing the EXAM key. When the rotary switch is in the MD position, each of the 32-bit words can be examined.

If bootstrap timing operates properly, the SINGLE STEP and CONTINUE keys may be used to single-step the bootstrap. This technique may be used to find out if data is being deposited correctly.

SECTION 6 SPARE PARTS

Table 4-2 lists the recommended spare parts for the MI8-E. These parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

Table 4-2
Recommended MI8-E (M847) Spare Parts

DEC Part No.	Description	Quantity
19-10436	IC DEC 74123	1
19-09004	IC DEC 7402	1
19-05547	IC DEC 7474	1
19-09935	IC DEC 8235	1
19-10041	IC DEC 74164	1
19-05575	IC DEC 7400	1
19-09705	IC DEC 8881	2
19-09686	IC DEC 7404	2
19-09485	IC DEC 380	1
19-09486	IC DEC 384	1
15-03100	Transistor DEC 3009B	1
11-00114	Diode D664	10
13-01423	Resistor 6.8K, 1/4W, 5%	2
10-00006	Cap., 0.01 μF, 100V, 20%	2