CHAPTER 7
KP8-E POWER-FAIL AND AUTO-RESTART

SECTION 1 INTRODUCTION

The KP8-E Power-Fail and Auto-Restart option monitors the computer's primary power source and initiates a controlled shut-down sequence if a power failure occurs. This power-fail sequence protects the operating program by storing the contents of the PC Register, AC Register, MQ Register, and the Link in known memory locations. When normal primary power is restored, the KP8-E automatically restarts the computer in location 0000.

The Power-Fail and Auto-Restart option consists of the M848 quad module which is inserted into the OMNIBUS and connected to the computer ac power supply by a 7007128 power cable. The PDP-8/E supplies 28 Vac and the PDP-8/F and PDP-8/M supply 56 Vac. The 56 Vac input is reduced to 28 Vac by removing a jumper (W2) on the M848 module.

SECTION 2 M848 BLOCK DIAGRAM

The KP8-E block diagram is shown in Figure 7-1. The power monitor logic checks the PDP-8/E power supply 28 Vac output or the PDP-8/F and PDP-8/M 56 Vac power supply output which reflects the condition of the primary power source. If line voltage drops below a predetermined minimum value, the UP signal is negated and the PWR LOW flip-flop is set, asserting the OMNIBUS INT RQST L signal. Filter capacitors in the power supply guarantee continued operation for 1 ms; this is sufficient time for the interrupt request to be recognized and the program interrupt routine to be carried out (because of the time limitation, the KP8-E SPL instruction, Skip on PWR LOW flag, 6102, should be the first status check made by the program interrupt routine).

SECTION 3 M848 DETAILED LOGIC

7.1 SELECT LOGIC

The select logic is shown in Figure 7-2. When the SPL instruction (6102) is decoded, the logic asserts the INTERNAL I/O L signal that causes the positive I/O bus interface to ignore the IOT instructions. The status of the PWR LOW flip-flop is checked; if the flag is set, indicating a power failure has occurred, the SKIP L signal is asserted. The program then skips the next sequential instruction and jumps to a subroutine that begins executing the power-fail routine.

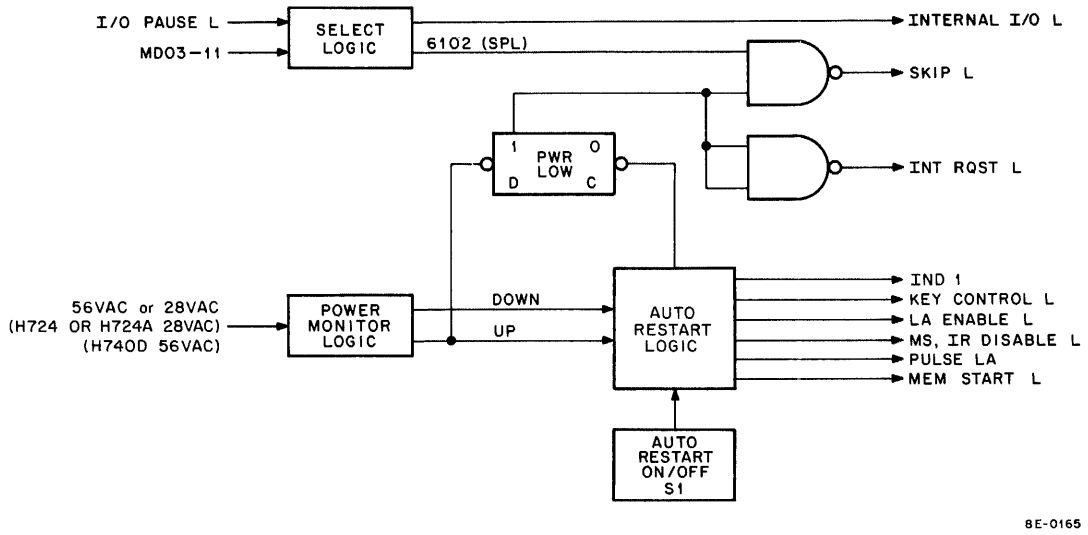


Figure 7-1 M848 Power Fail and Auto-Restart Option, Block Diagram

7.2 POWER MONITOR LOGIC

The power monitor logic is shown in Figure 7-3. The logic directly monitors the ac output of the computer's power supply, to which the option is connected by a cable. The cable connects to the option with an 8-pin connector (2 pins are not used). Each ac input at J1 is wired via the board etch to an adjacent pin so that the ac is not dead-ended (the DK8-E Real-Time Clock option (line frequency) also uses the ac output of the power supply; if both options are in the system, one is connected directly to the power supply while the second is connected to J1 of the first).

NOTE

The W2 jumper must be removed when the KP8-E is installed in a PDP-8/F or PDP-8/M.

The ac is full-wave rectified and applied to two comparator circuits. One of these circuits includes transistor pair Q4/Q5 and initiates the auto-restart sequence. The second circuit includes transistor pair Q2/Q3 and initiates the power-fail sequence. There are two thresholds for power fail. An upper threshold, 105 Vac, that is used to start the RESTART logic, and a lower threshold, 95 Vac, that sets the PWR LOW flip-flop. Q4 and Q5 detect the 105 Vac threshold; Q2 and Q3 detect the 95 Vac threshold. The upper and lower thresholds have a tolerance of ±15%. Q2 provides a trigger for one-shot E7 when the amplitude of the line voltage, and hence, the amplitude of the ac input of J1, is above the desired minimum. The -10.3 Vdc reference voltage is generated by a precision voltage regulator that is not shown (see the option schematic for this and for resistor values).

Figure 7-4 presents idealized waveforms to illustrate how E7 is controlled by the comparator circuit. If the line voltage is above the selected minimum value, the positive transition at the collector of Q2 will be of sufficient amplitude to trigger E7. Because the period of the collector waveform is less than the triggered delay time of E7, the one-shot will remain active. If the line voltage falls below the minimum value for as little as one-half cycle, as illustrated, E7 times out and an interrupt request is generated. Even though the power recovers almost instantaneously, the power-fail sequence is carried out.

The timing diagram shows the UP signal being asserted by the half-cycle immediately following the missing half-cycle. Thus, the auto-restart sequence begins 1500 ms later, as detailed in the following paragraphs.

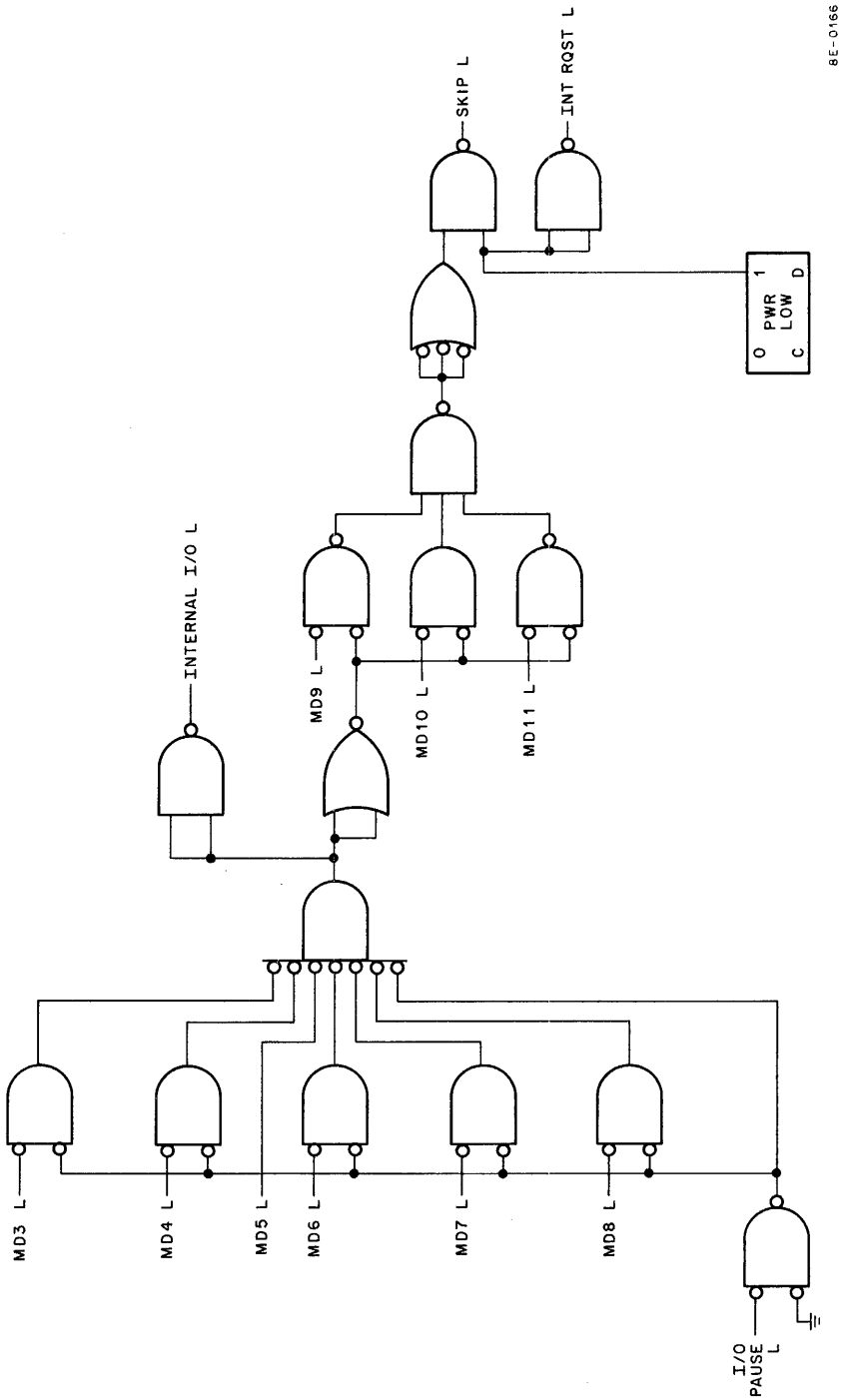


Figure 7-2 Select Logic

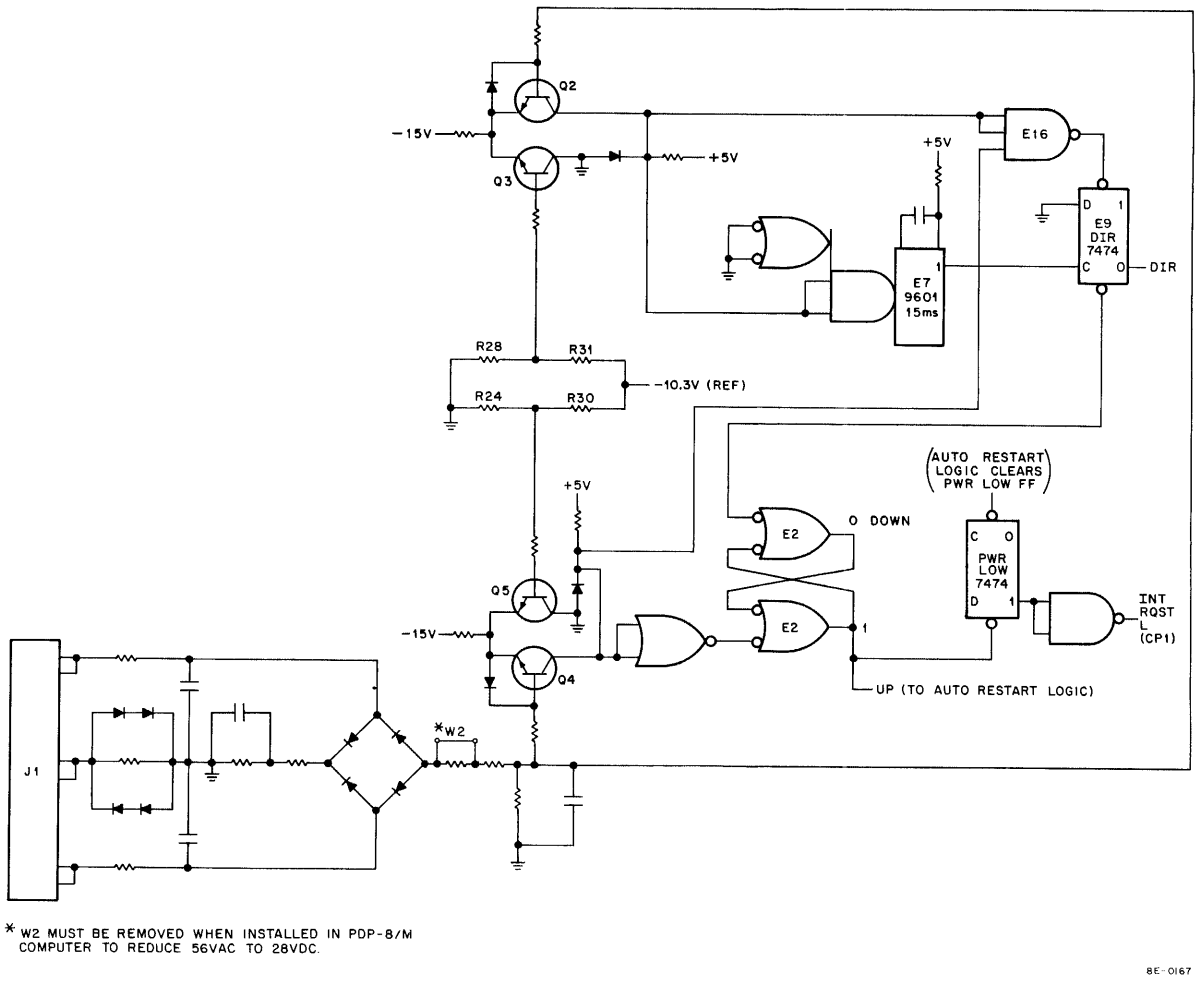


Figure 7-3 Power Monitor Logic

7.3 AUTO-RESTART LOGIC

The computer must resume operation by executing the instruction that was stored in location 0000, field 0, by the power-fail routine. Consequently, the CPMA Register and the IF and DF Registers of the KM8-E option must be loaded with 0s before CPU timing is renewed. Furthermore, the CPU Major State Register must be manipulated so that a FETCH cycle is entered when timing begins. The auto-restart logic meets these requirements by simulating some of the operations that normally occur when the programmer's console is being used.

Thus, to load the CPMA Register with 0s, the auto-restart logic first asserts the LA ENABLE L signal (at the same time, the MS, IR DISABLE L signal is asserted; this signal places the CPU in the DMA state, ensuring that the first timing cycle begins in the FETCH state). The LA ENABLE L signal:

a. ensures that only "bus" information is placed on the DATA 0-11 lines; because nothing has access to "bus" at this time, the DATA 0-11 lines carry 0s (Volume 1, Section 5, Paragraph 3.3.3, for clarification);

b. causes the 0s on the DATA 0-11 lines to be gated through the CPU Major Register gating to the MAJOR REGISTERS BUS.

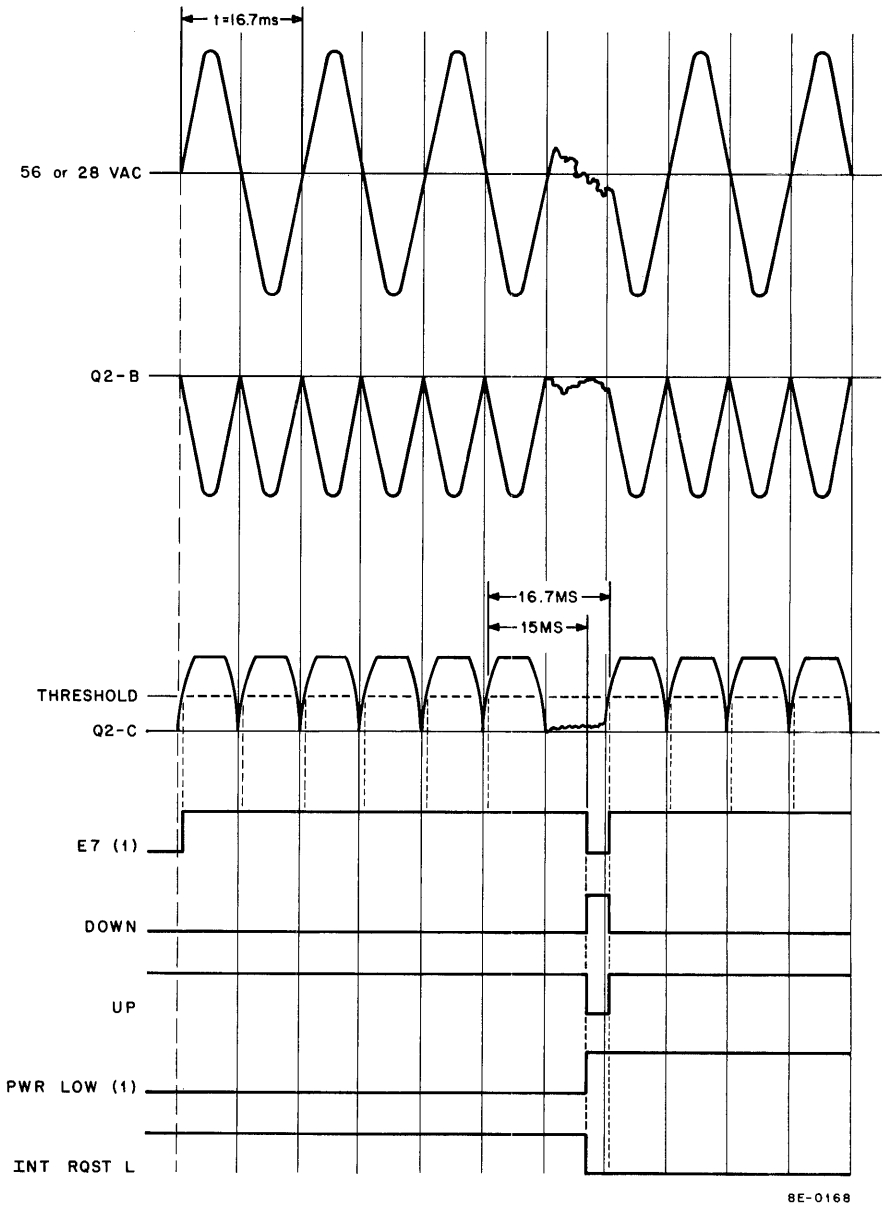


Figure 7-4 Power Fail Timing

After a delay to ensure that the control lines have settled, the logic asserts PULSE LA. This signal causes the CPU to generate the CPMA LOAD L signal that loads the CPMA Register with address 0000. CPMA LOAD L also sets the F flip-flop of the Major State Register; thus, a FETCH cycle will be entered when timing begins. IND1 is asserted at the same time as LA ENABLE to ensure only 0s are on the bus if the programmer's console is not installed (Volume 1, Paragraph 3.33.10).

When the CPMA Register has been loaded and the F flip-flop set, the auto-restart logic asserts the KEY CONTROL L signal. After a delay that enables the control line to settle, PULSE LA is asserted again. However, because KEY CONTROL L is true, CPMA LOAD L is not generated by this assertion of PULSE LA, nor is the Major State Register clocked.

Rather, the 0s on the DATA 0-11 lines are loaded into the IF and DR Registers of the KM8-E option (the auto-restart logic allows for the KM8-E option even if the option is not contained in the system). After this assertion of the PULSE LA signal, the MS, IR DISABLE L, IND1, and LA ENABLE L signals are negated and a final delay period is allowed. When this delay times out, MEM START L is asserted, initiating CPU timing, and the computer fetches the instruction from location 0000.

The auto-restart logic is shown in Figure 7-5; the relative timing of the logic is shown in Figure 7-6. The ENABLE/DISABLE switch, S1, must be in the ENABLE position (up) if the automatic restart is to function after a power interrupt has occurred. If S1 is in the DISABLE position, the PWR LOW flip-flop is cleared when ac power comes up, but the program must be restarted manually.

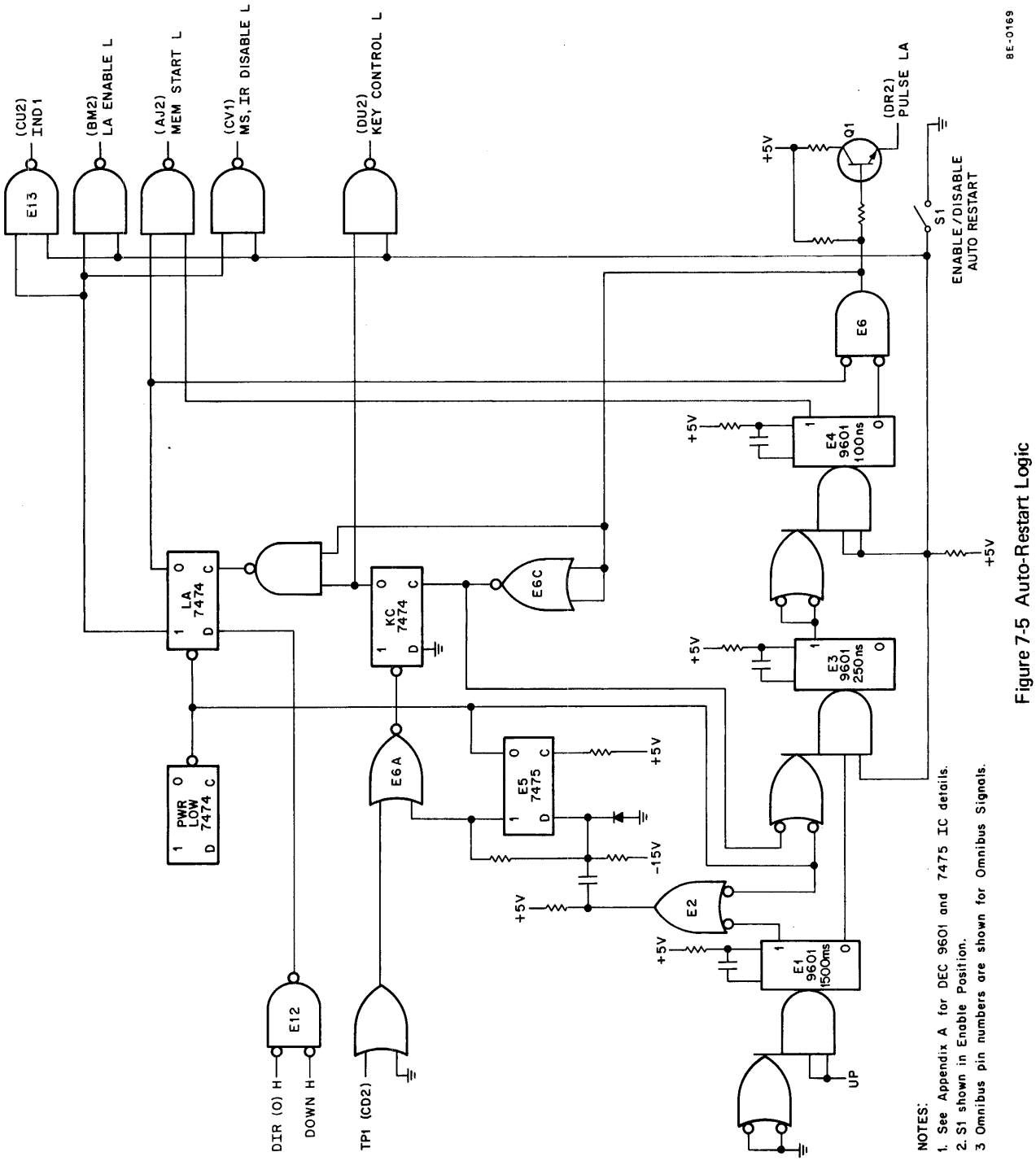
The auto-restart sequence begins when the power monitor logic asserts the UP signal. The positive transition of this signal triggers one-shot multivibrator E1. During the active 1500 ms of this one-shot, all system equipment (computer, peripherals, options) can complete operations initiated by the OMNIBUS INITIALIZE signal. At the end of the 1500 ms delay, bistable latch E5 is triggered and the LA flip-flop is set. This latch sets the KC (key control) flip-flop, clears the PWR LOW flip-flop, and triggers the E3 one-shot (the 0-output of E1 provides a required high signal at one input of E3; as the timing diagram illustrates, this high precedes the E3 trigger signal by an appreciable amount of time). The 1-output of the LA flip-flop asserts the LA ENABLE L, IND1 and MS, IR DISABLE L signals. The E3 one-shot, when it times out after 250 ns, triggers one-shot E4, which is active for 100 ns. During the 100 ns period, NAND gate E6 is enabled and PULSE LA is asserted. Thus, the CPMA Register is loaded and the FETCH flip-flop is set. The E3 one-shot is retriggered, via NOR gate E6C, coincidently with the leading edge of the PULSE LA signal; while the KC flip-flop is cleared 100 ns later to assert the KEY CONTROL L signal. When E3 times out the second time, PULSE LA is produced again. Thus, the IF and DF Registers are loaded at this time. As before, E3 is retriggered coincidently with the leading edge of PULSE LA. At the end of PULSE LA, when E4 times out for the second time, the LA flip-flop is cleared, and LA ENABLE L and MS, IR DISABLE L are negated.

When E3 times out for the third time, it once again triggers E4. However, because the LA flip-flop is now clear, no PULSE LA signal is produced. Instead, the 1-output of E4 asserts MEM START L and CPU timing begins by fetching the instruction in location 0000. At TP1 time of this FETCH cycle, the KC flip-flop is set by NOR gate E6A and the KEY CONTROL L signal is negated.

The DIR (Direction) flip-flop ensures that a Restart Sequence is initiated only when ac voltage is rising, through the Restart threshold, toward normal line Voltage Condition.

SECTION 4 MAINTENANCE

General instructions concerning preventive and corrective maintenance are given in Volume 1, Chapter 4. When corrective maintenance is required, the technician should use the maintenance program, MAINDEC-8E-DOKC-D (D), to determine the nature of the problem. The option schematic, drawing no. E-CS-M848-0-1, must be referred to for IC locations and pin numbers. Tests points have been provided on the option to facilitate troubleshooting.



NOTES:
1. See Appendix A for DEC 9601 and 7475 IC details.
2. S1 shown in Enable Position.
3 Omnibus pin numbers are shown for Omnibus Signals.

Figure 7-5 Auto-Restart Logic

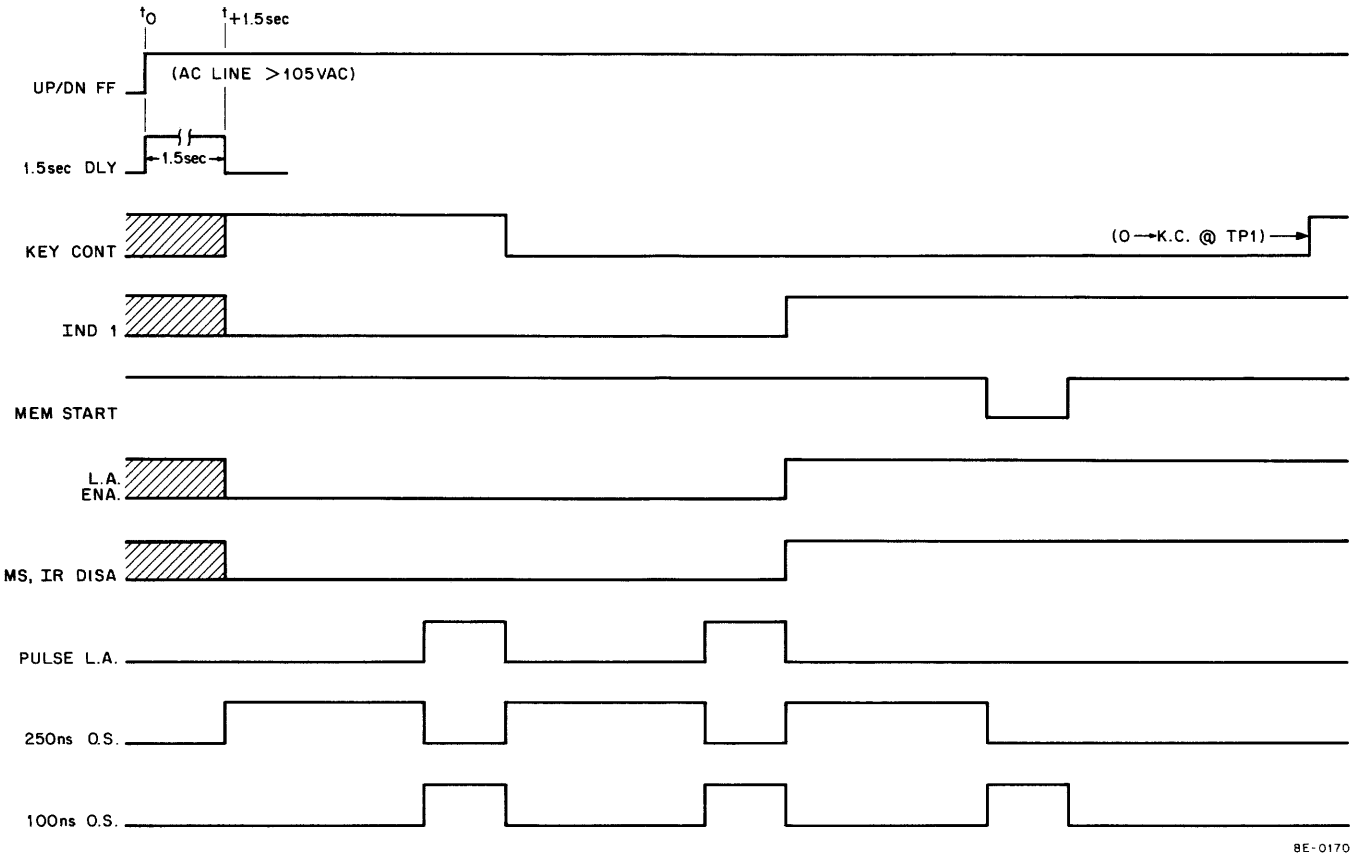


Figure 7-6 Auto-Restart Timing

SECTION 5 SPARE PARTS

Table 7-1 lists recommended spare parts for the KP8-E. These parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

Table 7-1

Recommended KP8-E Spare Parts

DEC Part Number	Description	Quantity
11-09991	Diode, AZ1-1/4M, 6.8V	1
11-00114	Diode, D664	1
11-00275	Diode, D672	1
15-03100	Transistor, 3009B	1
15-03409-01	Transistor, DEC 6534B	1
19-05547	IC DEC 7474	1
19-05575	IC DEC 7400	1
19-05576	IC DEC 7410	1
19-09004	IC DEC 7402	1
19-09050	IC DEC 7475	1
19-09373	IC DEC 9601	1
19-09486	IC DEC 384	1
19-09705	IC DEC 8881	1
19-09971	IC DEC 6380	1
19-09972	IC DEC 6314	1