

MASTER DRAWING LIST

MAINTENANCE MANUALS		UNIT VARIATIONS													
NO.	TITLE	KK8-E													
KK8-E	CENT. PROC.	X													

USED ON OPTIONS											
PDP8/E											
PDP8/M											
PDP8/i											

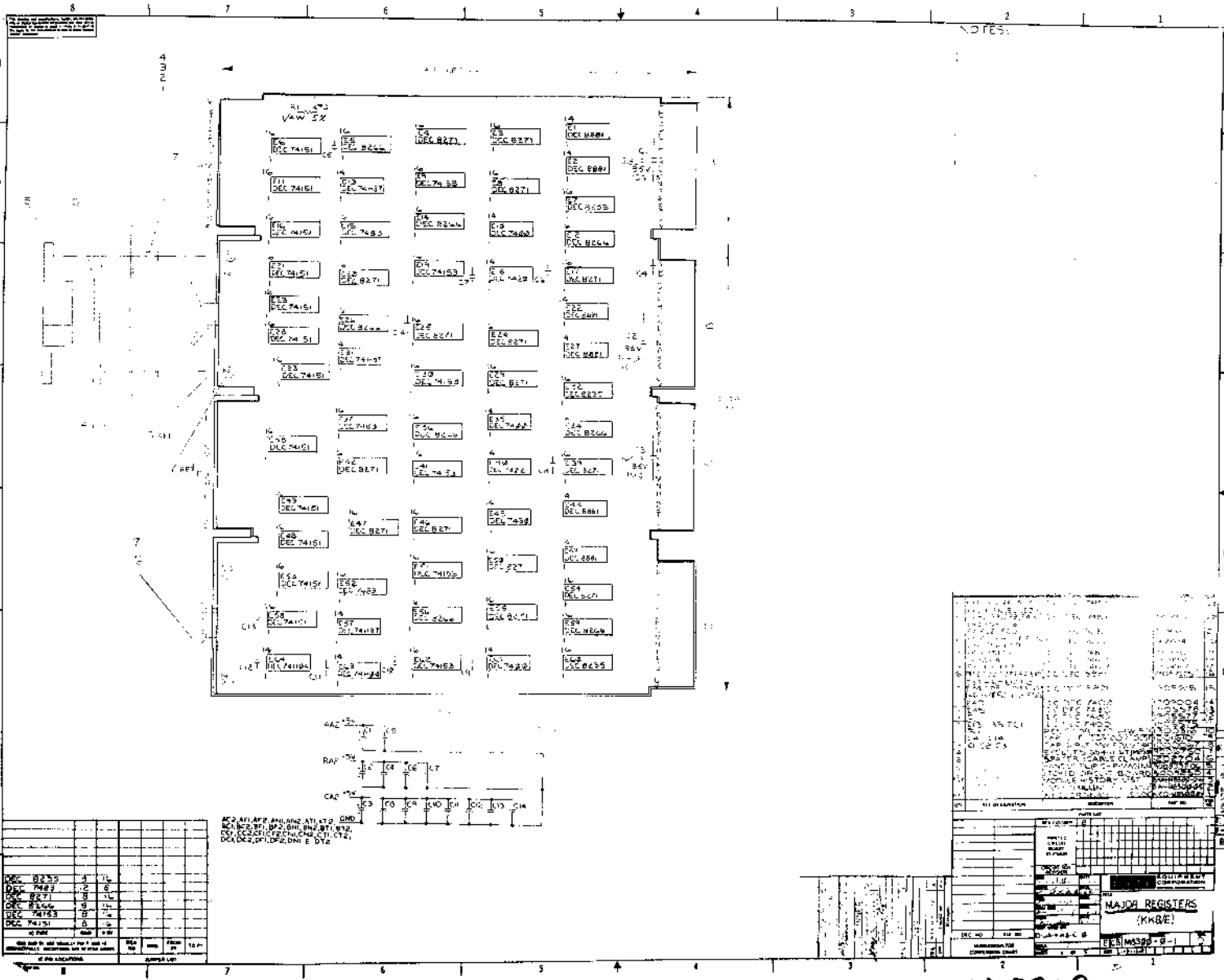
REV.	DATE	CHG. NO.	APPD.	DRN.	DATE	 DIGITAL EQUIPMENT CORPORATION <small>MAYNARD, MASSACHUSETTS</small>						TITLE
A	1/71	KK8E-1	D.C.	K. GULICK	12/28/70							CENTRAL PROCESSOR (KK8-E)
B	3/71	KK8E-2	R.V.	K. GULICK	12/29/70							
C	4/71	KK8E-3	L.K.	L. KLOTZ	12/71							
D	5/71	MB33-6	L.N.	PROJ. ENG. VOGELSANG	12/71							
E	7/71	MISC-86	A.V.	PROD. L. SAYLOR	13/71							
F	1/72	8E-55	J.C.									
H	10/73	KK8E-4	J.K.									
J	12/74	KK8E-5										

FIRST USED ON	SIZE	CODE	NUMBER	REV.
A-ML-PDP8 E-Ø	A	ML	KK8-E	J
SCALE #				
SHEET 1 OF 2				

REV.	DATE	CHG. NO.	APPD.	DRN.	DATE	 DIGITAL EQUIPMENT CORPORATION <small>MAYNARD, MASSACHUSETTS</small>						TITLE							
X				E-CS-M8300-Ø-1	#							5	CENTRAL PROCESSOR (KK8-E)						
Y				F-CS-M8310-Ø-1	#	4	CENTRAL PROCESSOR (KK8-E)												
X				E-CS-M8320-Ø-1	#	2													CENTRAL PROCESSOR (KK8-E)
X				E-CS-M8330-Ø-1	#	2							CENTRAL PROCESSOR (KK8-E)						
X				B-CS-M840-Ø-1	#	1	CENTRAL PROCESSOR (KK8-E)												
																			CENTRAL PROCESSOR (KK8-E)
X				D-UA-KK8-E-Ø	C	1							CENTRAL PROCESSOR (KK8-E)						
							CENTRAL PROCESSOR (KK8-E)												
X				A-SP-KK8-E-1	B	3													CENTRAL PROCESSOR (KK8-E)

PRINT SET	DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE	OPTION NO.
X	E-CS-M8300-Ø-1	#	5	MAJOR REGISTERS	
Y	F-CS-M8310-Ø-1	#	4	MAJOR REGISTER CONTROL	
X	E-CS-M8320-Ø-1	#	2	BUS LOADS	
X	E-CS-M8330-Ø-1	#	2	TIMING GENERATOR	
X	B-CS-M840-Ø-1	#	1	RFI SHIELD	
X	D-UA-KK8-E-Ø	C	1	CENTRAL PROCESSOR	
X	A-SP-KK8-E-1	B	3	ENGINEERING SPECIFICATIONS	

TITLE	SIZE	CODE	NUMBER	REV.
CENTRAL PROCESSOR KK8-E	A	ML	KK8-E	J
SHEET 2 OF 2				



NOTES:

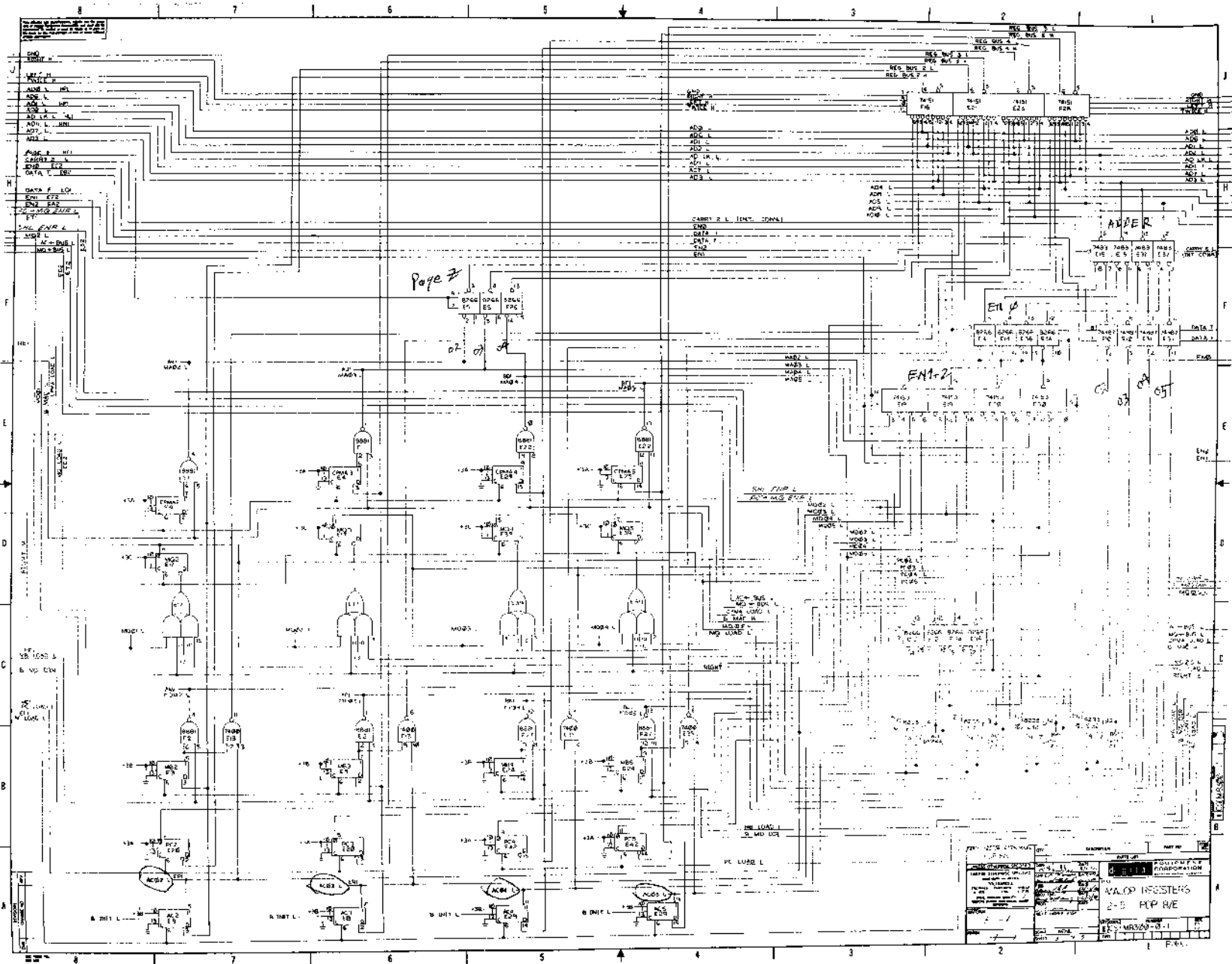
NO.	DESCRIPTION	QTY	UNIT	AMOUNT
DEC 8255	A	1	TL	
DEC 7487	B	2	B	
DEC 8271	B	1	TL	
DEC 8266	B	1	TL	
DEC 74153	D	1	TL	
DEC 74151	D	1	TL	

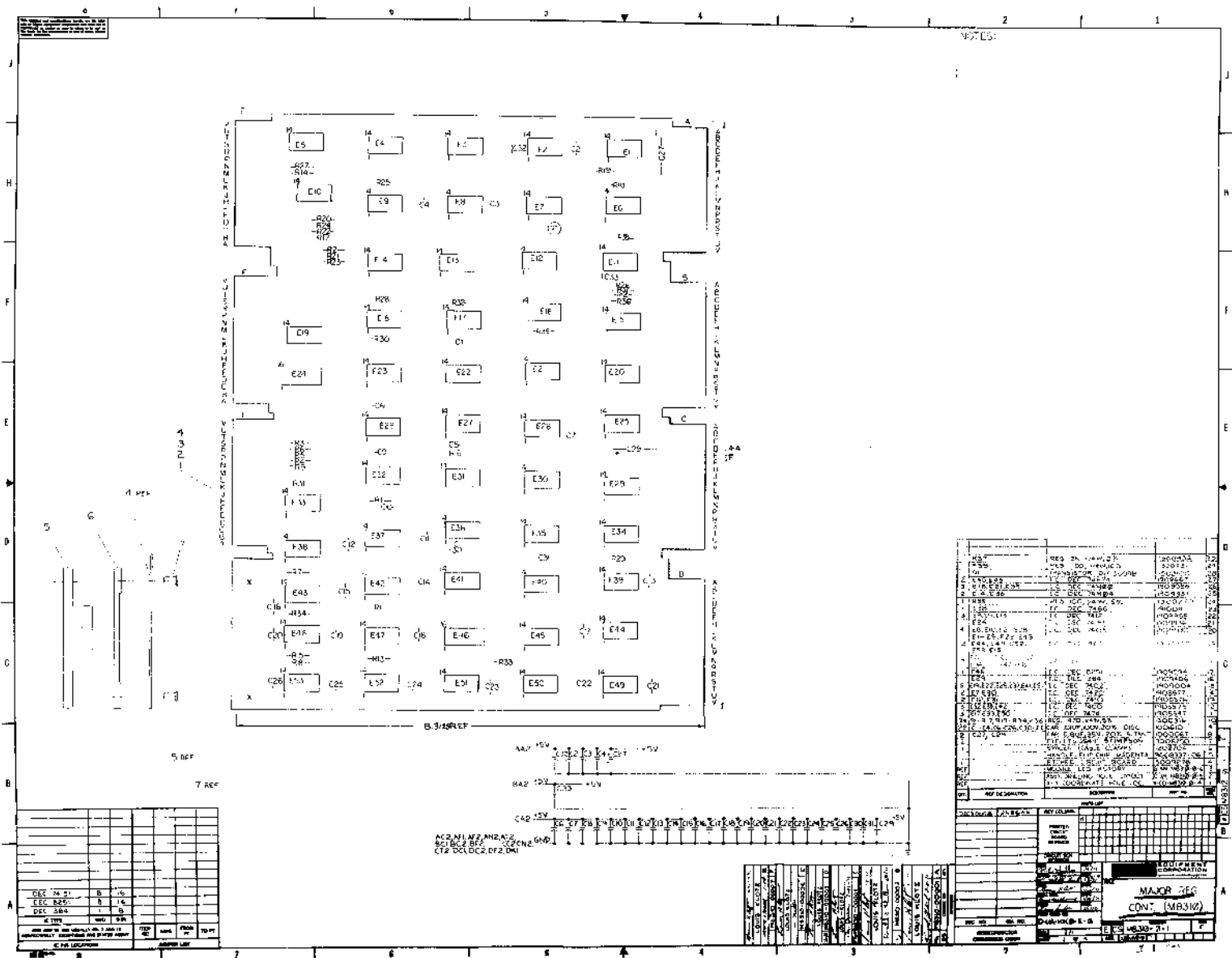
AC2, AT1, AF2, AN1, AN2, AT1, AT2, DND
 AC1, BC2, BT1, BT2, BN1, BN2, BT1, BT2,
 CT1, EC1, EC2, EC3, EC4, EC5, CT1, CT2,
 DC1, DC2, DF1, DF2, DN1, E, DT1

EQUIPMENT
 MAJOR REGISTERS
 (KRB/E)
 ESI 103398-8

11-8300

Getting Form
R.3, A, S





NOTES:

1. SEE PLAN FOR ROOM SCHEDULES
2. SEE PLAN FOR ROOM SCHEDULES
3. SEE PLAN FOR ROOM SCHEDULES
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NO.	DESCRIPTION	DATE	BY	CHKD.
1	REVISED	11/14/54
2	REVISED	11/14/54
3	REVISED	11/14/54
4	REVISED	11/14/54
5	REVISED	11/14/54
6	REVISED	11/14/54
7	REVISED	11/14/54
8	REVISED	11/14/54
9	REVISED	11/14/54
10	REVISED	11/14/54

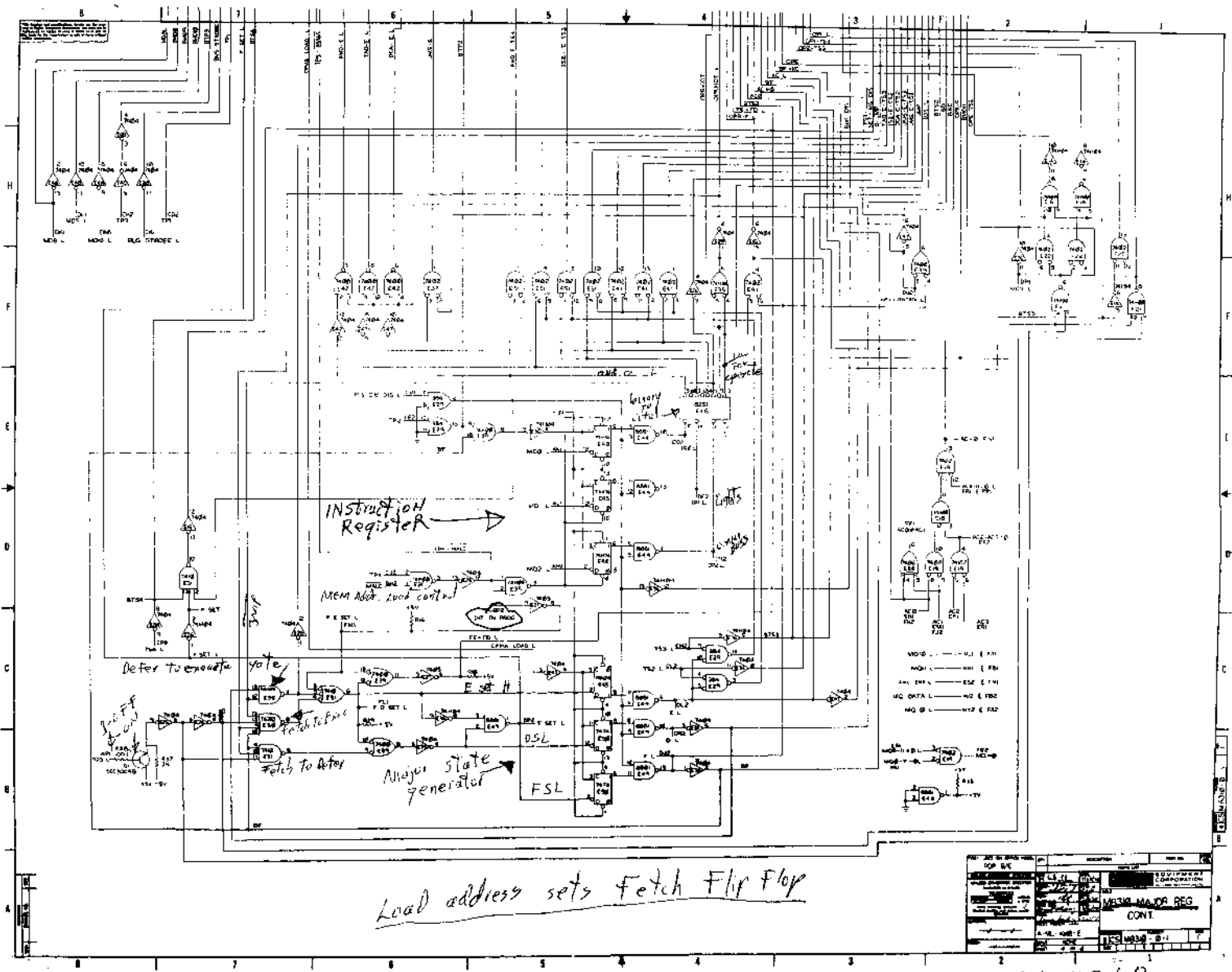
ACR:NL1FZ,ANR:AZ
 SC1BC2,BF2
 CT2 DCLDC2,DF2,DN1

NO.	DESCRIPTION	DATE	BY	CHKD.
1	REVISED	11/14/54
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5	REVISED	11/14/54
6	REVISED	11/14/54
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8	REVISED	11/14/54
9	REVISED	11/14/54
10	REVISED	11/14/54

NO.	DESCRIPTION	DATE	BY	CHKD.
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7	REVISED	11/14/54
8	REVISED	11/14/54
9	REVISED	11/14/54
10	REVISED	11/14/54

MAJOR REC
 CONT. (MBS102)

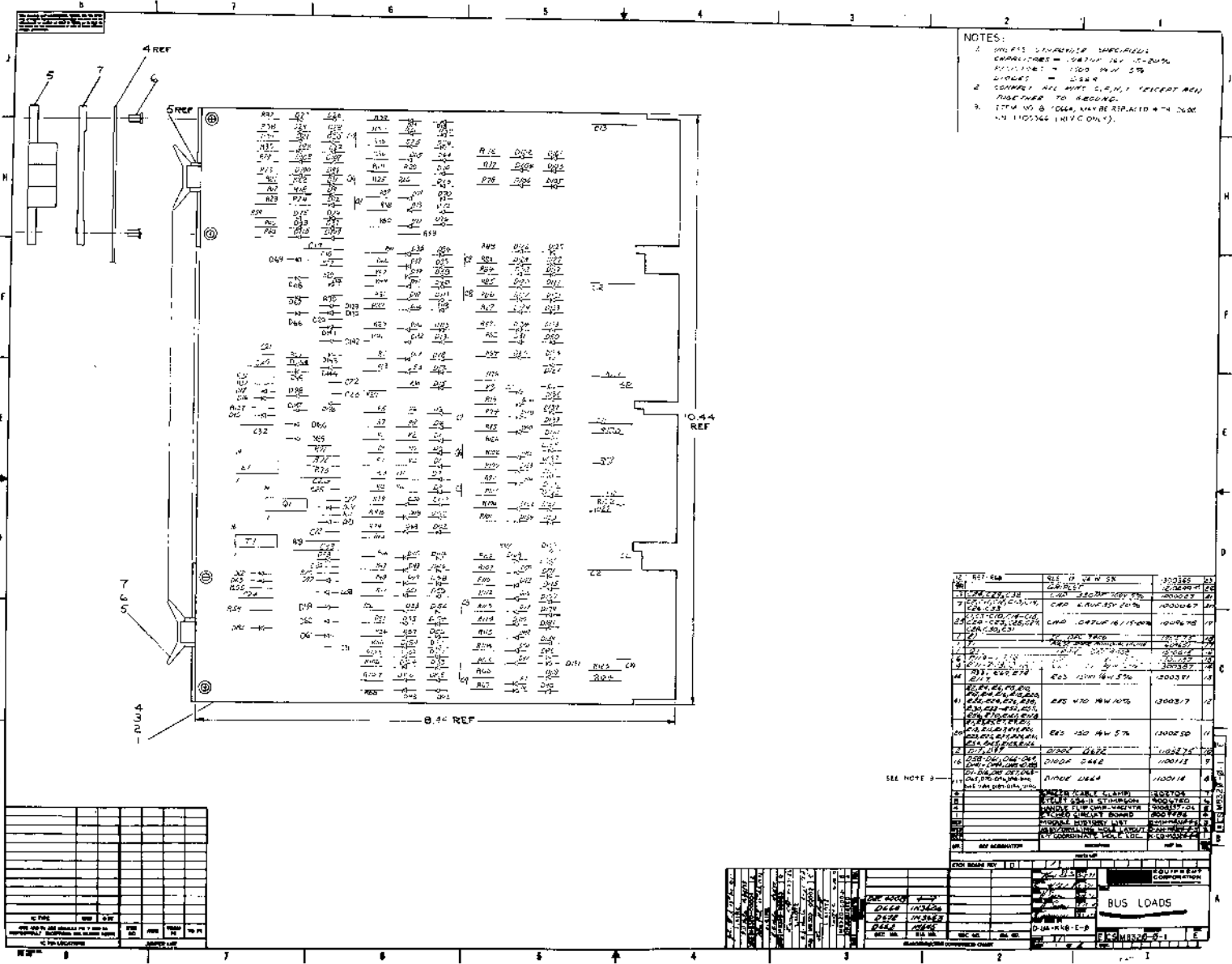
Engineering Drawing
 10 + 11
 12



Load address sets Fetch Flip Flop

Part No.	Description	Quantity
MEMO L	MEMO L	
MEMO H	MEMO H	
MEMO L	MEMO L	

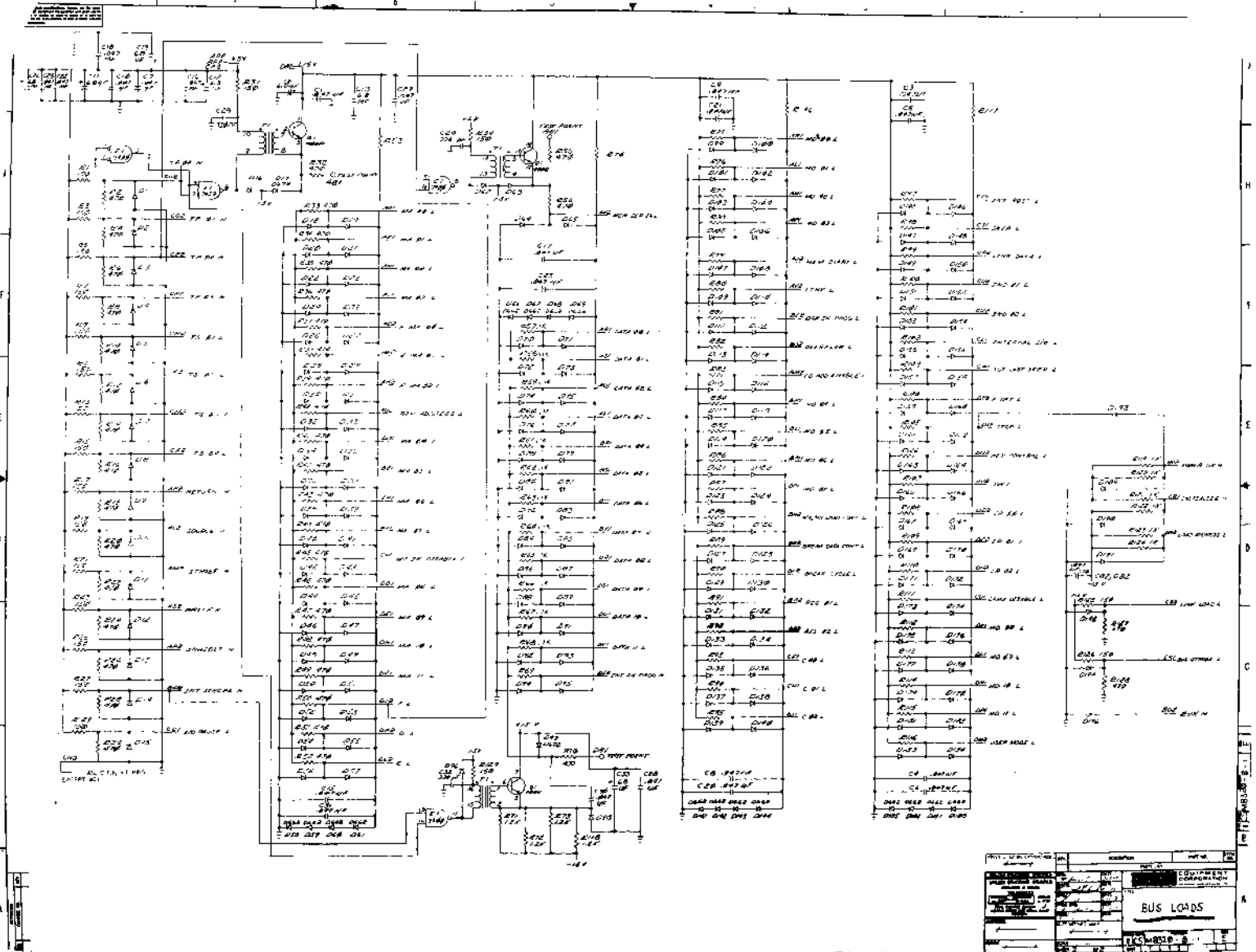
M8310



NOTES:
 1. ALL BUS LOADS ARE SHOWN IN THE PLAN.
 2. ALL WIRING SHALL BE IN ACCORDANCE WITH THE NATIONAL ELECTRICAL CODE (NEC) AND ALL APPLICABLE LOCAL CODES.
 3. THE CONTRACTOR SHALL BE RESPONSIBLE FOR OBTAINING ALL NECESSARY PERMITS AND APPROVALS FROM THE LOCAL AUTHORITIES.

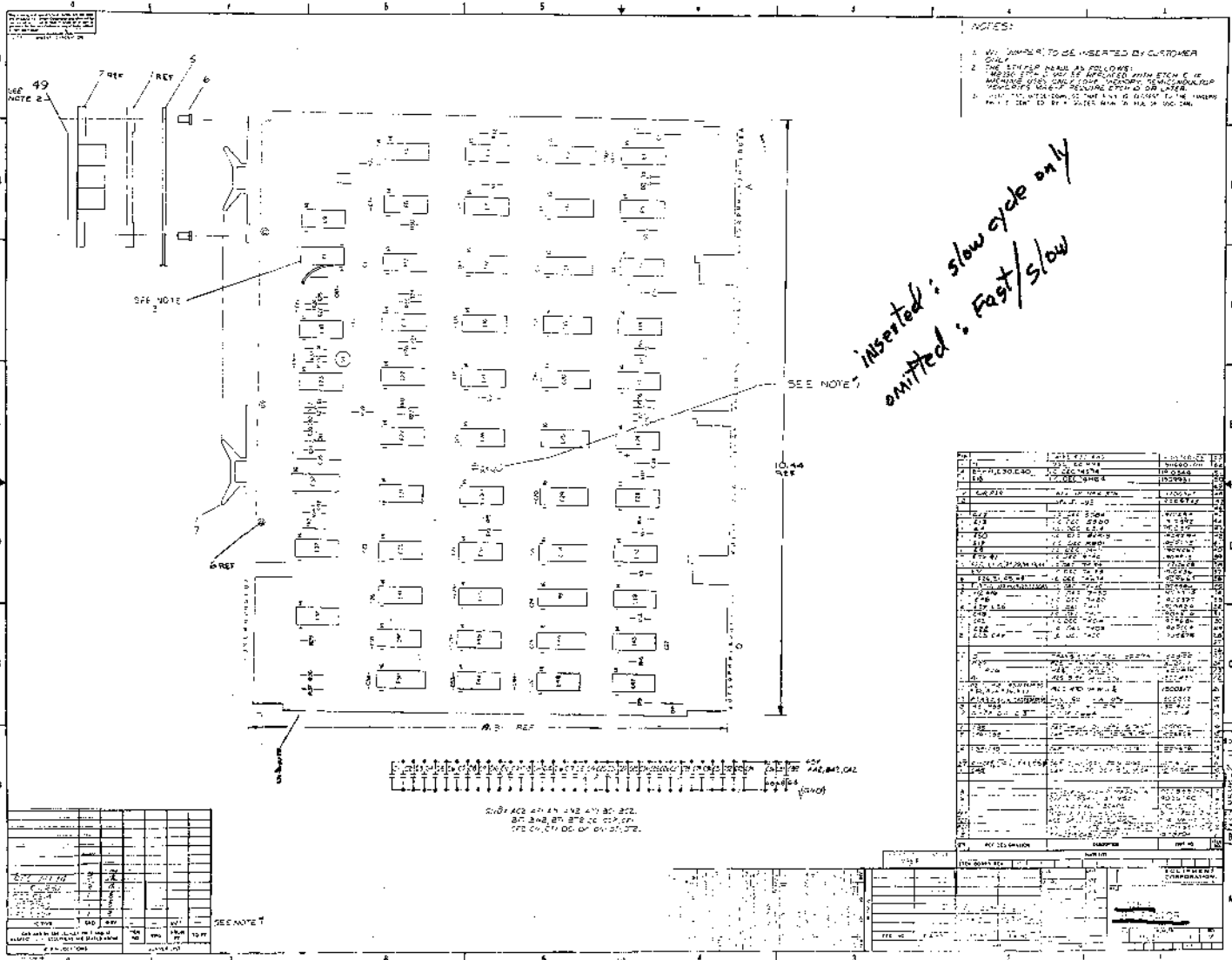
NO.	DESCRIPTION	LOAD TYPE	LOAD VALUE	TOTAL
1	REF 4-4	SEE IN VIEW SK	30000	30000
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M 8320



NO.	DESCRIPTION	UNIT	REMARKS
1	BUS 1		
2	BUS 2		
3	BUS 3		
4	BUS 4		
5	BUS 5		
6	BUS 6		
7	BUS 7		
8	BUS 8		
9	BUS 9		
10	BUS 10		

M8320



- NOTES:
1. ALL DIMENSIONS TO BE INSERTED BY CUSTOMER
 2. THE STRIP IN PANEL AS SHOWN IS TO BE USED IN ALL PANELS UNLESS OTHERWISE SPECIFIED
 3. THE STRIP IN PANEL AS SHOWN IS TO BE USED IN ALL PANELS UNLESS OTHERWISE SPECIFIED
 4. THE STRIP IN PANEL AS SHOWN IS TO BE USED IN ALL PANELS UNLESS OTHERWISE SPECIFIED

*inserted: slow cycle only
omitted: Fast/Slow*

NO.	DESCRIPTION	QTY.	UNIT PRICE	TOTAL PRICE
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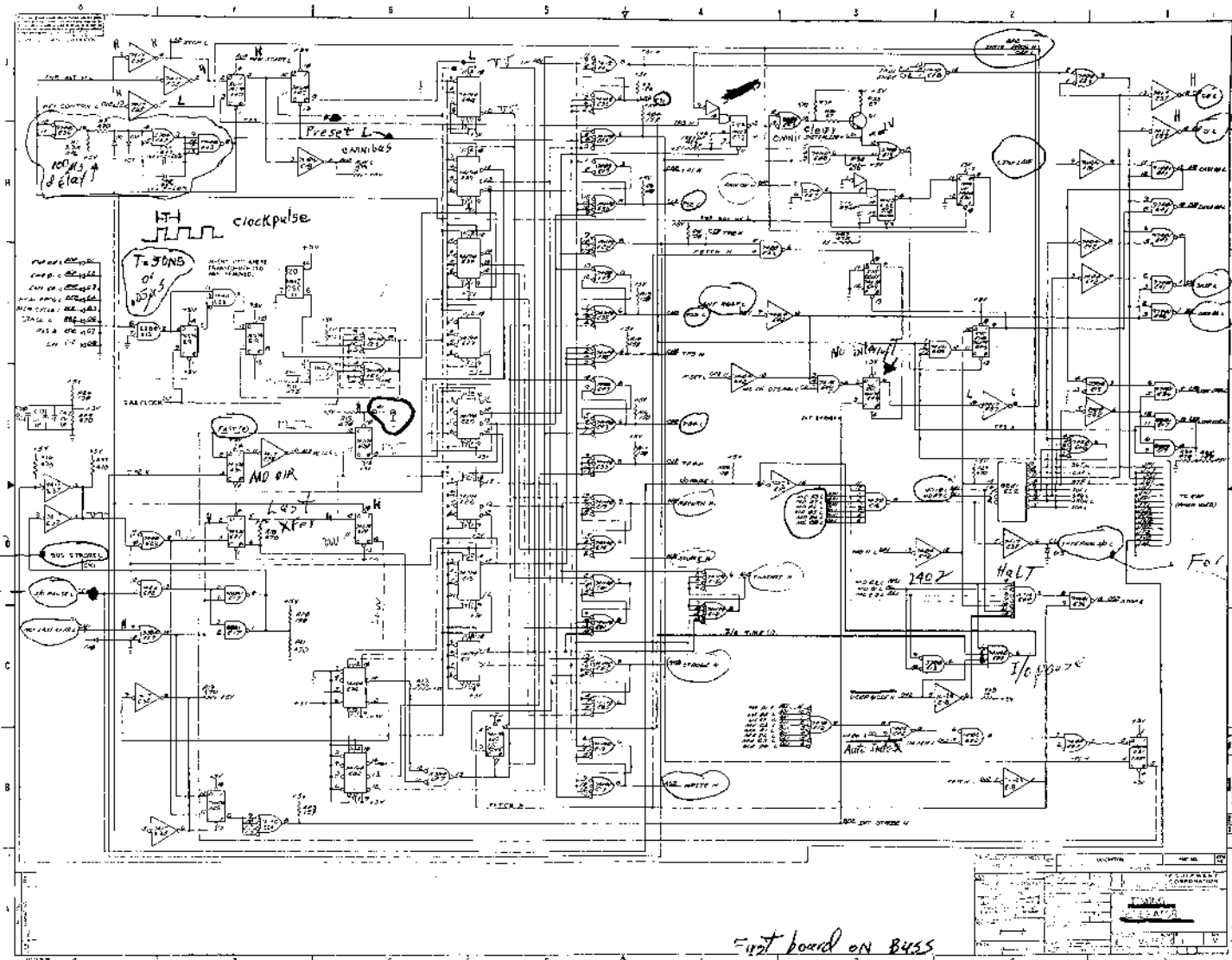
NO.	DESCRIPTION	QTY.	UNIT PRICE	TOTAL PRICE
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SEE NOTE T

M 8330

Provides synchronizing signals for memory & processor operations.
 8 processor timing signals, 5 memory timing signals.

.V1 can be jumpered for easier trouble shooting



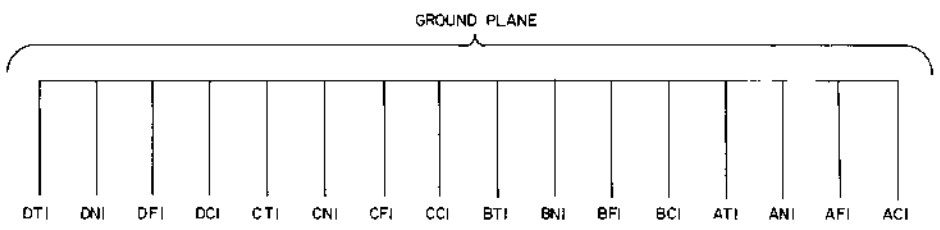
For External device with Pci/I/O BUS.

= 127 board on BUSS

M8330

REV. C
 NUMBER MB49-0-1
 SIZE CODE B CS

THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY. COPYRIGHT 1970 BY DIGITAL EQUIPMENT CORPORATION



REVISIONS CHK'D NO. REL	DRN. NANCY MOORE	DATE 8/18/70	TRANSISTOR & DIODE CONVERSION CHART				 EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	TITLE RFI SHIELD M849			
	CHK'D R. S. L.	DATE 11/17/70	DEC	EIA	DEC	EIA		SIZE B	CODE CS	NUMBER MB49-0-1	REV C
	ENG. R. S. L.	DATE 11/17/70						PRINTED CIRCUIT REV. D			
	PROD. R. S. L.	DATE 2/6/71									

12447432 2 1/16