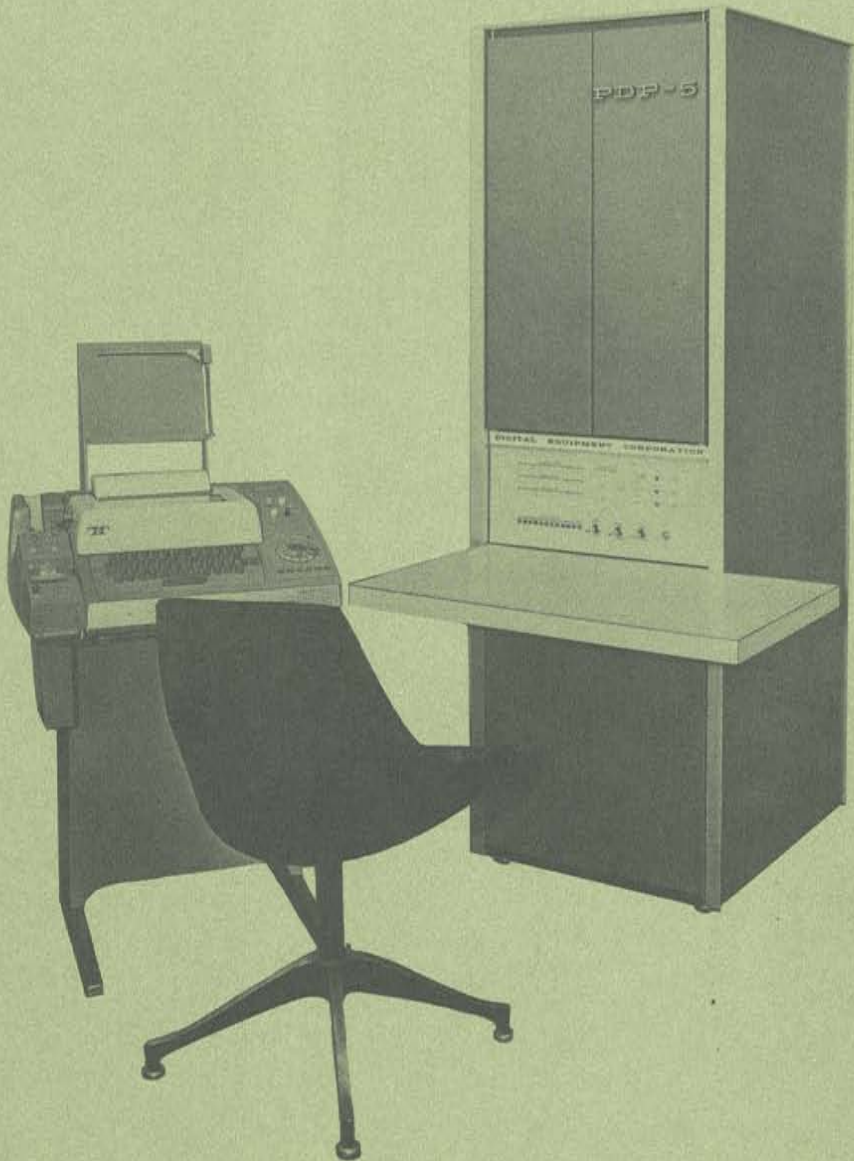


PROGRAMMED DATA PROCESSOR-5



PDP
5

FORTRAN . . . operates with basic PDP-5 and 4096-word memory

6-microsecond memory cycle . . . only machine in its price range with high-speed, random-access, core memory

Large core memory capacity . . . from 1024 to 32,768 12-bit words

High-speed input-output . . . in-out data transfers at rates up to two million bits per second

Data interrupt . . . gives direct access to memory for input-output data transfers without disturbing program execution

Program interrupt . . . initiates sub-programs specified by external devices or conditions; frees the processor from time-dependency on external devices

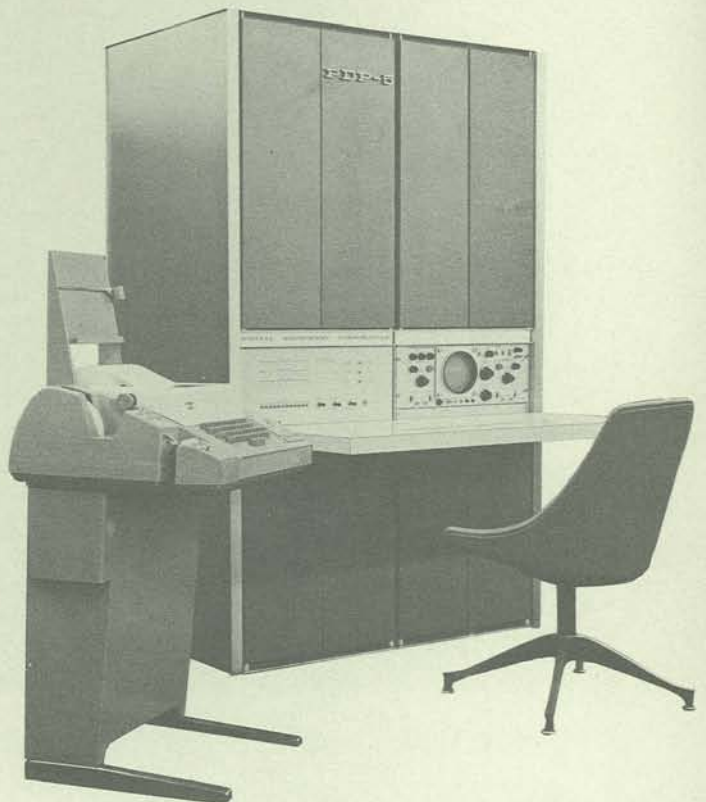
Computer-aided programming . . . program can be debugged and tape can be edited on line

12- or 24-bit arithmetic . . . single and double precision routines are provided

Micro programming . . . saves program execution and preparation time by performing multiple operation instructions

Indexing . . . eight auto-indexing registers simplify list processing, matrix manipulation, and table lookups

Indirect addressing . . . simplifies subroutine linkage



PDP-5

SCIENTIFIC COMPUTATION ■ SYSTEMS
AND CONTROL APPLICATIONS ■ ON-
LINE DATA COLLECTION AND REDUCTION

The Programmed Data Processor-5 (PDP-5) makes available to engineering and scientific applications a random-access, high-speed, magnetic-core memory in a compact but complete general-purpose digital computer. It is intended for use in computation or as a control or processing element in an on-line data handling, experiment monitoring, or process control system.

The PDP-5 performs binary operations on 12- or 24-bit 2's complement numbers. Its 6-microsecond core memory cycle time gives it a computation rate of 55,555 additions per second and permits it to handle input-output data at rates up to two million bits per second.

It is capable of servicing up to 64 external devices, each requiring up to three commands, or 96 devices, each requiring two commands, or 192 devices, each requiring one command. The external devices can be special-purpose units or any of Digital's wide selection of unique display or tape equipment and more conventional card, tape, and mass storage equipment. The addition of devices in the field requires no modification to the central processor. PDP-5 circuits use Digital's customer-proven solid-state circuit modules and incorporate provisions for marginal checking to insure reliability even under difficult operating conditions.

Its programming system includes a FORTRAN compiler which operates in a basic PDP-5 with 4096 words of core memory. An expanded FORTRAN operating system is also available for installations with Digital's new Micro Tape. Other elements of the programming system are the Symbolic Assembler, Symbolic On-Line Debugging Program, Symbolic Tape Editor, Floating Point Package, mathematical function routines, and utility and maintenance programs. On-line debugging and tape editing, a unique Digital combination, establish a close programmer-machine operating mode in which the computer assists in the program debugging and edits program tapes to incorporate the programmer's changes. The result is far more speed in preparing operating programs and getting them on-line.

STANDARD PDP-5

The standard PDP-5 includes the central processor (shown in the diagram), 1024- to 32,768-word, 12-bit random-access, magnetic-core memory, input-output control, and input-output tape teleprinter. Standard features include the FORTRAN Compiler, the Symbolic Assembler, and other elements of the programming system, 12- or 24-bit arithmetic, indirect addressing, data and program interrupts, and eight auto-indexing core memory locations.

CENTRAL PROCESSOR

carries out arithmetic operations, provides memory access, and controls information entering or leaving the machine. It consists of registers and information handling elements.

MEMORY ADDRESS REGISTER (MA) — used to address a word in memory; provides addressing for 1024 or 4096 words of memory. Can be cleared or incremented by one.

MEMORY BUFFER REGISTER (MB) — holds information which is being written into or read out of the core memory. Can be cleared, incremented by one or two, or shifted right.

INSTRUCTION REGISTER (IR) — contains the operation code of the instruction currently being performed by the machine.

ACCUMULATOR (AC) — performs the arithmetic operations with the memory buffer register. Acts as an input-output register and can be combined with the memory buffer register to act as a successive approximation analog-to-digital converter.

LINK (L) — used to extend the precision of the accumulator. Permits more rapid performance of double-precision (24-bit) operations and acts as the carry register for twos complement arithmetic.

SWITCH REGISTER — 12 switches whose settings can be sensed to let the operator intervene while programs are running. Operator can modify a program by depositing data in the memory address register, a memory register, or the accumulator.

PROGRAM COUNTER — determines the sequence in which instructions are performed. It is core memory location 0 and can be manipulated by the program just as any other memory location can be.

INPUT MIXER — accepts information from external devices and feeds it sequentially to the accumulator. In combination with the device selector, the input mixer gives the PDP-5 a greater flexibility in dealing with its environment than other computers in its price range.

DEVICE SELECTOR (DS) — produces control pulses to transfer information between external devices and the accumulator or to activate external devices.

CORE MEMORY

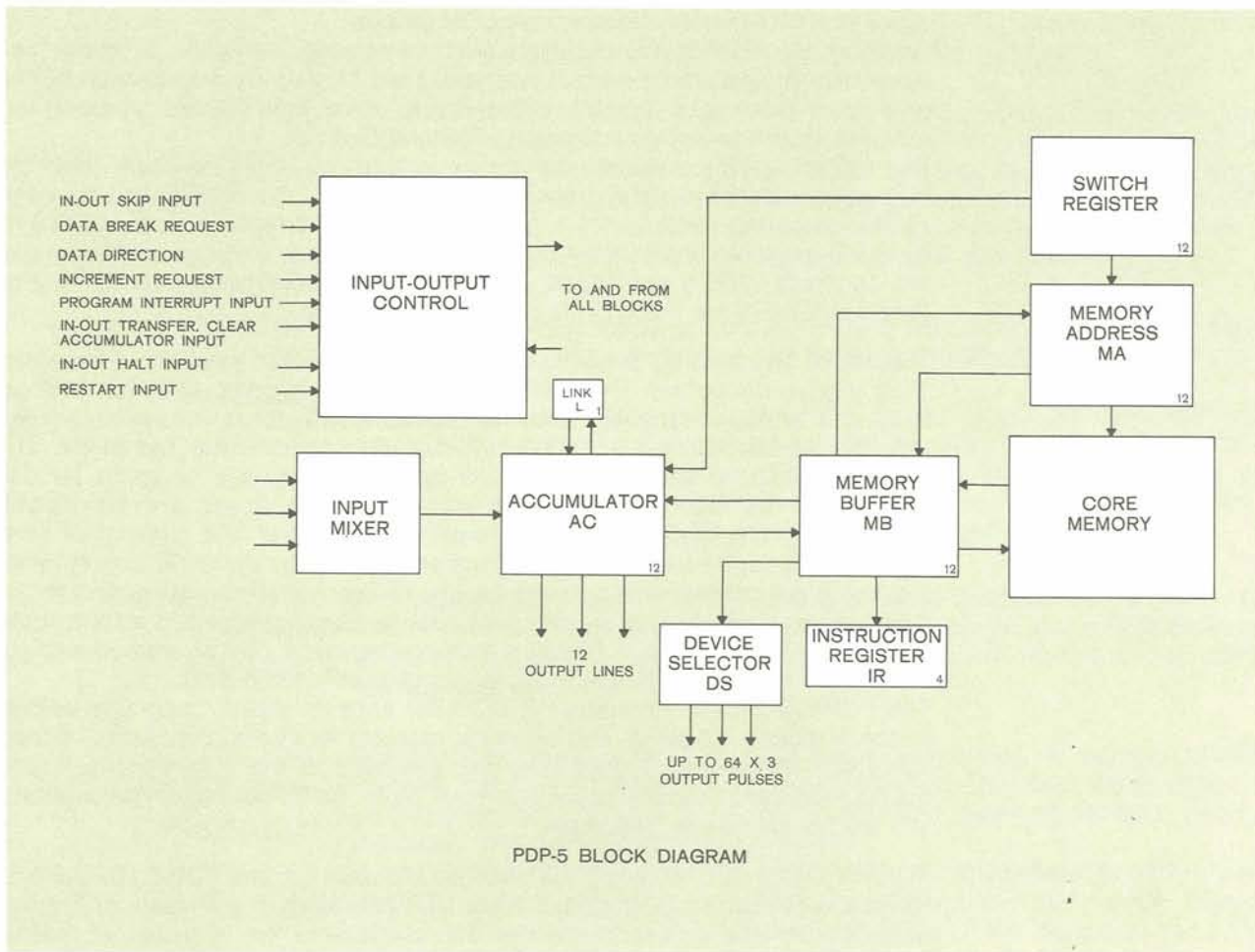
provides storage for operands and instructions to be performed by the internal processor and holds information being collected or distributed. This is a random-access, magnetic-core memory available with 1024 to 32,768 12-bit words and with a cycle time of 6 microseconds. The PDP-5 is the only computer in its price range with such a memory.

INPUT-OUTPUT CONTROL

provides a means of transmitting data to or receiving data from external devices. It has several different classes of inputs.

DATA BREAK — permits the transmission of data directly to core memory. It includes three types of requests: data break, data direction, and increment. An increment request transfers data at sequential addresses automatically after the first address is specified.

PROGRAMMED IN-OUT — makes it possible to specify input-output transfer (IOT) instructions which affect the state of selected devices. The IOT



instruction allows one basic instruction to handle many devices. Command pulses occur at various times to allow flags to be sampled (and an instruction skipped), buffers to be cleared, and data to be transmitted to or from the accumulator.

IN-OUT SKIP (IOS) — allows computer programs to determine the status of external devices and to skip a succeeding instruction when specified conditions exist.

IN-OUT HALT — permits the computer to be halted while an external device is operating and then restarted by a pulse from the device.

IN-OUT TRANSFER, CLEAR ACCUMULATOR — enables the accumulator to be cleared by an IOT instruction.

PROGRAM INTERRUPT — initiates execution of subprograms to transfer control to external devices for recording or processing event signals or data.

INPUT-OUTPUT TAPE TELEPRINTER

permits the operator to receive data from or send it to the processor on perforated paper tape or by keys and keyboard. It is standard Teletype equipment with a speed of ten characters a second.

OPERATOR CONSOLE

contains the indicators, keys and switches to operate the machine and to observe and modify the status of the internal processor. The functions of the keys and switches are described below.

PROGRAMMING SYSTEM

The programming system for the PDP-5 consists of the Symbolic Assembler, FORTRAN II System, Symbolic On-Line Debugging Program, Symbolic Tape Editor, Floating Point Package, mathematical function subroutines, and utility and maintenance programs. All will operate with the basic computer: processor, 4096-word memory, tape teleprinter.

Because the PDP-5 makes high-speed computing available to many new users, the programming system was designed to simplify and accelerate the process of learning to program. At the same time, experienced programmers will find that it incorporates many advanced features.

The system is intended to make immediately available to each user the full, general-purpose data processing capability of the PDP-5 and to serve as the operating nucleus for a growing library of programs and routines to be made available to all installations. New techniques, routines, and programs are constantly being developed, field-tested, and documented in the Digital Program Library for incorporation in users' systems.

ASSEMBLER

The use of an assembly program has become a standard practice in programming digital computers. This process lets the programmer code his instructions in a symbolic language, one he can work with more conveniently than with the 12-bit binary numbers which actually operate the computer. The assembly program then translates the symbolic language program he has written into its machine code equivalent. The advantages are significant: the symbolic language he writes in is more meaningful and convenient than a numeric code; he can refer to instructions or data by symbolic names without being concerned with or even having to know their actual addresses in the memory; decimal and alphabetical data can be expressed in a form more convenient to him than in binary numbers; programs can be altered without extensive changes; and debugging is considerably simplified.

The PDP-5 Symbolic Assembler (DEC-5-36) accepts source programs written in the symbolic language and converts memory locations, computer instructions, and operand addresses from the symbolic to the binary form. It produces an object program tape, a symbol table defining memory allocations, and useful diagnostic messages.

COMPILER

The FORTRAN (for FORMula TRANslation) System for the PDP-5 (DEC-5-6-S) lets the user express the problem he is trying to solve in a mixture of English words and mathematical statements that is close to the language of mathematics and also intelligible to the computer. In addition to reducing the time needed for program preparation, it enables users with little or no knowledge of the computer's organization and operating language to write effective programs for it. The FORTRAN Compiler contains the instructions the computer requires to perform the clerical work of translating the FORTRAN version of the problem statement into an object program in machine language. It also produces diagnostic messages. After compilation, the object program and the data it will work with are loaded into the computer for solution of the problem.

The FORTRAN language consists of four general types of statements: arithmetic, logic, control, and input-output. Fixed and floating point arithmetic expressions can be used, both simple and subscripted. FORTRAN functions include addition, subtraction, multiplication, division, sin, cos, arctan, square root, natural log, and exponential.

The Extended FORTRAN System for PDP-5 installations with Micro Tape permits users to compile programs of arbitrary length, permits the use of multidimensional arrays to simplify matrix manipulation, and provides more input-output capability.

SYMBOLIC ON-LINE DEBUGGING PROGRAM

DDT-5 (DEC-5-5-S) lets the programmer use the PDP-5 to debug his object programs on line, giving him instantaneous feedback when he makes changes. This dynamic debugging has been extensively developed by Digital. One of its principal advantages is that it gives the programmer close control, preventing flaws in his program from destroying significant portions of the memory contents.

Using the tape teleprinter, the user can communicate conveniently with the PDP-5 in the symbols of his source language. He can control the execution of any portion of his object program by inserting breaks, or traps, in it. When the computer reaches a break, it transfers control of the object program to DDT. The user can then examine and modify the contents of individual memory registers to correct and improve his object program.

**SYMBOLIC
TAPE
EDITOR**

The Symbolic Tape Editor program is used to edit, correct, and update symbolic program tapes using the PDP-5 and the tape teleprinter. With the editor in memory, the user reads in portions of his symbolic tape, removes, changes, or adds instructions or operands, and gets back a new, complete, symbolic tape with errors removed. He can work through the program instruction by instruction, spot-check it, or concentrate on new sections.

**FLOATING
POINT
PACKAGE**

The Floating Point Package lets the PDP-5 user perform arithmetic operations that many other computers can perform only after the addition of costly optional hardware.

Floating point operations automatically align the binary points of operands, retaining the maximum precision available by discarding leading zeros. In addition to increasing accuracy, floating point operations relieve the programmer of the scaling problems common in fixed point operations. This is of particular advantage to the inexperienced programmer.

**MATHEMATICAL
FUNCTION
ROUTINES**

The programming system also includes a set of mathematical function routines to perform the following operations in both single and double precision: addition, subtraction, multiplication, division, square root, sin, cos, arctan, natural logarithm, and exponential.

**UTILITY AND
MAINTENANCE
PROGRAMS**

PDP-5 utility programs provide printouts or punchouts of memory contents in octal, decimal, or binary form, as specified by the user. Subroutines are provided for octal or decimal data transfer and binary-to-decimal, decimal-to-binary, and tape teleprinter conversion.

A complete set of standard diagnostic programs is provided to simplify and expedite system maintenance. Program descriptions and usage manuals permit the user to effectively test the operation of the computer for proper memory functioning and execution of instructions. In addition, diagnostic programs to check the performance of standard and optional peripheral devices are provided with the devices.

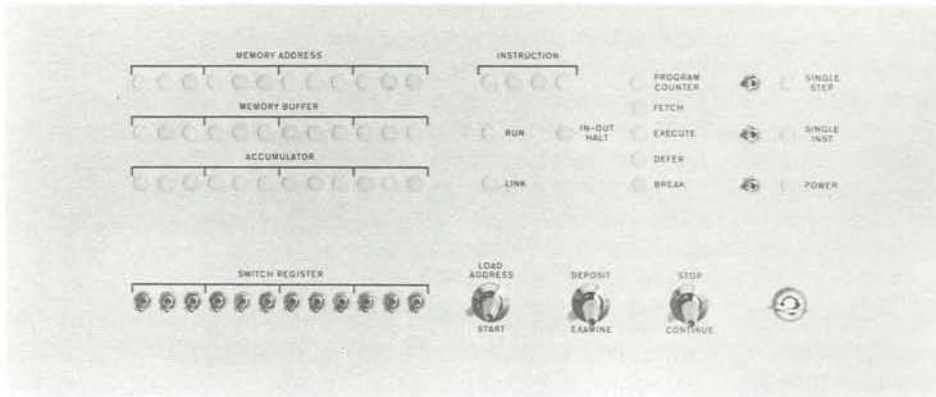
**TRAINING AND
ASSISTANCE**

Digital offers monthly courses in programming and maintaining each of its computer models as part of the service provided to purchasers. These courses include instruction by experienced Digital personnel, training manuals, and supplies. Classes are kept small to insure adequate individual attention.

Digital will assist you with specific programming problems before, during, and after installation of your computer and can provide a computer at our home office to let you check out your programs under the guidance of Digital programmers until your own computer is on line.

**DECUS LIBRARY
AND
NEWSLETTER**

In addition to the Digital Program Library, users of Digital equipment have access to the growing DECUS Library of utility programs, subroutines, and other programming materials. DECUS (for Digital Equipment Computer Users' Society) was formed to promote a free and effective interchange of information. A principal channel for the information flow is DECUSCOPE, a monthly technical newsletter to which users contribute their ideas, techniques, routines, and program summaries. The DECUS Library distributes to members program write-ups and the corresponding program tapes and listings. Certification of these materials is under the direction of the users' programming committee, which also guides the operation of the Library. DECUS also publishes the proceedings of its annual symposiums and frequent seminars.



All keys, switches and indicators are located on a convenient control panel just above the console shelf on the front of the PDP-5.

CONSOLE KEYS

6	<p>START Starts computer. Executes CLA (clear accumulator), CLL (clear link) and IOF (interrupt off) and takes the first instruction from the memory at the address presently in the memory address register.</p> <p>STOP Causes the computer to stop at the completion of the memory cycle in progress at the time of key operation.</p> <p>CONTINUE Causes the computer to resume operation at the point where it was stopped.</p> <p>EXAMINE Sets the contents of the memory location selected by the memory address register into the accumulator and the memory buffer. The memory address register is then</p>	<p>DEPOSIT Sets the word selected by the switch register into the memory at the location specified by the memory address register. The results remain in the memory buffer. The memory address register is then incremented by one, permitting the operator to deposit words in consecutive registers without re-loading the addresses.</p> <p>LOAD ADDRESS Deposits the contents of the switch register in the memory address register.</p>
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CONSOLE TOGGLE SWITCHES

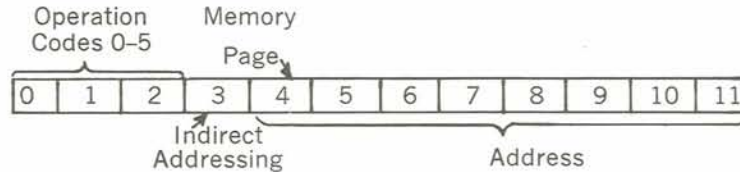
<p>SWITCH REGISTER Permits operator to deposit a word in memory or in the memory address register by means of the LOAD ADDRESS or DEPOSIT keys. The contents of the switch register can be deposited in the accumulator under program control.</p> <p>SINGLE STEP Causes the computer to halt at the completion of each memory cycle. Repeated operation of the CONTINUE key will step the program one cycle at a time so that the</p>	<p>SINGLE INSTRUCTION state of the machine can be examined at each step. Causes the computer to stop at the completion of each instruction.</p> <p>POWER Turns on power.</p> <p>LOCK SWITCH Disables all keys and switches on the console except the SWITCH REGISTER to prevent inadvertent power turn-off or program interference while a program is in progress.</p>
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PDP-5 INSTRUCTIONS

The PDP-5 performs two types of instructions: memory reference and augmented. Memory reference instructions store or retrieve the data they use in core memory. Augmented instructions do not store or retrieve data in memory. They let the programmer use the address portion of the instruction to specify logical operations, giving the PDP-5 a microprogramming capability. Instruction execution times are multiples of the 6-microsecond core-memory cycle time. Memory reference instructions are executed in 12, 18, or 24 microseconds, with an additional 6 microseconds required for those which use indirect addressing. Augmented instructions are executed in 12 microseconds.

MEMORY REFERENCE INSTRUCTIONS

The word format for memory reference instructions is shown below.



The first three bits contain the octal code number of the instruction to be performed. This can be 0_8 through 5_8 , corresponding to the six instructions in the table below. Bit 3, when it contains a one, instructs the computer to use the indirect, or deferred, address selection mode.

Indirect addressing lets the computer use more memory than the 256 (2^8) words directly addressable by the 8-bit address portion of the instruction word. In the indirect addressing mode, the computer finds in the memory location specified by the address portion a 12-bit actual address in which to retrieve or store the data it needs or is working with. The memory cycle required to find the actual address adds 6 microseconds to the time required for instructions using indirect addressing.

The memory page bit of the instruction word refers to the organization of the computer memory in 128 (200_8)-word "pages." For direct addressing, the programmer uses bits 4 through 11 to select one of 256 memory locations. To reach the other pages, the programmer uses indirect addressing.

TABLE 1 MEMORY REFERENCE INSTRUCTIONS

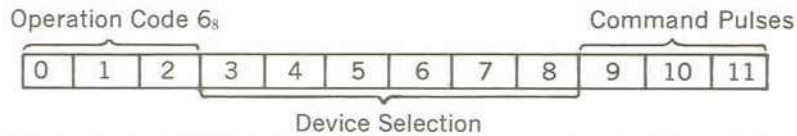
Mnemonic Code	Octal Code	Operation	Time (μsec)
AND Y	0	Logical AND. The logical AND function is performed between the contents of the accumulator and the contents of Y. The result is left in the accumulator and the original contents of the accumulator are lost.	18
TAD Y	1	Twos complement add. The contents of Y are added to the contents of the accumulator in 2's complement arithmetic. If there is a carry out of bit 0 of the accumulator, the link will be complemented. The contents of Y are unchanged. This feature is useful in multiple precision arithmetic.	18
ISZ Y	2	Index and skip if zero. The contents of Y are replaced by the contents of Y plus one. The contents of the accumulator are unaffected by this instruction. If the resulting sum is zero, the instruction following the ISZ is skipped. This instruction is useful for incrementing operand addresses and in loop iteration counting.	18
DCA Y	3	Deposit and clear accumulator. The contents of the accumulator are deposited in memory register Y. The accumulator is then cleared.	18
JMS Y	4	Jump to subroutine. The contents of the program counter contained in register 0 are deposited in register Y. Upon completion, Y will contain the address of the instruction following the JMS. The next instruction will be taken from Y + 1. This instruction is primarily useful for subroutine linkage.	24

TABLE 1 MEMORY REFERENCE INSTRUCTIONS (continued)

Mnemonic Code	Octal Code	Operation	Time (μ sec)
JMP Y	5	Jump. The contents of the program counter contained in memory register 0 are reset to address Y. The next instruction that will be executed will be taken from memory register Y. The original contents of the program counter are lost. This instruction is useful for transferring program control to randomly selected memory locations.	12

AUGMENTED INSTRUCTIONS

Augmented instructions are input-output transfer (IOT) and operate. They permit microprogramming, letting the user extend the operation code from bit 0 through bit 11 to perform several operations with one instruction word. The IOT instruction transfers data between the processor and peripheral devices. The format is shown below.



Bits 0 through 2 contain the IOT operation code, 6_8 . Bits 3 through 8 select one of 64 devices, and bits 9 through 11 are used to generate timed pulses to start and stop the devices and clear their flags. (Signals which indicate that the devices have data to send to the processor.) If only two command pulses are needed, up to 96 devices can be serviced or up to 192 devices which need only one pulse.

The operate instruction includes two groups of microinstructions, listed below. Group 1 (opr 1), designated by a 0 in bit 3 of the instruction, is primarily for performing clearing, complementing, incrementing, and rotating operations. Group 2 (opr 2), designated by a 1 in bit 3, is used primarily for checking the contents of the accumulator and link for instruction-skipping conditions. Several microinstructions can be combined in one step to perform more powerful operations.

TABLE 2 AUGMENTED INSTRUCTIONS
(12-microsecond execution times)

Mnemonic Code	Octal Code (in Address Portion)	Operation
opr 1		
cla	200	Clear accumulator
cil	100	Clear link
cma	40	Complement accumulator
cml	20	Complement link
rtr	12	Rotate accumulator and link right two positions
rar	10	Rotate accumulator and link right one position
rtl	6	Rotate accumulator and link left two positions
ral	4	Rotate accumulator and link left one position
iac	1	Index accumulator
nop	0	No operation
opr 2		
cla	200	Clear accumulator
spa	110	Skip on plus accumulator
sma	100	Skip on minus accumulator
sna	50	Skip on non-zero accumulator
sza	40	Skip on zero accumulator
szl	30	Skip on zero link
snl	20	Skip on link equals one
skp	10	Skip unconditionally
osr	4	OR with switch register
hlt	2	Halt

OPTIONAL EQUIPMENT

MEMORY EXTENSION CONTROL TYPE 154

Allows expansion of the PDP-5 memory from 4096 to 32,768 words in increments of 4096 words. Can be attached to any PDP-5 without requiring changes to the processor.

HIGH SPEED MULTIPLY AND DIVIDE TYPE 153

Reduces multiplication and division times to 48 and 78 microseconds.

HIGH SPEED PERFORATED TAPE PUNCH TYPE 75A

Punches 8-level tape at 63.3 characters a second.

HIGH SPEED PERFORATED TAPE READER TYPE 750

Reads perforated paper tape photoelectrically at 300 characters a second.

MAGNETIC TAPE TRANSPORT TYPE 50

Reads and writes IBM-compatible magnetic tape at transfer rates of 15,000 and 41,700 cps.

AUTOMATIC MAGNETIC TAPE CONTROL TYPE 57A

Automatically controls up to eight Type 50 Magnetic Tape Transports. Provides information transfer through the data interrupt facility of the computer. Controls tape reading or writing at 15,000 or 41,700 cps transfer rate, 200 or 556 bits per inch. The tape format is compatible with that of IBM equipment.

OSCILLOSCOPE DISPLAY TYPE 34B

Provides a low-cost display on a 5-inch cathode ray tube scope with 1024×1024 addressable points.

PRECISION CRT DISPLAY TYPE 30N

Plots data on a 16-inch cathode ray tube at 20,000 points per second. More than one million points are individually addressable.

LIGHT PEN TYPE 32

Detects information displayed on a Type 30N Display and sends an identifying signal to the computer.

MICRO TAPE SYSTEM

Provides a fixed-address magnetic tape facility for high speed loading, reading, and program updating. Consists of a Type 555 Dual Transport Unit and a Type 552 Control Unit.

INCREMENTAL PLOTTER TYPE 350

Performs high-resolution plotting in eight directions on paper 12 or 31 inches wide and up to 120 feet long. Rates are 12,000 and 18,000 per minute, with point-to-point increments of 0.005 and 0.01 of an inch.

ANALOG TO DIGITAL CONVERTER TYPE 137

Wired into the computer, but modules to activate it are optional extras. Uses the successive approximation technique. Offers accuracy of up to 11 bits, depending on speed required.

ADDITIONAL EQUIPMENT BAY

Accommodates optional equipment requiring more space.

CARD PUNCH CONTROL TYPE 450

Controls on-line buffered operation of standard card punch equipment. Maximum speed is 100 cards a minute. Any or all positions can be punched in any format.

CARD READER TYPE 451A

Reads up to 200 standard cards a minute. Cards are read optically, column by column, in binary or alphanumeric modes.

HIGH SPEED CARD READER TYPE 451B

Reads standard punched cards at rates up to 800 a minute.

AUTOMATIC LINE PRINTER TYPE 64

Prints 300 lines a minute, 120 columns a line, any one of 64 characters a column.

SERIAL MAGNETIC DRUM SYSTEM TYPE 250

Stores and transfers information in blocks of 128 12-bit words. Total storage is 8,192, 16,384, or 32,768 words. Computation continues during transfers.

DATA CHANNEL MULTIPLEXER TYPE 129

Permits high speed transfer between core memory and up to four input-output devices. Maximum combined transfer rate is 166,666 12-bit words a second.

digital

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