Digital Equipment Corporation
Maynard, Massachusetts

digital

LAB-8/E MAINTENANCE MANUAL

DEC-LB-H8EMM-B-D

LAB-8/E
MAINTENANCE MANUAL

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CONTENTS

pg 2-17 Tech 602 mod's

CONTENTS (Cont)

CONTENTS (Cont)

CONTENTS (Cont)

CONTENTS (Cont)

CONTENTS (Cont)

ILLUSTRATIONS

ILLUSTRATIONS (Cont)

ILLUSTRATIONS (Cont)

TABLES

TABLES (Cont)

TABLES (Cont)

CHAPTER 1
INTRODUCTION

1.1 PURPOSE OF MANUAL

This manual provides the user with the installation procedures, theory of operation, and maintenance procedures necessary to install and operate the LAB-8/E System manufactured by Digital Equipment Corporation.

The theory of operation and maintenance procedures for the LAB-8/E processor are contained in the *PDP-8/E Maintenance Manual, Volume I*. When operating and performing maintenance on the LAB-8/E, the user should be familiar with Chapter 4 of the PDP-8/E manual. This manual deals with the options that have been added to the PDP-8/E to form the LAB-8/E System. Paragraph 1.4 contains a list of companion documents to this manual and other documentation for the LAB-8/E.

1.2 SYSTEM FEATURES

The LAB-8/E System performs arithmetic calculations, controls machine operations, makes on-line measurements of both analog and digital information, displays data on an oscilloscope, and stores large quantities of data for future use and/or modification. The user may use control tapes provided by Digital, or write his own programs to shape the LAB-8/E to his own needs and to perform sophisticated handling of analog or digital data. The LAB-8/E is a truly sophisticated system allowing flexibility for the user in data acquisition and processing.

The LAB-8/E design enables the user to purchase the basic LAB-8/E and to add on options as requirements increase. The basic system comprises the following:

a. A PDP-8/E general purpose 12-bit digital computer with a basic 4096-word memory and a 1.2-μs cycle time.

b. A 33 ASR Teletype®, 10-bit I/O device with a paper-tape reader and punch.

c. A laboratory mounting panel with precision power supply for use with LAB-8/E peripherals.

d. A 10-bit Analog-to-Digital Converter with sample and hold circuitry and optional preamplifier and multiplexer expander.

e. A 10-bit Point-Plot Display Control for the graphical display of data on an oscilloscope.

f. A Real-Time Clock with five programmable ranges from 1 μs per count to 10 ms per count, plus three Schmitt triggers.

Expansion is easily accommodated through a two-way bus, called OMNIBUS™, which all LAB-8/E modules plug into directly or indirectly. Figure 1-1 shows the basic PDP-8/E and the options added, shown inside the dotted lines, to form the basic LAB-8/E. One OMNIBUS contains 20 non-dedicated slots that can contain up to

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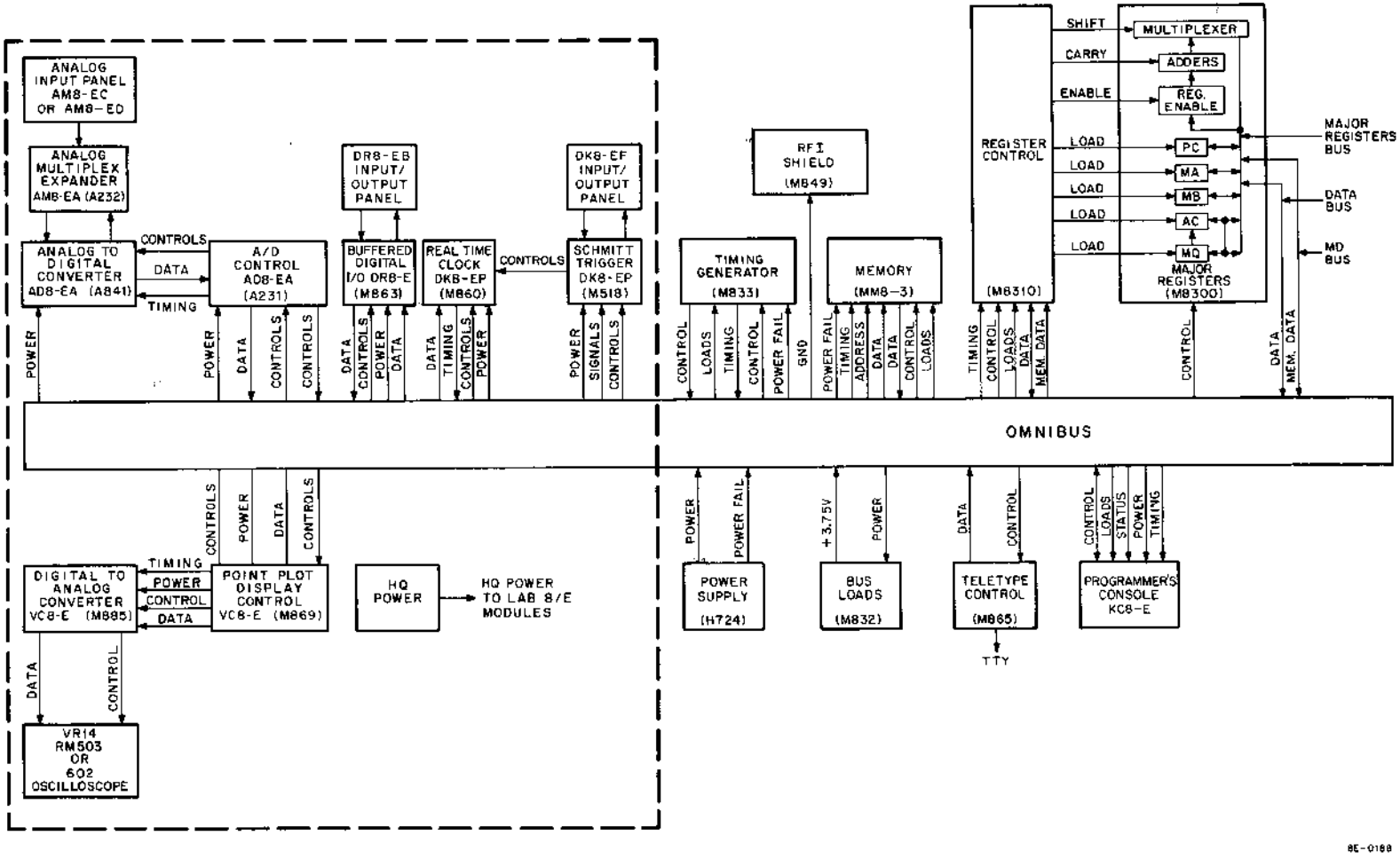


Figure 1-1 LAB-8/E Basic System

20 PDP-8/E or LAB-8/E options. The user can add one or more additional OMNIBUS modules to accommodate more options, if required.

Three categories of options are provided with the LAB-8/E: internal options, OMNIBUS options, and external options. Internal options are units, such as Extended Memory, and Extended Arithmetic Element, that extend the capability of the processor but do not control peripherals. OMNIBUS options include internal and external options that plug directly into the OMNIBUS. External options are units that indirectly plug into the OMNIBUS through an I/O Bus Adapter interface.

The specifications for the LAB-8/E Central Processor and options are shown in Table 1-1. The options are described in the following paragraphs.

1.2.1 Analog-to-Digital Converter (AD8-EA)

The Analog-to-Digital (A/D) Converter consists of the A841 and A231 modules. The A841 module contains analog circuitry, including the A/D weighing switches, comparator, and sample and hold. The A231 module contains all the control logic for the A841 module. The AD8-EA receives a ±5 Vdc signal and produces a 9-bit + sign digital word representing the input. The two modules are joined by an H851 Edge Connector.

1.2.2 Analog Preamplifier and Multiplexer (AM8-EA)

The AM8-EA is a single A232 quad module containing eight analog preamplifiers and eight multiplexer channels that select the output of one preamplifier to be applied to the A/D converter. An additional module expands the multiplexer to 16 channels. Input to the AM8-EA is ±1V differential and the output is ±5V single-ended to the A841 module of the AD8-EA.

1.2.3 Point-Plot Display Control (VC8-E)

The VC8-E consists of the M885 and M869 modules. The M885 module receives 9 bits + sign of digital data and converts it to ±5 Vdc voltage to be applied to the oscilloscope display. The M869 module contains all the control logic to control the Digital-to-Analog (D/A) converter.

1.2.4 Buffered Digital I/O (DR8-EA)

The DR8-EA consists of one M863 module. It can provide 12 digital inputs and 12 digital outputs for the LAB-8/E and can be used to sense external events. The inputs and outputs are TTL compatible; ground (0V) represents logical true and high (+3V) represents logical false.

1.2.5 Real-Time Programmable Clock (DK8-EP)

The DK8-EP consists of the M860 and M518 modules. The M518 module contains the input logic and Schmitt triggers. The M860 module contains the control logic, registers, and IOT decoding logic. The DK8-EP provides a programmable time base that allows the user to control and/or record internal and external events. It can be used to measure time between events, record number of events in a given time, or initiate repetitive operations at specified intervals of time.

NOTE

The following panels are single-width or double-width modules which are mounted in the H945 option cabinet, Nuclear Installation Module (NIM) Binary Loader (BIN), for connecting inputs and/or outputs to the LAB-8/E System.

1.2.6 Analog Input Panels (AM8-ED and AM8-EC)

The AM8-ED and AM8-EC panels are used to supply inputs to the analog multiplexer and are mounted in the H945 cabinet. The AM8-ED has two DB-25S 25-pin connectors with matching plugs. The AM8-EC has four inputs from potentiometer channels 0 through 3. As on the AM8-ED, channels 4_8 through 17_8 are supplied on the DB-25S.

1.2.7 Real-Time Programmable Clock Input Panel (DK8-EF)

The DK8-EF panel has inputs for the Schmitt triggers. It also provides connections for EXT CLOCK or EXT START signals.

1.2.8 Digital I/O Panel (DR8-EB)

The DR8-EB provides a front panel assembly with two M904 modules, with connections for input and output to the DR8-EA Buffered Digital I/O.

Table 1-1
LAB-8/E System Specifications

Equipment	Specifications
Central Processor	
Processor Speed	Two memory cycles: *a.* Fast cycle accomplishes a FETCH, Internal IOT, or DEFER (non-Auto Index) in 1.2 μs. *b.* Slow cycle accomplishes (after FETCH) an instruction execution, or DEFER (Auto Index) in 1.4 μs.
Instruction Execution Time (MRI only)	The instruction execution time, beginning with the instruction completely executed, requires one fast and one slow memory cycle, or 2.6 μs.
Word Length	12 bits
Addressing	Direct memory addressing is controlled on front panel or through the Data Break system. Programmed addressing is accomplished as a function of software. 200 octal memory locations may be directly accessed (except when on page 0) by the program during any one memory cycle.
Program Loading	Programs may be loaded by Read-In-Mode (RIM) or Binary Loader (BIN). RIM is read into memory using toggle switches on front panel. BIN is a program used to load other programs.
Input/Output Capability	Three types of input/output transfers (IOTs) are provided: *a.* Programmed input/output or transfers *b.* Programmed Interrupts *c.* Data Break Data Break is a method used to read out of, or write into, a block of memory during normal processing.

(continued on next page)

Table 1-1 (Cont)
LAB-8/E System Specifications

Equipment	Specifications
Central Processor (Cont)	
Memory Capacity	4096 12-bit word memory locations which can be expanded to 32K of memory
Power Requirements	95–130 Vac, 47–63 Hz, approximately 6A single-phase, or 185–250 Vac, 47–63 Hz, approximately 3A single-phase with 450W power dissipation
Power Requirements (Teletype)	115 ± 10% Vac, 60 Hz ± 0.45 Hz, or 230 ± 10% Vac, 50 Hz ± 0.50 Hz, 2A line current drain, 150W power dissipation
Environment	The LAB-8/E is designed to operate at 0°C to 55°C with a relative humidity of 10% to 95% (without condensation).
Cable Requirements	The LAB-8/E I/O cable is a combination shielded and coaxial cable. The maximum length of Data Break I/O Bus cable is 30 ft, using a coaxial cable. Maximum length of the programmed I/O Bus is 50 ft, using a coaxial cable.
Instructions	Eight basic instructions constitute the instruction set: AND 0000 Logical AND TAD 1000 2's complement add ISZ 2000 Increment and skip if 0 DCA 3000 Deposit and clear AC JMS 4000 Jump to subroutine JMP 5000 Jump to another memory location IOT 6000 In/out transfer OPR 7000 Operate
A/D Converter (AD8-EA)	
Input Voltage	±5.0 Vdc
Input Impedance	Differential. Plus input greater than 10 MΩ; negative input with jumper, greater than 10 kΩ (negative input intended for use as an external ground sense; i.e., impedance from negative lead to computer ground < 20 Ω for given common mode rejection (CMR) specification).
Output Format	Parallel data, 10 bits, right justified, and sign extended 2's complement
Common Mode Rejection	At least 35 dB at 60 Hz. Common mode voltage less than 5V to ground
Resolution	0.1% (1 bit in 1024)
Accuracy	0.2% of full scale*
Conversion Rate	50 kHz maximum
Power Requirements	±5 Vdc ± 10% 1A, +15 Vdc ± 0.1% 150 mA, -15 Vdc ± 0.1% 150 mA
Temperature Stability**	0.01% full scale/°C

(continued on next page)

Table 1-1 (Cont)
LAB-8/E System Specifications

Equipment	Specifications
Analog Multiplexer (AM8-EA)	
Input Voltage	Differential ± 1V; 16 channels, maximum
Input Impedance	Non-inverting input is 70 kΩ in parallel with 300 pF. Inverting input is 35 kΩ in parallel with 300 pF.
Common Mode Rejection	Greater than 25 dB, 35 dB typical
Overload Protection	±67V from fault line
Overload Recovery Time	8 μs
Frequency Response	Flat from 0 to 30 kHz, -3 dB at 60 kHz
Leakage Current	Negligible at 70k impedance
Temperature Stability**	0.01% full scale/°C
Output	±5V full scale, single-ended, 0.2% accuracy*
Point-Plot Display Control (VC8-E)	
Input Format	10 bits of data in 2's complement format
Output Voltage	+5.01 to -5.01 ± 0.1 Vdc offset (adjustable)
Resolution	10 mV ± 2.5 mV
Slewing Speed	1.25 V/μs
Driving Capability	Capable of driving loads greater than 1 kΩ minimum, in parallel with 5000 pF; i.e., 100 ft of 50 pF/ft cable
Power Requirements	+5 Vdc = 10% 1A, +15 Vdc ± 0.1% 150 mA, -15 Vdc ± 0.1% 150 mA
Z Axis Intensity Pulse	1 μs, + 4V to -2V or + 4V to -10V positive- or negative-going
Buffered Digital I/O (DR8-EA) Programmable Input and Output	
Input	12 parallel bits or 12 independent bits selected by jumpers.
Output	12 parallel buffered bits or 12 independent bits
Input Levels	TTL compatible levels. Input lines are clamped at +5V for positive input protection. Input source must sink 3 mA in the 0 (true) state.
Output Levels	TTL compatible levels. Outputs can sink 20 mA in the 0 (true) state.
Power Requirements	+5V, 2.25A (worst case)
Programmable Real-Time Clock (DK8-EP)	
Control	20 MHz crystal controlled
Schmitt Triggers	Three threshold detectors that accept pulse or varying analog inputs (±5V variations)

(continued on next page)

Table 1-1 (Cont)
LAB-8/E System Specifications

Equipment	Specifications
Programmable Real-Time Clock (DK8-EP) (Cont)	
Input	±50V maximum differential input, 50 kΩ. Input impedance, common mode rejection 35 dB
Input Pulse Width	Minimum input pulse width 2 μs
Propagation	60 ns
Time Base	Programmable time base, rate set in clock. Enable Register 1 MHz to 100 Hz
Slope	± switch selectable
Data Format	12 parallel bits

* Overall system accuracy with AD8-EA and AM8-EA is 0.3% full scale.
** Overall system temperature stability with AD8-EA and AM8-EA is ± 0.02% full scale/°C.

1.3 PHYSICAL DESCRIPTION

The LAB-8/E System is available in rack-mounted and table-top configurations. Both configurations can be installed in a small space for easy operation and maintenance, and can be expanded as the user's requirements are increased.

The rack-mounted version of the LAB-8/E allows the user to place the processor and an assortment of peripherals in one area. The basic cabinet (see Figure 1-2) will hold all of the peripherals in the basic LAB-8/E System. The two pairs of frame uprights have 9/32 in. holes drilled at standard EIA spacings (5/8 – 5/8 – 1/2) the full length of the 63 in. mounting panel height. The processor and peripherals can be installed on slides to allow easy access for maintenance and troubleshooting. The cabinet has a filter cover for equipment ventilation.

The table-top LAB-8/E requires less space than the rack-mounted version. The table-top version, placed on a desk or table-top puts all controls within easy reach of the operator. The display or other peripherals can be installed in a system-expander box and placed alongside the processor. This configuration will allow the user to sit at his desk, operate the LAB-8/E, and have access to all controls on the processor and display units.

1.4 DOCUMENTATION

Computer handbooks, maintenance manuals, and engineering drawings are supplied with the LAB-8/E to assist the operation and maintenance personnel. A list of the documents necessary for the LAB-8/E System is provided in Table 1-2. Some of the documents listed are used for only one option and will not be shipped with the system if that option was not purchased. Additional copies of these documents may be purchased from Direct Mail, Digital Equipment Corporation, Maynard, Massachusetts 01754.

Figure 1-2 LAB-8/E Rack-Mounted Version

Table 1-2
LAB-8/E Handbooks, User's Manuals, Maintenance Manuals, and Engineering Drawings

Title and Document No.	Description
LAB-8/E User's Handbook DEC-LB-HRZA-D	Provides installation, system description and operating instructions for the LAB-8/E System.
PDP-8/E Maintenance Manual DEC-8E-HRIB-D	Installation, acceptance test theory of operation, and maintenance procedures, programming data for LAB-8/E processor
PDP-8/E Small Computer Handbook — 1972	PDP-8/E options, interface, installation, and DEC support services
VR14 CRT Display User's Manual DEC-12-HRZA-D	Provides operation, maintenance, and interfacing information for the VR14 display.
33 ASR Teletype Operators Manual Bulletin 273B, Volume 1	Provides operation and maintenance information for the Teletype Model 33 ASR.
A-ML-VC8-E Print Set	Prints for Point-Plot Display Control modules (M869 and M885)
A-ML-DK8-EP-0	Prints for Real-Time Clock and Schmitt trigger modules (M860 and M518)
A-ML-DK8-ES-0	Prints for Real-Time Clock Input and Output Panel
A-ML-DR8-EA-0	Print set for Buffered Digital I/O module (M863)
A-ML-AM8-EA-0	Print set for Analog Multiplexer module (A232)
A-ML-AD8-EA-0	Print set for A/D Converter modules (A841 and A231)
A-ML-AM8-ED-0	Print set for Analog Input Panel with two DEC 25-pin connectors
A-ML-AM8-EC-0	Print set for Analog Input Panel with two DEC 25-pin connectors, phone jacks, and potentiometers on channels 0 octal through 3 octal
A-ML-AD8-ES-0	A/D Converter and AM8-ED panel (modules A231 and A841)
A-PL-DR8-EB-0 D-UA-DR8-EC-0	Prints for Buffered Digital I/O panel assembly with M904 and M953 modules
A-ML-LAB-8/E-0	Print set for LAB-8/E
845X 00471 1513/C03/2.5	LAB-8/E Programming Card

CHAPTER 2
INSTALLATION

This chapter contains supplementary information and procedures for installation of the LAB-8/E System. Basic installation and planning information, such as space requirements, installation requirements, and system configuration is provided in Chapter 11 of the *PDP-8/E Small Computer Handbook* and Chapter 2 of the *PDP-8/E Maintenance Manual*. Installation functions and requirements are summarized in Table 2-1 of this manual. I/O cabling requirements and cables supplied by DEC for use in interfacing with the LAB-8/E and connecting options to each other are listed in Paragraph 2.2.

Table 2-1
Summary of Installation Functions

Responsibility	Function
User	Identify space and power required for system configuration.
User/DEC Representative	Survey proposed site.
User	Prepare site in accordance with environmental space and power requirements.
User/DEC Representative	Unpack equipment and check inventory checklist.
DEC Representative	Install equipment.

2.1 SITE CONSIDERATIONS

Adequate site planning and preparation can simplify the installation process and result in an efficient, more reliable LAB-8/E installation. DEC Sales Engineers or Field Service Engineers are available for consultation with user personnel regarding the installation.

Site planning should include a list of the actual components to be used in the installation and a list of such items as storage cabinets, Teletype supplies, work tables, peripherals, etc.

Primary planning considerations are:

a. The availability and locations of adequate power
b. Protection against direct heat sources
c. Electrical-noise radiation
d. Protection from shock
e. Existence of fire protection devices

2.1.1 Power Source

The power source should be free of conductive interference. DEC offers a line filter, as an option, to provide an interference-free power source. All computer system supplies should be connected to the same power source to avoid loading and source differentials that may affect operation.

2.2 I/O PANELS AND CABLING REQUIREMENTS

The cabling for table-top and rack-mounted computers differs slightly. For rack-mounted equipment, cables can be routed into the cabinet through a panel located at the bottom of the cabinet. Subflooring is not necessary because casters elevate the cabinet enough to provide sufficient cable clearance. For table-top models, cables are routed from the lower rear side through the adjustable strain relief of the processor. All cabling should be located where it cannot be damaged. This is especially important if the processor and peripherals are not in proximity.

The A/D converter, multiplexer, digital I/O, and the point-plot display require additional cabling and panels for interface with the outside world. The following paragraphs discuss each of the LAB-8/E peripherals and their special cabling requirements.

2.2.1 A/D Converter Connections

The A/D converter provides a differential input capable of 35-dB rejection of common-mode noise at 60 Hz. Inputs can be single-ended or differential. For differential connections, potential between input source and chassis ground must be less than 5V, and the impedance from negative input to computer ground should be less than 20 Ω. Figures 2-1 and 2-2 show the two input wiring schemes.

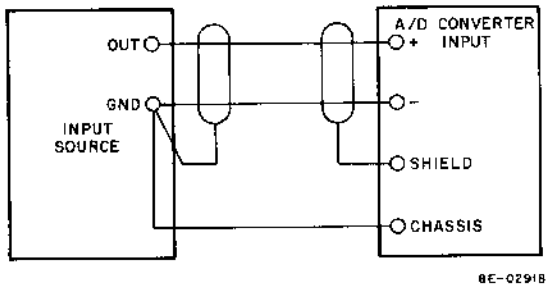


Figure 2-1 Single-Ended Measurement Connection

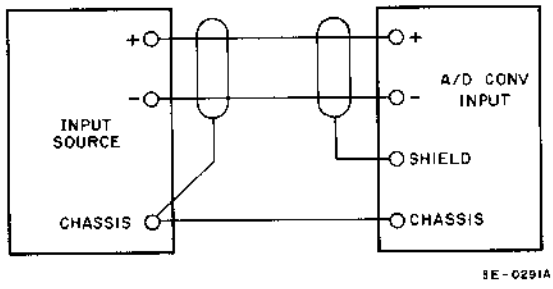


Figure 2-2 Differential Input Measurement Connection

The AM8-ED and the AM8-EC Analog Input Panels (see Figures 2-3 and 2-4), and a cable are available for use with the A/D converter. The AM8-ED panel provides the user with two DB-25S receptacles (see Figure 2-5). This provides ample inputs for a maximum configuration 16-channel system. The same panel is supplied with an AD8-ES option where the single input is wired into channel 0 of the panel. Field expansion with AM8-EA (two maximum) options can utilize the same panel for signal inputs. Two DEC 12-05886 DB-25P connectors are supplied with these options. The second panel available, the AM8-EC analog panel, is similar to the first type, except that parameter potentiometers are supplied for channels 0 through 3.

The potentiometers, with ±1 Vdc applied, are useful for varying thresholds and moving pointers across display tubes. The ±1 Vdc inputs to channels 0 through 3 can be disconnected from the potentiometers by installing a 3-conductor 1/4 in. phone jack (DEC No. 12-09430) in the proper channel. Four phone jacks are supplied with each AM8-EC panel. Table 2-2 and Figure 2-5 show pin connections on the AM8-ED and AM8-EC panels. The wiring of channels 10 to 17 on both panels is identical to the wiring of channels 0 through 7 on the AM8-ED panel, except that channel 0 corresponds to channel 10, 1 to 11, etc.

Figure 2-3 AM8-ED Analog Input Panel

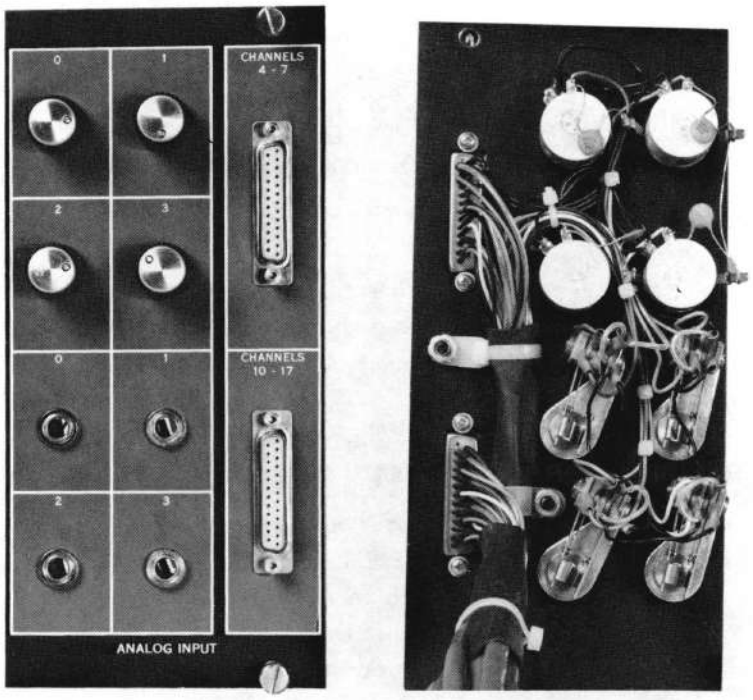


Figure 2-4 AM8-EC Analog Input Panel, Front and Rear View

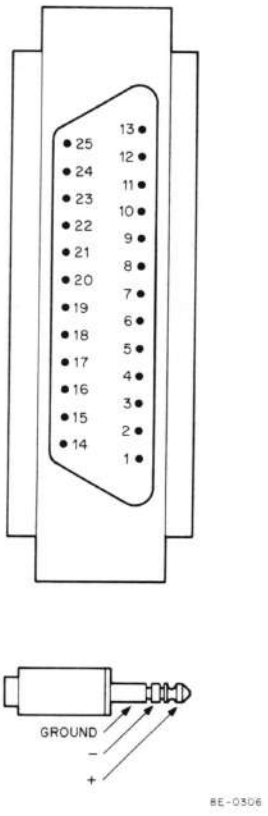


Figure 2-5 Front View of DB-25S Connector and Telephone Plug

Table 2-2
AM8-ED and AM8-EC Analog Panel Pin Connections

Channel Number	Input	Pin on AM8-ED	Pin on AM8-EC
0	+	1	Phone plug
	–	2	Phone plug
	Shield	3	Phone plug
1	+	4	Phone plug
	–	5	Phone plug
	Shield	6	Phone plug
2	+	7	Phone plug
	–	8	Phone plug
	Shield	9	Phone plug
3	+	10	Phone plug
	–	11	Phone plug
	Shield	12	Phone plug
4	+	14	1
	–	15	2
	Shield	16	3
5	+	17	4
	–	18	5
	Shield	19	6
6	+	20	7
	–	21	8
	Shield	22	9
7	+	23	10
	–	24	11
	Shield	25	12

A 7008533 cable is also available for analog input connections; Table 2-3 shows the connections for this configuration. No analog panel is required when this cable is used.

The A/D converter can also receive inputs from the AM8-EA Preamplifier and Multiplexer via an edge connector. When the AM8-EA is used, the cables from the analog panel or the 7008533 cable will be connected to the AM8-EA module.

Table 2-3
Analog Connection Using 7008533 Cable

Channel Number	Input	Cable Number	Wire Color
0	+	1	Red
	−		Black
	Shield		Drain
1	+	1	Green
	−		Black
	Shield		Drain
2	+	1	White
	−		Black
	Shield		Drain
3	+	2	Red
	−		Black
	Shield		Drain
4	+	2	Green
	−		Black
	Shield		Drain
5	+	2	White
	−		Black
	Shield		Drain
6	+	3	Red
	−		Black
	Shield		Drain
7	+	3	Green
	−		Black
	Shield		Drain

NOTE: Channel 10 is the same as channel 0, 11 as 1, etc.

2.2.2 Buffered Digital I/O Connections

The Buffered Digital I/O provides 12 digital inputs and 12 digital outputs for the LAB-8/E System. Inputs and outputs are TTL compatible (low true), giving the user the option of providing level converters or signal conditioners. Each input may monitor the external line directly, or may sense the occurrence of a negative-going transition. Skip and Interrupt capabilities are provided for the Input Register.

Two ways of interfacing to the Buffered Digital I/O are available. The first is by two BC08J-X cables. Each of these cables is a ribbon type, terminated by a Berg connector on one end and a standard DEC cable connector module on the other end. One cable is used for input and the other for output. See Table 2-4 for cable pin assignments. The second interface is by way of the DR8-EB panel which contains two H807 module connectors. A standard M904 is used for cable connection. The DR8-EB panel is NIM-dimensionally compatible and may be used in the DEC H945 Laboratory Expander Box or any NIM BIN. Table 2-5 shows correct configuration for connection to the DR8-EB panel.

Table 2-4
BC08J-X Connection and Bit Assignments

Bit No.	Pin No.	Bit No.	Pin No.
0	B1	6	H1
1	D2	7	K2
2	D1	8	J1
3	E2	9	M2
4	E1	10	L1
5	H2	11	P2

Grounds A1, C1, F1, K1, N1, R1, T1, C2, F2, J2, L2, N2, R2, U2

Table 2-5
Connections For DR8-EB Panel Assembly

Bit No.	Pin No.	Bit No.	Pin No.
0	V2	6	P2
1	S1	7	L1
2	T2	8	M2
3	P1	9	J1
4	S2	10	K2
5	M1	11	H1

Grounds A1, C1, F1, K1, N1, R1, T1, C2, F2, J2, L2, N2, R2, U2

2.2.3 Real-Time Programmable Clock Input Connections

Inputs to the clock are supplied by a DK8-EF panel containing three cables which connect to the M518 module. Inputs and outputs to the panel are supplied by three phone jacks and five BNC connectors. Table 2-6 shows the panel connectors and pins.

Table 2-6
Real-Time Programmable Clock Connections

Panel Connector	Description	Pin
In 1*	Schmitt trigger, 1-Input	(+) Plug tip (−) Plug center (ground) Shell
In 2	Schmitt trigger, 2-Input	(+) Plug tip (−) Plug center (ground) Shell
In 4	Schmitt trigger, 4-Input	(+) Plug tip (−) Plug center (ground) Shell
Out 1	Schmitt trigger, 1-Output	BNC
Out 2	Schmitt trigger, 2-Output	BNC
Out 4	Schmitt trigger, 4-Output	BNC
Ext. Clock In**	User-supplied clock frequency	BNC
Overflow	Clock-overflow bit output	BNC

*Each slope switch and threshold potentiometer determines the input slope and firing voltage of the respective Schmitt trigger.

**Rate Select 001 chooses the External Clock In as the time base rather than internal timing (see Paragraph 4.6.2.3).

2.2.4 Point-Plot Display (VC8-E) Control Connections

The VC8-E interfaces with the VR14 by means of the BC01K cable, and with the Tektronix 602 by means of the BC01L cable. Both cables connect to a Berg connector on the M885 module. A 7008499 Cable Assembly is supplied with basic systems when an oscilloscope is not purchased to connect to the M885 module. Table 2-7 shows connections for each of the cable assemblies used on the VC8-E. All three cables have a DB-25P connector to connect to the DB-25S Berg connector on the VC8-E.

Table 2-7
VC8-E Cable Connections

VC8-E Signal Name	Berg Connector Pin	BC01K* 25-Pin Side	BC01L*	7008499 Wire Color	VR14 Signal Name**
CHANNEL L	Z	1		Green	Z SELECT
Shield	U	2		Shield	Chassis ground
LOGIC GROUND	BB	3		Black	Chassis ground
Z AXIS	X	4	Z BNC	Red	Z INPUT
Shield	Y	5		Shield	Chassis ground

*Connection of cable determined by user.

**See the *VR14 CRT Display User's Manual*, page 2-5, for more information on pin assignments.

(continued on next page)

Table 2-7 (Cont)
VC8-E Cable Connections

VC8-E Signal Name	Berg Connector Pin	BC01K* 25-Pin Side	BC01L*	7008499 Wire Color	VR14 Signal Name**
LOGIC GROUND	V	6	Z BNC	Black	Chassis ground
X ANALOG	D	7	X BNC	Green	+ X INPUT
ANALOG GROUND	F	8	X BNC	Black	− X INPUT
Shield	C	9		Shield	± X INPUT SHIELD
Y ANALOG	L	10	Y BNC	Red	+ Y INPUT
ANALOG GROUND	N	11	Y BNC	Black	− Y INPUT
Shield	K	12		Shield	± Y INPUT SHIELD
		13			

*Connection of cable determined by user.
**See the *VR14 CRT Display User's Manual*, page 2-5, for more information on pin assignments.

2.3 FIRE AND SAFETY PRECAUTIONS

The power supplies for the LAB-8/E contain a thermal cut-out switch, a circuit breaker, and fuses for protection against overheating and overloading. The thermal cut-out switch will remove the ac input when the temperature reaches 90 ± 5°C. The *PDP-8/E Maintenance Manual* lists the fusing and circuit breakers used on power supplies in Paragraph 3.5. Both the cabinets and power receptacle must be adequately grounded to ensure safe operation. A water pipe or steel beam provides an adequate ground. Refer to Chapter 11 of the *PDP-8/E Small Computer Handbook* for grounding and power installation procedures.

WARNING
The frame of the computer must be grounded to protect personnel from dangerous electrical shock.

Grounding is usually automatically achieved if a 3-wire plug is used; however, a voltage reading from ground to frame should be performed during installation.

Electrical fires, although extremely unlikely, should be extinguished by a Class 3 (CO_2) fire extinguisher.

2.4 INSTALLATION PROCEDURES

Installation of a LAB-8/E requires only normal hand tools. No special tools or equipment are necessary; however, a fork lift, truck, or pallet handling equipment should be available for installing the rack-mounted system.

NOTE
Refer to the *PDP-8/E Maintenance Manual* for processor installation.

2.4.1 Unpacking and Inspection

Unpack and inspect the LAB-8/E using the following procedure:

CAUTION
Do not attempt to unpack or install the system until the DEC Sales Office has been notified and a Field Service Representative is present. This is required to validate the warranty.

Step	Procedure
1	Remove the packing material.
2	Visually inspect system.
3	Inventory all components and accessories. Refer to the tables listed below for a list of items to be shipped with each option.

a. AD8-EA Table 2-8
b. AD8-ES Table 2-9
c. AM8-EA Table 2-10
d. AM8-EC Table 2-11
e. AM8-ED Table 2-12
f. DK8-EF Table 2-13
g. DK8-EP Table 2-14
h. DK8-ES Table 2-15
i. DR8-EA Table 2-16
j. DR8-EB Table 2-17
k. DR8-EC Table 2-18
l. VC8-E Table 2-19
m. VM03 Table 2-20

Table 2-8
AD8-EA Accessory and Component List

Item Number	Identification Number	Description	Quantity	
			AD8-EA Alone	AD8-EA with AM8-EA, ED, or EC
1	A231	AD8-EA control module	1	1
2	A841	10-bit A/D converter module	1	1
3	H851	Edge connector	2	2
4	7008533	Analog cable assembly	1	–
5		Analog HQ power supply assembly	*	*
	7008370-1	115 Vac table-top mounting		
	7008370-2	230 Vac table-top mounting		
	7008477-1	115 Vac rack mounting		
	7008477-2	230 Vac rack mounting		
6	7008375	Analog power cable	1	1
7	AD8-EA-0	AD8-EA master drawing set	1	1
8	LAB-8/E	LAB-8/E master drawing set	1	1
9	MAINDEC-8E-D6BB-PB	AD8-EA/AM8-EA diagnostic binary tape	1	1
10	MAINDEC-8E-D6BB-D	AD8-EA/AM8-EA diagnostic document	1	1
11	DEC-LB-HRZA-D	*LAB-8/E User's Handbook*	1	1
12	DEC-LB-HXZA-D	*LAB-8/E Maintenance Manual*	1	1
13	845X 00471 1513/C-03	LAB 8/E programming card	1	1

*Item number 5 is not to be supplied to system in the field with a VC8-E installed. HQ power supply type and part number are tailored to a specific system in systems production.

Table 2-9

AD8-ES Accessory and Component List

Item Number	Identification Number	Description	Quantity
1	A231	AD8-ES control module	1
2	A841	10-Bit A/D converter module	1
3	H851	Edge connector	2
4	7008386	LAB-8/E simple analog input assembly	1
5	12-05886	DB-25P connector	2
6	12-05885	DB-51226-1 hood	2
7		Analog HQ power supply assembly	*
	7008370-1	115 Vac table-top mounting	
	7008370-2	230 Vac table-top mounting	
	7008477-1	115 Vac rack mounting	
	7008477-2	230 Vac rack mounting	
8	7008375	Analog power cable	1
9	AD8-ES-0	AD8-ES master drawing set	1
10	LAB-8/E	LAB-8/E master drawing set	1
11	MAINDEC-8E-D6BB-PB	AD8-EA/AM8-EA diagnostic binary tape	1
12	MAINDEC-8E-D6BB-D	AD8-EA/AM8-EA diagnostic document	1
13	DEC-LB-HRZA-D	*LAB-8/E User's Handbook*	1
14	DEC-LB-HXZA-D	*LAB-8/E Maintenance Manual*	1
15	845X 00471 1513/C-03	LAB-8/E programming card	1

*Item number 7 is not to be supplied to systems in the field with a VC8-E already installed. HQ power supply type and part number are tailored to a specific system in systems production.

Table 2-10

AM8-EA Accessory and Component List

Item Number	Identification Number	Description	Quantity	
			AM8-EA Alone	AM8-EA with AM8-EC or AM8-ED
1	A232	Analog Preamplifier and Multiplexer Expander	1	1
2	H851	Edge connector	1	1
3	7008533	Analog cable	1	0
4	AM8-EA-0	AM8-EA master drawing set	1	1
5	D-IA-7008533-0-0	Analog cable assembly drawing	1	0

Table 2-11
AM8-EC Accessory and Component List

Item Number	Identification Number	Description	Quantity
1	7008387	LAB-8/E Analog Input Assembly	1
2	AM8-EC-0	Analog panel master drawing set	1
3	12-05886	DB-25P connector	2
4	12-05885	DB-51226-1 hood	2
5	12-09430	Phone plug, Switchcraft No. 90	4

Table 2-12
AM8-ED Accessory and Component List

Item Number	Identification Number	Description	Quantity
1	7008386	LAB-8/E simple analog input assembly	1
2	AM8-ED-0	Simple analog input assembly print set	1
3	12-05886	DB-25P connector	2
4	12-05885	DB-51226-1 hood	2

Table 2-13
DK8-EF Accessory and Component List

Item Number	Identification Number	Description	Quantity
1	7008382	LAB-8/E clock assembly panel	1
2	7008492	DK8-EP diagnostic cable assembly	1
3	D-CS-7008382-0-1	DK8-EF circuit schematic	1
4	A-PL-DK8-EF-0	DK8-EF panel parts list	1
5	12-01455	BNC plug, Amphenol No. 31-002	5
6	12-09430	Phone plug, Switchcraft No. 90	3
7	A-PL-7008382-0-0	Real-Time Clock assembly parts list	1

Table 2-14
DK8-EP Accessory and Component List

Item Number	Identification Number	Description	Quantity
1	M518	Schmitt trigger module	1
2	M860	Real-Time Clock Control module	1
3	H851	Edge connector	1
4	DK8-EP	DK8-EP master drawing list	1
5	LAB-8E	LAB-8/E master drawing	1
6	MAINDEC-8E-D8AB-PB	DK8-EP diagnostic binary tape	1
7	MAINDEC-8E-D8AB-DL	DK8-EP diagnostic document	1
8	DEC-LB-HRZA-D	*LAB-8/E User's Handbook*	1
9	DEC-LB-HXZA-D	*LAB-8/E Maintenance Manual*	1
10	845X 0047 1513/C-03	LAB-8/E programming card	1

Table 2-15
DK8-ES Accessory and Component List

Item Number	Identification Number	Description	Quantity
1	M518	Schmitt trigger module	1
2	M860	Real-Time Clock Control module	1
3	H851	Edge connector	1
4	7008382	LAB-8/E clock panel assembly	1
5	7008492	DK8-EP diagnostic cable assembly	1
6	12-01455	BNC plug, Amphenol No. 31-002	5
7	12-09430	Phone plug, Switchcraft No. 90	3
8	DK8-ES-0	DK8-ES master drawing set	1
9	MAINDEC-8E-D8AB-PB	DK8-EP diagnostic binary tape	1
10	MAINDEC-8E-D8AB-DL	DK8-EP diagnostic document	1
11	DEC-LB-HRZA-D	*LAB-8/E User's Handbook*	1
12	DEC-LB-HXZA-D	*LAB-8/E Maintenance Manual*	1
13	845X 00471 1513/C-03	LAB-8/E programming card	1
14	LAB8-E-0	LAB-8/E master drawing list	1

Table 2-16
DR8-EA Accessory and Component List

Item Number	Identification Number	Description	Quantity
1	M863	12-channel Buffered Digital I/O module	1
2	BC08S-1	1-ft I/O cable assembly	1
3	BC08J-10	10-ft I/O cable assembly	2
4	DR8-EA	DR8-EA master drawing list	1
5	LAB8-E	LAB8-E master drawing set	1
6	MAINDEC-8E-D0OA-PB	DR8-EA diagnostic binary tape	1
7	MAINDEC-8E-D0OA-DL	DR8-EA diagnostic document	1
8	DEC-LB-HRZA-D	*LAB-8/E User's Handbook*	1
9	DEC-LB-HXZA-D	*LAB-8/E Maintenance Manual*	1

Table 2-17
DR8-EB Accessory and Component List

Item Number	Identification Number	Description	Quantity
1	7008388	Digital I/O panel assembly	1
2	BC08R-12	12-ft I/O cable assembly	1
3	M904	Coaxial cable connector module	2
4	A-PL-DR8-EB-0	DR8-EB parts list	2
5	D-UA-DR8-EC-0	DR8-EC unit assembly drawing	1
6	DEC-LB-HRZA-D	*LAB-8/E User's Manual*	1

Table 2-18
DR8-EC Accessory and Component List

Item Number	Identification Number	Description	Quantity
1	M863	12-channel Buffered Digital I/O module	1
2	BC08R-12	12-ft I/O cable assembly	2
3	7008388	Digital I/O panel assembly	1
4	M904	Coaxial cable connector module	2
5	BC08S-1	1-ft I/O cable	1
6	DR8-EC	DR8-E digital I/O master set	1
7	LAB-8/E	LAB-8/E master list	1
8	MAINDEC-8E-D0OA-RB	DR8-EA diagnostic binary tape	1
9	MAINDEC-8E-D0OA-DL	DR8-EA diagnostic document	1
10	DEC-LB-HRZA-D	*LAB-8/E User's Handbook*	1
11	DEC-LB-HXZA-D	*LAB-8/E Maintenance Manual*	1

Table 2-19
VC8-E Accessory and Component List

Item Number	Identification Number	Description	Quantity		
			VC8-E only	VC8-E and VR14	VC8-E and VM03
1	M869	VC8-E Point-Plot Display Control module	1	1	1
2	M885	Point-Plot Display Control, D/A module	1	1	1
3	H851	Edge connector	2	2	2
4	7008499	User display cable	1	0	0
5	BC01K	VR14 display cable	0	1	0
6	BC01L	Tektronix 602 Display cable	0	0	1
7		Analog HQ power supply assembly	*	*	*
	7008370-1	115 Vac table-top mounting			
	7008370-2	230 Vac table-top mounting			
	7008477-1	115 Vac rack mounting			
	7008477-2	230 Vac rack mounting			
8	7008375	Analog power cable	1	1	1
9	VC8-E	VC8-E master drawing set	1	1	1
10	LAB-8/E	LAB-8/E master list	1	1	1
11	MAINDEC-8E-D6CA-PB	VC8-E diagnostic binary tape	1	1	1
12	DEC-LB-HRZA-D	*LAB-8/E User's Handbook*	1	1	1
13	DEC-LB-HXZA-D	*LAB-8/E Maintenance Manual*	1	1	1
14	845X 00471 1513/C-03	LAB-8/E programming card	1	1	1

*Item number 7 is not to be supplied to systems in the field with an AD8-EA already installed. The HQ power supply type and number are tailored to a specific system in systems production.

Table 2-20
VM03 Accessory and Component List

Item Number	Identification Number	Description	Quantity
1	74-08919	Single panel	1
2	74-08926	Oscilloscope support	1
3	74-08927	Oscilloscope brace	1
4	74-08931	Front panel	1
5	BC01L-10	10-ft oscilloscope cable assembly	1
6	1-300479	Resistor 10 KΩ, 1/4W 5% CC	2
7	1-300365	Resistor 1 KΩ, 1/4W 5% CC	2
8	1-300510	Resistor 33 KΩ, 1/4W 10% CC	1
9	1-301327	Resistor 68 KΩ, 1/4W 5% CC	1
10	1-000026	Capacitor 680 MMF, 100V 5% DM	2
11	74-09544	High voltage oscilloscope cover	1
12	74-09545	Hold-down bracket	2
13	VM03-0	VM03 master drawing set	1

2.4.2 Installation Procedure

NOTE

Refer to Step 13 for procedure needed to install each of the LAB-8/E options as they are added to the basic system. Table 2-21 shows recommended module positions.

Table 2-21
Recommended LAB-8/E Module Installation Positions

Module	Description
KC8/E	Control Panel
M833	Timing Board
M8340	Extended Arithmetic Element (EAE)
M8310	Central Processor Major Register Control
M8300	Central Processor Major Registers
M837	Extended Memory and Time Share Control
⋮	⋮
M869	Point-Plot Display Control
M885	Digital-to-Analog Converter
A841	Analog-to-Digital Converter
A231	Analog-to-Digital Control Module
A232	Analog Multiplexer Expander
M860	Real-Time Clock
M518	Schmitt Triggers
M863	Buffered Digital I/O
M835	External I/O Bus Interface
M849	RFI Shield
G104	Memory Sense Inhibit (0)

(continued on next page)

Table 2-21 (Cont)
Recommended LAB-8/E Module Installation Positions

Module	Description
H220	Memory Stack (0)
G227	Memory X/Y Drivers (0)
G104	Memory Sense Inhibit (n)
H220	Memory Stack (n)
G227	Memory X/Y Drivers (n)
	⋮
	Other Memories
G105	Memory Sense/Inhibit (Parity)
H220	Memory Stack (Parity)
G227	Memory X/Y Drivers (Parity)
M832	Bus Loads (always in last slot)

Install the LAB-8/E using the following procedures:

Step	Procedure
1	Ensure all ac power is supplied by one source.
	WARNING **Do not touch computer after plugging it in, until it is checked for proper ground.**
2	Connect ac power.
3	Before touching computer, check frame-to-ground voltage. If a voltage is read, disconnect power and check power and ground cables before continuing.
4	Connect ac power.
5	Turn on computer power switch and circuit breaker.
6	Check dc voltage at output of H724 power supply. See *PDP-8/E Maintenance Manual* for voltages and monitoring points. Cover must be removed from power supply for access to test points.
7	Turn off computer power switch.
8	Install HQ power supply on back of cabinet for rack-mounted system, or in H945 option box for table-top system.
9	Connect HQ power ac input cable.
	NOTE **HQ power for 115 Vac system indicated by −2, and 240 Vac indicated by −4 after part number on power supply.**
10	Connect HQ power supply to A231 or M869 module in this order.
11	Turn on computer power and measure HQ power supply voltages with a dc voltmeter. Voltages and monitoring points are shown in Table 2-22.

(continued on next page)

Table 2-22
High Quality Power Supply Parameters

Output Voltage*	Wire Color	Minimum Voltage	Maximum Voltage	Current Rating	Maximum Ripple
+15V	Orange	+14.985	+15.015	1.5A	1 mV rms
-15V	Blue	-14.985	-15.015	1.5A	1 mV rms

*When installing the system in the field, a crude measurement (±5%) of HQ power ±15V may be made to assure proper operation of the supply. If the HQ power supply is replaced, a precision measurement should be made to the specifications in this table. The 7008375 HQ power cable must be plugged into a module to join the voltage-sense lines before measurements are made.

Step	Procedure
12	Turn off power.
13	Check module positions with Table 2-21 and install modules. Refer to the steps indicated below for installation of specific LAB-8/E options:

Option	Step to Install
a. AD8-EA	14
b. AM8-EA, EC, ED	15
c. VC8-E	16
d. DR8-EA, EB, EC	17
e. DK8-EP, ES	18
f. VM03	19
g. VR14	20
h. RM503	21

NOTE
The recommended order of modules on the OMNIBUS will result in best-case timing and permit widest margins.

14 Install AD8-EA as follows:

a. If HQ power supply is not installed, install the HQ power assembly 7008370 in second OMNIBUS mounting holes on basic cabinet or in the H945 option box in the expanded system. Assembly 7008482 is to be installed in the rack-mounted system in back of the LAB-8/E cabinet.

NOTE
If AM8-EA is to be installed, remove jumper W1 on split lugs in upper right-hand corner of A841 module and install W2 jumper on the module.

b. Install A231 and A841 modules in the OMNIBUS. See Table 2-21 for recommended module positions.

c. Install edge connectors as shown in Figure 2-6.

d. Connect HQ power supply to Mate-N-Lok connector on the A231 module.

e. Connect ac input to HQ power supply.

(continued on next page)

Step	Procedure
14 (cont)	*f.* Connect analog input cable to Berg connector on the A841 module. If an AM8-EA preamplifier is installed, the analog input will be supplied by an edge connector from the A232 module.

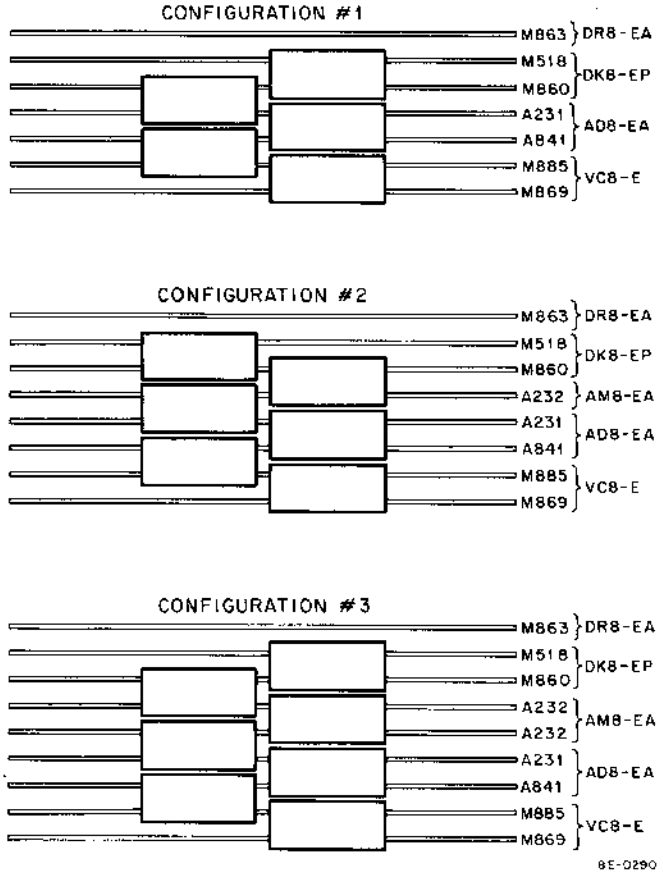


Figure 2-6 Edge Connector Installation (top view)

15 Install AM8-EA, AM8-EC, or AM8-ED as follows:

a. Install one or two A232 modules in the OMNIBUS. Refer to Table 2-21 for recommended module positions.

b. Install edge connectors as shown in Figure 2-6.

c. If an AM8-EC or AM8-ED front panel is installed, insert cable for channels 0 through 7 in the A232 module behind the A231 module. Insert cable for channels 10 through 17 in the second A232 module (see Table 2-2).

d. If front panels are not installed, connect the 7008533 cables supplied with the modules.

16 Install VC8-E as follows:

a. Set switches and install jumpers as shown in Table 2-23 if oscilloscope is used.

(continued on next page)

Step	Procedure
16 (cont)	*b.* If AD8-EA was not previously part of system, install HQ power supply (see Step 14 *a*) on back of cabinet for rack-mounted, or in H945 option box for table-top system. If BE8-E is not used, install power supply in the back of the OMNIBUS.
	c. Install M869 and M885 module in OMNIBUS. Refer to Table 2-21 for recommended module positions.
	d. Install edge connectors as shown in Figure 2-6.
	e. Connect HQ power supply cable to Mate-N-Lok connector on M869 module if AD8-EA is not installed.
	f. Check HQ power with a dc voltmeter (see Table 2-22).
	g. Connect cable to Berg connector on M885 module. Refer to Table 2-7 for cable to match system configuration.

NOTE

If two VC8-E options are installed, device selection code on one must be 05 and the other must be 15. The device code is selected by changing jumpers on the M869 module.

Table 2-23
Switch Requirements for VC8-E Modules

Oscilloscope	Z Switch	Delay Switch
VR14	Negative	Long
Tektronix 602	Positive	Short
RM503	Positive	Long

NOTE

On the RM503, remove W1 and install a jumper in AB.

17 Install DR8-EA, DR8-EB, or DR8-EC as follows:

NOTE

When more than one DR8-EA is installed, increment the IOTs to 51, 52, etc. A maximum of eight M863 modules can be installed in the system. If an AD8-EA is installed, device code 53 must not be used.

a. Ensure all flip-flop jumpers installed in the A position.

b. Ensure all Interrupt jumpers are installed in W1 to W12.

c. Ensure all IOT jumpers are in the H position (on device code 50 only).

d. Install M863 module in OMNIBUS. See Table 2-21 for recommended module positions on the OMNIBUS.

e. If the DR8-EB panel is not installed, connect BC08J cables to connectors marked INPUT and OUTPUT.

f. If the DR8-EB panel is installed, connect BC08R cables and the module adapters. See Table 2-5 for connections.

NOTE

Cable connection is standard on M863 module, but cable connected to front panel must be inserted with writing on cable plug adjacent to module (upside down).

(continued on next page)

Step	Procedure
18	Installation of DK8-EP or DK8-ES:

a. Install M860 and M518 in the OMNIBUS. Refer to Table 2-21 for module positions.

b. Install edge connectors as shown in Figure 2-6 for DK8-ES or DK8-EP.

c. If this is a DK8-ES, install DK8-EF front panel and connect front panel cable to M518 module.

19 Install VM03 modification kit for the Tektronix 602 oscilloscope as follows:

NOTE
See Table 2-24 for parts list.

a. Refer to page 2-3, Figure 2-2 in the Tektronix manual.

b. Remove the jumper wire from the stand-off pins on the X and Y deflection amplifier. Replace the jumpers (add in series) with a 10K resistor on the X and Y axis.

c. Install the 1K resistor and a 680 pF capacitor in the slots marked ADD SHUNT on the X and Y deflection amplifiers.

d. Refer to page 2-4, Figure 2-3 in the Tektronix manual. Remove the resistor and capacitor from the stand-off pins marked SERIES RESISTOR (Z axis).

e. Install the 33K resistor (shunt and 68K resistor in series).

f. Connect BC01L cable to VC8-E option.

NOTE
Refer to Paragraph 5.4.7 for calibration procedure.

Table 2-24
VM03 Tektronix 602 Modification Kit Parts List

Part	Quantity	Description	DEC Part No.
Resistor	2	10K, 1/4W, 5%	13-00479
Resistor	2	1K, 1/4W, 5%	13-00365
Resistor	2	33K, 1/4W, 10%	13-00510
Resistor	1	68K, 1/4W, 5%	13-01327
Capacitor	2	680 pF, 100V 5%	10-000026
Interface Cable	1		BC01L

20 Install VR14 oscilloscope as follows:

a. Install VR14 oscilloscope in the H945 equipment rack or place on a table beside the LAB-8/E if this is a table-top system.

b. Connect BC01K cable between VR14 and VC8-E (see Table 2-7).

(continued on next page)

Step	Procedure
20 (cont)	**CAUTION** **Ensure the intake and exhaust for equipment cooling are not blocked. Air is drawn in from the bottom of the unit and exits through the rear. The VR14 must not be pushed against a wall or other vertical surface which blocks the cooling air flow.**
	c. Connect ac power cable to the VR14.
	NOTE **Refer to the VR14 manual and Paragraph 3.2 of this manual for more information on the VR14.**
21	Install the RM503 as follows:
	a. Connect ac power to the RM503.
	b. Connect a 7008491 cable between the VC8-E and the RM503 oscilloscope.
	NOTE **Refer to the RM503 instruction manual for operation and calibration of the RM503.**
22	Turn on power.
23	Check HQ power for +15V on orange lead and −15V on blue lead.
	NOTE **Procedures for assembling and installing the PDP-8/E and the Teletype are in Chapter 2 of the *PDP-8/E Maintenance Manual*.**

2.5 ACCEPTANCE TEST

The acceptance test will check out the central processor and each of the LAB-8/E options to ensure that they function properly as a system. The acceptance test should be performed before operating the system, after installation is completed, and periodically thereafter to verify there has been no system deterioration or change in calibration of the analog units. If performance of the acceptance test indicates units are out of calibration, or should other problems develop, refer to Chapter 5 for calibration and troubleshooting procedures. Users are advised not to adjust the LAB-8/E System until they are familiar with the calibration and maintenance procedures, which should be followed closely to accomplish an accurate calibration.

The following paragraphs describe the procedures for testing the LAB-8/E System. All modules, connectors, panels, etc., should be installed as specified in Paragraph 2.4 before attempting the acceptance test.

The acceptance test diagnostics needed to check the LAB-8/E and its peripherals are shown in Table 2-25.

NOTE

All diagnostics require a programmer's console, a working Teletype, and at least 4K of memory with the basic system.

Table 2-25
LAB-8/E Acceptance Test Diagnostics

Program Name	DEC Diagnostic Number	SA/SR Setting	Execution Time	Acceptance Time
Instruction Test I & II	MAINDEC-8E-D0AA	200/000	2 sec	3 min
Instruction Test II	MAINDEC-8E-D0BA	200/000	2 sec	3 min
Adder Test	MAINDEC-8E-D0CA	200/000	35 min	35 min
Basic JMP JMS Test	MAINDEC-8E-D0IA	200/000	10 sec	3 min
Random TAD Test	MAINDEC-8E-D0EA	200/000	5 sec	3 min
Random AND Test	MAINDEC-8E-D0DA	200/000	2 sec	3 min
Random ISZ Test	MAINDEC-8E-D0FA	200/000	8 sec	3 min
Random DCA Test	MAINDEC-8E-D0GA	200/000	5 sec	3 min
Random Jump Test	MAINDEC-8E-D0JA	200/000	8 sec	3 min
Random JMP JMS	MAINDEC-8E-D0JA	200/000	11 sec	3 min
Memory Address Test	MAINDEC-8E-DLEA	200/000	50 sec	5 min
Checkerboard Test	MAINDEC-8E-DLAA	200/000	5 min	15 min
Teletype Control Test	MAINDEC-8E-02AA	200/000		40 min
Memory ON/OFF Test	MAINDEC-8E-DLGA	200/000		
Symbolic Tape Editor				
Real-Time Clock (DK8-EP) Test	MAINDEC-8E-D8AB	200/4000		2 passes
Buffered Digital I/O (DR8-EA) Test	MAINDEC-8E-D00A	200/000		10 min
Point-Plot Display Control (VC8-E)	MAINDEC-8E-D6CA	200/000		20 passes
A/D Converter (AD8-EA) and Analog Multiplexer (AM8-EA) Test	MAINDEC-8E-D6BA	200/000		20 passes

NOTE: When ordering from Program Library:

PB for Binary Tape
D for Document
} e.g., after MAINDEC-8E-D0AA-PB

2.5.1 Central Processor Acceptance Test

Perform the acceptance tests listed in Table 2-25. If abnormal indications are encountered, terminate testing and refer to Chapter 5 for maintenance procedures. The procedure to load the diagnostic programs is in Chapter 3.

NOTE

Refer to the *PDP-8/E Maintenance Manual* for information on the Central Processor Acceptance Test.

2.5.2 Analog-to-Digital Converter (AD8-EA) and Analog Multiplexer (AM8-EA) Acceptance Test

The AD8-EA and AM8-EA options are used in many configurations in the LAB-8/E; the configuration for each system is determined by the users needs. Table 2-26 shows the different options and the item designations in Paragraph 2.5.2.1 that contain the procedures to be followed to check each configuration.

Table 2-26
A/D Converter and Analog Preamplifier
and Multiplexer Acceptance Test

Option	Designation
AD8-EA	*A, B*
AD8-EA, AM8-ED	*A, B*
AD8-EA, AM8-EA	*A, C*
AD8-EA, AM8-EA, AM8-EC	*A, C, D*
AD8-EA, AM8-EA, AM8-ED	*A, C*
AM8-EA	*A, C*
DK8-E	*E*
DK8-E, VC8-E, VR14 or equivalent	*E, F*

2.5.2.1 Acceptance Test – The following steps will checkout all the configurations of the Analog-to-Digital Converter and Analog Preamplifier and Multiplexer options.

A. **Control Logic Test**

Step	Procedure
1	Load MAINDEC-8E-D68B-PB. Refer to diagnostic document, for loading instructions.
2	Set the switch register (SR) to 0200, depress ADDR LOAD, and then clear the switch register.
3	Depress the CLEAR key and then the CONT (continue) key.
4	When the program halts, set the SR to 0000, then continue.
5	After each pass, the program will print END OF LOGIC TEST (every 12 sec).
6	Run the test for 5 min.
7	Pass if there are no error printouts for the 5-min run.

B. **Accuracy Check – AD8-EA**

Step	Procedure
1	Ensure W1 and W2 are removed from the A841 module. Connect the Electronic Development Corporation (EDC) precision dc voltage source to the side connector on the A841 in a double-ended configuration as shown in Figure 2-7.

NOTE
Ensure the connections are properly made, or large errors may result. Connect test equipment to the processor.

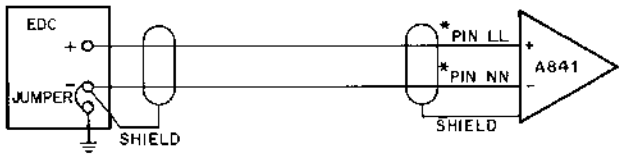


Figure 2-7 Analog Inputs for Accuracy Check

Step	Procedure
2	Connect a ground wire from the EDC voltage source chassis to the computer chassis.
3	Load 0202 into the switch register.
4	Clear the switch register, then depress CLEAR and CONT.
5	Check the switching points as listed in Table 2-27.

NOTE

Each point must fall within ±10 mV of the given theoretical voltage. Carefully check that the converter does not triple state.

Table 2-27
Switching Points and Theoretical Voltage Readings

Switching Point		Theoretical Voltage
From	To	± 10 mV
7000	7001	−4.995
7001	7002	−4.985
7003	7004	−4.966
7007	7010	−4.927
7017	7020	−4.849
7037	7040	−4.692
7077	7100	−4.380
7177	7200	−3.755
7377	7400	−2.505
7777	0000	−0.005
0000	0001	0.005
0001	0002	0.015
0002	0003	0.024
0377	0400	2.495
0577	0600	3.745
0776	0777	4.985

6	Pass if all switching points fall within ±10 mV of the theoretical voltage and triple stating is not observed.
7	Connect the input as shown in Figure 2-8.
8	Set the EDC voltage source to +5V, then set the polarity switch to −.

a. The Accumulator (AC) Register should be at full scale of 0777 ±2 counts.

b. Set polarity switch to + position; the AC Register should read 7000 ±2 counts.

C. Accuracy Test — AM8-EA

Step	Procedure
1	Connect the EDC voltage source to each channel in succession (see Tables 2-2 and 2-3).

(continued on next page)

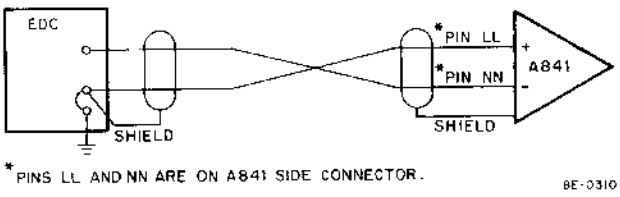


Figure 2-8 Negative Input Checkout

Step	Procedure
	NOTE **Ensure all connections are properly made or large errors may occur.**
2	Load 0202 into the switch register. *a.* Set the switch register to 0000. *b.* Depress CLEAR and CONT. *c.* Bits 8–11 determine the channel selected.
3	Check the voltages listed in Table 2-28 for each channel to be within the theoretical number ±2 counts.

NOTE
For AM8-EC panel, test the first four channels with phone plug removed by rotating the four potentiometers 0, 1, 2, and 3, and reading 7000_8 to 0777_8.

Table 2-28
Theoretical Voltage and Reading in the AC

Theoretical AC Reading ±2 Counts	Theoretical Voltage
7000	-1.000
7001	-0.9981
7002	-0.9962
7004	-0.9922
7010	-0.9844
7020	-0.9687
7040	-0.9375
7200	-0.7500
7400	-0.5000
0000	0.0000
0400	+0.500
0777	+0.998

4	Pass if all points on each channel fall within ±2 counts of the theoretical number.

NOTE
Connect negative terminal to the shield terminal on the EDC.

(continued on next page)

D. **Complex Analog Panel Test**

Step	Procedure
1	Connect the AM8-EC into the A232 module. Do not apply an input to the panel.
2	Load 0202 into the switch register. Depress ADDR LOAD.
3	Clear the switch register, then depress CLEAR and CONT. The AC Register is now displaying channel 00.
4	Rotate the potentiometer on the panel for channel 00. Ensure that from one end of the potentiometer to the other, the AC displays 7000 up to 0777.
5	Repeat steps 1 through 4 for channels 1 through 3. Select the next channel with SR8—11.

E. **External Start Test**

CAUTION

This test is to be performed only if the system configuration contains a DK8-EP clock option that has undergone prior acceptance testing.

Step	Procedure
1	Load address 0203 into the switch register. Depress ADDR LOAD.
2	Set the switch register to 0200, then depress CLEAR and CONT.
3	The Teletype bell should ring approximately every 4 sec for each pass. Run test for 1 min.
4	Pass if no error printout for 1 min.

F. **System Test**

CAUTION

This test is to be performed only if the system configuration contains a DK8-EP, a VC8-E, and a VR14 display oscilloscope that have undergone prior acceptance testing.

Step	Procedure
1	Load 0210 into the switch register. *a.* Depress ADDR LOAD. *b.* Clear the switch register.
2	Depress CLEAR, then CONT. Program will halt.
3	Set the desired clock frequency into SW3—5 of the switch register. Refer to LAB-8/E programming card for SR setting and frequency.
4	Depress CONT.
5	Follow the instructions that are printed out. *a.* For a system with the AD8-EA and AM8-EA, the switch register would be set to 0107.

(continued on next page)

Step	Procedure
	NOTE **Unless a voltage is applied to every channel, the sweeps on the oscilloscope will all be in the middle of the screen.**
	b. Depress CONT.
6	The oscilloscope should show a trace for every channel that the operator selected.
	a. Can have from 1 to 16 traces, depending upon system configuration.
	b. The trace vertical position reflects the input voltage to that channel.

2.5.3 Point-Plot Display Control (VC8-E) Acceptance Test

Perform the following steps to set-up the VC8-E, M869, and M885 modules for the acceptance test:

Step	Procedure
1	Set switches on M869 module as follows:
	a. If VR14 is installed, set Z switch to – and delay switch to L.
	b. If Tektronix 602 is installed, set Z switch to + and delay switch to S.
	c. If RM503 is installed, set Z switch to + and delay switch to L.
	d. On M885 module, ensure that the W1 jumper is removed and the AB jumper next to W1 is installed if RM503 is used.
2	Reinstall the M869 module into the OMNIBUS.
3	Connect HQ power cable to M869 module unless it is connected to the A231 module on the OMNIBUS.
4	Turn system power on.
5	Measure the HQ power supply with a precision meter for ±15 Vdc (see Table 2-22).
6	Reinstall the M885 module into the OMNIBUS.
7	Connect oscilloscope cable if an oscilloscope is installed in the system.

2.5.3.1 Control Logic Acceptance Test

Step	Procedure
1	Load MAINDEC-8E-D6CA-PB according to the diagnostic document.
2	Set switch register to 0200.
3	Depress ADDR LOAD.
4	Clear switch register.
5	Depress CLEAR, then CONT.
6	After the printout is complete, set bit 11, then bit 07, on the switch register.
	a. Teletype will print CONTROL LOGIC TEST.

(continued on next page)

Step	Procedure
	NOTE **The system is now running the Control Logic Test.**
	b. After each pass, the program prints CONTROL LOGIC TEST. One pass takes approximately 1 min, 50 sec.
7	Run the Control Logic Test and pass if test runs for 5 min without an error printout.

2.5.3.2 VC8-E Ramp Slewing Test

NOTE
This test is performed only if the system configuration does not include a display oscilloscope option.

Step	Procedure
1	The diagnostic should still be running (see Paragraph 2.5.2.1); if not, restart the program.
2	Set bit 10 to 1, and bit 11 to a 0 on the switch register.
3	Set bit 07 to a 0, then back to 1.
4	Teletype will print out RAMP TEST.
5	Connect an oscilloscope probe from the 453 oscilloscope to the point marked X on the M885 module.
6	The oscilloscope should display a positive-going ramp starting at the −5V level and rising to the +5V level, then deflecting full scale and starting again. See Figure 2-9.
7	To check the Y output, repeat steps 2 through 6 with bit 01 set to 1.

NOTE
The ramp should be a straight unbroken line. Any breaks or steps in the ramp indicate the D/A module is not calibrated properly. If display is not correct, refer to Paragraph 5.4 for calibration procedure.

8	Monitor the ramp for 1 min.

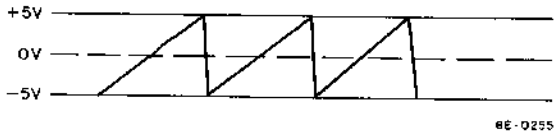


Figure 2-9 Oscilloscope Display for Ramp Test

2.5.3.3 VC8-E Display Test

CAUTION
Perform this test only if the system configuration contains a display oscilloscope.

A. **Crossing Diagonals Display**

Step	Procedure
1	Clear the switch register and then set bits 09 and 11 to 1.
2	Set bit 07 to 1 and monitor printout for CROSSING DIAGONALS.
3	On the display oscilloscope, monitor the crossing diagonals. The diagonal lines do not extend fully from corner to corner.
4	Ensure that the pattern is in the center of the oscilloscope. If it is not, perform calibration according to the procedure for display used with the system.

NOTE

Display sizes refer to approximate size of the display on a VR14 oscilloscope; size may vary on other oscilloscopes.

B. **Horizontal Flyback Display Test**

Step	Procedure
1	Ensure diagnostic is still running.
2	Clear the switch register and then set bits 9 and 10 to 1.
3	Set bit 07 to 1 and monitor printout for HORIZONTAL FLYBACK.
4	On the display oscilloscope, monitor the display for four horizontal bars, one in each corner of the display. Each bar is 1-1/2 in. long and should start in the corners.

NOTE

If display is not correct, perform appropriate oscilloscope calibration procedure.

C. **Vertical Flyback Display Test**

Step	Procedure
1	Ensure diagnostic is still running.
2	Clear the switch register, then set bits 09, 10, and 11 to 1.
3	Set bit 07 to 1 and monitor the printout for VERTICAL FLYBACK.
4	On the display oscilloscope, monitor the display for four vertical bars, one in each corner. Each bar is about 2 in. long and should start in the corners.

NOTE

If display is not correct, perform the appropriate calibration for oscilloscope used in the system.

D. **Corners Display Test**

Step	Procedure
1	Ensure diagnostic is still running.
2	Clear the switch register, then set bit 08 to 1.

(continued on next page)

Step	Procedure
3	Set bit 07 to 1 and monitor the printout for CORNERS TEST.
4	On the display oscilloscope, the display will have four diagonal arrows pointing to the four corners. The head of the arrow starts at the corner and the shaft runs diagonally toward the center. Each arrow is about 1-1/2 in. long. Ensure each corner has an arrow in it.

NOTE

If display is not correct, calibrate the oscilloscope with the calibration procedure for oscilloscope installed in the system.

E. **Diagonal Line Display Test**

Step	Procedure
1	Ensure diagnostic is still running.
2	Clear the switch register, then set bits 08 and 11 to 1.
3	Set bit 07 to 1 and monitor printout for DIAGONALS.
4	Monitor the oscilloscope display for a diagonal line running from the lower left corner to the upper right corner.
5	Ensure the line is straight without lines in it. If the line is not straight, calibrate the oscilloscope using appropriate procedure (see Paragraph 5.4).

F. ~~**Diagonal Line Display Test**~~ Vertical Bar Test

Step	Procedure
1	Ensure diagnostic is still running.
2	Clear the switch register, then set bits 08 and 10 to 1.
3	Set bit 07 to 1 and monitor printout for VERTICAL BAR TEST.
4	Monitor the oscilloscope display for a vertical line running from top to bottom and sweeping left to right across the oscilloscope.
5	Ensure the line does not have spaces or bright spots in it. If there are spaces or bright spots, the Point-Plot Display Control D/A module needs calibration.

NOTE

The line may be held at any position on the screen by setting switch register position 5 = 1 when performing Vertical or Horizontal Bar Display Test. The line must be completely scanned before test can be changed.

G. **Horizontal Bar Display Test**

Step	Procedure
1	Ensure diagnostic is still running.
2	Clear the switch register, then set bits 08, 10, and 11 to 1.

(continued on next page)

Step	Procedure
3	Monitor Printout for SELECT TEST.
4	Set bit 07 to 1 and monitor printout for HORIZONTAL BAR TEST.
5	Monitor the display oscilloscope for a horizontal bar from left side to right side, sweeping from the bottom to the top of the oscilloscope.
6	Ensure the horizontal line does not have spaces or bright spots in it. If it does, the Point-Plot Display Control D/A converter module needs calibration.

NOTE

If the system contains two VC8-E options, the second VC8-E should be set for IOT 615X. When running the acceptance test for the second VC8-E, bit 06 is set to 1 to tell the program that the second VC8-E is being tested.

2.5.4 Real-Time Clock (DK8-EP and DK8-ES) Acceptance Test

The following tests will check the Real-Time Clock and the clock panel.

2.5.4.1 Acceptance Tests

A. **DK8-EP and DK8-ES Register Test**

Step	Procedure
1	Load MAINDEC-8E-D8AB-PB. Follow directions on diagnostic document.
2	Load 0200 into the switch register.
3	Depress ADDR LOAD, then clear the switch register. Set SW0 to 1.
4	Depress CLEAR, then CONT.
5	Monitor printout for DK8E CLOCKS DIAGNOSTIC.
6	After each pass the program will printout DK8E PASS COMPLETE.
7	Allow the test to run for five passes. Each pass takes approximately 3.5 min.
8	Pass if five passes are completed without an error printout.

NOTE

If the clock option is a DK8-ES, proceed to Paragraph 2.5.4.2.

B. **External Pulse Test**

Step	Procedure
1	Load 0200 into the switch register and depress ADDR LOAD.
2	Set switch register to 0200 and depress CLEAR, then CONT.
3	Monitor printout for DK8E CLOCKS DIAGNOSTIC.

(continued on next page)

Step	Procedure
4	With the oscilloscope, observe a 40-μs pulse rate at pins FJ2, FJ1, HM1, and HM2 on the edge connectors which connect the M860 and the M518 modules.

NOTE

Set TIME/DIV to 10 μs to observe this signal. Oscilloscope synchronization may be difficult; the waveform is aperiodic.

2.5.4.2 DK8-ES Acceptance Test

A. **External Pulse Test**

Step	Procedure
1	Load 0200 into the switch register, then depress the ADDR LOAD key.
2	Set switch register to 0020, depress CLEAR, then CONT.
3	Monitor printout for DK8E CLOCKS DIAGNOSTIC.
4	With the oscilloscope, observe a 40-μs pulse rate at pins FJ2, FJ1, HM1, and HM2 on the edge connectors that connect the M860 and M518 modules.

NOTE

Set TIME/DIV to 10 μs to observe this signal. Oscilloscope synchronization may be difficult; the waveform is aperiodic. Period of pulse is approximately 40 μs.

5	Place the oscilloscope probe on the connector labeled OVERFLOW on the front panel. Observe a 40-μs pulse rate signal.

B. **External Clock Test**

Step	Procedure
1	Load 0020 into the switch register, then depress ADDR LOAD.
2	Set the switch register to 0014. Depress CLEAR, then CONT.
3	Monitor printout for DK8E CLOCKS DIAGNOSTIC.
4	On the DK8-EF front panel, ground the input CLOCK IN. The Teletype bell should ring when pass is complete.

WARNING

Never install or remove the 7008492 cable while power is on. Serious damage to the H724 power supply transformer may occur as plug is inserted or removed.

C. **DK8-EF Front Panel Check**

Step	Procedure
1	Plug the test cable No. 7008492 into the 28-Vac receptacle J5 on the processor. Plug the three phone jacks into the front panel inputs marked IN 1, IN 2, and IN 4. Place SLOPE 1, 2, and 3 switches to the + position.

(continued on next page)

Step	Procedure
2	Place an oscilloscope probe on OUT 1.
	a. Observe a 60-Hz square wave.
	b. Check OUT 2 and OUT 4 for the same square wave.
3	Place a probe on OUT 1 and a second probe on OUT 2.
	a. Place SLOPE 2 to the − position.
	b. OUT 2 signal should be 180° out of phase with OUT 1.
4	Place the second probe from OUT 2 to OUT 4.
	a. Place SLOPE 4 to the − position.
	b. OUT 4 signal should be 180° out of phase with OUT 1.
	c. OUT 1 and OUT 4 should be in phase. Place the three SLOPE switches to the + position.
5	While monitoring OUT 1 on the scope, rotate the appropriate THRESHOLD potentiometer.
	a. There should be a noticeable movement of the waveform in both ends of the THRESHOLD potentiometer movement.
	b. Repeat for OUT 2 and OUT 4. Leave the THRESHOLD potentiometers at midtravel.

D. **Schmitt Trigger Input Logic Test**

Step	Procedure
1	Load 0200 into the switch register.
	a. Depress ADDR LOAD.
	b. Set switch register to 2000.
	c. Depress CLEAR, then CONT.
2	Monitor printout for DK8E CLOCKS DIAGNOSTIC.
3	After each pass, the program will printout DK8E PASS COMPLETE.
	NOTE **Random errors may be caused by noisy 60-Hz power. This can be verified by using a single generator set to 60 Hz as the input to the Schmitt triggers.**
4	Allow the program to make five passes. Each pass takes approximately 2 min.
5	Pass for five passes without an error printout.

2.5.5 Buffered Digital I/O (DR8-EA) Acceptance Tests

The following tests will check the DR8-EA Buffered Digital I/O.

2.5.5.1 Visual Inspection and Test Setup

Step	Procedure
1	Ensure the A flip-flop jumpers are installed on all 12 bits on the M863 module.
2	Ensure the W interrupt jumpers are installed on all 12 bits.
3	Ensure the selected device code is the same as the device code label on the module. H and L jumpers are used to select device code. See Paragraph 4.5 for more information.

2.5.5.2 DR8-EA Acceptance Test Without DR8-EB Panel

Step	Procedure
1	Connect test cable 7008418 (BC08S) between J1 and J2 on the M863 module.
2	Install M863 module in the OMNIBUS (see Figure 2-6 for correct location).
3	Load diagnostic MAINDEC-8E-D0QA-PB (refer to diagnostic document for loading information).
4	Load 0200 into the switch register.
5	Depress ADDR LOAD.
6	Clear the switch register, depress CLEAR, then depress CONT.
7	Monitor printout for SET SR, DEVICE CODE, and CONT.
8	After printout, set the switch register to 00X0. X is equal to 0—7 determined by the device code label on the module under test.
9	Monitor printout for SET SR, INTERRUPT JUMPERS, and CONT.
10	After printout, set the switch register to 7777 and depress CONT.
11	Monitor printout for SET SR, FLIP-FLOP JUMPERS, and CONT.
12	After printout, set the switch register to 7777 and depress CONT.
13	Monitor printout for SET SR, RUN, and CONT.
14	After printout, set the switch register to 0100 and depress CONT.
15	Allow the test to run for 5 min. After each pass (10 sec), the TTY bell will ring.
16	Pass if there are no error printouts for the 5-min run.

CHAPTER 3
OPERATING PROCEDURES

3.1 COMPUTER OPERATION

The LAB-8/E computer allows the operator to manually program the machine using the switch register located on the programmer's console. The processor can also be loaded automatically by means of the 33 ASR Teletype console which contains the paper-tape reader/punch combination, as well as the standard Teletype keyboard. This chapter defines the operations required to communicate with the processor in both the manual and program modes.

The user should be thoroughly acquainted with the contents of Chapters 4 and 5 of this manual, and the *PDP-8/E Maintenance Manual,* before operating the LAB-8/E System.

3.1.1 Controls and Indicators

Figure 3-1 shows the controls and indicators on the programmer's console that provide manual control and indicate the program conditions. The controls on the console provide the operator with the hardware to start, stop, examine, modify, or continue a program. The controls are switches and keys; the keys are momentary (spring-return) switches.

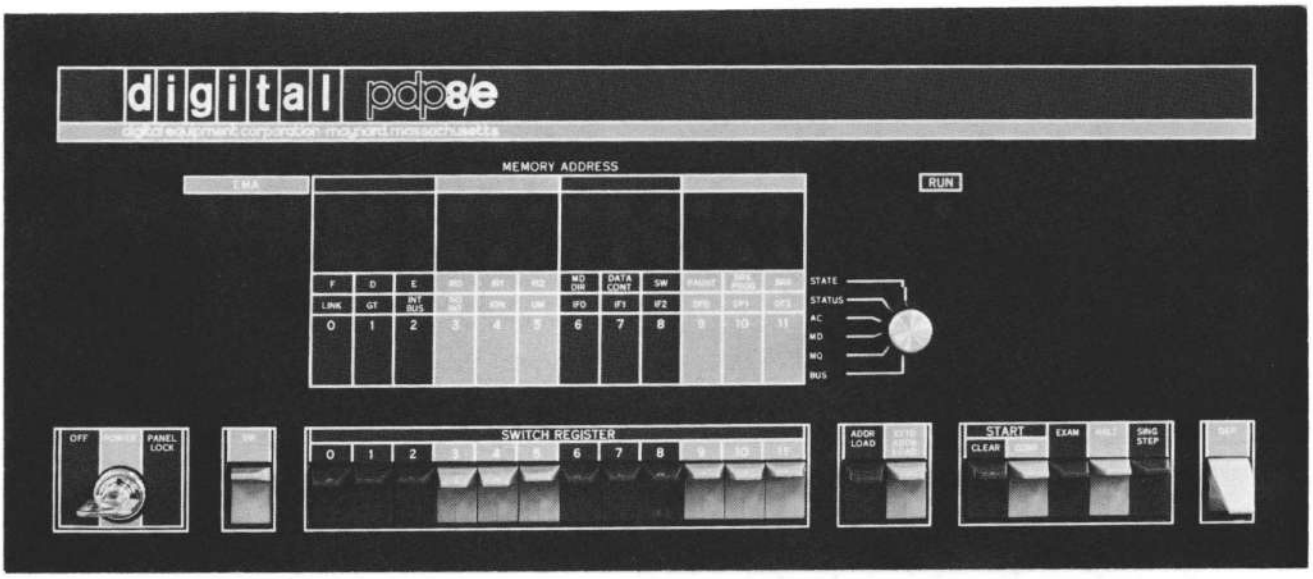


Figure 3-1 Programmer's Console

The indicators on the console provide a visual indication of the machine's status and current program, the contents of the major registers, and the condition of the control flip-flops. A lighted indicator denotes the presence of a binary 1 in a specific register bit position or control flip-flop.

Figure 3-2 shows the controls and indicators on the standard 33 ASR Teletype console. Table 3-1 describes the functions of the controls and indicators on both consoles.

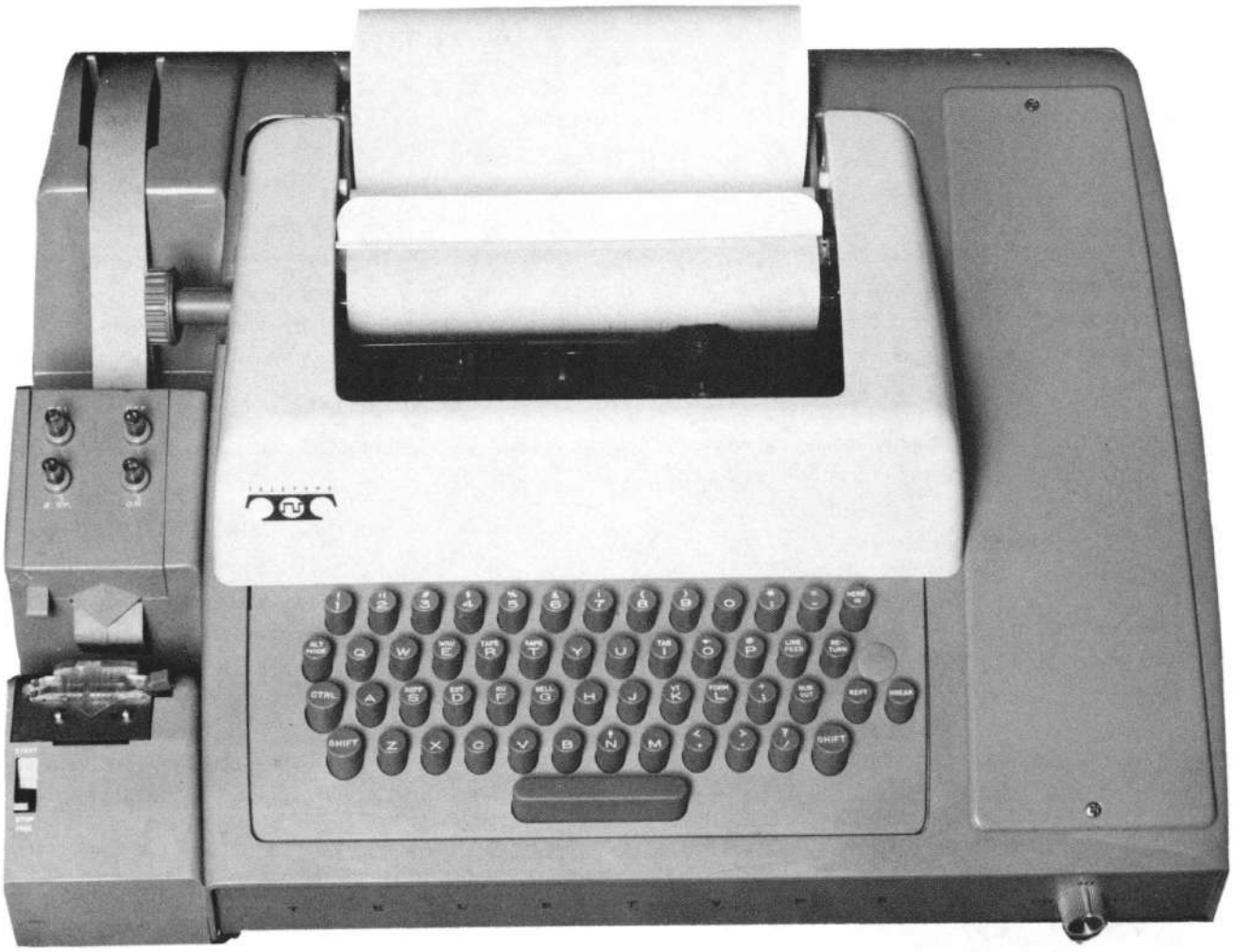


Figure 3-2 Teletype Model 33 ASR Console

Table 3-1

Programmer's Console Control and Indicator Functions

Control or Indicator	Function
OFF/POWER/PANEL LOCK	This is a key-operated switch. In the counter-clockwise, or OFF position, the switch disconnects all primary power to the machine. In the POWER, or straight up position, it enables all manual controls and applies primary computer power. In the PANEL LOCK, or clockwise position, it disables all keys and switches, with the exception of the switch register (SR). In this position, a running program is protected from inadvertent switch operation, and all panel indicators except the RUN light are turned off.

(continued on next page)

Table 3-1 (Cont)

Programmer's Console Control and Indicator Functions

Control or Indicator	Function
SW	When this switch is up, the line on the OMNIBUS line called SW is high; when the lever is down, the line is low. This switch is used by special peripheral controls, such as the Bootstrap Loader.
SWITCH REGISTER Switches	These 12 switches provide a means of communication between operator and machine. They allow a 12-bit word to be input. When the switch is up, it designates a binary 1 to the machine; switch down designates a 0. These switches are used during manual operations or under program control.
Load Address Key (ADDR LOAD)	This key loads the contents of the switch register into the CPMA and forces FETCH to be set (no major states while ADDR LOAD is depressed).
Extended Address Load Key (EXTD ADDR LOAD)	This switch loads the contents of SR6–11 into the Data Field and Instruction Field Registers of the Memory Extension Control. SR9–11 goes to Data Field 0–2. SR6–8 goes to Instruction Field 0–2.
Clear Key (CLEAR)	This key issues an INITIALIZE PULSE, clearing the AC, LINK, interrupt system, and I/O flags.
Continue Key (CONT)	This key resumes the computer program by issuing a MEM START and setting the RUN flip-flop. The word stored at the address currently held by the CPMA is taken as the first instruction.
Examine Key (EXAM)	Puts the contents of core memory at the address specified by the contents of the CPMA into the MB. The contents of the PC and CPMA are incremented by one to allow examination of the contents of sequential core memory addresses by repeated operation of the EXAM key.
Halt Switch (HALT)	This switch clears the RUN flip-flop and causes the machine to stop at TS1 of the next FETCH cycle. This switch is also used for single instruction stepping.
Single-Step Switch (SING STEP)	This switch clears the RUN flip-flop and causes the machine to stop at TS1 of the next cycle. Thereafter, repeated depressing of CONT steps the program one cycle at a time, so that the contents of registers can be observed in each state.
Deposit Key (DEP)	Loads the contents of the SR into the MB and core memory at the address given by the current contents of the CPMA. Then the contents of the PC and CPMA are incremented by one. This allows storing of information in sequential memory address by repeated operation of the deposit switch.
Indicator Selector Switch	This is a 6-position rotary switch, used to select a register for display. The six positions are as follows: *a.* STATE – Indicates an individual function for each bit: Bit 0 – FETCH 1 – DEFER 2 – EXECUTE 3 – IR0

(continued on next page)

Table 3-1 (Cont)

Programmer's Console Control and Indicator Functions

Control or Indicator	Function
Indicator Selector Switch (cont)	*a.* (cont) Bit 4 – IR1 5 – IR2 6 – MD DIR 7 – DATA CONTROL 8 – SW 9 – PAUSE 10 – BREAK IN PROG 11 – BREAK *b.* STATUS – Indicates an individual function for each bit: Bit 0 – LINK 1 – GREATER THAN flag 2 – INTERRUPT BUS 3 – NO INTERRUPT ALLOWED 4 – INTERRUPT ON 5 – USER MODE 6 – INSTRUCTION FIELD 0 7 – INSTRUCTION FIELD 1 8 – INSTRUCTION FIELD 2 9 – DATA FIELD 0 10 – DATA FIELD 1 11 – DATA FIELD 2 *c.* AC – Indicates bits 0–11 of the accumulator at TS1. *d.* MD – Indicates information just written or rewritten into memory. *e.* MQ – Indicates contents of MQ Register during TS1. *f.* BUS – Indicates bits 0–11 of the DATA Lines.
MEMORY ADDRESS	Indicates the contents of the memory address that will be accessed next.
EMA	Indicates which Extended Memory Field is being accessed.
RUN Light	Machine's timing is enabled and capable of executing instructions when lit.
REL Pushbutton	Disengages the tape in the punch to allow tape removal or tape loading.
B SP Pushbutton	Backspaces the tape in the punch by one space, allowing manual correction or rub out of the character just punched.
OFF/ON Pushbuttons	Controls use of the paper-tape punch with operation of the Teletype keyboard/printer.
START/STOP/FREE Switch	Controls use of the paper-tape reader with operation of the Teletype. In the FREE position, the reader is disengaged, permitting the paper tape to be manually moved within the reader without reloading or unloading it. In the STOP position, the reader mechanism is engaged but de-energized. In the START position, the reader

(continued on next page)

Table 3-1 (Cont)
Programmer's Console Control and Indicator Function

Control or Indicator	Function
START/STOP/FREE Switch (cont)	is engaged and operated under program control. The tape may be loaded or unloaded in either the FREE or STOP positions.
Keyboard	Provides a means of printing on paper when used as a typewriter, and of punching tape when the punch ON pushbutton is pressed; also provides a means of supplying input data to the computer when the LINE/OFF/LOCAL switch is in the LINE position.
LINE/OFF/LOCAL Switch	Controls application of primary power to the Teletype and data connection to the processor. In the LINE position, the Teletype is energized and connected as a computer I/O device. In the OFF position, the Teletype is de-energized. In the LOCAL position, the Teletype is energized for off-line operation, and signal connections to the processor are disconnected. Both LINE and LOCAL use of the Teletype require that the computer be energized through the POWER switch.

3.1.2 Keyboard Operation

The Teletype keyboard shown in Figure 3-3 is similar to a typewriter keyboard, except that some non-printing characters are included as upper case elements. For typing characters or symbols such as $, %, #, which appear on the upper portion of numeric keys and certain alphabetic keys, the SHIFT key is held depressed while the desired key is operated.

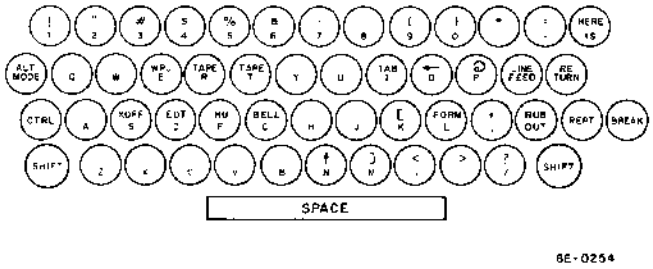


Figure 3-3 Teletype Keyboard

Designations for certain non-printing functions are shown on the upper part of some alphabetic keys. By holding the Control Key (CTRL) depressed and then depressing the desired key, these functions are activated. Table 3-2 lists several commonly-used keys that have special functions in the symbolic language of PDP-8/E systems.

Table 3-2
Special Keyboard Functions

Key	Function	Use
SPACE	Space	Used to combine and delimit symbols or numbers in a symbolic program.
RETURN	Carriage return	Used to terminate line of symbolic program.
HERE IS	Blank tape	Used for leader/trailer (effective only in LOCAL).
RUB OUT	Rub out	Used for deleting characters, punches all channels on paper tape.
CTRL/REPT/P	Code 200	Used for leader/trailer of binary program paper tapes (keys must be released in reverse order: P, REPT, CTRL).
LINE FEED	Line feed	Follows carriage return to advance printer one line.

3.1.3 Printer Operation

The printer provides a typed copy of input and output at 10 characters per second, maximum rate. When the Teletype unit is on-line (LINE), the copy is generated by the computer; when the Teletype unit is off-line (LOCAL), the copy is automatically generated whenever a key is struck.

3.1.4 Paper-Tape Reader Operation

The paper-tape reader is used to input into memory, data punched on 8-channel perforated paper tape at a maximum rate of 10 characters per second. The reader control positions are shown in Figure 3-2 and are described below.

START	Activates the reader; reader sprocket wheel is engaged and operative.
STOP	Deactivates the reader; reader sprocket wheel is engaged but not operative.
FREE	Deactivates the reader; reader sprocket wheel is disengaged.

3.1.5 Operating Procedures

The method used for loading and unloading LAB-8/E information is dependent upon the form of information, time limitations, and the peripheral equipment connected to the system. The following procedures are basic to any use of the systems, and although they may be used infrequently as the programming and use of the computer become more sophisticated, they are valuable in preparing the initial programs and in learning the function of machine I/O transfers.

3.1.6 Manual Data Storage and Modification

Programs and data can be manually stored or modified by means of the programmer's console. Manual data storage is primarily used to load the Read-In-Mode (RIM) Loader program into the computer core memory. The RIM Loader is a program used to automatically load programs into the computer from perforated tape in RIM format (see Paragraph 3.1.9). Use the following procedures to manually store data in the computer core memory.

3.1.6.1 Power For Manual Operation

Step	Procedure
1	Turn the OFF/POWER/PANEL LOCK switch clockwise to the POWER position.

3.1.6.2 Memory Addressing for Manual Operation

Step	Procedure
1	Set the SR switches to correspond to the address bits of the word to be stored.
2	Depress the ADDR LOAD key.
3	Observe that the address in the switch register is held in the computer as designated by lighted MEMORY ADDRESS indicators corresponding to switches in the 1 (up) position and unlighted indicators corresponding to switches in the 0 (down) position.

3.1.6.3 Manual Data Input to Addressed Memory Location

Step	Procedure
1	Set the SR switches to correspond to the data or instruction word to be stored at the address just set into the CPMA.

(continued on next page)

Step	Procedure
2	Rotate the Indicator Selector switch to MD.
3	Lift and release the DEP key.
4	Observe that the data in the switch register is the same as the data shown on the MD indicators. Data is now stored in the addressed location.
5	Check to see that the MA has been incremented by one so that additional data can be stored at sequential addresses by repeated switch register settling and DEP key operation.

3.1.6.4 Checking the Contents of Any Address In Core Memory

Step	Procedure
1	Perform the memory addressing procedure.
2	Depress the EXAM key.
3	Rotate the Indicator Selector switch to the MD position.
4	Observe the data shown on the MD indicators.
5	To observe the next location in core, the contents of the PC and the CPMA are automatically incremented by one. The operator depresses the EXAM key and observes the contents of the new location.

3.1.7 Loading Data Under Program Control

Information can be automatically stored or modified only by using programs previously stored in core memory. The RIM Loader stored in core memory allows RIM format tape to be loaded as described in the following paragraphs.

3.1.7.1 Initializing the System

Step	Procedure
1	Rotate the OFF/POWER/PANEL LOCK switch clockwise to the POWER position.
2	Set the Teletype LINE/OFF/LOCAL switch to the LINE position.
3	Load the tape in the Teletype reader by settling the START/STOP FREE switch to the FREE position, releasing the cover guard by means of the latch at the right, loading the tape so that the sprocket-wheel teeth engage the feed holes in the tape, closing the cover guard, moving the tape eight forward or backward until the punched leader section is over the read station, and setting the switch to the STOP position. Tape is loaded in the back of the reader so that it moves toward the front as it is read. Proper positioning of the tape in the reader results in three bit positions being sensed to the left of the sprocket wheel and five bit positions being sensed to the right of the sprocket wheel. The directional arrow printed on the tape should point toward the operator.
4	Load the starting address of the RIM Loader program (not the address of the program to be loaded) into the PC by means of the SR and the ADDR LOAD switches.
5	In sequence, press the CLEAR and CONT keys, and set the 3-position Teletype reader switch to the START position. The tape is then read automatically.
6	Stop the computer program by means of the HALT switch when the reader reaches the trailer section of tape.

3.1.8 Program Loading Operation

Automatic storing of the BIN program is performed by means of the RIM Loader program, as described below. With the BIN Loader stored in core memory, program tapes assembled in the program assembly language (PAL III) binary format can be sorted as described in the previous procedure, except that the starting address of the BIN Loader (usually 7777) is used in step 4. When the BIN program is loaded, the computer stops. At this point, the AC should contain all 0s if the program is stored properly. If the computer stops with a number other than 0 in the AC, a checksum error has been detected. When the program has been stored, it can be initiated by loading the program starting address (usually designated on the leader of the tape) into the PC by means of the SR and ADDR LOAD switches, then pressing and releasing the CLEAR key, and then pressing the CONT key.

The steps involved in loading programs and bringing the system to the point where the user can communicate with the processor is illustrated in Figure 3-4. The loading flow diagram for each type of program to be loaded is referenced, and each flow diagram is accompanied with a corresponding procedure.

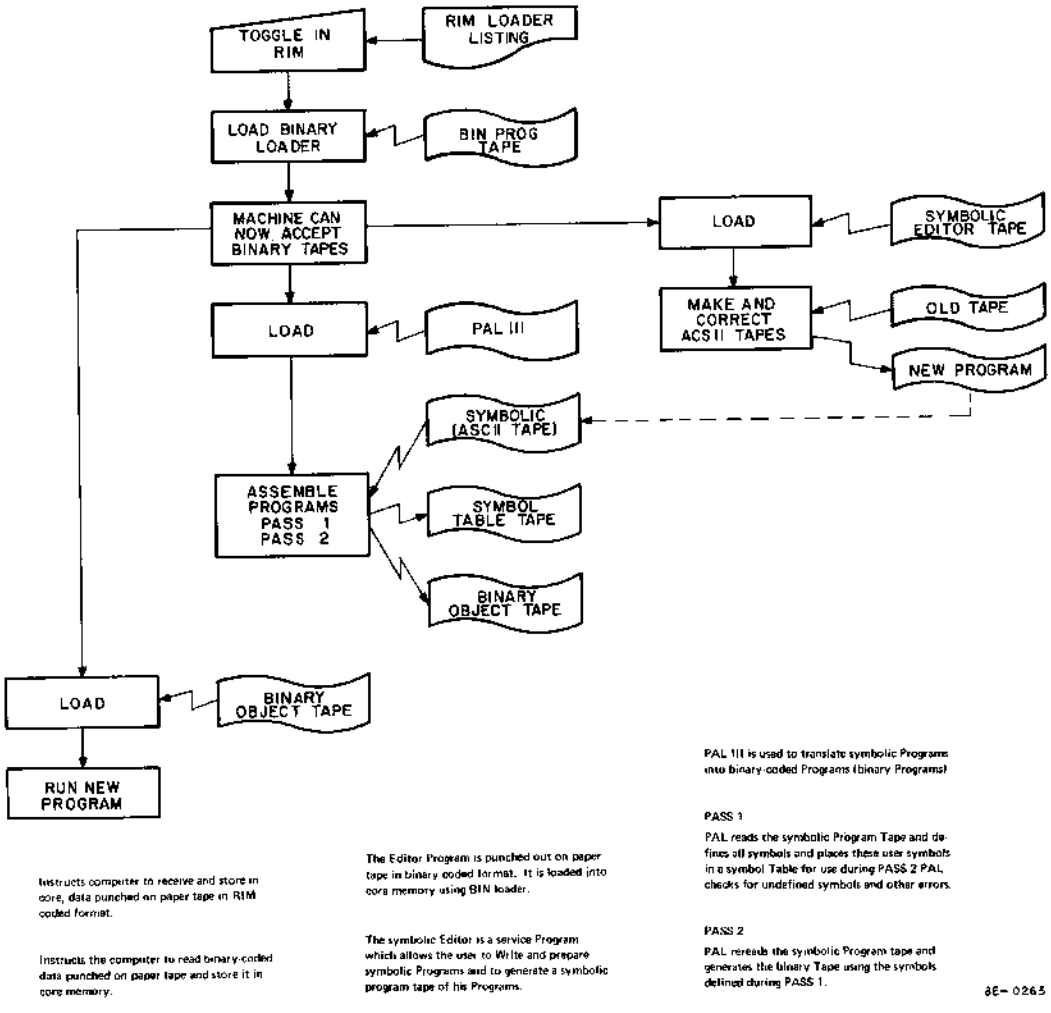


Figure 3-4 Loading Data Under Program Control

This loading procedure is greatly simplified when the user employs a mass storage device such as the Disk Monitor System. Using the monitor, stored programs are called in from disk files. This is illustrated in Figure 3-5.

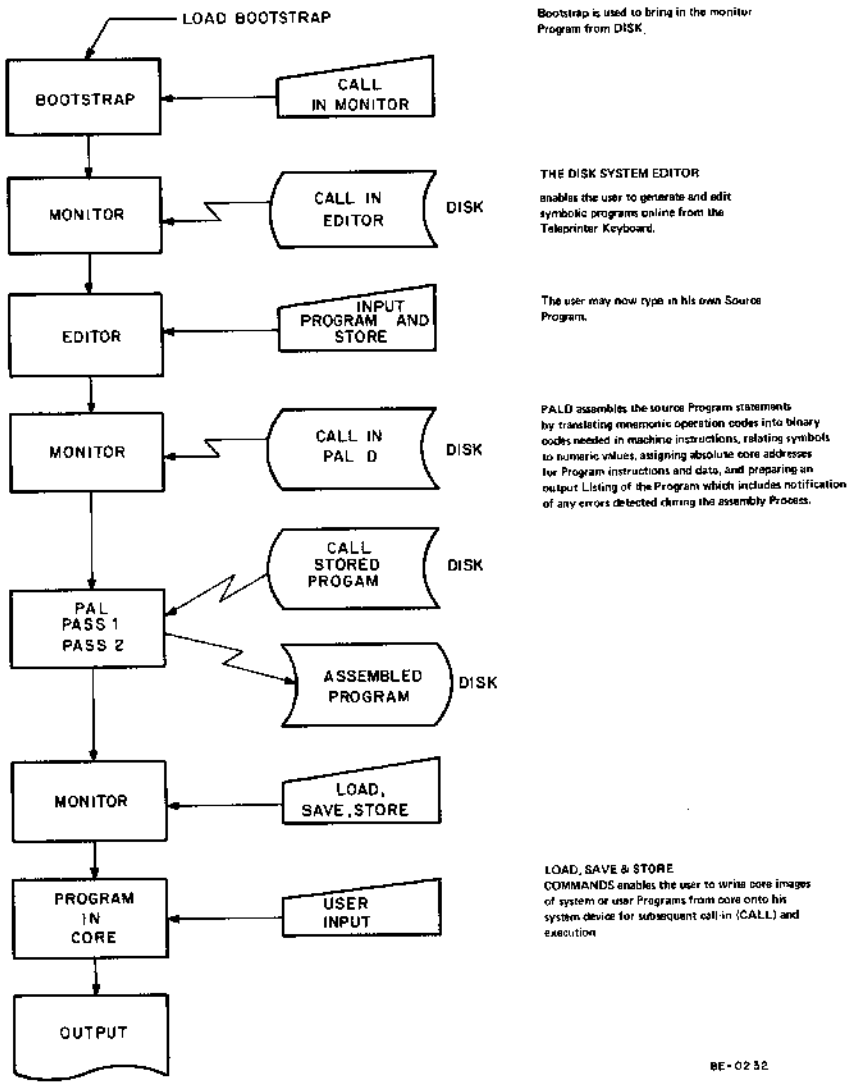


Figure 3-5 Loading Programs with Mass Storage Devices

3.1.9 Loaders

When a LAB-8/E System is first received, it should be assumed that no useful information is in memory. The system cannot perform any arithmetic operations or receive data.

Because all tapes in the Program Library are written in binary format, the user must load the system so that it can accept binary tapes. Initially 16 RIM instructions are manually toggled into memory. The BIN Loader tape is then used to eliminate the necessity of toggling in 86 additional instructions.

RIM allows the BIN Loader tape to be read into memory; and BIN, in turn, allows the use of any tape in the Program Library, such as a symbolic editor.

3.1.9.1 Read-In-Mode (RIM) Loader -- The RIM Loader, the first program loaded into the system, is loaded by the programmer using the console switches. The RIM Loader instructs the computer to receive and store in core, data punched on paper tape in RIM-coded format. The RIM Loader is used to load the BIN Loader described in Paragraph 3.1.9.2.

There are two RIM Loader programs: one is used when the input is to be from the low-speed paper-tape reader; the other is used when input is to be from the high-speed paper-tape reader. The locations and corresponding instructions for both loaders are listed in Table 3-3.

The procedure for loading (toggling) the RIM Loader into core is illustrated in Figure 3-6.

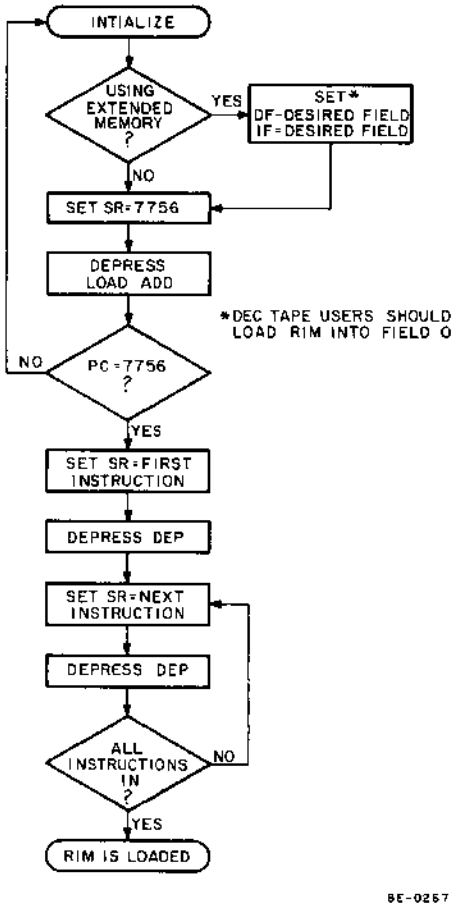


Figure 3-6 Loading the RIM Loader

After RIM has been loaded, it is good programming practice to verify that all instructions were stored properly. This can be done by performing the steps illustrated in Figure 3-7, which also shows how to correct an incorrectly-stored instruction. When loaded, the RIM Loader occupies absolute locations 7765 through 7776.

Table 3-3
RIM Loader Programs

Location	Instruction	
	Low-Speed Reader	High-Speed Reader
7756	6032	6014
7757	6031	6011
7760	5357	5357
7761	6036	6016
7762	7106	7106
7763	7006	7006
7764	7510	7510
7765	5357	5374
7766	7006	7006
7767	6031	6011
7770	5367	5367
7771	6034	6016
7772	7420	7420
7773	3776	3776
7774	3376	3376
7775	5356	5357
7776	0000	0000

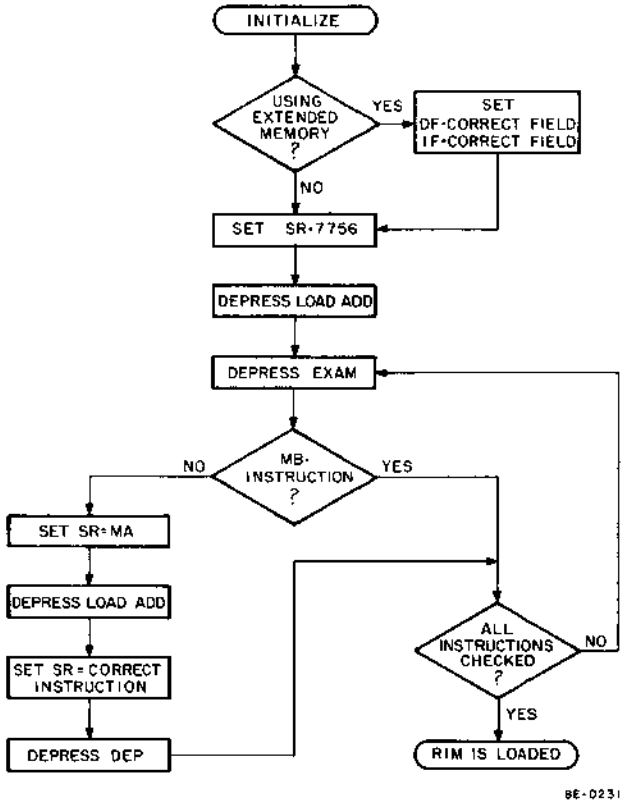


Figure 3-7 Checking the RIM Loader

3.1.9.2 Binary (BIN) Loader – The BIN Loader is a short utility program which, when in core, instructs the computer to read binary-coded data punched on paper tape and store it in core memory. BIN is used primarily to load the programs furnished in the software package (excluding the loaders and certain subroutines) and the programmer's binary tapes.

BIN is furnished to the programmer on punched paper tape in RIM-coded format. Therefore, RIM must be in core before BIN can be loaded. Figure 3-8 illustrates the steps necessary to properly load BIN. When loading, the input device (low- or high-speed reader) must correspond to the version of RIM loaded in the machine. When stored in core, BIN resides on the last page of core, occupying absolute locations 7625 through 7752 and 7777.

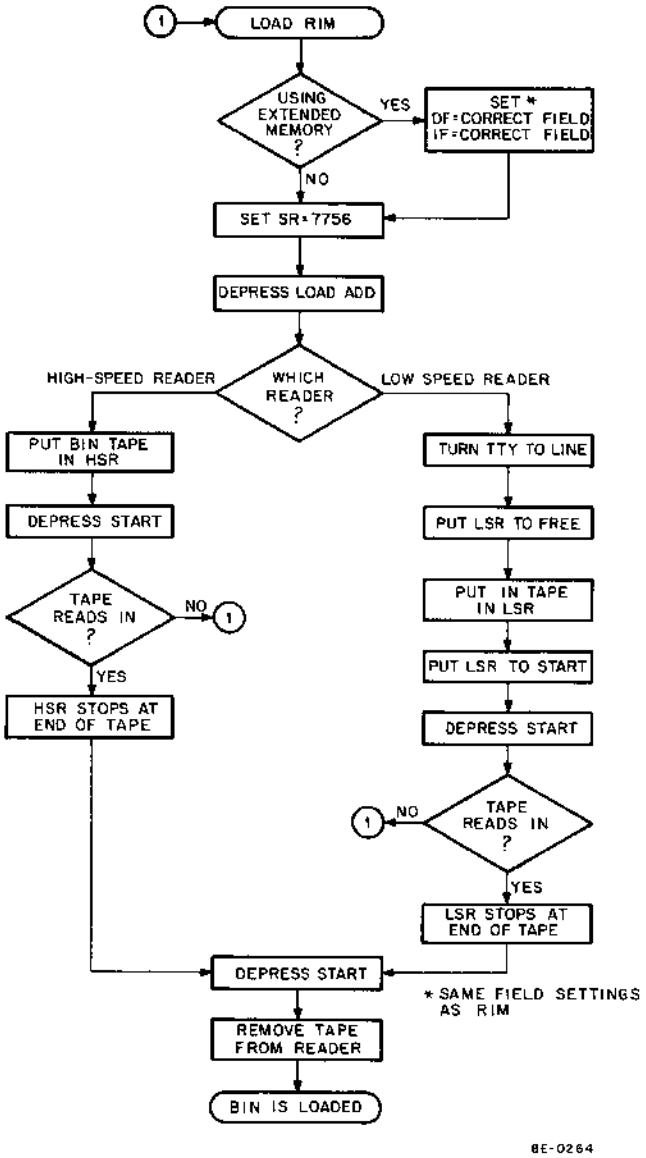


Figure 3-8 Loading the BIN Loader

BIN was purposely placed on the last page of core so that it would always be available for use in DEC's software package. The programmer must be aware that if he writes a program which uses the last page of core, BIN will be destroyed when that program runs. When this happens, the programmer must load RIM, and then BIN, before he can load another binary tape. Figure 3-9 illustrates the procedure for loading binary tapes into core.

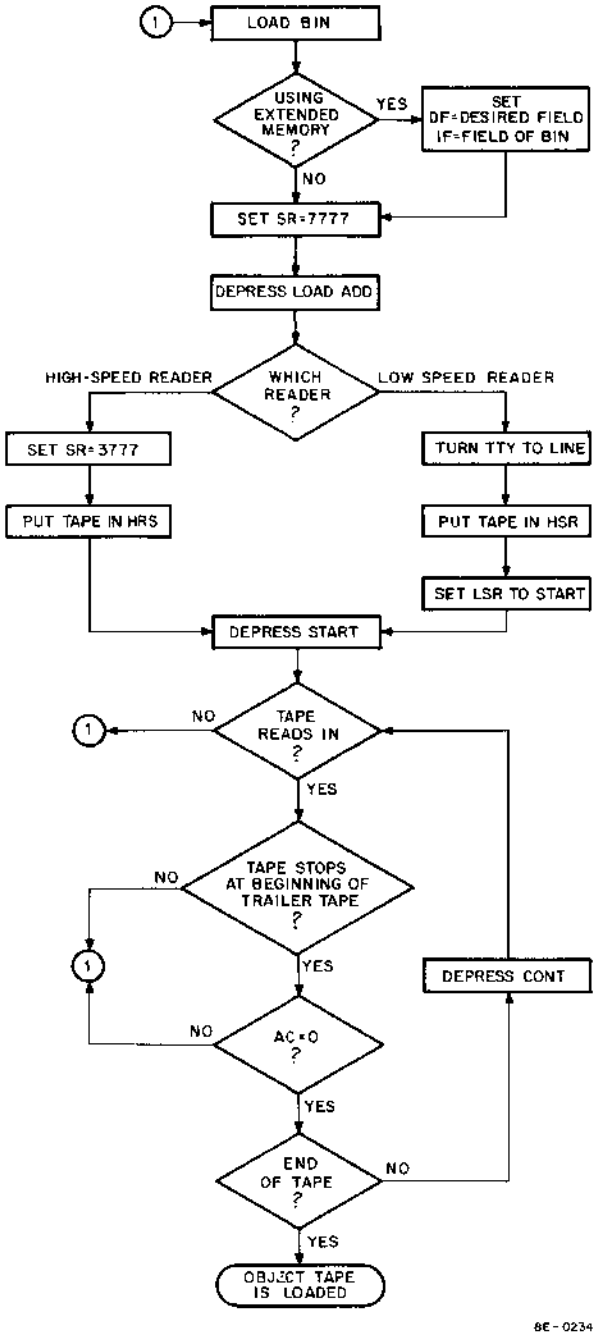


Figure 3-9 Loading a Binary Tape Using BIN

3.1.10 Off-Line Teletype Operation

The Teletype can be used separately from the computer for typing, punching tape, or duplicating tapes. The following procedures will enable the Teletype to be used in this manner:

Step	Procedure
1	Ensure that the computer OFF/POWER/PANEL LOCK switch is positioned to the PANEL LOCK position.
2	Set the Teletype LINE/OFF/LOCAL switch to the LOCAL position.

(continued on next page)

Step	Procedure
3	If the punch is to be used, load it by raising the cover, manually feeding the tape from the top of the roll into the guide at the back of the punch, advancing the tape through the punch by manually turning the friction wheel, and then closing the cover. Energize the punch by pressing the ON pushbutton, and produce about 2 ft of leader. The leader-trailer can be code 200 to 377. To produce the code 200 leader, simultaneously press and hold the CTRL and SHIFT keys with the left hand, press and hold the REPT key, and press the ## (P) key. When the required amount of leader has been punched, release the ## (P) key, and then all keys. To produce the 377 code, simultaneously press and hold the REPT and RUB OUT keys until a sufficient amount of leader has been punched.

3.2 DISPLAY SYSTEM OPERATING PROCEDURES

The following paragraphs deal with the operation and use of the LAB-8/E display options. The user must be familiar with the controls and adjustments to effectively use the displays. Guidelines for VC8-E interface with oscilloscopes are in Paragraph 3.2.2. Refer to the appropriate manual for more display information.

3.2.1 VR14 Display Operation

The VR14 is supplied either as a standard Retma 19 in. x 10-1/2 in. x 10-1/2 in. rack-mounted unit, or as a table-top model with its own decorator cover (see Figure 3-10). The VR14 can operate with a power line frequency of 47 to 63 Hz. The input line voltages are specified by the letter designation after VR14 (see Table 3-4). The VR14 can be made to operate with any of these voltages; refer to the VR14 user's handbook for instructions to change jumpers for different voltage inputs.

Table 3-4
VR14 Input Voltages

Designation Letters	Line Voltage
VR14C	115 Vac
VR14AD	230 Vac
VR14BE	100 Vac

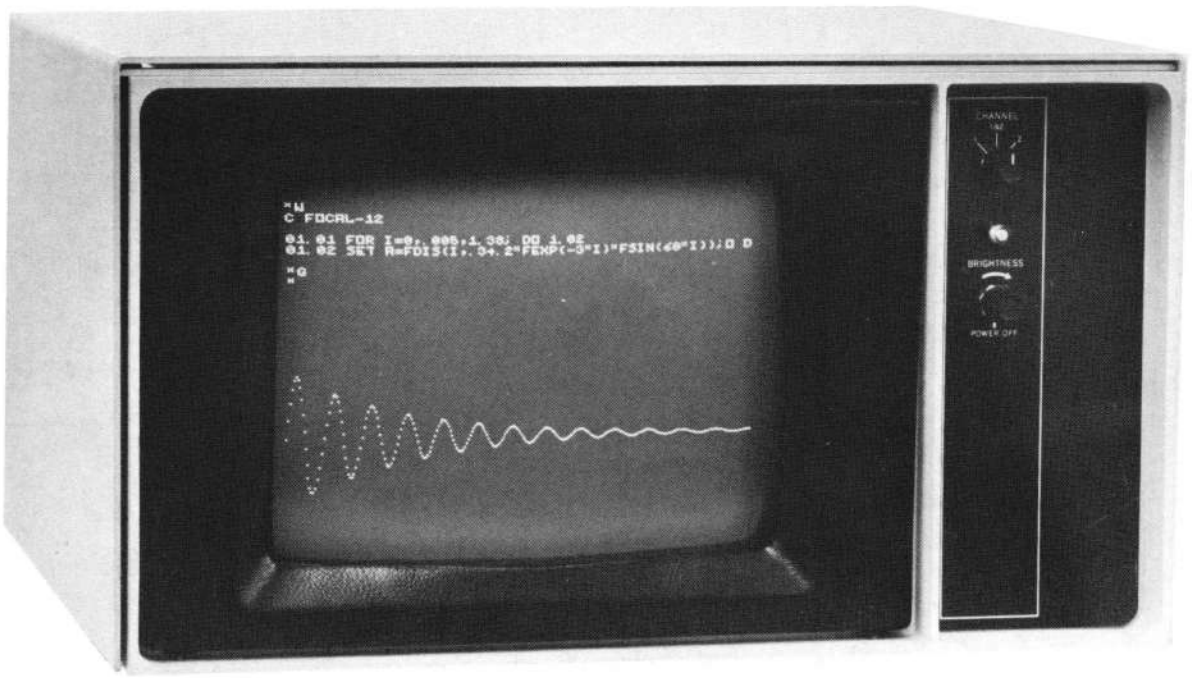


Figure 3-10 VR14 Display Oscilloscope

Equipment cooling is the most important VR14 installation requirement. There should be sufficient space below and behind the unit for fans to draw air from the bottom of the unit and for air to exit behind the unit.

The controls and connections necessary for operating the VR14 are shown in Tables 3-5 and 3-6. If the VR14 oscilloscope requires calibration or internal adjustment, refer to the VR14 manual for adjustment and calibration procedures.

Table 3-5
VR14 Controls

Controls	Location	Function
ON/OFF/BRIGHTNESS	Front Panel	Turns on input power and adjusts brightness of display when turned clockwise.
CHANNEL Select	Front Panel	Selects channel 1, channels 1 and 2, or channel 2. When in the 1 and 2 position, channel will be selected by instructions to control display.
X-slide switch	Rear Panel	Selects polarity of the X-channel input signal by switching BNC connectors.
Y-slide switch	Rear Panel	Selects polarity of the Y-channel input signal by switching BNC connectors.

Table 3-6
Unit Top Panel Control Settings*

Input Deflection	Position Setting	Rear Polarity Switch
±2V to 5V 0, 0 = center ±2V to 5V is up and to right	With no inputs, set position on X and Y to center (0V at A02-A (for X) A03-A (for Y))	Down (–)
0V to +2V to +5V 0, 0 = upper right screen	With no inputs, set –2.2V @ A02-A, A03-A with X- and Y-position potentiometers	Up (+)
0V to –2V to –5V 0, 0 = lower left	With no inputs, set +2.2 Vdc @ A02-A A03-A with X- and Y- position potentiometers	Up (+)

* Refer to VR14 manual.

NOTE

All signals are +BNC with respect to –BNC. Reversing input connections is the same as reversing the rear polarity switches. All single-ended signals applied to +BNC must have –BNC tied to signal-source ground. The negative signals are automatically grounded when the BC01K cable is inserted in rear panel connector.

3.2.2 Guidelines for VC8-E Interfacing for Oscilloscopes and XY Plotters

The VC8-E Display Controller was designed to accommodate the VR14, Tektronix 602, and the RM503 oscilloscopes. However, with certain modifications, the VC8-E can interface to many other oscilloscopes and plotters. The responsibility for interfacing with other oscilloscopes lies with the user. The following guidelines must be considered before attempting to control an oscilloscope that has not been specified by DEC.

3.2.2.1 Intensification Pulse – The VC8-E can supply a 1-μs pulse width; however, to avoid reflection on long cables, a 200-μs rise time (fall time if negative) is incorporated into the pulse width. Therefore, the width is defined from the start of the pulse to the completion.

Many oscilloscopes, other than the ones mentioned above, require longer pulse widths. As an example, some storage oscilloscopes require approximately a 5- to 6-μs pulse width. The VC8-E cannot accommodate such oscilloscopes unless the user changes the 1-μs pulse generator (on M869) to a larger value. This would require changing the capacitor to another value which is appropriate to the user's application. All oscilloscope manuals should define pulse width.

The VC8-E contains provisions to change the polarity of the output signal by a switch or by the M869 module. Improper value of the intensity polarity will result in signal blanking at the wrong times. (Retraces may be seen.)

The VC8-E can generate pulse voltages from +4V to −2V. With the removal and addition of certain jumpers on the M885 module, it can also generate a +4V to −10V voltage swing; however, note that the rise and fall times will be greater. In many cases, the intensity pulse input requirements to various oscilloscopes are 0V to 1V. An external adjustment on the oscilloscope or a special attenuating network must be used. This is the user's responsibility and must be considered before attempting to interface. As in the case of the Tektronix 602, DEC offers a VM03 kit which includes mounting hardware, and attenuating resistors and capacitors to be applied to the 602. The Tektronix 602 has provisions in its circuitry for the addition of external components; however, this may not be true of other oscilloscopes.

3.2.2.2 X and Y Outputs – The voltages generated by the X and Y outputs of the VC8-E are ±5V; this cannot be modified. The user must have external attenuators or an internal oscilloscope gain adjustment. Note that many oscilloscopes call for only positive voltage swings; however, an offset position can usually be adjusted to correct input polarity problems.

The VC8-E is an oscilloscope control and not a D/A converter. The settling time from maximum deflection is 4 μs. Many oscilloscopes have settling times faster than 4 μs. In this case, the user should use the internal delay set by the option at its minimum value (6 μs).

Oscilloscope settling times may vary from 1 μs to 50 μs. A DONE flag will occur when either oscilloscope has reached its settling time; i.e., 20 μs for the VR14, and 6 μs for the Tektronix 602. Note that all oscilloscopes differ somewhat in settling times. The user must determine if the VC8-E time delay is adequate for his oscilloscope. For slow oscilloscopes, software delays may be incorporated in the system or the user may change the 20-μs delay circuit by adding a larger capacitor.

3.2.2.3 Drive Capabilities – Cabling should be carefully selected. The X and Y outputs are capable of driving loads greater than 1K in parallel with 5000 pF of capacitance; e.g., 100 ft of cable at 50 pF/ft.

3.2.2.4 External Controls – The VR14 has a 2-channel input whereby the user can select a channel by setting a bit in the Status Register. This signal is usually not used by other oscilloscopes; however, the user may be able to use it as a pen-up, pen-down capability on an X/Y plotter. The output signal is 0 to +5V with a 10-mA source and a 30-mA sink current. This bit can also be used as a signal for partially controlling a storage oscilloscope.

3.2.2.5 Ground Loops – The analog signals present at the output of the VC8-E are the ANALOG VOLTAGE, the ANALOG GROUND, and the LOGIC GROUND (shield). When using differential inputs, the ANALOG VOLTAGE and ANALOG GROUND must be used.

When using single-ended inputs, use only ANALOG VOLTAGE and LOGIC GROUND. Do not connect the ANALOG GROUND to the SYSTEM GROUND.

3.2.2.6 VC8-E Restrictions

a. The VC8-E cannot fully control storage oscilloscopes; it can only plot points.

b. The VC8-E can use two different IOT device codes: 05 and 15.

c. Maximum of two VC8-E controllers in one system.

CHAPTER 4
PRINCIPLES OF OPERATION

This chapter presents the theory of operation of the LAB-8/E System and of the options that have been added to the PDP-8/E to form the LAB-8/E. The options are presented in three levels of discussion. First, a simplified block diagram presenting the primary parts of the option is discussed. Second, a block diagram relating instructions to time states is presented and discussed with appropriate references to the third level discussion. The third level discussion presents logic theory and is divided into functional groups of logic.

Chapter 4 is divided into seven sections: one section for system operation, and one section for each option.

Section 1 System Operation

Section 2 Analog-to-Digital Converter (AD8-EA)

Section 3 Analog Preamplifier and Multiplexer (AM8-EA)

Section 4 Point-Plot Display Control (VC8-E)

Section 5 Buffered Digital Input/Output (DR8-EA)

Section 6 Real-Time Clock (DK8-EP or DK8-ES)

Section 7 High Quality Power Supply

This sectional format is provided to aid the user in understanding the principles of operation and to distinguish the individual parts or circuits of each option.

NOTE

The component designations are for reference only and do not necessarily correspond to those designations on Engineering drawings.

SECTION 1
SYSTEM OPERATION

4.1 INTRODUCTION

The LAB-8/E System (see Figure 4-1) consists of the PDP-8/E processor and memory, a 33 ASR Teletype, and the following options which plug into the OMNIBUS or are mounted in the equipment rack or expansion box:

a. Analog-to-Digital Converter (AD8-EA)

b. Analog Preamplifier and Multiplexer Expander (AM8-EA)

c. Point-Plot Display Control (VC8-E)

d. VR14 or Tektronix 602 Displays (mounted in equipment rack, expansion box, or placed in the area of the LAB-8/E)

e. Buffered Digital I/O (DR8-EA)

f. Real-Time Programmable Clock (DK8-EP)

g. HQ Power Supply (mounted in expansion box or in back of equipment rack)

The LAB-8/E can be operated in many configurations using one or all of the options listed, depending on the users application. The system can be expanded at a later date to include all the options shown in Figure 4-1. To expand the system, the user need only insert modules and connect necessary cables and edge connectors (see Chapter 2 for installation and test procedures).

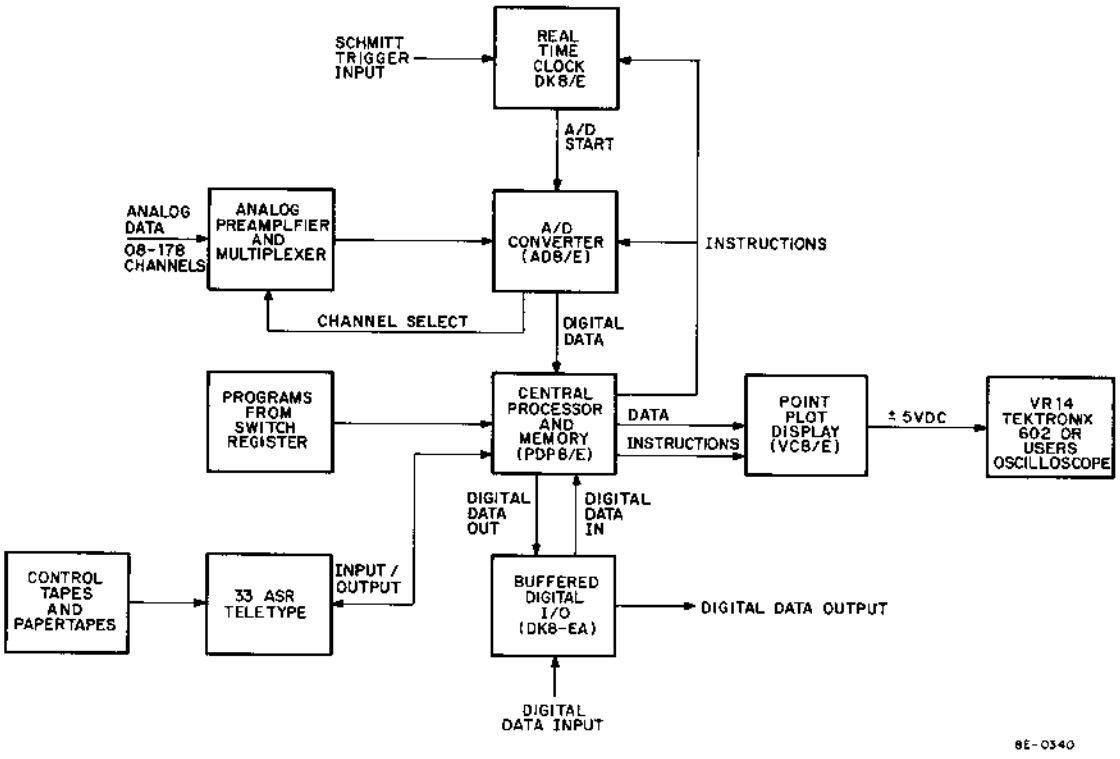


Figure 4-1 LAB-8/E Block Diagram

4.1.1 Analog Data Input to the A/D Converter

The A/D converter can be used in the LAB-8/E with one input to a side connector on the A841 module; or the system can be expanded using the AM8-EA Preamplifier and Multiplexer Expander option (see Figure 4-1). One AM8-EA will supply 8 channels of analog data; an additional module will expand the system to 16 channels. The AM8-EA receives ±1V inputs through a cable tied to a side connector on the A232 module, or from an analog panel and cable assembly. The AM8-EA supplies its ±5V output to the A/D converter through H851 Edge Connectors which connect the output of the AM8-EA to the A/D converter. The AM8-ED (simple analog panel) or AM8-EC analog panels can be used to supply inputs to the AM8-EA. The AM8-ED is a single-width front panel to mount on the H945 option cabinet. The AM8-ED has a DEC 25-pin (DB-25S) receptacle and a matching plug (DB-25P) to provide 16 analog inputs to the AM8-EA. The AM8-EC provides four potentiometer inputs for channels 0 through 3. Channels 4 through 17 octal are available on a 25-pin connector, as in the AM8-ED. Four phone jacks are provided to disconnect inputs from the potentiometers and to utilize channels 0 through 3 as analog channels. Note that there are several ways to supply inputs to the A/D converter and that the LAB-8/E can be expanded from a 1-channel system to provide for 16 channels of analog data by adding 2 AM8-EA modules.

4.1.2 A/D Converter (AD8-EA)

The AD8-EA (see Figure 4-1) is a 10-bit successive approximation A/D converter. The option is contained on the A841 and A231 quad modules which plug into the OMNIBUS. The A841 module contains analog circuitry, including A/D weighing switches and comparator, sample and hold, and an Analog Input Buffer. The A231 module contains all control logic for the A841 module; the modules are tied together by an H851 Edge Connector. The AD8-EA can have a single bipolar input or it can be multiplexed to provide 16 channels of data. The analog input is converted to 10 bits of digital data in 2's complement form to be transferred to the AC by programmed instructions. The digital data in the AC can be displayed, stored, or transferred to another system, as the user requires. Inputs to the A/D converter from the Real-Time Clock (see Figure 4-1) can be used to start an A/D conversion and, under program control, set up sampling rate and determine the number of samples to be taken. A detailed discussion of the A/D converter is contained in Paragraph 4.2.

Figure 4-2 is a flow chart of the programmed instructions used to monitor and control an A/D conversion. These instructions will also provide enabling signals for Interrupt and Skip logic, and for selecting alternate methods of starting the A/D converter. See Paragraph 4.2 for a detailed description of instructions used in the AD8-EA, the AM8-EA, or the DK8-EP. Note that the only interaction between modules is between the AD8-EA and the DK8-EP, or AM8-EA; all other options interact only through the central processor by programmed instructions.

4.1.3 Buffered Digital I/O (DR8-EA)

The DR8-EA Buffered Digital I/O provides 12 digital inputs to the LAB-8/E and 12 digital outputs to the outside world. The DR8-EA is contained on an M863 quad module installed in the OMNIBUS. The system can be expanded to include a maximum of eight modules. Inputs and outputs can be supplied directly to the M863 module through cables or a DR8-EB panel. The DR8-EB panel has two M904 modules to connect signals from the outside world to the panel. Two BC08J cables are used to connect to the M863 module when the panel is not used. A diagnostic jumper cable is provided to jumper input to output for troubleshooting and testing of the DR8-EA. See Paragraph 4.5 for a detailed discussion of the DR8-EA.

Figure 4-3 is a flow chart of the Buffered Digital I/O instructions. These instructions provide the means to clear and set the registers, and to transfer the contents of the I/O Register to the AC. INTERRUPT ENABLE is also provided to generate an Interrupt request when an input is applied to the digital I/O from the outside world to assert the IN flag.

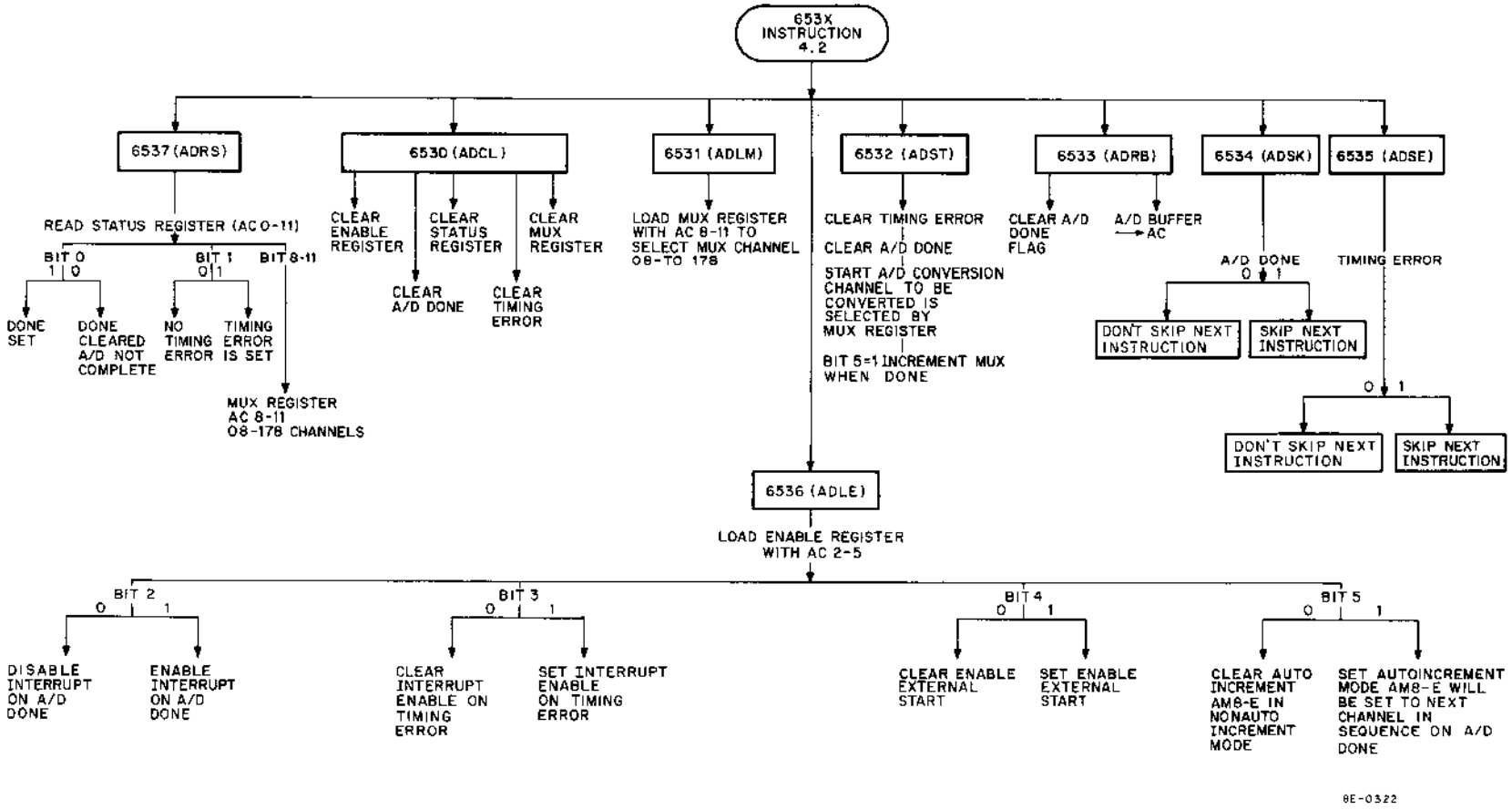


Figure 4-2 A/D Converter Flow Chart

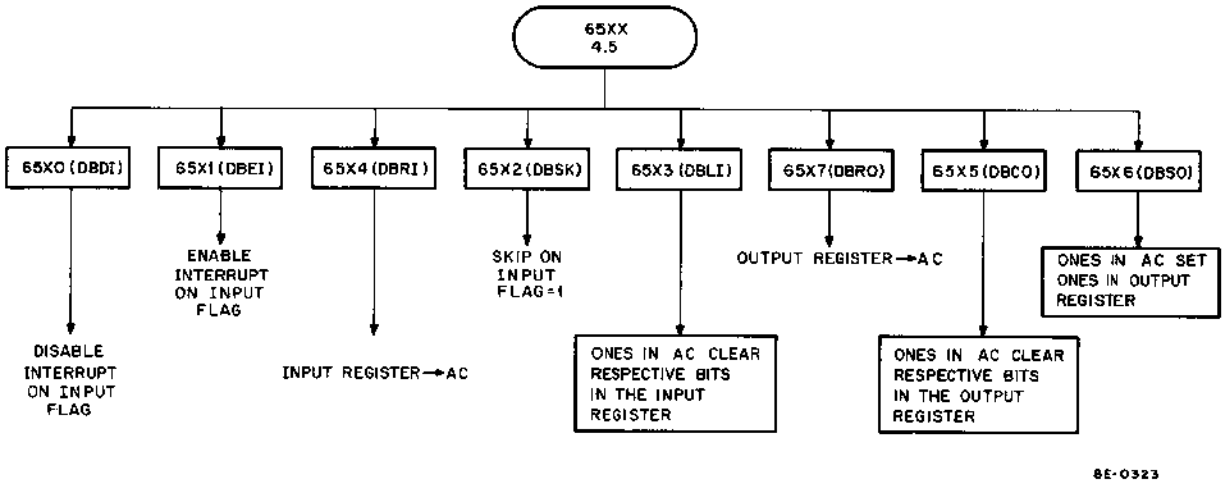


Figure 4-3 Buffered Digital I/O Flow Chart

4.1.4 Real-Time Programmable Clock (DK8-EP)

The Real-Time Programmable Clock consists of two quad modules that plug into the OMNIBUS and are interconnected by an H851 Edge Connector. The M860 module, Real-Time Clock Control, contains control logic. The M518 module contains input logic and Schmitt triggers. The DK8-EP provides a programmable time base that allows the user to record and/or control the occurrence of internal and external events. The Real-Time Clock can be used in the LAB-8/E to start an A/D conversion and, under program control, set up sample rates and control the number of samples taken. Note that the Schmitt triggers can also be used to control the A/D converter since they are threshold detectors that trigger when a signal reaches a certain level. The DK8-EF clock panel can be added to supply external clock inputs and to set up Schmitt trigger threshold levels. The DK8-EP panel provides three adjustable inputs to the Schmitt triggers and slope switches to change the direction of the triggering on the input signal. See Paragraph 4.6 for a detailed discussion of the clock.

Figure 4-4 is a flow chart showing the instructions used by the DK8-EP and their functions to control clock operation. The instructions will set up the mode of operation and generate signals to control external devices or options in the LAB-8/E (A/D converter). See Paragraph 4.6 for an explanation of the instructions.

4.1.5 Point-Plot Display Control (VC8-E)

The VC8-E Point-Plot Display Control converts 10 bits of digital data in 2's complement form ($\pm 0777_8$) to ±5 Vdc analog signals. The ±5 Vdc signal is applied to the deflection circuits of an oscilloscope; an intensity pulse generated by the VC8-E will intensify a point on the oscilloscope. A series of points can be plotted on the oscilloscope to produce a graphical display of X and Y coordinate data.

The VC8-E comprises the M869 control module and the M885 module with analog circuits and switches. These modules plug into the OMNIBUS and interface with each other by H851 Edge Connectors. The input to the VC8-E is from the AC in the central processor and the output is supplied by a 7008499 cable. A BC01K cable will be supplied if the VR14 is used; if the Tektronix 602 is ordered, a BC01L cable will be supplied. The RM503 user will require a 7008491 cable.

The VC8-E is controlled by programmed instructions from the central processor. Figure 4-5 is a flow chart of VC8-E instructions (see Paragraph 4.4 for a list of instructions). The instructions applied to the VC8-E will load the X and Y Holding Registers, Enable Registers, and will generate Skips or Interrupts to control the display of data.

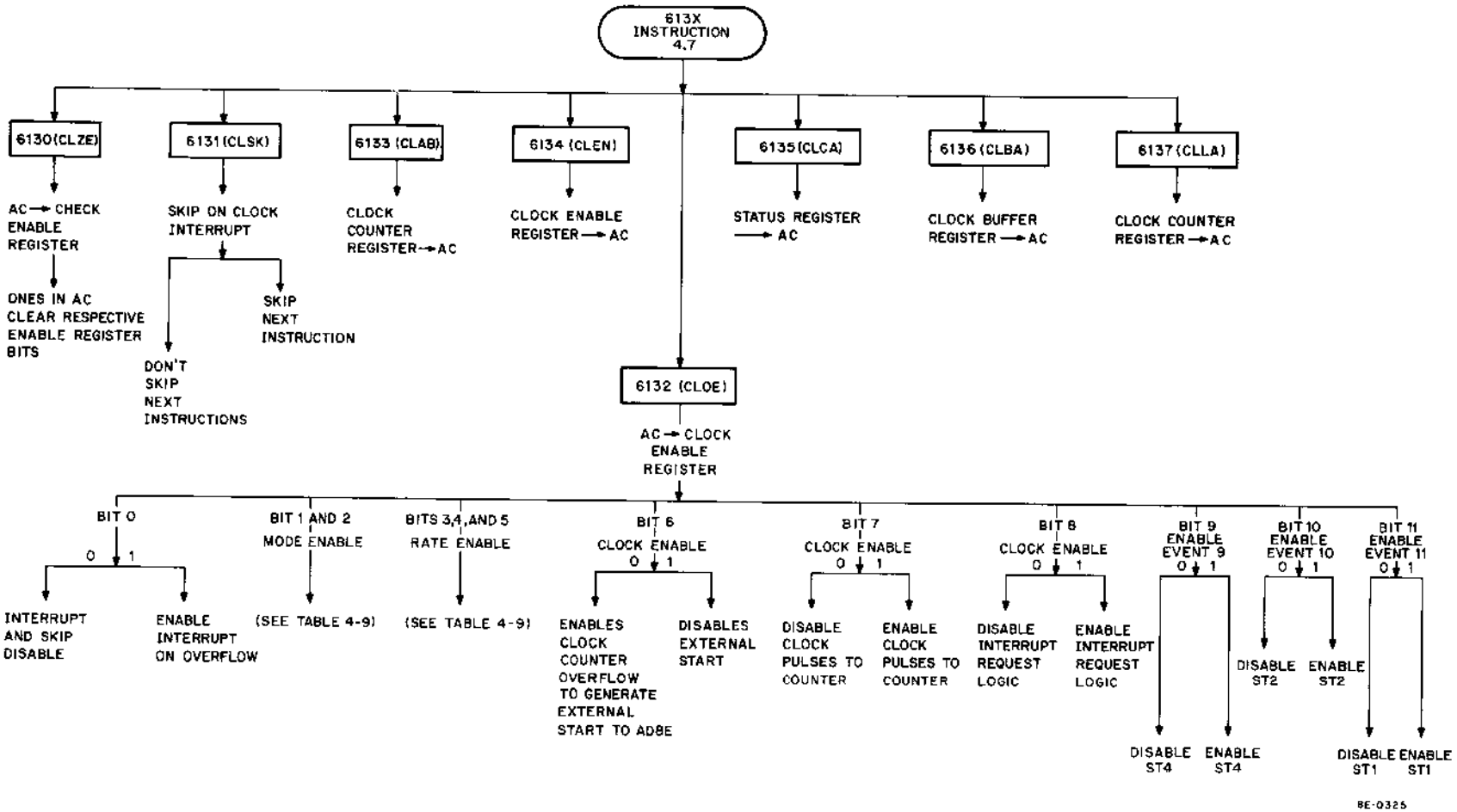


Figure 4-4 Real-Time Programmable Clock Flow Chart

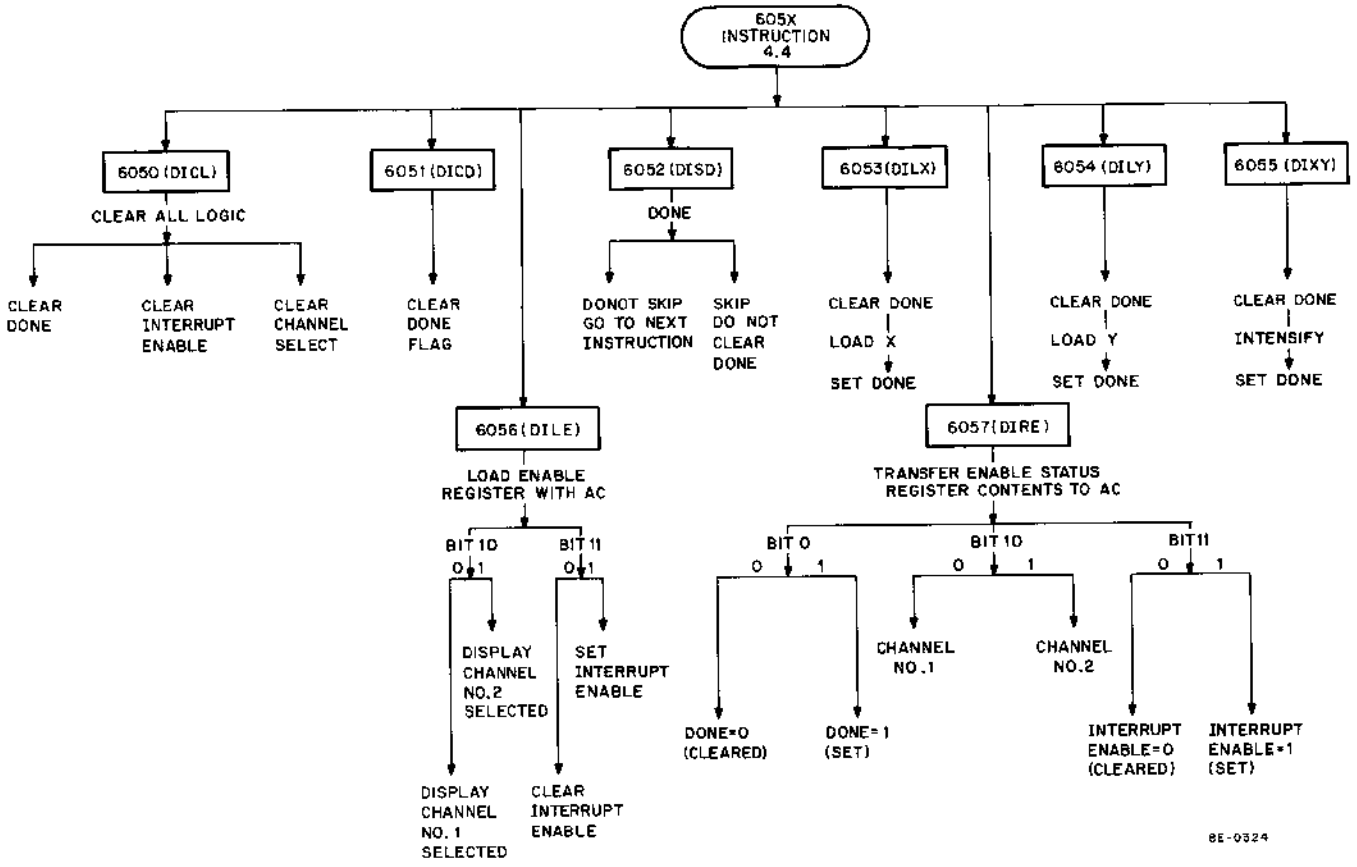


Figure 4-5 Point-Plot Display Control Flow Chart

4.1.6 33 ASR Teletype

The 33 ASR Teletype, used as an I/O device, enables the user to load programs into the LAB-8/E System from control and program tapes. Operation and maintenance information for the Teletype is presented in Volume 1 of the *PDP-8/E Maintenance Manual.*

In addition to using the 33 ASR Teletype as an I/O device, the user can also program the LAB-8/E using the switch register on the operator's console. There are several short programs in Paragraph 5.1.1 that may be used for troubleshooting and maintenance (see Chapter 3 for loading procedures).

4.1.7 HQ Power Supply

The ±15 Vdc HQ power supply provides high quality power to the LAB-8/E options. The output of the power supply is tied to the AD8-EA or VC8-E by a cable and is distributed to the other modules through H851 Edge Connectors.

SECTION 2
ANALOG-TO-DIGITAL CONVERTER (AD8-EA)

4.2 INTRODUCTION

Figure 4-6 shows a block diagram of the A/D converter. The I/O panel receives analog voltages which are fed to the analog preamplifier and multiplexer. Two AM8-EAs can be added to expand the system to 16 channels. A single bipolar input can be supplied to the A/D converter by an edge connector from the AM8-EA, or by a cable to a Berg connector on the A841 module. The AM8-EC and AM8-ED analog panels can be installed in the equipment rack to supply inputs to the AM8-EA or the A841 module (see Paragraph 2.2.1).

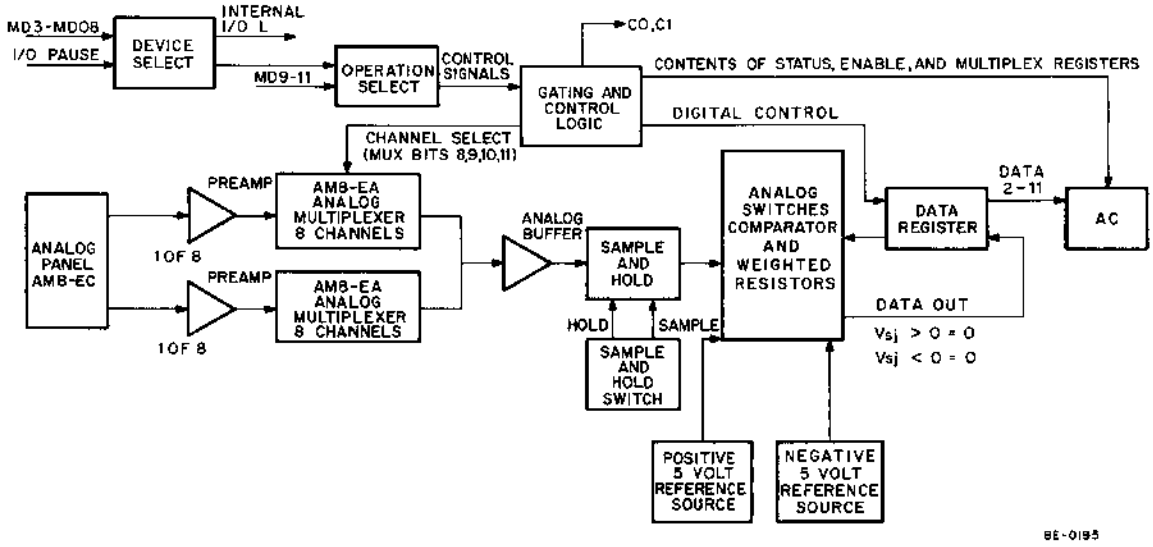


Figure 4-6 Analog-to-Digital Converter Block Diagram

The selected channel of the multiplexer, or the input to the side connector on the A841 module (if the multiplexer is not used), will be applied to the Analog Buffer and the sample and hold circuits in the A841 module. The sample and hold circuits will hold a dc level to allow sampling of fast-changing signals. The analog signal will be sampled during the Sample Mode. When a HOLD signal is generated by the control module, it will go into a Hold Mode and will apply the analog voltage to a summing junction for the A/D conversion process.

The comparator will monitor the voltage at the summing junction and send a signal to the control module, which will determine the final condition of the analog switches. The comparator will output a 1 when the voltage at the summing junction is less than 0V, and a 0 if the voltage is greater than 0V. The analog switches will be turned on to supply current to the summing junction. Each analog switch has a weighted resistor which will supply a current to the summing junction proportional to its position in the weighted-resistor network. The control logic will cause the right combination of switches to be turned on to null the voltage at the summing junction.

The A231 module, which controls the A/D conversion process, consists of the Enable/Status Register, Multiplexer (MUX) Register, Data Register, Clock and Switch Register, Device and Operation Select Decoder, and the Interrupt and Skip logic.

The Enable/Status Register is used to transfer the status of the A/D converter to the processor and to enable logic in the control module (see Figure 4-7). The Status Register provides the DONE flag and TIMING ERROR flag to the AC in bit 0 and 1 positions. The Enable Register consists of AC bits 2–5 and is used to enable Interrupts on TIMING ERROR or A/D DONE, enable EXT A/D START, or select the Auto-Increment Mode of selecting multiplexer channels.

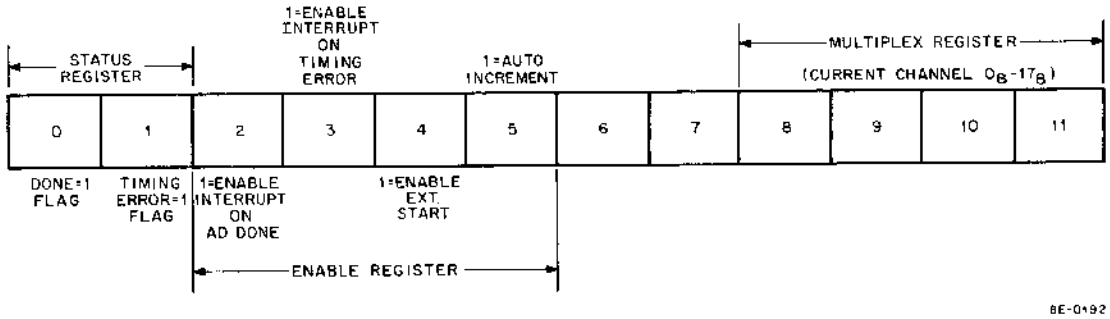


Figure 4-7 Enable/Status Register Contents

The MUX Register consists of AC bits 8–11 and is used to select the multiplexer channel from the AC; or if it is incremented in the Auto-Increment Mode, to select channels in sequence from 0_8 to 17_8. When the MUX Register reaches 17_8 in the Auto-Increment Mode, it will reset to 0_8 and start over. Loading the MUX Register from the AC after each A/D conversion will allow random sampling of multiplexer channels.

The Data Register will contain 10 bits of data after the A/D conversion is complete; this data will be transferred to the AC by programmed instructions. The Data Register will also select the analog switches to null the summing junction during the A/D conversion when it is strobed by the (internal) Clock and (Analog) Switch Register.

The Clock and Switch Register provides logic to strobe each bit position in the Data Register, starting with the most significant bit, and to generate a LAST SHIFT pulse when the last bit is strobed to complete the A/D conversion.

The Device Select logic will notify Operation Select logic that an A/D conversion is to take place. The Operation Select logic will decode the instructions from the processor and control the A/D conversion. The Operation Select logic will also gate information from the Enable/Status and MUX Registers to the AC.

The following instructions will be decoded by the control module and used to control the A/D conversion:

Clear All Logic (ADCL)

Octal Code: 6530

Operation: Clear A/D DONE and TIMING ERROR flags. Clear MUX and Enable/Status Registers.

Load MUX Register (ADLM)

Octal Code: 6531

Operation: Load MUX Register from AC bits 8–11, then clear AC.

Start Conversion (ADST)

Octal Code: 6532

Operation: Clear A/D DONE and TIMING ERROR flags, start A/D converter. Channel to be converted is determined by MUX Register.

Read A/D Buffer (ADRB)

Octal Code: 6533

Operation: Clear A/D DONE flag and transfer contents of A/D Buffer into AC bits 0—11.

Skip on A/D DONE (ADSK)

Octal Code: 6534

Operation: Skip next instruction if A/D DONE = 1. Do not clear DONE flag.

Skip on TIMING ERROR (ADSE)

Octal Code: 6535

Operation: Skip next instruction if TIMING ERROR flag = 1. Do not clear TIMING ERROR flag.

Load Enable Register (ADLE)

Octal Code: 6536

Operation: Load Enable Register from AC bits 2–5. Clear AC (see Table 4-1).

Read Status Register (ADRS)

Octal Code: 6537

Operation: Read A/D Status Register into AC bits 0—11 (see Table 4-1).

Table 4-1
Enable/Status Register

Bit Position	Signal Name	Function
0	DONE flag	DONE indicates A/D conversion is complete when DONE is set (DONE = 1).
1	TIMING ERROR flag	TIMING ERROR flag is set (1) when ADLM or ADRB is attempted while an A/D conversion is taking place.
2	ENABLE INTERRUPT on A/D DONE	When bit position 2 is a 1, ENABLE INTERRUPT will allow an Interrupt to be generated when DONE is set (1).
3	ENABLE INTERRUPT on TIMING ERROR	When bit position 3 is a 1, TIMING ERROR INTERRUPT ENABLE will allow an Interrupt to be generated when TIMING ERROR = 1. TIMING ERROR is set if an A/D conversion is attempted while an ADRB or ADLM is being executed.
4	ENABLE EXT START flag	When ENABLE EXT START is set (1), an A/D conversion can be started by an EXT CLOCK or EXT START signal.
5	AUTO INCREMENT	When AUTO INCREMENT is set, the multiplexer channels will be incremented after each A/D conversion and will select each channel in sequence 0_8 to 17_8.
6	Not used	
7	Not used	

(continued on next page)

Table 4-1 (Cont)
Enable/Status Register

Bit Position	Signal Name	Function
8–11	MUX Register	Bits 8–11 are used to load the MUX Register with channel to be sampled for an A/D conversion. They can be transferred to the AC to indicate current channel being sampled.

4.2.1 A/D Converter Block Diagram

Figure 4-8 shows the functional block diagram of the Analog-to-Digital Converter. The A/D converter will be broken down into the following functional areas for discussion purposes:

a. Device Select
b. Operation Select
c. Analog Buffer
d. Sample and Hold
e. Analog Switches and Comparator
f. Interrupt and Skip Logic
g. Enable Register
h. Status Register
i. A/D Buffer

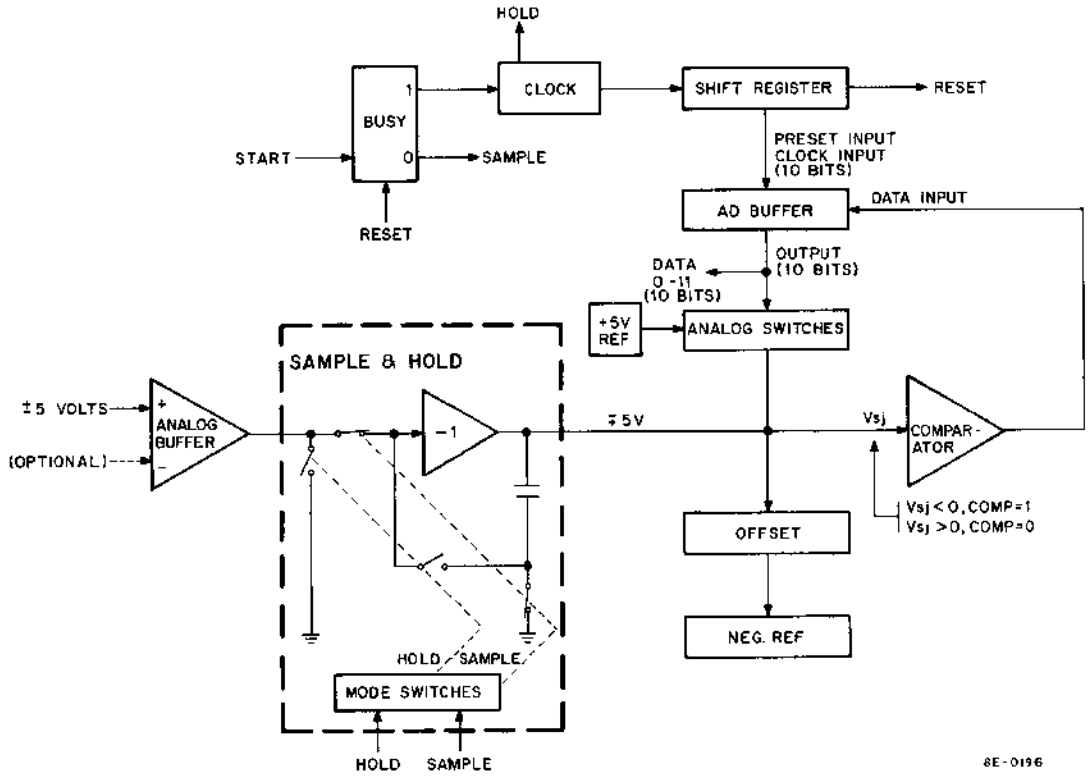


Figure 4-8 A/D Converter Functional Block Diagram

The analog preamplifier and multiplexer is not part of the A/D converter but is shown on the functional block diagram to illustrate how the A/D converter interfaces with an analog input.

The Analog Buffer on the A841 will receive ±5V analog data from the analog preamplifier and multiplexer or from the outside world. The channel in the multiplexer will be selected by bits 8—11 from the MUX Register in the A/D converter. In the Auto-Increment Mode, these bits will be incremented and applied to the multiplexer after each cycle of A/D conversion to select the next multiplexer channel; bits 8—11 of the AC will be used to select an analog channel in the Non-Auto-Increment Mode. If the AM8-EA is not used, one channel of analog input will be applied directly to the A841 module by a 7008533 cable to the side connector.

The output of the Analog Buffer will be applied to the sample and hold circuitry for an A/D conversion. For this discussion, we will leave the signal applied to the sample and hold circuits and deal with the operation of control logic to perform the A/D conversion.

Before an A/D conversion can be executed, the control logic must be initialized and instructions must be generated to set up the logic for an A/D conversion. The first step in this process will be the generation of an IOT instruction which will be decoded by the Device Select logic. The Device Select logic will have MD03—MD08 applied to its input and when a 653X instruction is generated, it will output an INTERNAL I/O L and a SELECT L (see Figure 4-6). The INTERNAL I/O L will cause the positive I/O bus to ignore all other IOTs. The SELECT L will gate bits MD9—MD11 to the Operation Select Decoder. The Operation Select Decoder will decode the instructions and apply them to the control logic (see Paragraph 4.2.2.1).

The control logic will be initialized when a 6530 instruction is performed. The 6530 instruction will clear A/D DONE and TIMING ERROR flags, the Enable Register, Status Register, and the MUX Register. After the logic is cleared, the Enable Register may be loaded with bits AC2—AC5 to set up the logic for an A/D conversion. The 6536 instruction is used to load the Enable Register, (see Figure 4-6). A 1 will set the flip-flop and select the condition indicated; i.e., a 1 in bit position 5 will select the Auto-Increment Mode of channel selection (see Paragraph 4.2.6).

The channel selected for the A/D conversion will be determined by the contents of the MUX Register. The MUX Register will be loaded and the channel selected by a 6531 instruction. If the Auto-Increment Mode in the Enable Register was selected (bit 5 = 1), the MUX Register will start at the channel loaded into the MUX Register and increment the MUX Register to select a new channel. If the MUX Register is not loaded with a 6531 instruction, and if the 6530 was performed, the first channel selected will be channel 0_8 if the ADCL instruction cleared the MUX Register. In the event neither instruction was performed, the MUX Register will start at whatever channel it contains.

Random selection of the channel to be converted can be accomplished by loading the MUX Register with a new channel after each A/D conversion. If the AM8-EA is not installed, the MUX Register will have no effect and the input to the A841 module will be applied to the Analog Buffer. (See Paragraph 4.2.5 for detailed MUX Register logic.)

The Status Register, a part of the control logic, contains the TIMING ERROR and A/D DONE flags. TIMING ERROR will set if a 6533 or 6531 instruction is attempted while an A/D conversion is in progress. A/D DONE will set when LAST SHIFT is generated by the Clock and Shift Register logic at the time the last bit position is strobed. A/D DONE may be used to enable a Skip after the A/D conversion is complete and data is ready for transfer to the AC. A 6535 instruction will check the TIMING ERROR flag and generate a Skip if the flag is set. The contents of the Status Register can be transferred to the AC by a 6537 instruction for status checks. (See Paragraph 4.2.2 for detailed logic.)

After the logic in the control module is initiated, a 6532 (A/D START) instruction may be performed to start the A/D conversion. The 6532 instruction will clear TIMING ERROR and A/D DONE, and set the BUSY flip-flop used to generate a HOLD command in the sample and hold circuits. Note that the A/D converter can be started by an EXT START or EXT CLOCK START if the EXT START ENABLE (bit 4 of Enable Register is 1) flip-flop was set by a 6536 instruction. An EXT START or EXT CLOCK START would set the BUSY flip-flop and start the A/D conversion if EXT START ENABLE is set. The EXT START and EXT CLOCK START signals originate in the Real-Time Clock when an overflow signal is generated or a Schmitt trigger fires (see Paragraph 4.6).

The signal on the input to the Analog Buffer will be applied to the sample and hold circuits shown inside the dotted lines in Figure 4-8. The sample and hold circuit has two modes of operation: Sample or Hold. In the Sample Mode of operation, the input to the amplifier will be applied to a capacitor on the output. The switches will, as shown in the diagram, apply a ground to the other side of the capacitor allowing the capacitor to charge to the input voltage. The other two switches will be as shown to allow the capacitor to charge. In the Hold Mode, the two switches that are shown closed will open and remove the input to the amplifier and the capacitor. The other two switches will close, ground the output of the Analog Buffer, and allow the voltage on the capacitor to be applied to the input of the amplifier. The amplifier will maintain the voltage on the capacitor at the summing junction during the Hold Mode for an A/D conversion. The mechanical switches shown are for explanation only. The switches in the sample and hold circuits are FET semiconductors. The mode of operation is determined by the BUSY flip-flop in the control logic. When BUSY is cleared, the Sample Mode is enabled; when BUSY sets, the Hold Mode is enabled.

The BUSY flip-flop will set when a 6532 instruction or an EXT CLOCK START pulse is present. The setting of the BUSY flip-flop will trigger a 2-μs delay network in the clock and assert the PRESET and HOLD signals. PRESET will set the switch register to the most-significant-bit position of the A/D Buffer and the HOLD signal will switch SAMPLE and HOLD to the Hold Mode. The clock pulse will be delayed an additional 100 ns to allow the sample and hold amplifier to settle before the A/D conversion starts. After the delay, the clock pulses will start the Shift Register counter which was preset to bit position 2. The Clock and Shift Register will strobe each bit position from MSB (2) to LSB (11). (See Paragraph 4.2.2 for detailed logic).

As the Shift Register strobes each bit position (see Figure 4-8), the comparator will be checking the summing junction and comparing it with 0. If the summing junction is below 0, the comparator will output a 1; if the comparator is above 0, a 0 output will be applied to the data input of the flip-flops in the A/D converter. This will determine the final state of each bit in the A/D Buffer. (See Paragraph 4.2.10 for detailed logic.)

The analog switches and weighted resistors will act as current sources for the voltage at the summing junction to supply the current necessary to reduce the voltage at the summing junction to 0V. Each switch and weighted resistor will supply current to the summing junction if the switch is turned on by the flip-flop in the A/D Buffer. Figure 4-9 shows one flip-flop in the A/D Buffer and an analog switch tied to the 0 side of the flip-flop. Initially, the flip-flop will be reset, producing a high output to I1. I1 will have a low output and will enable E2 to apply positive voltage to the base of Q1. Q1 will conduct and cut Q2 off. No current will be supplied to the summing junction by Q2 or to the weighted resistor tied to its emitter. When a clock pulse and Shift Register pulse are applied to E3, the gate will be enabled and will set the flip-flop to apply a 0 to I1. I1 will invert the low to a high and turn Q2 on to supply current to the summing junction. If the comparator output is 1 (summing junction $<$ 0), the flip-flop will set when SR02 is applied to the clock input and will turn the switch off. The Clock and Switch Register will strobe all the bit positions to turn on the right combination of switches to null the voltage at the summing junction. Each switch will supply current to the summing junction, the amount determined by its position in the network. After the last bit is checked, a LAST SHIFT will set the A/D DONE flip-flop. A/D DONE will generate a Skip if the 6534 instruction was performed, or an Interrupt if the A/D DONE INTERRUPT

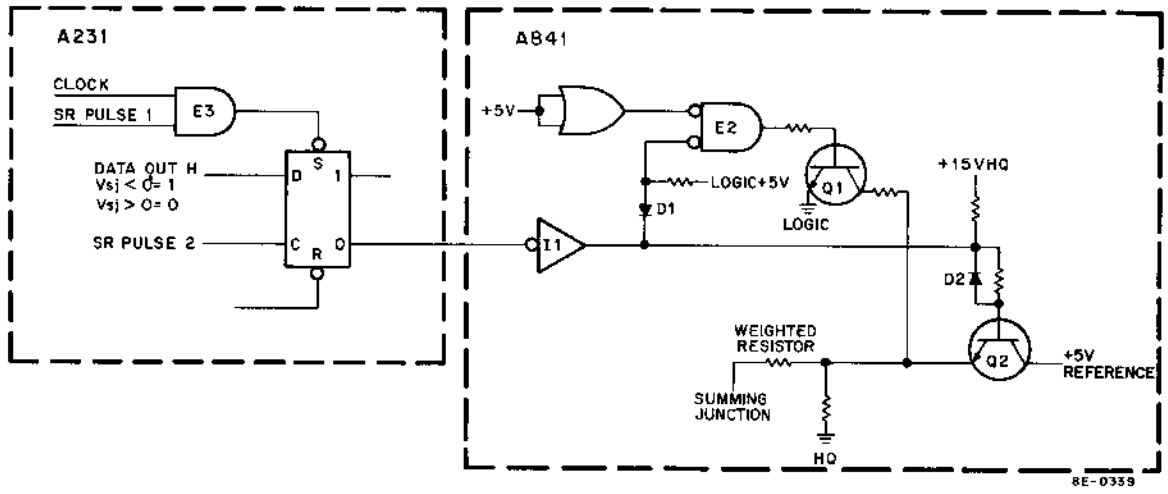


Figure 4-9 A/D Buffer and Switch Logic

ENABLE was set in the Status Register. The contents of the A/D converter may then be transferred to the AC by programmed instructions. (See Paragraph 4.2.2 for detailed logic.)

4.2.2 A/D Converter Detailed Logic

4.2.2.1 Device and Operation Select Logic – The Device Select logic (see Figure 4-10) will receive bits MD3 L–MD8 L and the I/O PAUSE L signal as inputs. I/O PAUSE will be generated 150 ns after the generation of TP1 in the FETCH cycle. The I/O PAUSE will be applied to AND gates in the Device Select logic to gate bits MD3 L–MD8 L. If these bits are 53 octal, an INTERNAL I/O L will be generated to indicate that the A/D converter will perform this operation.

The operation to be performed by the A/D converter will be determined by bits MD09 L and MD11 L. INTERNAL I/O L will be applied to the AND gates and will allow the bits to be applied to the 8251 IC, which is a BCD-to-Decimal Decoder. The IC will output a low on the appropriate line for the instruction that has been decoded. Truth tables, timing diagrams, and logic for the 8251 IC are shown in Appendix A of the *PDP-8/E Maintenance Manual*.

4.2.2.2 External A/D START and Time Pulse Logic – Figure 4-10 shows the EXT START and EXT CLOCK START logic. EXT CONV START out of E2 will be low if the EXT START ENABLE flip-flop in the Enable register is set and EXT START L is asserted. This signal is used to start an A/D conversion when the Real-Time Programmable Clock, or other peripheral, is used to determine when an A/D conversion is to be performed.

The TP3 AND ADLE signal will be used to allow loading of the Enable Register from bits 2–5 of the AC. The INIT or TP3 AND ADCL signal will generate a CLEAR L to clear all flip-flops in the control logic. INIT is generated to clear all logic when CLEAR is depressed on the control console, or when the power is turned on.

4.2.2.3 Interrupt, Skip, and Control Logic – The control logic (see Figure 4-11) will select the proper C lines and generate or receive a BUSY, TIMING ERROR, A/D DONE, Interrupt request, and Skip. It will also clear all the registers in the A/D converter.

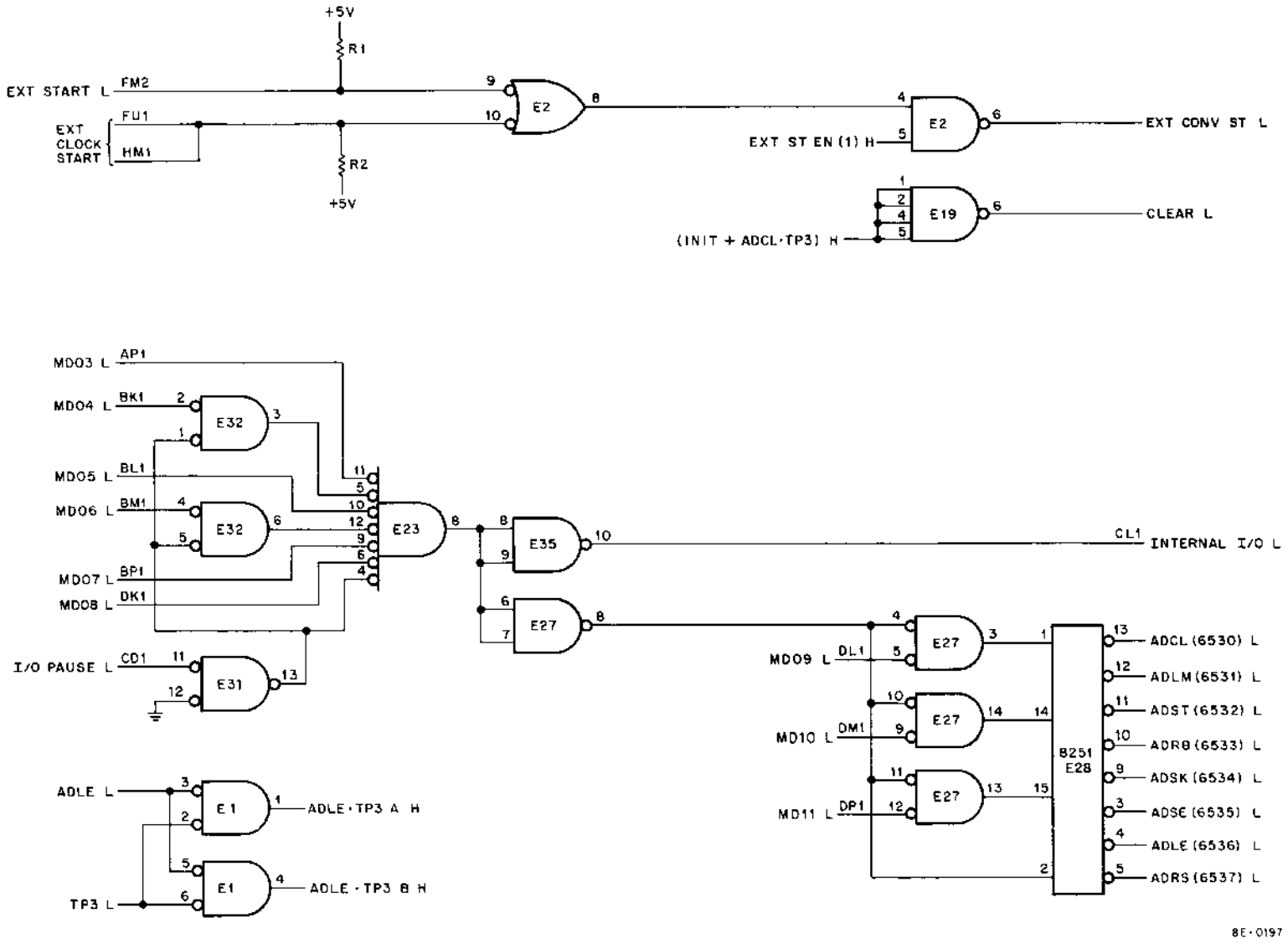


Figure 4-10 Device and Operation Select Logic

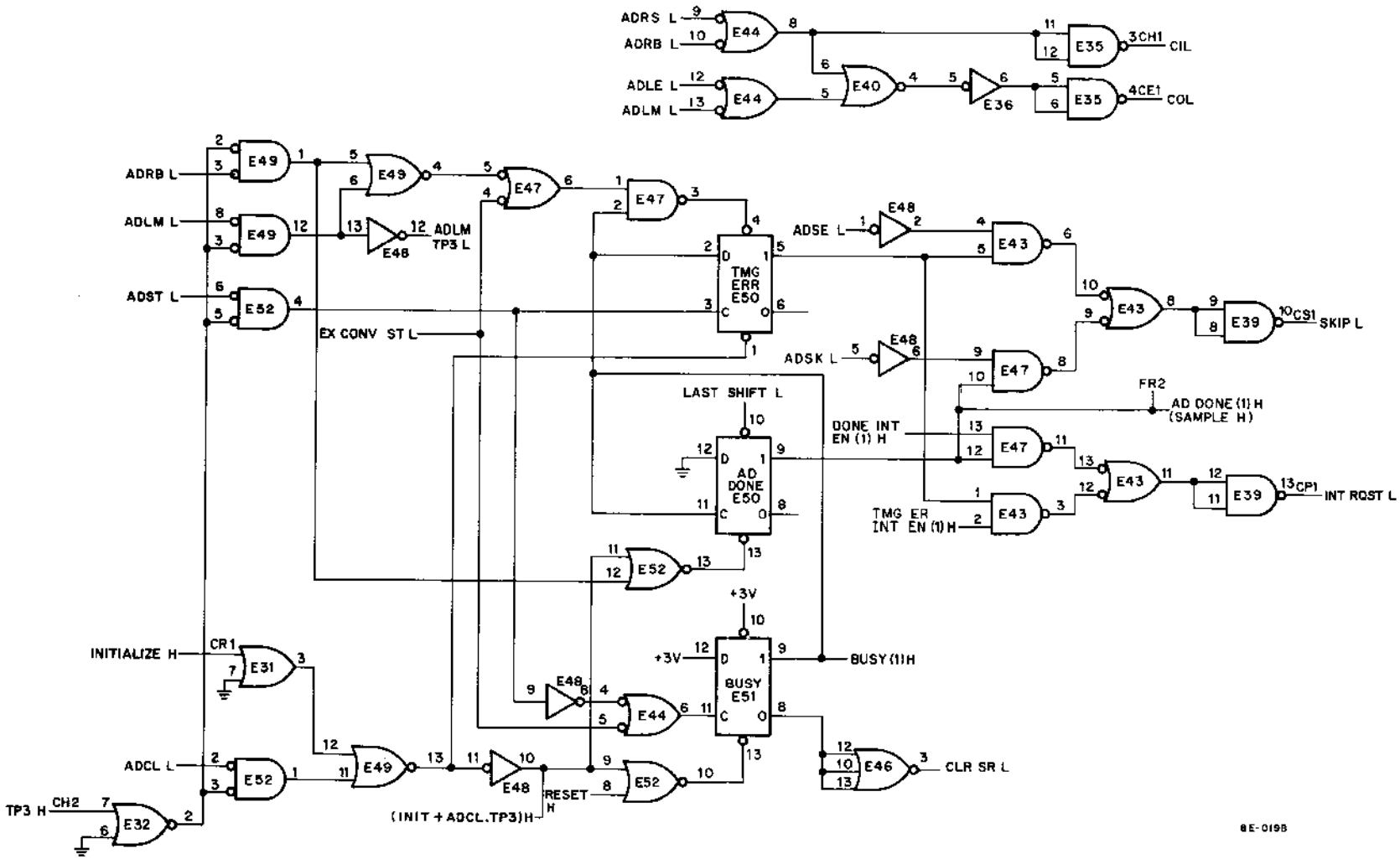


Figure 4-11 Interrupt, Skip, and Control Logic

4.2.2.3.1 C-Line Select Logic – The C-Line Select logic will be used to control the direction of data flow to and from the AC by asserting C0 and C1 (see Figure 4-12). C0 and C1 will be pulled high or low by programmed instructions to OR gate E44. ADRS or ADRB will cause a high output on pin 8 of E44, which will cause E35 pin 3 to go low and pull C1 low. Any of the instructions applied to pins 9, 10, 12, and 13 of E44 will cause the OR gates to output a 1, which will cause pin 4 of E40 to be low. The low out of E40 will be inverted and applied to pin 5 and 6 of E35 and will pull C0 low. Table 4-2 shows the status of C lines to control data flow between the A/D converter and the processor. C2 will remain high because the A/D converter never asserts this line for any instruction.

Table 4-2
C-Line Logic Levels

Type of Transfer	C0	C1	C2
Output, AC unchanged	HI	HI	HI
Output, AC cleared	LO	HI	HI
Input, AC cleared with input data	HI	LO	HI
JAM input	LO	LO	HI

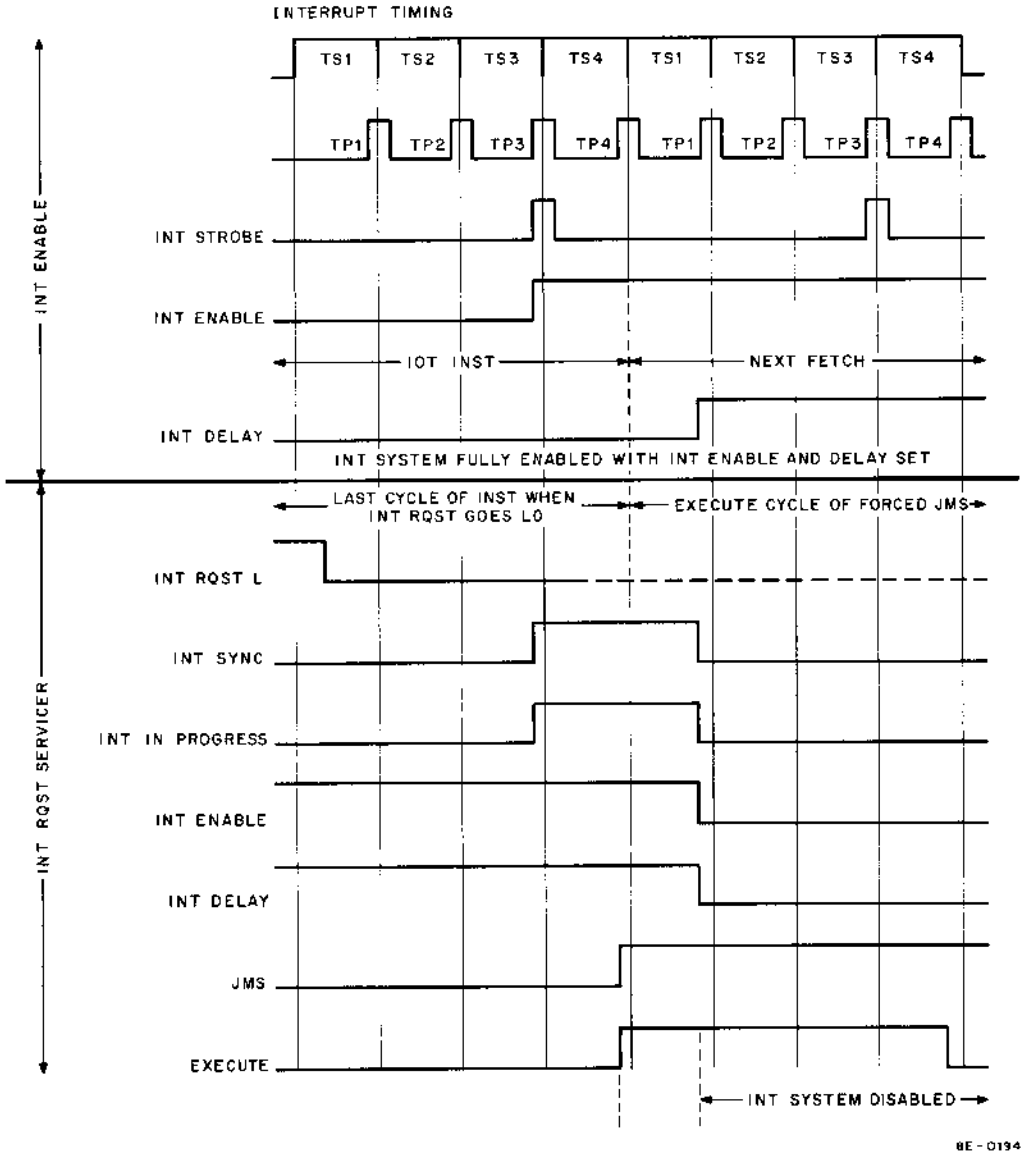


Figure 4-12 Interrupt Timing Diagram

4.2.2.3.2 Interrupt and Skip Logic – Program interrupts are used in the A/D converter to allow the processor to continue the program while the A/D conversion is performed, and to interrupt the processor if a timing error is detected. To generate an Interrupt when the TIMING ERROR flip-flop sets, the TIMING ERROR ENABLE flag must be set in the Enable Register. The TIMING ERROR INT ENABLE flag and TIMING ERROR flip-flop input to pins 1 and 2 of E43 will enable the OR gate and assert the Interrupt request line at pin 13 of E39. An Interrupt on A/D DONE is similar to the timing for Interrupt logic shown in Figure 4-12. Refer to Paragraph 3.9.6 of the *PDP-8/E Maintenance Manual* for a more detailed discussion of Interrupts.

4.2.3 Status Register

The Status Register consists of TIMING ERROR and A/D DONE flags (see Figure 4-7). The TIMING ERROR flag will be used by the A/D converter to detect application of new data to the sample and hold circuits while the A/D conversion is in process. A TIMING ERROR will be generated if instructions ADRB L or ADLM are decoded during an A/D conversion. The BUSY applied to pin 2 of E47 will be present while the HOLD portion of the A/D conversion is in process. If these programmed instructions or EXT CONV START are applied to pin 1 of E47, the gate will output a 1, and set the TIMING ERROR flip-flop. The TIMING ERROR may cause a Skip to be generated and the processor may go to the next instruction without completing the A/D conversion if the ADSE instruction was programmed. Instruction ADSE enables gate E43 and generates a Skip if the TIMING ERROR flip-flop sets. TIMING ERROR will generate an Interrupt request if a TIMING ERROR INTERRUPT ENABLE flag is set in the Enable Register.

The A/D DONE flip-flop will be set by the LAST SHIFT L signal from the Shift register. The set side of the A/D DONE flip-flop will be ANDed with ADSK instruction to generate a Skip. If the DONE INTERRUPT ENABLE flag is set, A/D DONE will enable AND gate E47 and will generate an Interrupt request.

4.2.4 BUSY Flip-Flop

The BUSY flip-flop is set to start an A/D conversion by EXT CONV START or an ADST instruction (see Figure 4-11). The EXT CONV START or the ADST instruction will cause the set side of BUSY to go high, clear A/D DONE, and start the A/D internal clock. The clear side of BUSY will clear the switch register in the switching logic when BUSY is cleared by CLEAR L, INIT, or an ADCL instruction and TP3.

4.2.5 MUX Register Logic

The MUX Register (see Figure 4-13) will select a channel to be applied to the sample and hold circuitry of the A/D converter. The contents of the register will indicate which channel in the multiplexer is currently being sampled. In the Auto-Increment Mode (INC EN = 1), the output will be incremented to select the next channel.

The 8235 IC will be used to gate MUX8–MUX11 to the AC when the ADRS instruction is performed, or to gate ADB8–ADB11 to the AC when an ADRB instruction is performed. The ADRB bits are not used in the MUX Register, but this portion of the IC is used to supply these bits to the Data Bus from the A/D Buffer. Truth tables, timing diagrams, and logic for the 8235 IC are shown in Appendix A of the *PDP-8/E Maintenance Manual.*

The 8235 IC is a 4-bit dual-channel data input logic element. The output is controlled by instructions ADRB and ADRS.

The Look-Ahead data bits, or MUX data bits, will be gated to the data input on the MUX Register flip-flops and will set them to the channel desired. The flip-flops can be set to any octal number 0 through 17. The Look-Ahead output, which is one more than the MUX Register, will also be gated back to the MUX Register by NOT ADLM H, and will increment the register by 1 on RESET H asserted. The Look-Ahead will always be one channel ahead of the MUX Register to allow selection of the next channel. Table 4-3 shows the MUX Register contents and the output of logic which produces the incremented Look-Ahead bits for all 17_8 channels.

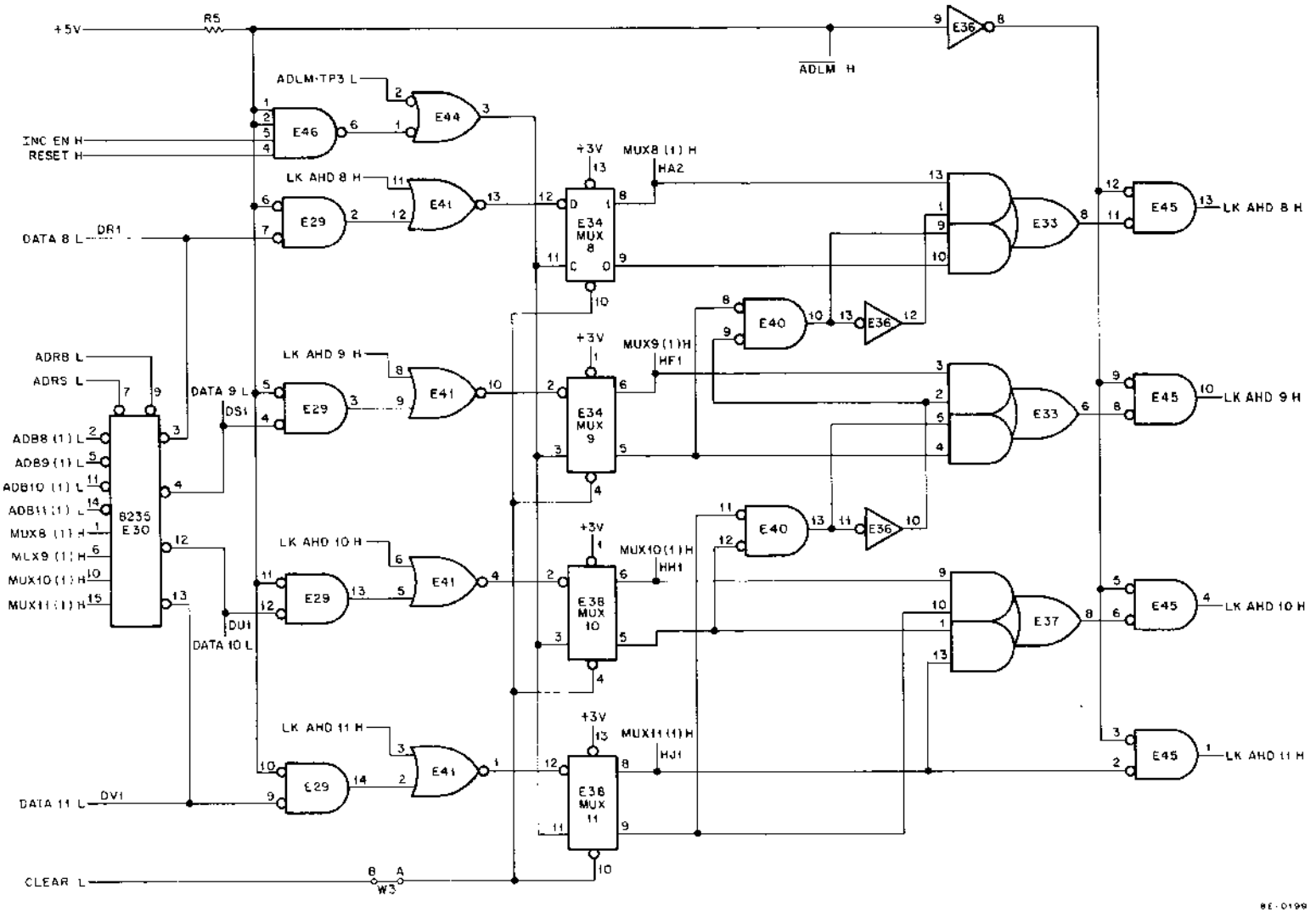


Figure 4-13 MUX Register Logic

Table 4-3
MUX Register Contents and Look-Ahead Bits

Contents of MUX Register				Look-Ahead Bits			
MUX8	MUX9	MUX10	MUX11	LK AHD 8	LK AHD 9	LK AHD 10	LK AHD 11
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	1	1	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	1	0
1	1	1	0	1	1	1	1
1	1	1	1	0	0	0	0

The MUX Register will be cleared by CLEAR L which was generated in the control logic by the ADCL instruction and the INIT L signal. The W3 jumper between A and B of the Clear line can be removed to isolate malfunctioning ICs when troubleshooting.

4.2.6 Enable Register

The Enable Register (see Figure 4-14) will receive AC2—AC5, and will provide enabling signals to the Interrupt and control logic in the A/D converter. The Enable Register (see Table 4-1) is made up of DONE INTERRUPT ENABLE, TIMING ERROR INTERRUPT ENABLE, EXTERNAL START ENABLE, and INCREMENT ENABLE. Any flip-flop in the Enable Register will be set by a 1 from the appropriate AC bit to enable the control logic in the A/D Converter. The 8235 IC will select either ADB2—ADB7 from the A/D Buffer or the contents of the Enable Register for transfer to the AC. The 8235 IC is a 4-bit dual-channel data input logic element which will be controlled by instructions ADRB or ADRS to gate data to the AC. The ADRB instruction will gate the A/D Buffer bits to the Data Bus and the ADRS instruction will gate the contents of the Enable Register to the Data Bus. The ADLE instruction will gate AC data bits 2—5 from the Data Bus to the Enable Register. ADLE and TP3 will be applied to the clock input of each flip-flop to set the flip-flop if there is a 1 on the data input.

The set side of the flip-flops in the Enable Register will be used to enable gates in the control logic (see Figure 4-7). DONE INTERRUPT ENABLE will allow an Interrupt request at the completion of the A/D conversion. To set DONE INTERRUPT ENABLE, a 1 must be transferred from the AC in bit position 2. The other flip-flops will be set in the same manner by bits 3, 4, and 5 from the AC enable gates in the control logic. See Figure 4-7 for bits used by the Enable Register.

4.2.7 Analog Buffer and Sample and Hold Circuits

Figure 4-15 shows the Analog Buffer and the sample and hold circuitry. The E8—E9 Analog Buffer is a differential amplifier with a common-mode balancing potentiometer to balance amplifier gain and null unwanted inputs.

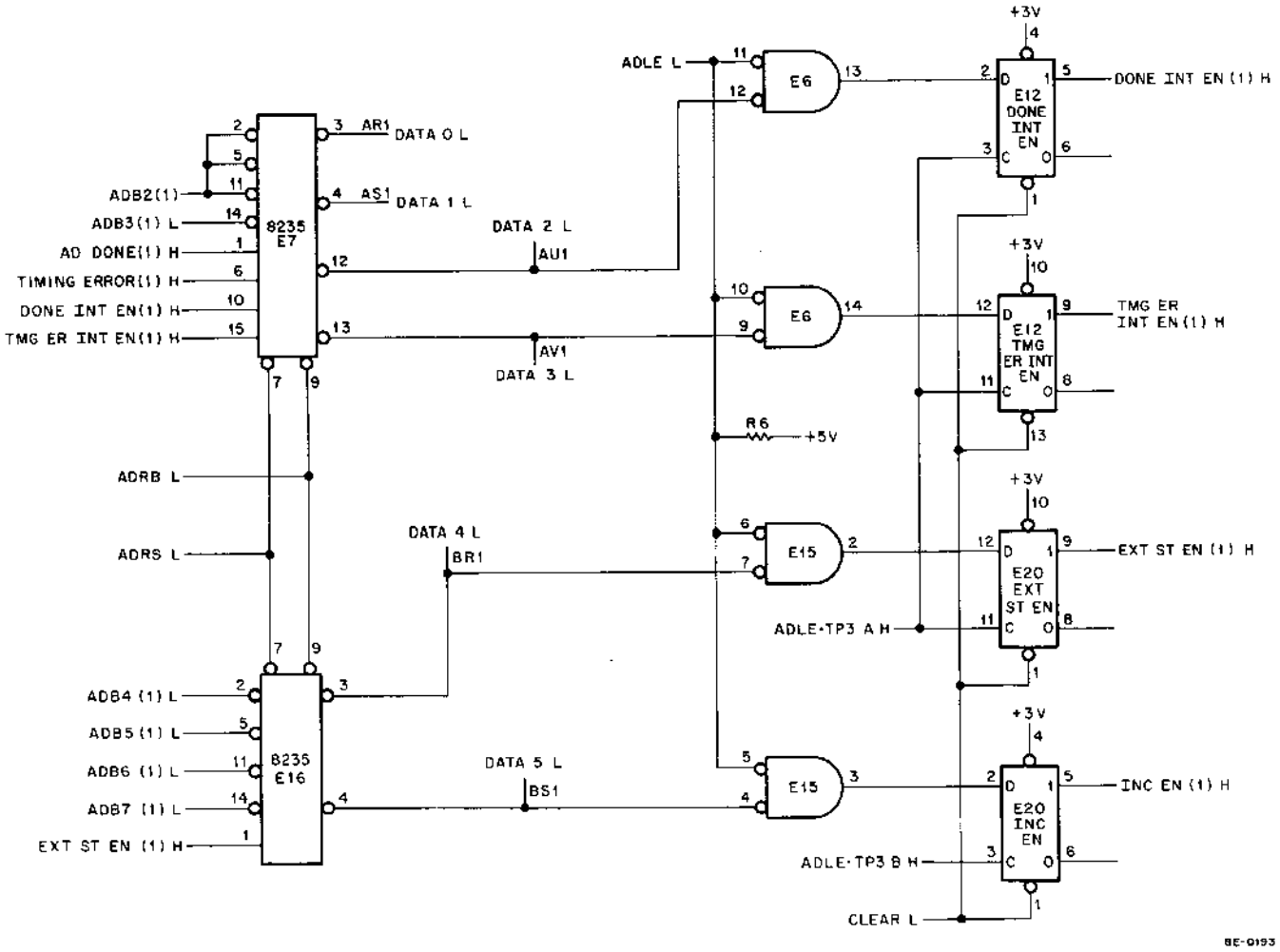


Figure 4-14 Enable Register Logic

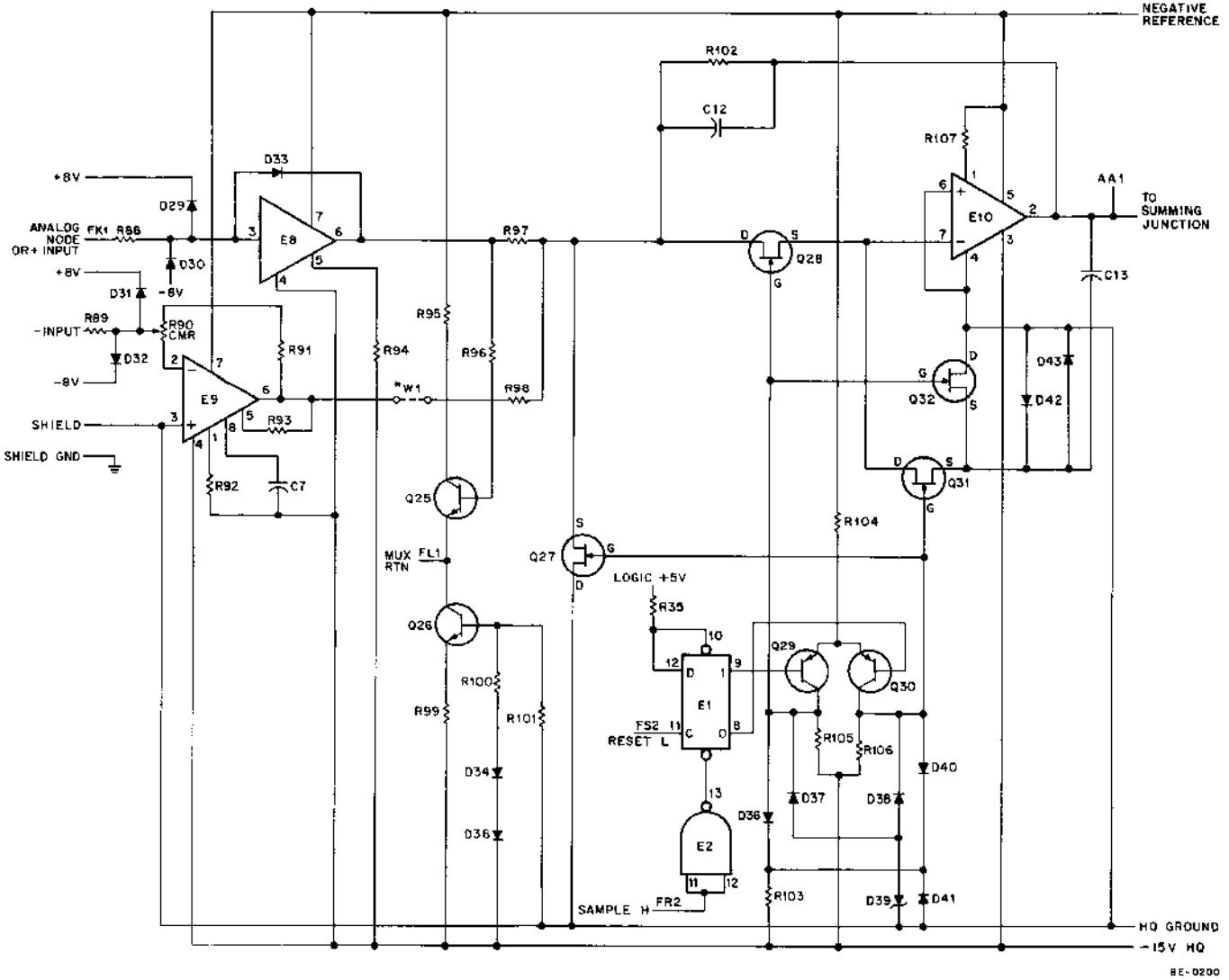


Figure 4-15 Analog Buffer and Sample and Hold Circuits

The CMR potentiometer is adjusted at the factory with a 60-Hz signal applied to both input lines. The signal is monitored at AA1 and the CMR potentiometer is adjusted for a minimum signal. A W1 jumper must be installed if the A232 Analog Preamplifier and Multiplexer Expander module is not installed. The CMR circuit is only useful when W1 is installed to apply differential inputs to the A841 module.

The output of the Analog Buffer is applied to switching circuits which will determine if it is applied to the sample and hold amplifier. Amplifier E10 has two inputs: the output of the Analog Buffer during Sample Mode, and the voltage on capacitor C13 at the summing junction during the Hold Mode. The input to E10 will be determined by the FET transistors Q28, Q27, Q31, and Q32, which are controlled by the MODE SELECT flip-flop E1 and its associated transistors. The FET transistor characteristics are such that they will conduct with 0V on the gate, and cut off with - 15V on the gate. When the FETs are conducting, they look like closed switches; when they are cut off, they look like open switches.

During the Sample Mode, SAMPLE H will enable E2 and clear E1. This will put a low on the base of Q30 and a high on the base of Q29. The Q29 collector will rise to 0V and allow Q32 and Q28 to conduct. Q32 will apply a ground to C13 to allow it to charge to the input voltage, and Q28 will allow the analog signal to be applied to E10. Q31 and Q27 will be cut off by the negative voltage on the gates. The output of E10 will charge C13 during the Sample Mode for sampling during the Hold Mode.

During the Hold Mode, the SAMPLE signal will be removed and HOLD H will be applied to the clock input of E1. E1 will now set and switch the voltages on Q29 and Q30. When the voltage switches, Q28 and Q32 will cut off and remove the ground from C13 and the analog input from E10. Q31 will conduct and the voltage on C13 will be applied to the input of E10. Q27 will conduct and ground the analog input voltage. E10 will maintain the voltage on C13, which will be applied to the summing junction for an A/D conversion. The Sample and Hold Modes can be monitored by applying a 0V to 5V ramp input to the A/D converter, and by monitoring at AA1 (see Figure 4-16). The hold time should be 20 μs; the sample rate will be determined by the program.

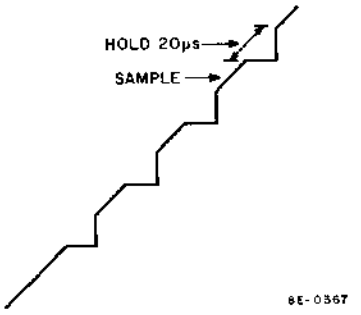


Figure 4-16 Signal at AA1 with a Slow Ramp Input to the A/D Converter

4.2.8 A/D Converter Internal Clock

The A/D converter internal clock (see Figure 4-17) will be used to delay the BUSY signal and to generate a HOLD signal. The clock will supply clock pulses to the Shift Register (see Figure 4-18) to cause the Shift Register to preset to bit position 2 (MSB) and strobe each bit position during an A/D conversion. The clock will start when the BUSY signal is received and generate PRESET, which is applied to the sample and hold circuit putting it into the Hold Mode. The BUSY signal will be applied to three delay networks and will produce a clock high on the outputs of E5. Once the clock is started, it will produce 100-ns pulses, 1.8 μs apart, as long as the BUSY signal is present at E5. These clock pulses will cause the Shift Register to supply a clock input to each flip-flop in the A/D Buffer (see Figure 4-19) to allow each bit position's analog switch to be turned on for checking by the comparator. The timing diagram for the A/D clock is shown in Figure 4-18. PRESET is used to preset the switch register to bit position 2. SR1 through SR10 will be applied to the clock input on each flip-flop in the A/D Buffer to turn on the analog switch for that position. The clock signal is delayed to allow the sample and hold to settle before the A/D conversion starts.

4.2.9 Analog Switches

The analog switches in Figure 4-20 will be turned on to supply current to the summing junction. Each switch has a transistor and weighted resistor which will supply current to the summing junction when a high is applied to the

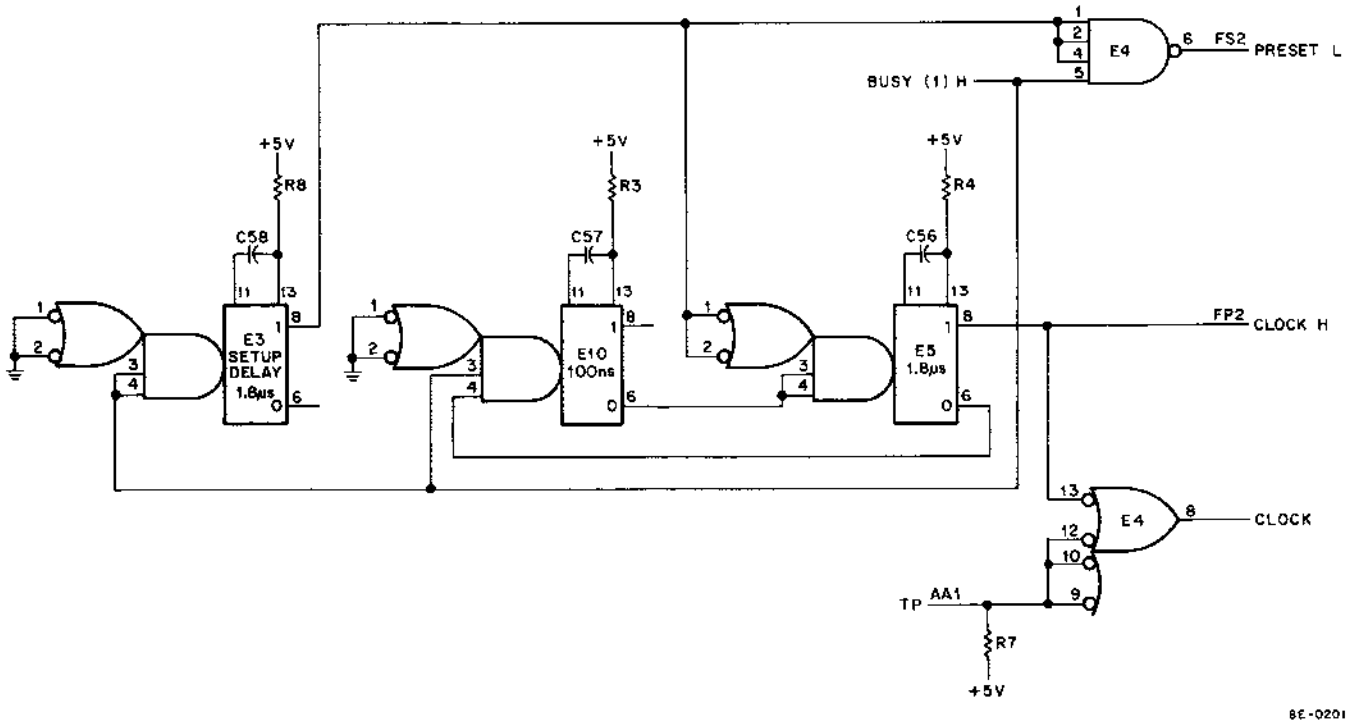


Figure 4-17 Analog-to-Digital Converter Internal Clock

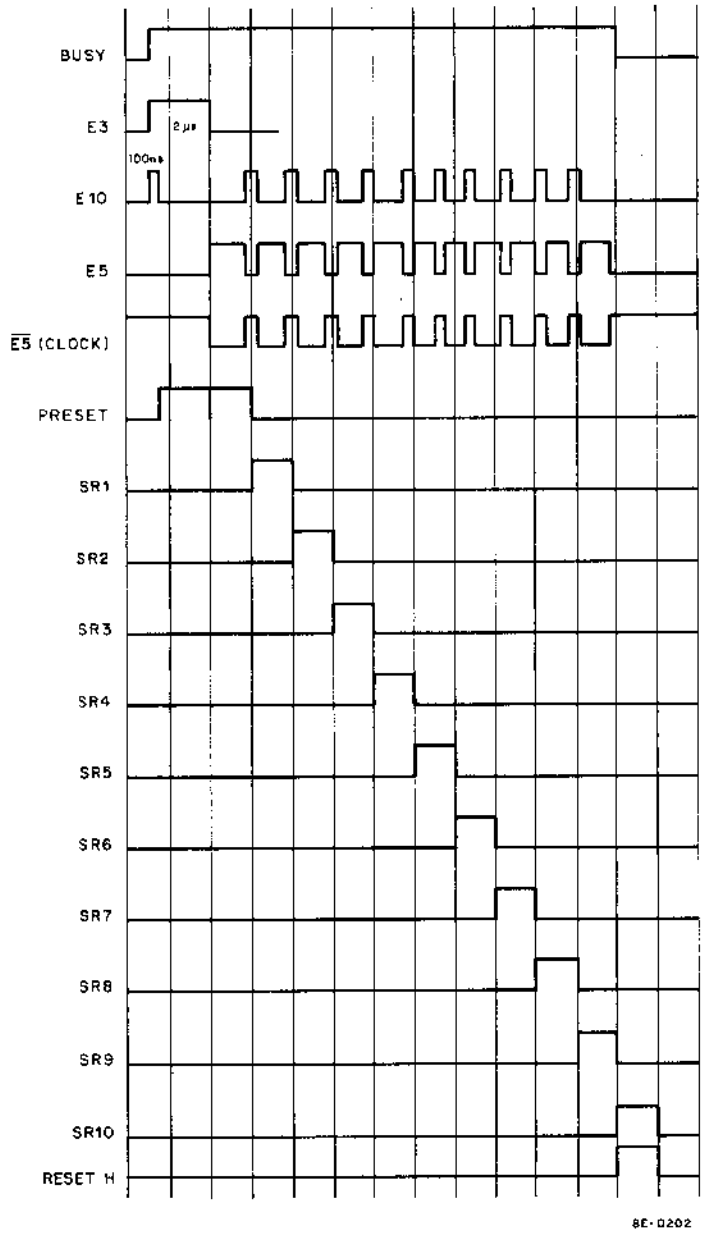


Figure 4-18 Analog-to-Digital Converter Internal Timing Diagram

transistor associated with it. The conduction of the transistor will be determined by the flip-flop in the A/D Buffer, which is set by the Shift Register, to allow each switch to be turned on for the comparator to check the summing junction (see Figure 4-21). The output of the comparator will determine whether the switch is to be turned off or left on. Each switch will supply a given amount of current to the summing junction, based on its position in the weighted-resistor network. The right combination of switches will be selected to supply current to the summing junction and reduce the summing junction to a null voltage when the last bit (bit 11) is checked. The summing junction will be very near 0V. Switches that remain on or off in the A/D Buffer will represent a digital value in proportion to the input voltage.

A switch is turned on (see Figure 4-21), bit ADB10 for example, when the inverter receives a low input. The low into the inverter will apply a high to the base of Q2. Q2 will conduct and supply current to the summing junction through R8, a part of the weighted-resistor network. The switch emitter circuits are discharged to ground through Q3, R7 and R9 to provide a fast recovery time for switches during the A/D conversion.

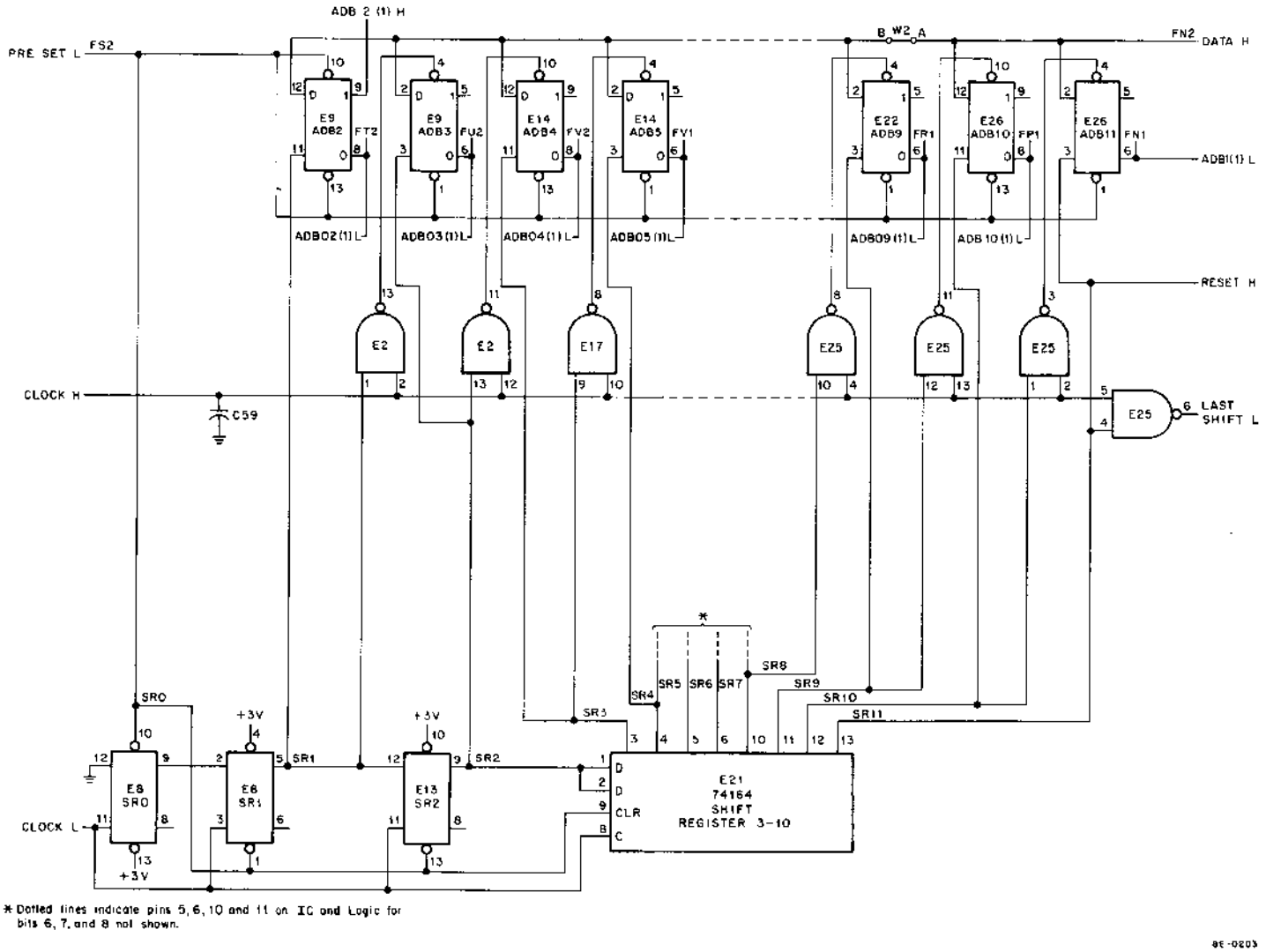


Figure 4-19 A/D Converter Shift Register and Data Buffer

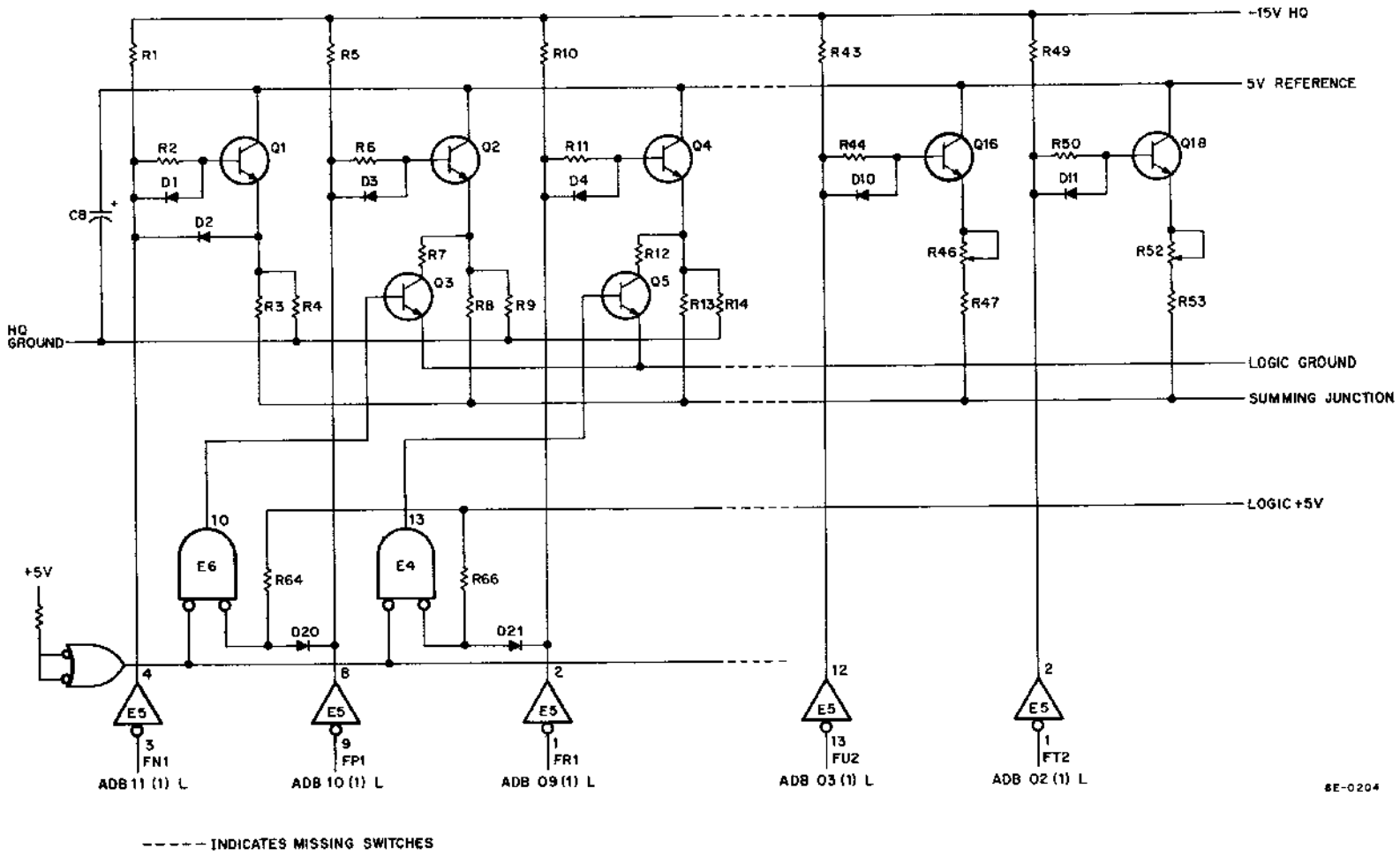


Figure 4-20 Analog Switches

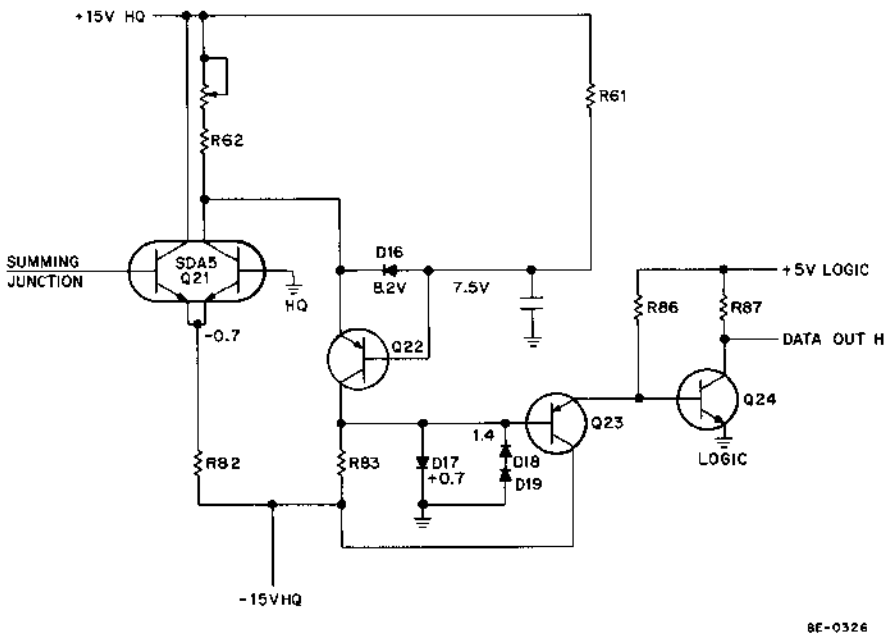


Figure 4-21 Comparator Circuits

4.2.10 Comparator

The comparator (see Figure 4-21) will compare the voltage at the summing junction with 0V (HQ ground) and output a 1 if the voltage at the summing junction is less than 0V, and a 0 if the voltage at the summing junction is greater than 0V. The comparator output will be used to determine the final condition of the flip-flops in the A/D Buffer that control the analog switches.

When the summing junction voltage applied to the base of Q21 is greater than 0V, that side of the transistor will conduct; current from R60 and R62 will flow through the emitter of Q22 to the −15V power supply. The voltage at R83 will be applied to the base of Q23 and will cause the emitter to go positive. The positive voltage on the collector of Q23 will be applied to the base of Q24 and the collector of Q24 will go to 0. A 0 on the collector of Q24 will give a low data output to the A/D Buffer.

When the summing junction is less than 0, the right-hand side of Q21 will conduct and current will flow through the right half of Q21 instead of Q22. The collector on Q22 will go negative and be applied to the base of Q23. The emitter of Q23 will go negative and cause the collector on Q24 to go positive and produce a 1 to be applied to the A/D Buffer as DATA H.

4.2.11 A/D Buffer and Shift Register

The A/D Buffer and Shift Register (see Figure 4-19) will control the analog switches and provide a storage register for the 10 bits of digital data until they are transferred to the AC.

The Shift Register will receive a preset input to clear the flip-flops in the A/D Buffer and select bit position 2 to start the A/D conversion. The clock will also supply pulses to clock the Shift Register and set each bit position for checking by the comparator. The clock pulses (see Figure 4-17) will be 100 ns in duration, will occur every 1.8 μs, and will cause the switch register to strobe each bit position.

The clock pulse (see Figure 4-19) will also enable the gates for the output of the Shift Register to be applied to the set input of the flip-flops in the A/D Buffer. The flip-flop will set and turn on the analog switch to supply

current to the summing junction and will supply an amount of current proportional to its position in the weighted-resistor network. The comparator will be monitoring the summing junction; it will supply a 0 if the voltage at the summing junction is greater than 0V, and a 1 if it is less than 0V. The Shift Register will then switch to the next bit position, supply a signal to be gated by the clock pulse, and set the next flip-flop. It will also supply the clock input of the previous flip-flop. This flip-flop will now have a positive-going edge on the clock input and low or high on the data input. If the data input is high (Vsj>0), the flip-flop will remain set and that bit position will output a low (0). If the data input is low (Vsj<0), the flip-flop will clear and that bit position will output a high (1). Note that the output of the buffer is taken from the 0 side of the flip-flop and the digital data will be in 2's complement form.

The Shift Register and clock will check each bit position and when bit position 11 is checked, LAST SHIFT will be low. LAST SHIFT will be applied to the set side of the A/D DONE (Figure 4-11). It will set A/D DONE to generate an Interrupt request if A/D DONE Interrupt is enabled, or a Skip if the ADSK instruction is performed. The contents of the A/D Buffer will be transferred to the AC using an ADRB instruction. RESET H will be applied to the BUSY flip-flop (Figure 4-11) and will clear the BUSY flip-flop. When BUSY clears the A/D converter, sample and hold will return to the Sample Mode.

Each flip-flop in the A/D Buffer will hold a 1 or a 0 when the A/D conversion is complete. The output of bit position 2 will be taken from the set (1) output and all others will be taken from the clear (0) side of the flip-flop. ADB2 will be used to indicate the sign of the 2's complement number transferred to the AC. If ADB2 remains set, it will be transferred to the AC as a 0, to indicate a positive number, or if it is cleared, a 1 will indicate a negative number. Table 4-4 shows the applied voltages and octal numbers in 2's complement form generated by the A/D conversion. The display-converted value in the AC program in Chapter 5 may be used to read the contents of the A/D Buffer.

Table 4-4
Applied Voltages and Octal Equivalents

Applied Voltages	Octal Equivalent
+4.990	0777
+3.750	0600
+2.500	0400
0.000	0000
−2.500	7400
−3.750	7200
−5.000	7000

The A/D Buffer contents may also be monitored with an oscilloscope at test points on the A841 module. The test points are marked 012 for bit 2, and 3–11 for the remaining bits. With a −7V input to the A/D converter, the A/D Buffer will contain 0000_8, or all 0's. If the display in the AC program is run with a −7V input and the AC reads 7000, the signal for each bit will be as shown in Figure 4-22. The oscilloscope should display a 1.8-μs square pulse with a rise and fall time of less than 750 ns. A rise of fall time of more than 750 ns indicates that the bit being checked is not settling fast enough for the A/D converter to perform accurate conversions.

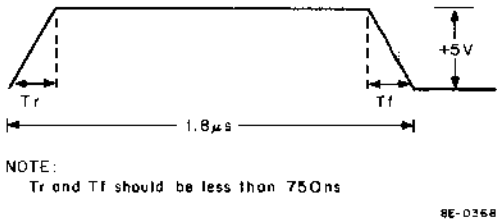


Figure 4-22 A/D Buffer Signal

The signal monitored at AA1, the output of the operational amplifier, should be as shown in Figure 4-23 with a 5V input. AA1 should display a pedestal less than ± 50 mV, approximately 20 μs wide. These pulses are not clearly defined nor free of noise when displayed on the oscilloscope. A faster oscilloscope loop may be loaded to display a brighter waveform.

The summing junction signal and the comparator response to that signal is shown in Figure 4-24. The upper trace shows the summing junction response to an input voltage corresponding to 0106 octal. The first bit is inverted and the remaining bit positions are at different levels to produce a 0106 octal value. The lower trace shows the

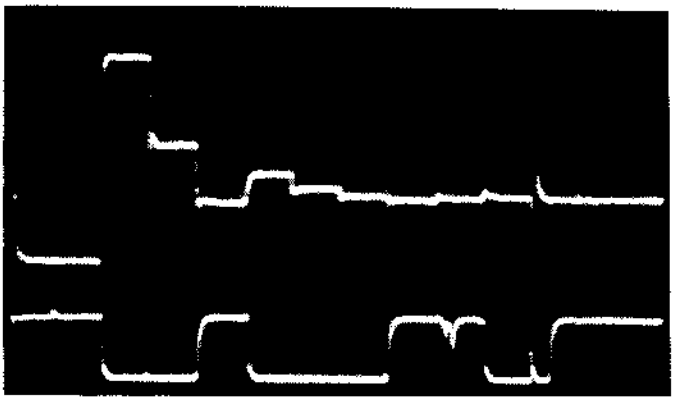


Figure 4-23 Signals at AA1 and Collector of Q20 on the A841 Module

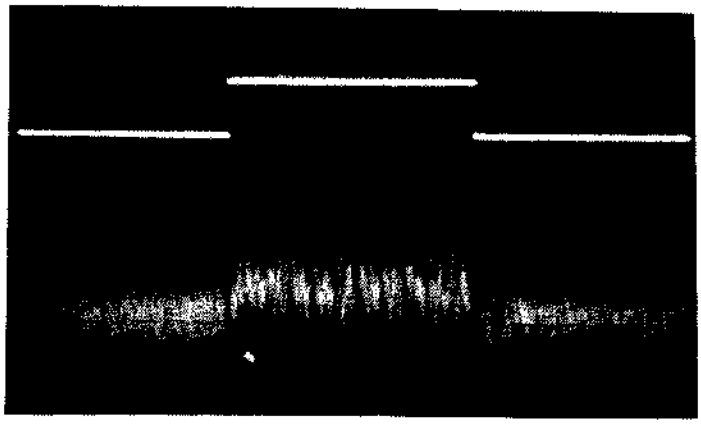


Figure 4-24 Signals at AA1 and Collector of Q20 on the A841 Module

signal produced on the data output in response to the input signal. When the voltage at the summing junction is greater than 0V, data output is 0. When the voltage at the summing junction is less than 0V, the data output will be 1.

NOTE

The signals in Figure 4-23 illustrate SAMPLE and HOLD. The top trace is from the collector of Q20 and the bottom trace was taken from test point AA1. AA1 was monitored with the Y axis set to 10 mV/cm and data output was monitored at 10 V/cm. Input selector should be set to AC to prevent saturating the oscilloscope.

4.2.12 Positive and Negative References

The positive and negative references (see Figure 4-25) are set as a constant current source for the summing junction during an A/D conversion. The positive reference will be applied to the transistor for each analog switch (see Figure 4-20) to supply a +5V reference. R57 is used to adjust the positive reference. The reference voltages effectively adjust the gain and offset of the A/D converter. The positive reference affects gain and the negative reference affects the offset. If ±5V inputs cannot be spanned, the reference voltages should be adjusted (see Chapter 5). The negative reference will supply a constant current to the summing junction; R35 is used to adjust the negative reference.

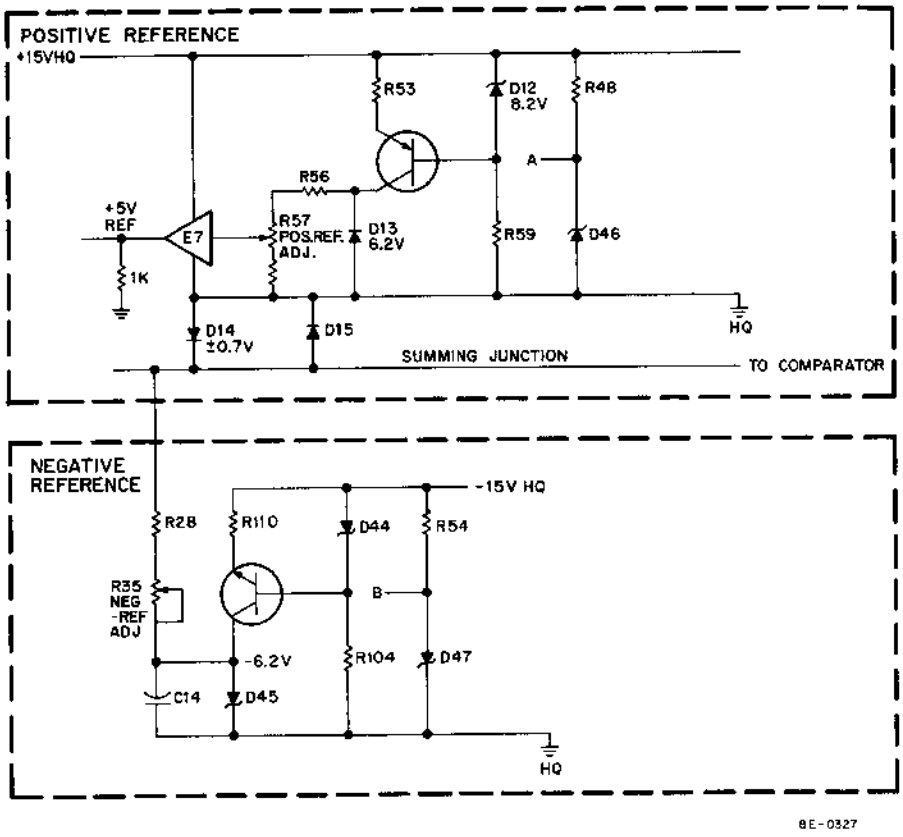


Figure 4-25 Positive and Negative References

SECTION 3
ANALOG PREAMPLIFIER AND MULTIPLEXER

4.3 INTRODUCTION

The AM8-EA Analog Preamplifier and Multiplexer consists of one A232 quad module plugged into the OMNIBUS (see Figure 4-26). The AM8-EA interfaces with the AD8-EA by an H851 Edge Connector, and with the outside world through an AM8-ED or AM8-EC Analog Input Panel, or a 7008533 cable plugged into a side connector. Each A232 module provides for eight ±1V inputs and provides the A/D converter with ±5V output. The AM8-EA 8-channel multiplexer consists of multiplexer switches and scaling amplifiers for 8 analog channels. The AD8-EA A/D converter can be expanded to 16 channels by using 2 AM8-EA modules.

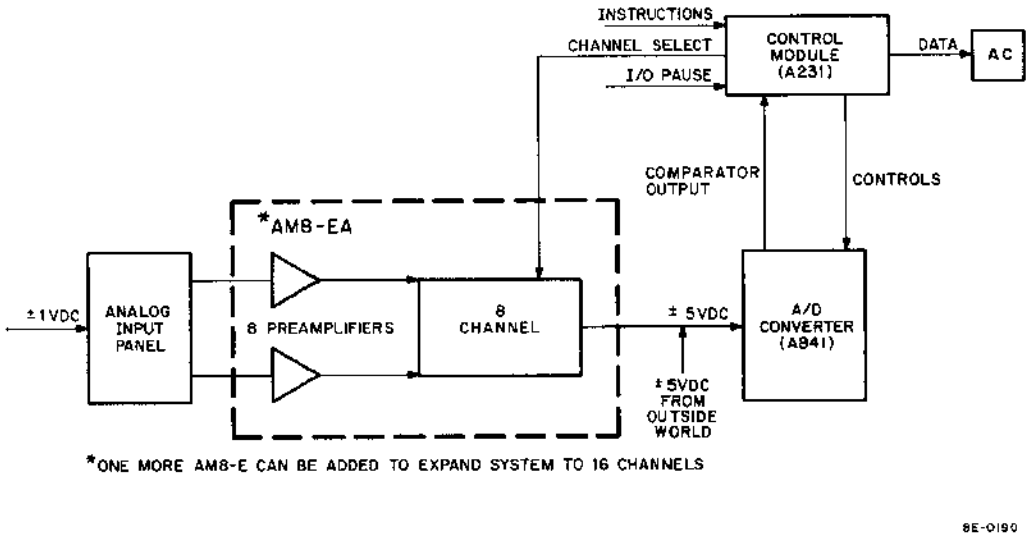


Figure 4-26 Analog Preamplifier and Multiplexer Block Diagram

Multiplexer channel selection is controlled by the AD8-EA Analog-to-Digital Converter to allow random or sequential sampling of analog inputs. There are two modes of operation: Auto-Increment and Non-Auto-Increment. The mode of operation is selected by the ADLE instruction which loads the Enable Register in the A/D converter. If bit 5 is a 1, the INCREMENT ENABLE flip-flop will set and the multiplexer will be in the Auto-Increment Mode. The Look-Ahead bits from the A/D converter will select channels 0 octal through 17 octal, in sequence. If bit 5 is a 0, the INCREMENT ENABLE flip-flop will not be set and the MUX Register in the A/D converter will be loaded from the AC to select a channel in the multiplexer.

HQ ±15 Vdc power is supplied by an H851 Edge Connector from the AD8-EA. The AM8-EA provides ±1 Vdc to the AM8-EC analog panel, if it is part of the system. This voltage is applied to the four potentiometers on channels 0 through 3.

4.3.1 Analog Preamplifier and Multiplexer Expander Block Diagram

The analog multiplexer expander (see Figure 4-27) consists of eight differential amplifiers, a Channel Select Decoder, and eight analog switches. The input to the differential amplifiers is a ±1V signal which will be amplified to ±5V for the A/D converter. The differential amplifiers have a gain of 5 and contain compensation circuits for amplifier stability. Linearity is maintained by feedback networks and gain adjustments.

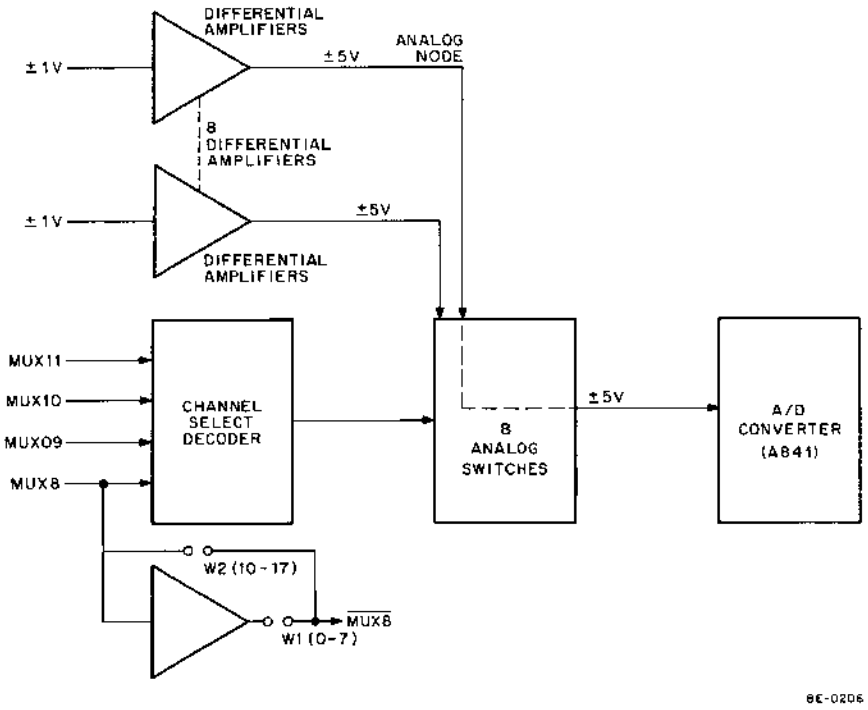


Figure 4-27 Analog Preamplifier and Multiplexer Expander Functional Block Diagram

The Channel Select Decoder will receive MUX8—MUX11 and will generate a low on one line to the analog switch. This turns the switch on to choose that channel of data. The switch will be turned off with −15V when a high output is supplied by the decoder to the gate of the switch. The analog switches are FET transistors which look open with −15V on the gate, and short with 0V tied to the gate. The output of the differential amplifier selected will be fed through an edge connector to the A/D converter. MUX8 will be inverted and supplied to the second multiplexer module, if there is one installed, to expand the system to 16 analog channels. The second module will be selected when MUX8 is 1. The 0—7 or 10—17 jumper must be installed on the corresponding A232 module to allow correct channel selection.

4.3.2 Analog Preamplifier and Multiplexer Expander Detailed Logic

4.3.2.1 Differential Amplifiers – Figure 4-28 shows one of the eight differential amplifiers used in the preamplifier and multiplexer expander module. For this discussion, we will refer only to channel 1 (E9 circuitry). The positive input to channel 1 is applied to pin FF, negative to JJ. Two adjustments are provided for this circuit. R138 (bias) is an offset adjustment which sets to amplifier output (OUT 1) equal to 0V for 0V input between FF and JJ. The gain adjustment, R133, will set the amplifier gain to swing ±5V for a ±1V change across FF and JJ.

Diodes D47 and D48 clamp pin 3 at ±3V, while diodes D51, D52, D49, and D50 tend to keep E9 from going into saturation when the output voltage begins to exceed ±6V. This allows an 8-μs recovery time due to input overvoltage and protects the circuitry from damage. Capacitor C33 rolls off the gain at about 30 kHz to give the amplifier a low pass characteristic and to stablize the circuit against oscillations.

The amplifier output circuit contains a number of resistances in series-to-ground connected to R131 on the amplifier output. When the gain is properly adjusted, 1/5 of the output voltage will appear on the wiper of R133. This signal is fed back to the input to give the amplifier its inherent gain of 5. The voltage on R130 is varied by

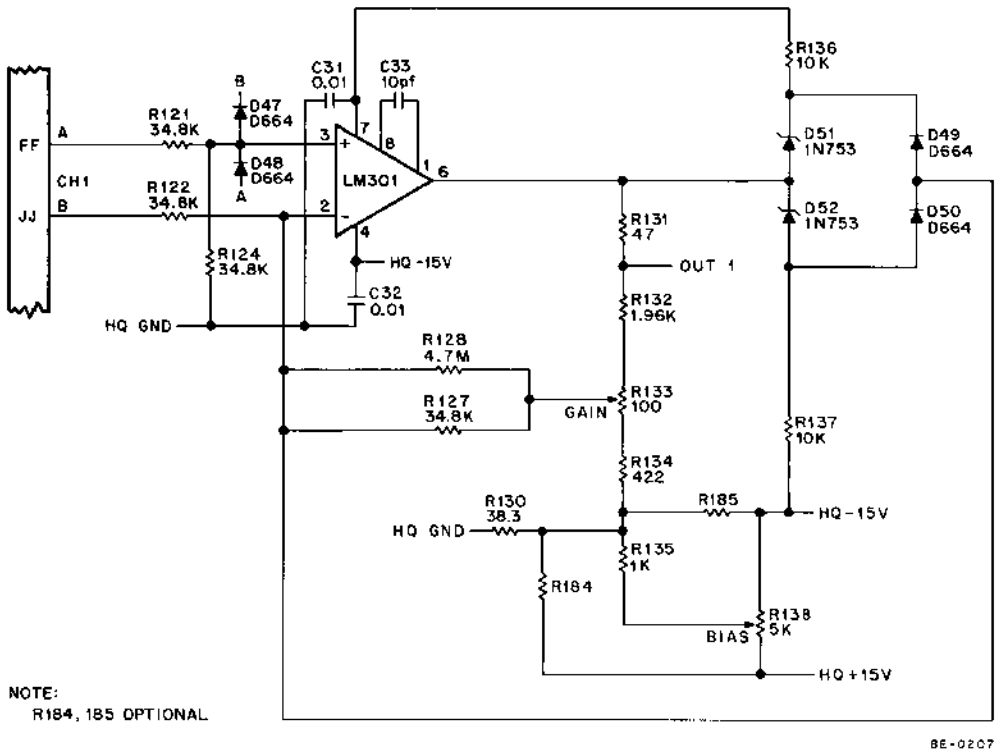


Figure 4-28 Differential Amplifier

adjusting the potentiometer R138, which is reflected on the amplifier output as a dc offset. R184 and R185 are optional resistors used to shift the offset above or below 0V. R131 serves as a current limiter to protect the E9 operational amplifier from damage in case of a short circuit.

4.3.2.2 Channel Decoder and Analog Switches

The Channel Decoder (see Figure 4-29) will receive MUX8—MUX11 from the A/D converter, decode the four bits, and produce a low on one output line. The 8251 is a BCD-to-Decimal decoder which will produce a low output on one line to represent one number. As an example, 0011 on the input will produce a low on line 3 to allow the channel 3 voltage to pass through the analog switch to the analog node. The truth table, logic diagram and pin locator for the 8251 IC are shown in Figure A-7 of the *PDP-8/E Maintenance Manual.*

The FET transistors are used as analog switches. All but one of the switches will be cut off to select an output channel. To cut off the switch, −8V must be applied from gate-to-source and 0V must be applied to turn it on. As an example, assume channel 1 is turned off and pin 12 of E1 is high. Q44 is turned on because of a current flowing through R180 to the base of Q44 (clamped at 3.6V). Because Q44 is on, the collector current will raise the potential on R172, turning Q35 on and reducing the voltage on Q27 to almost −15V. The gate of Q27 is now negative, thus making the drain-to-source resistance of Q27 very high, not allowing the channel 1 output to appear on ANALOG NODE.

Turning the channel on involves the use of the MPX RETURN signal. The MPX RETURN signal, originating in the A841 module, is identical to ANALOG NODE except that it is 0.7V (1 diode drop) less. When channel 1 is selected, the current through R180 is removed from Q44 and channeled through D73. Q44 and Q35 turn off and the gate of Q27 (the FET) starts rising towards +15V. As soon as this voltage is 0.7V higher than MPX RETURN, diode D65 is turned on and the gate rests at a voltage equal to that of ANALOG NODE. The gate-to-source voltage of Q27 is now near 0V, leaving the drain-to-source resistance at its minimum, and allowing channel 1 to appear on ANALOG NODE. The rise time of the maximum change on ANALOG NODE (10V) should be less than 2 μs.

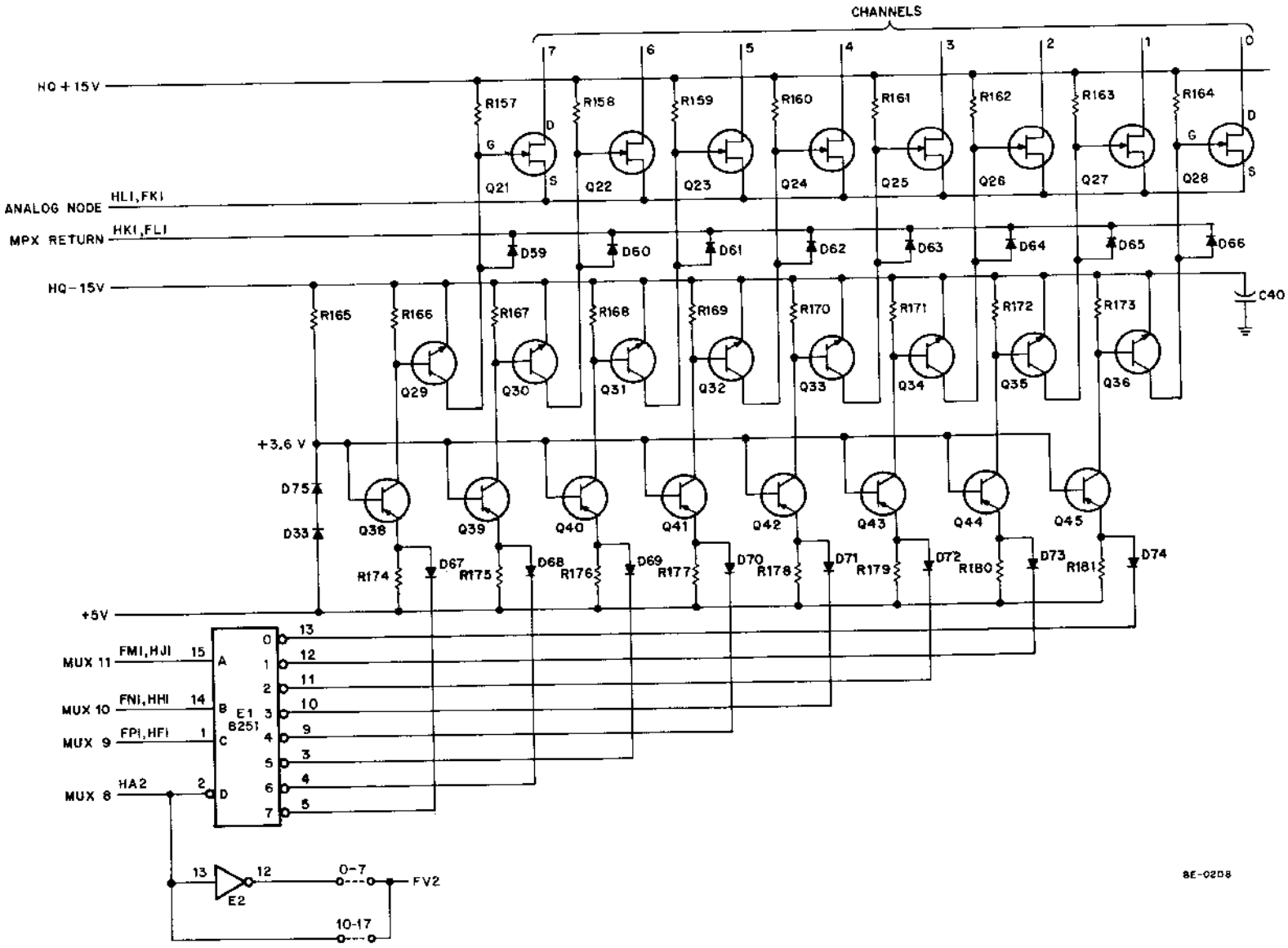


Figure 4-29 Channel Decoder and Analog Switches

4.3.2.3 Reference Voltages – The AM8-EA provides ±1 Vdc and A or B ±2.1 Vdc reference voltages (see Figure 4-30). The ±3 Vdc is used by the diodes on the input of the differential amplifiers to limit the input to ±6 Vdc. The ±2.1V is taken off the diodes as shown in Figure 4-30. The diodes and resistors make up voltage divider networks to produce ±3V. The ±1V reference is generated in the AM8-EA and applied through a cable to the AM8-EC panel, if it is installed, for parameter potentiometers. The ±1V is produced by a voltage divider network made up of a 6.2V Zener and resistors. The ±15V HQ power is supplied to the voltage dividers from the H851 Edge Connector.

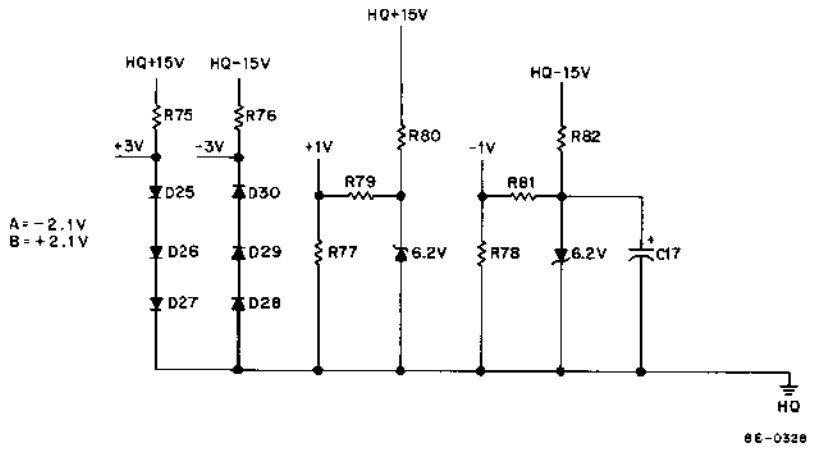


Figure 4-30 AM8-EA Reference Voltages

4.3.2.4 Optional Multiplexer Configurations

The A232 preamplifier and multiplexer module is standardly supplied with a ±1V input to achieve a ±5V output (gain of 5). It is sometimes useful to a given application to be able to span other input ranges in a given experiment or process measurement.

Should a user wish to have special input parameters, each channel can be adapted by changing components on the module. Note that alteration of the module is not the responsibility of Digital Equipment Corporation, nor is it the company's responsibility to warrantee or maintain the module once it has been altered. Note also that alteration of channels 0 through 3_8 of a system will affect the operation of the parameter knobs of the AM8-EC panel. These knobs have a ±1V output, and feeding this into an amplifier of other than ±1V input will not allow the knob to properly span the full 10-bit range.

Table 4-5 shows the differences in values for the most useful input ranges. Channel 1 is cited as an example, but again, it is not recommended that the first 4 channels be altered.

The components in Table 4-5 may be ordered from DEC using the part numbers shown in Table 4-6. All component changes are part-for-part replacements except in the case of R184 and R185. Mounting holes for these optional resistors are provided on A232 etch-revision D modules and higher. Lower revisions will require mounting these parts on the module where convenient.

Any change to the module may alter any of the specifications stated for the unit so that parameters such as gain, common mode rejection, input impedance, etc., will vary in accordance with the part values and tolerances utilized.

Table 4-5

Resistors for Changing Input Configuration

Input Range	R121	R122	R124	R127	R128	R132	R134	R130	R184	R185
±1 Standard	34.8K	34.8K	34.8K	34.8K	4.7M*	1.96K	422	38.3	None	None
0 – +2	34.8K	34.8K	34.8K	34.8K	4.7M*	1.96K	348	90.9	None	1.2K*
±5	68.1K	68.1K	12.1K	12.1K	365K	2.61K	422	90.9	None	None
±10	64K	64K	3.48K	3.48K	39K	2.61K	261	38.3	None	None
0 – –2	34.8K	34.8K	34.8K	34.8K	4.7M	1.96K	348	90.9	1.2K*	None
0 – +10	68.1K	68.1K	12.1K	12.1K	274K	2.61K	422	75	None	1.2K*
0 – +5	68.1K	68.1K	21.5K	21.5K	1M*	2.74K	422	51.1	None	1.2K*

*These resistors are 1/4W carbon composition devices; all other resistors are 1/8W 1% metal film units.

Table 4-6

AM8-EA Configuration Change Parts List

Part Number	Description	Part Number	Description
1303156	Resistor 34.8K 1/8W 1% 100 MFP	1302873	Resistor 261 1/8W 1% 100 MFP
1304833	Resistor 1.96K 1/8W 1% 100 MFP	1303155	Resistor 21.5K 1/8W 1% 100 MFP
1303067	Resistor 422 1/8W 1% 100 MFP	1301506	Resistor 1M 1/4W 10% CC
1305121	Resistor 38.3 1/8W 1% 100 MFP	1305131	Resistor 274K 1/8W 1% 100 MFP
1309341	Resistor 4.7 Meg 1/4W 5% CC	1305515	Resistor 64K 1/8W 1% 25 MFP
1305122	Resistor 51.1 1/8W 1% 100 MFP	1305266	Resistor 365K 1/8W 1% 100 MFP
1303303	Resistor 2.61K 1/8W 1% 100 MFP	1304868	Resistor 2.74K 1/8W 1% 100 MFP
1305252	Resistor 68.1K 1/8W 1% 100 MFP	1303064	Resistor 75 1/8W 1% 100 MFP
1303313	Resistor 12.1K 1/8W 1% 100 MFP	1303037	Resistor 90.9 1/8W 1% 100 MFP
1305114	Resistor 3.48K 1/8W 1% 100 MFP	1301320	Resistor 1.2K 1/4W 5%
1302514	Resistor 39K 1/4W 5% CC	1304858	Resistor 348 1/8W 1% 100 MFP

When an amplifier has been modified, the unit's bias and gain adjustment will have to be adjusted. The bias adjust (R138) should be set to switch the AC between 7777 and 0000 with the analog input 1/2 bit below midscale (see calibration procedure in Chapter 5 for set up). The value of 1 bit can be determined by dividing 9.76 mV by the amplifier gain. Next, adjust the gain adjust (R133) to switch between 0776 and 0777 when the input voltage is 1-1/2 bits below full scale. Setting the input voltage 1/2 bit positive above negative full scale should achieve the 7000–7001 switching point in the AC. Slight readjustment of the gain and bias potentiometers might be required to get the best symmetry near midscale.

For example, on a 0V to +5V amplifier, readjust gain and bias as follows:

a. The gain is: $\frac{10V\ (output)}{5V\ (input)} = 2$

b. 1 bit = $\frac{9.76\ mV}{2} = 4.88\ mV \approx 5\ mV$

c. Set 0000–7777 switching point at:

$2.500 - .0025 \cong 2.498V$

with bias potentiometer.

d. Set 0776—0777 switching point at:

$5.000 - .0075 \cong 4.993V$

with gain potentiometer.

e. Check 7000—7001 switching point at:

$0.000 + .0025 = 2.5\ mV$

Readjust gain and bias, if required, to obtain correct readings in the AC.

NOTE

The components utilized, and the environment in which the A232 module operates, do not allow operation of unit at a gain greater than 5.

SECTION 4
POINT-PLOT DISPLAY CONTROL (VC8-E)

4.4 INTRODUCTION

The VC8-E Point-Plot Display Control is made up of two quad modules which plug into the OMNIBUS. The VC8-E consists of one M869 control module and one M885 D/A converter module. The two modules are joined by H851 Edge Connectors. The inputs to the VC8-E are two 10-bit digital words from the AC, representing X and Y coordinate data. The outputs of the VC8-E are two analog signals proportional to the digital input, and an intensity pulse. The analog signals are ±5 Vdc for display on an oscilloscope.

The VC8-E display control provides deflection and intensity signals for DEC VR14, VR20, Tektronix 611, 613, 602, or user oscilloscopes. The display on the oscilloscopes is in the form of a 1024_8 by 1024_8 dot array (see Figure 4-31). The LAB-8/E can produce a bright spot at any point on this array and a series of bright dots can be programmed to produce a graphical display.

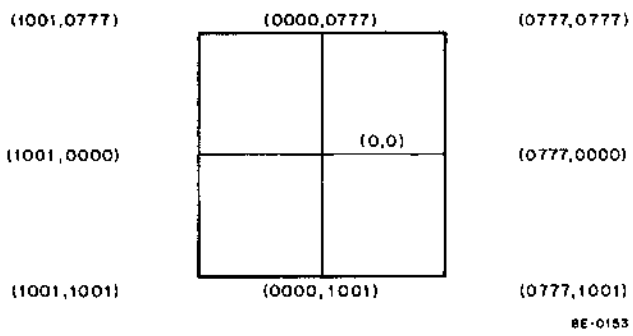


Figure 4-31 Point-Plot Display of Coordinate Data

The basic VC8-E (see Figure 4-32) comprises the following functional logic and controls:

a. OMNIBUS interface, IOT decoding, Skip, CLEAR AC, and Interrupt Control.

b. X-axis Buffer, D/A converter, summing amplifier, and bipolar line driver.

c. Y-axis Buffer, D/A converter, summing amplifier, and bipolar line driver.

d. Z-axis control consisting of INTENSIFY PULSE and CHANNEL SELECT signals for the oscilloscope.

e. A color, 611, 613 controller available only on M869 Rev D and M885 Rev F or higher revs.

NOTE
The VR20 color display is no longer available at the time of this printing. However, information pertaining to the VR20 control is supplied for information purposes.

The VC8-E receives two 10-bit data words from the accumulator for each dot to be displayed on the oscilloscope. One word will represent the X-axis position and one word will represent the Y-axis position. This data comes from bits 2–11 of the accumulator and must be in the range of ±0777 (octal) (see Figure 4-33). Bit 2 is the sign bit that determines the polarity of the dc voltage out of the Point-Plot Display Control (1 = negative, 0 = positive).

The 10 bits of data from the AC will be used by the Point-Plot Display Control to control analog switches (see Figure 4-34) in series with the input to a summing amplifier. The analog switches, in conjunction with a weighted resistor, will supply current to the input of a summing amplifier. Each switch that is turned on will supply a current to the summing amplifier proportional to its position in the weighted-resistor network. The sum of all the currents flowing through the individual switches and resistors will be proportional to the 10-bit octal value transferred from the AC. The switches shown in Figure 4-34 are mechanical switches, but the electrical switches (see Figure 4-35) will perform the same function. A low input on the transistor will cut the transistor off and allow

diode D1 to conduct and supply current through the weighted resistor RW to the input to the summing amplifier. A high input will cause the transistor to conduct; current flow will be through the transistor to ground and no current will be supplied to the node by the weighted resistor. Using two sets of analog switches and two summing amplifiers (X and Y axis), along with the necessary control logic, the Point-Plot Display Control will produce ±5 Vdc analog signals for display on an oscilloscope.

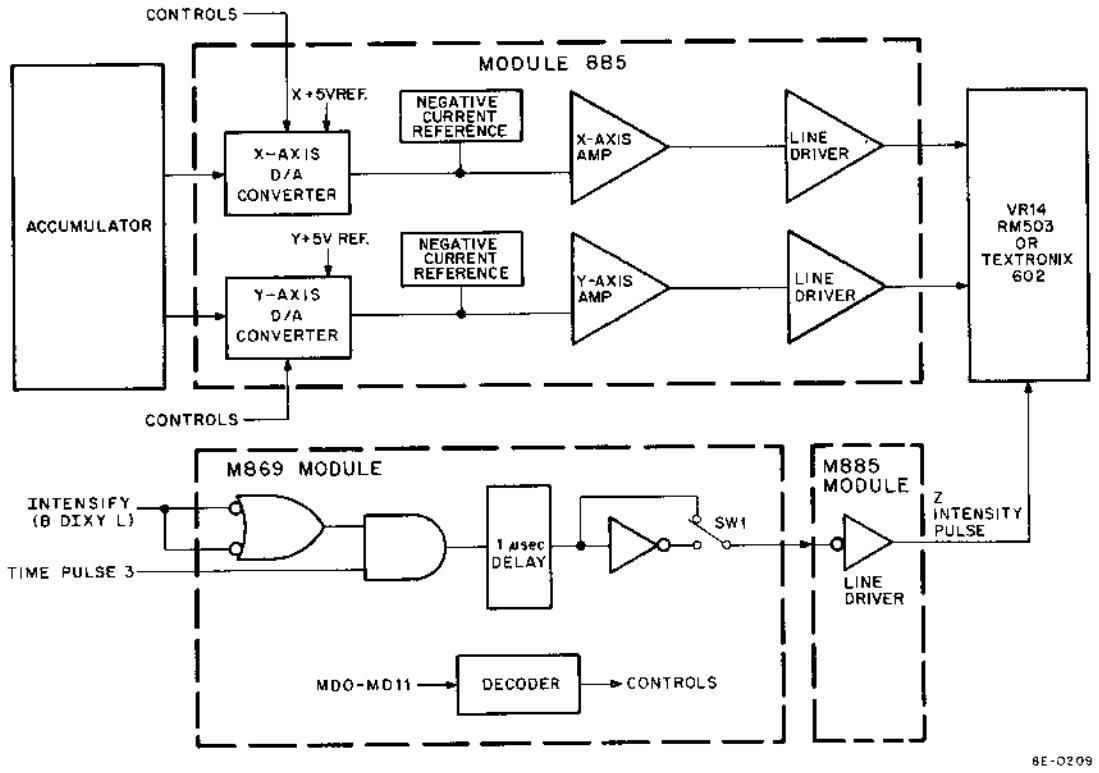


Figure 4-32 Point-Plot Display Control Block Diagram

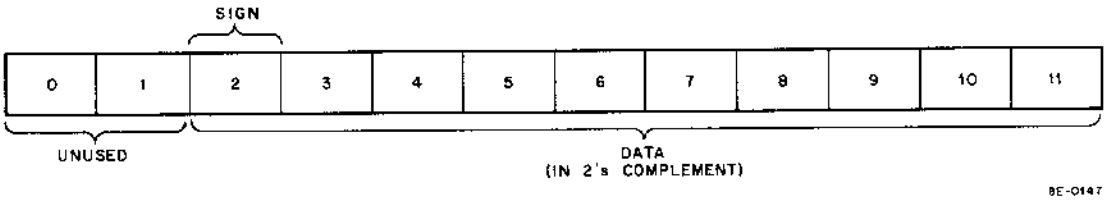


Figure 4-33 AC Input Data Format

The following instructions are decoded and used by the Point-Plot Display Control to control the generation of analog data and an intensity pulse for an oscilloscope to display X and Y coordinate data.

Clear All Logic (DICL)
Octal Code: 6050
Operation: Clears ENABLEs, flags, and delays.

Clear DONE Flag (DICD)
Octal Code: 6051
Operation: Clear DONE flag.

Skip on DONE Flag (DISD)
Octal Code: 6052
Operation: Skip if DONE flag = (1). Do not clear DONE flag.

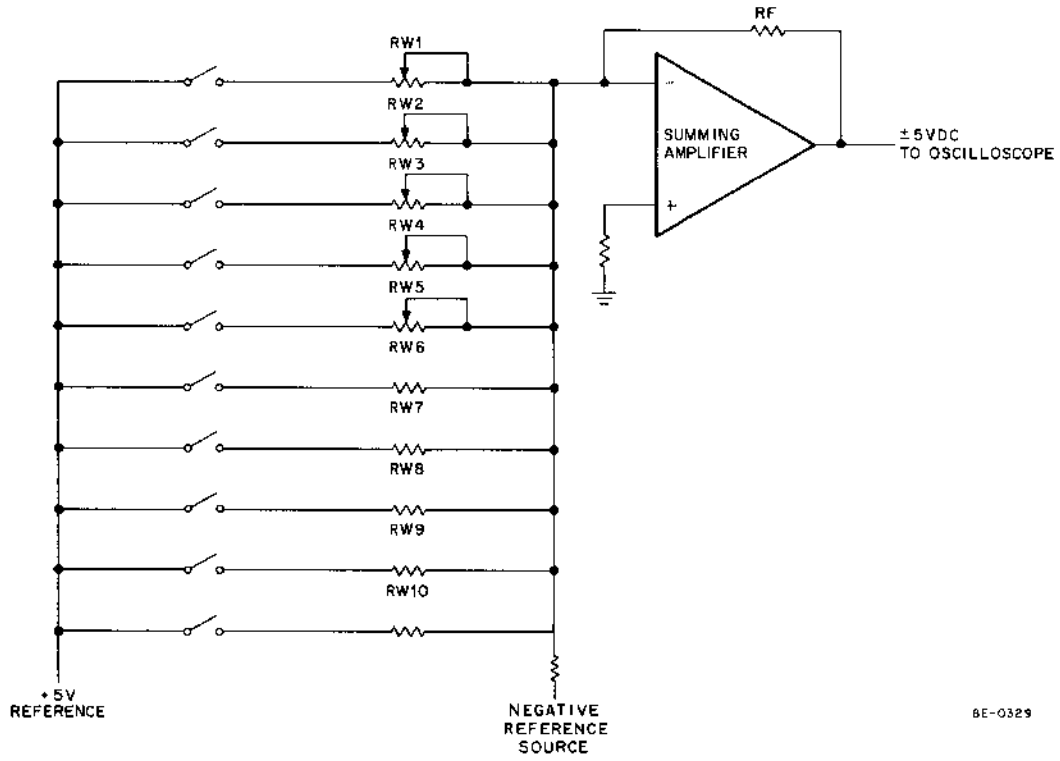


Figure 4-34 Analog Switches and Summing Amplifier

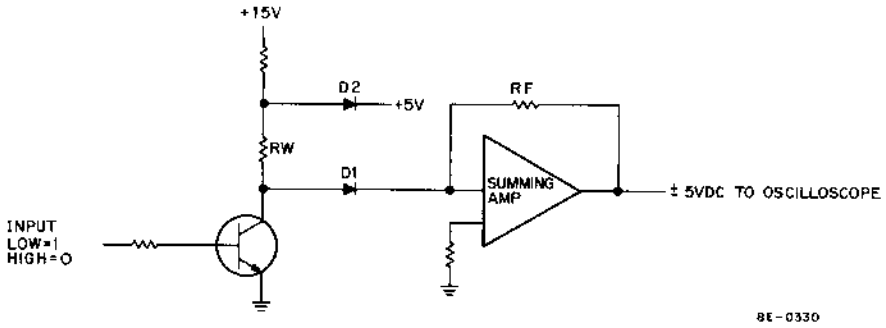


Figure 4-35 One Analog Switch and Summing Amplifier

Load X Register (DILX)

Octal Code: 6053

Operation: Clear DONE flag, load X, wait for settle, set DONE flag. Do not clear AC.

Load Y Register (DILY)

Octal Code: 6054

Operation: Clear DONE flag, load Y, wait for settle, set DONE flag. Do not clear AC.

Clear DONE and Intensify (DIXY)

Octal Code: 6055

Operation: Clear DONE flag, intensify, set DONE flag.

Load Enable Register (DILE) (see Table 4-7)

Octal Code: 6056

Operation: Load Enable Register, clear the AC.

Transfer Enable Register to AC (DIRE)

Octal Code: 6057

Operation: Transfer contents of Enable Register to the AC.

Table 4-7
Point-Plot Display Control Enable/Status Register

Bit Position	Signal Name	Operation
0	DONE Flag	Set (DONE = 1) to indicate data point has been intensified.
6	Write Through	When set to a (1) causes the 611 or 613 to go into a write through mode.
7	Store	When set to a (1) causes the 611 or 613 to go into a store mode. When equal to a (0) causes the 611 or 613 to go into a non-store mode.
8	Erase	When set to a (1) will cause the 611 or 613 to initiate an erase cycle.
9	Color	When color is set to a (1), the controller is in a red mode. When color is set to a (0) the controller is in a green mode.
10	CHANNEL	When CHANNEL SELECT is set (1), channel 2 is selected; when it is cleared (0), channel 1 is selected.
11	INTERRUPT ENABLE Flag	When INTERRUPT ENABLE flag is set (1), an INTERRUPT can be generated to intensify the display, after the display settles.

NOTE: Bits 1–5 are not used by the Enable/Status Register.

4.4.1 Functional Block Diagram Description

The primary logic functions are indicated by the blocks in Figure 4-32. The Device Select logic ensures that the processor is communicating with the display control, and not some other device. It receives bits MD3–MD8, decodes them, and when a 605X is decoded, sends SELECT L to the Operation Decoder so that it can process bits MD9–MD11 to determine the operation to be performed. The I/O PAUSE signal is used as a gating input to ensure that the instruction is an IOT instruction. I/O PAUSE is generated 150 ns after TP1 of all IOT instructions. (See the *PDP-8/E Maintenance Manual* for more information on IOTs.)

The Operation Decoder begins to function when the Device Select logic asserts INTERNAL I/O L. The Operation Decoder looks at bits MD9–MD11 and determines what type of instruction is to be performed. The Operation Decoder then enables the necessary blocks to perform the instruction. If the instruction is to Load X Register (DILX), the Operation Decoder will cause LOAD ENABLE and LOAD X to be generated; the X-axis data will then be loaded into the X Holding Register from the AC. If the instruction is Load Y Register (DILY), the de-

coder will generate LOAD ENABLE and LOAD Y to allow the contents of the AC to be loaded in the Y Holding Register. The instructions will also set up C0 and C1 to transfer data from the AC to the Holding Registers. The input data gate (see Figure 4-32) is used to transfer X- and Y-axis data from the Data Bus to the X- and Y-axis Holding Registers. The DIXY and DILY instructions are used to generate LOAD ENABLE and to enable the gates to load the X- and Y-axis Buffer Registers (see Paragraph 4.2.6).

The Buffer Register is a 74193 IC with its control input pulled high at all times by +5V through a resistor. When the Buffer Register is loaded, the 12 bits of data will be applied immediately to the analog switches because the control input is always high.

The analog switches are in series with the input to the summing amplifier. Switches that are turned on will supply current to the summing amplifier. Each bit will be applied to its respective analog switch and will turn on, or cut off, the switch in that position. A logic 0 (high) in the AC will cause current to be supplied to the summing amplifier input by the weighted resistor; a logic 1 in the AC will cause the current to flow to ground through a transistor. The sum of the current supplied to the node (summing amplifier input) will produce an output from the summing amplifier proportional to the digital input. The summing amplifier will supply ±5 Vdc to the line drivers which act as boosters to drive the deflection circuits in the oscilloscope.

The DIXY instruction will be delayed, and after the X and Y Registers have been loaded, the DIXY instruction will be used to intensify the dot on the array to display the X- and Y-axis data. The Operation Decoder will decode this instruction, and when TP3 is generated, the intensity pulse will be generated by a one-shot and be applied to the display circuits. The intensity pulse will be delayed 6 μs for the Tektronix 602, 100 μs for the 611 or 613, 21 μs for the VR14, 21 μs for green and 16 μs for red for a VR20. The delay and pulse polarity are selected by SW1 and SW2 on the M869 module. The delay allows the deflection circuits in the oscilloscope to settle before intensifying the oscilloscope. The delay switch, marked LONG and SHORT, will be set to LONG for the VR14, VR20, 611 and 613 and to SHORT for the Tektronix 602. The Z-axis switch, marked + and –, will be set to + for the 602, 611, 613 and – for the VR14, and VR20. The positive and negative reference voltages are applied to the node and switches to supply a constant current source.

The Channel Select logic is used to select a channel on the oscilloscope for data display. The DILE instruction will be decoded, and if data-bit 10 is a 1, the CHANNEL SELECT flip-flop will set and select channel 2. If the flip-flop is not set, the data will be displayed on channel 1.

An Interrupt will be generated by setting the DONE flag if the INTERRUPT ENABLE flip-flop is set. The DISD instruction will generate a Skip after the display has been performed if an Interrupt is not used. Interrupts are used if it is necessary to use all available time for performance of an instruction. If an INTERRUPT ENABLE is set, the processor can perform instructions while waiting for a DONE flag.

The Enable/Status Register contains INTERRUPT ENABLE, the DONE flag, and a CHANNEL SELECT flip-flop, color flip-flop, erase, store, and write through. The INTERRUPT ENABLE flip-flop can be set by transferring a 1 in bit position 11 from the AC, using the DILE instruction. Channel 2 is selected by transferring a 1 in bit position 10, a 0 will select channel 1; color (red) can be selected by transferring a 1 in bit position 9, a 0 will select green; a bit in position 8 will select an erase; a 1 in bit position 7 will select a store mode, 0 will select a non-store mode; a 1 in bit position 6 will select a write through. The status of the DONE flip-flop (set = 1) can be checked using the DIRE instruction to transfer bit position 0 to the AC for checking. The DIRE instruction also transfers bits 6, 7, 9, 10, and 11 to the AC to show the channel selected, the status of the INTERRUPT ENABLE flip-flop, and the status of the color, store, and write through flip-flop.

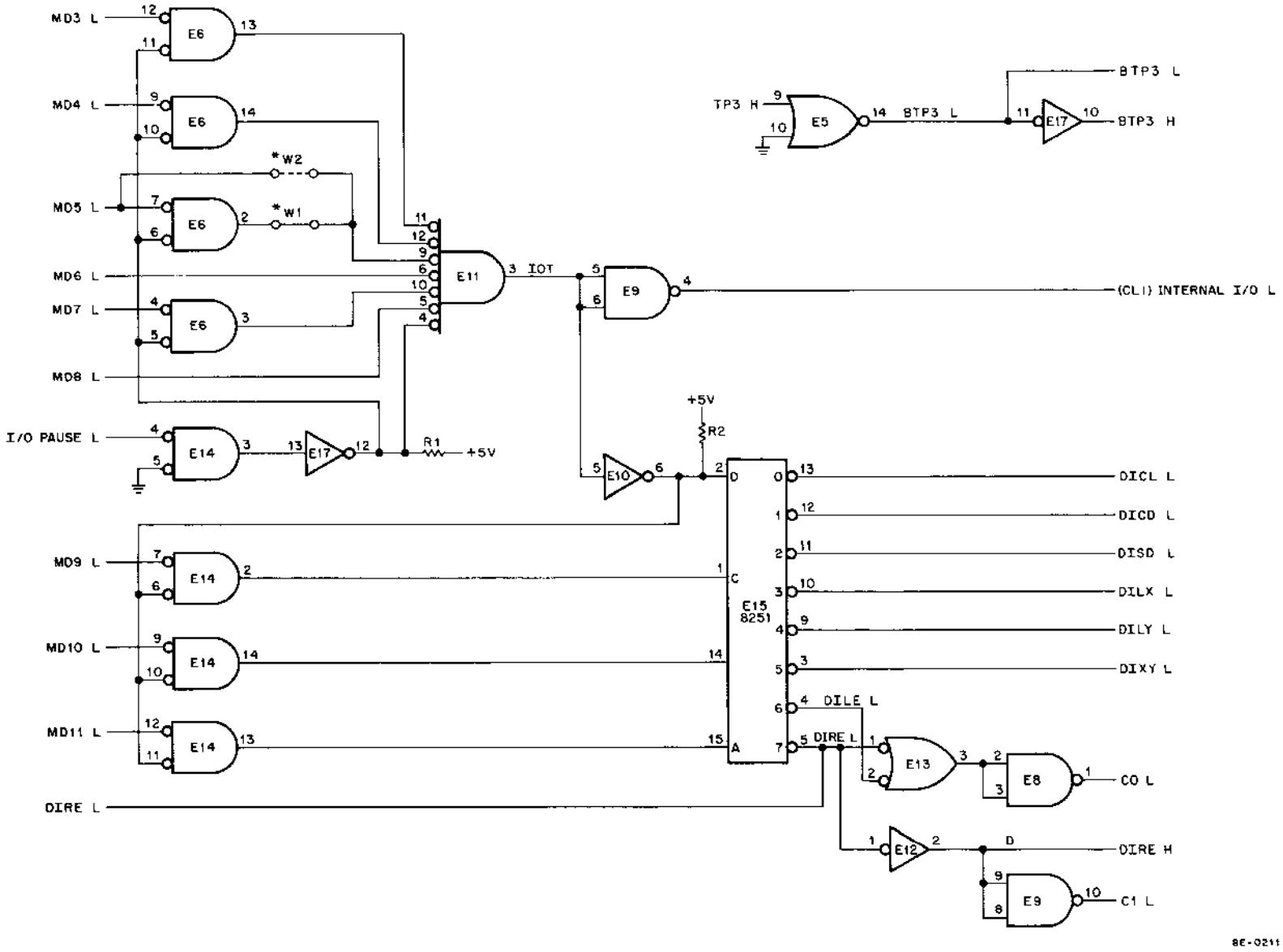


Figure 4-36 Device and Operation Select Logic

4.4.2 Point-Plot Display Control Detailed Logic

4.4.2.1 Device and Operation Select Logic — The Device and Operation Select logic (see Figure 4-36) decodes MD03—MD11 and selects the device and type of operation that will be performed. MD3—MD8 are gated for each MD Line by I/O PAUSE. An internal I/O PAUSE signal is generated in the timing generator whenever MD bits 0—8 are decoded as a 65 (octal). The 8251 IC is a BCD-to-Decimal Decoder that will provide low outputs on one line; e.g., MD9—MD11 is 011. Pin 3 will have a low output, indicating that this is a 6053 (DILX) instruction. The truth tables, logic diagrams, and pin locator for the 8251 IC are in Appendix A of the *PDP-8/E Maintenance Manual.* The output of the Operation Select logic will provide signals to enable Interrupt logic, select the C lines, allow loading of the X and Y Registers, generate a Z-axis pulse, and clear the logic after the data is displayed.

C1 and C0 control the direction of data flow between the AC and the Data Bus. C0 and C1 should be high for data to be transferred from the AC to the Data Bus; they are not asserted for a DILX or DILY instruction. A DILE instruction will assert C0 to transfer data from the AC to the Enable Register and then clear the AC. The DIRE will assert both C0 and C1 to JAM-transfer the contents of the Enable/Status Register to the AC.

Timing Pulse 3 logic is shown with the Device and Operation Select logic in Figure 3-36. The logic will generate a high and low output to enable various gates for DILY and DILX instructions in the Point-Plot Display Control logic during EXECUTE.

4.4.2.2 Enable/Status Register — The Enable/Status Register consists of the CHANNEL SELECT, COLOR SELECT, ERASE, STORE, WRITE THROUGH, INTERRUPT ENABLE, and DONE flip-flops (see Figures 4-37 and 4-38). The Enable/Status Register will provide signals to enable the interrupt system, select a channel in the oscilloscope for displaying data, select color, store, write through, produce an erase cycle, and provide status bits to be transferred to the AC.

4.4.2.2.1 DONE Logic — The DONE flip-flop on the M869 module is used to indicate the completion of the display and to generate an Interrupt if the INTERRUPT ENABLE flag is set (1) (see Figure 4-39).

DONE can be cleared by any of the inputs to pins 1, 4, 2, or 5 of E2. INITIALIZE or CLEAR H, applied to pin 1, will be applied to the clear side of DONE and will clear the flip-flop. The DICD and DIXY instructions applied to pins 4 and 2 will clear the DONE flip-flop. When changing color or generating an erase, the done flag will be cleared by CLEAR DONE L on E 19 Pin 11. The DIXY instruction is used to clear DONE to ensure that it will not be set before the LOAD DELAY signal is applied to the clock input. LOAD ENABLE, which is pulled low by DILX or DILY, is present at pin 8 of E16, or pin 13 of E13. DONE will be cleared by the load instructions to ensure that it is not set until the LOAD DELAY signal is applied to the set input.

DONE will be set by LOAD DELAY, which is generated by LOAD ENABLE and TP3. LOAD DELAY will be delayed 21 μs for the VR14; 16 μs in red, 21 μs in green for the VR20; 100 μs for the 611, 613; and 6 μs for the Tektronix 602. SW2 will select the delay time by selecting C24 or C20 in the LOAD DELAY network. SW2 will be set to the LONG position for the VR14, and to the SHORT position for the Tektronix 602. When the VR14, or VR20, 611, 613, or Tektronix 602 are not used, the user should refer to the handbook for the oscilloscope being used and see Paragraph 3.2 for information on interfacing an oscilloscope with the VC8-E. A JUMPER is provided to select either VR14, VR20 delay or 611, 613 delay (refer to E-CS-M869-0-1).

When LOAD DELAY is applied to pin 3 (clock), DONE will set and apply a 1 to E8 and E9. If INTERRUPT ENABLE is set (see Figure 4-39), an Interrupt will be generated. DONE will also enable E9 pin 3 to allow a skip if the DISD instruction is performed. If the DIRE instruction is performed and DONE is set, DATA 0 will be gated to the Data Bus to indicate the status of the DONE flag. A high will be transferred to the Data Bus, if DONE is not set, when the DIRE instruction is executed.

LOAD X, LOAD Y, and LOAD ENABLE will be used to load the X- and Y-axis Holding Registers in the M885 module.

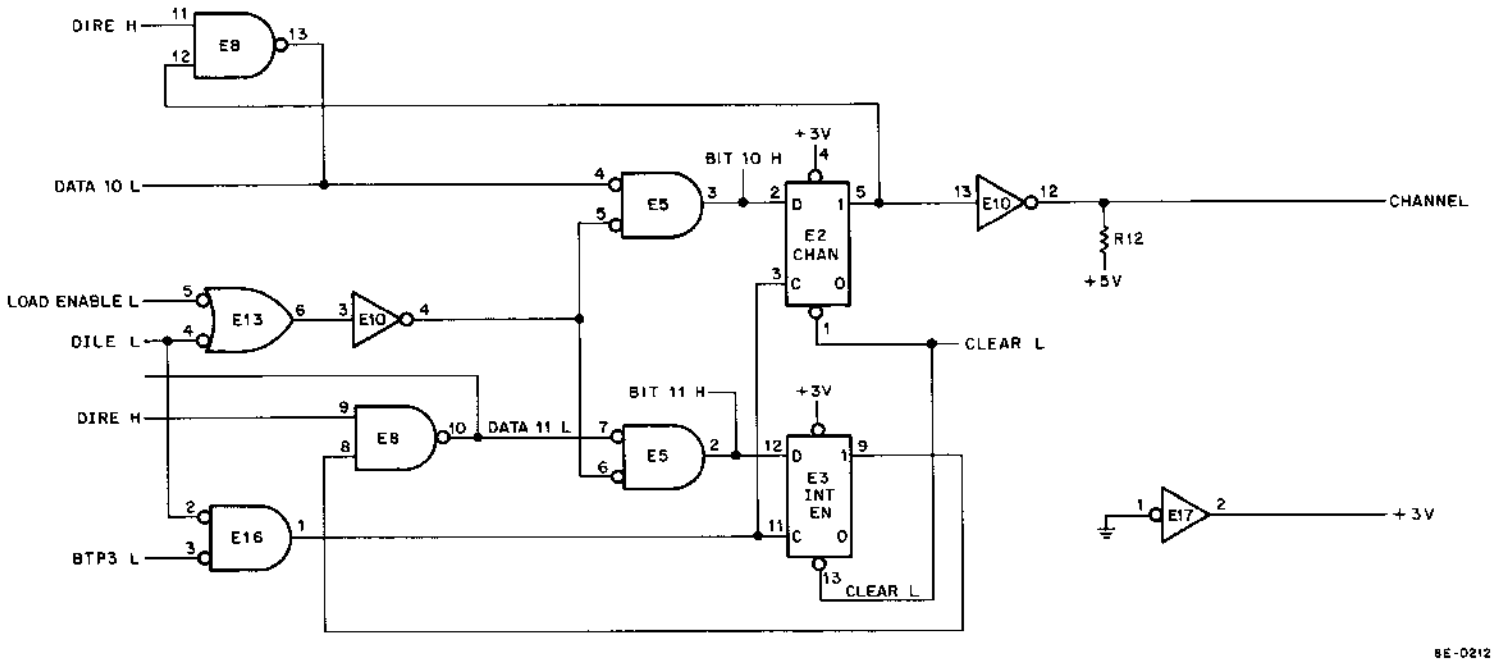


Figure 4-37 Enable/Status Register

4.4.2.2.2 INTERRUPT ENABLE Logic – INTERRUPT ENABLE is used to enable the Interrupt logic shown in Figure 4-39. INTERRUPT ENABLE E3 will be cleared by CLEAR L from the programmer's console, or by the DILE instruction ANDed with TP3 at E16 if DATA 11 is low. When DATA 11 is high, the INTERRUPT ENABLE flag will set. DATA 11 is transferred to the M869 module by the DILE instruction (see Figure 4-37). DIRE on pin 9 of E8 will enable E8 and will allow the set side of E3 to be applied to the Data Bus. The set side of E3 will be transferred to the AC by a DIRE instruction to indicate the status of the INTERRUPT ENABLE flag.

4.4.2.2.3 CHANNEL SELECT Logic – The CHANNEL SELECT flip-flop E2 will be used to select one channel on the oscilloscope for display of data (see Figure 4-37). DATA 10 is transferred from the AC by a DILE instruction to set E2 if bit 10 is low, or clear E2 if bit 10 is high. DILE out of E13 and E10 will enable E5. If DATA 10 is low, E2 will set and select channel 2. If DATA 10 is high, the data input to E2 will be low and the clock input from E16 will clear E2 to select channel 1. The set side of E2 is tied to pin 12 of E8 and the DIRE instruction will enable E8. When E2 is set, a low (1) will be transferred to the AC to indicate channel 2 is selected. When E2 is cleared, DATA 10 will be high (0), and will indicate channel 1 is selected when DIRE is executed.

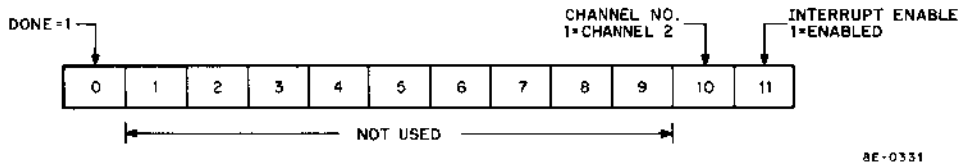


Figure 4-38 Enable/Status Register Word Contents

4.4.2.3 INTENSITY PULSE GENERATION – The intensity pulse for the system is generated when a DIXY instruction is fed to the control module. It will be gated by TP3H and applied to a 2 μs one-shot or a 6 μs one-shot. When color (0) H is low and non-store is high, this will reverse bias D1 and switch in R18. The time will be determined by R18 and C40 and will produce the 6 μs intensity pulse. When non-store (H) is high and color (0) H to high, this will forward bias D1 and put R18 in parallel with R17. The time will then be determined by R18 in parallel with R17 and C40, and produce a 2 μs intensity pulse. The delayed output will feed to the Polarity Select switch. The intensity pulse is applied to an amplifier in the M885 module for pulse shaping and amplification. The amplitude of the pulse can be changed by the A–B jumper to select R58 or R59. With the jumper installed as shown by the dotted lines in Figure 4-40, the pulse will be +4V to –2V. If the jumper is removed and placed between the other two split lugs, the pulse will be +4V to –10V. The jumpers will change the amplitude of the voltage, but the polarity will be determined by the position of SW1 in the M869 module.

4.4.2.4 Data Gates – The Data Gates (see Figure 4-41) receive their inputs from the Data Bus when the DILX or DILY instruction is executed. LOAD ENABLE, also generated by these instructions (see Figure 4-39), will enable the Data Gates to apply the 10 bits to the X and Y Holding Registers. Data Gates for bits 02–09 are located in the M885 module; the gates for bits 10–11 are located in the M869 module. Bits 10 and 11 are applied to the Holding Register through the H851 Edge Connector.

4.4.2.5 Holding Registers – The X- and Y-axis Holding Registers (see Figure 4-42) will receive inputs from the Data Gates when the DILY and DILX instructions are executed, and will provide outputs to the analog switches. The Holding Registers consist of three 74193 ICs for each axis. (See Appendix A for the logic diagram and pin locations of the 74193 IC.) Figure 4-42 shows only the X Holding Register, but the Y Holding Register is identical. The LOAD X or LOAD Y generated by DILX or DILY (see Figure 4-38) will enable gates in the IC to load bits 02–11 into the Holding Register. The output of the Holding Register will be applied to the analog switches (see Figure 4-43).

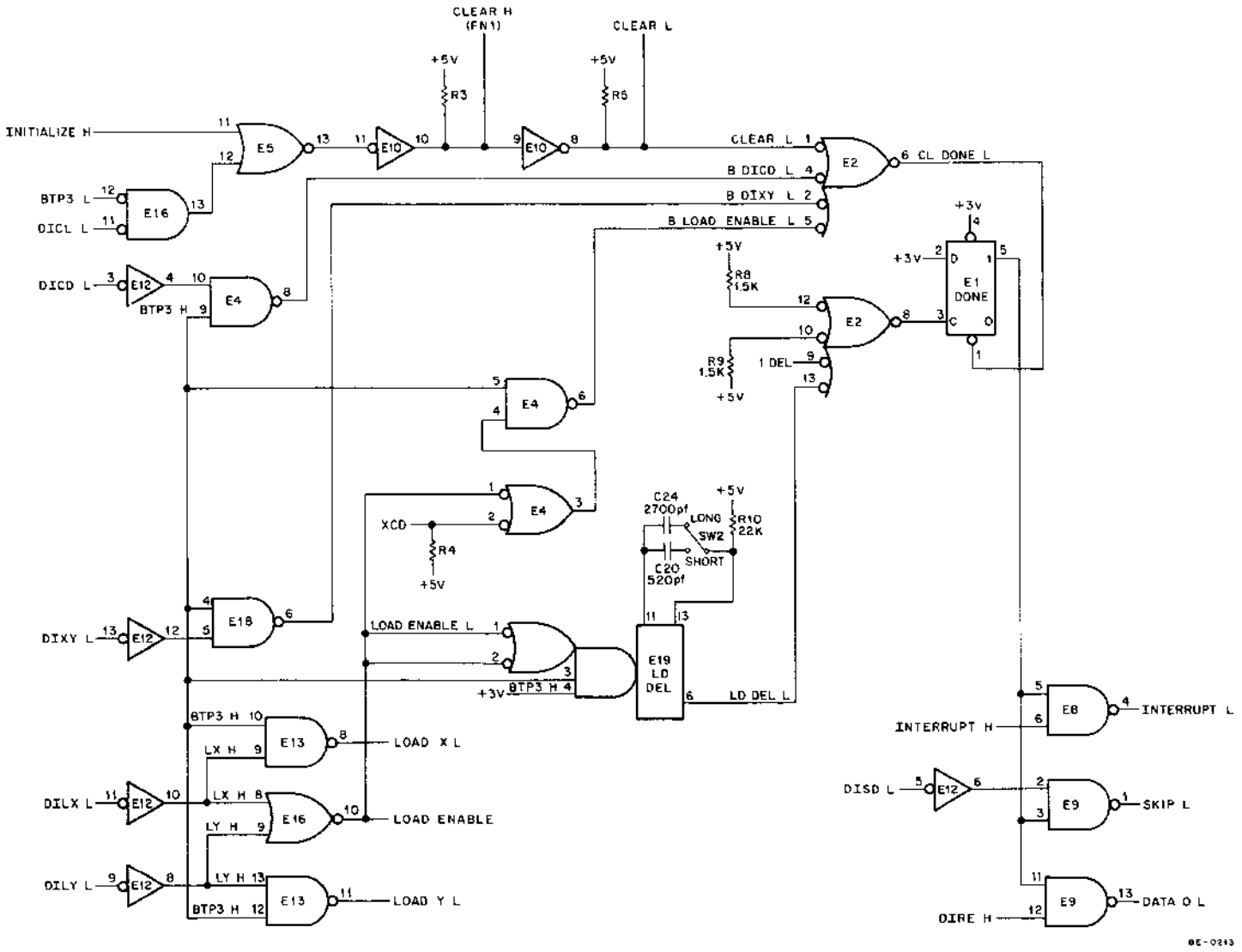


Figure 4-39 DONE and Interrupt Logic

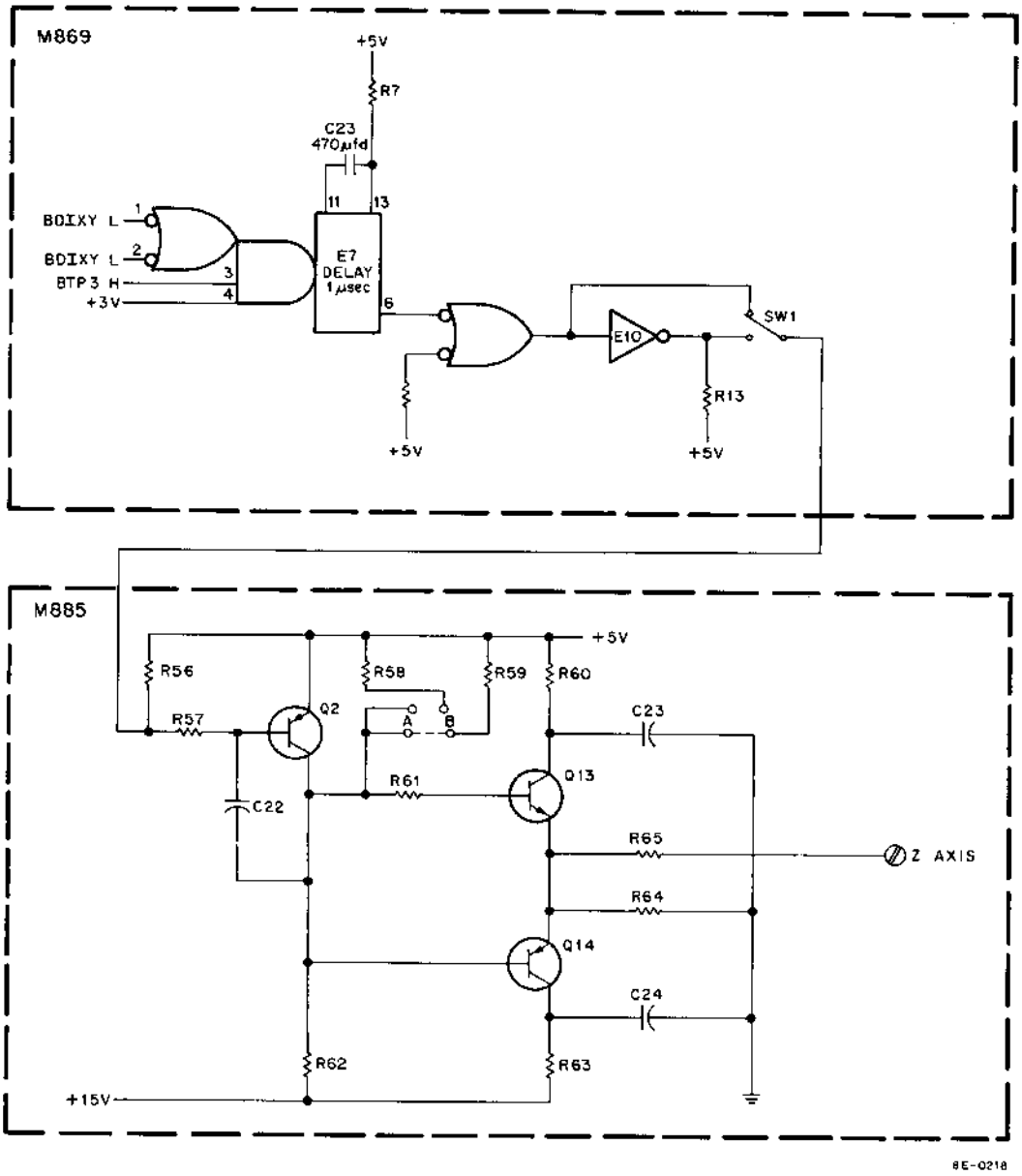


Figure 4-40 Intensity Pulse Logic

4.4.2.6 Analog Switches and Summing Amplifier – The analog switches, weighted resistors, and summing amplifier will receive 10 digital bits as input and will supply a ±5 Vdc output (see Figure 4-43). The digital input will turn on or cut off the switches which supply current to the summing junction. The summing junction is tied to the input of E17. The sum of the currents supplied by the analog switches will produce a voltage on the output of the summing amplifier which is proportional to the contents of the Holding Register.

The analog switches (see bit 11 in Figure 4-43) supply current from the +5V reference to the summing junction through D3 when a low input is applied to the base of Q1. The current supplied will be determined by the resistance of the weighted resistor R99. The current produced by turning off Q1 and allowing D31 to conduct will be approximately 5V/Rw; Rw being the value of R99. D30 and D33 are added to the least-significant bit positions to isolate the transistor capacitance from the summing junction. When a high input (1) is applied to Q1, the transistor will cut off D30 and all the current will flow through the transistor to ground.

The negative reference is used as a constant current source for the summing junction. Q17, Q18, and the Zener diodes in the negative reference will supply a constant current. R88 will adjust the output of the negative reference to allow the summing amplifier to span the full range of voltages for the ±0777 octal input to the analog switches. The negative reference offsets the amplifier output by +5V.

The E17 summing amplifier is a feed-back amplifier that tries to seek the same voltage on both inputs. The current supplied by the analog switches and weighted resistors will flow through the feed-back resistor. The output will adjust in a negative direction to drop the amount of voltage necessary to satisfy Ohm's law (V=IR). Q29 and Q30 are boosters that drive the oscilloscope circuitry.

4.4.2.7 Positive Reference Source – The +5V reference is used by the analog switches to supply a constant current to the summing junction (see Figure 4-44). E14 and E15 are adjusted to maintain a constant output current The output will be adjusted to 5.12V ±5 mV and the amplifiers will maintain this level as current requirements change.

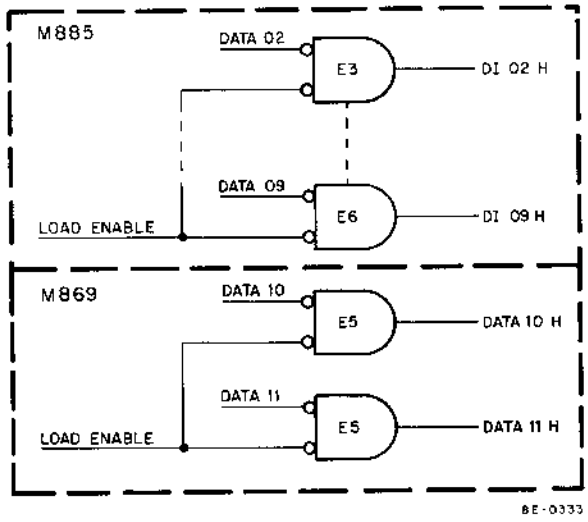


Figure 4-41 Data Gates

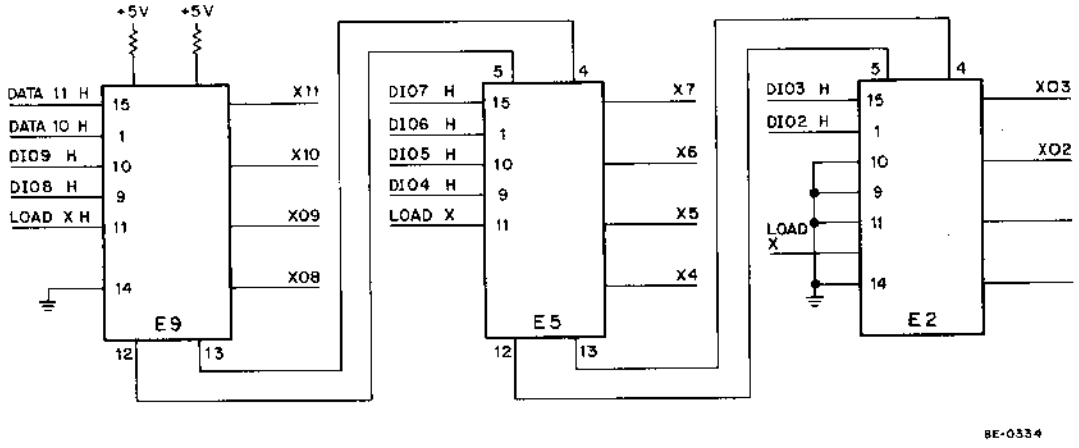


Figure 4-42 X-Axis Holding Register

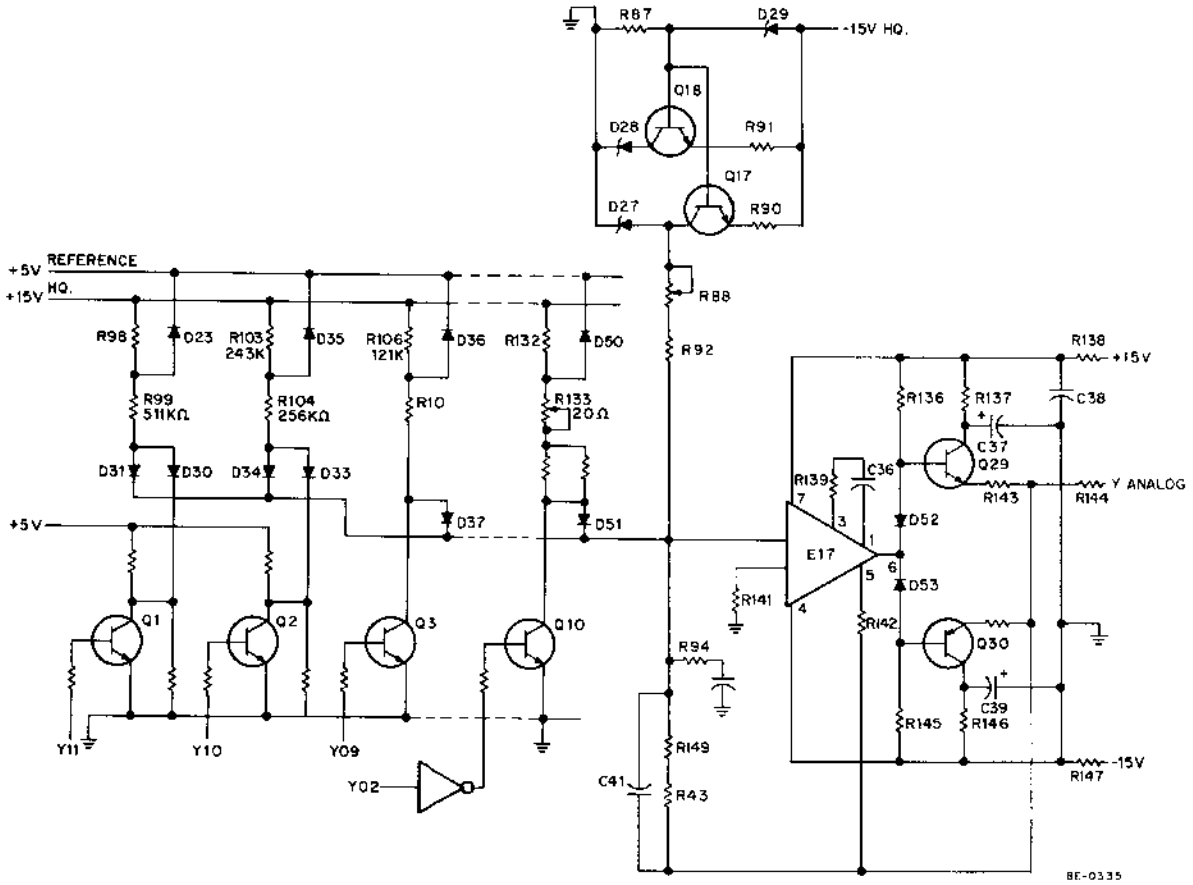


Figure 4-43 Analog Switches and Summing Amplifier

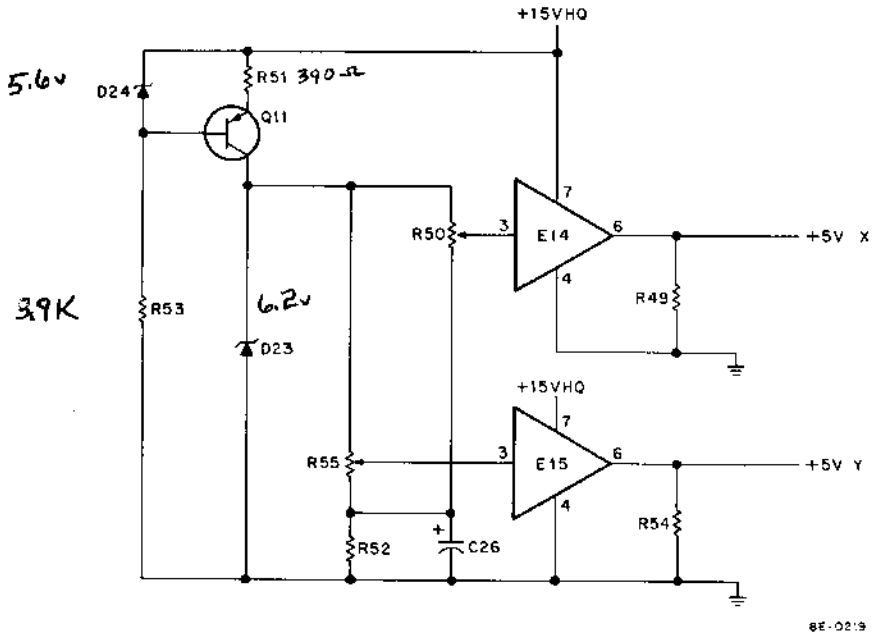


Figure 4-44 +5V Reference

SECTION 5
BUFFERED DIGITAL I/O (DR8-EA)

4.5 INTRODUCTION

The DR8-EA 12-channel Buffered Digital I/O provides 12 digital inputs and 12 digital outputs. The DR8-EA is contained on one M863 quad module inserted into the OMNIBUS. The M863 module consists of an Input Register, Output Register, AC Bus Register, and control logic. The Input Register will receive 12 bits of data from the outside world or from the AC, with instructions. The Output Register will receive data from the AC and supply 12 bits of data to the outside world. The contents of the Output Register may be transferred to the AC or cleared by 1's from the AC. The AC Bus Register will select the contents of the Input or Output Register for transfer to the AC. Inputs and outputs are TTL compatible (low true), giving the user the option of providing level converters or signal conditioners. Each input may monitor an external line directly, or may sense the occurence of a negative-going transition. Skip and Interrupt capabilities are provided for the Input Register when the IN flag is asserted. Up to eight DR8-EA modules can be utilized in one system, but if an AD8-EA is installed, only seven DR8-EA modules can be used. The DR8-EA is connected to the outside world by a DR8-EB panel, one for each module, or two BC08J cables tied to the J1 input and the J2 output on the M863 module. The DR8-EB panel has two M904 modules for connecting user cables to the panel.

4.5.1 Buffered Digital I/O Functional Block Diagram

The basic module is divided into two sections: 12-bit digital inputs and 12-bit digital outputs (see Figure 4-45). The 12-bit digital Input Register consists of 12 flip-flops and associated circuitry. Each flip-flop can be cleared by an IOT instruction (DBCI) in which the AC clears the respective bits in this register. INITIALIZE will clear all flip-flops. Each flip-flop can be set independently by a signal from the outside world. Jumpers can be used to select either the flip-flop output, or go directly to the Buffer OMNIBUS. Each jumpered bit can be read (DBRI) into the AC. All jumpered bits are ORed together to form a Skip condition if pulled by the computer (DBSK), or to cause a Program Interrupt if Interrupts are enabled (DBEI) and jumpers are installed to assert the IN flag.

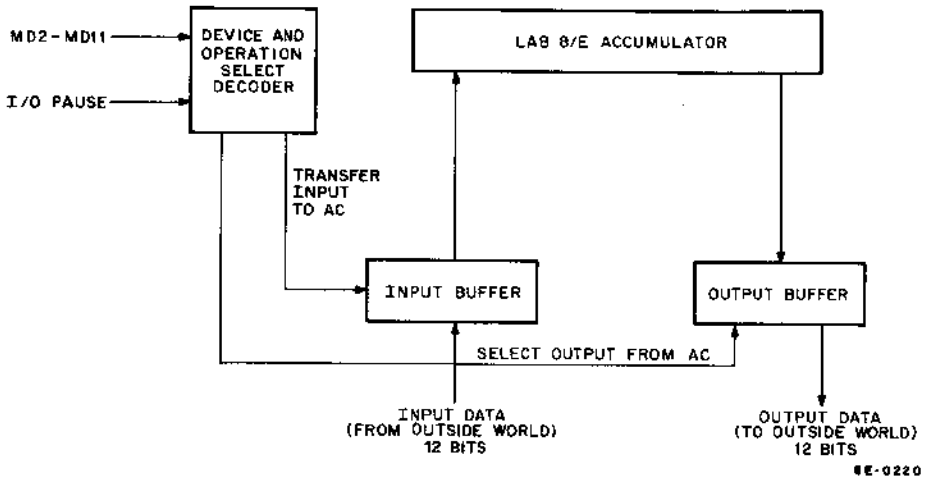


Figure 4-45 Buffered Digital I/O Block Diagram

The 12-bit digital output flip-flops can be set, each bit independently, by the DBSO instruction and respective 1's in the AC. The DBCO instruction clears the respective flip-flops in the AC; INITIALIZE will clear all flip-flops.

Jumpers are provided so that the device code 5X can be used, where X is 0 through 7, allowing use of eight DR8-EAs if an AD8-EA is not used. When the AD8-EA is installed, octal code 53 is illegal; therefore, only seven DR8-EA modules can be used.

When an IOT cycle using a 65XX octal code is selected, the instruction will be decoded by the Operation Select logic and will allow data to be transferred from the outside world to the AC, or from the AC to the outside world. Programmed instructions can also clear the Input or Output Buffers when the DBCO or DBSO instructions are executed.

The following programmed instructions are decoded by the Operation Decoder and used to perform operations in the Buffered Digital I/O:

Disable Interrupts (DBDI)

Octal Code: 65X0 ($X_8 0_8$ through 7_8, dependent on jumper)

Operation: Disables all Interrupts.

Enable Interrupts (DBEI)

Octal Code: 65X1

Operation: Enables Interrupts.

Skip on INPUT Flag (DBSK)

Octal Code: 65X2

Operation: Skip on INPUT flag.

AC Clear Input Register (DBCI)

Octal Code: 65X3

Operation: 1's in AC clear respective bits in Input Register.

Transfer Contents of Input Register to the AC (DBRI)

Octal Code: 65X4

Operation: The contents of the Input Register are transferred to the AC.

Clear Output Register (DBCO)

Octal Code: 65X5

Operation: 1's in AC clear respective bits in Output Register.

AC Set Output Register (DBSO)

Octal Code: 65X6

Operation: 1's in AC set respective 1's in Output Register.

Transfer Output to AC (DBRO)

Octal Code: 65X7

Operation: Transfer contents of the Output Register to the AC.

4.5.2 Buffered Digital I/O Detailed Logic

The detailed logic of the Buffered Digital I/O is divided into the following functional groups for purposes of discussion:

a. Device Select and Operation Decoder

b. Interrupt and Skip Logic

c. Input and Output Registers

4.5.2.1 Device Select and Operation Decoder – The Device Select logic in Figure 4-46 will have bits MD3L–MD11 and I/O PAUSE as inputs. I/O PAUSE will be generated 150 ns after TP1 of any IOT cycle. In the Buffered Digital I/O, it will enable the AND gates to allow decoding of MD3L–MD8L. When these gates are enabled and a 6X octal code is present, a SELECT H and INTERNAL I/O are generated. SELECT H will be used to enable the Operation Decoder.

The device code can be changed by changing jumpers in the Device Select logic. Table 4-8 shows the jumper combination required for each code. Octal 50 is the normal configuration and the unit comes from the factory with this code selected.

The Operation Select logic will receive bits MD9L–MD11L. When SELECT H is present, these bits will be gated to the Operation Decoder, which is a BCD-to-Decimal Decoder. The logic diagram, the truth table, and pin locations are shown in Appendix A of the *PDP-8/E Maintenance Manual.*

The 3-bit input to the BCD-to-Decimal Decoder will qualify one gate and produce one low output; all other gates will be disqualified. As an example, 011 on the input would enable gate 3, pull line 3 low, and allow the DBCI instruction to be executed.

Table 4-8
IOT Device Code

Octal Code	Jumper		
50	6H	7H	8H
51	6H	7H	8L
52	6H	7L	8H
*53	6H	7L	8L
54	6L	7H	8H
55	6L	7H	8L
56	6L	7L	8H
57	6L	7L	8L

*Device Code 53 cannot be used if the AD8-EA is installed.

4.5.2.2 Interrupt and Skip Logic – The Interrupt and Skip logic (see Figure 4-47) is used to generate a Skip or an Interrupt request when the IN flag is asserted, indicating that data has been transferred to the DR8-EA Input Register. To generate an Interrupt request, DBEI must be executed to set INTERRUPT ENABLE E9. The DBEI instruction is ANDed with TP3 and applied to the set input of E9 to set INTERRUPT ENABLE. If INTERRUPT ENABLE is set, the IN flag applied to E48 will generate an Interrupt request and a subroutine may be performed to transfer the contents of the Input Register to the AC. INTERRUPT ENABLE is cleared by the execution of the DBDI instruction or by INITIALIZE.

The DBSK instruction will be ANDed with the IN flag to generate a Skip if the DBSK instruction is programmed. Note that the IN flag is pulled low by data inputs when the proper jumpers are installed in the Input Register (see Figure 4-48).

C-line Select logic (see Figure 4-47) is used to control the direction of data flow between the registers and the AC. DBRI will assert C0 and C1 to allow the contents of the Input Register to be transferred to the AC. DBRO will assert C0 and C1 to allow the contents of the Output Register to be transferred to the AC.

4.5.2.3 Input Register and Control Logic – The Input Register (see Figure 4-48) receives inputs from the outside world at J1. Inputs from J1 will be applied through an inverter to the clock input of the flip-flop in the Input Register. The data input is high at all times; therefore, a 1 applied to the clock input will set the flip-flop. The output of the Input Register is taken from the set side and applied to a group of split lugs that can be jumpered.

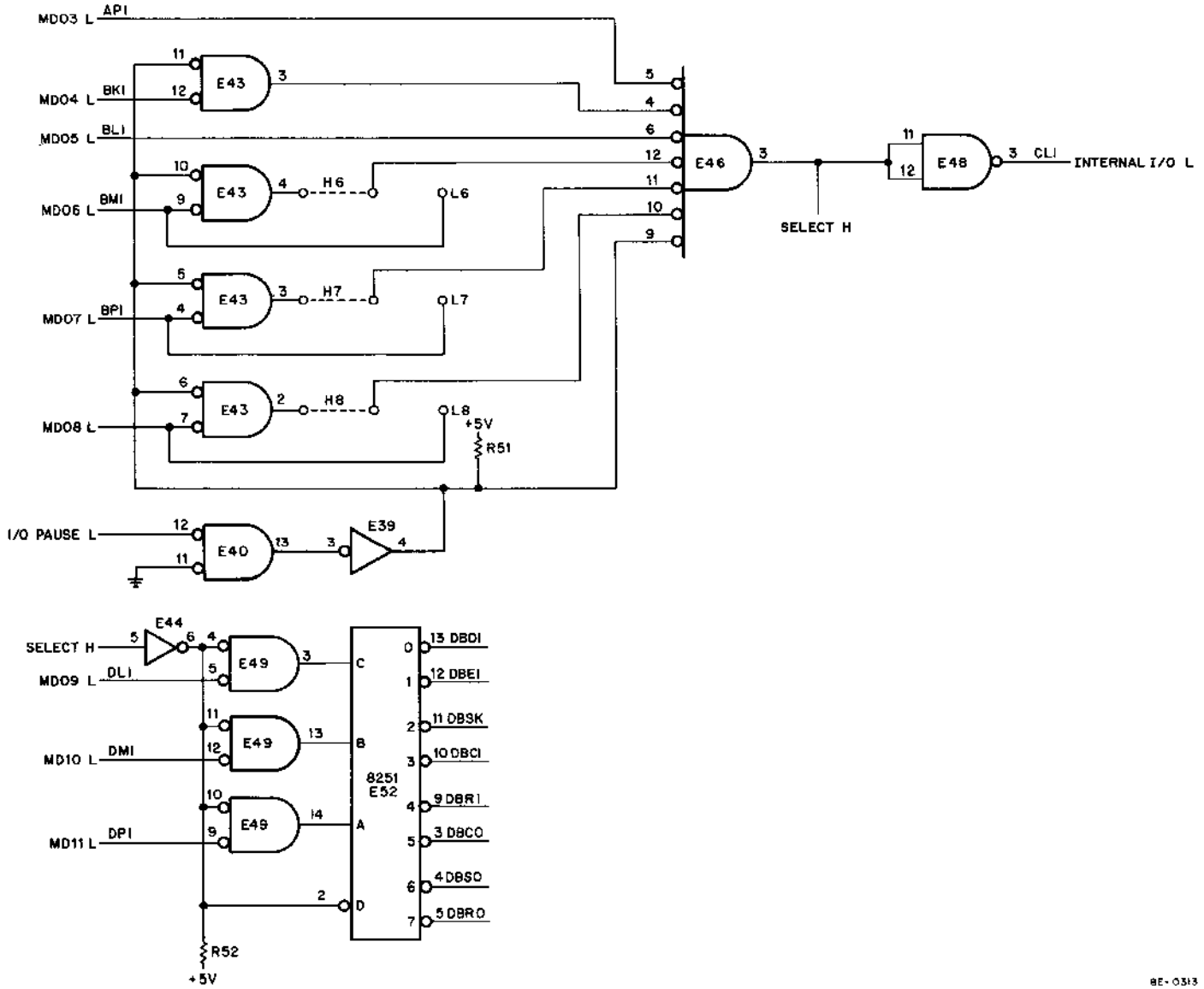


Figure 4-46 Device Select and Operation Decoder Logic

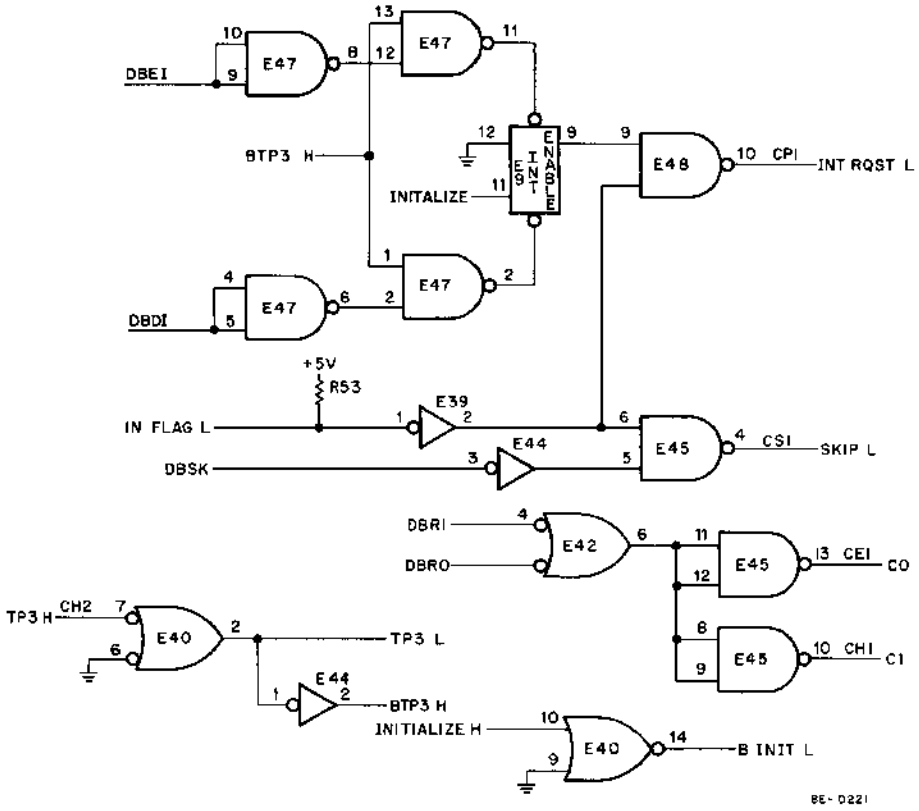


Figure 4-47 Interrupt and Skip Logic

The output of inverter E2 is also applied to the split lugs. The jumpers can select the high input from the inverter or from the set side of the flip-flop and apply it to the AC Bus Register. The set side of the flip-flop can also be jumpered to an inverter (see E8 in Figure 4-48) to assert the IN flag. The IN flag will generate an Interrupt request if it is asserted and INTERRUPT ENABLE has been set by the DBEI instruction.

The Input Register can be cleared by 1's from the AC when a DBCI instruction is performed. To clear a flip-flop, there must be a 1 input to an AND which is enabled by the DBCI instruction (see E3 Figure 4-46). Inverter E1, which has its output tied to E3, will receive B00 H from the Data Bus. The contents of the AC (see Figure 4-48) will be applied to AND gates (see E6 in Figure 4-48); the gates will be enabled by SELECT H which is present on any instruction to the DR8-EA. The outputs of the AND gates (B00 H—B11 H) will be applied to the gates enabled by the DBCI instruction (see Figure 4-48). The DBCI and the output of E1 will enable E3 and be applied to E2. The output of E2 is tied to the clear side of the flip-flop; a 1 will clear this bit. The Input Register will also be cleared if CLEAR or INITIALIZE are applied to E2.

4.5.2.4 Output Register and Control Logic — The Output Register (see Figure 4-49) receives inputs from the AC and applies them to the outside world. The Output Register can be cleared by 1's in the AC and the contents transferred to the AC.

To set the Output Register flip-flops with 1's from the AC, the data bits tied to E6 (see Figure 4-49) will be gated to E5 by SELECT H. Note that data bits 03L — 11L are tied to identical gates and only bit 00 will be discussed. E5 will be enabled by the DBSO instruction from E2 and the data input (1) will set the E16 flip-flop. The set side of E16 is applied to inverter E14, and then to J1 which is connected to the outside world. The DBCO instruction and TP3 will enable gate E7 and a 1 from the AC (data 00 — data 11) will be applied to the clear side of E16 to clear it.

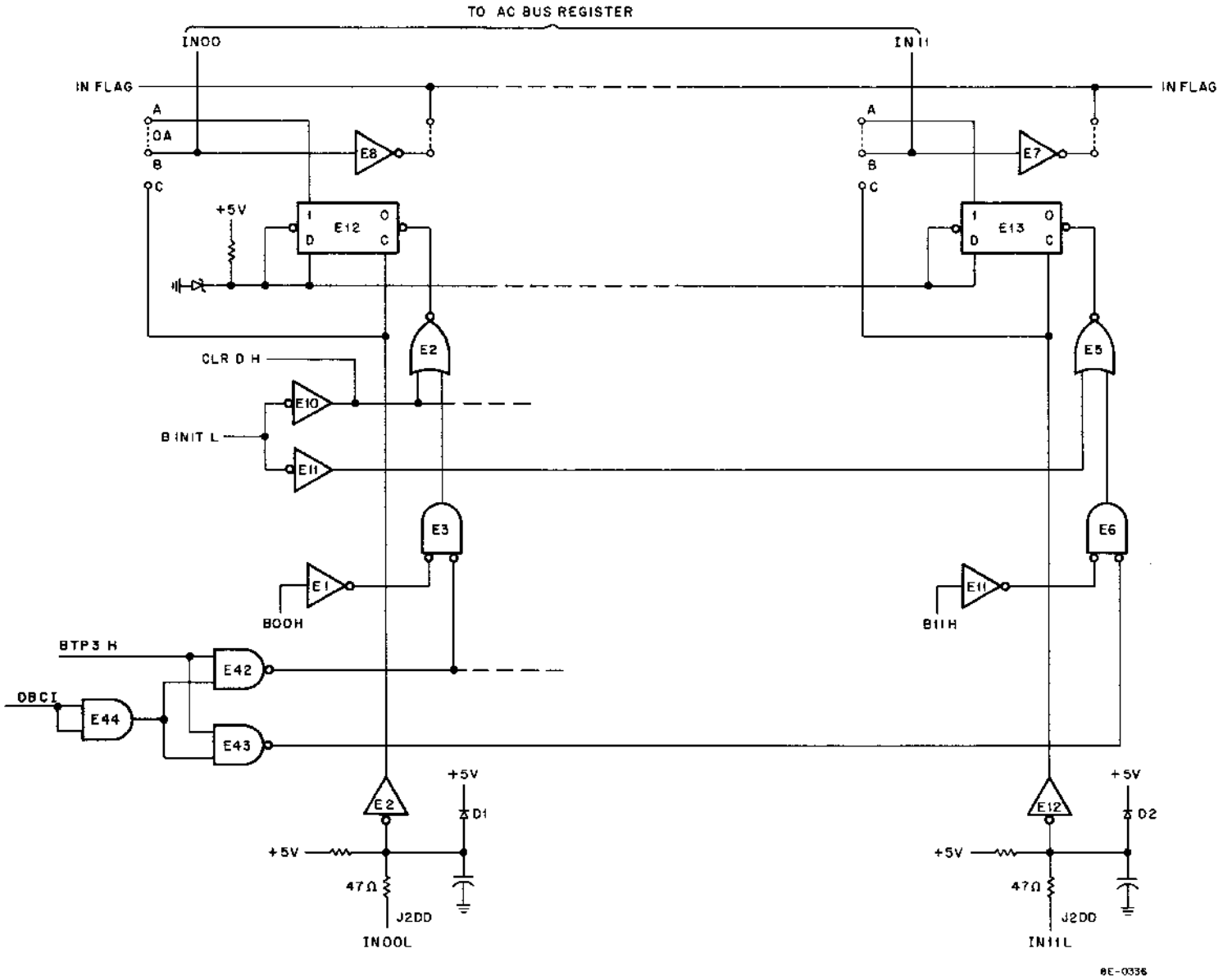


Figure 4-48 Input Buffer Register and Logic

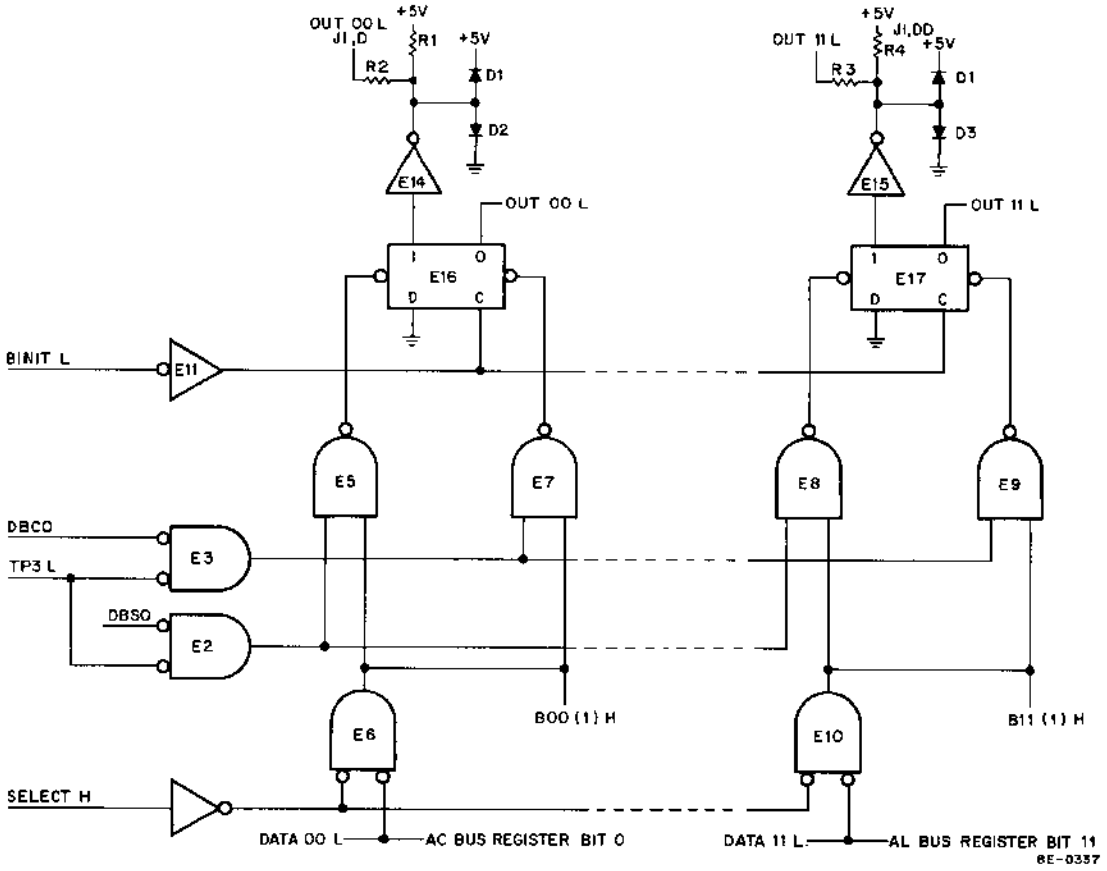


Figure 4-49 Output Register and Logic

The clear sides of the flip-flops in the Output Register are applied to the AC Bus Register (see Figure 4-50) for transfer to the AC when a DBRO instruction is performed. INITIALIZE will clear all flip-flops in the Output Register as it is tied to the clock input and the data input is grounded. A high on the clock input from the inverter will clear the flip-flop if the data input is low.

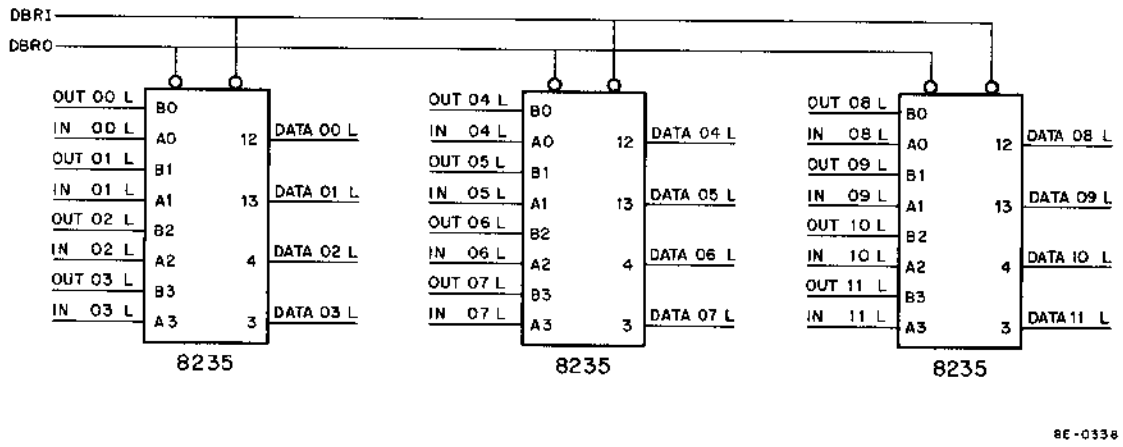


Figure 4-50 AC Bus Register

4.5.2.5 AC Bus Register – The AC Bus Register (see Figure 4-50) will have OUT 00 L – OUT 11 L and IN 00 L – IN 11 L applied to it from the Output and Input Registers. The AC Bus Register will select the contents of either the Output or Input Register to be applied to the Data Bus for transfer to, or from, the AC. The DBRI and DBRO instructions are applied as control inputs for the 8235 IC. See Appendix A of the *PDP-8/E Maintenance Manual* for the truth table, logic diagram, and pin locator for the 8235 IC. DBRO will enable gates to select the Output Register contents; DBRI will enable gates to select the Input Register contents. The selected output will be applied to the Data Bus to load the AC.

SECTION 6
REAL-TIME PROGRAMMABLE CLOCK (DK8-EP)

4.6 INTRODUCTION

The DK8-EP Real-Time Programmable Clock consists of two PDP-8/E quad modules that plug into the OMNIBUS and are interconnected by an H851 Edge Connector. The M860 module, Real-Time Clock Control, contains a 12-bit binary counter, a 12-bit buffer register, and logic. The logic controls the counter/register operation and the companion quad module operation. This second quad module is the M518, containing Input logic and Schmitt triggers. Included on this module is a 12-bit storage register, logic that derives five different clock frequencies from a crystal-controlled oscillator, and three Schmitt trigger circuits that enable the user to control certain clock operations from external sources.

The DK8-EP provides a programmable time base that allows the user to control and/or record the occurrence of events both internal and external to the PDP-8/E. The clock can be used to count the number of events in a given amount of time, to measure the amount of time between two given events, or to initiate repetitive operations at specified intervals of time.

To perform these and similar operations, the major logic components listed must interact. The fundamental component is the 12-bit storage register, called the Clock Enable Register. This register can be loaded, bit by bit, under program control. Different bits are used to control different functional sections of the DK8-EP. For example: bit 7 of the register enables internally-generated clock pulses to be applied to the Clock Counter Register; bit 9, by enabling one of the Schmitt trigger circuits, allows an external source to control some aspects of clock operation. The Clock Enable Register can be set or cleared under program control and its contents can be transferred to the CPU AC Register at any time by a program instruction.

The Clock Counter Register counts clock pulses in a way that is predetermined by the state of Clock Enable Register bits 1 and 2. For example, the Clock Counter Register can count from 0 to 4096 repetitively, generating a signal (OVERFLOW L) each time it overflows to 0. In other circumstances, the programmer might wish the OVERFLOW L signal to be generated each 2000 clock pulses. The Clock Counter Register can be preset, to a count of 2096 in this example, in order to produce the desired result. The contents of the Clock Counter Register can be transferred to the AC Register at any time by a program instruction; however, to accomplish this transfer, the logic makes use of a 12-bit Clock Buffer Register.

The Clock Buffer Register is essential to the DK8-EP operation. Data is transferred between the AC Register and the Clock Counter Register via the Clock Buffer Register. To preset the Clock Counter Register, as in the example given, the program causes the Clock Buffer Register to be loaded from the AC Register with the preset count. Bits 1 and 2 of the Clock Enable Register can then be set so that the preset count, 2096, is loaded into the Clock Counter Register each time the OVERFLOW L signal is generated. Thus, the Clock Counter Register counts repetitively from 2096 to 4096. The Clock Buffer Register can be controlled by the program, and to a certain extent, by an external source. For example, Clock Enable Register bits 9–11 allow an external source to cause the Clock Buffer Register to be loaded; however, transfers between the AC and Clock Buffer Registers are limited to program control.

4.6.1 Block Diagram Discussion

The functional block diagram shown in Figure 4-51 illustrates the relationship between the registers and the remainder of the clock logic. Each functional block is discussed in detail in the following paragraphs and the applicable logic can be found in the indicated figures.

The IOT Decoder logic provides signals in response to the eight IOT instructions listed in Table 4-9. These IOT signals are distributed to the various functional sections as shown in Figure 4-52. The enabling signals from the Clock Enable Register are shown on the block diagram and are listed and explained in detail in Table 4-10.

For operations not involving external sources, the signal flow description can begin with the Clock Rate Select logic. The desired frequency of clock pulses is selected by the Rate Enable bits, while the Count Enable bit gates the clock pulses to the Load Buffer Register logic. This logic converts the clock pulses to B COUNT pulses that are counted by the Clock Counter Register. The logic also generates the LOAD BUFFER signal in response to program instructions and ensures that the B COUNT and LOAD BUFFER signals do not occur at the same moment (the significance of this is detailed in Paragraph 4.6.2.4).

The LOAD BUFFER signal causes the Clock Buffer Register to be loaded with data from either the AC Register, via the DATA 0—11 lines, or from the Clock Counter Register. The B COUNT pulses are counted by the Clock Counter Register in a way that is determined by signals from the Buffer/Counter Control Signal logic. These signals are asserted by combinations of IOT signals and Mode Enable bits 1 and 2.

The OVERFLOW L signal that is generated by the Clock Counter Register is applied to the OVERFLOW flip-flop logic. This logic asserts two signals that can be used by devices (e.g., analog-to-digital converters) to initiate some operation. OVERFLOW (0) L is suitable for external devices, while EXT PULSE L is designed to be used by OMNIBUS devices (A/D START). The status of the OVERFLOW flip-flop can be checked under program control and transferred to bit 0 of the AC Register via the DATA 0 line.

The logic also provides the OVERFLOW (1) signal that is applied to the Interrupt/Skip logic. Thus, each time the Clock Counter Register overflows: internal and external devices can begin some operation; the DK8-EP can request a program Interrupt; a program instruction can be skipped; or any combination of these events can occur, depending on the state of Clock Enable bits 0, 6, and 8.

Except for transfers between the Clock Buffer Register and the AC Register, the clock operates in much the same manner when an operation is initiated by external sources. Signals applied to the external input channels can activate one or more of the Schmitt triggers. The resulting signal, SCHMITT IN 1 L (or 2, or 3) is applied to the Input/Overflow Status logic. Here the status of each input channel can be checked under program control and forwarded to the AC Register. (Event Enable bit 9 enables the status of Schmitt trigger input 1 to be transferred to AC9 via DATA 9.)

The Input/Overflow Status logic allows the external event to generate the appropriate INT RQST (1, 2, or 3) L signal. This signal is applied to the Interrupt/Skip logic and can cause a program Interrupt. The INPUT 1+2+3 L signal is also asserted by the Input/Overflow Status logic and causes the Clock Rate Select logic to produce clock pulses. The Load Buffer Register logic and the Buffer/Counter logic then operate as already outlined.

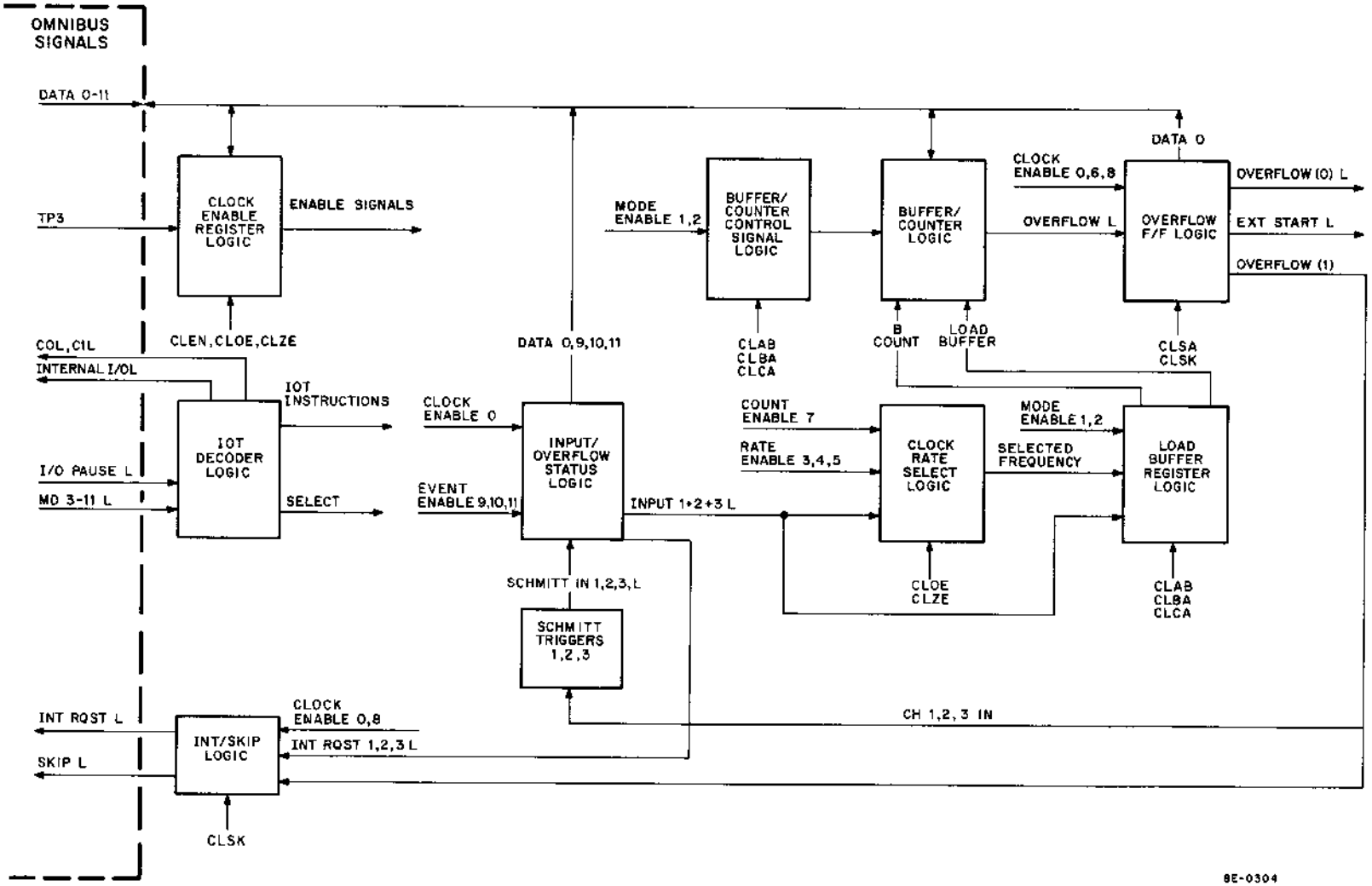


Figure 4-51 DK8-EP Functional Block Diagram

Table 4-9
DK8-EP IOT Instructions

Octal Code	Mnemonic	Function
6130	CLZE	Clear Clock Enable Register per AC Register. Each bit in the Clock Enable Register is cleared if the corresponding bit in the AC Register is set. The AC Register is unchanged.
6131	CLSK	Skip on a CLOCK flag. The next program instruction is skipped if either of the following skip conditions exists: *a.* An enabled Schmitt trigger has fired *b.* The Clock Counter Register has overflowed
6132	CLOE	Set Clock Enable Register per AC Register. Each bit in the Clock Enable Register is set if the corresponding bit in the AC Register is set. The AC Register is unchanged.
6133	CLAB	AC Register to Clock Counter Register. The contents of the AC Register are transferred to the clock and loaded into both the Clock Buffer and the Clock Counter Registers. The AC Register is unchanged.
6134	CLEN	Clock Enable Register to AC Register. The contents of the Clock Enable Register are transferred to the computer and JAMed into the AC Register. The Clock Enable Register is unchanged.
6135	CLSA	Status to AC Register. The state of the OVERFLOW flip-flop and of the three Schmitt input circuits is transferred to the computer and JAMed into the AC Register. Only the following AC bits are affected: **AC Bit — Status Condition** 0 — Enabled OVERFLOW flip-flop 9 — Enabled Schmitt input 3 10 — Enabled Schmitt input 2 11 — Enabled Schmitt input 1
6136	CLBA	Clock Buffer Register to AC Register. The contents of the Clock Buffer Register are transferred to the computer and JAMed into the AC Register. The Clock Buffer Register is unchanged.
6137	CLCA	Clock Counter Register to AC Register. The contents of the Clock Counter Register are transferred, via the Clock Buffer Register, to the computer and JAMed into the AC Register. The Clock Counter Register is unchanged.

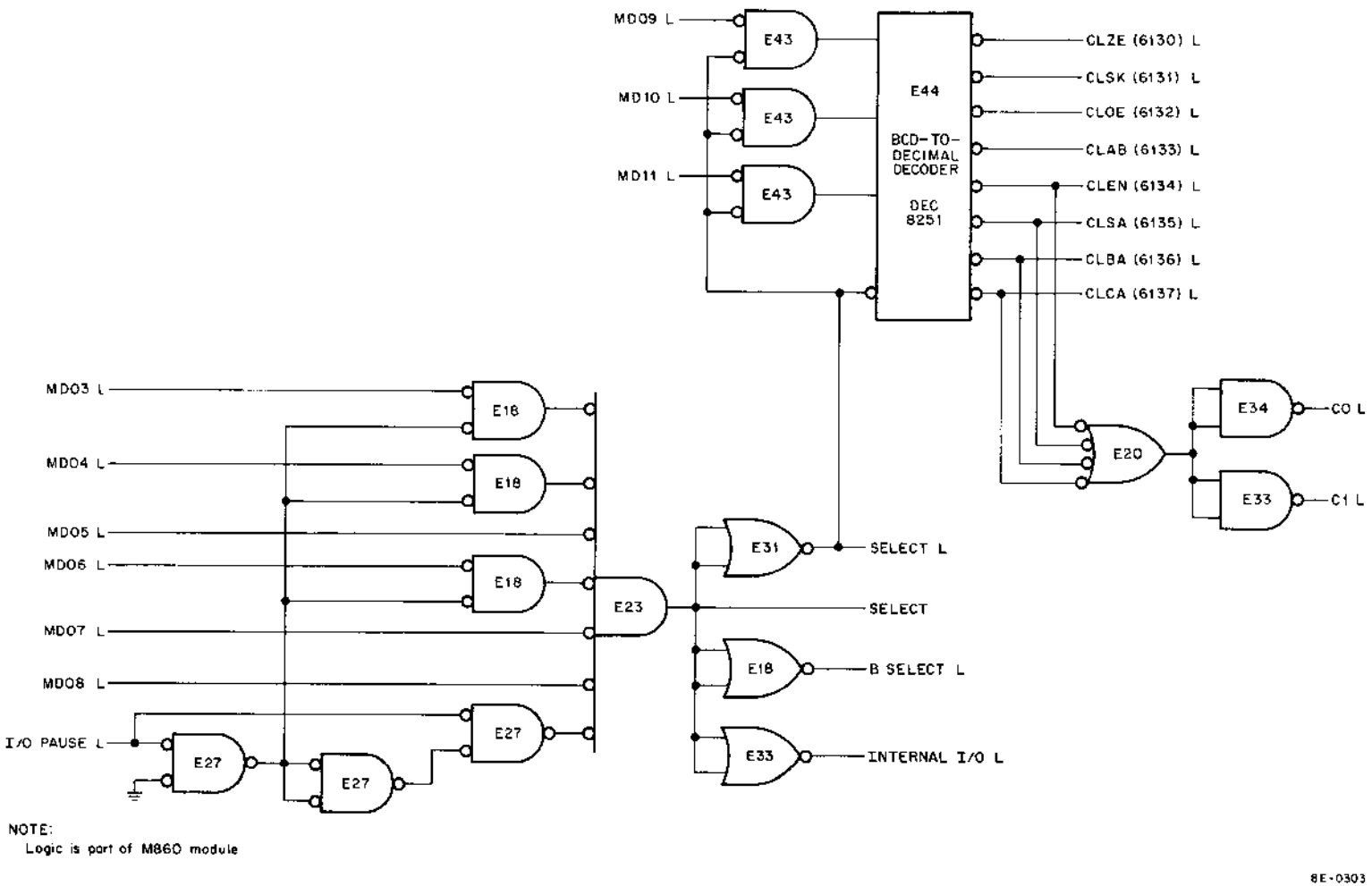


Figure 4-52 IOT Decoder Logic

Table 4-10
Clock Enable Register Enable Signals

Register Bit	Enable Signal Name	Function
0	CLOCK ENABLE 0	Enables a status check of the OVERFLOW flip-flop (CLSA), an instruction Skip on an overflow condition (CLSK), and a possible Interrupt request on an overflow condition.
1–2	MODE ENABLE 1 MODE ENABLE 2	Determine the Clock Counter Register mode of counting. The four possible modes are: 00 Register counts at the selected rate with overflow occurring every 4096 counts (see Table 4-11 for rates). 01 Register counts at the selected rate. At each overflow a preset count is loaded into the register from the Clock Buffer Register. Thus, overflow occurs every 4096 (preset) counts. 10 Register counts at the selected rate. An external event can sample the register at any time, causing the sample count to be transferred to the Clock Buffer Register. The Clock Counter Register continues counting. 11 Register counts at the selected rate. An external event can sample the register at any time. The sample count is transferred to the Clock Buffer Register and the Clock Counter Register is cleared before it resumes counting.
3–5	RATE ENABLE 3 RATE ENABLE 4 RATE ENABLE 5	Select the frequency of the internally-generated clock pulses (see Table 4-9 and Paragraph 4.6.2.3).
6	CLOCK ENABLE 6	Enables each Clock Counter Register overflow to generate the EXT PULSE L pulse that can be used by other OMNIBUS-connected devices (A/D START).
7	COUNT ENABLE 7	Inhibits clock pulses from being applied to the Clock Counter Register. (This bit can be cleared by firing an enabled Schmitt trigger.)
8	CLOCK ENABLE 8	Connects the Clock Interrupt logic to the computer interrupt system, enabling the Clock Interrupt conditions to assert the OMNIBUS INT RQST L signal.
9–11	EVENT ENABLE 9 EVENT ENABLE 10 EVENT ENABLE 11	Enable Schmitt trigger firings to turn on the clock, to cause a program interrupt, and to sample the Clock Counter Register (as set by bits 1, 2, 7, and 8).

Table 4-11
Frequencies Selected by Rate Enable Bits 3–5

Contents of Bits 3–5	Selected Multiplexer Output
000	No output
001	External frequency
010	100 Hz
011	1 kHz
100	10 kHz
101	100 kHz
110	1 MHz
111	No output

4.6.2 Detailed Logic

4.6.2.1 IOT Decoder Logic – The IOT Decoder logic is shown in Figure 4-52. The SELECT signal is asserted by NAND gate E23 when a 613X instruction is decoded. The SELECT signal, in turn, asserts the B SELECT L signal; the INTERNAL I/O L signal, which causes the positive I/O Bus interface to ignore the IOT instruction; and the SELECT L signal, which is used to gate MD bits 9–11 to the BCD-to-Decimal Decoder. The DEC 8251 IC decoder provides instructions 6130 through 6137, as illustrated in Figure 4-52.

Note that instructions 6134 through 6137 cause the OMNIBUS C0 L and C1 L signals to be asserted. Each of these instructions call for a transfer of data to the CPU AC Register. With C0 L and C1 L both asserted, the data is JAM-transferred into the AC Register, instead of being ORed with data already in the register.

4.6.2.2 Clock Enable Register Logic – The Clock Enable Register logic is shown in Figure 4-53. The register consists of 12 DEC 7474 flip-flops, only 2 of which are shown in the logic. Each flip-flop is given a descriptive title that characterizes the function of the flip-flop. For example: the MODE ENABLE 1 flip-flop is used to select, along with MODE ENABLE 2, the particular mode of operation of the Clock Counter Register; the COUNT ENABLE 7 flip-flop inhibits the Frequency Multiplexer from producing clock pulses at the selected frequency; the EVENT ENABLE 9 flip-flop enables an external event to control clock operations. (See Table 4-10 for a complete listing of the enable signals and their functions.)

Three program instructions deal exclusively with the Clock Enable Register. The CLEN (6134) instruction gates the register contents onto the DATA 0–11 lines. The information on the DATA lines is gated through the CPU Major Register and loaded into the AC Register. The CLZE (6130) and CLOE (6132) instructions clear and set, respectively, those Clock Enable Register flip-flops that correspond to set AC Register bits. For example, if bit 0 of the AC Register is logic 1, the CLOCK ENABLE 0 flip-flop can be set by the CLOE instruction or cleared by the CLZE instruction.

The Clock Enable Register can be cleared by the CLEAR signal. This signal is generated by the INITIALIZE signal that is produced when power is turned on, when the CLEAR key is depressed, or when the CAF instruction is issued.

4.6.2.3 Clock Rate Select Logic – The Clock Rate Select logic is shown in Figure 4-54. The basic 20-MHz clock frequency is provided by a crystal-controlled oscillator (see logic drawing E-CS-M518). This frequency is divided by the J-K flip-flop, E33. (When both the J and K inputs are high, the 1 output is changed with each positive transition at the C input.) The 10-MHz clock frequency is applied to a chain of DEC 7490 decade counters, each counter being wired to divide by ten. The output of each counter, which can be monitored at a test point, is applied to the E10 Frequency Multiplexer, a DEC 74151 IC. An external pulse source of any frequency can also be applied to the multiplexer, via pin RR on J1 of the M518 module. The desired frequency of clock pulses is obtained by selectively setting or clearing RATE ENABLE flip-flops 3, 4, and 5 with the CLOE or CLZE IOT instructions. Table 4-11 shows the relationship between the 1 outputs of these flip-flops and the multiplexer-output frequency.

Note that COUNT ENABLE 7 must be cleared if output pulses are to be obtained from the multiplexer. This particular Clock Enable Register flip-flop is illustrated because it differs from the remaining register flip-flops in an important way. Bit 7 can be cleared by an external event as well as by program instructions. Any of the three Schmitt-trigger input circuits can cause the INPUT 1+2+3 L signal to be asserted, thereby clearing the COUNT ENABLE 7 flip-flop and turning on the clock.

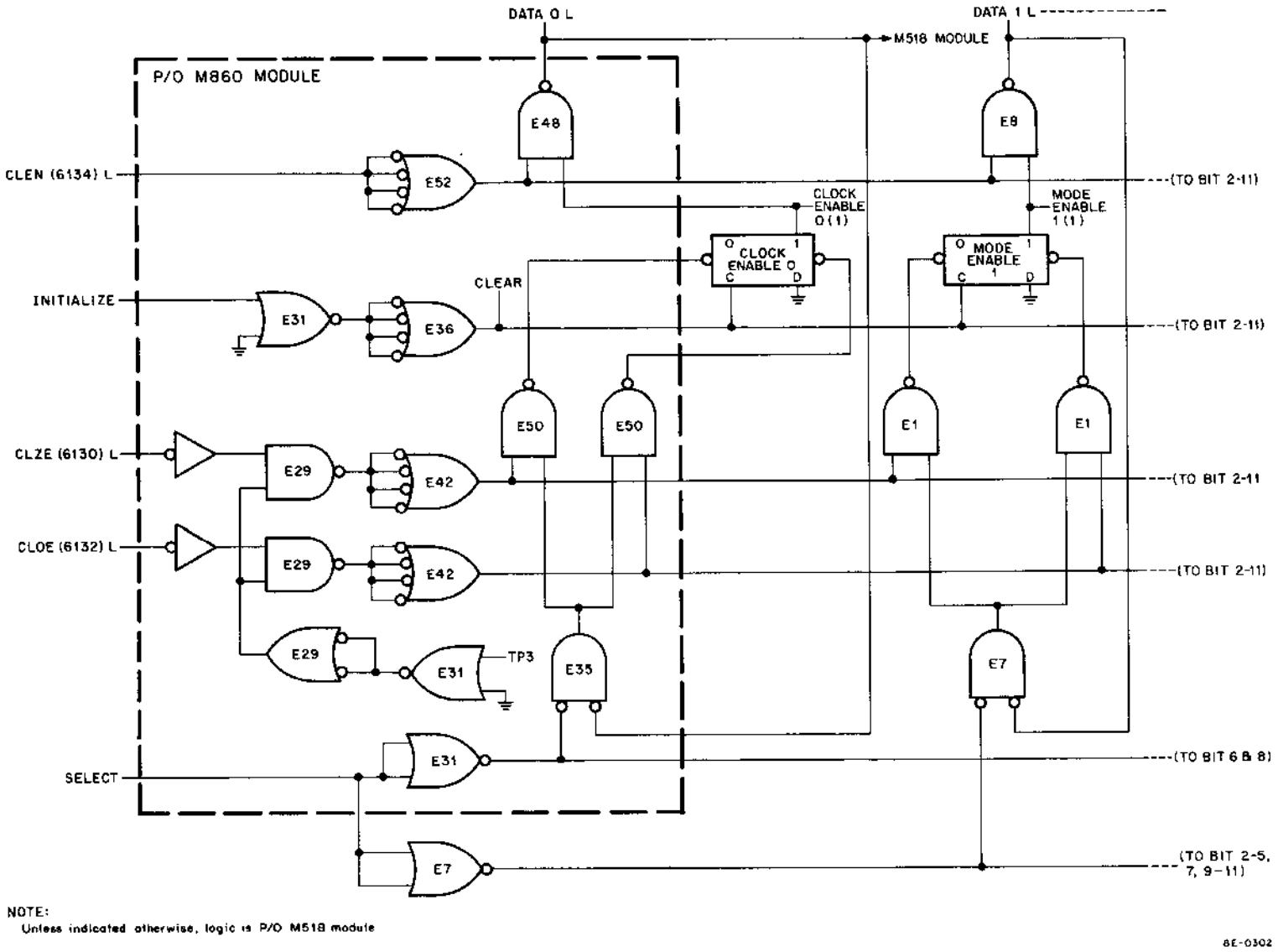


Figure 4-53 Clock Enable Register Logic

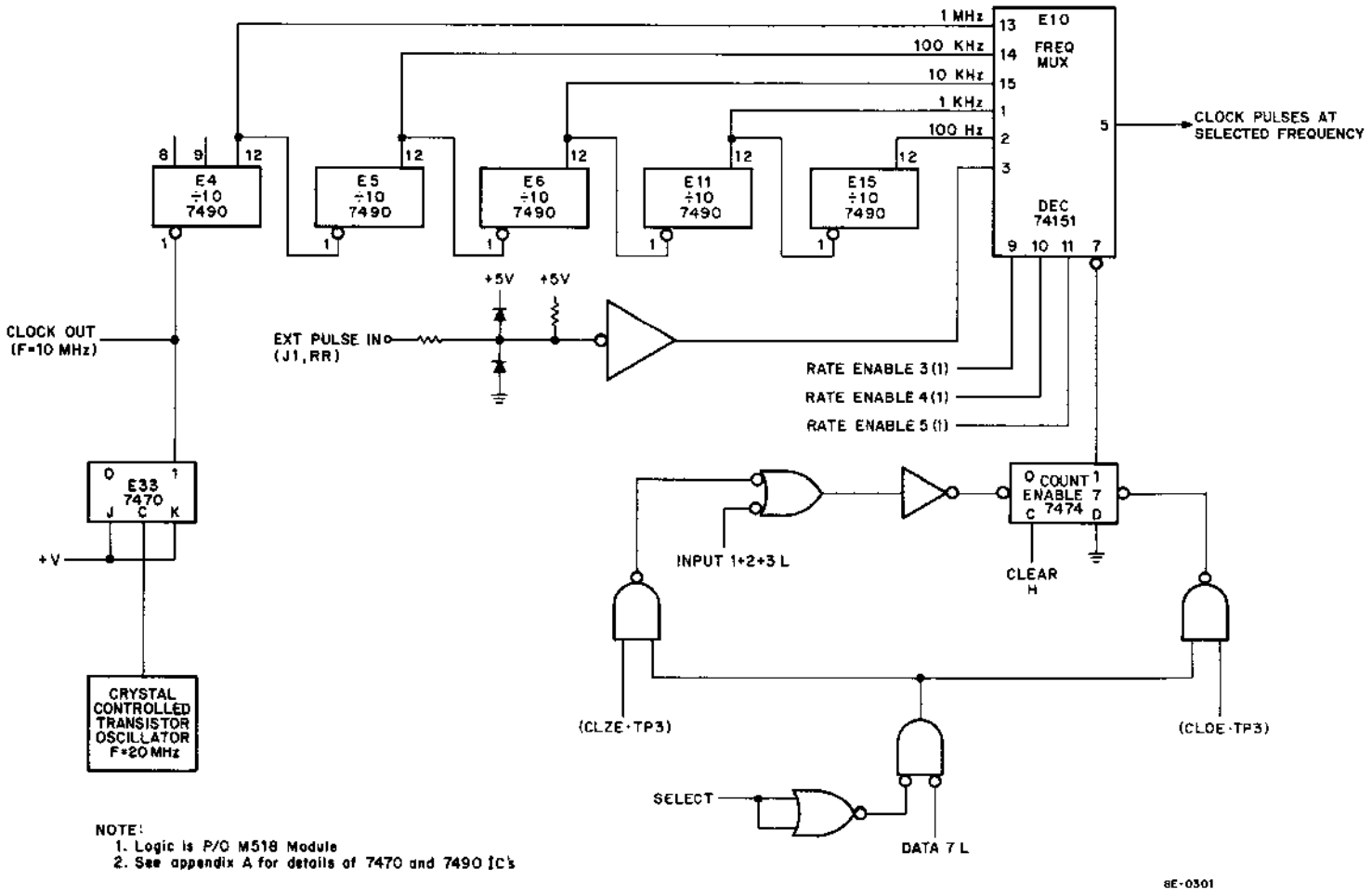


Figure 4-54 Clock Rate Select Logic

4.6.2.4 Load Buffer Register Logic – The Load Buffer Register logic is shown in Figure 4-55. The logic generates the LOAD BUFFER signal that loads the Clock Buffer Register and the B COUNT L pulses that are counted by the Clock Counter Register. The LOAD BUFFER signal can be asserted in response to either the 6133 IOT instruction, or the 6137 IOT instruction. The signal can also be asserted in response to an external event.

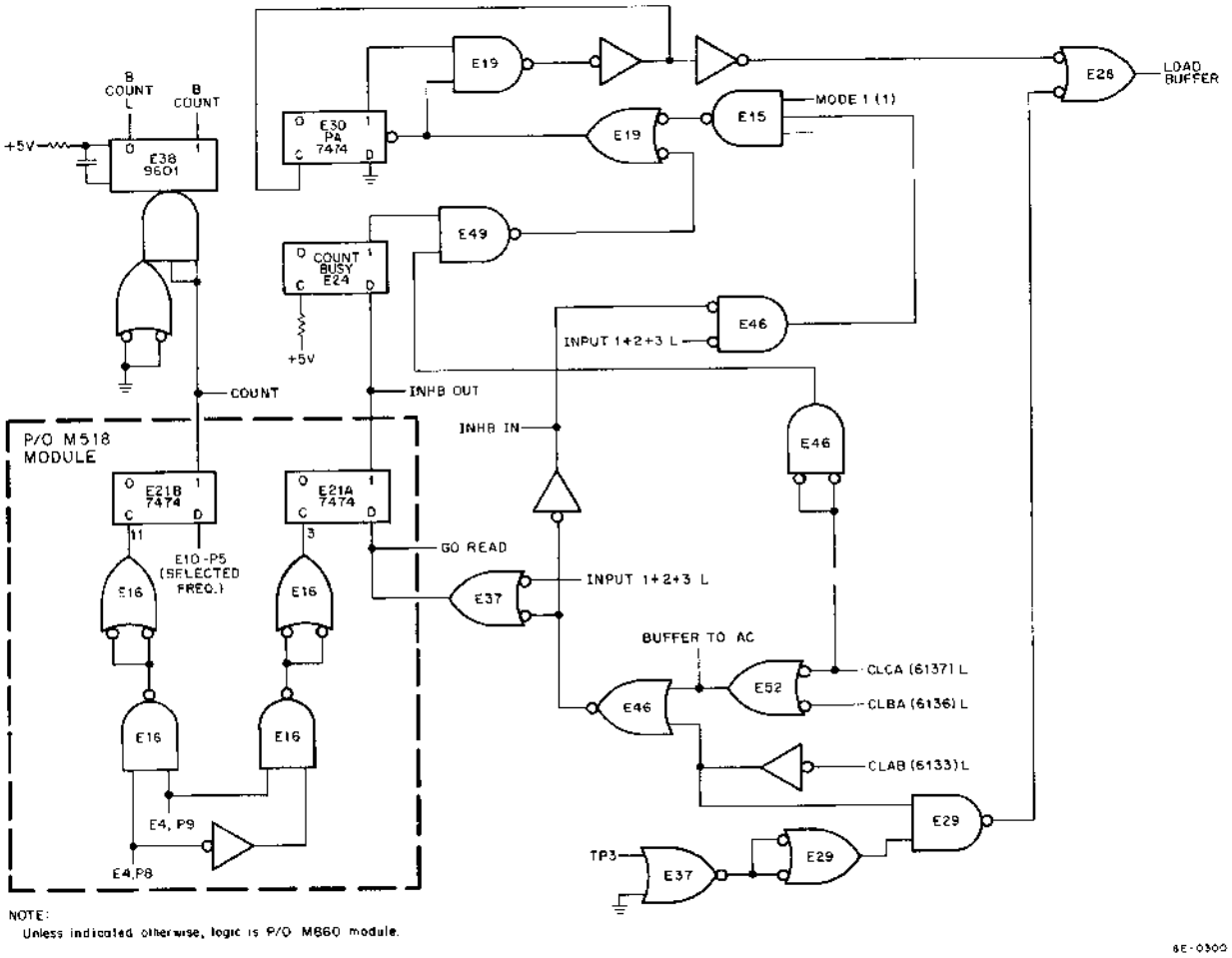


Figure 4-55 Load Buffer Register Logic

If the 6133 instruction is decoded, NAND gate E29 is enabled at TP3 time and, in turn, enables NOR gate E28 to assert the LOAD BUFFER signal. If an external event generates the INPUT 1+2+3 L signal, E28 again asserts the LOAD BUFFER signal. However, the enabling path is more complex than that of the 6133 instruction, for two reasons. First, the external event is allowed to generate the LOAD BUFFER signal only when Mode 10 or Mode 11 has been selected by Mode Enable bits 1 and 2 (NAND gate E15 can be enabled in either case). Second, an external event must not be allowed to assert the LOAD BUFFER signal when an IOT instruction is being carried out (NAND gate E46 is inhibited by the INHB IN signal during an IOT instruction). To illustrate the need for this prohibition, consider the 6136 and 6137 instructions. If the 6136 instruction is issued, the BUF TO AC signal is asserted. This signal gates the Clock Buffer Register output to the DATA lines. If the INHB IN signal were not asserted, an external event could generate the LOAD BUFFER signal during the IOT. Thus, the result would be identical to that achieved by a 6137 instruction.

The majority of the logic is designed to make the 6137 instruction operative. While the 6133 instruction loads the Clock Buffer Register with data from the CPU AC Register, the 6137 instruction loads the Clock Buffer with

the contents of the Clock Counter Register. Precautions have been taken to ensure that, if the 6137 instruction is issued, the LOAD BUFFER signal is not asserted at the moment the Clock Counter is changing its count. This prevents false counts that would result from reading the Clock Counter as one or more bits are in transition.

The precautionary logic includes flip-flop E21A and latch E24 shown in Figure 4-55. These two components and related gates generate signals that are illustrated in the timing diagram of Figure 4-56. Also shown in the timing diagram are signals generated by flip-flop E21B and one-shot E38. Both figures are referred to during the following discussion.

Flip-flops E21A and E21B are clocked by signals derived from the first decode counter in the Clock Rate Select logic (see Figure 4-54). The D input of E21B is controlled by the selected frequency output of the Frequency Multiplexer. In the timing diagram, this frequency is chosen as 1 MHz. When E21B is set, its 1 output triggers one-shot E38; E38 produces the B COUNT L signal for approximately 300 ns. The Clock Counter Register then counts the B COUNT L pulses which occur at the selected frequency.

When the 6137 instruction is issued, the CLCA L signal produced by the IOT Decoder logic asserts the GO READ signal. Because the clock is free-running, the GO READ signal can occur at any time with respect to the signal at the C input of E21A. If it occurs at the instant shown in the timing diagram, just before the pulse marked (A), E21A is set 200 ns before the B COUNT L signal is asserted. Because each bit of the Clock Counter Register consists of a master/slave flip-flop, the register bits are in transition on the leading edge of the B COUNT L pulse. Thus, the LOAD BUFFER signal causes the Clock Counter to be loaded into the Clock Buffer approximately 100 ns before the Clock Counter can change in response to the next B COUNT L pulse. (A delay of approximately 100 ns is introduced by the gating between E21A and NOR gate E28.) If the GO READ signal is asserted just after the leading edge of pulse (A), E21A is set by pulse (B), 300 ns after the B COUNT L signal is asserted. Thus, the Clock Buffer is loaded approximately 200 ns after the Clock Counter changes in response to the B COUNT pulse; enough time for the data to settle in the Clock Counter.

The amount of time between pulse (A) and pulse (B) is always 500 ns; therefore, the GO READ signal must be asserted for a longer amount of time to ensure that either (A) or (B) can set flip-flop E21A. This requirement is not met by normal CPU timing. In addition, under normal CPU timing it would be possible to lose the data that is being transferred from the Clock Counter Register. This could happen if the CLCA L signal were asserted just after the (A) pulse, for example. Under normal CPU timing for an internal IOT instruction (6137 is such an instruction), the AC LOAD L signal is asserted at TP3 time. In the present example, TP3 could occur before the count has been placed on the CPU Major Register Bus; thus, the count would be lost. Both these difficulties may be overcome by increasing the period of time during which the CLCA L signal is asserted. The logic shown in Figure 4-57 is designed to increase the available time to approximately 650 ns.

When the BUF TO AC signal is asserted, one-shot E47 is triggered and remains set for approximately 650 ns. The OMNIBUS NOT LAST TRANSFER L signal is asserted for the same amount of time. Because NOT LAST TRANSFER L is low when TP3 of the IOT instruction (6137 in the present example) occurs, the CPU timing is interrupted and stalled in TS3. Until normal timing is resumed, the OMNIBUS I/O PAUSE L signal remains low, keeping CLCA L low and, thus, GO READ high. When one-shot E47 times out, NOT LAST TRANSFER L is negated. Perhaps 40-ns later, time enough for the NOT LAST TRANSFER line to settle, latch E24 causes the OMNIBUS BUS STROBE L signal to be asserted. This signal causes normal CPU timing to begin from the point of interruption. I/O PAUSE L is negated, in turn negating the CLCA L signal and, finally, the GO READ signal.

4.6.2.5 Clock Buffer/Clock Counter Logic – The Clock Buffer/Clock Counter logic is shown in Figure 4-58. The logic for bits 1–10 is identical to that for bit 11. The Clock Buffer Register is a storage register composed of DEC7474 IC flip-flops. The Clock Counter Register is a presettable binary counter composed of DEC 74197 ICs (see Appendix A for a detailed description). Each bit can be preset at the S input and cleared at the R input.

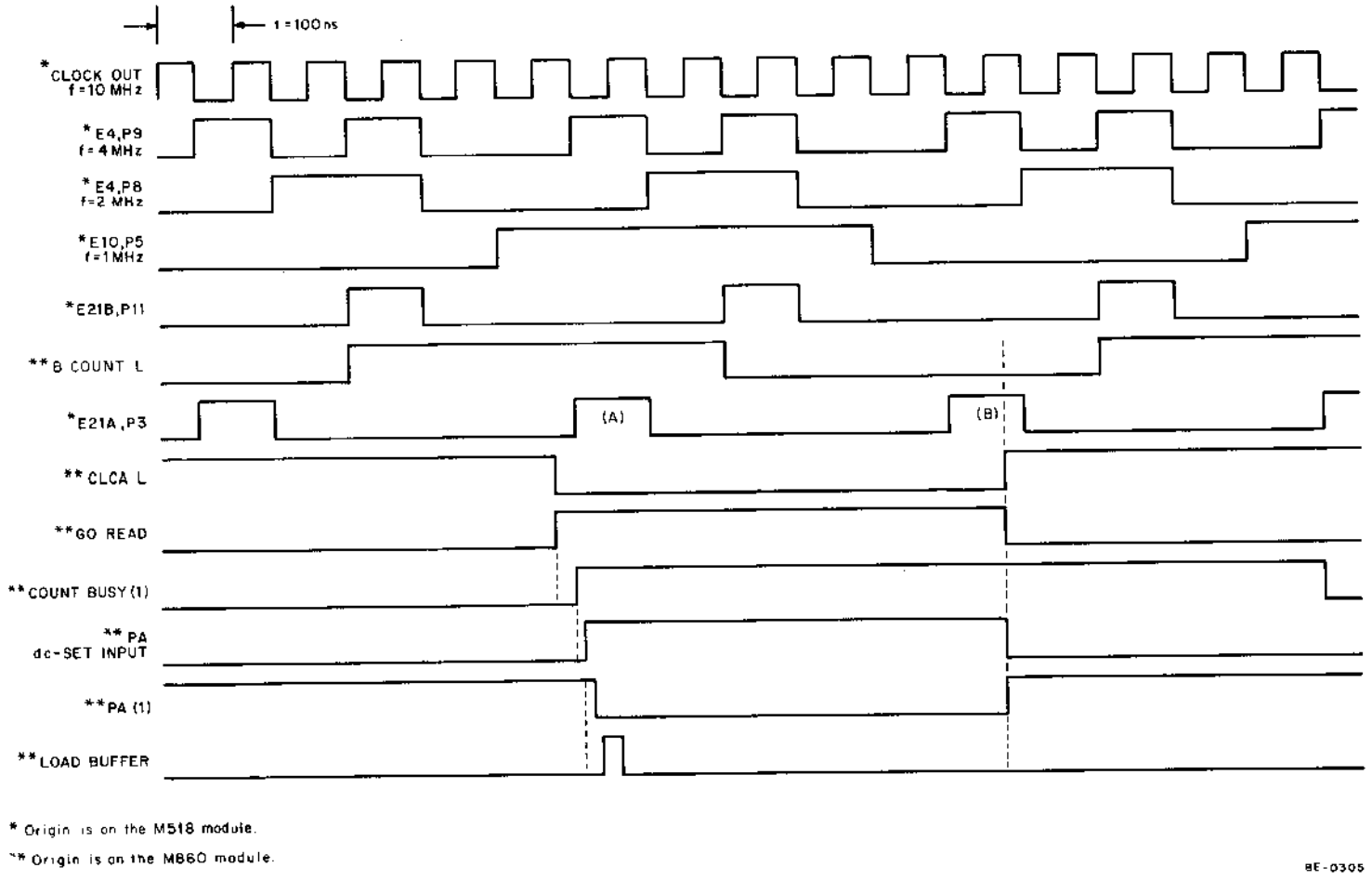


Figure 4-56 Load Buffer Register Timing

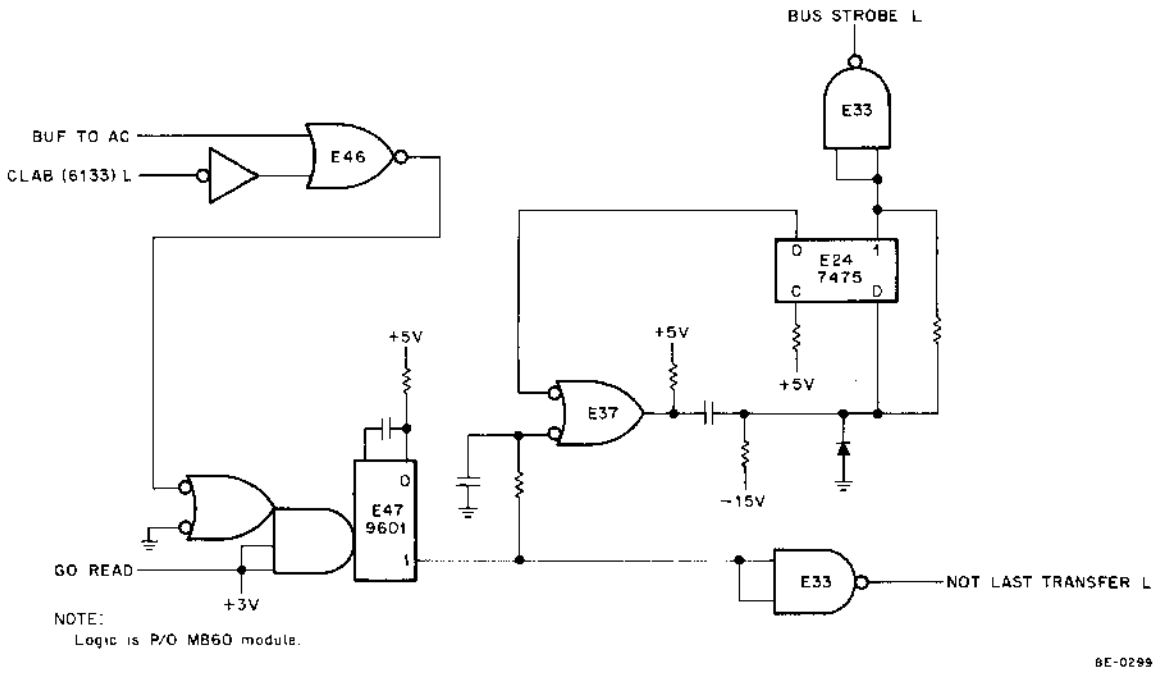


Figure 4-57 NOT LAST TRANSFER Logic

The B COUNT pulses are applied to the bit 11 toggle (T) input; the negative transition of each B COUNT L pulse causes the 1 output to change. The 1 output of each bit is connected to the T input of the following bit and the Buffer Multiplexer, a DEC 8266 IC.

The logic enables the exchange of data between the Clock Buffer Register and the Clock Counter Register, and between these two registers and the CPU AC Register. Data transfers between the Clock Buffer and the Clock Counter can be controlled by external events; however, transfers between these two registers and the AC can be accomplished only under program control. The first type of transfer, between Clock Buffer and Clock Counter, can be considered an internal transfer (internal to the clock), while the second can be considered as external.

Three different transfers can be grouped under each type, as shown in column 1 of Table 4-12. Column 2 of this table shows both the source register and the destination register of each transfer. Column 3 shows the control signals that must be asserted for each transfer. For example, if the DK8-EP is operating in mode 10, an external event can cause a transfer from the Clock Counter to the Clock Buffer by asserting the CTR ENABLE and the LOAD BUFFER signals. The output of the Clock Counter Register is applied to the Buffer Multiplexer. Because CTR ENABLE is asserted (this signal is asserted for all transfers except CLAB), the Clock Counter data is gated through the multiplexer to the Clock Buffer, which is then loaded by the LOAD BUFFER signal. Note that Mode 11 transfers are similar, but that the CLR CTR L signal clears the Clock Counter after data is transferred to the Clock Buffer.

The data placed in the Clock Buffer by any of these internal transfers can be passed to the AC only by an external-type transfer. The CLBA instruction asserts the BUF TO AC signal that gates the Clock Buffer output onto the OMNIBUS DATA lines. The information on the DATA lines is then gated to the AC Register and loaded at BUS STROBE L time.

Data can be transferred from the AC to the Clock Counter by the CLAB instruction. In this case, information in the AC Register is placed on the DATA lines and gated to the Buffer Multiplexer (B SELECT L is asserted by the IOT Decoder logic). The AC ENABLE signal is asserted, gating the data to the Clock Buffer. The LOAD BUFFER signal loads the register and the BUF TO CLR L signal gates the Clock Buffer output to the S input of the Clock Counter.

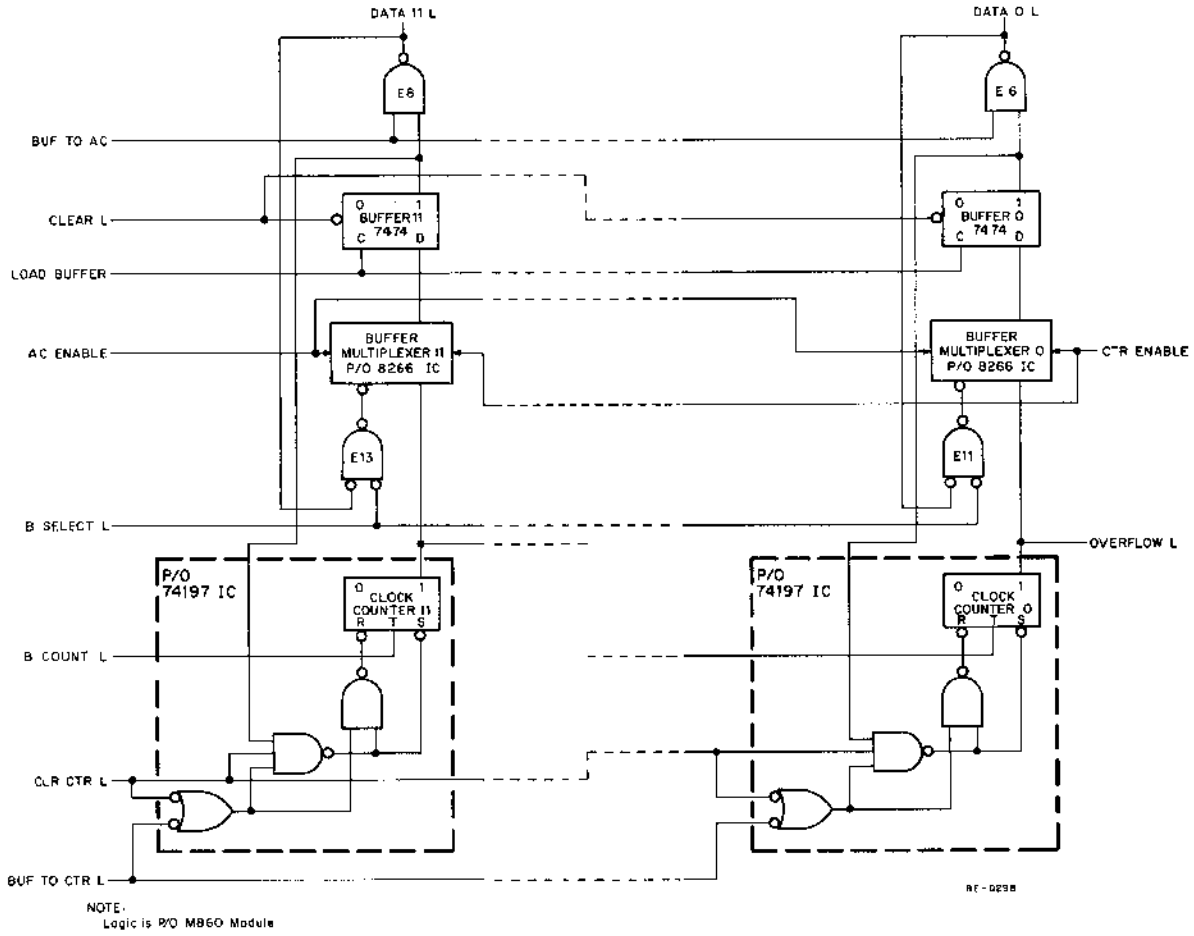


Figure 4-58 Clock Buffer/Clock Counter Logic

Table 4-12
Control Signals for Clock External and Internal Transfers

Transfer Type	From/To	Control Signal Asserted
Internal		
Mode 01	Clock Buffer/Clock Counter	BUF TO CTR L, CTR ENABLE
Mode 10	Clock Counter/Clock Buffer	CTR ENABLE, LOAD BUFFER
Mode 11	Clock Counter/Clock Buffer	CTR ENABLE, LOAD BUFFER, CLR CTR L
External		
CLAB	AC Register/Clock Counter	AC ENABLE, LOAD BUFFER, BUF TO CTR L
CLBA	Clock Buffer/AC Register	BUF TO AC, CTR ENABLE
CLCA	Clock Counter/AC Register	CTR ENABLE, LOAD BUFFER, BUF TO AC

The control signals are asserted by the logic illustrated in Figure 4-59. BUF TO AC and AC ENABLE are used only during external transfers and, thus, are asserted only by program instructions. (Note that the AC ENABLE and CTR ENABLE signals are mutually exclusive.) However, because the Clock Buffer is loaded during both

external and internal transfers, external events, as well as program instructions, can generate the LOAD BUFFER signal. The BUF TO CTR L signal is also used for both internal and external transfers (the Mode 01 transfer can be accomplished only when the MSB of the Clock Counter Register asserts the OVERFLOW L signal).

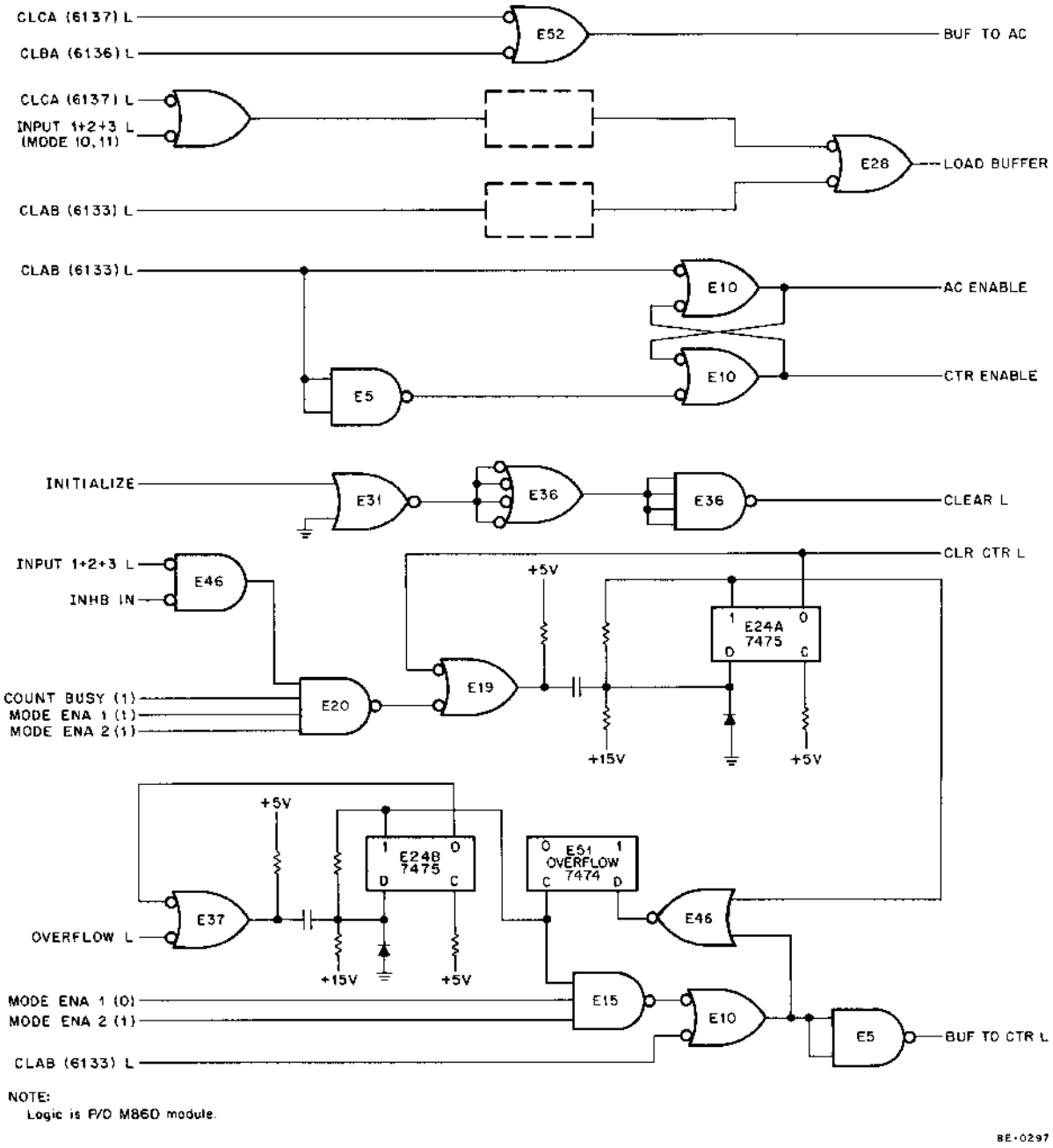


Figure 4-59 Clock Buffer/Clock Counter Control Signals

The CLR CTR L signal is asserted only when a Mode 11 transfer is initiated by an external event. Bi-stable latch E24A (one-shot) asserts the CLR CTR L signal. Note that the 1 output of the latch is applied to the E51 OVERFLOW flip-flop via NOR gate E46. The MSB of the Clock Counter might go from a high to a low when CLR CTR L is asserted. Such a transition asserts the OVERFLOW L signal, thereby enabling NOR gate E37. The 1 output of latch E24B goes high (one-shot). The OVERFLOW flip-flop would be set unintentionally if E46 was

not enabled. The same problem could arise when the CLAB instruction is issued; thus, NOR gate E10 is also applied to E46.

Although the CLR CTR L signal can be asserted only by an external event, the Clock Counter can be cleared under program control. The Clock Buffer must first be cleared. This can be done either by issuing a CAF (Clear All Flags) instruction, or by depressing the CLEAR key on the programmer's console. The INITIALIZE signal is asserted by either method (and by power turn-on). The CLEAR L signal then clears the Clock Buffer Register and the contents of the Clock Buffer can be transferred to the Clock Counter.

4.6.2.6 OVERFLOW Flip-Flop Logic – The OVERFLOW flip-flop logic is shown in Figure 4-60. The logic monitors the MSB of the Clock Counter Register via the OVERFLOW L signal. When the register asserts the OVERFLOW L signal, the OVERFLOW flip-flop, E51, is normally set. (NOR gate E46 prevents the flip-flop from being set unintentionally; see Paragraph 4.6.2.5.) The set state of the flip-flop enables the logic to assert various signals selectively. The selectivity depends on the state of certain Clock Enable Register flip-flops and on the particular program instruction, if any, that is issued.

The OVERFLOW (0) L signal and the EXT PULSE L signal have similar purposes; i.e., to initiate some operation, such as analog-to-digital conversion, when overflow of the Clock Counter Register occurs. When OVERFLOW L is asserted, latch E24 enables NAND gate E5, provided that the CLOCK ENABLE 6 flip-flop was set by a previous CLOE instruction, and sets the E51 OVERFLOW flip-flop. The 1 output of E51 enables NAND gate E19, thereby asserting the EXT PULSE L signal. E24 remains latched for approximately 100 ns. (The duration of the latch is determined by the RC time constant of the D input; see Appendix A for details.) Thus, the EXT PULSE L signal is a pulse that can be generated each time an overflow occurs.

The EXT PULSE L pulse is designed to be used with an A/D converter that plugs into the OMNIBUS. (The signal can be taken from the M860 module, conveniently, only via an H851 Edge Connector.) In such an application, the EXT PULSE L pulse sets the rate at which an analog signal is sampled by the A/D converter.

The 0 output of E51 is buffered before it asserts the OVERFLOW (0) L signal. This signal, once asserted, remains so until E51 is cleared under program control. The OVERFLOW (0) L signal is made available at a 40-pin connector on the M518 module. Thus, it can be used by both external and internal devices in a variety of applications.

No matter what the application, the OVERFLOW (0) L signal is useful, generally, only when it can be continuously asserted. Therefore, flip-flop E51 must be repeatedly cleared. The flip-flop can be cleared, not only by the INITIALIZE signal (generated at power turn-on, by the CLEAR key, or by the CAF instruction), but also by the 6135 instruction, STATUS TO AC. The 6135 instruction can clear E51 only if the CLOCK ENABLE 0 flip-flop has been previously set by a CLOE instruction. When E51 is set, NAND gate E50 is enabled and it, in turn, enables NOR gate E49. When CLSA is issued, the STATUS TO AC signal enables NAND gate E48, asserting the DATA 0 L signal. At TP3 time, E51 is cleared and can be set by the next Clock Counter Register overflow.

The status of E51 can be checked either by the CLSK instruction alone, or via the Interrupt system and the CLSK instruction. The Interrupt system can be used only if the CLOCK ENABLE 8 flip-flop has been set. E51 can then assert the INT RQST L signal. The CLSK instruction in the Interrupt-servicing routine will cause a Skip to the DK8-EP subroutine, where CLSA causes the status of E51 to be transferred via the DATA 0 line to AC0.

4.6.2.7 Interrupt/Skip Logic – The Interrupt/Skip logic is shown in Figure 4-61. As indicated in previous discussions, program Interrupts can be caused by external events and by overflow from the Clock Counter Register. The DK8-EP can be logically connected to the computer Interrupt system if the CLOCK ENABLE 8 flip-flop is set by a CLOE instruction. When this flip-flop alone is set, an external event can cause a program Interrupt. The event causes the INT REQ 1, 2, or 3 L signal to be generated by the Input/Overflow Status logic. This signal first enables NOR gate E15, and finally causes NAND gate E34 to assert the OMNIBUS INT RQST L signal.

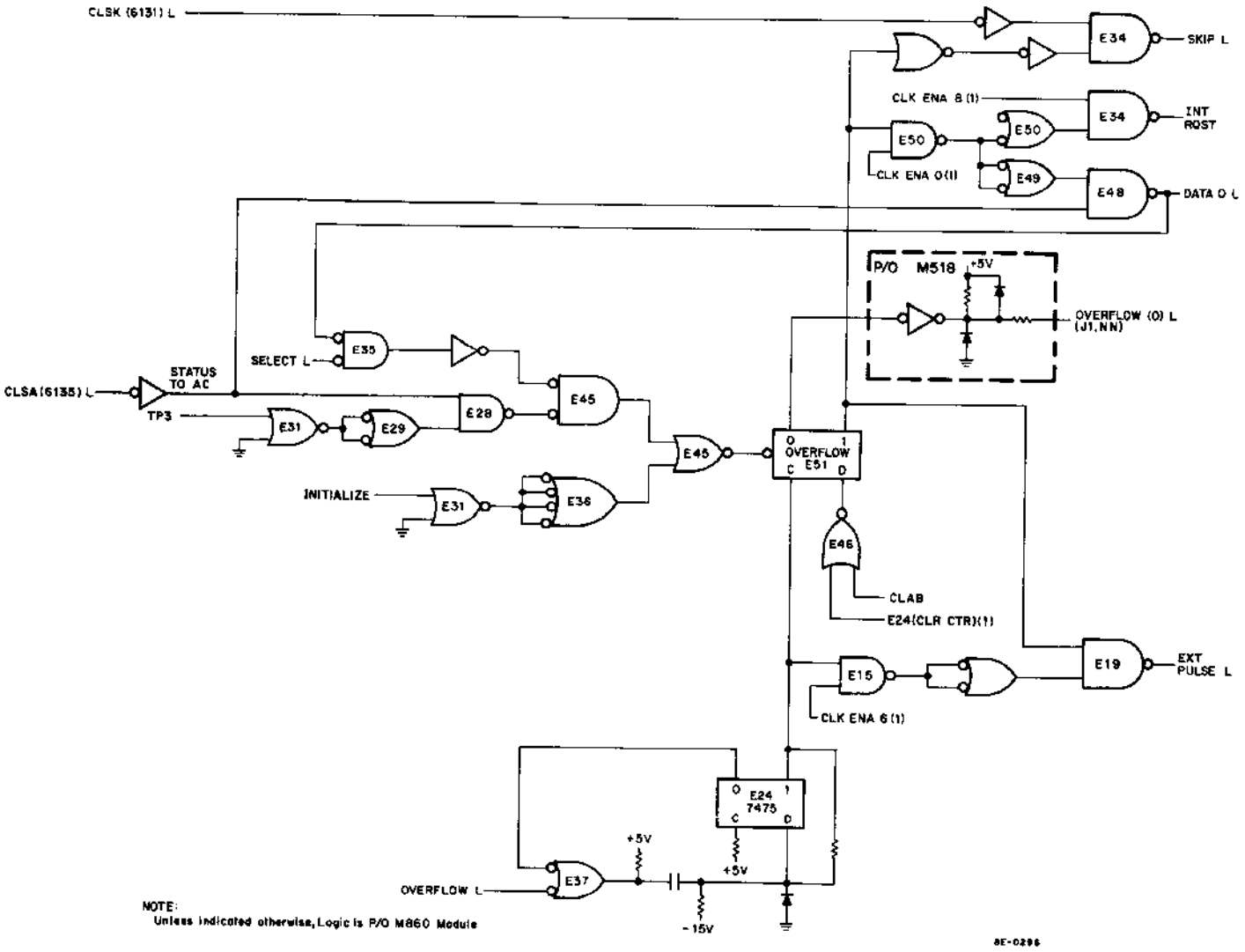


Figure 4-60 OVERFLOW Flip-Flop Logic

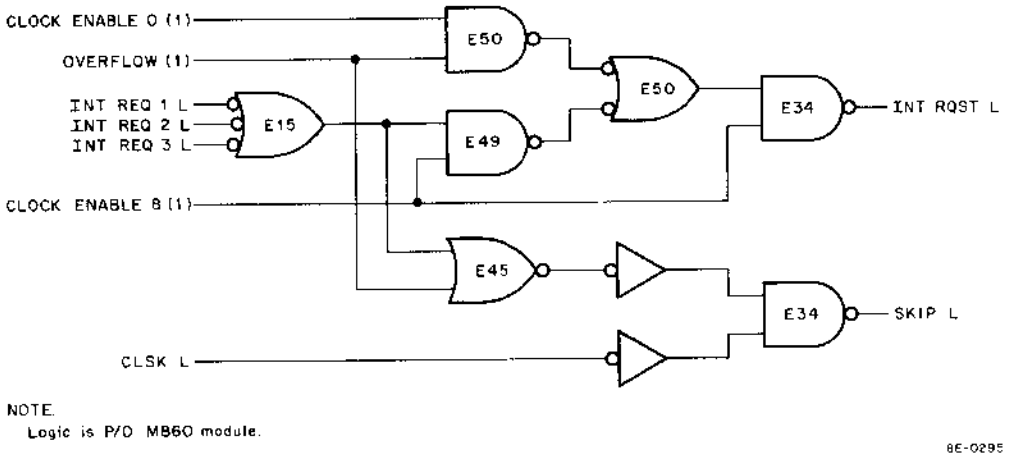


Figure 4-61 Interrupt/Skip Logic

If the OVERFLOW (1) signal from the OVERFLOW flip-flop logic is to generate an Interrupt request, the CLOCK ENABLE 0 flip-flop must also be set. This signal can then cause the INT RQST L signal to be asserted by NAND gate E34.

When the computer enters the Interrupt-servicing routine in response to the DK8-EP Interrupt request, the CLSK instruction causes NAND gate E34 to assert the OMNIBUS SKIP L signal. Thus, the computer can be directed to the particular subroutine that services the request. The CLSK instruction may still be used when the clock is not connected to the computer Interrupt system. The program can enter a waiting loop which checks the status of the two conditions (overflow and external event). When either condition is met, the appropriate subroutine is entered.

4.6.2.8 Input/Overflow Status Logic – The Input/Overflow Status logic, shown in Figure 4-62, enables the programmer to check the status of the OVERFLOW flip-flop and the Schmitt trigger input channels. Input channel 3 is illustrated fully in Figure 4-62; the logic functions are as follows. An external event can cause the SCHMITT IN 3 L signal to be asserted. If the EVENT ENABLE 09 flip-flop has been set by a previous CLOE IOT instruction, the SCHMITT IN 3 L signal sets the STATUS 3 flip-flop and asserts the INPUT 1+2+3 L signal. The latter signal can either actuate the clock or cause the contents of the Clock Counter Register to be transferred to the Clock Buffer Register. When the STATUS 3 flip-flop is set, it asserts the INT RQST 3 L signal. This signal can result in a program Interrupt request, if the CLOCK ENABLE 8 flip-flop has been set by some previous CLOE instruction.

Assume that the external event causes a program Interrupt. The OMNIBUS INT RQST L signal is asserted and the CPU enters the Interrupt-servicing routine. The CLSK instruction in the servicing routine causes the program to proceed to the DK8-EP subroutine. The CLSA IOT instruction determines how often the event occurs in a given amount of time and/or which input channel caused the program Interrupt. When this instruction is issued, the Select logic generates the CLSA L signal that, in turn, generates the STATUS TO AC signal (see Figure 4-62). The leading edge of the STATUS TO AC signal sets the SYNC 3 flip-flop (the D input of the flip-flop is high because the STATUS 3 flip-flop is set). NAND gate E3 and NAND gate E8 are enabled, the latter gate asserting the DATA 09 L signal. The CLSA L signal causes the OMNIBUS C0 L and C1 L signals to be asserted, resulting in a JAM-transfer to the AC Register of the information on the DATA 09 line.

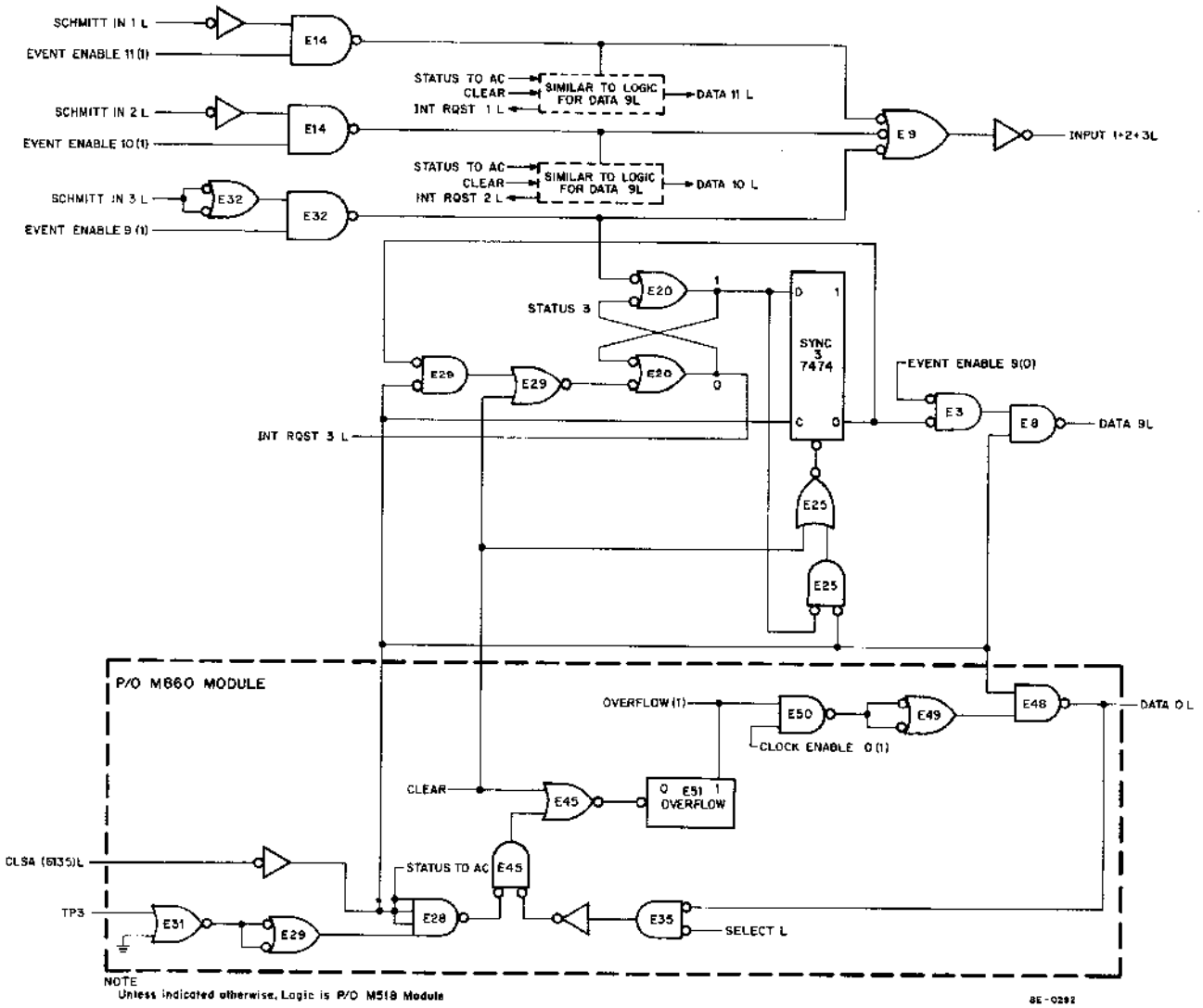


Figure 4-62 Input/Overflow Status Logic

At approximately the same time that the DATA 09 L signal is asserted, the STATUS 3 flip-flop is cleared via NAND gate E29 (the SYNC 3 flip-flop 0 output enables E29). Approximately 500 ns later (a function of the CPU Timing Generator), the CLSA L signal is negated. The SYNC 3 flip-flop is then cleared via NAND gate E25. The two flip-flops are cleared so that only one occurrence of an event is transferred for each interrogation, and so that an event is indicated only when the event actually does occur.

The OVERFLOW flip-flop also can cause a program Interrupt (see Figure 4-61 for the Interrupt logic). The CLSA instruction allows the programmer to differentiate between external-event-generated Interrupts and overflow-generated Interrupts. For example, if the OVERFLOW flip-flop is set, and if the CLOCK ENABLE 0 flip-flop has been set by a CLOE instruction, the CLSA L signal causes the DATA 0 L signal to be asserted. At the same time, the C0 L and C1 L signals are asserted and the data is JAMed into the AC Register. At TP3 time, the OVERFLOW flip-flop is cleared via NAND gate E45; the flip-flop can now be set by a new overflow from the Clock Counter Register.

4.6.2.9 Schmitt Trigger Logic – The Schmitt trigger logic for channel 1 is shown in Figure 4-63. The logic for channels 2 and 3 is identical to that shown for channel 1. The logic consists of a Schmitt trigger circuit, the components to the left of inverter E41, and the 2-output pulse-shaping circuits to the right of E41.

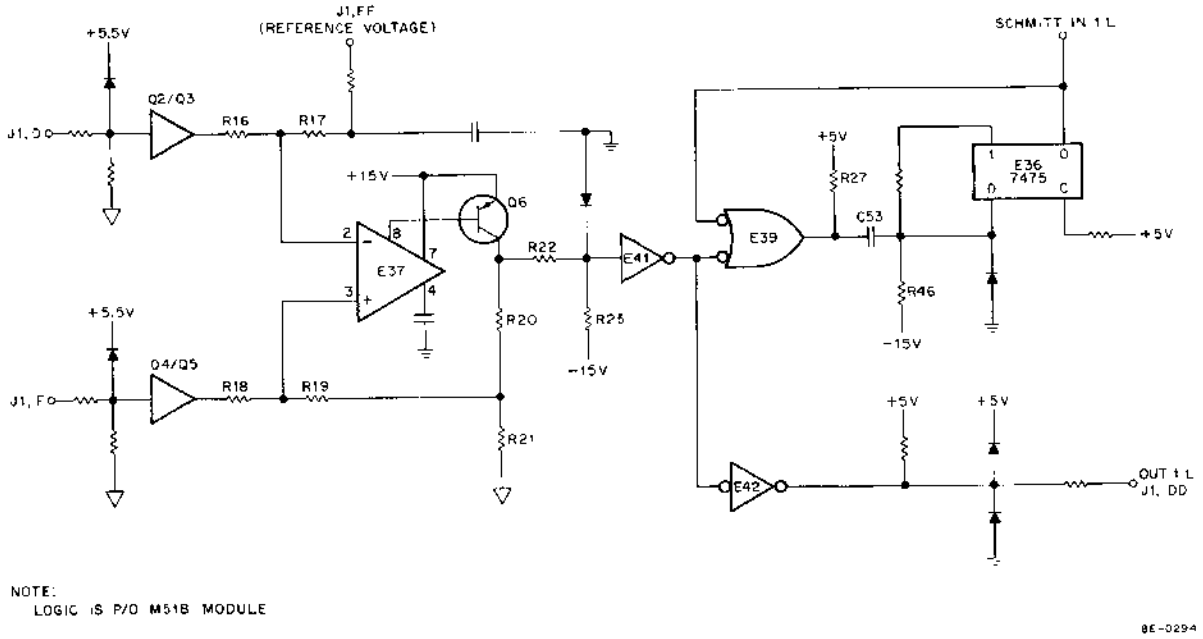


Figure 4-63 Schmitt Trigger Logic

The Schmitt trigger circuit is built around a DEC 1709C IC, E37 (see Appendix A for details). This IC is an operational amplifier used as a comparator in the Schmitt trigger. In this application, only half of the IC internal circuitry is being used; the output of E37 is taken from pin 8 rather than pin 6. The output at pin 8 has the same relationship to the input at pins 2 and 3, as does the output at pin 6; i.e., pin 8 inverts the input at pin 2, but not the input at pin 3. For clarity, many of the components comprising the Schmitt trigger inputs have been represented by the logic inverters designated Q2/Q3 and Q4/Q5 (see logic drawing E-CS-M518-0-1 for the actual circuits). The differential input to the Schmitt trigger is applied between J1D and J1F. The firing threshold voltage, which can be varied between ±5V, is applied at J1F. The hysteresis voltage, 0.3V, is determined by the value of resistors R20, R21, and R22.

Assume a threshold voltage of +4V. Until this voltage is exceeded by the differential input, the non-inverting input of E37 (pin 3) is positive with respect to the inverting input (pin 2), and pin 8 is at approximately +15V. Thus, transistor Q6 is in the non-conducting state and the input to inverter E41 is near ground. Both the SCHMITT IN 1 L and the OUT 1 L signals are negated. When the differential input crosses the threshold, going positive, the inverting input goes positive with respect to the non-inverting input. The voltage at pin 8 drops to near ground and Q6 switches on. The positive-going edge at the input of E41 triggers the latch circuit and E36 generates a pulse (duration determined by C53/R46 time constant), the SCHMITT IN 1 L signal, which is applied to the Input/Overflow Status logic. The OUT 1 L signal goes low when E41 is enabled, remaining low until the Schmitt trigger is reset. The trigger remains in the fired state until the differential input falls below +3.7V (threshold voltage minus hysteresis voltage). When this occurs, Q6 is turned off and remains off until the threshold is again exceeded.

The Schmitt trigger logic is part of the M518 module, Input logic, and Schmitt triggers. The DK8-EP user must provide cabling for the Schmitt trigger differential inputs and outputs, as well as for ground connections and threshold voltages; without these signals, the Schmitt triggers are inoperable. The connections to the M518 module are made via J1 on the module.

The DK8-ES user is provided with a DK8-EF front panel that not only simplifies the interconnection of signal sources and Schmitt triggers, but also includes potentiometers that allow the user to control the threshold voltages. The circuit schematic of this front panel is illustrated, in part, in Figure 4-64. The schematic is shown for channel 1 only; the circuits for channels 2 and 3 are identical.

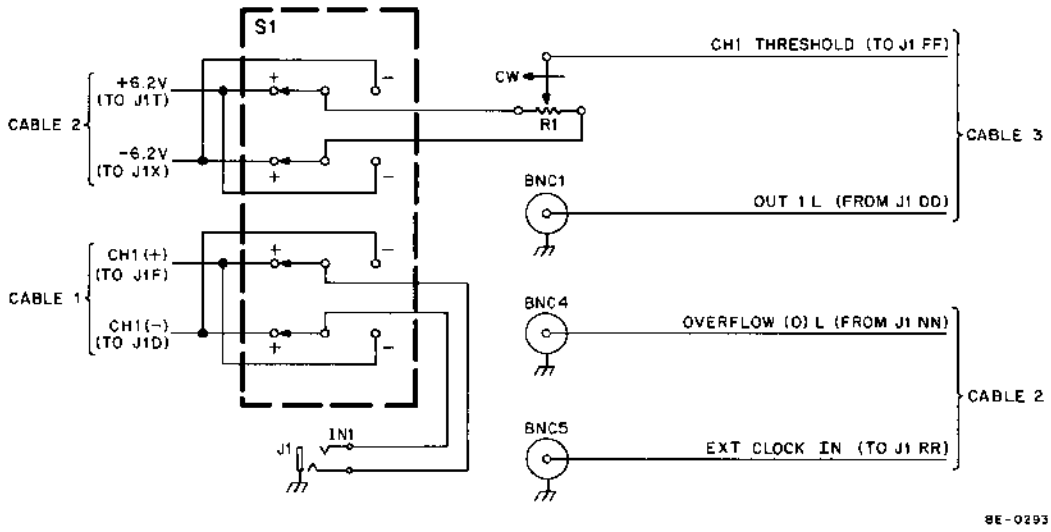


Figure 4-64 DK8-EF Front Panel Schematic

The source signal, designated IN1, is applied at phone jack J1 on the front of the DK8-EF. The SLOPE switch allows the user to select a positive- or negative-going slope on which to fire the Schmitt trigger. Note that a positive slope is accompanied by a positive threshold voltage; when a negative slope is selected, the threshold voltage is switched negative. The input signal is switched through S1 and connected by cable 1 to J1 on the M518 module. The reference voltage is taken from the wiper arm of R1 and connected by cable 3 to J1. The OUT 1 L signal from the M518 module is also connected by cable 3 to the BNC1 connector on the front panel. Channels 2 and 3 are wired in similar fashion. Note that cables 1, 2, and 3 are wired directly to the BNC connectors, the switches, and the potentiometers, with no intervening jacks or connectors. The three cables are joined in one 40-pin Berg connector that mates with J1.

Also note that two signals, not directly associated with the Schmitt triggers, are accessible at the front panel connectors. One of these signals is the OVERFLOW (0) L signal from the OVERFLOW flip-flop logic. The other is the EXT CLOCK IN signal (input) which is applied to the Clock Rate Select logic.

SECTION 7
HIGH QUALITY POWER SUPPLY

4.7 INTRODUCTION

The LAB-8/E High Quality power supply provides regulated ±15 Vdc power. The HQ power supply has remote sensing, supplies 1.5A, and has less than 1 mV/RMS of ac ripple on the output. Table 4-13 gives the power supply specifications and operating characteristics.

Table 4-13
High Quality Power Supply Parameters and Specifications

Parameter	Specification
Input Frequency	47 to 420 Hz
Output Voltage	15 ± 15 mV
Input Voltage	105 – 125 Vac (or 240 Vac)
Output Current	1.5A maximum, each half
Ripple	1 mV/RMS
Overload Protection	Can be overloaded or shorted indefinitely without damage
Remote Sensing	Remote load sensing provided at plug
Regulation	0.05% line, 0.2% load
Operating Temperature	–20°C to +71°C (ambient)

All transistors and diodes are silicon-type semiconductors. Two holes are provided on the case for power supply output adjustment. Table 4-14 shows the power supply input and output pin connections. The HQ power supply provides ±15 Vdc to the AD8-EA and VC8-E modules through a 7008375 cable to a side connector on the module.

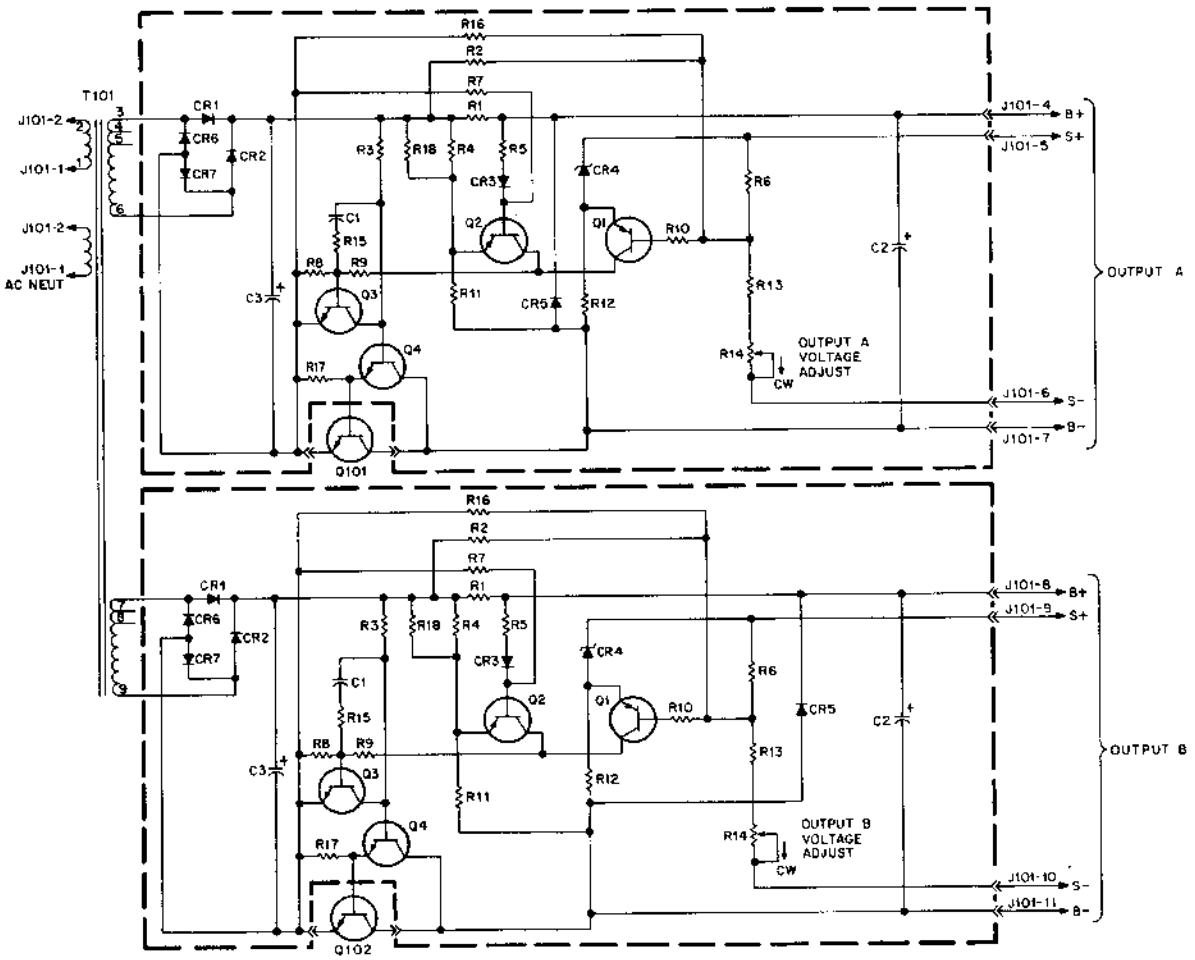
Table 4-14
Side Connector for HQ Power Input and Output

Pin	Color	Signal
1 (Top)	Orange	+15 Vdc
2	Orange	+15V sense
3	Blue	–15 Vdc
4	Blue	–15V sense
5	Black	HQ ground
6	Black	HQ ground
7 (Bottom)	Black	Logic ground

4.7.1 High Quality Power Supply Operation

The High Quality power supply shown in Figure 4-65 provides ±15 Vdc to the LAB-8/E System. The power supply is divided into parts A and B. The A side supplies +15 Vdc and the B side supplies –15 Vdc. The operation of both sides is identical so only the A side will be discussed.

4.7.1.1 Regulator Circuitry – The current-limiting circuitry shown in Figure 4-66 represents components of the regulator circuitry shown in Figure 4-67. Both circuits are part of the HQ power supply shown in Figure 4-65. The components regulate the output voltage. Because B+ and S+ are B– and S– are tied together at the end of the analog power cable (to provide local voltage sensing), they are shown tied together for simplicity.



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BE-0263

Figure 4-65 High Quality Power Supply Schematic

In operation, Q101 (on the outside of the case) is the controlled series-pass element that varies the current, and thus the voltage, applied to the external load (at output A). The voltage sense is proportional to output A, and is compared to Zener reference CR4. A change in voltage sense will alter the base current to Q1, and thus, vary the current through R9. A portion of this current is applied to the base of Q3, amplified, and applied to the base of Q101 via emitter follower Q4. The change in Q4 base current alters the collector current in Q101, and thus, changes the voltage across the load applied at output A.

This feedback action tends to decrease the output current when output A increases, and to increase the output current when the terminal voltage begins to drop. Capacitors C2 and C3 are filtering elements, while diode CR5 prevents negative transients on

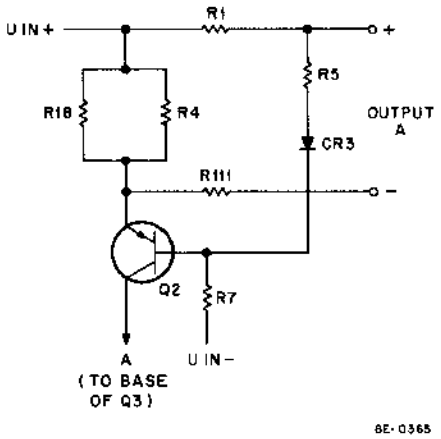

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Figure 4-66 Current Limiting Circuitry

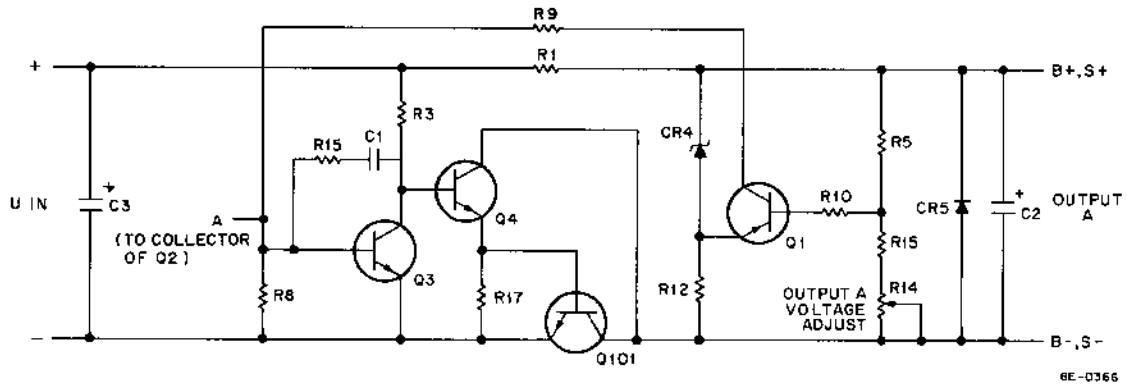


Figure 4-67 Regulator Circuitry

output terminals from damaging external circuitry during power-up. Potentiometer R14 (accessible on the outside of the case) will alter the voltage sense. This varies the nominal power supply output voltage by about 1V. Network R15—C1 gives the device a low-pass characteristic to avoid high-frequency oscillation. Point A is tied to the current-limiting circuit described below.

4.7.1.2 Current-Limiting Circuitry — The current-limiting circuitry (see Figure 4-66) is included to protect the regulator and external circuitry from damage when too much current (1.5A) is supplied to the load. It reduces the output voltage when the voltage-drop across R1 increases (due to increased output current).

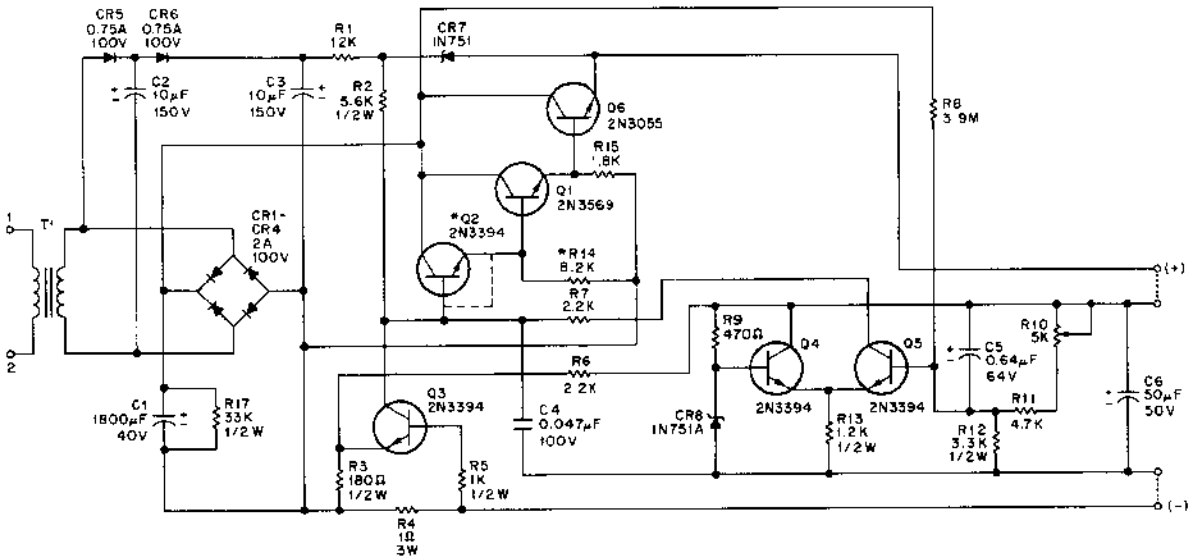
This increased voltage will cause a current to flow from the emitter to the base of Q2, and a collector current to be applied to the base of Q3 (via A). This extra current decreases the base drive of Q101 (see Figure 4-67) via Q4. The smaller base current reduces the output current that the regulator can supply to the overload.

The B— output of the A side of the power supply and the B+ side of the B output are tied to ground. By tying the points to ground, the A output will be +15 HQ power, and the B output will be —15V HQ power. The output of the HQ power supply is tied to side connectors on the AD8-EA or VC8-E and distributed to the other modules by H851 Edge Connectors.

All measurements must be made when the load and sense connections are made by connecting the power supply to the AD8-EA or VC8-E modules. When both modules are installed in the system, the HQ power supply should be connected to the AD8-EA module.

NOTE

The Power Mate (20885-8) or Deltron (C 13495) power supplies may be supplied with the LAB-8/E System. The schematics shown in Figures 4-68 and 4-69 should be used for troubleshooting.



NOTES:
*Jumper used only when Q2 and R14 are not used
Resistors are 1/4 W, unless otherwise indicated.

8E-0393

Figure 4-68 Power Mate (20885-8) HQ Power Supply

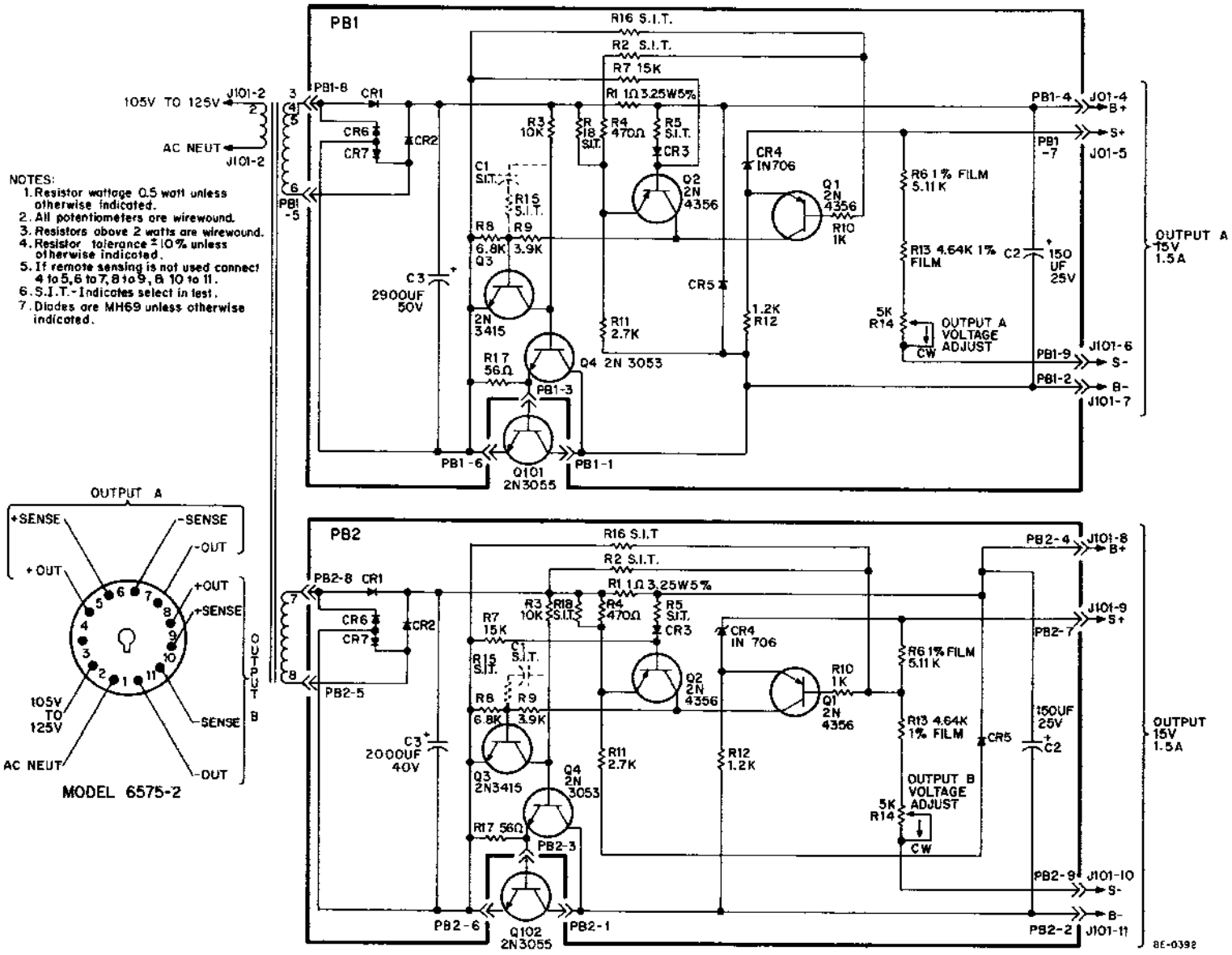


Figure 4-69 Deltron (C13495) HQ Power Supply

CHAPTER 5
MAINTENANCE

This chapter contains information pertinent to preventive maintenance, corrective maintenance, and troubleshooting techniques for the LAB-8/E. The chapter is divided into the following sections:

Section 1 Preparation for Maintenance and Maintenance Requirements

Section 2 Corrective Maintenance

Section 3 Teletype Maintenance

Section 4 System Calibration

Section 5 Preventive Maintenance Procedures

Section 6 Corrective Maintenance

Section 7 Special Troubleshooting Procedures

SECTION 1
PREPARATION FOR MAINTENANCE AND MAINTENANCE REQUIREMENTS

5.1 EQUIPMENT

Table 5-1 lists the equipment and relevant specifications needed for maintenance of the basic LAB-8/E System. Also included in the list is the equivalent equipment used by DEC Field Service personnel.

Table 5-1
Maintenance Equipment

Equipment	Specifications	Equivalent
Precision Voltmeter Multimeter	10 kΩ/V minimum	Triplett Model 310
Oscilloscope	dc to 50 MHz with calibrated deflection factors from 5 mV to 10V/div. Maximum horizontal sweep rate of 0.1 μs/div. Delaying sweep is desirable and dual trace is a necessity.	Tektronix Type 453
Probes	X10 with response characteristics matched to oscilloscope	Tektronix Type P6010
Recessed Probe Tip (2)		Tektronix
Ground Leads (for each probe)		Tektronix
Integrated Circuit Pin Extender	AP Inc	DEC 29-10246
Double-Height Extender (2)		W984
Double-Height, Double-Width Extender Module (2)		W983
DR8-E Diagnostic Jumper Cable		7008418
Edge Connector Extender Cables (2)		BC08M-OM
Light Bulb Extractor		DEC 12-09195
Tool Kit		DEC Type 142
Black Spray Paint		DEC 120-68
White Spray Paint		DEC 120-94
Jumper Wire		30-Guage with TERMI POINT Connections
Silicon Grease		Dow Corning Compound
1/16 in. Allen Wrench		Hunter 4Z 035
Single-Height Extender Module (1)		W980
Precision Voltage Standard		EDC No. MV105G or equivalent

5.1.1 Programs

Table 2-5 in Chapter 2 lists the maintenance programs supplied by DEC for ascertaining proper operation of the LAB-8/E. To supplement these programs, there are five short test routines detailed in the following paragraphs. These routines may be used as needed to perform the required maintenance. Chapter 5 of the *PDP-8/E Maintenance Manual* contains some programs which can be used to check the processor and Teletype.

NOTE

All diagnostics require a programmer's console, a working Teletype, and at least 4K memory with the basic system.

5.1.1.1 Display Line on VR14 or User Oscilloscope

NOTE

The system must have a VR14 to run this program.

Location	Contents	Function
200	6007	Initialize
201	7001	Increment AC
202	6053	Load X
203	6054	Load Y
204	6052	Skip on DONE
205	5204	Jump–1
206	6055	Intensify
207	5201	Jump to beginning

5.1.1.2 Display Converted Value in AC (AD8-EA only or channel 0 of AM8-EA)

Location	Contents	Function
200	6530	Clear all flags (A/D converter)
201	6532	Start A/D conversion
202	6534	Wait for flag
203	5202	Wait for flag
204	6533	Read converted value in AC
205	7000	No operation*
206	7000	No operation*
207	7000	No operation*
210	7000	No operation*
211	7000	No operation*
212	5200	Jump to beginning

*No operations are performed to allow operator to read value displayed in AC or monitor signals on an oscilloscope.

5.1.1.3 Display Converted Value in MQ with AM8-EA

Select channel with switch register 8–11.

Location	Contents	Function
200	6530	Clear all A/D flags
201	7604	Transfer contents of switch register to the AC
202	6531	Transfer contents of AC to MUX Register
203	6532	Start A/D conversion
204	6534	Wait for DONE flag
205	5204	Wait for DONE flag
206	6533	Transfer contents of A/D Buffer (converted value) to the AC
207	7421	Transfer contents of AC to MQ
210	7000	No operation*
211	7000	No operation*
212	7000	No operation*
213	7000	No operation*
214	7000	No operation*
215	5200	Jump to beginning

5.1.1.4 Display Converted Value of A/D on VR14

Choose channel from switch register 8–1, or Auto-Increment all channels with switch register 5 = 1.

Location	Contents	Function
200	6530	Clear all A/D flags
201	7604	Transfer contents of switch register to the AC
202	6531	Transfer contents of AC to MUX Register
203	7604	Transfer contents of switch register to the AC
204	6536	Transfer contents of AC to A/D Enable Register
205	6050	Clear display
206	1250	X axis left-most point
207	3253	X Coordinate Register
210	1251	Total number of points
211	3252	Counter
212	6532	Start A/D converter
213	7200	Clear AC
214	1253	X coordinate
215	6053	Load X Register
216	7001	Increment X
217	3253	Store new X value
220	6534	Skip on A/D DONE = 1
221	5220	Jump–1
222	6533	Read A/D
223	6054	Load Y Register
224	6052	Skip on Display = 1

(continued on next page)

*No operations are performed to allow operator to read displayed value in MQ or monitor signals on an oscilloscope.

Location	Contents	Function
225	5224	Jump Back –1
226	6055	Intensify point
227	2252	Increment count skip after 2000 points
230	5212	Start new A/D conversion
231	5200	Initialize and start again
250	1000	
251	6000	
252	0000	
253	0000	

5.1.1.5 Start A/D Converter with Real-Time Clock

The resulting conversion of the AD8-EA (or channel 0 of AM8-EA) will be displayed in MQ on every clock overflow. Overflow will be generated as set by the switch register every 1 to 4096 ms.

NOTE

The CLOCK START signal monitored at FJ1 on the M860 module, with the switch register set to 7777, is a 100-ns pulse with 1 ms between each pulse. For best results, oscilloscope should be set to 0.2 V/cm and 0.1 μs/cm.

Location	Contents	Function
200	7240	Set AC to 7777
201	6130	Clear Clock Enable Register
202	7200	Clear AC
203	1250	Clock Enable word
204	6132	1 to Clock Enable Logic
205	6530	Clear all A/D flags
206	7200	Clear AC
207	1251	A/D ENABLE word to Enable Register in A/D
210	6536	AC to A/D Enable Register
211	7604	Transfer contents of switch register to the AC
212	6133	Transfer AC to Clock preset
213	6534	Skip on A/D DONE = 1
214	5213	Jump–1
215	6533	Transfer contents of A/D Buffer to AC
216	7421	Transfer contents of AC to MQ
217	5211	Restart
250	1340	
251	0200	

5.1.2 Preventive Maintenance Inspections

Preventive maintenance consists of procedures that are performed prior to the initial operation of the computer, and periodically during its operating life. These procedures include visual inspections, cleaning, mechanical checks, and operational testing. A log should be kept for recording specific data that indicates the performance history and rate of deterioration; such a record can be used to determine the need and time for performing corrective maintenance of the system.

Scheduling of computer usage should always include specific time intervals that are set aside for scheduled maintenance purposes. Careful diagnostic testing can then reveal problems which may only occur intermittently during on-line operation.

5.1.3 Scheduled Maintenance

The LAB-8/E must receive certain routine maintenance attention to ensure maximum life and reliability. Digital Equipment Corporation suggests the schedule defined in Table 5-2.

Table 5-2
Processor Preventive Maintenance Schedule
(3 months or 500 hours)

Type	Action
Cleaning	*a.* Clean the exterior and interior of the computer cabinet, using a vacuum cleaner and/or clean cloths moistened in nonflammable solvent.
	b. Clean the air filters in the processor and the display unit. Use a vacuum cleaner to remove accumulated dirt and dust, or wash with clean hot water and thoroughly dry before using.
	c. Clean face of display unit.
Lubricate	*a.* Lubricate slide mechanisms and casters with a light machine oil or powdered graphite. Wipe off excess oil.
Inspect	*a.* Visually inspect equipment for general condition. Repaint any scratched areas.
	b. Inspect all wiring and cables for cuts, breaks, fraying, wear, deterioration, kinks, strains, and mechanical security. Tape, solder, or replace any defective wiring or cable covering.
	c. Inspect the following for mechanical security: key switches, control knobs, lamps, connectors, transformers, fans, capacitors, etc. Tighten or replace as required.
	d. Inspect all module mounting panels to be sure that each module is securely seated in its connector. Remove and clean any module that may have collected dirt or dust.
	e. Inspect power supply components for leaky capacitors, overheated resistors, etc. Replace any defective components.
	f. Check the output of the H724(A) power supply (see Table 5-8). Use a multimeter to make these measurements without disconnecting the load. If any output voltage is not within tolerance, the supply is considered defective and corrective maintenance should be performed.
Perform	*a.* Run all MAINDEC programs to verify proper computer operation in Table 2-25. Each program should be allowed to run for at least 3 min, or two passes, whichever is longer.
	b. Perform all preventive maintenance operations for each peripheral device included in the LAB-8/E System as directed in the individual maintenance instructions supplied with each peripheral device.
	c. Run the LAB-8/E calibration procedures in Paragraph 5.4, if required.
	d. Enter preventive maintenance results in log book.

5.1.3.1 Weekly Preventive Maintenance Schedule – Time should be scheduled each week to operate the MAINDEC programs as listed in Table 2-25 of Chapter 2. Run each program for a minimum of 3 min. Take any corrective action necessary at this time and log the results. External system cleanliness should also be maintained on a weekly basis.

Computer downtime can be minimized by rigid adherence to a preventive maintenance schedule. Because a dirty air filter can cause machine failure through overheating, all filters should be cleaned periodically. The procedure for filter cleaning is described in Table 5-2.

SECTION 2
CORRECTIVE MAINTENANCE

5.2 MAINTENANCE PROCEDURES

The LAB-8/E is constructed of highly-reliable MSI IC logic modules. Use of these circuits and a minimum amount of preventive maintenance ensures relatively little equipment downtime due to failure. If a malfunction occurs, maintenance personnel should analyze the condition and correct it as indicated in the following paragraphs. A broad-bandwidth oscilloscope, an EDC voltage source, and a multimeter are the only special test equipment required for corrective maintenance. The best corrective maintenance tool is a thorough understanding of the physical and electrical characteristics of the equipment. Persons responsible for maintenance should become thoroughly familiar with the system concept, the logic drawings, the operation of specific IC circuits, and the location of mechanical electrical components.

It is virtually impossible to outline any specific procedures for locating faults within complex digital systems such as the LAB-8/E; however, diagnosis and remedial action for a fault condition can be undertaken logically and systematically in the following phases:

a. Preliminary investigation
b. System troubleshooting
c. Logic troubleshooting
d. Circuit troubleshooting
e. Repairs and replacement
f. Validation tests
g. Log Entry

5.2.1 Preliminary Investigation

Before beginning troubleshooting procedures, explore every possible source of information. Gather all available information from those users who have encountered the problem and check the system log book for any previous reference to the problem. The troubleshooting flowchart (see Figure 5-1) should be used to localize the problem. This flowchart is not a complete guide to determining system fault; it is intended to give the user some thoughts on where a problem could be, possible solution, and how to describe it to the DEC representative before he arrives on site.

Do not attempt to troubleshoot by use of complex system programs alone. Run the MAINDEC programs and select the shortest, simplest program available that exhibits the error conditions. MAINDEC programs are carefully written to include program loops for assistance in system and logic troubleshooting.

5.2.2 System Troubleshooting

When the problem is understood and the proper program is selected, the logical section of the system at fault should be determined. The program that has been selected gives a reasonable idea of what section of the system is failing; however, faults in equipment that transmit or receive information, or improper connection of the system, frequently give indications similar to those caused by computer malfunctions.

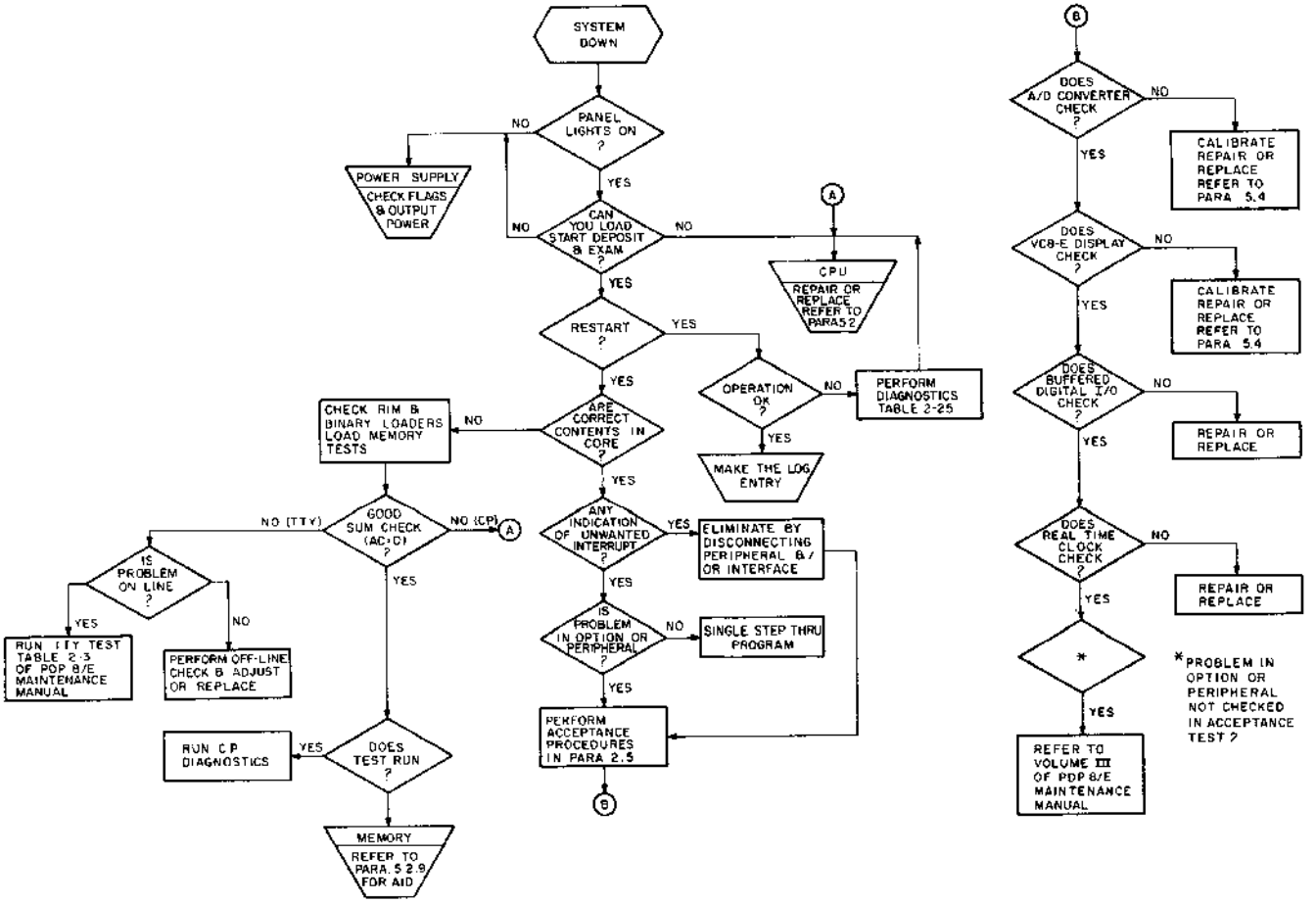


Figure 5-1 System Troubleshooting Flow Chart

Disconnect any peripheral devices that are not necessary to operate the failing program. At this time, reduce the program to its simplest oscilloscope loop and duplicate this loop in a dissimilar portion of memory to verify, for instance, that an operation failure is not dependent on memory location. This process can aid in distinguishing memory failures from processor failures. The techniques described above often pinpoint the problem to a module or several ICs.

5.2.3 Logic Troubleshooting

Before attempting to troubleshoot the logic, make certain that proper and calibrated test equipment is available. Always calibrate the vertical preamplifier and probes of an oscilloscope before using. Make sure the oscilloscope has a good ground via the ac line cord, and keep the ground to the probe as short as possible with the aid of probe ground leads.

To extend the suspected module in the OMNIBUS, perform the following procedure:

Step	Procedure
1	Turn off power.
2	Remove the H851 Edge Connector, if applicable, from the module.
3	Remove the module.
4	Insert two double-extender boards into the same slot.
5	Insert the suspected module into the extender board.
6	If applicable, connect the two edge connector extender cables (BC08M-OM).
7	Turn power on.
8	Use IC pin extender for signal tracing and for grounding the oscilloscope.

NOTE

Test points on individual modules can be observed by connecting the oscilloscope to available pins on the extender.

Use the oscilloscope and IC pin extender to trace signal flow through the suspected logic elements. Oscilloscope sweep can be synchronized by control pulses or by level transitions which are available on individual IC pins at the component side of the module. Exercise care when probing the logic, to prevent shorting between pins. Shorting of signal pins to power supply pins can result in damaged components. Within modules, unused gate inputs are held at +3V.

NOTE

If vibration of the LAB-8/E is desired during troubleshooting, make certain that the vibration amplitude is low enough that inter-module shorts will not occur.

5.2.4 Circuit Troubleshooting

Engineering schematic diagrams of each module are supplied with each LAB-8/E System and should be referred to for detailed circuit information.

Visually inspect the module on the component side and the printed wiring side to check for heated or broken components, or etch. If this inspection fails to reveal the cause of trouble, or to confirm a fault condition observed, use the multimeter to measure resistance of suspected components.

CAUTION

Do not use the lowest or highest resistance ranges of the multimeter when checking semiconductor devices. The X10 range is suggested. Failure to heed this warning may result in damage to components.

Measure the forward and reverse resistances of diodes. Diodes should measure approximately 20Ω forward and more than 1000Ω reverse. If readings in each direction are the same and no parallel paths exist, replace the diode.

Measure the emitter-collector, collector-base, and emitter-base resistances of transistors in both directions. Short circuits between collector and emitter, or an open circuit in the base-emitter path, cause most failures. A good transistor indicates an open circuit in both directions between collector and emitter. Normally 50 to 100Ω exist between the emitter and the base, or between the collector and the base in the forward direction; an open circuit condition exists in the reverse direction. To determine forward and reverse directions, consider a transistor as two diodes connected back-to-back. In this analogy, PNP transistors would have both cathodes connected together to form the base, and both the emitter and collector would assume the function of an anode. In NPN transistors, the base would be a common-anode connection; and both the emitter and collector, the cathode.

Multimeter polarity must be checked before measuring resistance because many meters apply a positive voltage to the common lead when in the resistance mode.

ICs contain complex integrated circuits with only the input, output, and power terminals available; thus, static multimeter testing is limited to continuity checks for shorts between terminals. IC checking is best done under dynamic conditions using a module extender to make terminals readily accessible. Using LAB-8/E logic diagrams and M-series module schematics, locate an IC on a circuit board as follows:

Step	Procedure
1	Hold the module with the handle in your left hand; component side facing you.
2	ICs are numbered starting at the contact side of the board; upper right-hand corner.
3	The numbers increase toward the handle.
4	When a row is complete, the next IC is located in the next row at the contact end of the board (see Figure 5-2).
5	The pins on each IC are located as shown in Figure 5-3.

5.2.5 Repairs and Replacements

When soldering semiconductor devices (transistor, diodes, rectifiers, or integrated circuits) that may be damaged by heat, physical shock, or excessive electrical current, take the following special precautions:

Step	Procedure
1	Use a heat sink, such as a pair of pliers, to grip the lead between the joint and device being soldered.
2	Use a 6V iron with an isolation transformer. Use the smallest iron adequate for the work. Use of an iron without an isolation transformer may result in excessive voltages presented at the iron tip. Use only pencil-pointed tip soldering irons on PC boards.
3	Perform the soldering operation in the shortest possible time to prevent damage to the component and delamination of the etched wiring.

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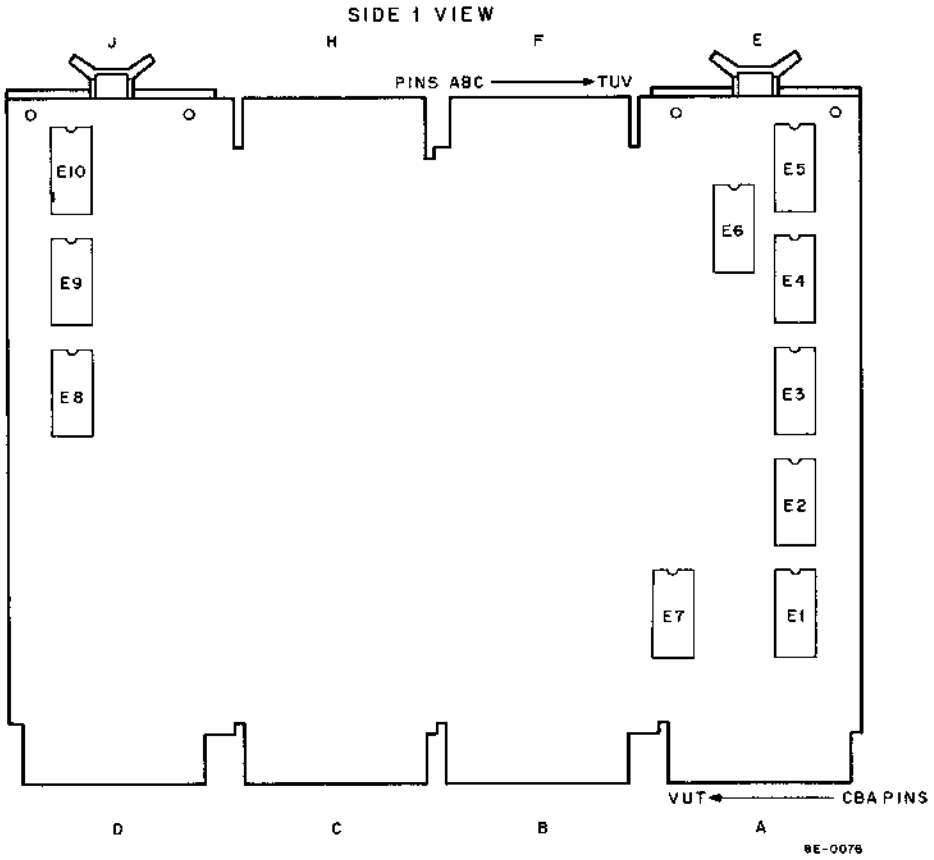


Figure 5-2 IC Location

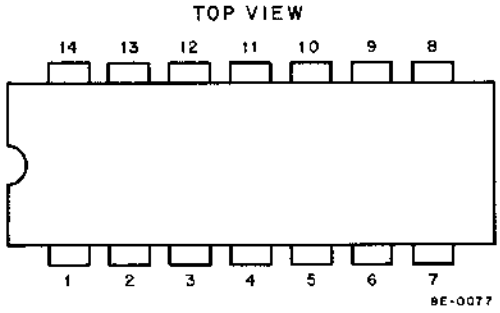


Figure 5-3 IC Pin Location

Step	Procedure
4	An IC may be removed by using a solder puller to remove all excessive solder from contacts and then, by straightening the leads, lift the IC from its terminal points. If it is not desired to save the defective IC for test purposes, perform steps 5 through 6. If the IC is to be saved, perform steps 7 through 12 (remove IC following step 8).
5	Clip IC leads at top of lead at the connection to chip.
6	Remove chip portion of IC.

(continued on next page)

Step	Procedure
7	Apply heat to individual leads from side 1 and remove leads slowly from side 1, using a pair of needle nose pliers. Do not hold lead with pliers while applying heat; the pliers will act as a heat sink.
8	Turn module over to side 2 and heat each hole individually, removing excess solder with desoldering tool.
9	Insert new component, bending appropriate leads. (Only leads with tear drop leads should be bent; they should be bent in the direction of the point.)
10	Clip protruding leads of components from side 2. Do not cut flush with the module. (Leads and solder joints cannot exceed 1/16 in. from bottom of the module.)
11	Solder all leads on side 2.
12	Clean flux from both sides of module with trichlorethylene, freon, or equivalent. Be careful; both substances will damage the plastic handle.

In all soldering and unsoldering operations in the repair and replacement of parts, avoid placing excessive solder or flux on adjacent parts or service lines. When repair has been completed, remove all excess flux by washing junctions with a solvent such as trichlorethylene. Be very careful not to expose painted or plastic surfaces to this solvent.

CAUTION

Never attempt to remove solder from terminal points by heating and rapping module against another surface. This practice can result in module or component damage. Remove solder with a solder-sucking tool or solderwick.

When removing any part of the equipment for repair and replacement, make certain that all leads or wires that are unsoldered, or otherwise disconnected, are legibly tagged or marked for identification with their respective terminals. Replace defective components only with parts of equal or better quality and equal tolerance.

To remove a switch on the programmer's console, follow the procedure below:

Step	Procedure
1	Turn off power.
2	Loosen Allen screw and remove knob from rotary switch.
3	Remove four screws from Bezel.
4	Carefully remove the face plate.
5	Remove two screws retaining aluminum mounting bracket.
6	Remove two wires from tab terminals on the left-hand side of the console.
7	Remove programmer's console board.
8	Remove faulty switch.
9	When replacing the panel, the yellow wire goes to the top tab terminal and the blue wire on the bottom.

To remove the power supply heat-sink assembly (see Paragraph 5.2.10), follow the procedure below:

Step	Procedure
1	Remove ac power by turning off CB1 and disconnecting the ac plug.
	NOTE **If the LAB-8/E is rack-mounted, remove carefully and place on table.**
2	Remove the power supply assembly from the chassis as follows:
	a. Remove five Phillips-head screws. Two are located on the front side of the chassis, one on the rear side, and two on the left side.
	NOTE **If the LAB-8/E is rack-mounted, the chassis tracks and the five mounting screws must be removed.**
	b. Unplug the OMNIBUS power and switch power harness.
	c. Lift up the power supply and slide it back just far enough to remove the blue and the yellow power wires from the front panel.
	d. Lift out the power supply.
3	Remove the protective screen from the side of the power supply by removing the 12 countersunk screws on the screen.
4	Remove the heat-sink assembly as follows:
	a. Remove the nylon plug from the heat-sink assembly bracket.
	b. Remove the six screws from the heat-sink assembly bracket.
	c. Lift out the heat-sink assembly.
5	During replacement, the yellow wire goes to the top tab terminal of the front panel.

5.2.6 Validation Tests

If a defective module is replaced by a new one while repairs are being made, tag the defective module noting the nature of the failure. When repairs are completed, ascertain that the repairs have resolved the problem.

To confirm that repairs have been completed, run all the tests that originally exhibited the problem. If modules have been moved during the troubleshooting period, return all modules to their original positions before running the validation tests.

5.2.7 Log Entry

A log book is supplied with each LAB-8/E System. Corrective maintenance is not complete until all activities are recorded in the log book. Record all data indicating the symptoms given by the fault, the method of fault detection, the component at fault, and any comments that would be helpful in maintaining the equipment in the future.

The log book should be maintained on a daily basis, recording all operator usage and preventive maintenance results.

5.2.8 CPU Troubleshooting

After it is established that the CPU is causing the problem (see Figure 5-1), Table 5-3 can be used as a trouble-shooting aid to isolate the trouble. The symptoms and causes are examples that may help the computer technician find the area in which to look, once an abnormal indication is noted on the programmer's console.

Table 5-3
Processor Troubleshooting

Item	Symptom	Likely Cause	Module
1	A signal on the OMNIBUS is always low.	Bus loads, diode from ground to the OMNIBUS is shorted.	M832
2	Unable to start automatic operations (RUN light always off).	*a.* Missing MEM START, M883, which is a 300- to 500-ns pulse for everytime CONT, DEP, or EXAM key is depressed	KC8/E
		b. POWER NOT OK L delayed, or POWER NOT OK L is true.	
3	Unable to change major states.	Missing CPMA LOAD L. MA, MS LOAD CONT grounded.	M831
4	Unable to modify any memory locations.	*a.* MB LOAD	M831
		b. Memory direction always low	M833
		c. INHIBIT H always low, WRITE stays low	M833
		d. WRITE stays low	M833
		e. SOURCE stays low	M833
		f. FIELD L is high	G104
		(Refer to Table 5-4, Memory Data Errors.)	
5	Data from memory is not getting to the MB.	*a.* Memory direction always high	M833
		b. No MB LOAD	M831
		c. No TIME STROBE	G104
		d. WRITE staying high	M833
		(Refer to Table 5-4, Memory Data Errors.)	
6	When loading an address, the word in the MA is not the same as the switch register.	LA ENABLE is always high (this causes the switch register to be ORed with the AC, MQ, or STATUS if the rotary switch is in one of these positions).	KC8/E
7	When using ADDR LOAD, DEP or EXAM, the MA changes to an incorrect value (EX:0020 ← 0634).	EN0, EN1, EN2, or LEFT, RIGHT, TWICE are incorrect levels. Refer to truth table on M831 logic print, sheet 3 of 3.	M831
8	Depressing ADDR LOAD key will enter all 1's in the MA. By examining and observing the MD, it will be noted that the register will change when the key is released.	DATA T always high.	M831
9	The MA decrements when doing an EXAM or DEPOSIT.	DATA F is always low. Refer to truth table on M831 logic print, sheet 3 of 3.	M831

(continued on next page)

Table 5-3 (Cont)
Processor Troubleshooting

Item	Symptom	Likely Cause	Module
10	When doing an EXAM, DEPOSIT, CONTINUE, or a JUMP instruction, the MA bits 0–4 are zeroed.	PAGE Z is high. (If just one of MA 0–4, check PAGE Z circuit on M830.)	M831 M830
11	CPMA, MB, PC, or AC do not increment.	CARRY IN L is always high to the adder. It should be generated: *a.* During TS1 with DEP, EXAM, or EX TO LOAD depressed. *b.* TS1 of FETCH state. *c.* TS2 of DEFER state. *d.* EXECUTE state and TS2 of an ISZ, or TS3 of a JMS. *e.* TS3 of a group 2 OPR instruction. *f.* If SKIP is set: TS2 of EXECUTE doing a JMS, or TS4 of an MRI.	M831
12	Unable to Skip on an ISZ instruction.	*a.* SKIP flip-flop will not clear. *b.* No carryout. *c.* No overflow.	M831
13	Information being read from Teletype is loading into MA and PC.	C2 is always low, which causes PC LOAD at Bus Strobe (TP3) time instead of AC loading.	M832 M831 M833

When troubleshooting the LAB-8/E, remember that the OMNIBUS is designed so that all pins that are lettered the same are connected to each other, and that a signal can be provided from more than one place. An example is MD06, which is on pins BM1 of all slots of the OMNIBUS. The source of MD06 can come from either the Major Register module (M830) or the Sense/Inhibit module (G104) and is used by five of the nine modules in the basic computer. To find the source and destination of all the signals used in the basic computer, refer to Appendix B.

5.2.9 Memory Troubleshooting

Establish that the memory is the source of the problem through system analysis, using the system troubleshooting flowchart in Figure 5-1, the memory troubleshooting flowchart in Figure 5-4, sheets 1 and 2, and associated troubleshooting Tables 5-4 and 5-5. The waveforms in Figure 5-5 may then be used to isolate the problem.

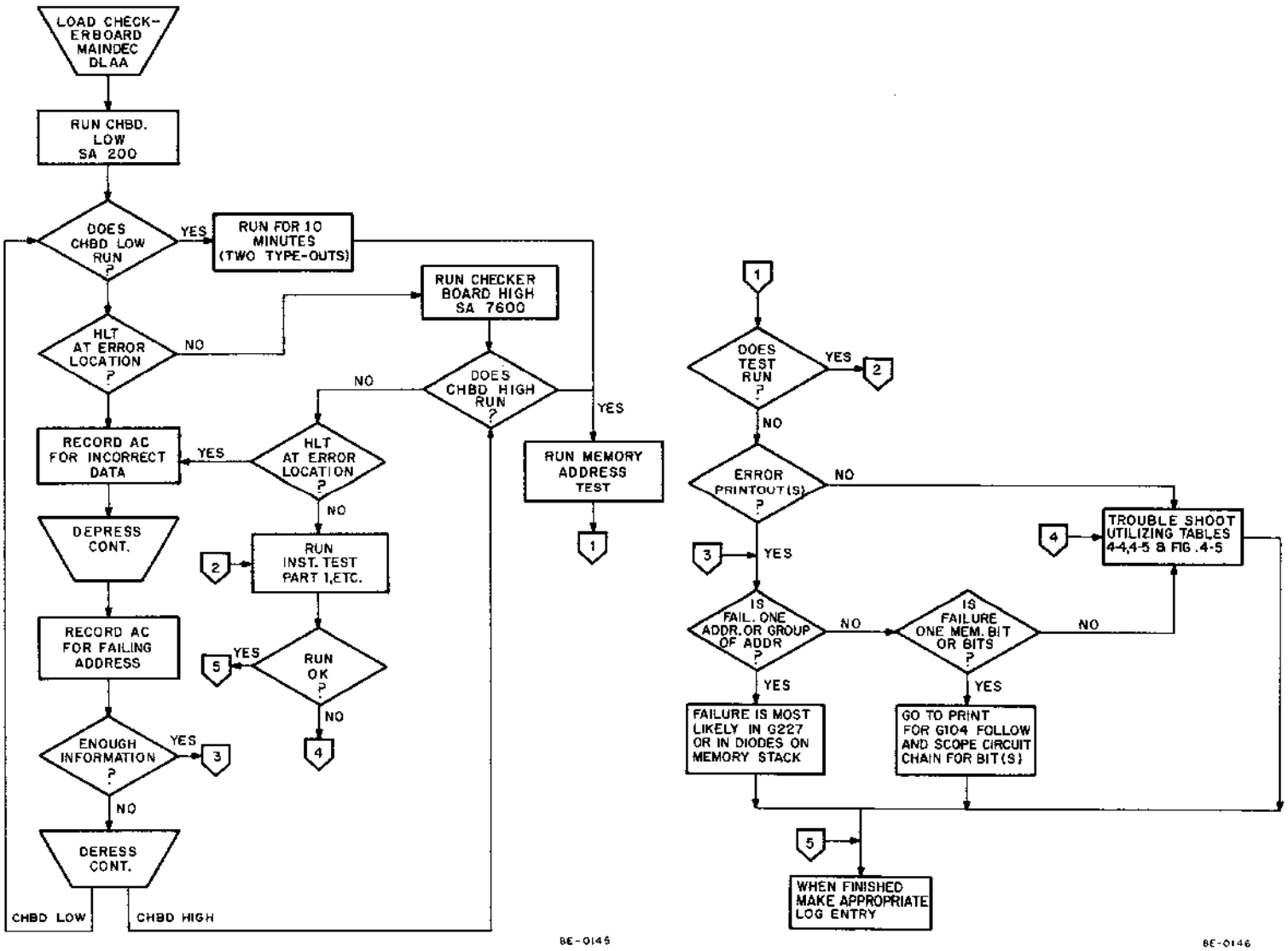


Figure 5-4 Memory Troubleshooting Flowchart

Table 5-4
Memory Data Errors – Possible Causes

Symptom	Cause	Module	Check
One Bit = 1 OR 0	Inhibit Driver	G104	Collector of 2007 transistors
One Bit = 1 OR 0	Sense Amplifier	G104	E31–42 pin 8
Random = 1 OR 0	Time Strobe	G104	E9–3
Random/All = 0	XY current/voltage is low	G227	≈ 5.3V across +5V and pin JU2
Random/All = 1	XY current/voltage is high	G227	Same as above
Random/All = 1	Slice voltage low	G104	≈ 5.3V across gnd and test point DA1
Random/All = 0	Slice voltage high	G104	≈ 5.3V across gnd and test point DA1
Random/All = 1	Inhibit current/voltage low	G227	−15 Vdc power
Random = 0	Inhibit current/voltage high	G227	−15 Vdc power

Table 5-5
Memory Module Test Point Voltage Levels

Signal	Pin	Module	Approximate Readings
Current Control	HA1	G104	1.2V
	HV2	G104	2.3V
Current Source	JU2	G227	1.4V
	FU2	G104	0.25V
Test Point	DA1	G104	−5.3V
Test Point	CB1	G104	6V
Test Point	DB1	G104	−6V
Current Source	HU2	G104	4V
	FA1	G104	2.3V
	FB1	G104	−4V
	Q17 emitter	G104	−4.8V
Memory Stack	Top of thermistor		2.5V
Test Points	Q18 collector	G104	−6V
	Q15, 16 emitter	G104	+3V
	Q13 base	G104	+1.3V

5.2.9.1 Memory Resistance Checks – Some resistance checks that can be performed to aid in isolating a trouble in the memory are summarized below:

Step	Procedure
1	Turn off power.
2	Remove memory stack module.
3	Resistance of thermistor network is approximately 150Ω.
4	Resistance of individual thermistor when out of the circuit is approximately 56Ω.
5	Resistance of winding for one bit is approximately 3Ω (for example, between pins FA and FB for bit 6).

(continued on next page)

Step	Procedure
6	Resistance of diodes FSA2501 is as follows: forward – approximately 24Ω; reverse – approximately greater than 1 MΩ.

CAUTION

Metal can transistors have their casing connected to the collector. Care should be exercised to prevent a ground lead or the back of another module from touching the metal can during troubleshooting.

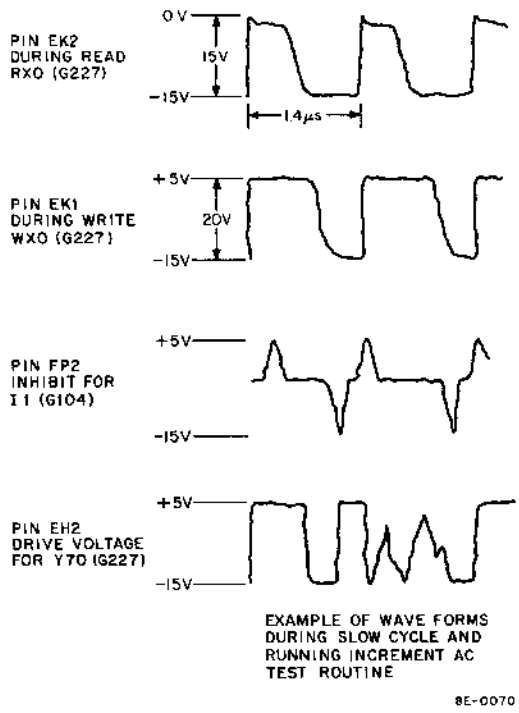


Figure 5-5 Memory Waveforms

5.2.9.2 Memory Circuit Variables – There are a number of variables in the MM8-E memory system, such as current, slice, and field, that have to be set properly. Although some of the settings are permanent for a particular board, interchangeability in the field is assured. These variables are summarized in Table 5-6 and detailed in the following paragraphs.

Table 5-6
Memory Circuit Variables

Variables on MM8-E Memory System	Means for Settings	Location	Who Makes the Settings
Field Select	Three Jumpers: EMA0, EMA1, EMA2	G104	Factory or Field Service
Strobe	6-position rotary switch	G104	Factory or Field Service
Slice	Two Jumpers: SLA, ALB	G104	Factory only
XY Current Control	Two Jumpers: CCA, CCB	G227	Factory only
Temperature Tracking	Thermistor/Resistor Combination R1, R2, R3	G619	Factory only

5.2.9.2.1 Field Select Jumpers – The octal combination of the appropriate cut jumpers represents the selected field; therefore, for the basic system (no extended memory), all jumpers must be in place.

5.2.9.2.2 Strobe Adjustment – A 6-position rotary switch optimizes the strobe positioning in discrete steps of 10 ns. For detailed setting procedures, see Paragraph 5.2.9.7.

5.2.9.2.3 Slice Level – Any variation on the +5V power supply will cause a proportional change of the absolute value of the slice level. The slice level can be set to four different levels according to the following truth table:

Jumpers		Slice Level
SLA	SLB	(Test point DA1 on G104)
In	In	−4.3V
Out	In	−4.8V
In	Out	−5.3V
Out	Out	−6V

CAUTION

Do not field-adjust the slice level under any circumstances.

5.2.9.2.4 XY Current Control (G227) – On the G227 module there are two jumpers in the upper center of the module. These jumpers can be removed and a 24 AWG wire loop soldered in their place, if it is necessary to measure currents with a current probe.

The XY current control can be set to four discrete levels to calibrate the current source. The nominal voltage varies with temperature. Its corresponding XY current is 370 mA, measured on a loop between the XY drive and the stack module. The pertinent truth table follows:

Jumpers		Current Control Voltage
CCA	CCB	(Voltage across +5V and Pin JU2 on G227)
In	In	+3.7V
In	Out	+2.2V
Out	In	(≈ +3.5V at 25°C)
Out	Out	−1.7V

CAUTION

Do not field-adjust current control voltage under any circumstances.

5.2.9.2.5 Temperature Tracking – A thermistor/resistor combination on the memory stack module provides a temperature-sensitive voltage divider that is connected to the current control circuit.

5.2.9.2.6 Inhibit Current – The inhibit current is fixed; however, it varies proportionally to the −15V supply and its corresponding nominal value is 340 mA.

5.2.9.2.7 Strobe Setting Procedure – Setting the strobe properly is very important and must be done carefully. The chosen setting scheme makes this procedure relatively simple. Figure 5-6 illustrates the relationship between the XY current-sense amplifier output and strobe.

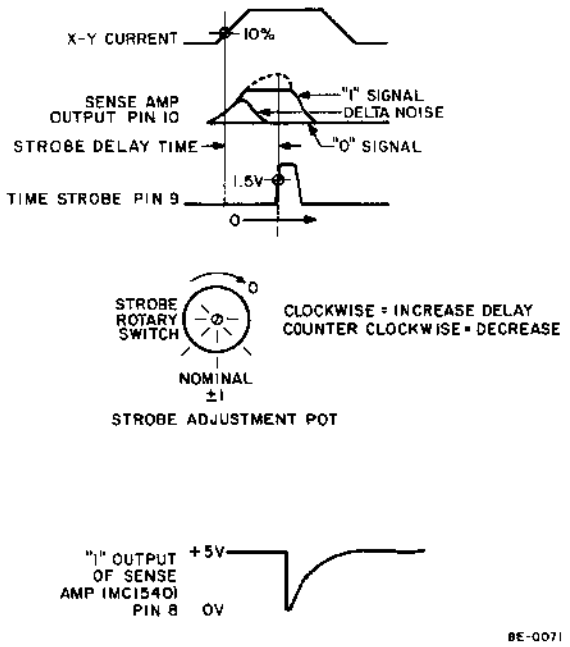


Figure 5-6 Setting of Strobe

It is not advisable to set the strobe timing using an oscilloscope and a current probe. Because of the length of the current probe cables, the bandwidth of the probe and scope may vary in each case. The resulting correlation error can exceed the tolerance allowed, resulting in a misadjusted memory. To set the strobe accurately, perform the following procedure at room temperature:

Step	Procedure
1	The switch has to be set to one of the three possible nominal positions (see Figure 5-6).
2	Load and run Memory Checkerboard maintenance program (MAINDEC-8E-D1AA-D).
3	Program should run without error.
4	Halt program and delay strobe 10 ns (1 position clockwise), then restart.
5	If program still runs without error, proceed to the next position. When errors occur, stop and memorize this strobe position.
6	Repeat the same procedure advancing the strobe (counterclockwise) until errors occur, then stop and memorize this position.
7	A reliable system must have a minimum of three working consecutive positions.
8	Finally, set strobe to the middle working position. If there is an even number of working positions, favor the most delayed (clockwise) of the two center positions.
9	In checkout, Memory Checkerboard should always run in the middle position, and for at least 15 min in the positions to the left and right of middle with no errors.
10	Acceptance is to be run only in the final strobe position.
11	Setting strobe for External Memories, load basic Memory Checkerboard into Extended Fields and proceed to set strobe position according to steps 1 through 10.

5.2.10 H724 Power Supply Troubleshooting Procedures

The H724 power supply provides power for CP logic, memory, bus loads, and the lamps on the programmer's console. If the power supply is established to be the source of the problem through symptom analysis, with the aid of the system troubleshooting chart (see Figure 5-1), voltage checks should be performed. Voltages and tolerances are given in Table 5-7. Component troubleshooting aid, Table 5-8, is included as an aid to isolating and correcting the malfunction.

Table 5-7
H724 Power Supply Parameters

Output Voltage	Wire Color	Minimum Voltage	Maximum Voltage	Tolerance	Current Maximum Rating Ripple
+5V	Red	4.85V	5.15V	±3%	20A, 50 mV pp
−15V	Blue	−14.25V	−15.75V	±5%	8A, 50 mV pp
+15V	Orange	13.5V	16.5V	±10%	1A, 75 mV pp
+8V	Yellow	6V	10V	±26%	2A
dc voltage OK	Gray	3.75V	5V		
Overvoltage Protection			6.5V		
14 Vac				±26%	0.2A
AC INTLK					0.12A

Table 5-8
Component Troubleshooting Aid for H724 Power Supply

Output Voltage	Wire Color	Jack Pin	Fuse	Module	Transistors	Adjustment	Use
+5 Vdc	Red	J3-3 J4-3	25A	A2	Q200 Q201-6	R21	CPU Logic
−15 Vdc	Blue	J3-4 J4-4 J6-3	10A	A1	Q300 Q301 Q304	R5	Memory
+15 Vdc	Orange	J3-5 J4-5	1A	A1	Q100	R5	Bus Loads
+8 Vdc	Yellow	J6-4	25A				Lights
14 Vdc	—	J5-1 J5-3	.5A				Options
Overvoltage Protection				A2			Power Surge
dc voltage OK (3.75)	Gray	J3-6 J4-6		A2		R29 (Factory-Adjustable Only)	Power Loss

NOTE: Static ohmmeter reading of thermistor is approximately 23Ω.

The following paragraphs describe some of the power supply features and characteristics that may aid in isolating the malfunction.

5.2.10.1 Overcurrent Protection – The power supply should not be loaded by more than 175 percent of the rated output current (see Table 5-7).

5.2.10.2 Hold-Up Time – The regulated output voltages under maximum load conditions should remain stable for a minimum of 2 ms after loss of line voltage.

5.2.10.3 Thermal Protection – A thermal switch is in series with the interlock circuit. This switch is located in the forward top section of the power supply. It will disconnect primary power at 90°C ±5°C. The thermal switch must be reset manually if it is tripped.

5.2.10.4 Contact Protection – Contact protection is provided to limit the primary power at the input to the convenience outlet to twice the nominal peak voltage. In addition, protection is provided against a rate of change in the voltage exceeding 10V per second as the solenoid or circuit breaker is opened.

5.2.10.5 Input Switching – The primary power is switched by a 24-Vdc relay, controlled by an interlock circuit. Grounding pin A on the interlock panel will operate the solenoid and apply power to the computer. The solenoid will break both sides of the line.

5.2.10.6 POWER ON/OFF Switch Adjustment – The POWER ON/OFF switch is cam-adjusted according to Table 5-9.

Table 5-9
POWER ON/OFF Switch Adjustment

Power Switch Position	Three Cam-Operated Switches Switch Position	
	Back 2 Switches	Front Switch
OFF	ON	OFF
ON	ON	ON
PANEL LOCK	OFF	ON

5.2.10.7 Parallel Operation – Two or more power supplies must not be wired in parallel to extend the current driving capability.

5.2.10.8 Large Configuration – When more than one box is in the system, the interlock panel is wired so that the front panel power switch of the first box and the thermal cut-out switch of each additional box is in series and will control power to all boxes, though they may be connected to independent primary power sources.

SECTION 3
TELETYPE MAINTENANCE

5.3 INTRODUCTION

This section contains information pertinent to the maintenance of the Teletype and associated control logic. Perform the test routines described in Paragraph 5.1.1 to localize trouble in the Teletype.

5.3.1 Special Tools

Table 5-10 lists the special tools needed for maintenance of the 33 ASR Teletype. All of these items may be obtained from Digital Equipment Corporation or from the Teletype Corporation.

Table 5-10
Teletype Maintenance Tools

Item	Part Number
Set of gauges	117781
Offset screwdriver	94644
Offset screwdriver	94645
Handwheel	161430
Handwheel adapter	181465
Contact adjustment tool	172060
Gauge	180587
Gauge	180588
Gauge	183103
Bending Tool	180993
Extractor	192697
Tweezer	151392
Spring hook (push)	142555
Spring hook (pull)	142554
Screw holder	151384

5.3.2 Programs

The Teletype control test referenced in Table 2-3 of Chapter 2 of the *PDP-8/E Maintenance Manual* serves as an aid in maintaining the 33 ASR Teletype and associated control logic.

SECTION 4
SYSTEM CALIBRATION

5.4 CALIBRATION OF THE LAB-8/E OPTIONS

Once the problem has been pinned down to a specific LAB-8/E option by performing the acceptance test (see Figure 5-1), the calibration procedures should be run for a better indication of the problem. The problem might be only a minor adjustment or a faulty component. The calibration procedures in the following paragraphs will tell you what adjustments to make to correct the problem.

5.4.1 A/D Converter (AD8-EA) Calibration Procedure

The following steps will calibrate the A/D converter and check the analog multiplexer. Paragraph 5.4.1.2 will be performed when the readings obtained are non-linear.

5.4.1.1 Minor Calibration – Perform the following steps for a minor calibration of the AD8-EA:

Step	Procedure
1	Toggle in the following program to display converted value in the AC:

Location	Contents	Function
200	6530	Clear All
201	6532	Start conversion
202	6534	Skip next instruction if A/D DONE = 1
203	5202	Wait for A/D DONE = 1
204	6533	Read into AC
205	2220	Increment and Skip if 0
206	5205	Time delay for reading AC easily
207	5200	Restart

2	Connect the EDC voltage source output as shown in Table 5-11 and Figure 2-7 and allow a 2-min warm up.
3	Run display converted value in AC.
4	Set EDC voltage source to ~~-4.692V.~~ -4.995
5	Adjust -5V reference for ~~7000~~ to ~~7040~~ displayed in AC. 7000-7001
6	Set EDC voltage source to +4.985V.
7	Adjust +5V reference for 0776 to 0777 in AC.
8	Set the EDC voltage source to values shown in Table 5-12 and check the AC readings.

NOTE

If AC readings are non-linear, a major calibration may be required.

Table 5-11
EDC Connection to A841 Module

Signal Input	AM8-ED or AM8-EC Panel	7008533 Cable
+	1	Red to LL
–	2	Black to NN
ground	3	Shield

Table 5-12
EDC Voltage and AC Readings

EDC Voltage	AC Reading
+4.990	0777
+3.750	0600
+2.500	0400
0.000	0000
–2.500	7400
–3.750	7200
–5.000	7000

5.4.1.2 Major Calibration – The following steps will accomplish a major calibration of the A/D converter.

Step	Procedure
1	Turn power off.
2	Mount the A841 on module extender and connect to the A231 control module.
3	Install temporary jumper across split lugs marked SUM JUNCTION and HQ POWER on A841 module.
4	Turn power on and allow equipment to warm up for 20 min.
5	Perform steps 1 and 2 of the minor calibration procedure (see Paragraph 5.4.1.1).
6	Run display converted value in the AC and adjust R60 for 0777–7000 in the AC.
7	Remove jumper from split lugs.
8	Connect EDC voltage source to A841 as shown in Table 5-11 and Figure 2-7.
9	Set EDC voltage source to –4.692V and adjust negative reference to 7037–7040 switching point in the AC.
10	Refer to Table 5-13 and calibrate bits 5, 4, 3, and 012 as follows: *a.* Adjust EDC voltage source to find switching point listed in column 1. *b.* Add +10 mV to negative voltage on EDC voltage source. *c.* Adjust the potentiometer listed in column 3 to the switching point in the AC listed in column 5. *d.* Repeat for other bit positions.
	NOTE **For example, in step *a*, adjust EDC to achieve 7076–7077 switching in AC. If EDC reads 4.397V, reduce to 4.387V and adjust bit 5 potentiometer to 7077–7100 switching point. If bit 5 turns on while trying to read 7076–7077, move it until problem ceases. If any bit does not calibrate properly, set as close as possible, finish the calibration, and attempt the calibration again.**
11	Set EDC voltage source to +4.985V and adjust +5V reference potentiometer to 0776–0777 switching in the AC. If this reading is obtained within ±5 mV, no adjustment is required.
12	Reinstall module in system, allow system to run for 20 min, and check all calibration points. The temperature change might make a minor calibration necessary.

Table 5-13
Major Calibration Voltages and AC Readings

Find Switching Point	Approximate EDC Voltage	Adjust Potentiometer	Approximate EDC Voltage +10 mV	AC Reading
7076–7077	−4.390	Bit 5	−4.380	7077–7100
7176–7177	−3.765	Bit 4	−3.755	7177–7200
7376–7377	−2.515	Bit 3	−2.505	7377–7400
7776–7777	−0.015	Bit 012	−0.005	7777–0000

5.4.2 Common Mode Rejection (CMR) Calibration

If the CMR potentiometer has been moved or the user wishes the CMR to be peaked at a particular frequency, perform the following steps:

NOTE
This calibration is performed for differential operation (with no AM8-EA) only. Jumper W1 must be installed on the A841 module and W2 must be removed.

Step	Procedure
1	Connect a sine wave generator to ± analog input as shown in Figure 5-7.

NOTE
Source output impedance must be less than 20Ω.

2	Monitor AA1 on the A841 module with an oscilloscope.
3	Set sine wave generator to 60 Hz or desired frequency. Signal input should be 3V/rms.
4	Adjust CMR for a minimum signal (nulled) at AA1.

NOTE
If a sine wave generator is not available, pins LL and NN can be jumpered together to allow adjustment of CMR potentiometer for minimum noise signal (nulled) at AA1.

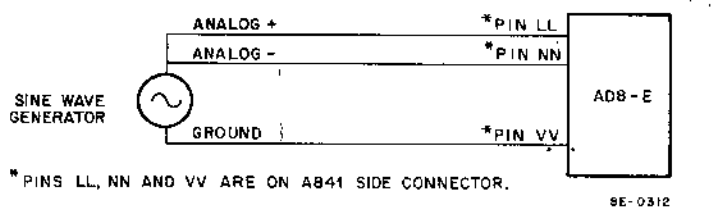


Figure 5-7 AD8-EA Common Mode Rejection Calibration Connection

5.4.3 Calibration of the Point-Plot Display Control (VC8-E) Using VR14 or Tektronix 602 Display

Perform the following steps to calibrate the Point-Plot Display Control using the VR14 or Tektronix 602:

NOTE
The VR14 or Tektronix 602 must be calibrated before performing this procedure. Refer to the calibration procedure for the VR14 in Paragraph 5.4.6.

Step	Procedure
1	Place M885 module on extender modules using a jumper cable from the F connector on the M885 to the F connector on the M869.
2	Place the DVM or the null meter between pin UU (+5V) and pin F (gnd) in the Berg connector located on the M885 module.
3	Adjust R50 (upper right-hand corner on the M885) for 5.120V to ±.002V.
4	Place the DVM or the null meter between pin SS (+5V) and pin F (gnd) on the Berg connector located on the M885 module.
5	Adjust R55 (upper right-hand corner on the M885) for 5.120V ±.002V.
6	Load and start VC8-E diagnostic according to diagnostic write-up.
7	Select TEST 4 of the diagnostic write-up. Use this test to calibrate the X-axis and Y-axis D/A converters as follows:

a. X axis = bit 1 = 0

Type out	Procedure
0000	Place the DVM or null meter between pin D (X output) and pin F (gnd) on the Berg connector. Adjust R86 for 0V ±.002V.
0001 0003 0007 0017 0037	There should be no discernable breaks or overlaps in the line displayed. If there are, a resistor value is incorrect or the diode to +5V reference shorted or opened.
0077	Adjust R29 for no gaps or overlap.
0177	Adjust R34 for no gaps or overlap.
0377	Adjust R38 for no gaps or overlap.
0777	Adjust R42 for no gaps or overlap.
1777	Adjust R46 for no gaps or overlap.

b. Y axis = bit 1 = 1

Type out	Procedure
0000	Place the DVM or null meter between pin L (Y output) and pin F (gnd) on the Berg connector. Adjust R88 for 0V ±.002V.
0001 0003 0007 0017 0037	There should be no discernable breaks or overlaps in the line displayed. If there are, a resistor value is incorrect or the diode to +5V reference shorted or opened.
0077	Adjust R116 for no gaps or overlaps
0177	Adjust R121 for no gaps or overlaps
0377	Adjust R125 for no gaps or overlaps
0777	Adjust R129 for no gaps or overlaps
1777	Adjust R133 for no gaps or overlaps

(continued on next page)

Step	Procedure
8	Select TEST 6. If the image is not within 1/4 in. of the edge of the screen, adjust R55 (gain for Y). There will be an interaction between R55 and R88. This procedure will require readjusting R88 as in step 7 *b*.
9	Select TEST 7. If the image is not within 1/4 in. of the edge of the screen, adjust R50 (gain for X). This procedure will require readjusting R86 as in step 7 *a*.
10	Select TEST 11. A straight diagonal line should be displayed. Check for gaps, overlaps, or steps in the line. If any small inconsistancies are seen, repeat steps 7 *a* and 7 *b*.

5.4.4 VC8-E Calibration Procedure Without a VR14 or VR03

Perform the following steps to calibrate the VC8-E when a VR14 or VR03 is not used:

Step	Procedure
1	Place M885 module on extender boards, and connect the jumper cable from the F connector on the M885 to the F connector on the M869.
2	Place the DVM or the null meter between pin UU (+5V) and pin F (gnd) on the Berg connector located on the M885 module.
3	Adjust R50 (upper right-hand corner on the M885) for 5.120V ±.002V.
4	Place the DVM or the null meter between pin SS (+5V) and pin F (gnd) on the Berg connector on the M885 module.
5	Adjust R55 (upper right-hand corner on the M885) for 5.120V ±.002V.
6	Load and start VC8-E diagnostic according to diagnostic write-up.
7	Select TEST 3. Place the DVM or the null meter between pin D (X output) and pin F (gnd) on the Berg connector on the M885.

NOTE
Voltage readings k1, k2, etc., are taken as a reference for the following step.

a. X axis

Type out	Procedure
0777	Adjust R86 for 5.11V ±.005V.
0776	Read 5.100V ±.005V.
0775	Read 5.090V ±.005V.
0773	Read 5.070V ±.005V.
0767	Read 5.030V ±.005V.
0757	Read 4.950V ±.005V.
0740	Read voltage K1.
0737	Adjust R29 for k1 -10 mV ±.002V.
0700	Read voltage K2.

(continued on next page)

Step	Procedure
7 (cont)	*a.* X axis (cont)

Type out	Procedure
0677	Adjust R34 for k2 -10 mV ±.002V.
0600	Read voltage k3.
0577	Adjust R38 for k3 -10 mV ±.002V.
0400	Read voltage k4.
0377	Adjust R42 for k4 -10 mV ±.002V.
0000	Adjust R86 for 0V ±.002V.
1777	Adjust R46 for -10 mV.

b. Y axis — Place the DVM or null meter between pin L (Y output) and pin F (gnd) on the Berg connector on the M885.

Type out	Procedure
0777	Adjust R88 for 5.110V ±.002V.
0776	Read 5.100V ±.002V.
0775	Read 5.090V ±.002V.
0773	Read 5.070V ±.002V.
0767	Read 5.030V ±.002V.
0757	Read 4.950V ±.002V.
0740	Read voltage k1.
0737	Adjust R116 for k1 -10 mV ±.002V.
0700	Read voltage k2.
0677	Adjust R121 for k2 -10 mV ±.002V.
0600	Read voltage k3.
0577	Adjust R125 for k3 - 10 mV ±.002V.
0400	Read k4.
0377	Adjust R129 for k4 - 10 mV ±.002V.
0000	Adjust R88 for 0V ±.002V.
1777	Adjust R133 for -10 mV.

5.4.5 Analog Preamplifier and Multiplexer (AM8-EA) Calibration Procedure

Perform the following steps to calibrate the preamplifiers in the AM8-EA:

Step	Procedure
1	Load A/D converter (AD8-EA) and Analog Preamplifier and Multiplexer (AM8-EA) diagnostic.
2	Run display converted value in AC test.

(continued on next page)

Step	Procedure
3	Connect EDC voltage source to channel to be checked as shown in Table 5-14.

Table 5-14
AM8-EA Calibration Connections

EDC Output	AM8-EA Input
+ Voltage	+ Channel
− Voltage	− Channel
Ground	Computer Ground

NOTE
Refer to Table 2-2 for pin numbers on all channels

4	Set EDC voltage source to 0V.
5	Read 0000 ±2 counts in AC, if not adjust bias.
6	Set EDC voltage source to +0.9972, adjust gain for channel 00 to 0776–0777 ±2 counts switching point in AC.
7	Set EDC voltage source to −.9991, check for 7000–7001 ±2 counts switching point in AC. If this is out of specification, readjust steps 5 and 6 until all readings are accurate. Refer to Table 2-28 for linearity checking.

NOTE
The gain and bias adjustments are located along the side of the module (see Table 5-15).

8	Repeat steps 1 through 7 for all channels on the AM8-EA.

5.4.6 VR14 Calibration

Perform the following steps to calibrate the VR14:

Step	Procedure
1	Remove signal input cables on the rear of the VR14.
2	Connect a meter between A02A and ground; adjust X position potentiometer for 0V.
3	Connect a meter between A03A and ground; adjust position potentiometer for 0V.
4	Reconnect the signal input cable.
5	Run display in AC test.
6	Connect meter between A02A and ground; adjust X gain for ±2.3V.
7	Connect meter between A03A and ground; adjust Y gain for ±2.3V.

5.4.7 Calibration of the Tektronix 602 Using the VC8-E

Perform the following steps to calibrate the Tektronix 602 oscilloscope.

NOTE
The VC8-E must be calibrated before connecting the Tektronix 602.

Step	Procedure
1	Load VC8-E diagnostic. Follow instructions in the diagnostic document.
2	Load portion of diagnostic that displays a point.
3	When point is displayed in center of oscilloscope, adjust intensity and focus on the Tektronix 602.
4	Adjust intensity and focus until point is in good focus.
5	Load test to display vertical line.
6	Adjust vertical gain and vertical position on the Tektronix 602 until the line spans the front grid.
7	Load test to display horizontal line.
8	Adjust horizontal gain until it spans the horizontal grid.
9	Load ramp test and examine the line for discontinuity and position error.

Table 5-15
Gain and Bias Potentiometers

Channel	Distance from Top	Purpose
00	1	Gain
	2	Bias
01	3	Gain
	4	Bias
02	5	Gain
	6	Bias
03	7	Gain
	8	Bias
04	9	Gain
	10	Bias
05	11	Bias
	12	Gain
06	13	Gain
	14	Bias
07	15	Bias
	16	Gain

SECTION 5
PREVENTIVE MAINTENANCE PROCEDURES

5.5 PREVENTIVE MAINTENANCE

Teletype preventive maintenance should be scheduled every three months.

CAUTION

Do not use alcohol, mineral spirits, or other solvents to clean plastic parts with protective decorative finishes. Normally, a soft, dry cloth should be used to clean parts or subassemblies.

To clean plastic surfaces, we recommend using any household cleaner/waxer liquid. To clean the printer platen, we recommend a lacquer thinner. During an overhaul, subassemblies and metal parts can be cleaned in a bath of trichlorethylene. Proper lubrication should be performed often.

5.5.1 Weekly Tasks

The following procedures should be followed on a weekly basis:

Step	Procedure
1	Inspect platen and paper guides, wipe clean, using a soft, dry cloth.
2	Clean external areas of paper-tape punch and reader, using a soft brush or cloth.
3	Remove and empty the paper-tape punch chad box.
4	Run the Teletype control test for approximately 15 min.

5.5.2 Preventive Maintenance Tasks

Follow the procedure outlined below:

Step	Procedure
1	Inspect platen and paper guides. Clean platen, using a lacquer thinner to remove shiny surface.
2	Clean ribbon guides and replace ribbon, if necessary.
3	Remove cover and check for vibration effects, loose nuts, screws, retaining clips, etc.
4	Clean distributor rotor and clean disk surface, using cotton swab moistened in freon or trichlorethylene.
5	Clean between selector magnet-pole piece and armature with bond paper to remove any lubricant or dirt.
6	Clean and lubricate the Teletype, per Teletype Bulletin 273B. Follow instructions carefully; do not over lubricate.

(continued on next page)

Step	Procedure
7	The following adjustments should be checked. Pages indicated are in Bulletin 273B, Volume 2.

Trip Shaft	574-122-700	Page 13
Trip Lever	574-122-700	Page 14
Brush Holder (Distributor)	674-122-700	Page 15
Clutches	574-122-700	Pages 16–24
Code Bar Reset	574-122-700	Pages 30–34
Print Suppression	574-122-700	Page 35
Blocking Levers	574-122-700	Page 37
Print suppression	574-122-700	Page 43
Carriage Drive Ball	574-122-700	Page 44
Print Trip Lever	574-122-700	Pages 61–62
Dashpotentiometer	574-122-700	Page 78
Final printing alignment	574-122-700	Page 85
Line Feed	574-122-700	Page 89–95
Keyboard Trip Lever	574-122-700	Page 141
Reader Trip Lever	574-122-700	Pages 6–9
Detent Lever	574-124-700	Page 10
Sensing Pin	574-124-700	Page 15
Tape Lid Latch Handle	574-124-700	Page 18
Feed Pawl	574-124-700	Page 11
Registration	574-124-700	Page 12

8	Run each of the Teletype MAINDEC programs; at least two passes each.
9	Check that tape holes are being cleanly punched.

SECTION 6
CORRECTIVE MAINTENANCE

5.6 CORRECTIVE MAINTENANCE PROCEDURES

Details of the cable connector fusing and test points are included in Table 5-16. During off-line operation, the keyboard distributor effectively drives the printer-selector magnet; thus, any character received from the keyboard or paper-tape reader is automatically reproduced on the printer and paper-tape punch. During on-line operation, this continuity is broken and a Teletype receiver (M865) is used to accept the input from the reader or keyboard, while a Teletype transmitter (M865) is used to drive the printer and paper-tape punch.

Table 5-16
Connections of Teletype Cable

33 ASR Connections	W0760 Split Lug	Mate-N-Lok Pin Number	M865 Split Lug	Keyboard	Printer	Reader Advance
		1 (N/C)	0 (N/C)			
*TB pin 6		2	2		X	
TB pin 3		3	3	X		
±15	-Relay	4	4			X
TB pin 7	7	5	5		X	
**To CP (F)	+Relay	6	6			X
TB pin 4	4	7	7	X		
	-30V (N/C)	8 (N/C)	0 (N/C)			

*Terminal board (TB)
**Wheellock Relay Card.

Table 5-17
Teletype Cabling, Fusing, and Test Points

Check	Reader	Receiver	Transmitter
Fuses	1/2A		3, 3/8, 2.5, 3A
Terminal No.	6 and 4	7 and 3	5 and 2
Test Points	DA1 Reader Run	AB1 Receiver Active	1

A crystal clock is used to shift the bits through the transmitter and receiver buffers; therefore, no clock adjustments are required. Most Teletype problems can be traced to one of the following.

a. 33 ASR keyboard or reader

b. 33 ASR printer or punch

c. M865 receiver/transmitter

Isolation of bit-related problems is relatively simple. Off-line duplication can usually determine whether the problem is in the teleprinter or the control logic. Steps may be taken to isolate the problem to subassemblies within the teleprinter. Bit pick-up during a read operation can be caused by a defect in any of three sets of contacts that

are tied in parallel. Reader, keyboard, and answer-back contacts provide parallel inputs to the distributor contact disk. Bit pick-up problems can be isolated to one of these areas by disengaging the related contact from the suspected contact set.

Printer/punch problems can sometimes be isolated by comparing the printed character with the output of the paper-tape punch. If the printed character agrees with the punch output and both are incorrect, then the problem lies in the selector mechanism or in the Teletype receiver/transmitter module (M865). If the printed character disagrees with the paper-tape punch output and the paper-tape punch output is correct, then the problem lies within the printer assembly. Figure 5-8 shows the Teletype signal relationship between the computer and the Teletype.

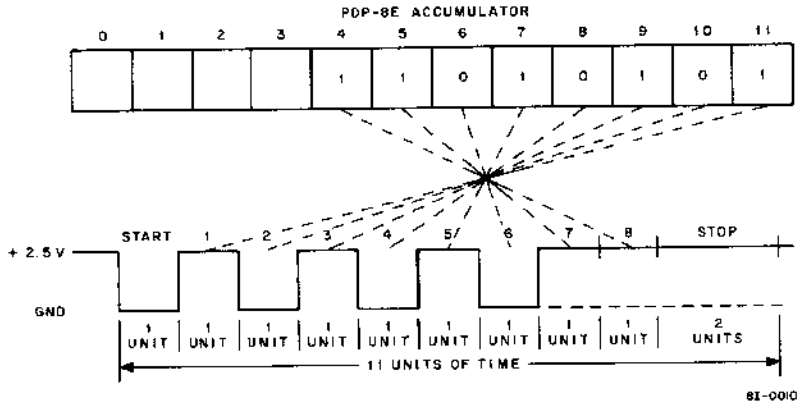


Figure 5-8 Teletype Signal Waveform and Bit Relationship for the Character U

SECTION 7
SPECIAL TROUBLESHOOTING PROCEDURES

5.7 TEST CLOCK (M499)

The Test Clock module serves as a troubleshooting tool for the LAB-8/E when problems within memory prevent the use of troubleshooting programs. The M499 module provides a MEM START signal of 100- to 500-ns width every 15 μs with the DEP or EXAM key depressed. This procedure makes signals available for associated troubleshooting at a continuous rate. Troubleshooting procedures using the M499 Test Clock are as follows:

Step	Procedure
1	Insert M499 into any slot in row A of the OMNIBUS. Refer to Figure 2-6 for open slots.
2	Depress the SING STEP key on the programmer's console.
3	The switch register may now be used in conjunction with the EXAM or DEP key to check manual functions.
4	The EXAM or DEP key may be taped into the depressed position (thus leaving the operator free).

CHAPTER 6
LAB-8/E SYSTEM SPARE PARTS

6.1 INTRODUCTION

This chapter identifies the recommended spare parts for the LAB-8/E System.

It is recommended that those spare parts needed to remove and replace components, in each of the options that make up the LAB-8/E System, be kept in stock at the computer facility to maintain minimum down time. If the user desires, he can purchase modules from DEC to allow removal and replacement at the module level. DEC Field Engineers will have spare modules available, if they are needed.

6.2 LAB-8/E CENTRAL PROCESSOR (PDP-8/E and 33 ASR TELETYPE SPARE PARTS)

The PDP-8/E and 33 ASR Teletype spare parts are listed in Volume I, Chapter 5, of the *PDP-8/E Maintenance Manual.*

6.3 BASIC LAB-8/E SYSTEM SPARE PARTS

The spare parts for each option in the basic LAB-8/E System are identified in Tables 6-1 through 6-5.

Table 6-1
Analog-To-Digital Converter (AD8-EA) Recommended Spare Parts

DEC Part Number	Number Recommended	Description	DEC Part Number	Number Recommended	Description
11-03441	1	Diode 1N756A	19-05547	2	IC 7474
11-01385	1	Diode 1N825	19-05575	1	IC 7400
11-00144	2	Diode D664	19-09004	1	IC 7402
15-09681	1	Transistor 2N5245	19-05579	1	IC 7440
15-09338	1	Transistor DEC 6531	19-09705	1	IC 881
15-09142	1	Transistor 2N4250	19-09485	1	IC 380
15-09090-01	1	Transistor DEC 6B	19-09686	1	IC 7404
15-03100	1	Transistor 3009B	10-09935	1	IC 8235
15-08157	1	Transistor SDA-5S	19-09373	1	IC 9601
15-01881	1	Transistor 2N2219	19-05580	1	IC 7450
19-09928	1	IC 7416	19-09486	1	IC 384
19-09848-03	1	IC BB 3278-2114	19-09704	1	IC 314
19-09761	1	IC 1439	19-09594	1	IC 8251
19-09343	1	IC 302	19-10041	1	IC 74164
19-09004	1	IC 7402			

Table 6-2
Point-Plot Display Control (VC8-E) Spare Parts

DEC Part Number	Number Recommended	Description	DEC Part Number	Number Recommended	Description
15-01881	1	Transistor 2219	19-09594	1	IC 8251
15-03100	1	Transistor 3009B	19-09485	1	IC 380
15-03409	1	Transistor 6534D	19-09373	1	IC 9601
15-05715	1	Transistor 2N4313	19-09058	1	IC 74H21
19-09343	1	IC LM 302	19-09004	1	IC 7402
19-09686	2	IC 7404	19-05575	1	IC 7400
19-94961	1	IC M6 1439	19-05547	1	IC 7474
19-09935	1	IC 8235	D664	1	Diode D664
19-09971	1	IC 6380	IN 825	1	Diode IN825
19-10018	1	IC 74193	IN 752A	1	Diode IN752A
19-09928	1	IC 7416	FD 777	1	Diode FD777
19-09705	1	IC 8881	IN 571	1	Diode IN571
19-09704	1	IC 314			

Table 6-3
Analog Preamplifier and Multiplexer Expander
(AM8-EA) Recommended Spare Parts

DEC Part Number	Number Recommended	Description
11-05508	1	Diode IN823
11-02451	2	Diode IN753
19-09686	1	IC 7404
19-09594	1	IC 8251
19-09344	1	IC MC 1709C
15-09233	1	Transistor 2N5163
15-09142	1	Transistor 2N425
15-03409-01	1	Transistor 6534-B
15-03100	1	Transistor 3009B

Table 6-4
Buffered Digital I/O (DR8-EA) Recommended Spare Parts

DEC Part Number	Number Recommended	Description	DEC Part Number	Number Recommended	Description
11-00114	2	Diode D664	19-09594	1	IC 8251
11-04860	1	Diode IN746A	19-09704	2	IC 7404
19-05547	1	IC 7474	19-09705	1	IC 8881
19-05575	2	IC 7400	19-09928	1	IC 7416
19-09004	2	IC 7402	19-09935	1	IC 7405
19-09485	2	IC 380	19-006735	1	IC 8235

Table 6-5
Real-Time Programmable Clock
(DK8-EP) Recommended Spare Parts

DEC Part Number	Number Recommended	Description
18-09880	1	20 MHz crystal
15-09142	2	Transistor 2N4250
15-03100	2	Transistor DEC 3009B
15-09090-01	2	Transistor DEC 6B
11-00114	2	Diode D664
11-02808	2	Diode IN752A
19-09485	1	IC 380
19-09686	1	IC 7404
19-09705	1	IC 8881
19-09936	1	IC 74151
19-09929	1	IC 7417
19-05575	1	IC 7400
19-05547	2	IC 7474
19-09004	2	IC 7402
19-09051	2	IC 7475
19-05589	1	IC 7470
19-09344	1	IC 1709C
19-09436	1	IC 384
19-09373	1	IC 9601
19-05579	1	IC 7440
19-05577	2	IC 7420
19-05576	2	IC 7410
19-10035	1	IC 74197
19-09594	1	IC 8251
19-09972	1	IC 6314
19-09971	1	IC 6380
19-09934	1	IC 8266

APPENDIX A
IC CIRCUIT DESCRIPTIONS

Only those integrated circuits used in the LAB-8/E which are not discussed in the *PDP-8/E Maintenance Manual* will be covered in this appendix.

A.1 SN 74193 IC

The SN 74193 monolithic circuit is a synchronous, reversible (up/down), 4-bit binary counter having a complexity of 55 equivalent gates. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters. See Figure A-1 for the logic diagram and Figure A-2 for the pin location.

The outputs of the four master/slave flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

The counter is fully programmable; i.e., the outputs may be preset to any state by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs, independently of the count pulses. This feature allows the counters to be used as Modulo-N Dividers by simply modifying the count length with the preset inputs.

A CLEAR input has been provided which forces all outputs to the low level when a high level is applied. The CLEAR function is independent of the count and load inputs. An Input Buffer has been placed on the CLEAR, COUNT, and LOAD inputs to lower the drive requirements to one normalized load. This is important when the output of the driving circuitry is somewhat limited.

This counter was designed to be cascaded without the need for external circuitry. Both BORROW and CARRY outputs are available to cascade both the up- and down-counting functions. The BORROW output produces a pulse equal in width to the COUNT-DOWN input when the counter underflows. Similarly, the CARRY output produces a pulse equal in width to the COUNT UP input when an overflow condition exists. The counters can then be easily cascaded by feeding the BORROW and CARRY outputs to the COUNT-DOWN and COUNT-UP inputs, respectively, of the succeeding counter.

NOTE

Voltage values are with respect to network ground terminal.

A.2 DEC 1709C IC

The DEC 1709C IC is an operational Amplifier. The circuit schematic and the pin locator are shown in Figure A-3.

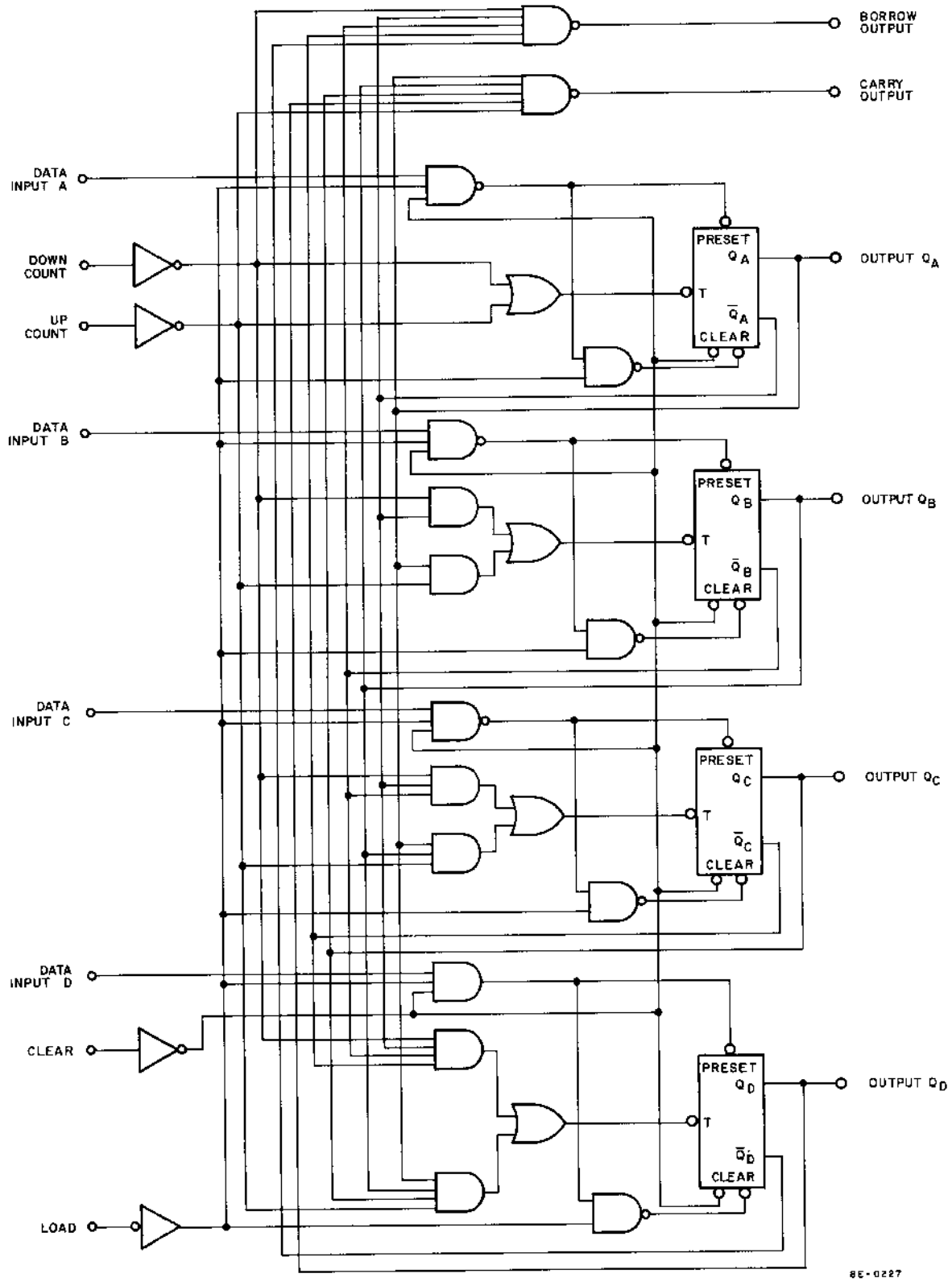


Figure A-1 74193 IC Logic Diagram

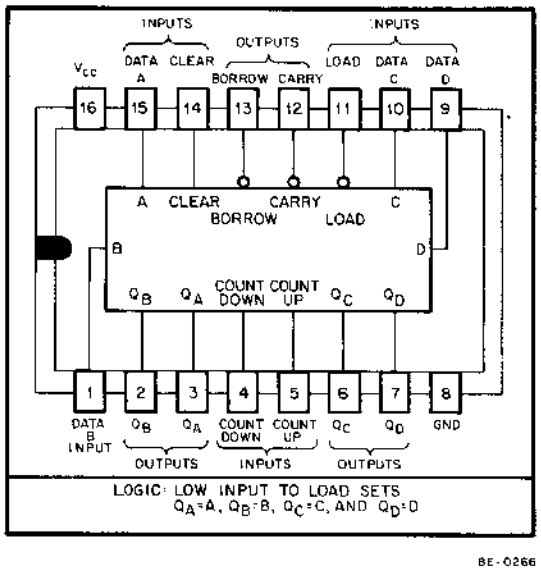


Figure A-2 74193 IC Pin Location (Top View)

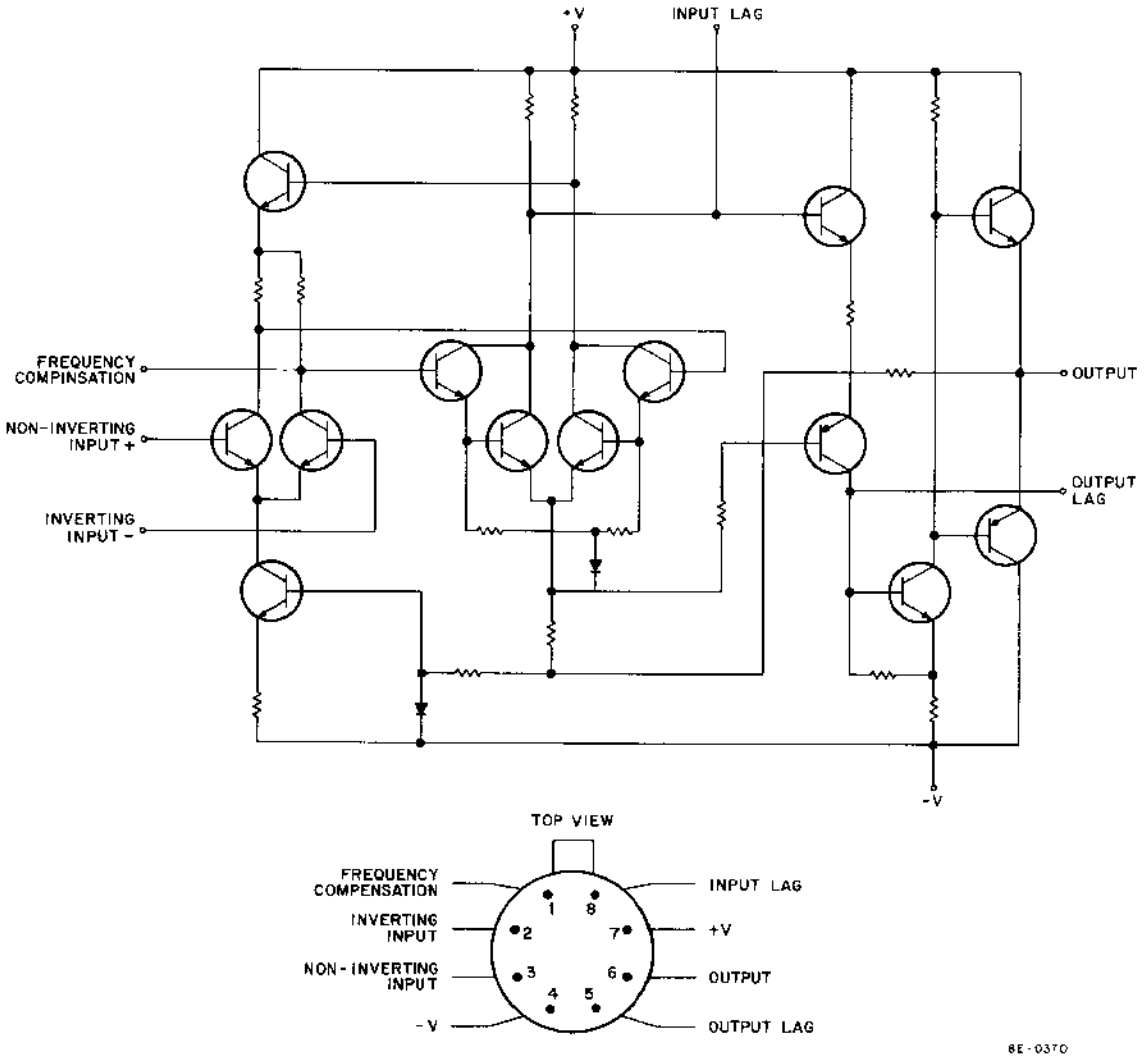


Figure A-3 DEC 1709C IC Illustrations

The IC is designed for general purpose analog amplifier application. In the Real-Time Programmable Clock option, DK8-EP, the 1709C is used as a comparator and, as such, is the central component in the Schmitt trigger circuits on the M518 module. In this application, only half the IC circuitry is used, the output being taken from pin 8 of the IC. As can be seen from the circuit schematic, the output at pin 8 has the same relationship to the summing inputs as does the output at pin 6.

A.3 DEC 7475 IC

The DEC 7475 IC is a 4-bit bi-stable latch. The logic diagrams, a truth table, and a pin locator are shown in Figure A-4.

Information present at the data input (D) of a latch is transferred to the 1 output when the clock input (C) goes high. If the C input remains high, the 1 output follows the D input. When the C input goes low, the 1 output holds the state it was in prior to the transition.

A.4 DEC 7490 IC

The DEC 7490 IC is a high-speed counter consisting of four master/slave flip-flops, connected to provide a divide-by-2 counter and a divide-by-5 counter. The logic diagram, truth tables, and a pin locator are shown in Figure A-5.

The 7490 can be used in three independent counting modes: a divide-by-2/divide-by-5 mode, a divide-by-10 mode, and a BCD-count mode. External interconnections of the IC pins are not necessary in the first mode. An input at pin 14 is divided by 2 by flip-flop A and the result is taken from pin 12; an input at pin 1 is divided by 5 by flip-flops B, C, and D, and the result is taken from pin 11. The output of each flip-flop is made available and all four flip-flops are reset simultaneously, if the gated reset lines are used.

If the divide-by-10 mode is desired, pin 11 must be connected to pin 14. The input at pin 1 is divided by 10 and the output is taken from pin 12. (This mode of operation is used in the Real-Time Programmable Clock option.) The third mode is obtained by connecting pin 1 to pin 12 and applying the input at pin 14; the BCD-count sequence is shown in Truth Table A. The reset inputs are provided to reset a BCD count for 9's complement decimal applications.

A.5 DEC 7470 IC

The DEC 7470 IC is an edge-triggered J-K flip-flop. The logic diagram, pin locator, and the truth table are shown in Figure A-6.

The 7470 features gated inputs and direct CLEAR and PRESET inputs. Input information is transferred to the outputs on the positive edge of the clock pulse. Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse; when the input threshold has been exceeded, the gated inputs are locked out. The PRESET and CLEAR inputs have effect only when the clock input is low.

A.6 DEC 74197 IC

The DEC 74197 IC is a presettable binary counter that can also be used as a latch. The IC consists of four dc-coupled master/slave flip-flops connected to provide a divide-by-2 counter and a divide-by-8 counter. The logic diagram, truth table, and pin locator are shown in Figure A-7.

The 74197 can be used in any one of three modes: the divide-by-2/divide-by-8 mode (requiring no external interconnection of IC pins), the latch mode, and the binary counter mode. If the first mode is used, an input at pin 8 is divided by 2 by flip-flop A and the result is taken from pin 5; an input at pin 6 is divided by 8 by flip-flops B, C,

and D and the result is taken from pin 12. Transfer of information to the outputs takes place on the negative-going (trailing) edge of the clock pulse.

If one wishes to use the latch mode, one must enter data at the four data inputs (pins 4, 10, 3 and 11) and enter a strobe pulse at pin 1. The output pins 5, 9, 2 and 12, respectively, will follow the inputs when pin 11 is low, but will remain unchanged when pin 1 is high and the clock inputs are inactive.

The binary counter mode is used in the Real-Time Programmable Clock option. Pin 5 must be externally connected to pin 6. The clock input is applied at pin 8. The initial count can be preset to any value by placing a low on pin 1 and entering the data on pins 4, 10, 3, and 11. When pin 13 is taken low, all outputs are set low, regardless of the state of the clock inputs.

t_n	$t_{(n+1)}$
D	1
High	High
Low	Low

NOTE: t_n = bit time before C-input transition
$t_{(n+1)}$ = bit time after C-input transition

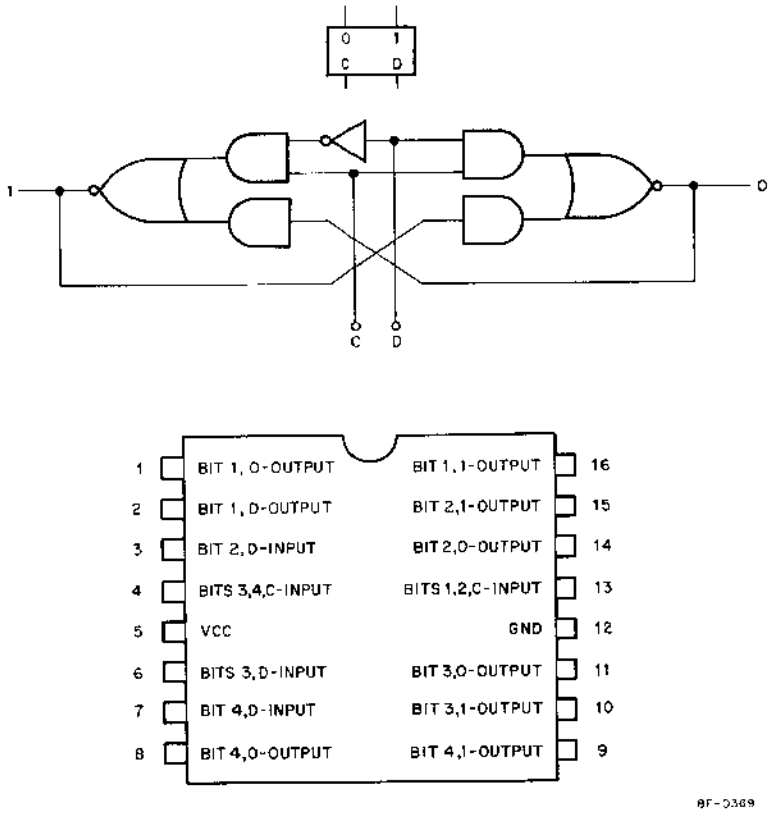


Figure A-4 DEC 7475 IC Illustrations

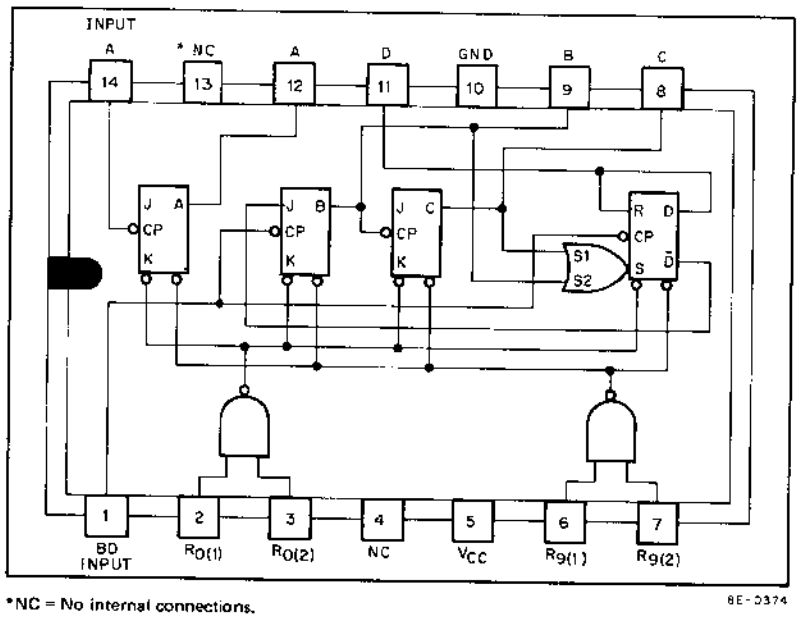
BCD-Count Sequence

	Output			
Count	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET/COUNT

Reset Inputs				Output
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	DCBA
1	1	0	X	0000
1	1	X	0	0000
X	X	1	1	1001
X	0	X	0	COUNT
0	X	0	X	COUNT
0	X	X	0	COUNT
X	0	0	X	COUNT

NOTE: X in table indicates either 1 or 0 may be present.



*NC = No internal connections.

Figure A-5 DEC 7490 IC Illustrations

t_n		t_{n+1}
J	K	Q
0	0	Qn
0	1	0
1	0	1
1	1	Qn

NOTES: 1. t_n = Bit time before clock pulse
2. t_{n+1} = Bit time after clock pulse
3. $J = J_1 \cdot J_2 \cdot J_3$
4. $K = K_1 \cdot K_2 \cdot K_3$

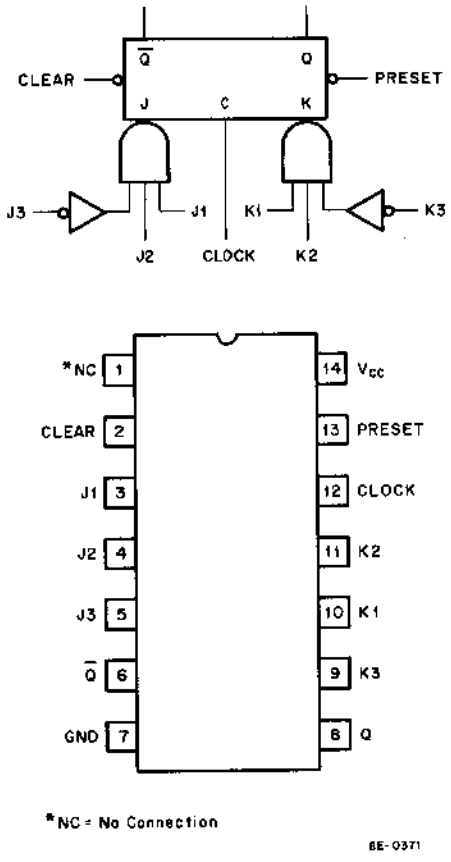
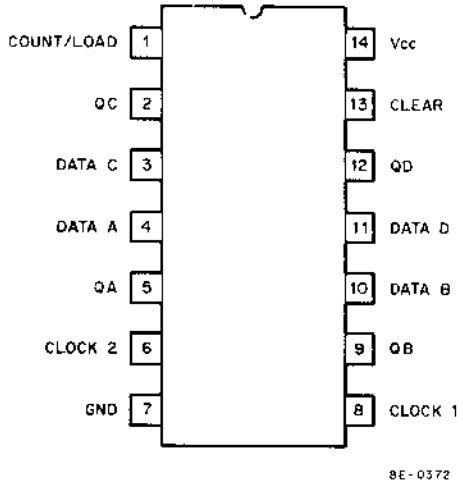


Figure A-6 DEC 7470 IC Illustrations

Count	Output			
Clock 1 Input	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

NOTE: Q_A connected to Clock 2 input.



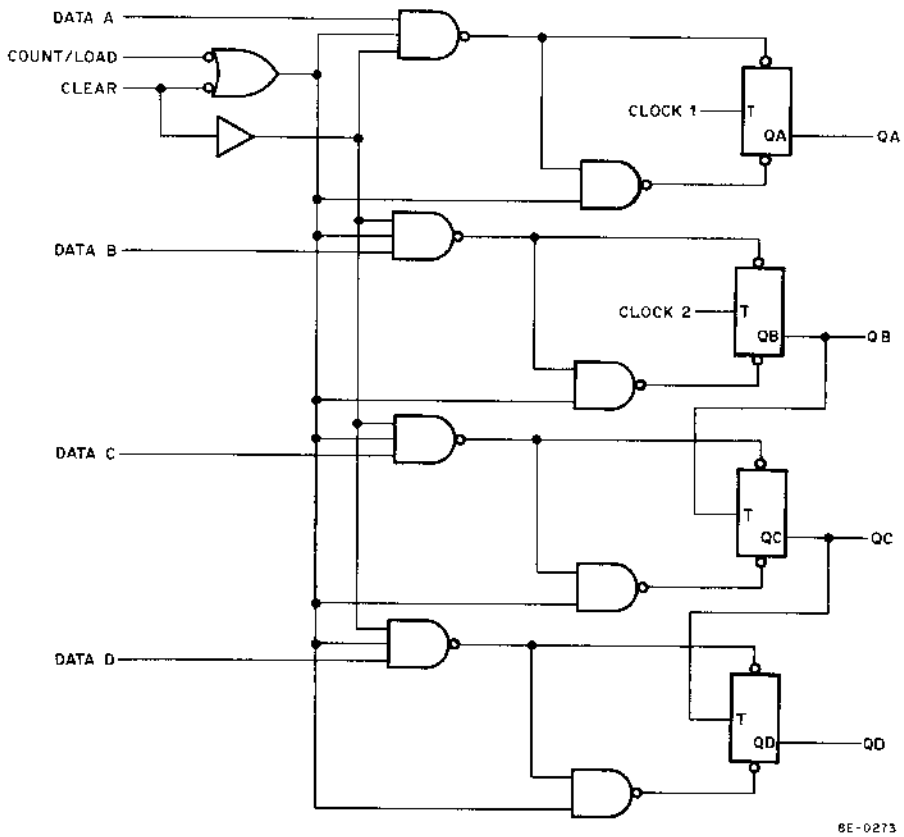


Figure A-7 DEC 74197 IC Illustrations

APPENDIX B
LAB-8/E MODULE JUMPER REQUIREMENTS

Option	Module	Jumper	Function
AD8-EA	A231	W1	Normally installed during system operation. W1 can be removed for troubleshooting if PRESET L is always low or ground.
		W2	Normally installed during system operation. W2 can be removed for troubleshooting to remove DATA OUT H from the comparator circuit. Removal of this jumper disables the A/D converter to allow a bad chip in the A/D Buffer to be located.
		W3	Normally installed during system operation. W3 can be removed for troubleshooting to break the CLEAR L line to the MUX Register flip-flops. Used to isolate bad CLEAR inputs to these chips.
		W4	Normally installed during system operation. W4 can be removed for troubleshooting to break the CLEAR L line to the Enable Register between E20 and E24. W4 is removed to isolate CLEAR inputs on the Enable Register.
		W5	Normally installed during system operation. W5 can be removed to break the BUSY H line to the clock and preset circuits. W5 is removed for module automatic testing only.
	A841	W1	W1 is installed to make the analog input differential. Do not install W1 if an AM8-EA (A232) is installed. On Etch Revision C and below, input pin NN on the Berg connector must be tied to pin MM (ground) when W1 is removed.
		W2	On Etch Revision D and above, W2 will be installed when W1 is removed.
AM8-EA	A232	W1	W1 selects the module as channels 0_8 through 7_8. W2 must not be installed (on Etch Revision D or higher).
		W2	W2 selects the module as channels 10_8 through 17_8. W1 must not be installed (on Etch Revision D or higher).
VC8-E	M869	W1	Installed to select device code (IOT) 05. W2 must be removed.
		W2	Installed to select device code (IOT) 15. W1 must be removed.

(continued on next page)

Option	Module	Jumper	Function
	M885	AB	Installed when the RM503 oscilloscope is used to increase the Z-output voltage. The jumper adjacent to AB must be cut when the AB jumper is installed.
		CD	Used only in special test.
		EF	Used only in special test.
DK8-EP	M518	None	
	M860	None	
DR8-EA	M863	0A through 11A	0A through 11 A select a flip-flop as an edge-detecting input buffer for individual bits 0 through 11.
		0B through 11B	0B through 11B select a direct input (for level-type signal inputs) for individual bits 0 through 11. Either an A or B jumper must be installed in each bit position.
		W1 through W12	W1 through W12 allow individual bits to generate an interrupt when they are set. Inputs must be present in the direct mode (B jumpers) long enough to avoid an unidentified interrupt.
		H6A and H6B through H8A and H8B	These jumpers are used to select the device code (IOT). The A jumpers select 0's and B jumpers select 1's when they are installed.

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