digital

logic handbook

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contents

foreword

This tenth edition of the LOGIC HANDBOOK is your guide to the most extensive line of products offered by Digital Equipment Corporation for implementing electronic logic designs for instrumentation, computer interfacing, data gathering or control. This handbook is a basic reference for anyone involved in specifying, manufacturing or using solid-state logic.

Our M Series TTL-integrated circuit modules are featured throughout this edition. The M Series line consists of more than 100 modules ranging from basic and fundamental logic modules to self-contained computer interfacing modules. The impact of advancing technology can be seen in M Series evolution. From the beginning, M Series was TTL integrated circuit-oriented; the current trend is toward MSI and LSI. The result is more complexity (and more built-in design solutions) per module. Many of the modules in this handbook amount to full-scale digital subsystems.

The microprocessor or "computer-on-a-chip" is the latest result of the continuing technological advancements. As the leading supplier of logic modules, DIGITAL applied this microprocessor concept to a family of modules designated Microprocessor Series (MPS). The major CPU functions are executed by a single-chip, MOS/LSI microprocessor. All input and output lines are TTL levels, thus making the MPS compatible with other M Series modules.

Further versatility has been added to the M Series line by the availability of six prewired Interfacing Kits, described herein. Five of the kits offer the user the capability of implementing more complex input/output interfacing between a PDP-11 computer and peripheral equipment at low cost and minimum design time. The sixth kit provides a convenient method of monitoring analog voltages at a remote location.

An alternative logic design concept has been made available to the designer of digital systems with the availability of RT Modules described in this handbook. These modules, using the Register Transfer concept, minimize design time, reduce documentation, and demand only a fundamental knowledge from the system designer.

This edition of the handbook also covers the K Series of industrial control modules, the A Series of analog modules, the W Series of wire wrappable modules, collage and blank boards in the FLIP CHIP form factor, and a complete line of power supplies, hardware, and cables. All these support support functions provide a total capability for designing, implementing, and assembling a modular system, small or large, at the lowest cost per function in the industry.

The data entry terminals section has been expanded to include the latest in remote data acquisition systems: The PDM70 Programmable Data Mover. Also described are the RT01 Numeric Data Entry Terminal, the RT02-A Alphanumeric Data Entry Terminal, RT02-B Full Keyboard Terminal, RT02-C Badge Reader Terminal, and the recently announced LA36 DECwriter and VT50 DECscope.

Extensive noncatalog products and services are also available from DIGITAL. If you require unique functions that are not listed in this handbook, contact your local DIGITAL office. The product you need may be available as a noncatalog item. In addition, DIGITAL maintains a Special Module Products Group with complete capability of module design, layout, manufacturing and test. Custom product capability is not limited to modules alone but extends to the support hardware and accessories, including cabling, wire wrapping, and cabinets.

A worldwide staff of DIGITAL sales engineers is prepared to respond to your technical and commercial needs. From a backlog of logic system design experience, DIGITAL may have a detailed solution to your application or interface requirement.

Please address any comments on this handbook, or inquiries concerning special services, to:

Digital Equipment Corporation
Components Group
One Iron Way
Marlborough, Massachusetts 01752

Attn: Logic Products
Sales Support Manager

introduction

ORGANIZATION OF HANDBOOK

This edition of the LOGIC HANDBOOK is organized into eight functional sections for maximum ease of reference. Within each section, module descriptions are arranged by categories according to functions. To locate a specific item, consult the Product List at the end of the handbook.

General Purpose Logic and Control: This section includes all of the M Series, A Series, and K Series basic logic modules and those complex functional modules that are not specifically computer-interface oriented. In addition, brief descriptions are provided of earlier modules that are still valid for spares and replacements.

Computer Interfacing: This group includes the M Series complex functional modules that simplify interfacing to the PDP-11 UNIBUS, PDP-8/A, 8/E, 8/F, 8/M OMNIBUS, PDP-12, and PDP-15. Also in this group are the modules for interfacing the external I/O bus of earlier PDP-8 family computers plus level converters and other interface-oriented support modules. Introductory information defines the control and data signals of the OMNIBUS, UNIBUS, and external I/O bus.

DECkits: These kits offer greater interfacing capability to the PDP-11 UNIBUS at the lowest cost possible. Complex logic module building block concepts are now expanded to greater limits of versatility in kit form. Capable of performing a highly complex computer interface, the kit is a collection of logic modules inserted by the user to a prewired system unit.

Microprocessors: Employing state-of-the-art semiconductor technology, DIGITAL's Microprocessor Series consists of a processor module, a read/write memory module, a programmable read-only memory module, and an external event detection module. Other support features, such as an operator's control panel and software routines, are also described in this section.

Register Transfer Modules: Register Transfer (RT) defines the next higher level of computing machine design above sequential and combinatorial logic operations. Digital system design is removed from the realm of the pure logic designer and is made easily achievable by persons such as students, laboratory technicians, researchers, etcs.

RT modules can be operated in 8-bit or 16-bit register configurations; registers may be linked to form words of 24, 32, or higher numbers of bits.

The modules are especially useful at the university teaching level, in experimental, medical, and research laboratories, industrial control, materials handling, and manufacturing.

Data Entry Terminals: This section describes the RT01 and RT02 Data Entry Terminals which provide easy, low-cost access to total information in a computer. They offer ideal communication links in numerous situations that require interactive communication between both local and remote operaters and the central data processor. Featured also is the PDM70 Programmable Data Mover, a complete remote data concentrator and the LA36 DECwriter and VT50 DECscope.

The terminals feature Teletype and EIA serial line compatibility. Interface to a computer is accomplished via a standard full-duplex 4-wire data communications Teletype interface. Standard interfaces are available for the PDP-8, -10, -11, -12, -15, and -16 computers. Modem interface signals corresponding to EIA RS-232C specifications are also provided.

Cables, Power Supplies, Hardware: This section describes a wide selection of prefabricated cables for interconnection of free-standing logic systems as well as computer-based installations. Bulk cables and cable cards are available so that the user can design and construct his own custom interconnections with a minimum of custom design and planning.

A wide selection of dc power supplies for small and large systems is provided here.

DIGITAL makes a complete line of hardware accessories to support its module series. Module connectors are available for as few as one module to as many as 64 in a single 19" mounting panel. A complete line of cabinets is available to house the modules and their connector blocks, as well as provide a convenient means for system expansion. Wiring accessories and a complete selection of support hardware simplify all phases of physical construction. This edition's hardware selection is expanded to include the latest cabinet and hardware features.

Lab Series: This group consists of the COMPUTER LAB digital logic trainer and the DEClab-RT for experimentation and system design of Register Transfer Modules.

general information

SPECIAL SYMBOLS AND ABBREVIATIONS

Logic symbols used in this handbook conform, in general, to widely accepted MIL standards. All basic M Series logic symbols (AND, OR, NAND, NOR, Inverter, Flip-Flop) are described in the introduction to the M Series logic and control modules.

Input Loading and Output Drive

On the logic diagrams of this handbook, input and output loading, expressed in TTL unit loads, appear in boxes terminating each input or output signal line. In the 2-input NAND gate example of Figure 1, both inputs (pins A1 and B1) present one TTL unit load. The output (pin C1) is capable of driving 10 TTL unit loads. The arrows eliminate any possible confusion as to the direction of signal flow.

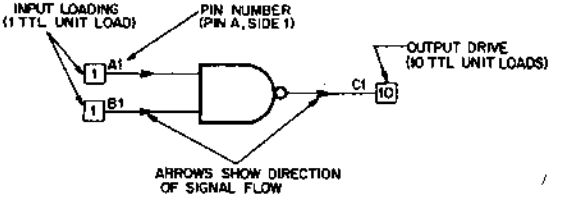


Figure 1. Logic Diagram Input Loading and Output Drive Symbols

Bus Drivers and Receivers

Drivers and receivers that transfer data along the bidirectional transmission lines of the PDP-8/e, 8/m OMNIBUS or the PDP-11 UNIBUS differ somewhat from similar TTL NAND gates or inverters. Typical examples are shown in Figure 2. The "B" in the loading box indicates that the driver or receiver circuit is to be connected to an OMNIBUS or UNIBUS signal or control line. In this application, unit loading need not be considered. "R" identifies a line receiver and "D" identifies a line driver. Inputs to line receivers or drivers may also be standard TTL levels, in which case, TTL unit loads are shown as usual in the loading box.

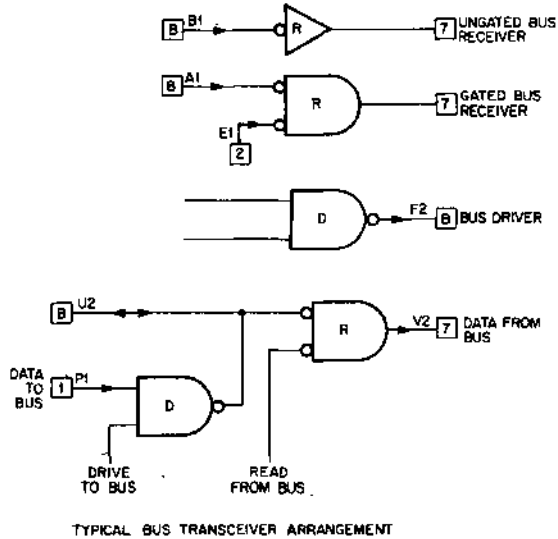


Figure 2. Bus Driver and Receiver Symbols

Electrical characteristics of these circuits are described in the introduction to M Series Computer Interfacing Modules.

Level Converters

Whenever logic levels are translated from one set of voltages to another, the conversion is shown taking place in a square level-converter symbol. Inside the box, the corresponding logic levels are related in a simple truth table. The example of Figure 3 shows a level converter stage that accepts TTL levels (LOW and HIGH) and delivers DEC negative voltage levels (—3 V and ground).

Input loading is two TTL unit loads. Whenever loading is peculiar, it is defined in a note on the drawing as in the output of Figure 3.

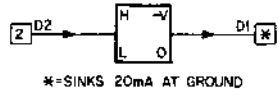


Figure 3. Typical Level Converter

Special Analog Symbols

Symbols used on analog circuit drawings to represent multiplex switches and operational amplifiers are shown in Figure 4. Loading boxes for analog inputs and outputs contain the letter "A"; do not connect such signals to logic levels.

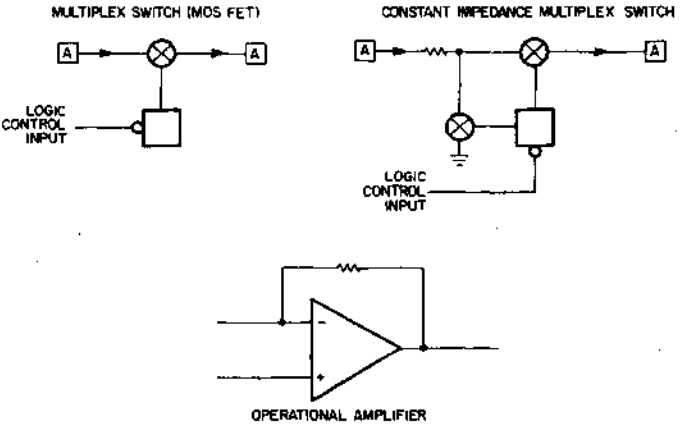


Figure 4. Special Analog Symbols

Signal and Function Names

Inputs and outputs of M Series logic modules may be assigned a signal name, a function name, or both. (See Figure 5.) Signal names appear outside blocks or logic symbols to identify typical input or output signals.

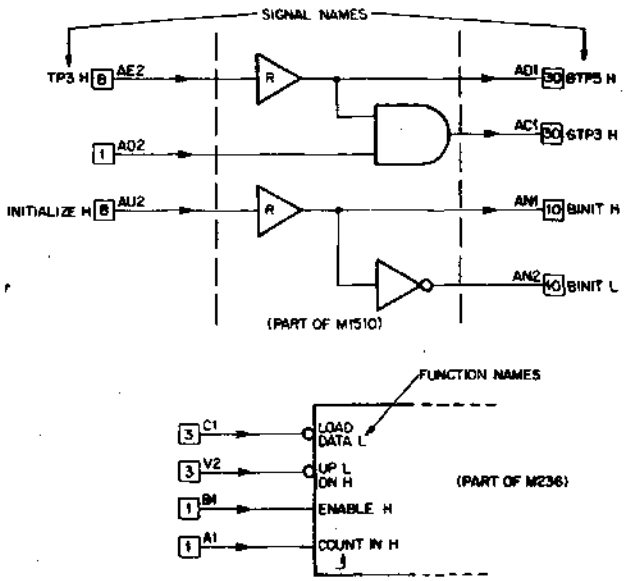


Figure 5. Signal and Function Names

Digital Equipment Corporation uses standard terminology to name signal lines to aid the reader in determining their active state. Either an H or L follows the signal name mnemonic, separated by a space. This letter indicates the asserted (true) state of the signal. An H means the signal is asserted when HIGH (+3 V) and an L means the signal is asserted when LOW (0 V). For example, a UNIBUS data line is called BUS D00 L and a grant line is called BUS BG4 H.

On the logic diagrams of many computer interfacing modules in this handbook, signal names peculiar to one computer, such as the PDP-11, appear as an example of typical usage. Signal names may be changed to those of another computer or interfacing device if logically appropriate.

Function names appear *inside* the blocks of functional modules. They identify the *function* of input or output signals. The user may add his own signal names.

Abbreviations

Abbreviations used in signal and function names in this handbook are defined in Table 1.

Table 1—Abbreviations

ABBREVIATIONS	DEFINITION
ALTN	Alternate
AMPL	Amplifier
ANLG	Analog
BPS	Bits Per Second
CAP	Capacitor
CLR	Clear
CMPR	Compare
COM	Common
CONT	Control
CVRSN	Conversion
DAC	Digital to Analog Converter
EXT	External
GND	Ground
H	High (TTL +3 V Logic Level)
INIT	Initialize
INT, INTR	Interrupt
INTL	Internal
L	Low (TTL 0 V Logic Level)
OUT	Output
P.I.	Program Interrupt
POT	Potentiometer
PRGM	Program
REF	Reference
RTN	Return
SER	Serial
S.H.	Sample and Hold
TRIG	Trigger

MODULE CONTACT FINGER AND MODULE CONNECTOR BLOCK CONTACT IDENTIFICATION

DIGITAL plug-in (FLIP CHIP) modules have contact fingers either on one side (single-sided modules) or on both sides (double-sided modules). Modules with contact fingers on only one side always have them on side 2 (the solder side) (Figures 6, 7, and 8). DIGITAL module connector blocks have module slots with contacts either on one or on both sides. Modules with contact fingers on only one side can be plugged into connector blocks with contacts on both sides of the module slots; then electrical contact between the module and the connector block is only via module slot side 2 contacts. The module contact fingers and connector block contacts are identified by alphanumeric codes. These alphanumeric codes are used throughout this handbook, the HARDWARE ACCESSORIES CATALOG, the PERIPHERALS HANDBOOK, individual module data sheets, engineering drawings, and other DIGITAL publications. This coded numbering scheme must be understood to ensure proper system interconnections (Figures 6, 7, and 8). Letters G, I, O, and Q are not used in this numbering scheme.

DIGITAL modules are SINGLE-HEIGHT, DOUBLE-HEIGHT, or QUAD-HEIGHT; STANDARD LENGTH or EXTENDED LENGTH; and SINGLE-WIDTH or DOUBLE-WIDTH (Figures 6, 7, and 8). Each DIGITAL module is a specific, fixed size; the size of each module is stated in the module description in the previously mentioned DIGITAL publications. DIGITAL SINGLE-HEIGHT and DOUBLE-HEIGHT modules are STANDARD LENGTH or EXTENDED LENGTH. DIGITAL QUAD-HEIGHT modules are always EXTENDED LENGTH. Any DIGITAL module can be SINGLE-WIDTH or DOUBLE-WIDTH; most, however, are SINGLE-WIDTH.

The height and length requirement is determined by the quantity and size of discrete components and integrated circuits located on side 1 of the module, and, to some extent, by the amount of etched printed circuitry on sides 1 and 2. The width requirement is determined by the distance the largest component extends from its mounting surface on the module.

All DIGITAL module connector blocks accommodate any height (standard or double) module. The length of the modules to be used in a logic system must, however, be considered when connector block mounting drawers, system unit mounting drawers, or cabinets are being selected; enough space must be provided to accommodate the longest module. DIGITAL's STANDARD-LENGTH modules are 5.40/5.60 in. (13.72/14.22 cm) long and EXTENDED-LENGTH modules are 8.84/9.04 in. (22.58/22.96 cm) long from the bottom of the contact fingers to the top of the attached handle(s).

All DIGITAL module connector blocks accommodate any width (single or double) module. The width of the module must be considered, however, when any connector block module slot is occupied by a DOUBLE-WIDTH module; this is because no module can be inserted into the module slot on the immediate right on the same connector block unless that connector block provides sufficient space between module slots for the mounted components, i.e., an H808 Module Connector Block. DIGITAL's SINGLE-WIDTH modules require 0.338/0.348 in. (0.859/0.884 cm) for conductive components and 0.370/0.380 in. (0.940/0.965 cm) for nonconductive components. DOUBLE-WIDTH modules require 0.820/0.839 in. (2.106/2.131 cm) for conductive components and 0.870/0.880 in. (2.210/2.235 cm) for nonconductive components. These component space requirements are the distance from the module's side 1 surface to the side 2 surface of the module mounted on the immediate right. Normal module spacing is on half-inch centers.

Some DIGITAL module connector blocks accommodate only SINGLE-HEIGHT modules and others accept either SINGLE-HEIGHT or DOUBLE-HEIGHT modules. No single connector block can accommodate QUAD-HEIGHT modules; QUAD-HEIGHT modules must be mounted in mounting frames, system units, or module drawers comprising module connector blocks with slotted ends so that four module slots are arranged end to end (i.e., at least two H863 or H8030 Module Connector Blocks mounted end to end). SINGLE-HEIGHT modules are 2.417/2.452 in. (6.139/6.228 cm) high, DOUBLE-HEIGHT modules are 5.167/5.202 in. (13.124/13.213 cm) high, and QUAD-HEIGHT modules are 10.437/10.472 in. (26.510/26.599 cm) high (Figure 9).

SINGLE-HEIGHT modules (standard length and extended length) may be plugged into the upper (row A, C, or E) or lower (row B, D, or F) module slot of a connector block (Figure 9). Contact fingers A1 through V1 are on side 1 (component side) of the module, and contact fingers A2 through V2 are on side (solder side) of the module (Figure 6).

DOUBLE-HEIGHT modules (standard length and extended length) have two plug-in sections of contact fingers and occupy two module slots (rows A and B, C and D, or E and F) of a connector block (Figure 9). The two plug-in sections are identified by the designations A and B. Contact fingers A1 through V1 and A2 through V2 of the A section are designated AA1 through AV1 and AA2 through AV2, respectively; contact fingers A1 through V1 and A2 through V2 of the B section are designated BA1 through BV1 and BA2 through BV2, respectively (Figure 7). Note that the positioning notch in the module base must mate with the protrusion on the connector block for correct positioning.

QUAD-HEIGHT modules (always extended length) have four plug-in sections of contact fingers and occupy four module slots (rows A through D or C through F) of two connector blocks (Figure 9). The four plug-in sections are identified by the designations A, B, C, and D. The four sections of contact fingers are designated AA1 through AV1 and AA2 through AV2; BA1 through BV1 and BA2 through BV2; CA1 through CV1 and CA2 through CV2; and DA1 through DV1 and DA2 through DV2 (Figure 8).

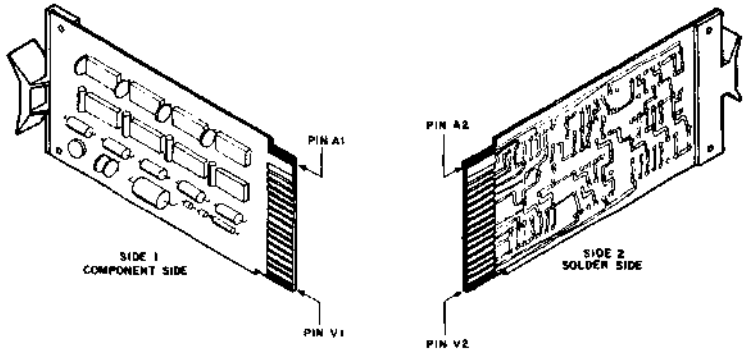


Figure 6. Single-Height Module

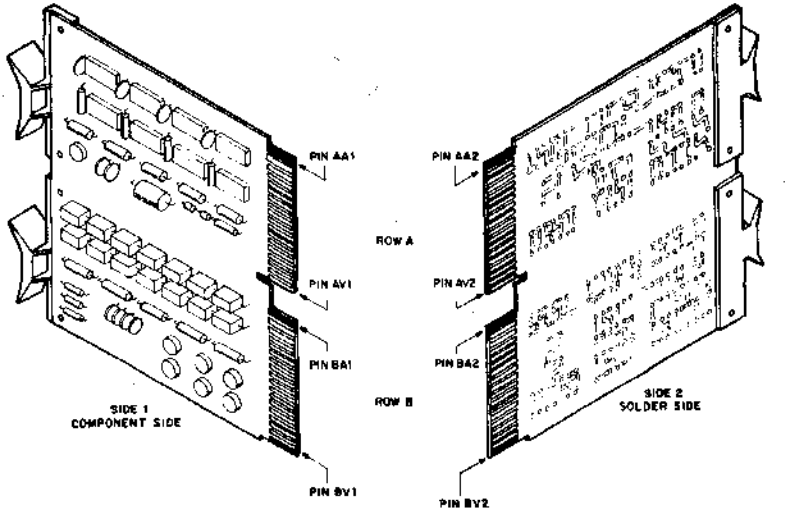


Figure 7. Double-Height Module

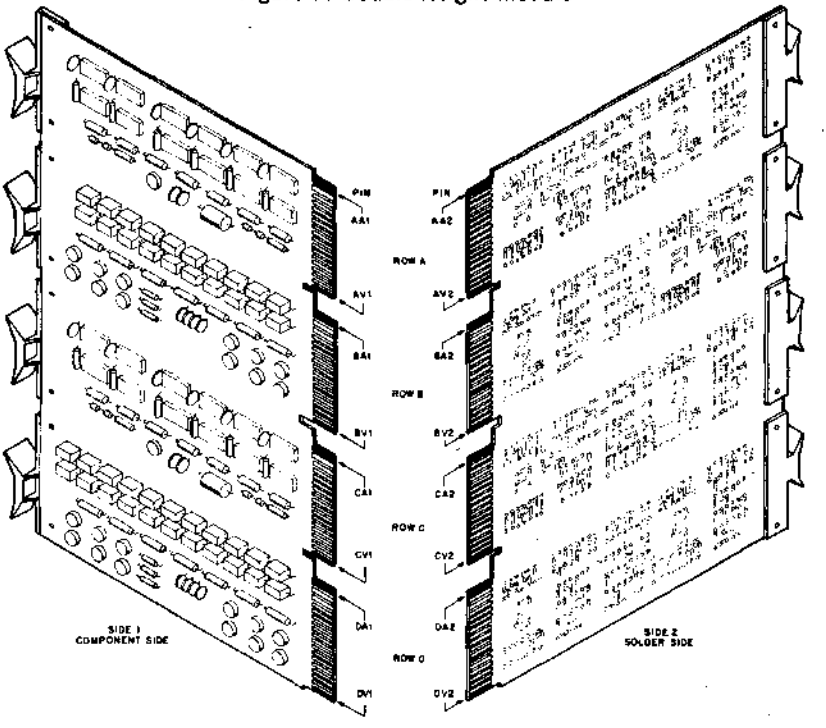


Figure 8. Quad-Height Module

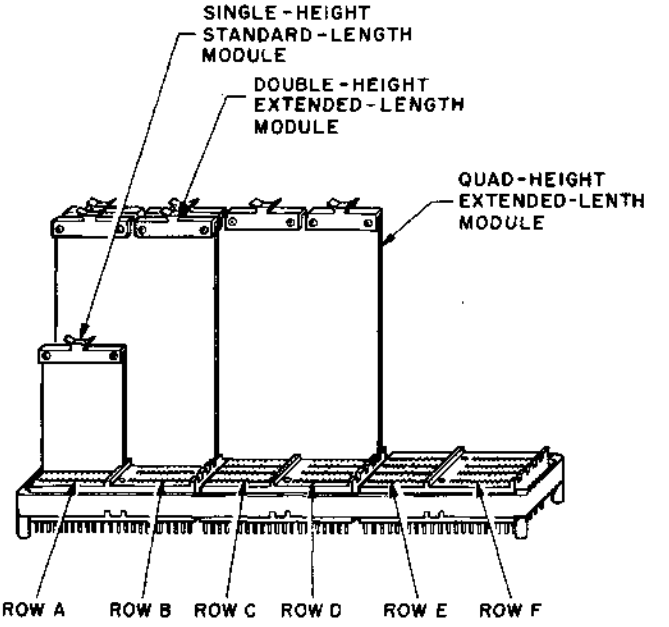


Figure 9. Connector Block Slot Identification

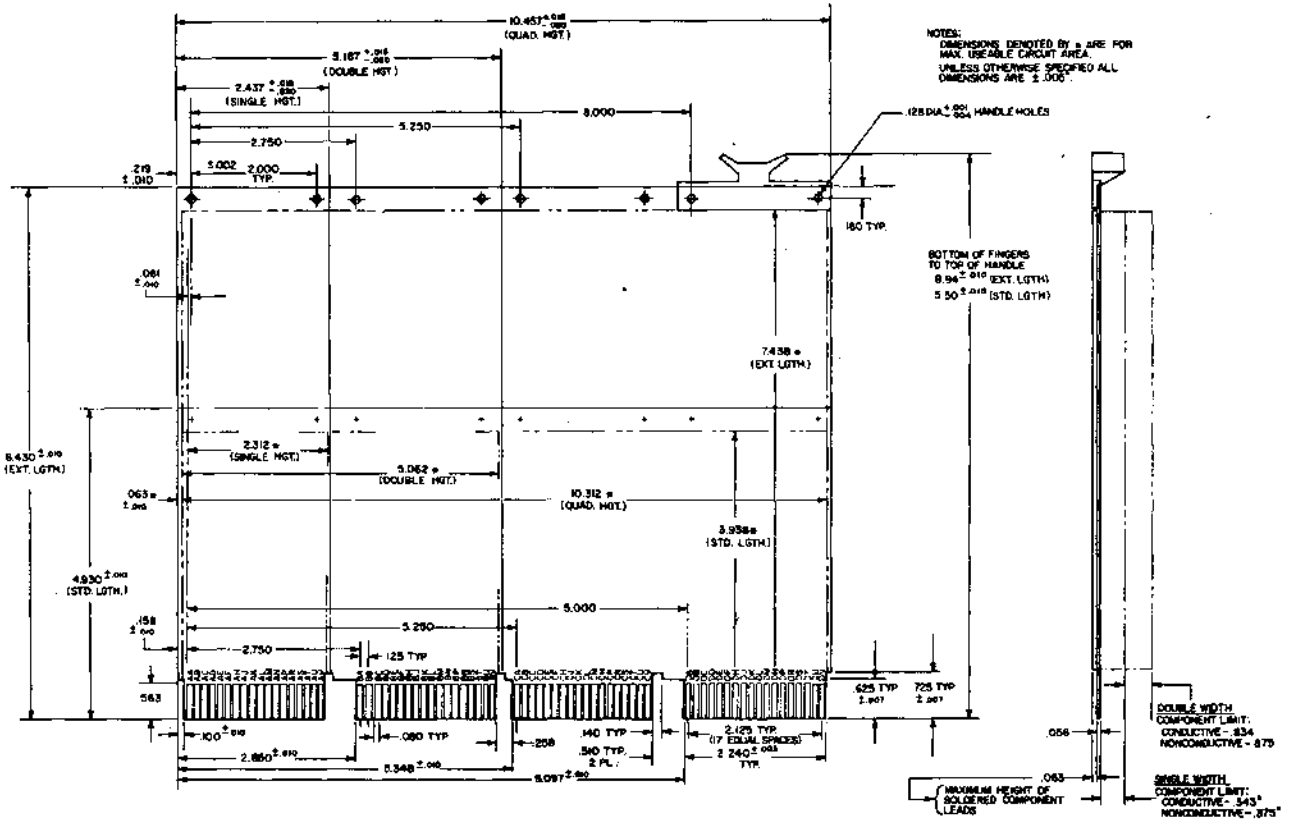


Figure 10. Module Dimensions

RELATED LITERATURE

Listed below are DIGITAL documents that supplement the material provided in this handbook. These documents are available from the nearest DEC Sales Office.

- HARDWARE/ACCESSORIES CATALOG
- PDP-11 PERIPHERALS HANDBOOK
- PDP-8/E, 8/F, 8/M SMALL COMPUTER HANDBOOK

MODULE CLEANING

Occasionally, modules which have been in service for a long period of time may develop resistive coatings on their gold-plated fingers. This coating, if allowed to build up, can cause malfunctions by decreasing the noise margin of a circuit.

There are two types of foreign material coatings which can develop on the gold-plated fingers of a module. The first type is INORGANIC. This type of contamination results when copper "bleeds" through the gold plating and oxidizes. This oxidized layer builds up and can create contact resistances of significant consequence. Inorganic contamination is strictly a matter of time; however, extremely dirty environments will speed up the process. For this reason, care should be taken to locate modules and systems in an area as free from smoke, pollution, and other air-bound particles as possible.

The second form of contamination involves ORGANIC substances, which usually are a result of careless handling, and are mainly made up of fingerprints, salts, and oils deposited when the modules are handled by the gold-plated fingers. Contamination by organic substances can be greatly reduced by careful handling of the modules.

Although the backplane connectors are of the self-cleaning type, it may become necessary to clean the module fingers to ensure reliable connection. When it has been determined that the module fingers are in need of cleaning, the following procedure is recommended.

Inorganic Contaminants

Immerse the fingers of the module in an ultrasonic bath of deionized water and a detergent, such as Liguinyx, for at least 30 seconds. Repeat with pure deionized water only.

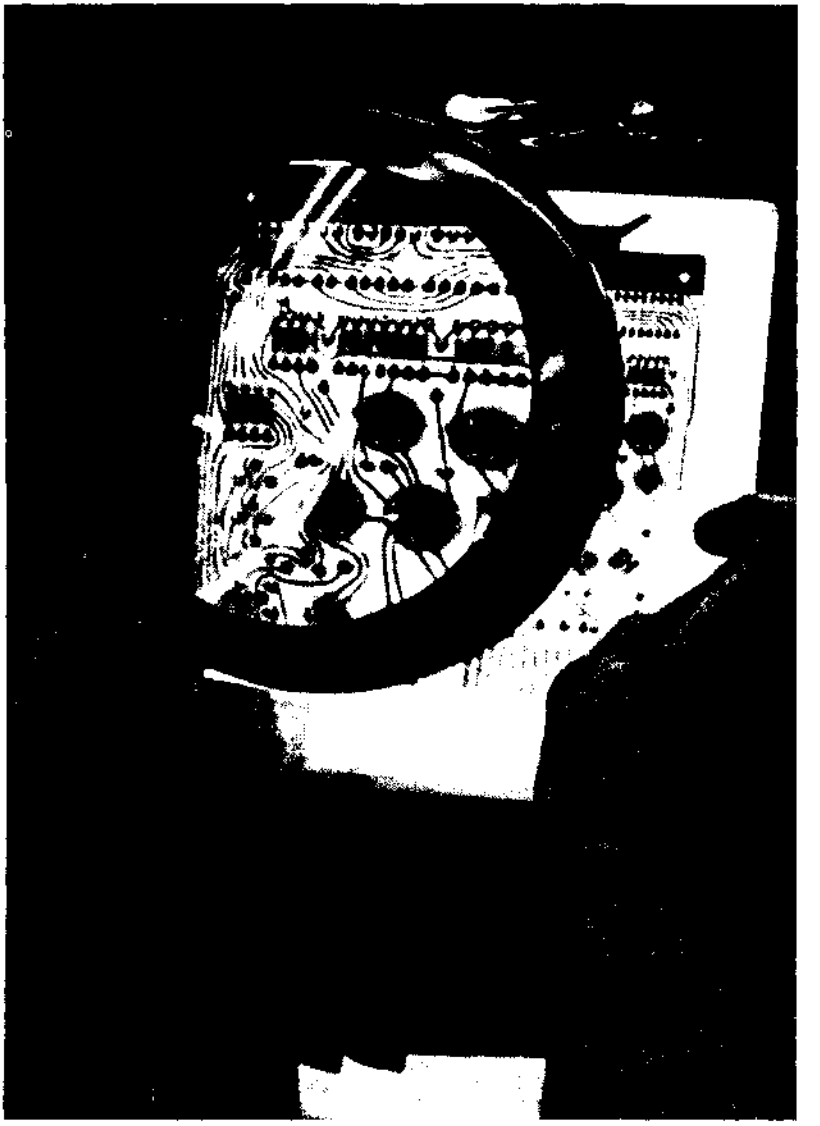
It is now necessary to remove the water from the module fingers. This should be done immediately following the ultrasonic rinse since water will damage the module fingers if allowed to remain. The water can be removed by immersing the module fingers in an ethand or methanol bath to the same depth used during the ultrasonic cleaning. Never wipe or use an abrasive cleaner on the module fingers. If wiping is necessary, the use of K-Dry is recommended.

Organic Contaminants

After inorganic contaminants and water have been removed, organic materials may be removed by immersion of the module fingers in trichloroethane for at least 30 seconds. The fingers can then be allowed to dry or may be wiped clean with a very fine, non-abrasive material such as K-Dry towels. In no case should an eraser ever be used on module fingers. The use of abrasive cleaners or erasers on modules will be considered physical abuse to the module and may void the module warranty.

general purpose

logic and control modules



DEC Module assembly lines combine automated manufacturing steps with visual inspection and computer controlled testing.

GENERAL PURPOSE LOGIC AND CONTROL MODULES

This section describes the computer industry's most extensive line of general purpose logic modules—modules used in DIGITAL's products and modules used by thousands of customers for computer interfacing, instrumentation, data gathering, and control. The module descriptions are organized into three main subsections: M Series, A Series, and K Series. In addition, a fourth subsection briefly describes earlier versions of selected M, W, R, and B Series modules.

M Series high-speed monolithic integrated circuit logic modules employ TTL (transistor-transistor logic) circuits which provide high speed, high fanout, large capacitance drive capability, and excellent noise margins.

The M Series includes a full digital system complement of basic modules which are designed with sufficient margin for reliable system operation at frequencies up to 6 mHz. Specific modules may be operated at frequencies up to 10 mHz. The integrated circuits are dual in-line packages.

In addition to the reduced cost of integrated circuits, DIGITAL's advanced manufacturing methods and computer-controlled module testing have resulted in considerable production cost savings, reflected in the low price of all M Series modules.

M Series modules are compatible with DIGITAL's K Series and, through the use of level converters, are compatible with all of DIGITAL's standard negative-voltage FLIP CHIP modules.

A Series analog modules support the M Series by providing a two-way translation between continually varying real-world voltage measurements and the digital realm of control and computation. The A Series emphasizes 10- and 12-bit performance in a family of mutually compatible functions—multiplexers, operational amplifiers, sample-and-hold circuits, D/A and A/D converters, reference voltage sources, and an expanded group of multiplying D/A converters.

K Series modules have been specially designed for the industrial environment to replace mechanical relay logic. They are extremely noise-immune and reliable, allowing optimum combinations of solid-state logic to be applied to industrial control applications.

The upper frequency range of the K Series modules is 100 kHz, with provision for reduction to 5 kHz for maximum noise immunity. These modules incorporate all-silicon diodes, transistors, and integrated circuits, deliberately slowed through the use of discrete components.

Either English (noninverting) logic or NAND/NOR logic is compatible with K Series. The hardware for this series is specifically designed for standard NEMA enclosures. FLIP CHIP mounting hardware can likewise be used for rack-mounting, since K Series modules fit standard FLIP CHIP module connectors.

The associated hardware for these general purpose modules, such as module connector blocks, mounting panels, cabinets, and power supplies, is summarized elsewhere in this handbook and described in detail in the Hardware/Accessories Catalog, also published by DIGITAL.

M SERIES
GENERAL CHARACTERISTICS

M Series high-speed, monolithic integrated circuit logic modules employ TTL (transistor-transistor logic) integrated circuits which provide high speed, high fan out, large capacitance drive capability and excellent noise margins. The M Series includes a full digital system complement of basic modules which are designed with sufficient margin for reliable system operation at frequencies up to 6 MHz. Specific modules may be operated at frequencies up to 10 MHz. The integrated circuits are dual in-line packages.

The M Series printed circuit boards are identical in size to the standard FLIP CHIP™ modules. The printed circuit board material is double-sided providing 36-pins in a single height module. Mounting panels (H910 and H911) and 36-pin sockets (H803 and H808) are available for use with M Series modules. Additional information concerning applicable hardware may be found in the Power Supply & Hardware and Accessories section of this handbook.

M Series modules are compatible with Digital's K Series and, through the use of level converters, are compatible with all of Digital's other standard negative voltage logic FLIP CHIP® modules.

TTL NAND GATE

The basic gate of the M Series is a TTL NAND GATE. Figure 1 is the basic two input NAND gate schematic diagram. The circuit is divided into 3 major sections, the multiple emitter input, the phase splitter and the totem pole output circuit. The two diode model of a transistor shown in Figure 2 will be used in the analysis of the circuit. A forward biased silicon junction (i.e. diode) gives a voltage drop of about 0.75 volts and a saturated silicon transistor has a collector emitter voltage of 0.4 volts average. These two figures will be used throughout the following discussion.

With either input at the LO logic level (0.0V-0.8V) the multiple emitter input transistor will be ON with its base residing at about $0.75 + 0.4 = 1.15$ volts. The three diode string consisting of Q_1's base collector diode, Q_2's base emitter diode, and Q_4's base emitter diode will have only 1.15 volts across it and will therefore be conducting only leakage currents ($0.75 + 0.75 + 0.75 =$ 2.25 volts required for forward bias). With no current flowing into the base emitter junction of Q_2, the transistor will be OFF and its collector emitter voltage is alowed to rise. Similarly with no current flowing in the base emitter diode of Q_4 the transistor is OFF and its collector emitter voltage is allowed to rise. When both Q_2 and Q_4 are OFF, Q_3 is freed to pull the output voltage to a HI level. The voltage levels present in the circuit with one or more LO inputs is shown in Figure 4.

If both inputs are HI (2.4-3.6 volts) the head of the three diode string will reside at about 2.25 volts and there will be a current path from the 4K base resistor on the input transistor through the diode string to ground as shown in Figure 5. With current flowing in the base emitter junctions of both Q_2 and Q_4, both transistors will be turned ON. Q_3 is held OFF whenever Q_2 is ON. The output is driven LO (0.0V-0.4V) by transistor Q_4. The voltage levels present in the circuit with both inputs HI and are shown in Figure 6.

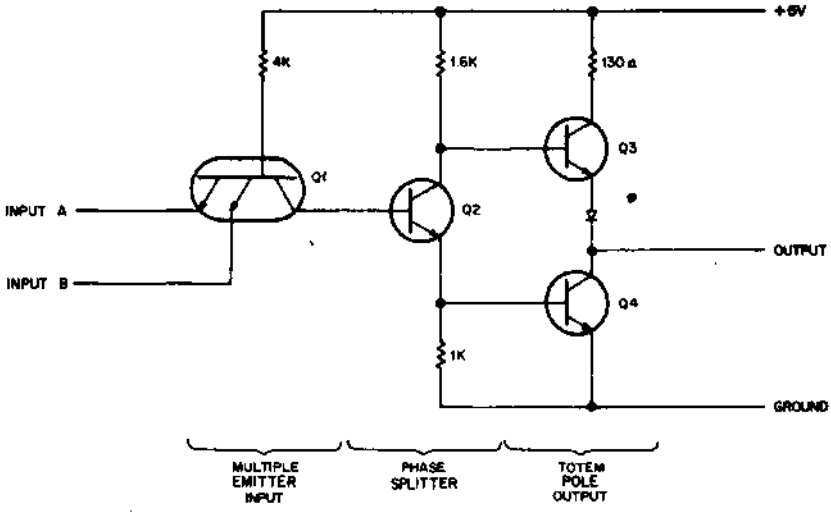


Figure 1 TTL NAND Gate Schematic Diagram

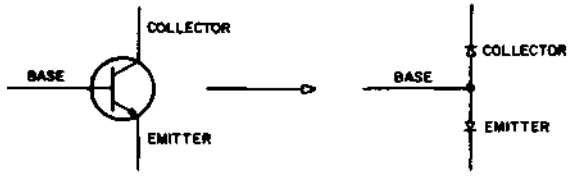


Figure 2 Two Diode Model For Transistor

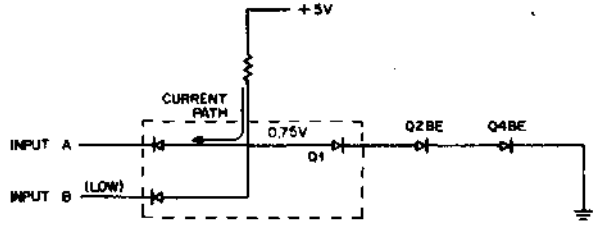


Figure 3 Diode Equivalent NAND Gate Circuit, One Input LO

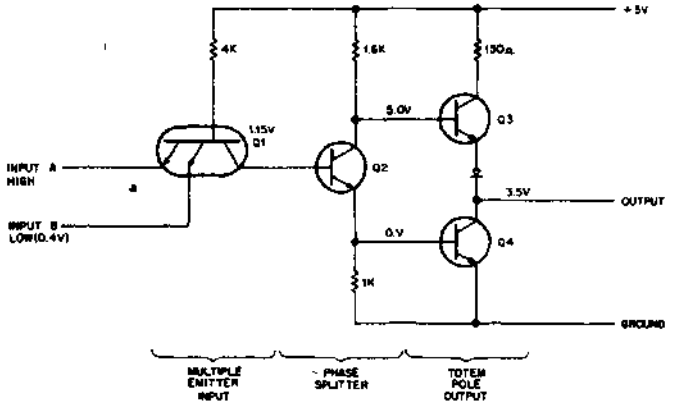


Figure 4 TTL NAND Gate Schematic Diagram, One Input LO

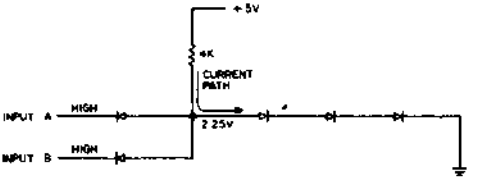


Figure 5 Diode Equivalent NAND Gate Circuit, Both Inputs HI

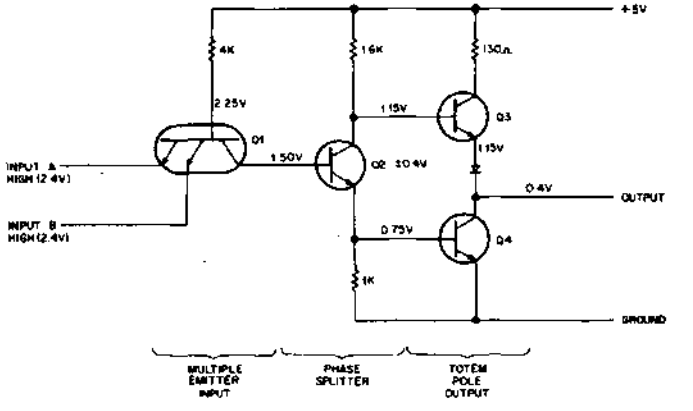


Figure 6 TTL NAND Gate Schematic Diagram, Both Inputs HI

OPERATING CHARACTERISTICS

Power Supply Voltage: 5 Volts ± 5%

Operating Temperature Range: 0° to 70°C

Speed: M Series integrated circuit modules are rated for operation in a system environment at frequencies up to 6 MHz. Specific modules may be operated at higher frequencies as indicated by the individual module specifications.

LOGIC LEVELS AND NOISE MARGIN
A gate input will recognize 0.0 volts to 0.8 volts as logical LO and 2.0 volts to 3.6 volts will be recognized as a logical HI. An output is between 0.0 volts and 0.4 volts in the logical LO condition. The logical HI output condition is between 2.4 volts and 3.6 volts. Figure 7 shows diagrammatically the acceptable transistor-transistor logic levels. The worst case noise margin is 400 millivolts that is, an output would have to make at least a 400 millivolt excursion to cause an input which is connected to it to go into the indetermined voltage region. For instance if an output were at 0.4 volts (worst case logical LO) there would have to be a + 400 mv swing in voltage to cause inputs connected to it to go into their indetermined region.

Input and Output Loading: The input loading and output drive capability of M Series modules are specified in terms of a specific number of unit loads. Typically the input loading is one unit, however certain modules may contain inputs which will present greater than one unit load. The typical M Series module output will supply 10 unit loads of input loading. However, certain module outputs will deviate from a 10 unit load capability and provide more or less drive. Always refer to the individual module specifications to ascertain actual loading figures.

Unit Load: In the logic 0 state, one unit load requires that the driver be able to sink 1.6 milliamps (maximum) from the load's input circuit while maintaining an output voltage of equal to or less than +0.4 volts. In the logic 1 state, one unit load requires that the driver supply a leakage current 40 microamps (maximum) while maintaining an output voltage of equal to or greater than +2.4 volts.

Timing: M Series pulse sources provide sufficient pulse duration to trigger any M Series flip-flop operating within maximum propagation delay specifications. Detailed timing information appears later in this section and in the module specifications.

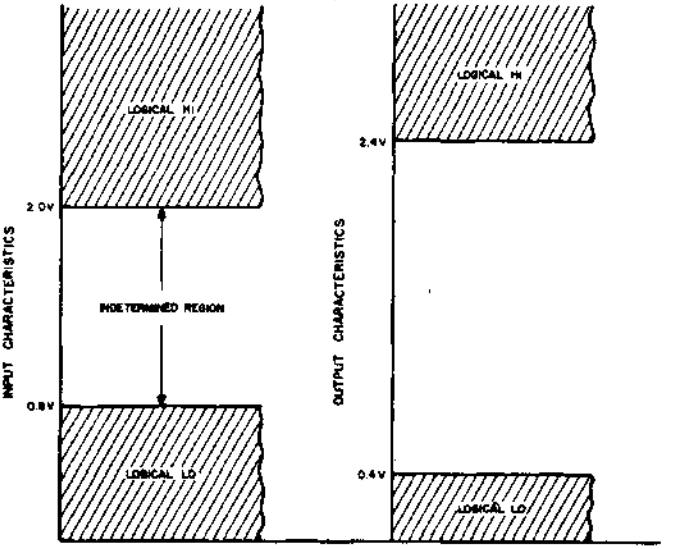
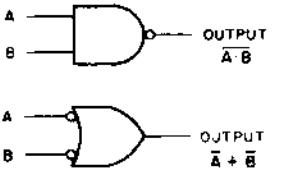


Figure 7 Logic Levels

NAND Logic Symbol: Logic symbology used to describe M Series modules is based on widely accepted standards. Logic symbols and a truth table for the NAND gate are shown in Figure 8.



A	B	OUTPUT
L	L	H
L	H	H
H	L	H
H	H	L

Figure 8 NAND Gate Logic Symbol and Truth Table

The first symbol is visually more effective in applications where two high inputs are ANDed to produce a low output. The second symbol better represents an application where low inputs are ORed to produce a high output.

TTL AND/NOR GATE

With a few modifications, the basic TTL NAND gate can perform an AND/NOR function useful in exclusive OR, coincidence, line selection and NOR gating operations. The modified circuit is shown in simplified form in Figure 9.

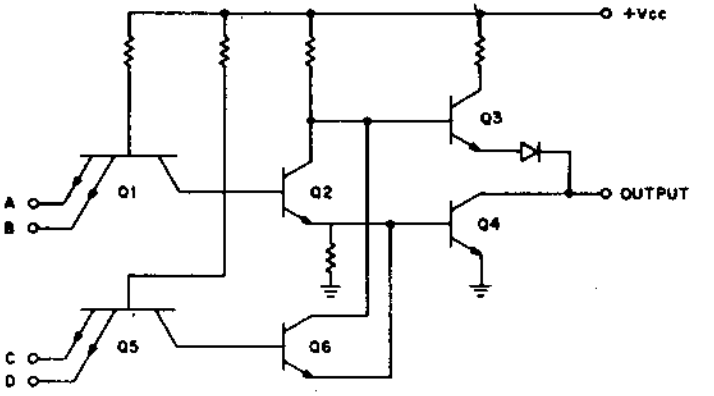
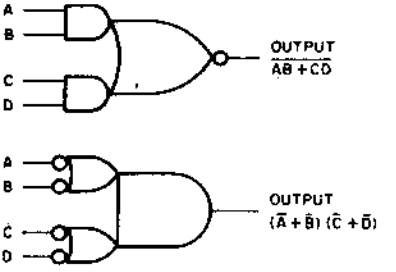


Figure 9 TTL AND/NOR Gate Simplified Schematic

Circuit Operation: The basic elements of the TTL NAND gate are used without modification. The phase-splitter (Q2) is paralleled with an identical transistor (Q6), also controlled by multiple-emitter input transistor which receives two additional inputs, C and D. When either of the input pairs are high, the phase inverter operates to switch the output voltage low. Circuit performance is essentially identical to the TTL NAND circuit.

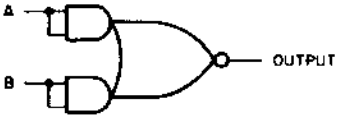
AND/NOR Logic Symbol: The logic symbols for the AND/NOR gate are shown and defined in Figure 10.



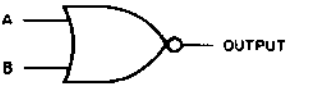
A	B	C	D	OUTPUT
H	H	ANY		L
ANY		H	H	
L	H	L	H	H
L	H	H	L	
H	L	H	L	
H	L	L	H	

Figure 10 AND/NOR Gate Logic Symbols and Truth Table

NOR Configuration: The AND/NOR gate can perform a straight NOR function if the AND gate inputs are tied together as shown in Figure 11.



AND/NOR INPUTS TIED

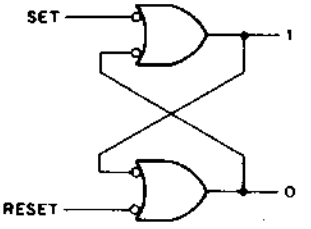


RESULTING NOR SYMBOL

Figure 11 NOR Connection of AND/NOR Gate

NAND GATE FLIP-FLOPS

RS Flip-Flop: A basic Reset/Set flip-flop can be constructed by connecting two NAND gates as shown in Figure 12.



PREVIOUS STATE		INPUT CONDITION		RESULT	
1	0	SET	RESET	1	0
L	H	L	H	H	L
H	L	H	L	L	H
L	H	H	H	NO CHANGE	
H	L	H	H	NO CHANGE	
H	L	L	H	NO CHANGE	
L	H	H	L	NO CHANGE	
L	H	L	L	H*	H*
H	L	L	L	H*	H*

*Ambiguous state: In practice the input that stays low longest will assume control.

Figure 12 RESET/SET NAND Gate Flip-Flop

CLOCKED NAND GATE FLIP-FLOPS

The Reset-Set flip-flop can be clock-synchronized by the addition of a two-input NAND gate to both the set and the reset inputs. (See Figure 13.) One of the inputs of each NAND is tied to a common clock or trigger line.

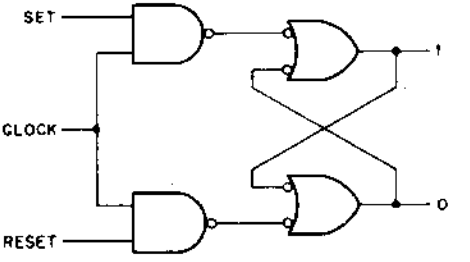


Figure 13 Clocked NAND Gate Flip-Flop

A change of state is inhibited until a positive clock pulse is applied. The ambiguous case will result if both the set and reset inputs are high when the clock pulse occurs.

M SERIES GENERAL-PURPOSE FLIP-FLOPS

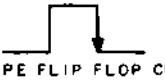
Two types of general-purpose flip-flops are available in the M Series, both of which have built-in protection against the ambiguous state characteristic of NAND gate flip-flops.

FLIP-FLOP CLOCK INPUT SYMBOLS

The D type flip-flop is a true leading (positive going voltage) edge triggered flip-flop and the D input is locked out until the clock input returns to low. The symbol to indicate this function will be as follows;

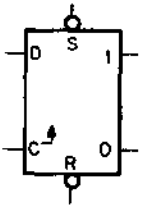
D TYPE FLIP FLOP CLOCK

The operation of the J-K type flip-flop is to transfer the information present at the J and K inputs just prior to and during the clock pulse to the master flip-flop when the threshold is passed on the leading (positive going voltage) edge of the clock pulse. The information stored in the master flip-flop is transfered to the slave flip-flop, and consequentially to the outputs, when the threshold is passed on the trailing (negative going voltage) edge of the clock pulse. The symbol to indicate this function will be as follows;



J K TYPE FLIP FLOP CLOCK

D Type Flip-Flop: The first of these is the D type flip-flop shown in Figure 14 In this element, a single-ended data input (D) is connected directly to the set gate input. An inverter is provided between the input line (D) and the reset input. This ensures that the set and reset levels cannot be high at the same time.



LOGIC SYMBOL

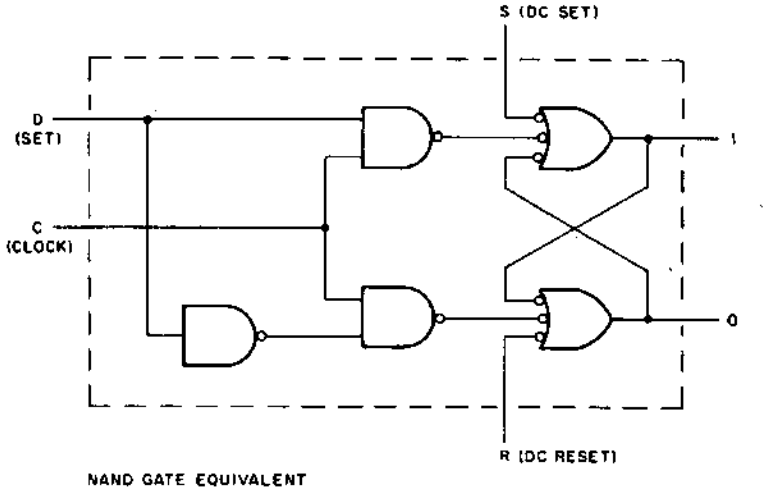


Figure 14. D Type General Purpose Flip-Flop

The flip-flop proper employs three-input NAND gates to provide for dc set and reset inputs.

D type flip-flops are especially suited to buffer register, shift register and binary ripple counter applications. Note that D type devices trigger on the leading (or positive going) edge of the clock pulse. Once the clock has passed threshold, changes on the D input will not affect the state of the flip-flop due to a lockout circuit (not shown).

A characteristic of the D type flip-flop which is not illustrated in the NAND gate equivalent circuit is the fact that the D input is locked out after the clock input threshold voltage on the leading (positive going voltage) edge of the clock has been passed. The D input is not unlocked until the clock input threshold voltage of the trailing (negative going voltage) edge has been passed.

"MASTER-SLAVE J-K FLIP-FLOP"

The two unique features of a J-K flip-flop are: A) a clock pulse will not cause any transition in the flip-flop if neither the J nor the K inputs are enabled during the clock pulse, and B) if both the J and the K inputs are enabled during the clock pulse, the flip-flop will complement (change states). There is no indeterminate condition in the operation of a J-K flip-flop.

A word of caution is in order concerning the clock input. The J and K inputs must not be allowed to change states when the clock line is high, the output will complement on the negative going voltage transition of the clock. It is for this reason that the clock line must be kept low until it is desired to transfer information into the flip-flop and no change in the states of the J and K inputs should be allowed when the clock line is high.

The J-K flip-flops used are master-slave devices which transfer information to the outputs on the trailing (negative going voltage) edge of the clock pulse. The J-K flip-flop consists of two flip-flop circuits, a master flip-flop and a slave flip-flop. The information which is present at the J and K inputs when the leading edge threshold is passed and during the clock high will be passed to the master flip-flop (The J and K inputs must not change after the leading edge threshold has been passed). At the end of the clock pulse when the threshold of the clock is passed during the trailing (negative going voltage) edge, the information present in the master flip-flop is passed to the slave flip-flop. If the J input is enabled and the K input is disabled prior to and during the clock pulse, the flip-flop will go to the "1" condition when the trailing edge of the clock occurs. If the K input is enabled and the J input is disabled prior to and during the clock pulse, the flip-flop will go to the "0" condition when the trailing edge of the clock pulse occurs. If both the J and K inputs are enabled prior to and during the clock pulse, the flip-flop will complement when the trailing edge of the clock pulse occurs. If both the J and K inputs are disabled prior to and during the clock pulse, the flip-flop will remain in whatever condition existed prior to the clock pulse when the trailing edge of the clock pulse occurs.

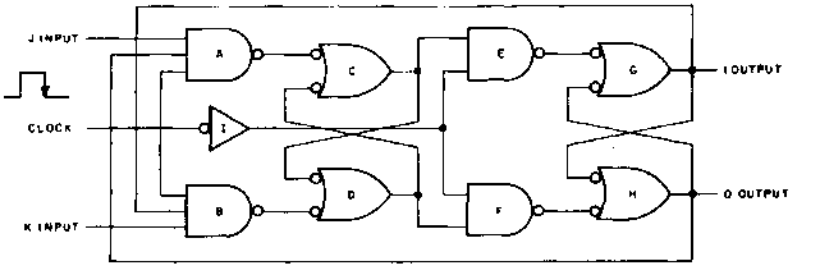


Figure 15. Master-Slave J-K Flip-Flop

Figure 16 shows a functional block diagram of a master slave J-K flip-flop using NAND gates. Gates C and D are the master flip-flop. Gates G and H are the slave flip-flop. Gates A and B are the steering network of the master flip-flop and the steering network for the slave flip-flop is comprised of gates E, F, and 1. The 1 output of the master flip-flop is point X. The operation of the flip-flop will be studied by examining the "1" to "0" transition of the flip-flops, with both the J and the K inputs enabled with a HI level before the clock pulse. When the leading edge of a HI clock pulse occurs, gate B will be enabled with three HI inputs. This will provide a RESET signal for the master flip-flop which will then go to the "0" condition. The slave flip-flop remains in the "1" condition while the clock pulse is HI because gate I is providing a LO signal to both gates E and F, thereby blocking inputs to the slave flip-flop. When the trailing edge of the clock pulse occurs, gate F will be enabled with a HI level at both its inputs and a RESET signal will be provided to the slave flip-flop, which will then go to the "0" condition. The next clock pulse, with both the J and K enabled, would cause the master flip-flop to go to the "1" condition on the leading edge of the clock pulse and cause the slave flip-flop to go to the "1" condition on the trailing edge of the pulse. Figure 16 is a truth table for the J-K flip-flop showing all eight possible initial conditions.

INITIAL CONDITIONS OUTPUTS		INPUTS		FINAL CONDITIONS OUTPUTS	
1	0	J	K	1	0
L	H	L	L	L	H
L	H	L	H	L	H
L	H	H	L	H	L
L	H	H	H	H	L
H	L	L	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	L	H	H	L	H

Figure 16. Master-Slave J-K Flip-Flop Truth Table

UNUSED INPUTS (GATES AND FLIP-FLOPS)

Since the input of a TTL device is an emitter of a multiple-emitter transistor, care must be exercised when an input is not to be used for logic signals. These emitters provide excellent coupling into the driving portions of the circuit when left unconnected. To insure maximum noise immunity, it is necessary to connect these inputs to a source of Logic 1 (High). Two methods are recommended to accomplish this:

1. Connect these inputs to a well filtered and regulated source of +3 volts. Pins U1 and V1 are provided on the M113, M117, M119, M121, M617, and M627 for this purpose.

2. Connect these inputs to one of the active inputs on the same gate. This results in a higher leakage current due to the parallel emitters and should be considered as an additional unit load when calculating the loading of the driving gate.

Connection of unused inputs to the supply voltage, Vcc, is not advisable, since power supplies are subject to transients and voltage excursions which could damage the input transistor.

TIMING CONSIDERATIONS

Standard Timing Pulse: In digital system design, a reference for system timing is usually required. The M Series modules M401 or M405 produces a standard pulse which provides such a reference. The standard pulse derived from each of these two modules is shown in Figure 17.

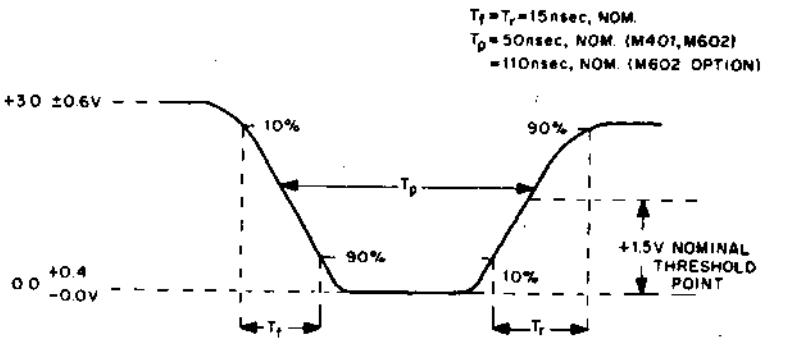


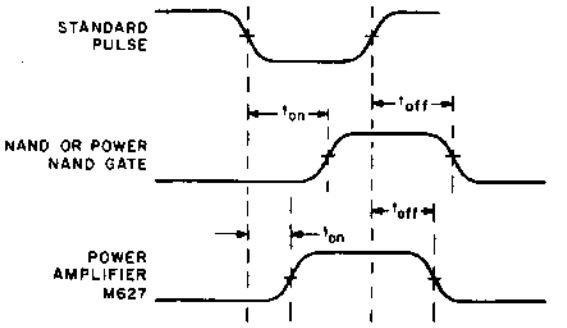
Figure 17. Standard Pulse

NAND Gate and Power Amplifier Propagation Delays: The standard pulse (Figure 17) is distributed throughout a system in negative form to maintain the leading edge integrity. (Since the TTL gate drives current in the logic 0 state, the falling edge is more predictable for timing purposes.) However, the standard pulse is of the wrong polarity for use as a clocking input to the type D and J-K flip-flops, requiring the use of a local inverter. Ordinarily, a NAND inverter is adequate. Where high fan-out is necessary, a M617 Power NAND is preferred.

For applications requiring both high fan-out and critical timing the M627 Power Amplifier is available. This module contains extremely high-speed gates which exhibit turn-on times differing by only a few nanoseconds.

Simultaneity is desirable in clock or shift pulses distributed to extended shift registers or synchronous counters.

Delays introduced by inverting gates and power amplifiers are illustrated in Figure 18. (Delays are measured between threshold points.)



DELAY (NANOSECONDS)			
t_{on}		t_{off}	
TYP.	MAX.	TYP.	MAX.
18	29	8	15
7	—	5	—

Figure 18. NAND Gate and Power Amplifier Delays

Flip-Flop Propagation Delays: D type flip-flops trigger on the leading or rising edge of a positive clock pulse; the propagation delay is measured from the threshold point of this edge. The set-up time of the D flop is also measured from this threshold point. Data on the D input must be settled at least 20 nanoseconds prior to the clock transition. The advantage of the D-flip-flop, however, is that the leading edge triggering allows the flip-flop AND gates to propagate while the clock pulse is still high. Figure 19 illustrates this situation.

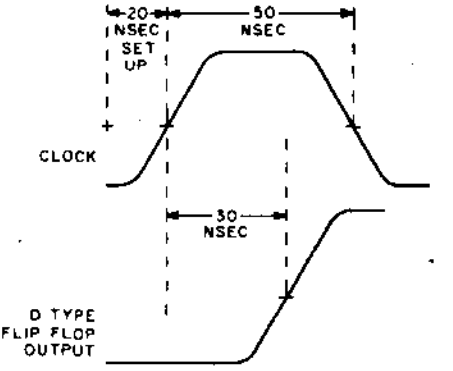


Figure 19. D Type Flip-Flop Timing

JK type flip-flops are, in effect, trailing edge triggering devices as explained previously. The only restriction on the J and K inputs is that they must be settled by the time that the rising edge occurs. Timing is shown in Figure 20.

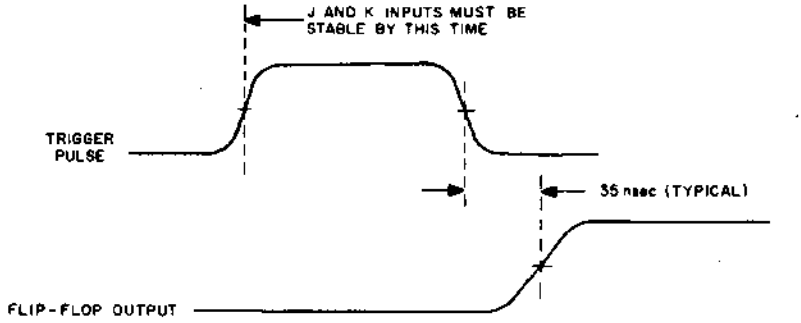


Figure 20. J-K Flip-Flop Timing

When using the dc Set or Reset inputs of either flip-flop type, propagation delays are referenced to the falling edge of the pulse. This is due to the inverted sense of these inputs. When resetting ripple type counters (where the output of one flip-flop is used as the trigger input to the next stage) the reset pulse must be longer than the maximum propagation delay of a single stage. This will ensure that a slow flip-flop does not introduce a false transition, which could ripple through and result in an erroneous count.

One-Shot Delay: Calibrated time delays of adjustable duration are generated by the M302 Delay Multivibrator. When triggered by a level change from a logical one to a logical zero, this module produces a positive output pulse that is adjustable in duration from 50 to 750 nsec with no added capacitance. Delays up to 7.5 milliseconds are possible without external capacitance. (See M302 specification.) Basic timing and the logic symbol are shown in Figure 21. The 100 picofarad internal capacitance produces a recovery time of 30 nsec. Recovery time with additional capacitance can be calculated using the formula:

$$t_r \text{ Nanoseconds} = 30 \frac{\text{C Total (Picofarads)}}{100}$$

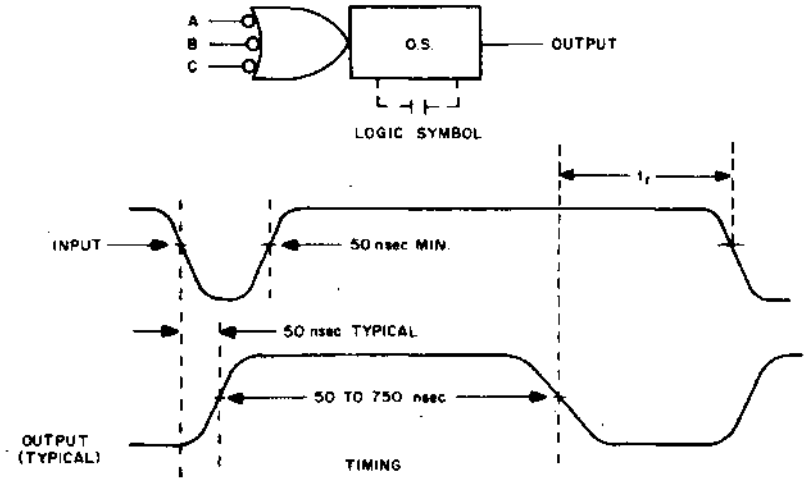


Figure 21. One-Shot Delay Timing and Logic Symbol

SYSTEM OPERATING FREQUENCY

Although individual propagation delays are significant in the design of digital logic, even more important is the maximum operating frequency of a system which is composed of these individual modules. Specifically designed systems may be operated at 10 MHz, but a more conservative design may result in a somewhat lower operating speed. M Series modules can be designed into a system with a 6 MHz clock rate with relative ease. This system frequency is derived by summing the delays in a simple logic chain:

1. A standard clock pulse width of 50 nsec is assumed. This period is measured from the threshold point of the leading edge to the threshold point of the trailing edge.

2. One flip-flop propagation delay of 35 nsec from the trailing edge of the clock pulse to the threshold point of the final state of the flip-flop is allowed.

3. Two gate-pair delays of 30 nsec each are assumed. (A gate-pair consists of two inverting gates in series.) Two gate-pair delays are usually required to perform a significant logic function with a minimum of parallel operations. The two gate-pair delays total 60 nsec.

The time necessary to perform these operations before the next occurrence of the clock pulse is the sum of the delays; 50 + 35 + 60, or 145 nsec. Allowing 20 nsec for variations within the system, the resulting period is 165 nsec, corresponding to a 6 MHz clock rate. This timing is demonstrated in Figure 22.

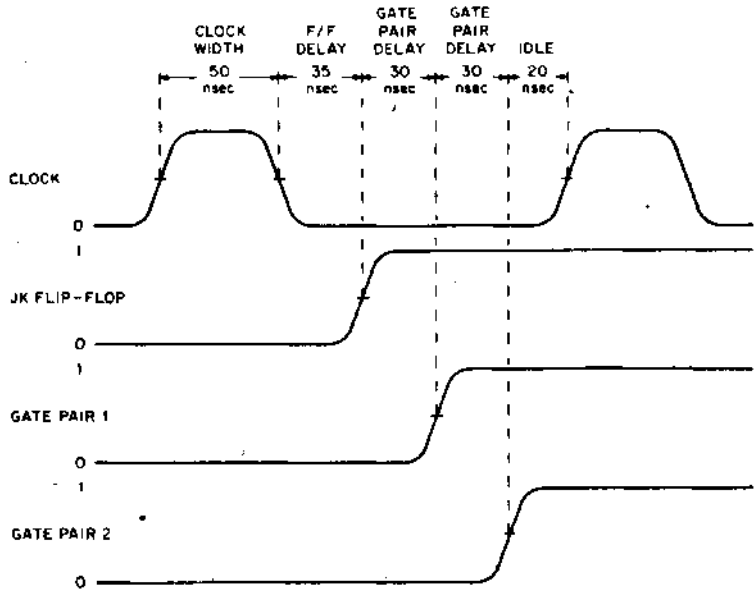


Figure 22. Delays Determining System Operating Frequency

Substitution of a D type flip-flop results in a similar timing situation. In a system using both D and J-K flip-flops, note that the D flip-flop triggers on the leading edge of the clock pulse and the J-K flip-flop triggers on the trailing edge. When calculating system timing using D flip-flops, remember that the flip-flop inputs must be settled at least 20 nsec prior to the occurrence of the clock pulse.

Preparation of a timing diagram that considers delays introduced by all logic elements will aid the designer in achieving predictable system performance.

M SERIES LOGIC AND CONTROL MODULES

Modules in this section are organized into six functional categories:

	GATES
M113	NAND Gates
M115	NAND Gates
M117	NAND Gates
M119	NAND Gates
M133	Two-Input NAND Gates
M135	Eight 3-Input NAND Gates
M137	NAND Gates
M139	Three 8-Input NAND Gates
M1131	Open-Collector NAND Gates
M141	NAND/OR Gates
M1103	Two-Input AND Gates
M1307	Four-Input AND Gates
M121	AND/NOR Gates
M116	Six 4-Input NOR Gates
M112	NOR Gates
M1125	Exclusive-OR Gates
M111	Inverter
M611	Inverter
M165	Eight Buffers

	FLIP-FLOPS AND REGISTERS
M205	General Purpose Flip-Flops
M206	General Purpose Flip-Flops
M207	General Purpose Flip-Flops
M246	Five D-Type Flip-Flops
M202	Triple J-K Flip-Flop
M203	Eight R/S Flip-Flops
M2001	Tri-State Flip-Flop
M204	General Purpose Buffer and Counter
M245	Dual 4-Bit Shift Register
M248	Dual 4-Bit Multipurpose Shift Register
M239	Four-Bit Counter/Register
M2500	MOS Memory

	TIME RELATED
M3020	Integrating One Shot
M306	Integrating One Shot
M501	Schmitt Trigger
M310	Delay Line
M401	Variable Clock
M403	RC Multivibrator Clock
M404	Crystal Clock
M405	Crystal Clock
M602	Pulse Amplifier
M671	M-To-K Converter
M521	K-To-M Converter

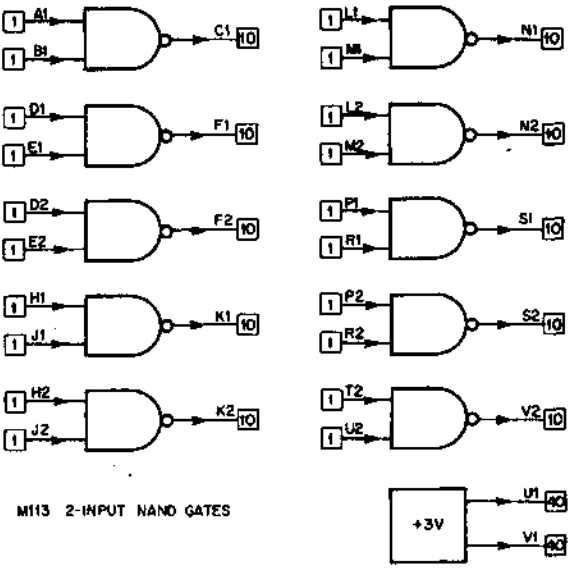
	NUMERIC
M161	Binary to Octal/Decimal Decoder
M163	Binary to Decimal Decoder
M230	Binary to BCD and BCD to Binary Converter
M236	12-Bit Binary Up/Down Counter
M237	3-Digit BCD Up/Down Counter
M238	Dual 4-Bit Binary Synchronous Up/Down Counter
M159	Arithmetic/Logic Unit
M191	ALU Look-Ahead Logic
M155	4-Line to 16-Line Decoder
M1701	Data Selector
M1713	16-Line to 1-Line Data Selector
M168	12-Bit Magnitude Comparator
M162	Parity Circuit
	LOGIC AMPLIFIERS
M040	Solenoid Driver
M050	Indicator Driver
M060	Solenoid Driver
M617	4-Input Power NAND Gates
M627	NAND Power Amplifier
M660	Positive Level Cable Driver
	MISCELLANEOUS
M002	Logic HIGH Source
M594	EIA/CCITT Level Converter
M598	One-Channel Transmit/Receive Optic-Coupled Current Isolator
M706	Teletype Receiver
M707	Teletype Transmitter
M906	Cable Terminator
M7389	Serial Line Transmitter/Receiver
M7390	Asynchronous Transceiver
M9970	H854 to Backplane Adapter

M113, M115, M117, M119
NAND GATES

GATES

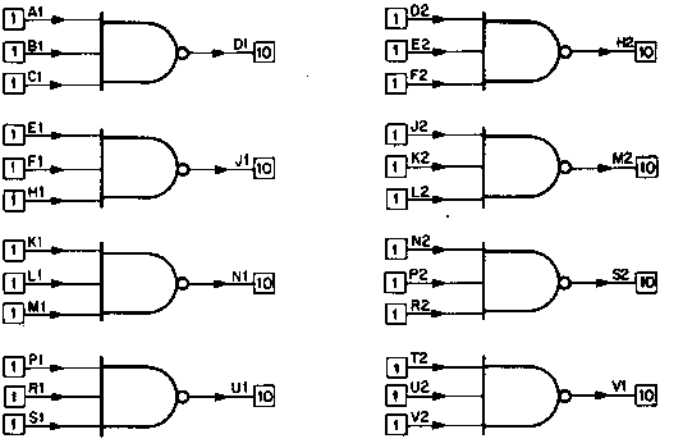
M SERIES

Length: Standard
Height: Single
Width: Single

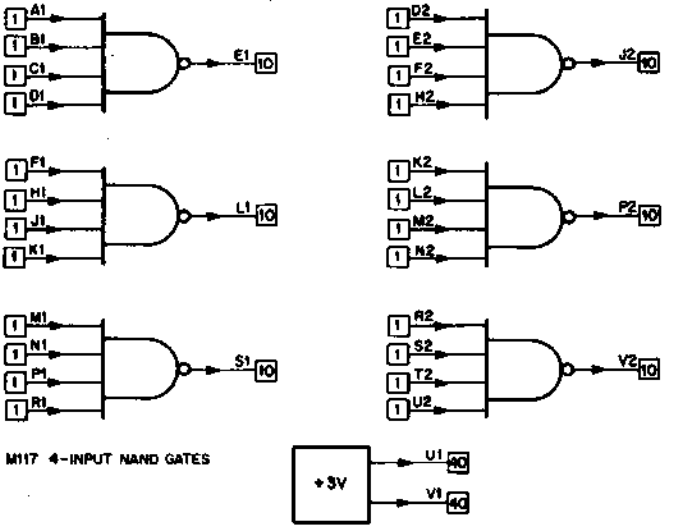


M113 2-INPUT NAND GATES

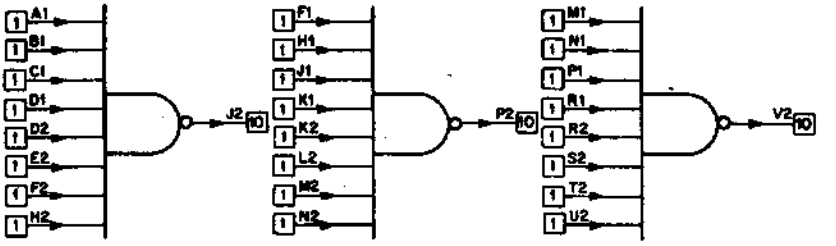
Volts	Power mA (max.)	Pins
+5	71 M113	A2
+5	41 M115	A2
+5	41 M117	A2
+5	19 M119	A2
GND		C2, T1



M115 3-INPUT NAND GATES



M117 4-INPUT NAND GATES



M119 8-INPUT NAND GATES

These modules provide general-purpose gating for the M Series, and are most commonly used for decoding, comparison, and control. Each module performs the NAND function ($\cdot B \cdot C \cdot \cdots \overline{N}$), depending upon the number of inputs.

APPLICATIONS
- Logic gating

FUNCTIONS
M113—Ten two-input NAND gates that also may be used as inverters.
M115—Eight, three-input NAND gates.
M117—Six, four-input NAND gates.
M119—Three, eight-input NAND gates.

Unused inputs on any gate must be either connected to a used input or returned to a source of logic HIGH, for maximum noise immunity. In the M113, M117, M119, M121, M617 and M627 modules, two pins are provided (U1 and V1) as source of +3 volts for this purpose. Each pin can supply up to 40 unit loads. M103, M111 and M002 provide additional sources of logic HIGH level.

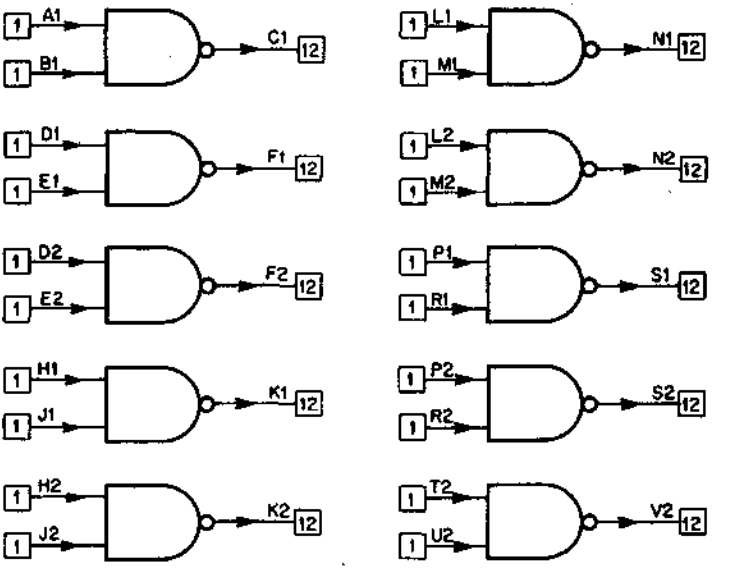
SPECIFICATIONS
Typical propagation delay of M Series gates is 15 ns.

M133
TWO-INPUT NAND GATES

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	160	A2
GND		C2, T1

This module provides general-purpose high-speed NAND gating.

APPLICATIONS
The high-speed characteristic of these gates frequently will solve tight timing problems in complex systems.

SPECIFICATIONS
Maximum output propagation delay to a logic HIGH or LOW is 10 ns.

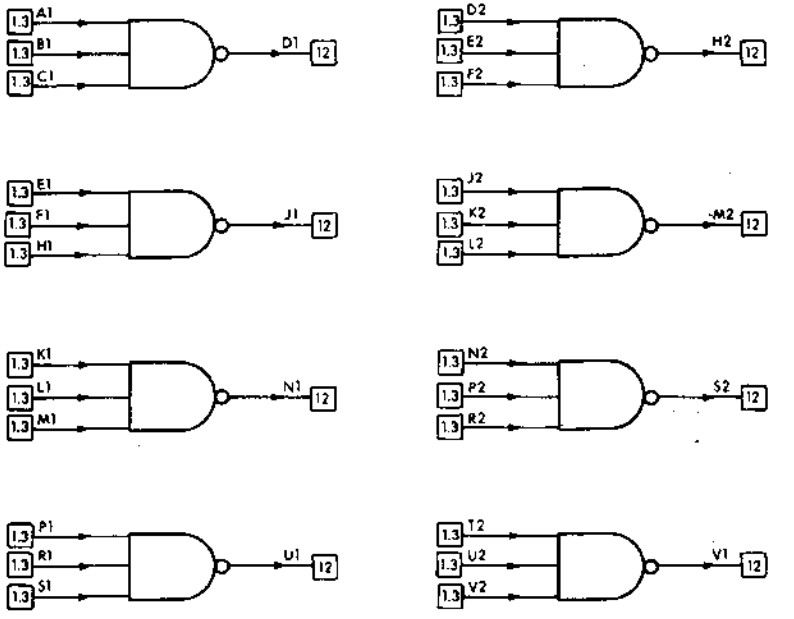
Unused inputs on any gate must be returned to a source of logic HIGH for maximum speed and noise immunity.

M135
8 3-INPUT NAND GATES

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	100	A2
GND		C2, T1

The M135 module consists of eight high-speed, 3-input, positive logic NAND gates. It is pin-compatible with the M115 module.

APPLICATIONS

- Logic gating

SPECIFICATIONS

Maximum propagation delay to a logic HIGH or LOW is 10 ns.

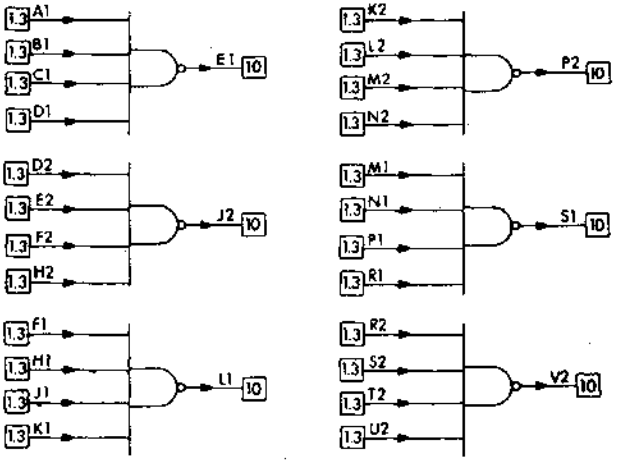
NOTE: All unused inputs must be returned to a source of logic HIGH for maximum noise immunity.

M137
SIX 4 INPUT NAND GATES

GATES

M SERIES

Length: Standard
Width: Single
Height: Single



Volts	Power mA (max.)	Pins
+5V	100 mA	A2
GND		C2, T1

The M137 Module consists of six high-speed, 4-input positive logic NAND gates that can be used in many logic gating applications.

Maximum propagation delay to a logic High or Low is 10 μs.

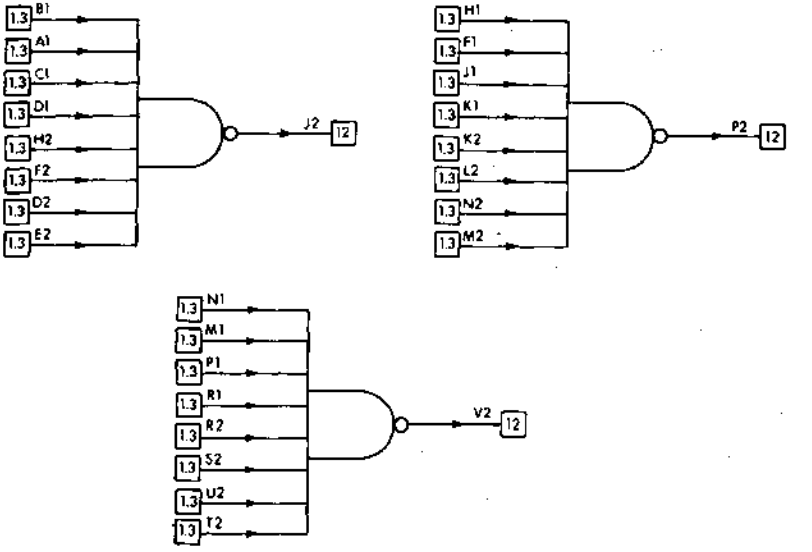
NOTE: All unused inputs must be either tied to a used input or to a source of logic High for maximum noise immunity.

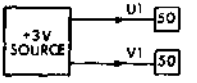
M139
3 8-INPUT NAND GATES

GATES

M SERIES

Length: Standard
Height: Single
Width: Single





Volts	Power mA (max.)	Pins
+5	50	A2
GND		C2, T1

The M139 module consists of three high-speed, 8-input, positive logic NAND gates. Pins U1 and V1 provide two separate logic HIGH sources (+3 V,) each capable of holding up to 50 unused M Series inputs HIGH.

APPLICATIONS

- Logic gating

SPECIFICATIONS

Maximum propagation delay to a logic HIGH or LOW is 10 ns.

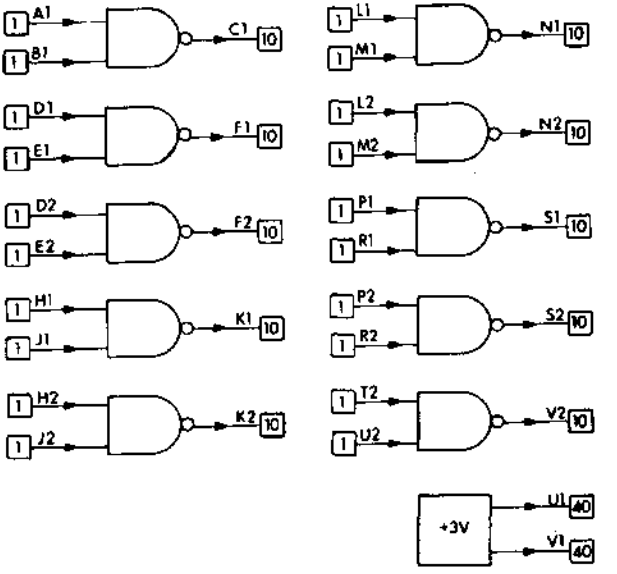
NOTE: All unused inputs must be returned to a source of logic HIGH for maximum noise immunity.

M1131
2-INPUT OPEN COLLECTOR NAND GATE

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	71	A2
GND		C2, T1

The M1131 module consists of ten high-speed, 2-input NAND gate circuits and a +3 Vdc source. Each of the NAND gates has an open collector output and the outputs can be paralleled for a wired AND function. Each gate input is a 1 unit load and each unparalleled output will drive up to 10 unit loads.

APPLICATIONS
Logic gating, Wired-OR multiplexing

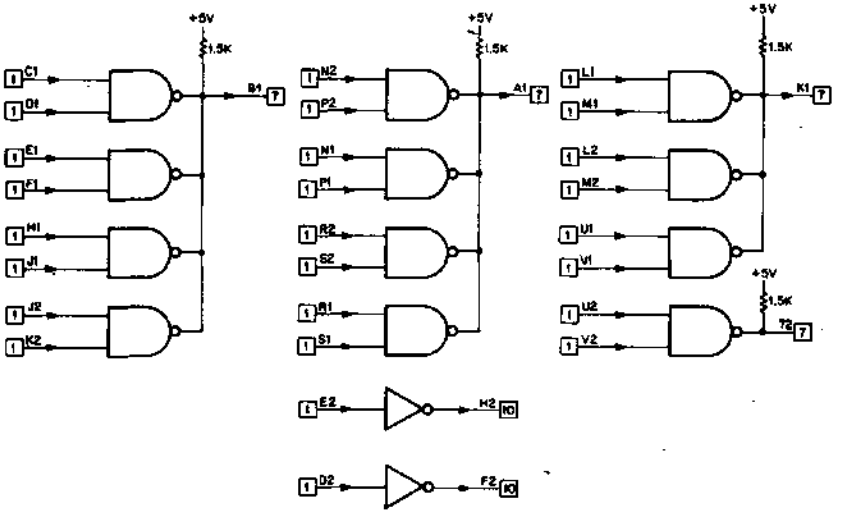
SPECIFICATIONS
Typical gate propagation delay time is 10 ns.

M141
NAND/OR GATES

GATES

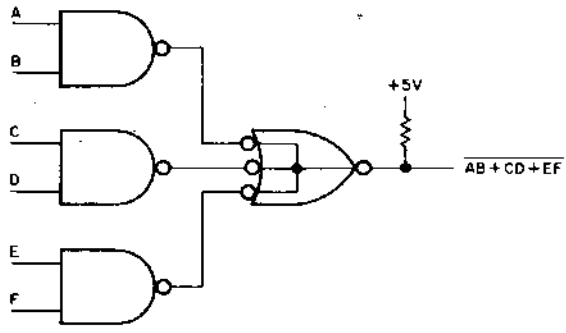
M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	117	A2
GND		C2, T1

This module provides NAND/OR gates arranged in four groups consisting of 4, 4, 3, and 1 two-input NAND gates respectively. The outputs in each group are connected together to provide a wired OR for low levels. The function of these gates can be shown as:



By using one of the two inverters provided, a true AND/OR function can be realized. A maximum of four groups of gates can be connected together. Connection is made by merely connecting output pins together.

APPLICATIONS

- Logic Gating

FUNCTIONS

The M141 NAND/OR gate performs two levels of logic. The first is the NAND function which is identical to the M113 NAND gate. The second level is that of a wired OR for low logic levels. The two-input NAND gate which is used in the M141 does not have the standard TTL output circuit, but only the lower half of the totem pole output. This allows the outputs of these gates to be connected together and to share a common pull-up resistor.

SPECIFICATIONS

Propagation Delay: 70 ns max.

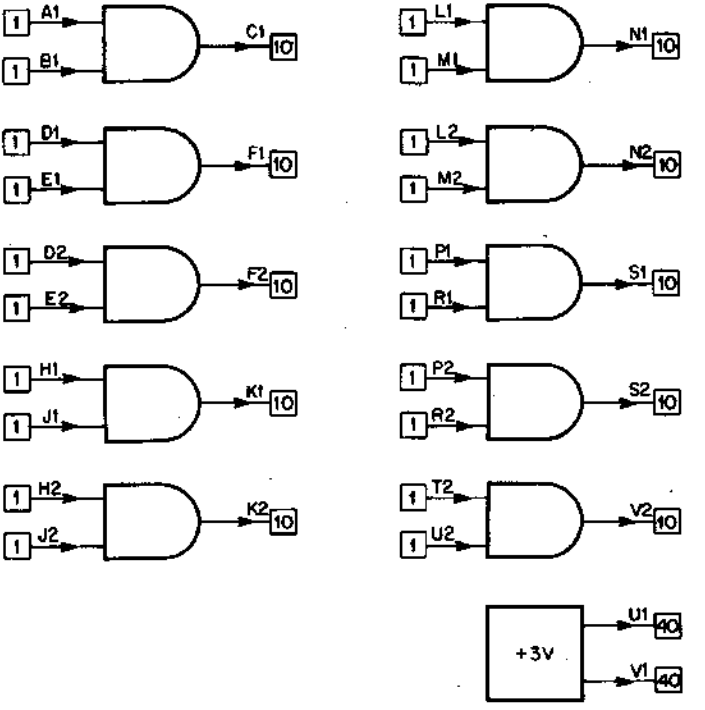
Loading: The load resistor of each output presents 2 unit loads when connected to another output. For example, when four groups are connected together, 3 groups present two unit loads each to the fourth group, totalling 6 unit loads. This leaves 1 unit load capability.

M1103
TWO-INPUT AND GATES

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	80	A2
GND		C2, T1

The M1103 contains ten 2-input AND gates. Unused inputs on any gate must be returned to a source of logic HIGH for maximum noise immunity. Two pins are provided (U1 and V1) as a source of +3 volts for this purpose.

APPLICATIONS

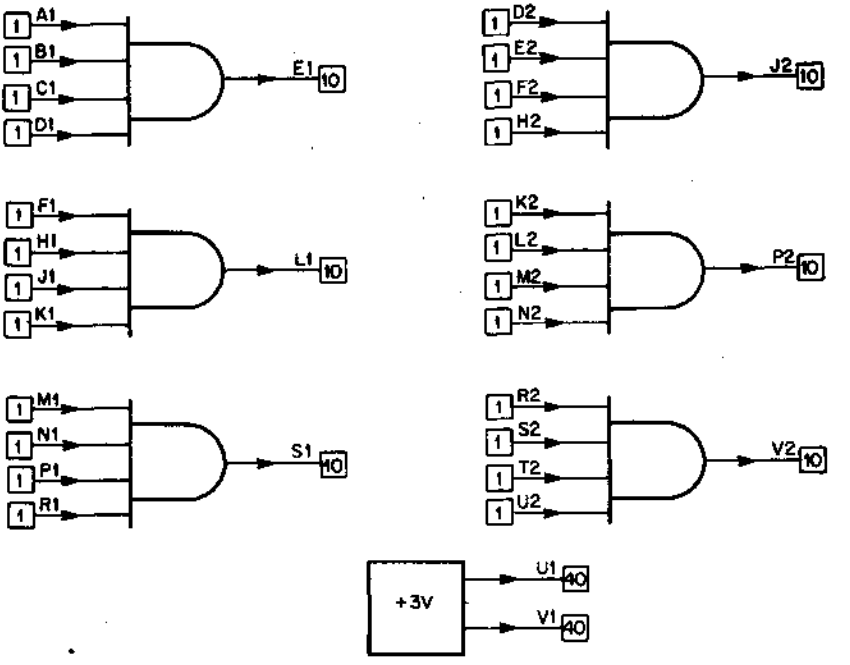
- Positive AND or negative OR gating

M1307
FOUR-INPUT AND GATES

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	100	A2
GND		C2, T1

The M1307 contains six high speed 4-input AND gates. Unused inputs on any gate must be returned to a source of logic HIGH for maximum noise immunity. Two pins are provided (U1 and V1) as a source of +3 volts for this purpose.

APPLICATIONS

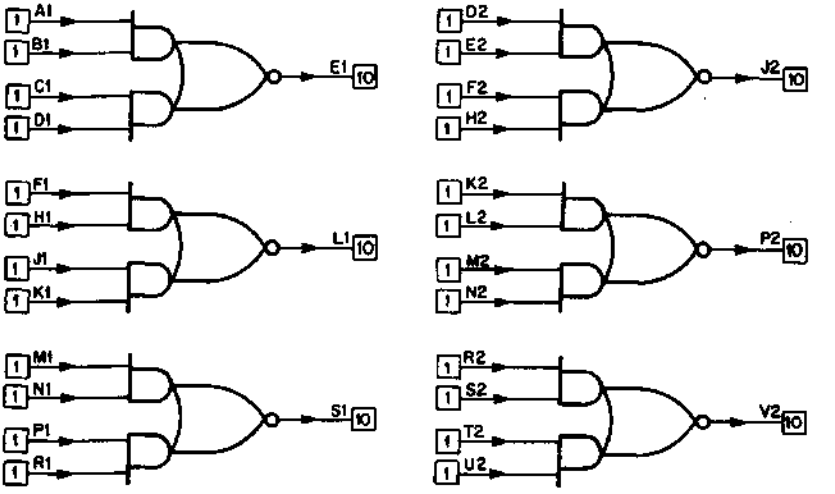
- Positive AND or negative OR gating

M121
AND/NOR GATE

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	50	A2
GND		C2, T1

The M121 module contains six AND/NOR gates which perform the function $(\overline{A \cdot B + C \cdot D})$. By proper connection of signals to the AND inputs, the exclusive OR, coincidence, and NOR functions can be performed.

APPLICATIONS
- Logic Gating

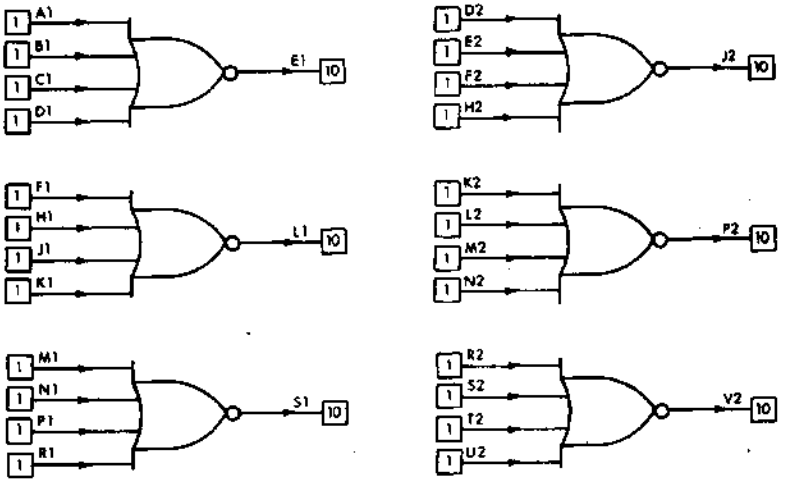
SPECIFICATIONS
Propagation Delay: Typically 15 ns

M116
6 4-INPUT NOR GATES

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	30	A2
GND		C2, T1

The M116 module consists of six high-speed, 4-input, positive logic NOR gates. Pins U1 and V1 provide two separate logic HIGH sources (+3V), each capable of holding up to 50 unused M Series inputs HIGH.

APPLICATIONS

- Logic gating

SPECIFICATIONS

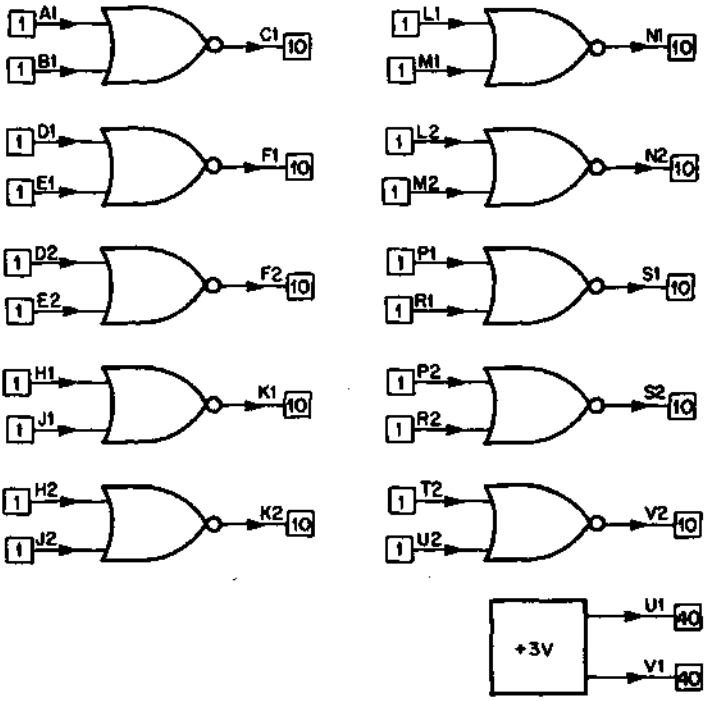
Maximum propagation delay to a logic HIGH or LOW is 10 ns.

M112
NOR GATE

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	50	A2
GND		C2, T1

The M112 contains ten positive NOR gates, each performing the function $\overline{A+B}$. Pins U1 and V1 provide two separate logic HIGH sources (+3V) each capable of holding up to 40 unused M Series inputs HIGH.

APPLICATIONS

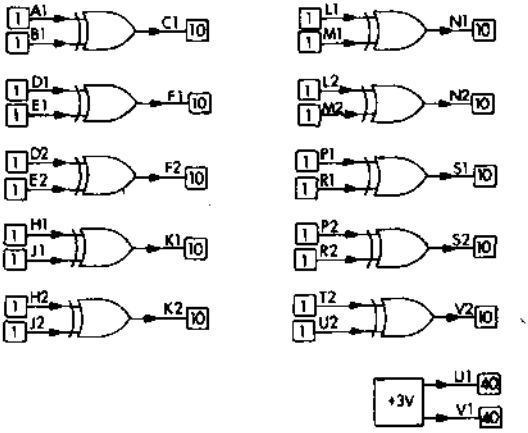
- Logic gating

M1125
EXCLUSIVE OR GATES

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5V	100	A2
GND		C1, T1

The M1125 Module consists of ten 2-input exclusive OR gates and two +3 Vdc voltage divider sources. Each module circuit performs the X-OR function ($A\cdot\overline{B} + \overline{A}\cdot B$) according to the following truth table.

TRUTH TABLE

INPUTS		OUTPUTS
L	L	L
L	H	H
H	L	H
H	H	L

APPLICATION
Logic gating and also used as an inverter by connecting one input to a High level.

FUNCTION
Comparitor or decoder-output is High when input levels are not the same.

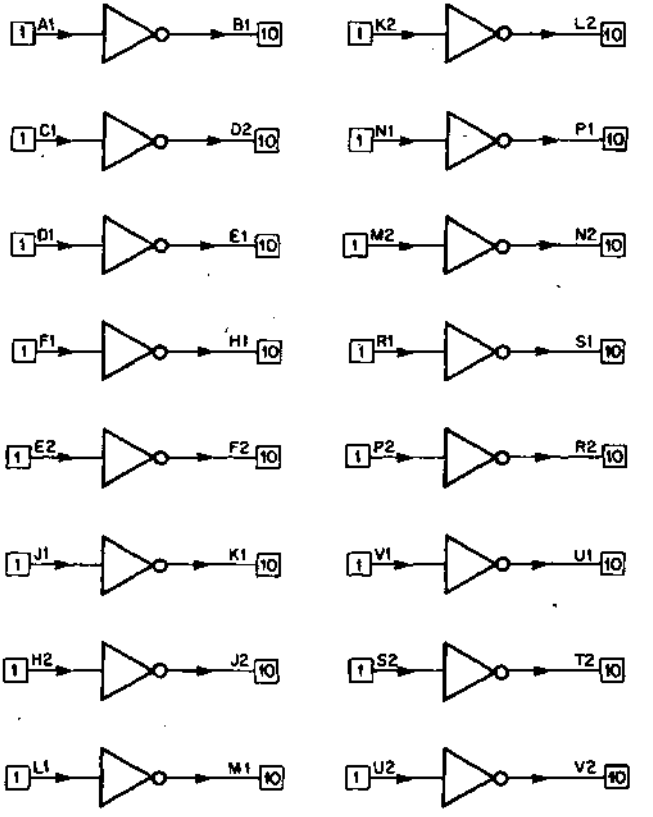
SPECIFICATIONS
Typical propagation delay time of the M1125 is 12 ns.

M111
INVERTER

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	87	A2
GND		C2, T1

Sixteen Inverters with input/output connections as shown.

APPLICATIONS

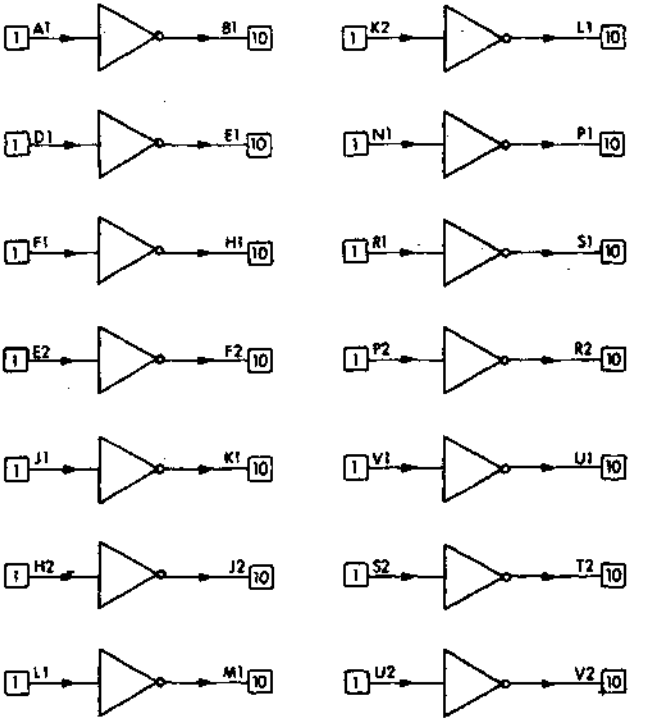
- Output Expansion
- Logical Inversion

M611
HIGH SPEED POWER INVERTER

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	87	A2
GND		C2, T1

Fourteen high speed Inverters with input/output connections as shown.

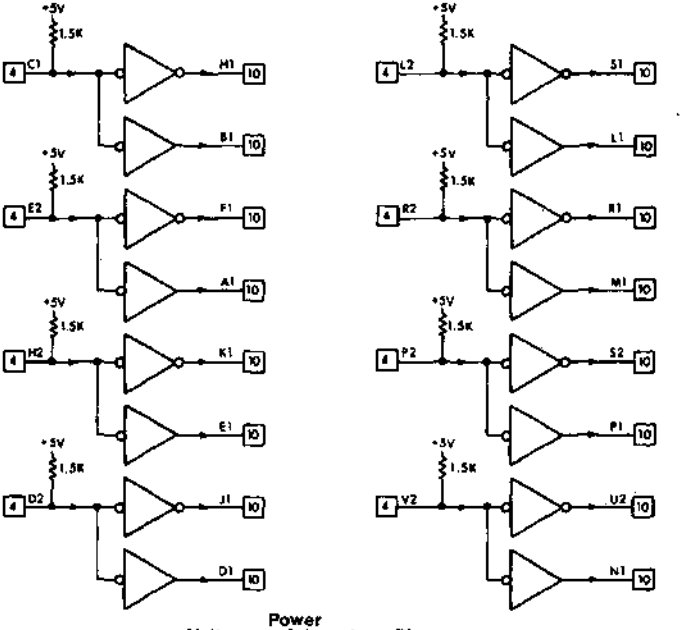
APPLICATIONS
- Output Expansion
- Logical Inversion

M165
8 BUFFERS

GATES

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	130	A2
GND		C2, F2, J2, K2, M2, N2, T1, T2

The M165 module is designed for use with circuits having open-collector output stages. The module provides a pull-up resistor for the open-collector stage and buffers the output through an inverting gate and a noninverting gate.

There are eight similar circuits on the M165 module. The value of the pull-up resistor on each input allows open-collector outputs which can sink at least 10 mA, and have a total leakage not exceeding 1.3 mA, to drive the M165 module, plus one other high-speed TTL load.

SPECIFICATIONS
Propagation Delay

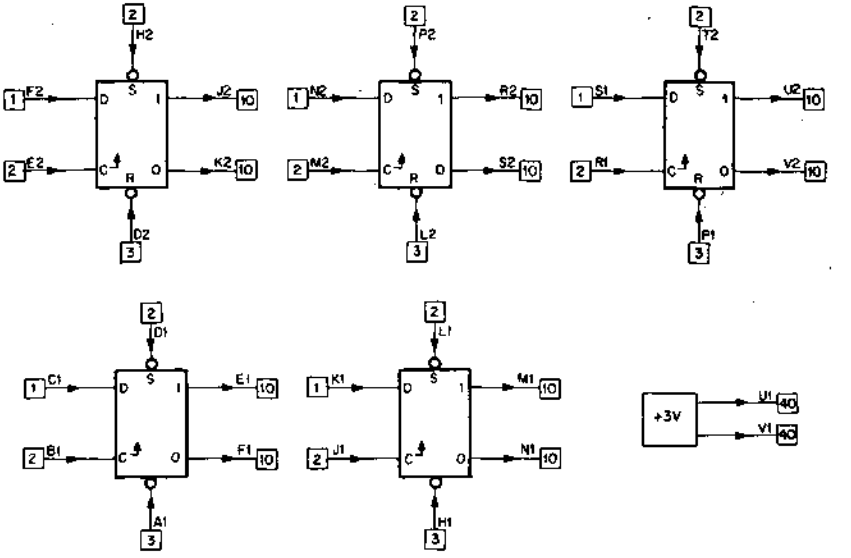
From:	To:
Input	Inverting Output, HIGH or LOW = 10 ns (max)
Input	Noninverting Output, HIGH or LOW = 15 ns (max)

M205
GENERAL-PURPOSE FLIP-FLOPS

FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	90	A2
GND		C2, T1

The M205 contains five separate D-Type flip-flops. Each flip-flop has independent gated data, clock, dc set, and dc reset inputs.

APPLICATIONS

- Storage Registers
- Counters and Shift Registers
- Flags and Control Storage

FUNCTIONS

For each flip-flop, information present on the D input is transferred to the output when the threshold is reached on the leading (positive going voltage) edge of the clock pulse.

SPECIFICATIONS

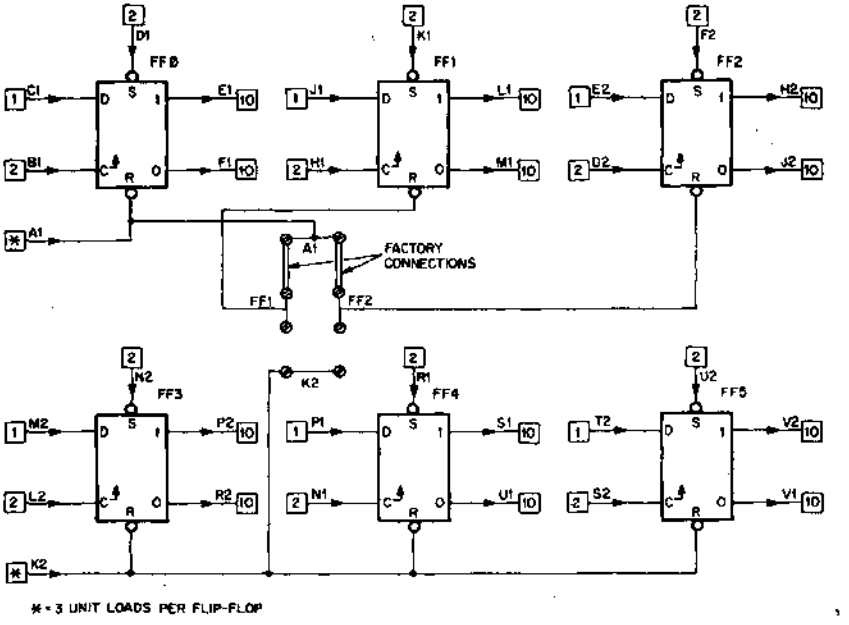
Information must be present on the D input 20 ns (max) prior to a standard clock pulse and should remain at the input at least 5 ns (max) after the clock pulse leading edge has passed the threshold voltage. Data transferred into the flip-flop will be stable at the output within 50 ns, maximum. Typical width requirement for the clock, dc reset and dc set pulses is 30 nsec each.

M206
GENERAL-PURPOSE FLIP-FLOPS

FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	87	A2
GND		C2, T1

The M206 contains six separate D-Type flip-flops. Each flip-flop has independent gated data, clock, and dc set inputs.

APPLICATIONS

- Registers
- Counters and Shift Registers
- Flags and Control Storage

FUNCTIONS

For each flip-flop, information present on the D input is transferred to the output when the threshold is reached on the leading (positive going voltage) edge of the clock pulse.

Provision is made on the printed circuit board for changing the configuration of the two CLEAR lines to the flip-flops. All M206 modules are supplied with the 3-3 configuration, but the grouping can be changed as follows.

CONFIGURATION	CLEAR 1 (A1)	CLEAR 2 (K2)	DELETE JUMPER	ADD JUMPER
3-3	FF0, 1, & 2	FF3, 4, & 5		
4-2	FF0 & 1	FF2, 3, 4, & 5	A1 to FF1	K2 to FF1
5-1	FF0	FF1, 2, 3, 4, & 5	A1 to FF2 A1 to FF1	K2 to FF2 K2 to FF1

A common CLEAR for all six flip-flops can be obtained by wiring pins A1 and K2 together externally.

PRECAUTION
Any unused SET or RESET input should be connected to a logic HIGH source.

Note that the loading of each CLEAR line is calculated on the basis of 3 unit loads per flip-flop. For example, the 4-2 configuration results in 12 unit loads at input K2 and 6 unit loads at input A1.

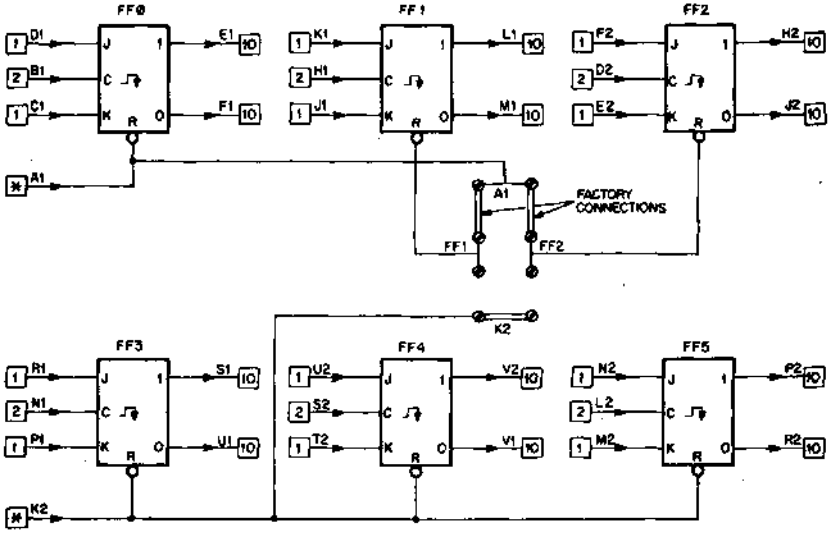
SPECIFICATIONS
Information must be present on the D input 20 ns (min) prior to a standard clock pulse and should remain at the input at least 5 ns (min) after the clock pulse leading edge has passed the threshold voltage. Data transferred into the flip-flop will be stable at the output within 50 ns, maximum. Minimum width requirement for the clock, dc reset and dc set pulses is 30 nsec each.

M207
GENERAL-PURPOSE FLIP-FLOPS

FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single



**2 UNIT LOADS PER FLIP-FLOP

Volts	Power mA (max.)	Pins
+5	96	A2
GND		C2, T1

The M207 contains six general-purpose J-K type flip-flops.

APPLICATIONS

- Buffers
- Control Flip-Flops
- Shift Registers
- Counters

FUNCTIONS

A truth table for clock set and reset conditions appears below. Note that when the J and K inputs are both HIGH, the flip-flop complements on each clock pulse.

STARTING CONDITION (OUTPUT)		INPUT CONDITION		RESULT AT END OF STANDARD CLOCK PULSE (OUTPUT)	
1	0	J	K	1	0
L	H	L	L	No change	
		L	H	No change	
		H	L	H	L
		H	H	H	L
H	L	L	L	No change	
		L	H	L	H
		H	L	No change	
		H	H	L	H

Two CLEAR inputs are provided, with jumper terminals for optional clearing in groups of 3 and 3 (standard), 4 and 2, 5 and 1, or 6 and 0. Provision is made on the printed circuit board for changing the configuration of the two CLEAR lines to the flop-flop. All M207 modules are supplied with the 3-3 configuration, but the grouping can be changed as follows:

CON-FIGURATION	CLEAR 1 (A1)	CLEAR 2 (K2)	DELETE JUMPER	ADD JUMPER
3-3	FF0, 1, & 2	FF3, 4, & 5		
4-2	FF0 & 1	FF2, 3, 4, & 5	A1 to FF1	K2 to FF1
5-1	FF0	FF1, 2, 3, 4, & 5	A1 to FF2 A1 to FF1	K2 to FF2 K2 to FF1

SPECIFICATIONS

J and K inputs must be stable during the leading-edge threshold of a standard CLOCK input and must remain stable during the positive state of the CLOCK. Data transferred into the flip-flop will be stable at the output within 30 ns (typical) of the CLOCK pulse trailing edge threshold (negative going voltage).

Application of a LOW level to an R input for at least 25 ns resets the flip-flop unconditionally.

PRECAUTION

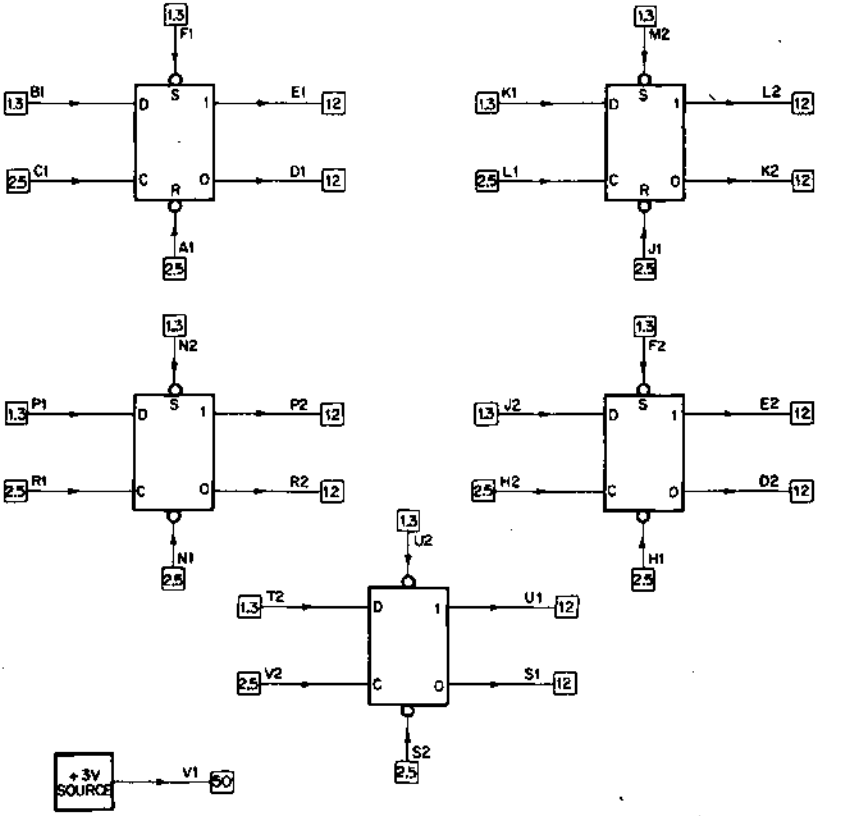
Any unused SET or RESET input should be connected to a logic HIGH source.

M246
5 D-TYPE FLIP-FLOPS

FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	160	A2
GND		C2, M1, T1

The M246 module contains five high-speed, general-purpose, D-type flip-flops. Each flip-flop has its SET(S), RESET(R), CLOCK(C), DATA(D), and outputs brought out to separate pins.

The information at the D or DATA input is transferred to the 1 output on the positive-going edge of the CLOCK pulse. The CLOCK-triggering occurs at a voltage level of the CLOCK pulse and is not directly related to the transition time of the positive-going pulse.

SPECIFICATIONS

Clock Freq	= 35 MHz (max)
CLOCK Pulse	= 15 ns (min)
SET Pulse	= 25 ns (min)
RESET Pulse	= 25 ns (min)
DATA Set-up Time	= 15 ns (min)

Propagation Delay Time

From:	To:
SET or RESET	LOW or HIGH Output = 20 ns (max)
CLOCK	LOW or HIGH Output = 20 ns (max)

TRUTH TABLE (Each Flip-Flop)

t_n	t_n+1	
INPUT D	OUTPUT 1	OUTPUT 0
L	L	H
H	H	L

where: t_n = bit time before CLOCK pulse

where: t_{n+1} = bit time after CLOCK pulse

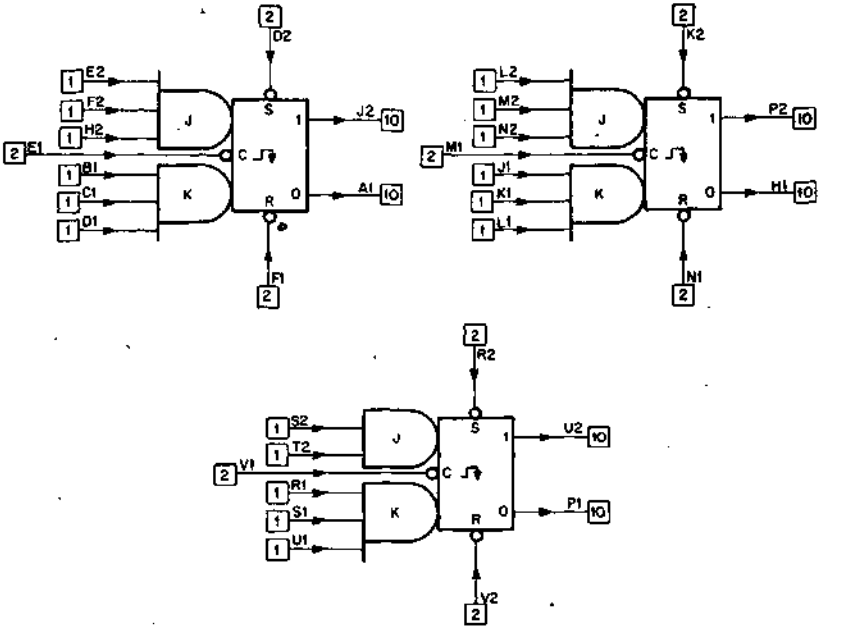
NOTE: The M246 module also contains a +3V logic High source at pin V1 which can be used to tie up to 50 M Series inputs High.

M202
TRIPLE J-K FLIP-FLOP

FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	57	A2
GND		C2, T1

The M202 contains three J-K flip-flops augmented by multiple-input AND gates.

APPLICATIONS

- For general use as gated control flip-flops or buffers.

FUNCTIONS

See M207 for detailed description of logical operation. The J-K flip-flops used in this module are identical to flip-flops used in the M207 except on the M202 clock inputs, J-K inputs, direct clear, direct set and both output lines for each flip-flop are independent.

PRECAUTION

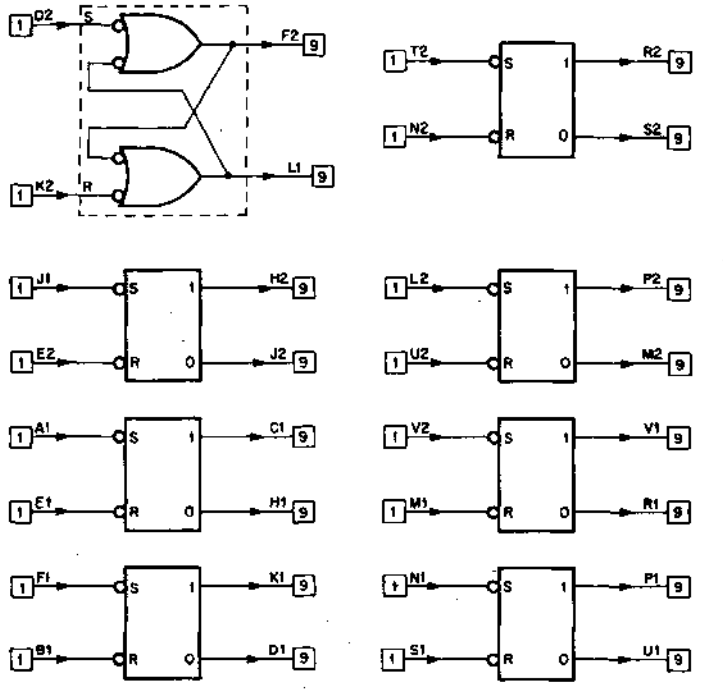
Set and clear lines should be tied to "1" level when not used.

M203
8 R/S FLIP-FLOPS

FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	55	A2
GND		C2, T1

The M203 is made up of 8 R/S-type flip-flops. Each flip-flop is made up of two 2-input NAND gates with cross-coupled outputs.

APPLICATIONS

- R/S flip-flops provide an inexpensive method of storage.

PRECAUTIONS

Care must be taken not to place the SET and RESET inputs LOW at the same time. The last of the inputs to go HIGH will determine the final state of the flip-flop.

SPECIFICATIONS

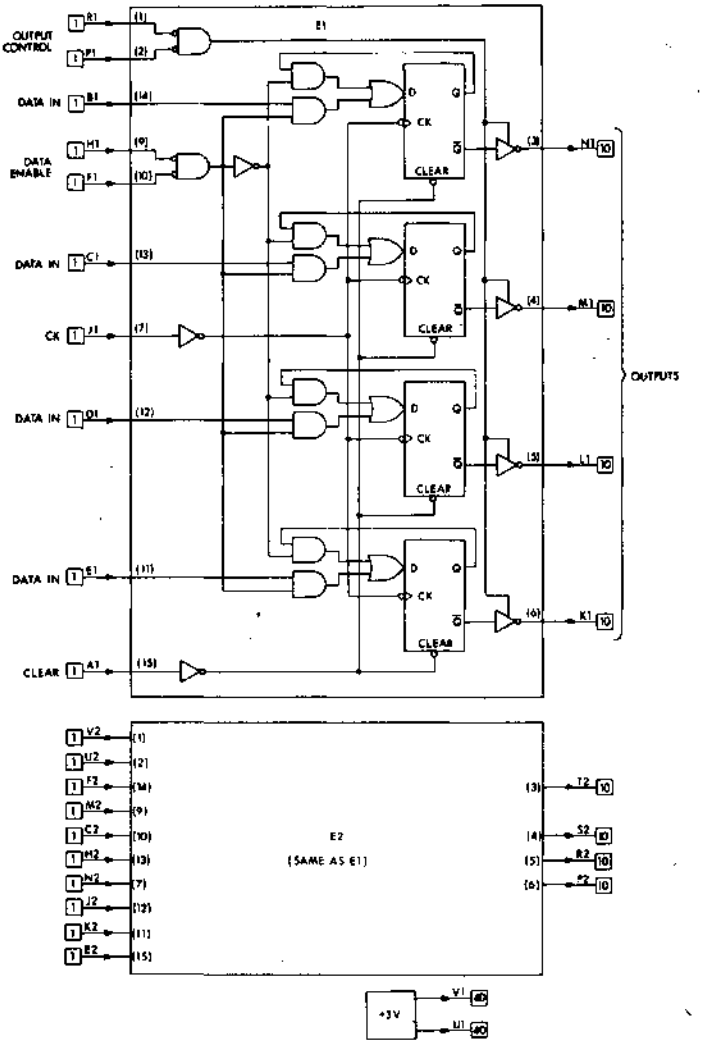
The propagation delay of the M203 is approximately 30 ns.

M2001
DUAL 4-BIT TRI-STATE REGISTERS

FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single



The M2001 is a dual, 4-bit register module consisting of D-type flip-flops and input and output gating. Each of the module outputs contains a tri-state circuit capable of driving low-impedance, high-capacitance loads without the use of pull-up or interface components. The third state of the output is a high-impedance state and is selectable by logic levels to the input of the module. This state effectively disconnects the register outputs from the bus when no information transfer is required.

Data is entered into each D-type flip-flop from an associated DATA IN line and is controlled by the DATA ENABLE gate. When both DATA ENABLE inputs are Low, the information on the data lines will be entered into the respective flip-flop on the next positive transition of the clock (CK) input.

The Q output from each flip-flop is inverted and controlled by the tri-state driver amplifier. Where either or both input to the output control gate is a High logic level, the outputs of the module are disabled to the high-impedance state; however, the sequential operation of the flip-flops are not affected.

When the CLEAR input to the logic element is High, each associated flip-flop is held in the reset condition, and the module outputs will remain in the Low state.

FUNCTION TABLE

DATA IN	CLOCK	CLEAR	DATA ENABLE		OUTPUT
			1	2	
L	L to H	L	L	L	L
H	L to H	L	L	L	H
X	X	H	X	X	L
X	L	L	X	X	Qo
X	L to H	L	H	X	Qo
X	L to H	L	X	H	Qo

L = Low level (steady)
H = High level (steady)
L to H = Low to high level transition
X = Irrelevant of any input including transition
Qo = Level of module output before steady state input conditions were established.

APPLICATIONS
Provides a total of eight bits of data storage and outputs to interface directly to system bus. All input and output signals are through edge board connector.

FUNCTION
Refer to Function Table for input and output signal and level requirements.

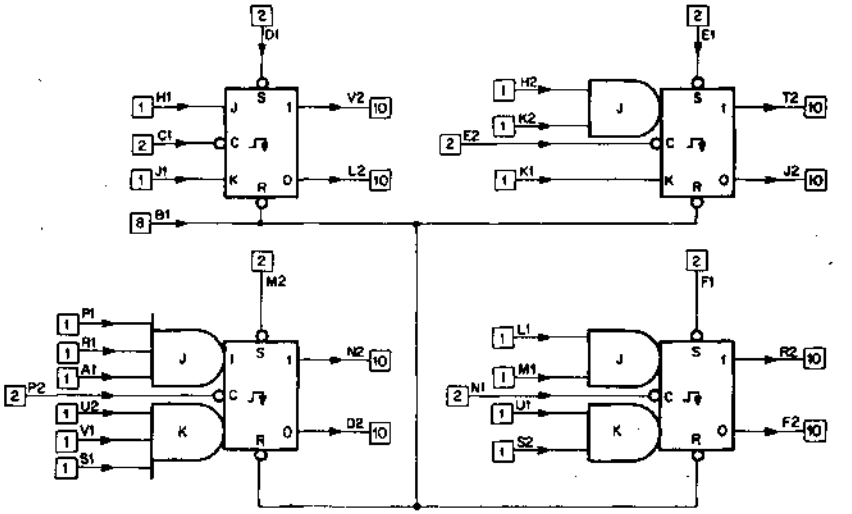
SPECIFICATIONS
Input Voltage — 4.5 Vdc (min.), 5.2 Vdc (max.)
Input Current — 72.0 mA (max.)
High Level Output Current — 5.2 mA (max.)
Low Level Output Current — 16 mA (max.)

M204
GENERAL-PURPOSE BUFFER AND COUNTER

FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	74	A2
GND		C2, T1

The M204 contains four J-K type flip-flops, augmented by multiple-input AND gates. The gating scheme permits the formation of counters of most moduli up to 16, by simple connector wiring. Clock, present, and input lines for each flip-flop are independent. A common CLEAR input is provided.

APPLICATIONS

- For general use as gated control flip-flops or buffers
- Counters
- Shift Registers

FUNCTIONS

Input information is transferred to the outputs when the threshold point is reached on the trailing (negative going voltage) edge of the clock pulse.

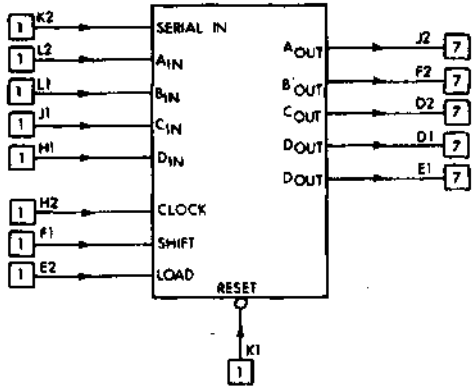
Logical operation of the J-K flip-flops used in this module is identical to the M207 (described in detail) except for the addition of preset inputs to the M204.

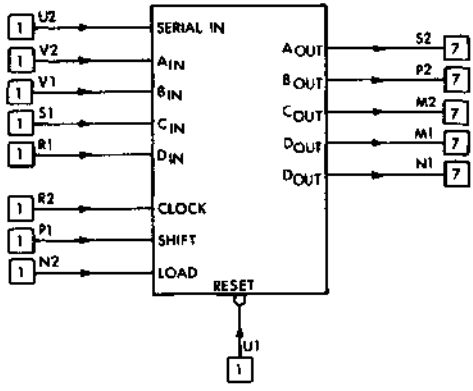
M245
DUAL 4-BIT
SHIFT REGISTER

FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single





The M245 module consists of two 4-bit shift registers with both serial and parallel data entry capability. They are shift-right only registers; that is, the output data is shifted from A toward D.

Three control modes are possible: serial shift right, parallel enter mode, and no change or hold mode. These control modes are chosen by inputs at the SHIFT and LOAD lines as shown in the Truth Table.

In the serial mode of operation, data present at the SERIAL INput, when the SHIFT input is High, is loaded on the Low-going edge of the CLOCK pulse.

In the parallel entry mode, data present at the data inputs A IN through D IN, when the LOAD line is High, is loaded on the Low-going edge of the CLOCK pulse.

The hold mode is created by holding both the LOAD and SHIFT lines Low. By doing this, the CLOCK pulse will have no effect on the output, regardless of data present at the SERIAL INputs or DATA INputs.

A RESET line has been provided for the registers which will clear the internal flip-flop circuitry.

SPECIFICATIONS

Transfer Rate	= 10 MHz (max)
SHIFT Set-up Time	= 50 ns (min)
LOAD SET-up Time	= 50 (min)
DATA IN Set-up Time	= 25 ns (min)

Propagation Delay

From:	To:
CLOCK	Output (HIGH or LOW) = 50 ns (max)

TRUTH TABLE

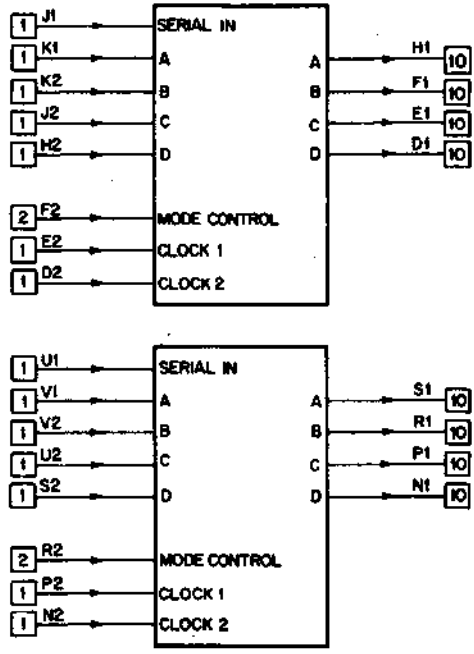
CONTROL STATE	LOAD	SHIFT
Hold	L	L
Parallel Entry	H	L
Serial Shift Right	L	H

M248
DUAL 4-BIT
MULTIPURPOSE SHIFT REGISTER

FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	130	A2
GND		C2, T1

The M248 module consists of two 4-bit Shift registers—multipurpose in the fact that they are capable of either serial or parallel entry, shifting right, or with simple external connections, shifting left.

When a logic LOW is applied to the MODE CONTROL input, a shift right operation is performed by clocking at the CLOCK 1 input. In this mode, serial data is entered at the SERIAL INput. CLOCK 2 and parallel inputs A through D are inhibited.

When a logic HIGH is applied to the MODE CONTROL input, it allows entry of parallel data through inputs A through D and CLOCK 2. This mode permits parallel loading of the register or, with external interconnection, shift left operation. In this mode, shift left can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop; that is, D output to C input, etc., and serial data is entered at input D.

Two clock inputs are available which permit separate clock sources to be used for the shift right and shift left modes. If both modes can be clocked from the same source, the clock input may be applied to both CLOCK 1 and CLOCK 2. The transfer of information to the output pins occurs when the clock input goes from a logic High to a logic Low.

SPECIFICATIONS

Shift Freq = 10 MHz (max)

Propagation Delay

From:	To:
CLOCKS	High or Low Output = 40 ns (max)

Set-up Time:

SERIAL Input A, B, C, D = 20 ns (min)

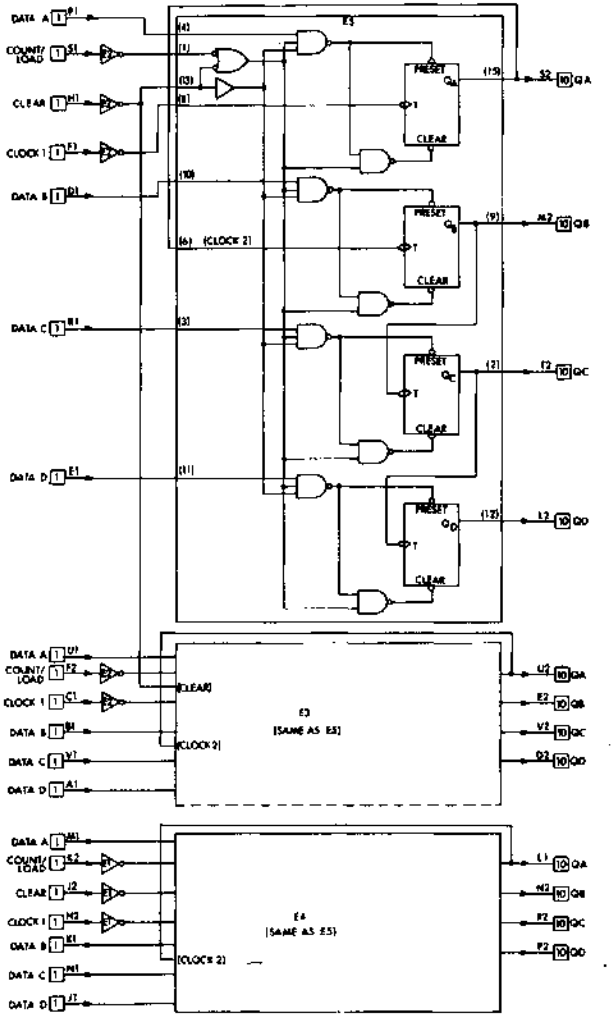
MODE CONTROL with respect to CLOCKS = 25 ns (min)

M239
THREE 4-BIT COUNTER/REGISTER

FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA	Pins
+5	70.0	A2
GND		C2, T1

The M239 Module consists of three high-speed, 4-flip-flop stage elements suitable for use as a storage register or a counter. Each of the 12 flip-flops has a data line input, and data information is entered by a COUNT/LOAD signal associated with each 4-bit stage. The output of the flip-flops assumes the logic state of the data inputs when the COUNT/LOAD input signal is High. When the COUNT/LOAD signal is Low, the data inputs are disabled, provided the clock inputs are inactive.

The Q_A output of each latch within a 4-stage element is connected to the toggle (T) input of the following latch. This allows the module to be used as a high-speed counter or serial-to-BCD converter.

The counters will accept frequencies of 0-50 MHz at the CLOCK 1 input, and the transfer of information to the outputs occurs at the positive-going edge of this clock pulse.

One CLEAR input is common to the eight latches in elements 1 and 2, and one CLEAR input is common to the four latches in the third element. When the CLEAR signal becomes a High logic level, all associated latch outputs will become Low regardless of the CLOCK 1 input level.

APPLICATIONS

Provides 12-bit data storage or a serial counter with 12-BCD outputs. All inputs and outputs are TTL or DTL compatible.

FUNCTION

When operated as a serial counter, the Q_D output of a 4-latch element must be connected to the CLOCK 1 input of the following 4-latch element. The separate CLEAR inputs may also be externally connected to reset all latch outputs using one CLEAR input signal (High transition). Output Q_A maintains 10 unit load capability in addition to driving the CLOCK 2 input. Refer to the Function Tables for the output levels of each count.

SPECIFICATIONS

Input Voltage (max.): 5.0 Volts ± 5%
Clock Frequency: 0-50 MHz

FUNCTION TABLE

CLOCK PULSE	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

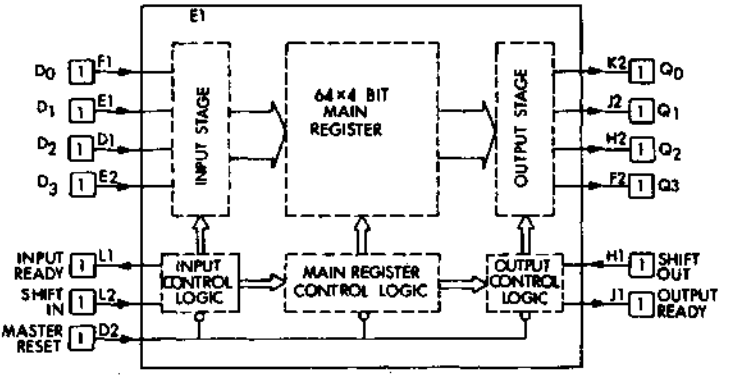
NOTE: Output count continues in sequence when Q_D output is connected to the clock 1 input of next 4-latch element.

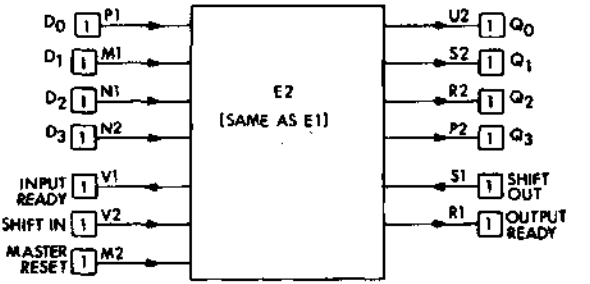
M2500
DUAL 64 WORD X 4 BIT FIRST-IN FIRST-OUT SERIAL MEMORY

FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single





Volts	Power mA (max.)	Pins
+5	100	A2
−12	23	J1
GND		C2, T1

The M2500 Module provides storage for 64 4-bit words in each of two memory elements. The words are stored and read asynchronously on a first-word-in, first-word-out basis. By series coupling the two memory elements, the total storage capacity can be increased to 128 4-bit words. The two memory elements can also be paralleled, using external logic, to form storage for 64 8-bit words.

FUNCTION

The first 4-bit word is entered into the memory register by initiating a High SHIFT IN pulse when the INPUT READY signal from the memory is High. With no data word previously stored in the first location of memory, the INPUT READY signal will be High. As the word enters the first memory location, the INPUT READY signal becomes Low and remains Low until the SHIFT IN pulse is brought Low. The Low transition of the SHIFT IN pulse transfers the first 4-bit word into the second memory location, and the INPUT READY signal again becomes High. The internal control logic then sequences the word to the first-out or 64th memory location which causes the OUTPUT READY signal to become High. This indicates that the first word entered is available to be read at the output. The second 4-bit word can then be entered into memory and is automatically stacked at the output. To read a word from memory and shift the next word to the output, a High SHIFT OUT pulse is required and causes the previously High OUTPUT READY signal to become Low. The data is shifted out by the trailing edge of the SHIFT OUT pulse when the OUTPUT READY signal is Low. The next 4-bit word is then automatically shifted to the 64th location causing the OUTPUT READY signal to again become High. When all locations are empty, OUTPUT READY will remain Low. When all the memory locations are full, the INPUT READY signal is held Low until a word is read, resulting in a vacant location.

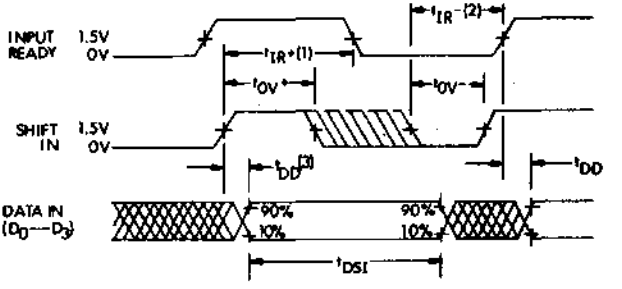
APPLICATIONS

The M2500 can be used as a synchronous or asynchronous serial storage device or as a buffer unit for data communication between devices operating at different data rates. The M2500 can be serial connected to increase the total number of 4-bit memory locations or connected in parallel to extend the word lengths. Both data and control inputs and outputs are direct TTL and DTL compatible.

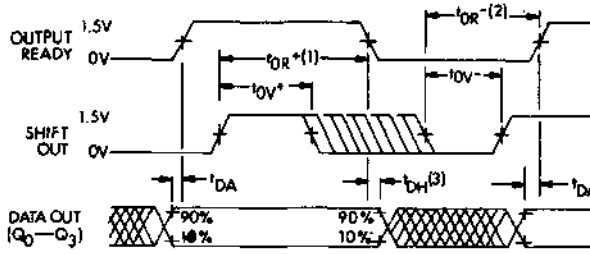
FUNCTION

The following input/output diagrams indicate the timing relationships and logic levels required to write into or read data from memory.

INPUT TIMING



OUTPUT TIMING



t_{IR}^+ (Input Ready HIGH Time)	300 ns (typ.)
t_{IR}^- (Input Ready LOW Time)	300 ns (typ.)
t_{OV}^+ (Control Overlap HIGH Time)	100 ns (min.)
t_{DSI} (Data Input Stable Time)	400 ns (min.)
t_{DD} (Data Input Delay Time)	25 ns (min.)
t_{OR}^+ (Output Ready HIGH Time)	300 ns (typ.)
t_{OR}^- (Output Ready LOW Time)	450 ns (typ.)
t_{DH}^- (Data Hold Time)	75 ns (min.)

NOTES:

t_{IR}^+ is referenced to the positive going edge of IR or SI, whichever occurs later.

t_{IR}^- is referenced to the negative going edge of IR or SI, whichever occurs later.

t_{DD} is referenced to the positive going edge of IR or SI, whichever occurs later.

t_{OV}^+ is referenced to the positive going edge of IR or SI, whichever occurs later. Control signals include Input Ready, Shift In, Output Ready, and Shift Out.

Data must be stable for t_{SOI} or t_{IR}^+, whichever is shorter.

Input data must remain stable during timing window t_{SOI}. Both SI and IR must be HIGH for t_{OV}^+.

t_{OR}^+ is referenced to the positive going edge of OR or SO, whichever occurs later.

t_{OR}^- is referenced to the negative going edge of OR or SO, whichever occurs later.

t_{DH} is referenced to the negative going edge of OR or SO, whichever occurs later.

t_{OV}^+ is referenced to the positive going edge of IR or SI, whichever occurs later.

Both SO and OR must be HIGH for t_{OV}^+.

Inputs

SHIFT IN	A High on this input causes INPUT READY to go Low and data to the shifted into the memory. Data will begin to shift to the last empty location when this input is brought Low again. Minimum pulse width is 100 ns. Data must be valid within 25 ns after SHIFT IN goes High. SHIFT IN must only be brought High when INPUT READY is High. Minimum Low time for SHIFT IN is 100 ns.
D0—D3	Data inputs. Data must be valid within 25 ns after SHIFT IN goes High and should remain valid for at least 400 ns.
SHIFT OUT	A High on this input initiates the output shifting process. Data will remain valid until 70 ns after both SHIFT OUT and OUTPUT READY have gone Low. Minimum pulse width is 100 ns. SHIFT OUT must remain Low for at least 100 ns.
MASTER RESET	Clears all memory locations.

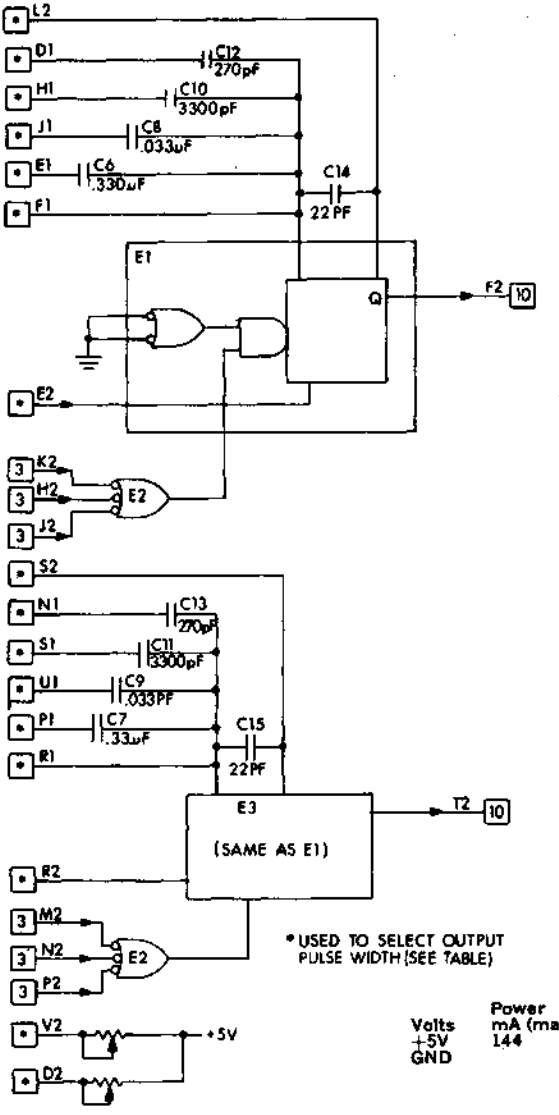
Outputs

INPUT READY	Indicates when data may be loaded into the memory. Goes Low 300 ns (typ) after the leading edge of SHIFT IN and goes High again when the next data word may be loaded. INPUT READY remains Low when the memory is full.
OUTPUT READY	Indicates when data is valid at the output of the memory. OUTPUT READY goes Low 300 ns (typ) after the leading edge of SHIFT OUT and goes High again when the next word has been shifted to the output. OUTPUT READY remains Low when the memory is empty.
Q0—Q3	Data outputs. Data is valid at the outputs whenever OUTPUT READY is High, even if SHIFT OUT is Low. Data will change 75 ns after OUTPUT READY goes Low. Typical propagation time from input to output of an empty memory is 10 μs.

M3020
DUAL DELAY MULTIVIBRATORS

TIME RELATED

M SERIES



Volts	Power mA (max.)	Pins
+5V	144	A2
GND		C2, T1

The M3020 Module contains two monostable multivibrators, each of which is activated by the output of a Schmitt Trigger circuit. A low input transition on any one of the three inputs to the Schmitt Trigger circuit produces a positive output pulse and triggers the multivibrator. The Schmitt Trigger circuit provides a hysteresis current which prevents the multivibrator from being triggered erroneously by noise signals at the input.

When activated, the multivibrator produces a positive pulse at the output. The width of the pulse is variable from 50 ns to 40 sec and is selected by the external connections to capacitors mounted on the M3020 and by the variable Vcc available.

The M3020 contains two delays (one-shot multivibrators) which are triggered by a level change from HIGH to LOW or a pulse to LOW whose duration is equal to or greater than 50 ns. When the input is triggered, the output changes from LOW to HIGH for a predetermined length of time and then returns to LOW.

The delay time is adjustable from 50 ns to 7.5 ms using the internal capacitors and can be extended by adding an external capacitor.

APPLICATIONS

- Time delays
- Variable width pulses

FUNCTIONS

Delay Range: The basic DELAY RANGE is determined by an internal capacitor. The delay range may be increased by selection of additional capacitance which is available by connecting various module pins or by the addition of external capacitance. An internal potentiometer can be connected for fine delay adjustments within each range or an external resistance may be used. If an external resistance is used, the combined resistance of the internal potentiometer and the external resistance should be limited to 10,000 ohms.

Delay Range	Capacitor Value (Internal)	Interconnections Required	
		Delay E1	Delay E3
50 ns — 750 ns	22 pF	None	None
500 ns — 7.5 μs	270 pF	D1 — L2	N1 — S2
5 μs — 75 μs	3300 pF	H1 — L2	S1 — S2
50 μs — 750 μs	.033 μF	J1 — L2	U1 — S2
500 μs — 7.5 ms	.33 μF	E1 — L2	P1 — S2

Adjustable Delays: Connect pins D2 to E2 for delay 1 and V2 to R2 for delay 2 in order to add the internal potentiometers. NOTE: If there is no external pot, these pins must be jumpered.

Without a potentiometer, the delay will not recover. An external potentiometer of less than 10 K ohms can be used by connecting it between E2 or R2 and ground pin C2. Use of an external adjustment resistor will cause some increase in jitter. It is recommended that leads to an external potentiometer be twisted pairs and as short as possible.

PRECAUTIONS
Care should be exercised in the selection of external capacitors to assure low leakage as leakage will affect the time delay.

SPECIFICATIONS
Trigger Input Fall Time: Must be less than 400 ns

Recovery Time: Defined as the time all inputs must remain HIGH before any input goes LOW to trigger the delay

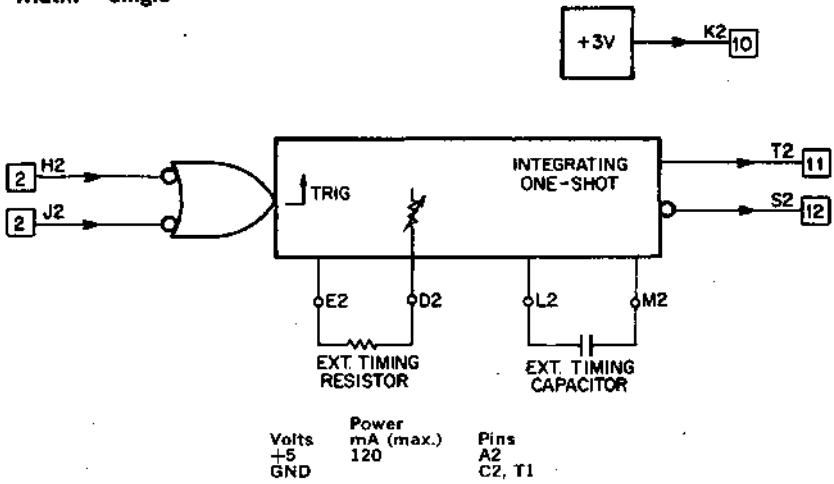
1. Without external capacitance: 30 ns min.
2. With external capacitance: 300 C ns min. where C is in nanofarads

M306
INTEGRATING ONE SHOT

TIME RELATED

M SERIES

Length: Standard
Height: Single
Width: Single

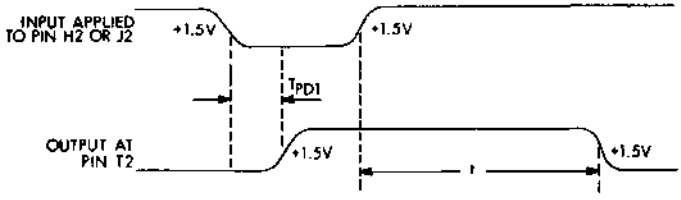


Volts	Power mA (max.)	Pins
+5	120	A2
GND		C2, T1

The M306 is a zero-recovery-time integrating monostable multivibrator with complementary outputs. The M306 has the ability to respond to an input even while in the active state, so that successive inputs above a preset frequency can postpone the return to the inactive state indefinitely.

FUNCTIONS

The operation of the M306 is illustrated in the timing diagram shown below:



The integration period is measured from the trailing edge of the input pulse to the trailing edge of the output pulse. The approximate integration time may be calculated by the following:

$$t \sim .68\,(R + 800\,\Omega)\,(C + 75 \times 10^{-12}F) + 70 \times 10^{-9}\ \text{Sec.}$$

where R is in ohms and C is in farads. The width of the input pulse is independent of the integration time.

Timing Capacitors: Coarse adjustment of the integration period is accomplished by customer-supplied capacitors which may be attached to module pins L2 and M2. When using polarized capacitors, the positive terminal should be connected to pin L2. Two split lugs are provided on the module for those customers who would like to permanently install the capacitor on the module itself. The minimum equivalent parallel resistance of capacitor leakage should always exceed 250K ohms.

Timing Resistance: Fine adjustment of the timing period may be accomplished by a multiturn potentiometer provided on the module. Provision is also made to allow the customer to connect an external timing resistor or potentiometer between pins D2 and E2. When an external potentiometer is used, care should be taken to prevent the coupling of externally generated electrical noise into the module. The maximum resistance of the timing resistance, including the internally provided potentiometer, should not exceed 25,000 ohms. If an external timing resistor is not used, pins D2 and E2 must be connected together.

SPECIFICATIONS

Trigger Duration: An input pulse of 30 ns will trigger the M306. TPD1 = 40 ns max.

Output Duration: The minimum pulse width is 225 ns and maximum pulse width is limited only by capacitor leakage (40 sec is a typical maximum).

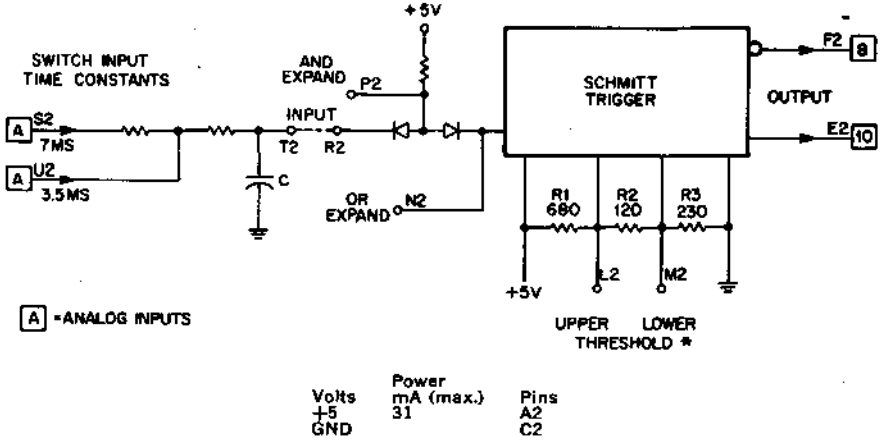
Stability: The inherent temperature stability of the M306 is normally —.06% per degree C, exclusive of the temperature coefficient of the timing capacitor.

M501
SCHMITT TRIGGER

TIME RELATED

M SERIES

Length: Standard
Height: Single
Width: Single



The M501 is a Schmitt Trigger with variable thresholds and complementary positive logic outputs.

APPLICATIONS

- Switch Filter
- Pulse Shaper
- Threshold Detector

FUNCTIONS

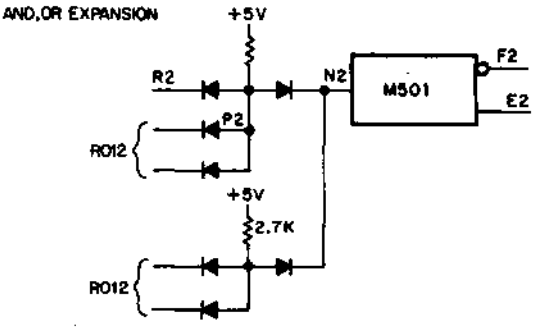
The input on pin R2 is compared with the thresholds set on pins L2 and M2 UPPER and LOWER respectively.

Pin F2 goes to LOW when the input on R2 rises above the UPPER THRESHOLD, having been below the LOWER THRESHOLD.

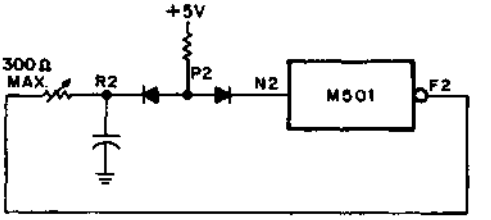
Pin F2 rises to +3 volts when the input on R2 falls below the LOWER THRESHOLD, having been above the UPPER THRESHOLD.

Pin E2 is the complement of F2.

Miscellaneous Input Functions: AND and OR expansion may be performed on P2 and N2. Modules R001 and R012 provide the diodes required. An integrator is provided on the input, allowing switches to be connected to the Schmitt Trigger with contact bounce effects eliminated. Two switch time constants are provided. Inputs to pin S2 result in a 7 ms time constant to pin U2 3.5 ms.



Oscillator Connection: Connecting a resistor from output pin F to input pin R with pin T tied to pin R forms an oscillator.



SPECIFICATIONS

Input Signal Swing: The voltage on pin R2 is limited to plus or minus 20 volts.

Thresholds: The UPPER and LOWER THRESHOLDS are preset at 1.7 and 1.1 volts. They may be modified by the addition of a resistor in parallel with the internal network; however, the UPPER THRESHOLD must not exceed 2.0 volts or the LOWER THRESHOLD fall below 0.8 volts.

R	IN	PARALLEL WITH	R2 — THRESHOLD CLOSER
R		PARALLEL	R1 — UPPER RISES
R		PARALLEL	R3 — LOWER FALLS

Input Pin R2 Loading: 2.7K ohms to +5 volts or 1.8 mA at ground.

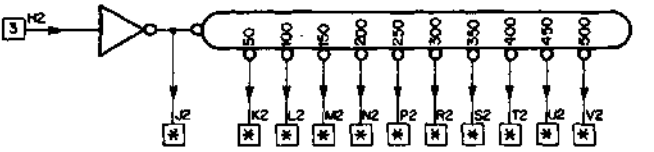
Pin P2 AND EXPAND input
Pin N2 OR EXPAND input
Pin S2 RC SWITCH input filter 7 ms
Pin U2 RC SWITCH input filter 3.5 ms
Pins L2, M2 are available for threshold modification

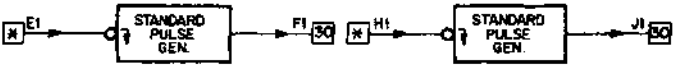
M310
DELAY LINE

TIME RELATED

M SERIES

Length: Standard
Height: Single
Width: Single





****SEE TEXT**

Volts	Power mA (max.)	Pins
+5	89	A2
GND		C2, T1

The M310 consists of a tapped delay line with associated circuitry and two pulse amplifiers. The total delay is 500 nanoseconds with taps available at 50 nanosecond intervals.

APPLICATIONS

- Timing pulse trains
- Pulse spacing

FUNCTIONS

The time delay is increased when the amplifier is connected to the delay line taps in ascending order as follows: J2, K2, L2, M2, N2, P2, R2, S2, T2, U2, and V2. The tap J2 yields the minimum delay and the tap V2 yields the maximum delay.

Loads J2-V2 designed to be loaded only by E1 or H1. They will not drive standard TTL loads.

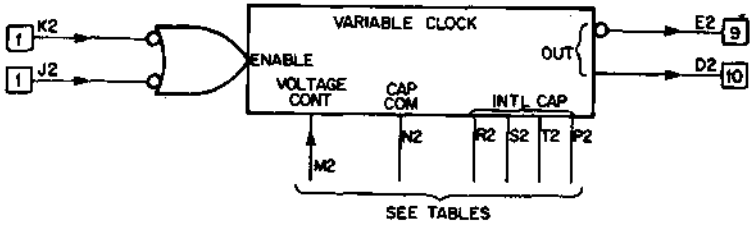
The pulse amplifiers are intended to be used to standardize the outputs of the delay line. The output of the pulse amplifier is a positive pulse whose duration is typically 50 to 200 nanoseconds. These amplifiers are not intended to be driven by TTL IC logic.

M401
VARIABLE CLOCK

TIME RELATED

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	80*	A2
GND		C2, T1

* using printed circuit board revision E or later

The M401 Variable Clock is a stable RC-coupled multivibrator which produces standard timing pulses at adjustable repetition rates.

Repetition rate is adjustable from 175 Hz to 10 MHz in five ranges. Internal capacitors, selected by jumper pin connections, provide coarse frequency control. An internal potentiometer provides continuously variable adjustment within each range.

A 0 to 10 volt control voltage will vary the frequency over about 30% of each frequency range.

APPLICATIONS

This module is intended for use as the primary source of timing signals in a digital system.

FUNCTIONS

Start Control: A two-input OR gating input is provided for start-stop control of the pulse train. A level change from HIGH to LOW with fall time less than 400 ns is required to enable the clock.

Frequency Range:

Frequency Range	Interconnections Required	
1.5 MHz to 10 MHz	(100 pf)	NONE
175 KHz to 1.75 MHz	(1000 pf)	N2 — R2
17.5 KHz to 175 KHz ➡	(.01 µfd)	N2 — S2
1.75 KHz to 17.5 KHz ⬅	(0.1 µfd)	N2 — T2
175 Hz to 1.75 KHz	(1.0 µfd)	N2 — P2

Fine Frequency Adjustment: Controlled by an internal potentiometer. No provision is made for any external connections. An external capacitor may be added by connection between pins N2 and C2.

Voltage Control of Frequency: The M401 may also be voltage controlled by applying a control voltage to pin M. This feature is available only in M401 modules using printed circuit board revision E or later. The voltage applied to pin M should be limited to the range of 0 volts to +10.0 volts. This voltage swing will allow the frequency to be shifted by approximately 30 percent in the frequency range using the internal capacitors of 1.0, 0.1, 0.01 and 0.001 μF. If the voltage applied to pin M is dc or low frequency (below 1 kHz), pin M will appear approximately as a +1.0 volt source with a Thevenin resistance of 800 ohms. Modulating the M401 with a 10 volt P-P signal about a center frequency, as derived by the application of a mean voltage of +5 volts to pin M, will yield a typical frequency excursion in excess of plus or minus 15% about the center frequency. Typical frequency excursions which may be obtained are shown below:

Voltage applied to Pin M	CAPACITOR			
	1.0 ufd.	0.1 ufd.	0.01 ufd.	.001 ufd.
0	1.000	10.00	100.0	1000
+1	1.054	10.49	104.6	1036
+2	1.101	10.94	109.2	1071
+3	1.147	11.39	113.6	1108
+4	1.193	11.83	118.0	1142
+5	1.238	12.26	122.2	1181
+6	1.282	12.69	126.4	1271
+7	1.325	13.10	130.4	1295
+8	1.368	13.50	134.2	1312
+9	1.408	13.87	137.7	1322
+10	1.443	14.20	140.9	1323
				Output frequency in KHz

SPECIFICATIONS

Maximum delay from enabling inputs to output E2 is 50 nanoseconds. The output pulse width is 50 nanoseconds.

$300 \times 16 = 4,800$

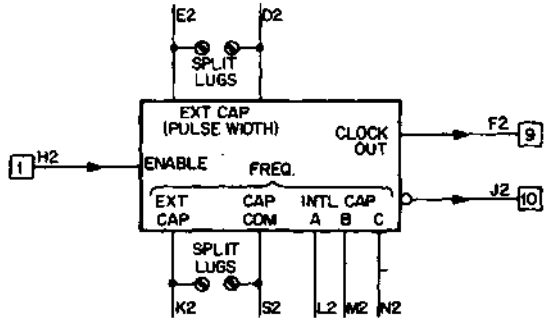
$1350 \times 16 \quad 21,600$

M403
RC MULTIVIBRATOR CLOCK

TIME RELATED

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	70	A2
GND		C2, T1

The M403 is an RC Multivibrator Clock which produces standard 10-microsecond timing pulses at repetition rates adjustable from 1 kHz to 50 kHz in three ranges. Internal capacitors, selected by jumper pin connections, provide coarse frequency control, while an internal potentiometer provides continuously variable adjustment within each range.

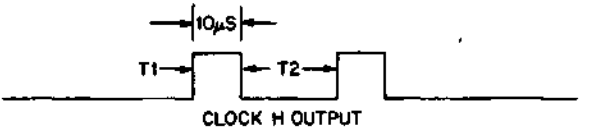
APPLICATIONS
This module can be used as a source of digital timing signals.

FUNCTIONS
ENABLE Input: The clock circuit is enabled by a HIGH level on pin H2. If a LOW level is applied to pin H2, the clock output at F2 will time out and return to ground and the output at pin J2 will time out and go HIGH. To prevent an erroneous count, pin H2 should not be retriggered for one complete period. This will allow the circuit to settle.

Selecting Frequency Range: The frequency range is selected by jumpers at backplane pins:

FREQUENCY RANGE	INTERCONNECTION REQUIRED
1 kHz to 5 kHz	N2 — S2
5 kHz to 20 kHz	M2 — S2
20 kHz to 50 kHz	L2 — S2

Lowering Frequency: If frequencies below the capabilities of this circuit are necessary, external capacitance can be added. Time 2 (see illustration) can be changd by installing capacitors to the split lugs provided or between pins K2 and S2. New timing values can be calculated using the following equation:



$T2 = 0.32 RC (1 + 0.7/R)$

T2 is in seconds, R is in ohms, and C is in farads. The internal potentiometer varies between 5.1K and 50K ohms.

Increasing Pulse Width: Larger pulse widths can also be obtained by adding capacitance to the other set of split lugs provided or between pins E2 and D2. The same equation as above may be used for T1 with the following exception:

$$C = 4.7 \text{ picofarads} + \text{capacitance added}$$

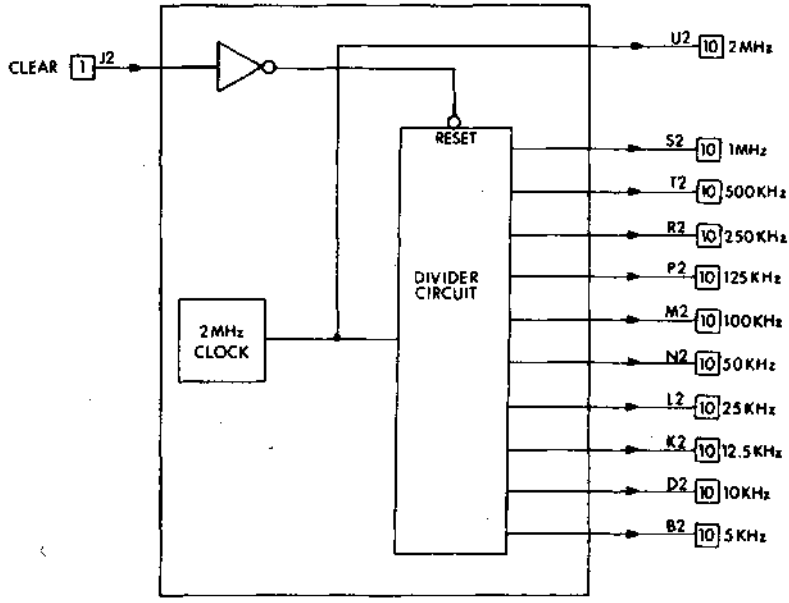
SPECIFICATIONS
Rise Time: 25 ns (max.)
Fall Time: 25 ns (max.)

M404
CRYSTAL CLOCK

TIME RELATED

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	535	A2
GND		C2, T1

The M404 clock contains a 2 MHz crystal oscillator and frequency dividers.

A HIGH on the CLEAR input clears the frequency divider and all outputs go LOW except the 2 MHz output, which is not affected.

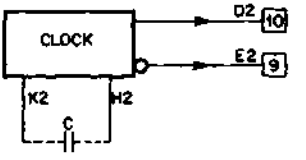
SPECIFICATIONS
Accuracy: Maximum error from specified output frequency is 0.01% between 0 degrees C and +55 degrees C.

M405
CRYSTAL CLOCK

TIME RELATED

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	50	A2
GND		C2, T1

The M405 employs a crystal oscillator to provide a highly stable, precisely known frequency between 5 kHz and 10 MHz. The frequency within this range may be specified by the user.

APPLICATIONS

- Stable clock frequencies

FUNCTIONS

Outputs: Outputs at pins D2 and E2 are respectively positive and negative going 50 ns pulses. Pulses at pins D2 and E2 are time shifted by one gate delay with the negative pulse at pin E2 leading the positive pulse at D2 by a maximum of 20 ns. The output pulse width can be modified by the addition of an external capacitor between pins K2 and H2. This capacitor will increase the output pulse width by approximately 1 ns per 2.5 pF of additional capacitance.

SPECIFICATIONS

Frequency Stability: 0.01% of specified value between 0 degrees C and +55 degrees C.

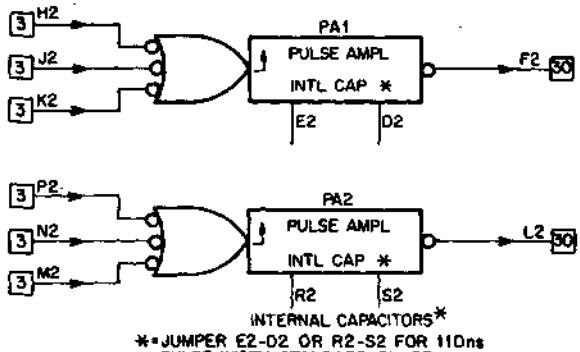
Ordering Information: When ordering the M405, always specify frequency. Allow six weeks for delivery.
Standard Stock Frequencies: 1.333 MHz, 2.000 MHz, 5.000 MHz.

M602
PULSE AMPLIFIER

TIME RELATED

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	213	A2
GND		C2, T1

The M602 contains two pulse amplifiers which provide power amplification, standardize pulses in amplitude and width, and transform level changes into a standard pulse.

FUNCTIONS

A negative pulse output is produced when the input is triggered by a transition from HIGH to LOW. An internal capacitor is brought out to pin connections to permit the standard 50 ns output pulse to be increased to 110 ns (nominal).

SPECIFICATIONS

Propagation Time: 30 ns max. between input and output thresholds.

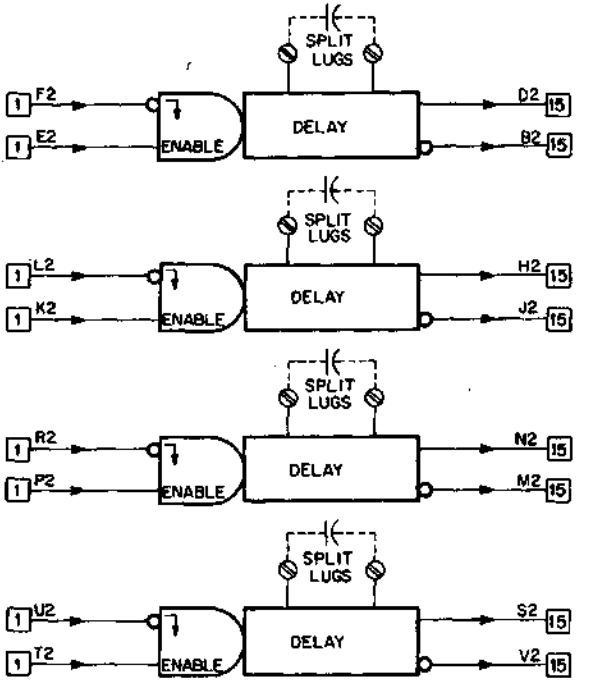
Recovery Time: Equal to that of the output pulse width. The input must have a fall time (10% to 90% points) of less than 400 ns and must remain below 0.8 volts for at least 30 ns. Maximum PRF is 10 MHz.

M671
M TO K CONVERTER

TIME RELATED

M SERIES

Length: Standard
Height: Single
Width: Single

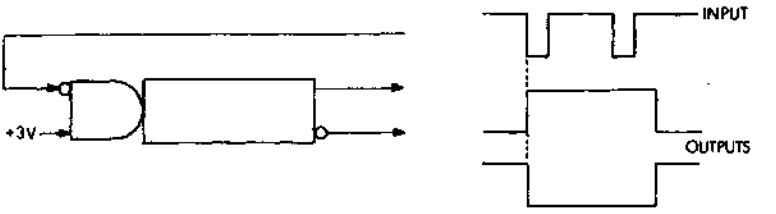


Volts	Power mA (max.)	Pins
+5	112	A2
GND		C2

The M671 M Series to K Series Converter contains four pulse stretching circuits which can convert an M Series input pulse of duration exceeding 50 ns to complementary K Series output pulses of 10 to 15 μs.

FUNCTIONS

Triggering: When the ENABLE input is HIGH, the delay is triggered by the negative-going edge of the trigger input pulse:



This circuit is insensitive to input transitions during its timeout period as shown in the example above.

Increasing Output Pulse Width: Non-electrolytic capacitors can be connected to the split lugs provided in each circuit if K Series output pulse widths longer than 15 μs are desired. Pulses of up to 40 seconds are possible using this technique. When capacitance is added, the output pulse width is increased by 6400 C seconds where C is the capacitance added in farads.

Precautions: Unused inputs should be connected to logic levels that will hold them in their unasserted states. Unused inputs that would be asserted High should be grounded. Unused inputs that would be asserted Low should be connected to a source of logic High. Also refer to "Unused Inputs" in the alphabetical index.

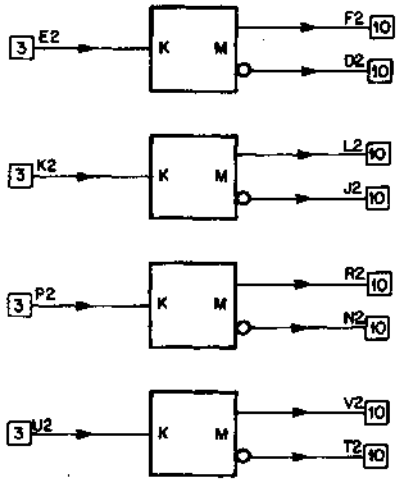
SPECIFICATIONS
Output drive: Each output is capable of driving a 15 mA load.

M521
K TO M CONVERTER

TIME RELATED

M SERIES

Length: Single
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	56	A2
GND		C2

The M521 K Series to M Series Converter contains four circuits which can convert any K Series input to complementing M Series outputs.

APPLICATIONS

- Rise Time Conversion — K to M Series

FUNCTIONS

Typically, a K Series input would have a 7 μs rise time and a 1.5 μs fall time. The M521 speeds both these rise and fall times to approximately 15 ns. The input circuit has built-in hysteresis and is slowed to a maximum frequency of 100 KHz.

SPECIFICATIONS

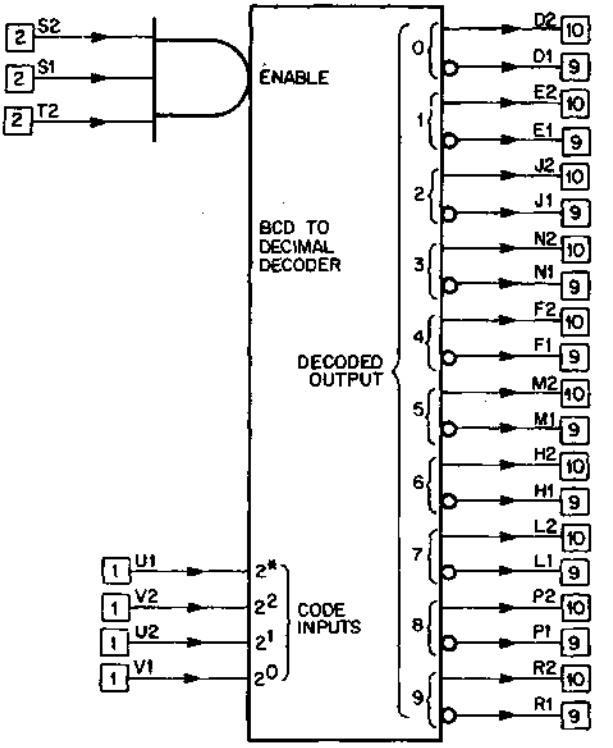
Each input represents three K Series unit loads.

M161
BINARY TO OCTAL/DECIMAL DECODER

NUMERIC

M SERIES

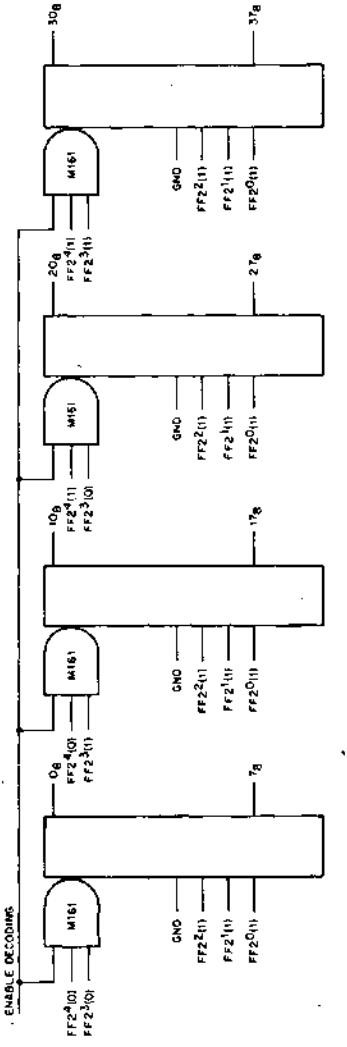
Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	120	A2
GND		C2, T1

The M161 is a functional decoding module which can be used as a binary-to-octal or binary-coded decimal (8421 or 2421 codes) to decimal decoder. In the binary-to-octal configuration, up to eight M161's can be linked together to provide decoding of up to six bits. Three ENABLE inputs are provided for selective enabling of modules in decoders of more than one digit. In the octal mode, the bit 2* input is connected to ground, which automatically inhibits the 8 and 9 outputs. Connections for a 5-bit binary/octal decoder (4 modules) are shown below. The figure assumes that the inputs to the decoder

are the outputs of flip-flops such as FF2° (1), 1 output side; and FF2° (0), 0 output side.
The 2* input may be of decimal value 2, 4, 6, 8 as long as illegal combinations are inhibited before connections to the inputs, and the 4-2-1 part of the code is in binary.
The propagation delay through the decoder is typically 55 nsec in the binary-to-octal mode, and 75 nsec in the BCD-to-decimal mode. The maximum delay in the BCD-to-decimal mode is 120 nsec, frequency-limiting this module to 8HMz when used in this fashion. The enable inputs can be used to strobe output data providing inputs 2° — 2* have settled at least 50 nsec prior to the input pulse.



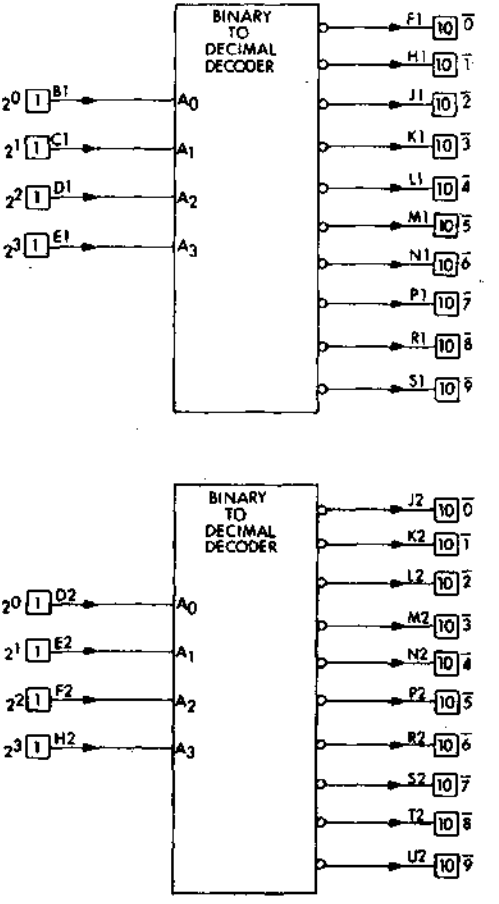
5-BIT BINARY/OCTAL DECODER

M163
DUAL BINARY-TO-DECIMAL DECODER

NUMERIC

M SERIES

Length: Standard
Width: Single
Height: Single



Volts	Power mA (max.)	Pins
+5V	44	A2
GND		C2, T1

The M163 Module consists of two binary-to-decimal decoder circuits, each of which accepts four inputs and provides 10 mutually exclusive outputs. The most significant 2^3 input can be used as an inhibit function to allow the circuits to be used as a binary-to-octal decoder.

APPLICATIONS
1-of-10 decoder or 1-of-8 decoder with selected output Low.

FUNCTION
Each of the decoder circuits on the M163 Module accepts four active High BCD inputs and provides 10 mutually exclusive active Low outputs. All outputs are High when binary codes greater than 9 are applied to the inputs. Refer to the truth table for input/output level sequences.

TRUTH TABLE (EACH SECTION)

A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	L	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

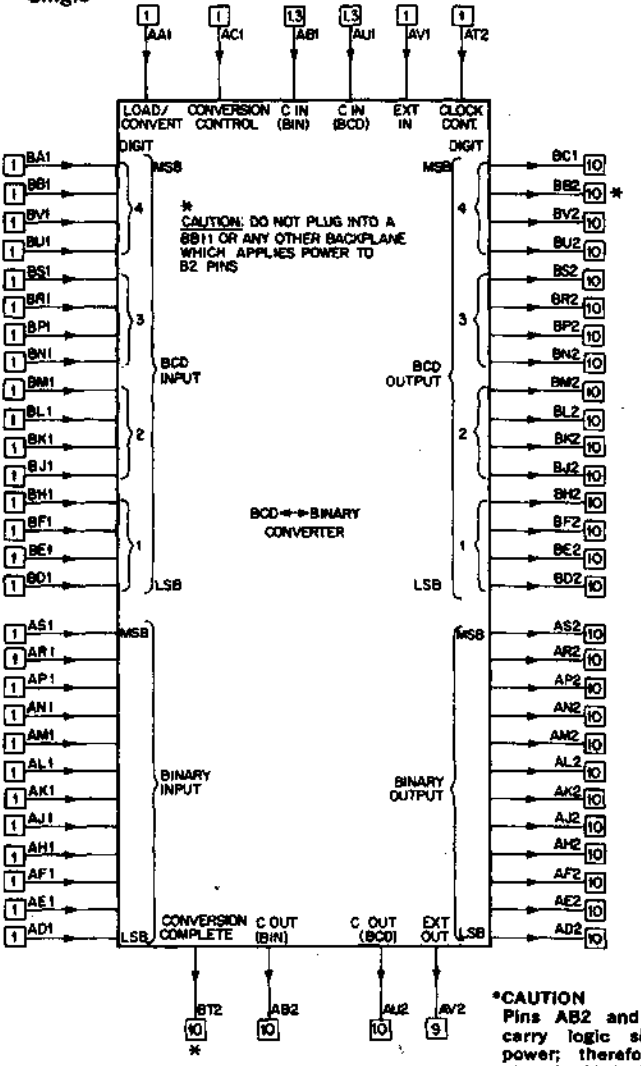
H = HIGH Voltage Level
L = LOW Voltage Level

M230
BINARY TO BCD AND BCD TO BINARY CONVERTER

NUMERIC

M SERIES

Length: Standard
Height: Double
Width: Single



Volts	Power mA (max.)	Pins
+5	860	A2
GND		C2, T1

***CAUTION**
Pins AB2 and BB2 both carry logic signals, not power; therefore do not plug the M230 into a BB11 system unit since the corresponding BB11 pins both carry −15V.

The M230 converts a binary number to its binary coded decimal equivalent or a binary coded decimal number to its binary equivalent.

The maximum number that can be converted from either binary to BCD or BCD to binary is 4095 which is 7777_4. This converter utilizes a counting technique where the count frequency is typically 5 MHz. Therefore, the conversion time for the maximum number 7777_4 is typically 0.82 millisec.

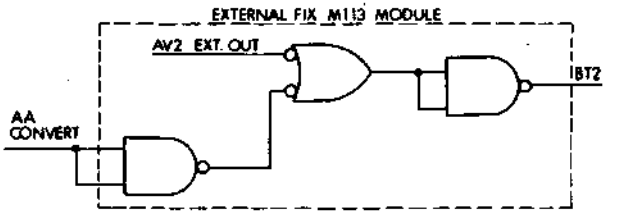
The M230 is fully cascadable. When using more than one M230 the C_{OUT} BIN. must be connected to the C_{IN} BIN. and the C_{OUT} BCD must be connected to the C_{IN} BCD of the next higher significant unit. C_{IN} BIN. and C_{IN} BCD of the least significant unit must be made a logic "1". C_{OUT} BIN. and C_{OUT} BCD of the most significant unit may be left open.

CONVERSION CONTROL on pin AC1 will cause a Binary to BCD conversion when connected to ground and a BCD to Binary conversion when connected to a logic "1" source. When cascading M230's, connect all CONVERSION CONTROL inputs in parallel.

LOAD/CONVERT on pin AA1 reads the input data when connected to a logic "1" level and starts the conversion when this input is returned to a logic "0" level. When cascading M230's, connect all LOAD/CONVERT inputs in parallel.

CONVERSION COMPLETE on pin BT2 goes High when the conversion process is finished.

There is no conversion complete signal when all low inputs are entered. This is because the circuit is designed to return the counters to a low state when load/convert signal goes high which initiates a low at all BCD and Binary inputs and the counters on the input side are always counting down to Zero. If it is likely that a circuit is required to convert Zero, use the following external configuration which utilizes the M113 Module (described elsewhere in this Handbook).



EXT. IN on pin AV1 and EXT. OUT on pin AV2 convey conversion finished information between cascaded M230's. This information travels from the most significant M230 to the least significant M230. Therefore, the EXT. IN of the most significant M230 must be connected to a logic "1" source. Each EXT. OUT is connected to the EXT. IN of the next less significant M230. The EXT. OUT of the least significant M230 is left unconnected.

CLOCK CONTROL on pin AT2 of the least significant M230 should be enabled by connecting it to a logic "1" source. All others should be connected to ground.

The following is an ordered summary for operating a single M230:

1. Make the conversion control (pin AC1) a logic "0" for converting Binary to BCD or a logic "1" for converting BCD to Binary.

2. When converting Binary to BCD, connect the Binary number to the BINARY INPUTS and ground the BCD INPUTS. Conversely, when converting BCD to Binary, connect the BCD number to the BCD INPUTS and ground the BINARY INPUTS.

3. C_{IN} BIN., C_{IN} BCD, EXT. IN, and CLOCK CONTROL inputs should be tied to a source of logic "1". The outputs C_{OUT} BIN., C_{OUT} BCD, and EXT. OUT should be left unconnected.

4. Pulse the LOAD/CONVERT input with a positive pulse of 150 nsec. minimum pulse width. There is no limit on the maximum width of this pulse. Conversion begins on the negative going edge of this pulse.

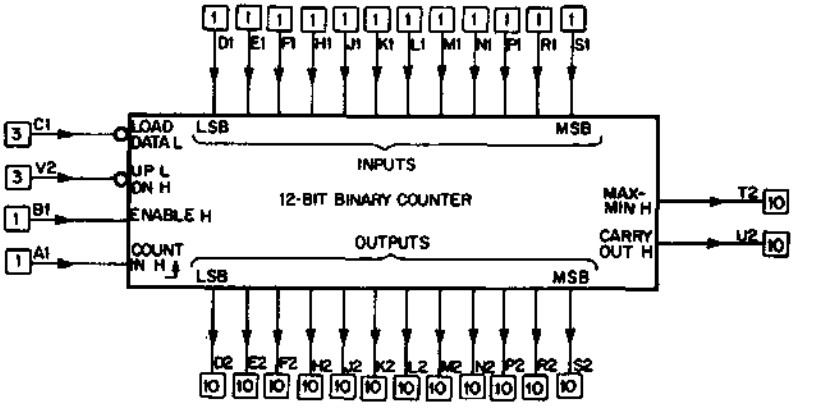
5. When converting Binary to BCD read the BCD OUTPUT for the BCD equivalent. For converting BCD to Binary read the BINARY OUTPUT for the Binary equivalent. The CONVERSION COMPLETE OUTPUT becomes a logic "1" when the conversion is through.

M236
12-BIT BINARY UP/DOWN COUNTER

NUMERIC

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	330	A2
GND		C2, T1

The M236 is a 12-bit synchronous binary up/down counter. It has a single control input that can switch the counting mode from up to down without disturbing the contents of the counter. The M236 is fully cascadable and programmable. Cascading simply involves paralleling the respective ENABLE, LOAD DATA, and UP/DOWN signals while one CARRY-OUT signal drives the COUNT IN input of the next M236.

APPLICATIONS

The programmability of the M236 makes it ideal for use as a modulo-N divider. Modification of the count length is easily done by setting the DATA input lines to N and loading each time the count down reaches zero. When counting down the MAX-MIN output goes HIGH when all twelve bits equal zero.

FUNCTIONS

COUNT IN: Counting occurs on a positive transition of the COUNT IN line. This input must remain LOW for at least 50 ns before the count. Time between pulses can be no less than 50 ns. There is no maximum for pulse width or time between pulses. The maximum count frequency is 10 MHz.

ENABLE: The ENABLE input permits counting while it is HIGH, and disables counting while it is LOW. Critical timing factors that must be observed when changing the enabled state are:

1. To enable counting, the ENABLE line must remain HIGH from 70 ns before to 30 ns after the positive transition of the COUNT IN signal.

2. To disable counting, the ENABLE line must go LOW at least 40 ns before the COUNT IN signal goes LOW, and remain LOW until at least 40 ns after the positive transition of the COUNT IN signal.

LOAD DATA: The outputs assume the same state as their associated data inputs, independent of the count, when LOAD DATA goes LOW for at least 50 ns. Loading data overrides all other input signals and may be done at any time. The maximum propagation delay from the LOAD DATA input to any output is 50 ns. The DATA inputs will have no effect upon the outputs within 15 ns after the LOAD DATA line goes HIGH.

UP/DOWN CONTROL: A logic LOW on this line yields an up count. A logic HIGH on this line yields a down count. This control signal may be changed when the COUNT IN signal is HIGH. It must not be changed while the COUNT IN is LOW or during the 40 ns period before the COUNT IN signal goes LOW.

CARRY OUT: When the counter has reached either the maximum up count state (4095 binary) or the minimum down count state (0000), the CARRY OUT signal follows the COUNT IN signal. The maximum delay time from the COUNT IN transition to the CARRY OUT transition is 60 ns.

MAX-MIN: This provides a logic HIGH output when the counter has reached either the maximum up count state (4095 binary) or the minimum down count state (0000). The maximum delay time for this output measured from the positive going edge of the COUNT IN signal is 120 ns. This signal is also used to accomplish look-ahead for very high speed operations.

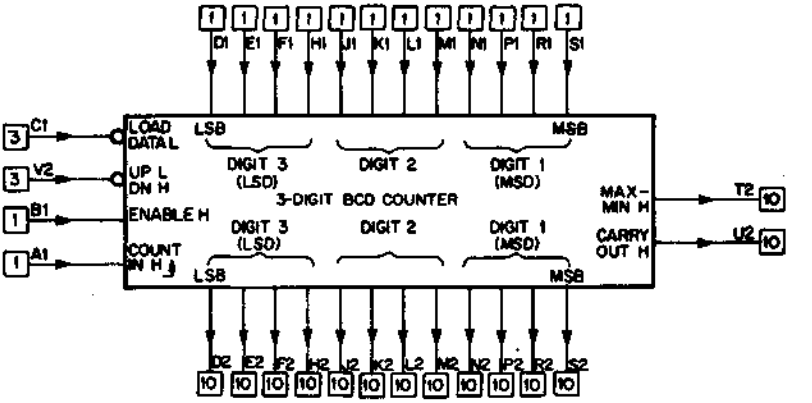
Cascading: When cascading M236's, the CARRY OUT should be connected to the COUNT IN of the next more significant unit. Also, the respective LOAD DATA, UP/DOWN, and ENABLE signals must be paralleled.

M237
3-DIGIT BCD UP/DOWN COUNTER

NUMERIC

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	330	A2
GND		C2, T1

The M237 is a 3-digit synchronous BCD up/down counter. It has a single control input that can switch the counting mode from up to down without disturbing the contents of the counter. The M237 is fully cascadable and programmable. Cascading simply involves paralleling the respective ENABLE, LOAD DATA, and UP/DOWN signals while one MAX/MIN signal drives the ENABLE input of the next M237.

APPLICATIONS

The programmability of the M237 makes it ideal for use as a modulo-N divider. Modification of the count length is easily done by setting the DATA input lines to N and loading each time the count down reaches zero. When counting down the MAX/MIN output goes HIGH when all three digits equal zero.

FUNCTIONS

COUNT IN: Counting occurs on a positive transition of the COUNT IN line. This input must remain LOW for at least 50 ns before the count. Time between pulses can be no less than 50 ns. There is no maximum for pulse width or time between pulses. The maximum count frequency is 10 MHz.

ENABLE: The ENABLE input permits counting while it is HIGH, and disables counting while it is LOW. Critical timing factors that must be observed when changing the enabled state are:

1. To enable counting, the ENABLE line must remain HIGH from 70 ns before to 30 ns after the positive transition of the COUNT IN signal.

2. To disable counting, the ENABLE line must go LOW at least 40 ns before the COUNT IN signal goes LOW, and remain LOW until at least 40 ns after the positive transition of the COUNT IN signal.

LOAD DATA: The outputs assume the same state as their associated data inputs, independent of the count, when LOAD DATA goes LOW for at least 50 ns. Loading data overrides all other input signals and may be done at any time. The maximum propagation delay from the LOAD DATA input to any output is 50 ns. The DATA inputs will have no effect upon the outputs within 15 ns after the LOAD DATA line goes HIGH.

UP/DOWN CONTROL: A logic LOW on this line yields an up count. A logic HIGH on this line yields a down count. This control signal may be changed when the COUNT IN signal is HIGH. It must not be changed while the COUNT IN is LOW or during the 40 ns period before the COUNT IN signal goes LOW.

CARRY OUT: When the counter has reached either the maximum up count state (999) or the minimum down count state (000), the CARRY OUT signal follows the COUNT IN signal. The maximum delay time from the COUNT IN transition to the CARRY OUT transition is 60 ns.

MAX-MIN: This provides a logic HIGH output when the counter has reached either the maximum up count state (999) or the minimum down count state (000). The maximum delay time for this output measured from the positive going edge of the COUNT IN signal is 120 ns. This signal is also used to accomplish look-ahead for very high speed operations.

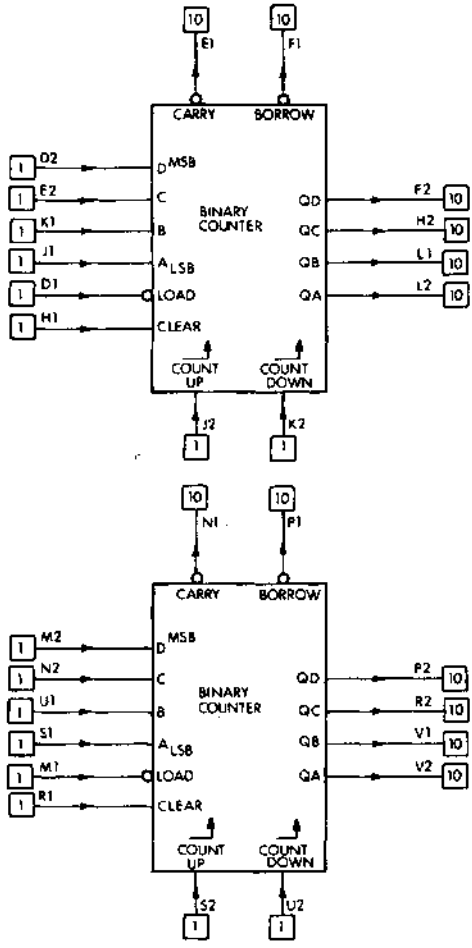
Cascading: When cascading M237's, the CARRY OUT should be connected to the COUNT IN of the next more significant unit. Also, the respective LOAD DATA, UP/DOWN, and ENABLE signals must be paralleled.

M238
DUAL 4-BIT BINARY SYNCHRONOUS UP/DOWN COUNTER

NUMERIC

M SERIES

Length: Standard
Width: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	180	A2
GND		C2, T1

The M238 module consists of two identical 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other.

The outputs are triggered by a LOW to HIGH level transition of either COUNT input. The direction of the counting is determined by which COUNT input is pulsed while the other COUNT input is High.

The counters are fully programmable; that is, the outputs may be preset to any state by entering the desired data at the DATA inputs while the LOAD input is LOW. The output will change to agree with the DATA inputs independently of the COUNT pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A CLEAR input has been provided which forces all outputs to the LOW level when a HIGH level is applied. The CLEAR function is independent of the COUNT and LOAD inputs.

These counters were designed to be cascaded without the need for any external circuitry. The counters can be cascaded by feeding the BORROW and CARRY outputs to the COUNT-DOWN and COUNT-UP iuputs respectively, of the succeeding counter.

CARRY L = (QA H, QB H, QC H, QD H) • (COUNT UP L)
BORROW L = (QA L, QB L, QC L, QD L) • (COUNT DOWN L)

SPECIFICATIONS
Refer to Table 1.

TABLE 1

Parameter	From Input	To Output	Max.
f max	—	—	10 MHz
t set up	—	—	25 ns
tp	Count-up	Carry	50 ns
tp	Count-down	Borrow	50 ns
tp	Either-Count	Q	50 ns
tp	Load	Q	50 ns
tp	Clear	Q	50 ns

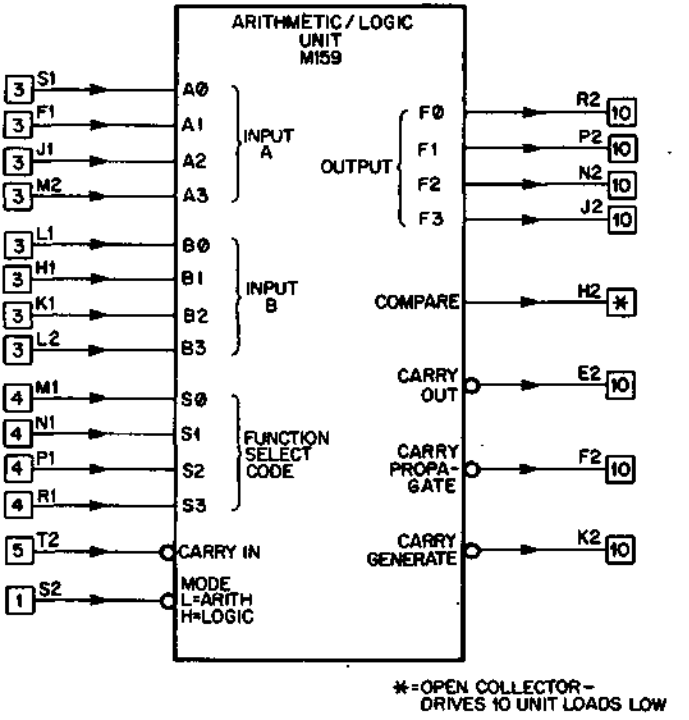
f max = Maximum Clock Freq.
tp = propagation delay time, for either a High-going or Low-going output change.

M159
ARITHMETIC/LOGIC UNIT

NUMERIC

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	150	A2
GND		C2, T1

The M159 can perform 16 word-oriented arithmetic operations and 16 bit oriented logic functions. Arithmetic operations are performed on two 4-bit input words and an input carry to produce one 4-bit output word and a carry out. In the logic mode the M159 looks like four 2-input functional gates. Where N indicates one out of four, the output F_N depends only on the inputs A_N, B_N, and the logic function code selected.

The M159 is fully cascadable. The CARRY OUT of the less significant M159 should be connected directly to the CARRY IN of the next more significant M159. The CARRY PROPAGATE and CARRY GENERATE output should be used with a carry look-ahead module or left unconnected.

The COMPARE output goes High whenever all the "F" outputs go High. This output is open-collector so that it can be wire-AND connected when M159 modules are cascaded. An example of how this output can be used is shown in the table below.

When the arithmetic operation A minus B minus 1 is selected, the M159 can be used as a comparator.

A and B Data Inputs	COMPARE Output	CARRY OUT
$A > B$	0	0
$A = B$	1	1
$A < B$	0	1

The maximum propagation delay from the "A_N" or "B_N" bit input to the output bit "F_N" in the logic mode is 48 nsec. which does not change as M159's are cascaded. In the arithmetic mode, the maximum delay from the "A" or "B" word input to the "F" word output, CARRY OUT, or COMPARE is 50 nsec. which increases by 19 nsec. per additional cascaded M159 when carry look-ahead is not used. When carry look-ahead is used, the maximum additional delay is limited to 20 nsec. for up to three additional M159's.

Table of Logic Mode Operations

(MODE Input = 1)

(CARRY IN has no affect on Logic Mode Operations)

Function SELECTION CODE				NOTE that F_N is complemented when the Function Selection Code is complemented		Complemented Function SELECTION CODE			
S3	S2	S1	S0	Bit F_N Equals	Bit F_N Equals	S3	S2	S1	S0
0	0	0	0	$\overline{A}_N$	A_N	1	1	1	1
0	0	0	1	$\overline{A}_N$ AND $\overline{B}_N$	A_N OR B_N	1	1	1	0
0	0	1	0	$\overline{A}_N$ AND B_N	A_N OR $\overline{B}_N$	1	1	0	1
0	0	1	1	0	1	1	1	0	0
0	1	0	0	$\overline{A}_N$ OR $\overline{B}_N$	A_N AND B_N	1	0	1	1
0	1	0	1	$\overline{B}_N$	B_N	1	0	1	0
0	1	1	0	(A_N AND $\overline{B}_N$) OR ($\overline{A}_N$ AND B_N)	(A_N AND B_N) OR ($\overline{A}_N$ AND $\overline{B}_N$)	1	0	0	1
0	1	1	1	A_N AND $\overline{B}_N$	$\overline{A}_N$ OR B_N	1	0	0	0

Table of Arithmetic Mode Operations

(MODE Input = 0)

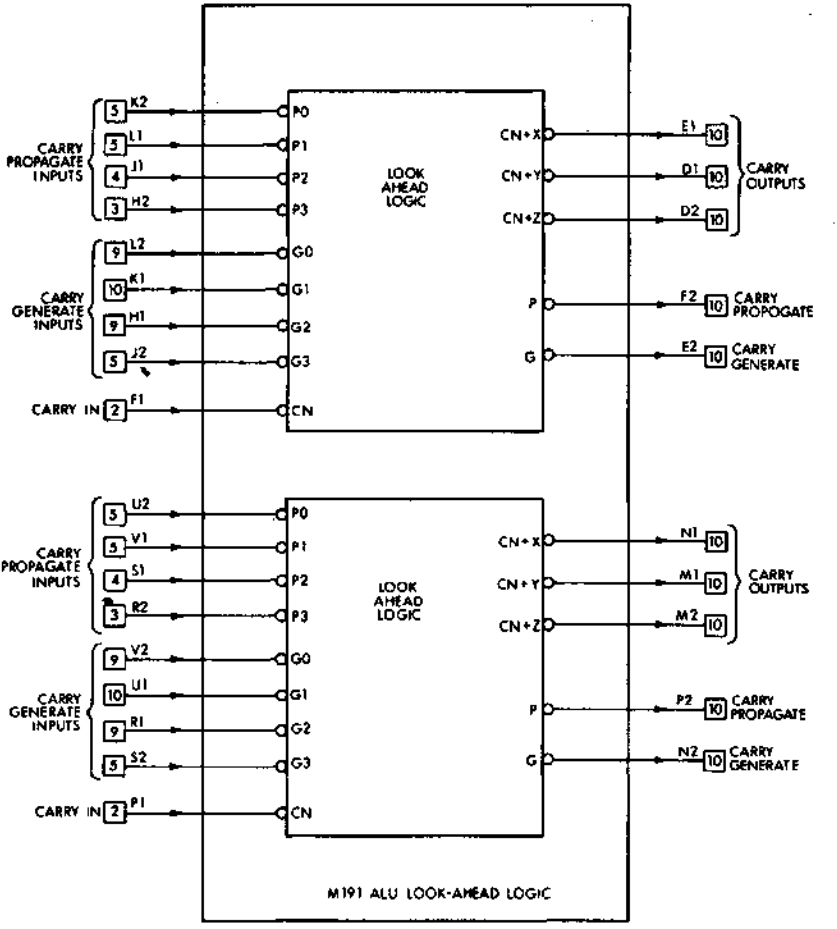
Function				Word F Equals	
SELECTION CODE				CARRY IN = 1	CARRY IN = 0
S3	S2	S1	S0		
0	0	0	0	WORD A	WORD A plus 1
0	0	0	1	A OR B	A OR B plus 1
0	0	1	0	A OR $\overline{B}$	A OR $\overline{B}$ plus 1
0	0	1	1	Minus 1 (2's Comp.)	ZERO
0	1	0	0	A plus (A AND $\overline{B}$)	A plus (A AND $\overline{B}$) plus 1
0	1	0	1	(A OR B) plus (A AND $\overline{B}$)	(A OR B) plus (A AND $\overline{B}$) plus 1
0	1	1	0	A Minus B Minus 1	A Minus B
0	1	1	1	(A AND $\overline{B}$) minus 1	A AND $\overline{B}$
1	0	0	0	A plus (A AND B)	A plus (A AND B) plus 1
1	0	0	1	A plus B	A plus B plus 1
1	0	1	0	(A OR $\overline{B}$) plus (A AND B)	(A OR $\overline{B}$) plus (A AND B) plus 1
1	0	1	1	(A AND B) minus 1	A AND B
1	1	0	0	A Times 2	A Times 2 plus 1
1	1	0	1	(A OR B) plus A	(A OR B) plus A plus 1
1	1	1	0	(A OR $\overline{B}$) plus A	(A OR $\overline{B}$) plus A plus 1
1	1	1	1	A minus 1	A

M191
ALU LOOK-AHEAD LOGIC

NUMERIC

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	130	A2
GND		C2, T1

The M191 contains two high-speed look-ahead units to be used to reduce the propagation delay of cascaded M159 Arithmetic Logic Units for Arithmetic Mode operations. The propagation delay is the maximum delay time from "A" to "B" word input to the "F" word output or COMPARE output. This time is 50 ns for one ALU and increases by 19 ns for each additional cascaded ALU without use of the M191. This increase is due to the 19-ns delay from 'A" or "B" word input to the first CARRY OUT and the added 19-ns delays to each succeeding CARRY OUT. However, when a look-ahead CARRY OUTPUT is substituted for an ALU CARRY OUTPUT, this time increase is only 7 ns per additional ALU. These advanced look-ahead CARRY OUTPUTS are determined by the states of the CARRY GENERATE, CARRY PROPAGATE and CARRY IN inputs.

APPLICATIONS

Figures 1 and 2 illustrate use of the module for up to 16-bit and 32-bit applications respectively.

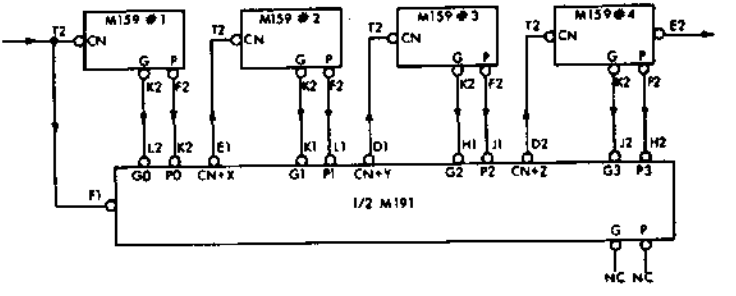


Figure 1. 16-Bit Application of M191 with M159.

NOTES:

1. Propagation Delay Time = 50 ns + 7 ns + 7 ns + 7 ns = 71 ns
2. CN+4 of most significant M159 (#4) becomes final CARRY OUT
3. For 12-bit application, M159 #4 not used; for 8-bit application, M159 #3 and #4 not used.

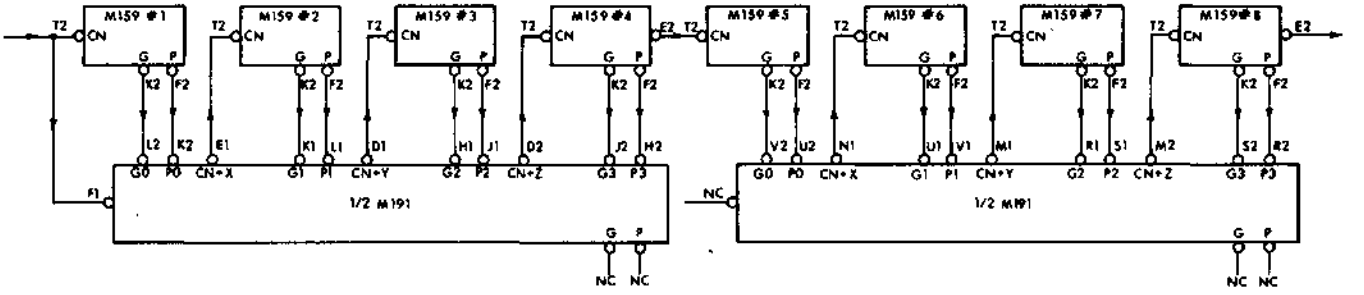


Figure 2. 32-Bit Application of M191 with M159.

NOTES:

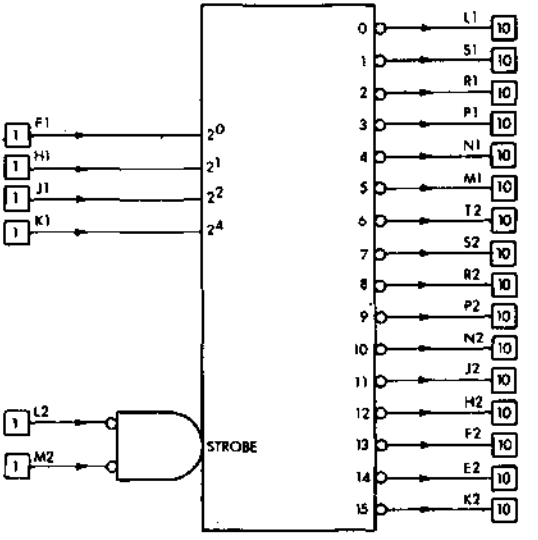
1. Propagation Delay Time = 50 ns + 7 ns + 7 ns + 7 ns + 19 ns + 7 ns + 7 ns + 7 ns = 110 ns
2. CN+4 of most significant M159 (#8) becomes final CARRY OUT
3. For 28-bit application, M159 #8 not used; for 24-bit application, M159 #8 and #7 not used, etc.

M155
4-LINE TO 16-LINE DECODER

NUMERIC

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	55	A2
GND		C2, T1

The M155 module decodes four binary-coded inputs into one of sixteen mutually exclusive outputs when both STROBE inputs, L2 and M2, are Low. The demultiplexing function is performed by using the four input lines to address the output line, passing data from one of the STROBE inputs with the other STROBE input LOW. When either STROBE input is HIGH, all outputs are HIGH. Refer to the Truth Table.

SPECIFICATIONS
Propagation Delay

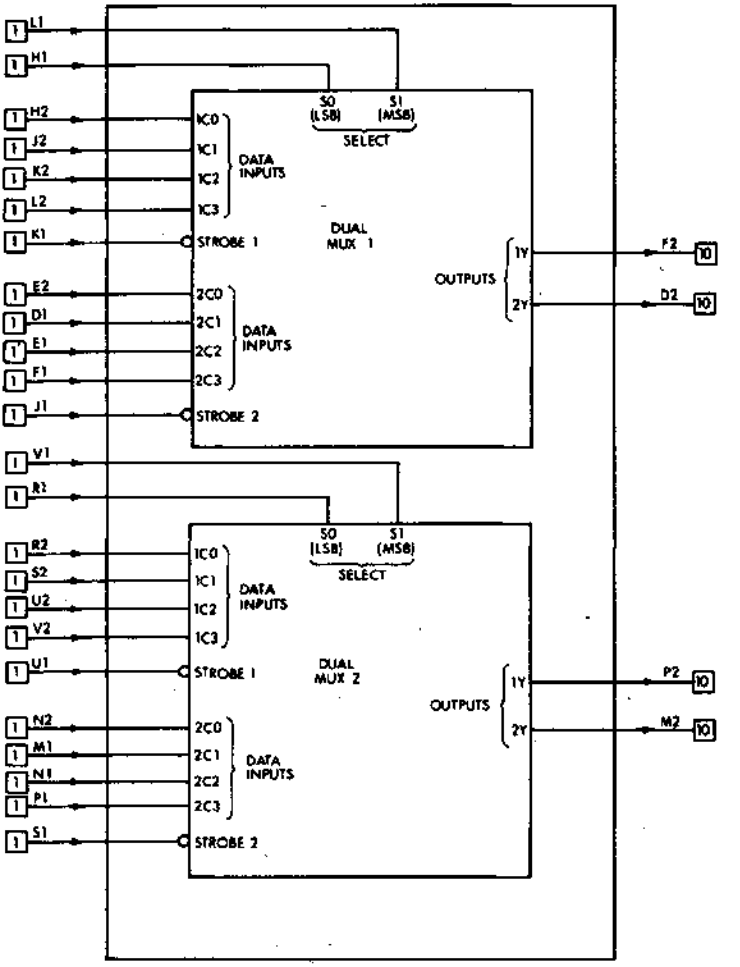
From:	To:
Data Inputs	HIGH or LOW Output = 36 ns (max)
Either STROBE Input	HIGH or LOW Output = 30 ns (max)

M1701
DATA SELECTOR

NUMERIC

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	110	A2
GND		C2, T1

The M1701 Data Selector contains two independent dual 4-line to 2-line multiplexers on a single-height module. Each dual multiplexer has two groups of DATA INPUTS, two STROBES, two OUTPUTS and common SELECT inputs. An OUTPUT becomes active for a DATA INPUT when the DATA INPUT is addressed by the SELECT lines and the corresponding STROBE brought LOW.

APPLICATIONS

- Multiplexing for parallel-to-serial conversion
- Timesharing
- Sampling

TRUTH TABLE

FUNCTIONS

SELECT		DATA INPUTS					
S1	S0	C3	C2	C1	C0	STROBE	OUTPUT Y
X	X	X	X	X	X	H	L
L	L	X	X	X	L	L	L
L	L	X	X	X	H	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
H	H	L	X	X	X	L	L
H	H	H	X	X	X	L	H

X = irrelevant

PROPAGATION DELAY TIMES

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	MAX	UNIT
t_{PLH}	Data	Y	25	ns
t_{PHL}	Data	Y	30	ns
t_{PLH}	Address	Y	40	ns
t_{PHL}	Address	Y	40	ns
t_{PLH}	Strobe	Y	35	ns
t_{PHL}	Strobe	Y	30	ns

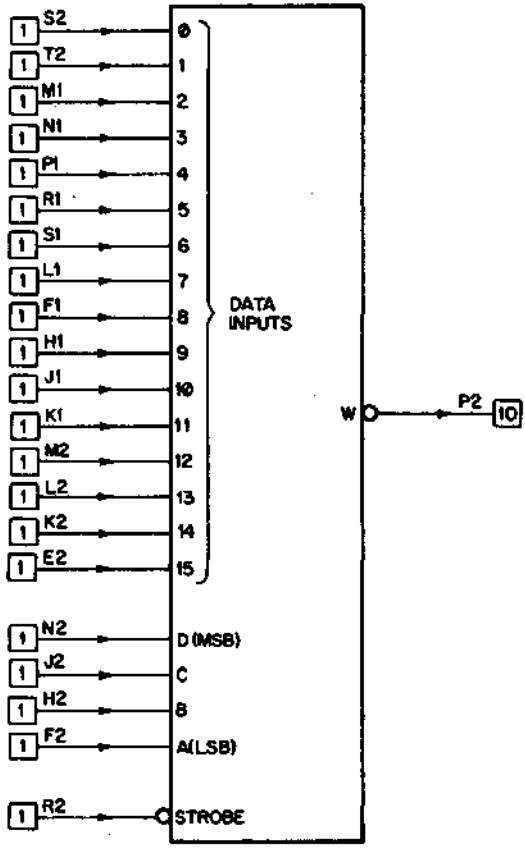
¶t_{PLH} = propagation delay time, Low-to-High-level output.
t_{PHL} = propagation delay time, High-to-Low-level output.

M1713
16-LINE TO 1-LINE
DATA SELECTOR

NUMERIC

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	70	A2
GND		C2, T1

The M1713 module is a 1-of-16 data selector/multiplexer. The binary code on inputs A-D defines which of the 16 data inputs will be connected to the output when STROBE is Low. Its operation is described by the following **TRUTH TABLE:**

INPUTS																		OUTPUT
D	C	B	A	STROBE	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	H
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	L
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	H
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	L
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	H
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	L
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	H
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	L
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	H
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	L
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	H
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	L
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	H
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	L
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	H
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	L
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	H
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	L
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	H
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	L
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	H
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	L
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	H
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	L
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	H
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	L
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	H
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	L

When used to indicate an input condition, X = High or Low

SPECIFICATIONS

Propagation Delay

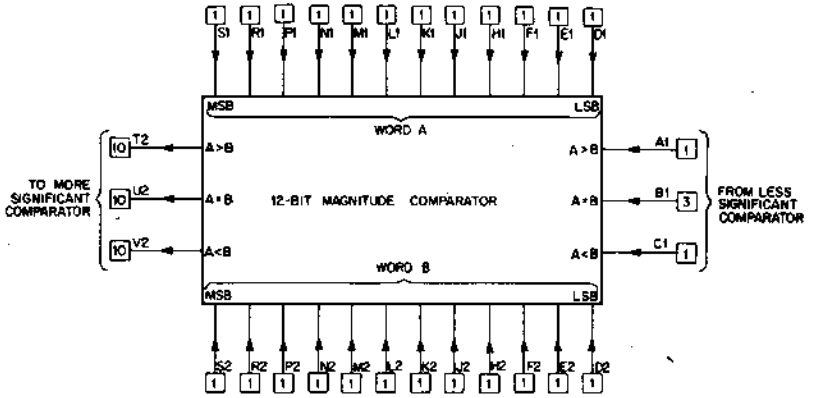
FROM:	TO:
Input A, B, C, D	Output W = 50 ns (max)
STROBE	Output W = 40 ns (max)
D0 through D15	Output W = 30 ns (max)

M168
12-BIT MAGNITUDE COMPARATOR

NUMERIC

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	250	A2
GND		C2, T1

The M168 12-Bit Magnitude Comparator performs magnitude comparison of two 12-bit words. When the comparison inputs are not connected to the comparison outputs of another M168, the "A=B" input must be connected to a logical "1". The A>B and A<B inputs may individually be made a logic "1" or logic "0". However, connecting both these inputs to GND, a logic "0" is recommended.

The M168 Comparator may be cascaded to compare longer words. The outputs T2, U2, and V2 should be connected to the corresponding inputs of the next comparator which are A1, B1, and C1 respectively. The inputs of the first comparator must all be made a logical "1".

The propagation delay time from Data (A and B) to outputs is 48 nsec typical and 72 nsec maximum for one unit.

When cascading the total typical time is 48 nsec plus 36 nsec per additional unit. The total maximum time is 72 nsec plus 54 nsec per additional unit.

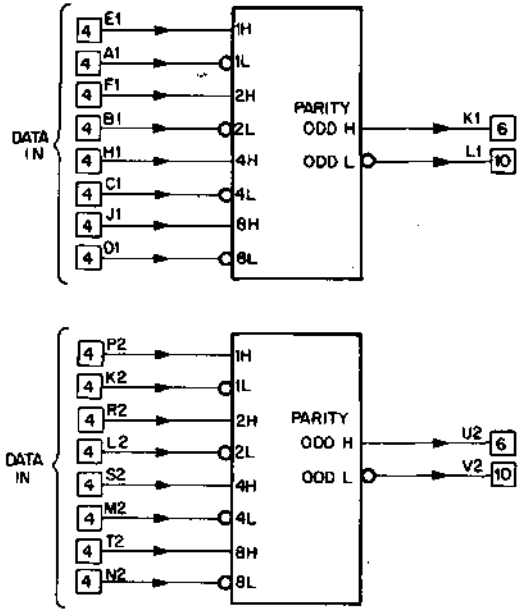
INPUTS				OUTPUTS		
A > B	A = B	A < B	Data	A > B	A = B	A < B
1	0	0	A > B	1	0	0
1	0	0	A = B	1	0	0
1	0	0	A < B	0	0	1
1 or 0	1	1 or 0	A > B	1	0	0
1 or 0	1	1 or 0	A = B	0	1	0
1 or 0	1	1 or 0	A < B	0	0	1
0	0	1	A > B	1	0	0
0	0	1	A = B	0	0	1
0	0	1	A < B	0	0	1

M162
PARITY CIRCUIT

NUMERIC

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	102	A2
GND		C2, T1

The M162 contains two parity detector circuits. Each circuit indicates whether the binary data presented to it contains an ODD or EVEN number of ONES. The data and its complement are required as shown.

APPLICATIONS

- Parity checking

FUNCTIONS

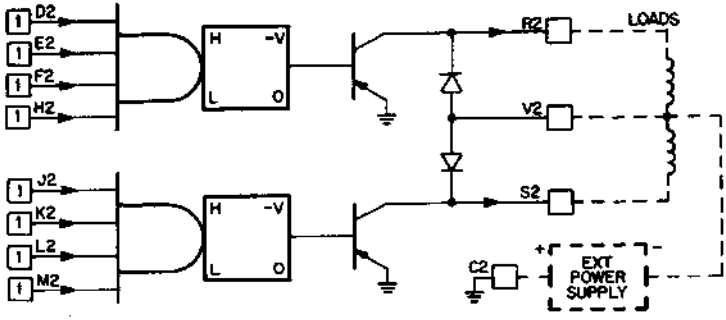
Indication of ODD PARITY is given by a HIGH level at pins K1 and U2 respectively. Pins L1 and V2, when HIGH, indicate EVEN PARITY or no input.

M040
SOLENOID DRIVER

LOGIC AMPLIFIERS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	47	A2
GND		C2, T1
−15	9	B2

The M040 contains two identical negative high-voltage driver circuits. Each consists of a 4-input positive NAND gate that controls a PNP transistor switch. The switch is capable of sinking up to 600 mA of current to ground from an external power supply of up to −70 volts. One terminal of the load device (relay, etc.) must be connected to the external voltage, the other to the drive output. The positive terminal of the external supply connects to the module ground.

APPLICATIONS

The M040 can drive relays, solenoids, stepping motor windings and similar inductive loads.

Restrictions: Not recommended for indicator drive.

FUNCTIONS

ON Condition: Each driver sinks current from the external circuit when all four control inputs are HIGH. The amount of current is determined by the external voltage and load impedance. (The internal switch is a saturated PNP transistor.) Typical output voltage when sinking 0.6 A is −2 volts.

OFF Condition: When one or more control inputs is LOW, the internal switch is a high impedance and the output voltage approaches the external voltage source. The output circuit draws a small amount of leakage current (typically 100 μA for a 70-volt external supply).

Anti-Kickback: Pin V2 of the driver module must be connected to the external supply so that the drivers will be protected from the back voltage generated by inductive loads. If the wire to the power supply is more than three feet long, it may have to be bypassed at the module with an electrolytic capacitor to reduce the pulse overshoot caused by the inductance of the wire.

Improving Recovery Time: If pin V2 is connected to the supply through a resistor, the recovery time of inductive loads can be decreased at a sacrifice in maximum drive voltage capability. Maximum rated supply voltage less actual supply voltage should be divided by load current to find the maximum safe resistance. When both circuits on a module are used, the load current for the above calculation is the sum of the currents.

PRECAUTIONS

Grounding: High current loads should be grounded directly at pin C2 of the M040, rather than at a frame or bus ground.

Parallel Operation: No more than two circuits should be paralleled to drive loads beyond the current capabilities of single circuits.

SPECIFICATIONS

Current sinking capability: 600 mA per circuit, max.

External supply voltage: 70 V dc max.

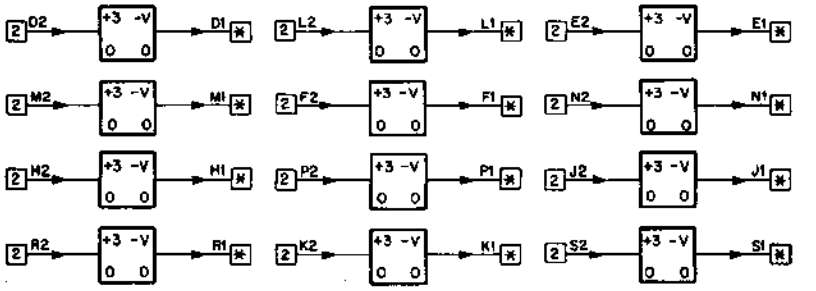
Circuit Delay: Typical propagation delay for each circuit is 5 μs (between 10% and 90% voltage points) for an external supply voltage of 70 volts.

M050
50 MA INDICATOR DRIVER

LOGIC AMPLIFIERS

M SERIES

Length: Standard
Height: Single
Width: Single



* = 50 MA, -30V MAX.

Volts	Power mA (max.)	Pin
+5	47	A2
GND		C2
−15	16	B2

The M050 contains twelve transistor inverters that can drive miniature incandescent bulbs such as those on an indicator panel.

APPLICATIONS
The M050 is used to provide drive current for a remote indicator, such as Drake 11-504, Dialco 39-28-375, or Digital Indicator type 4908, or as a level converter to drive 4917 and 4918 indicator boards.

Restrictions: Do not use to drive inductive loads (relays, solenoids).
Note: For those applications requiring the sinking of current, refer to K Series.

FUNCTIONS
A LOW level on the input of the driver causes current to flow in the output.

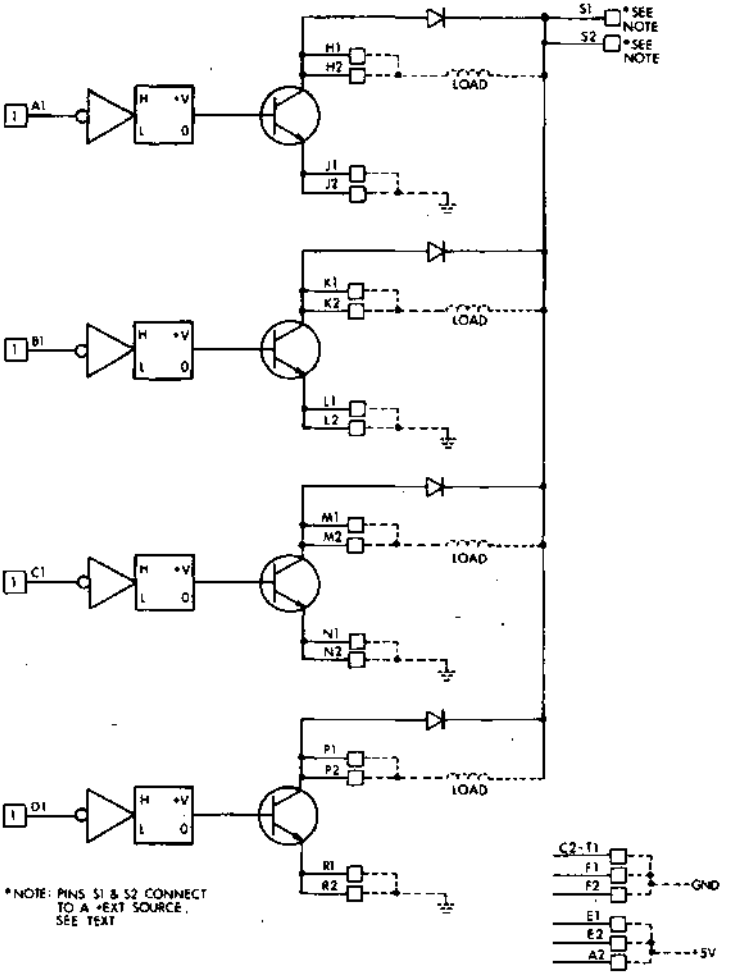
SPECIFICATIONS
Each output is able to drive 50 mA into an external load connected to any voltage between ground and −30 volts.

M060
SOLENOID DRIVER

LOGIC AMPLIFIERS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	80	A2, E1, E2,
GND		C2, T1, F1, F2,
Text	See Text	S1, S2

The M060 module consists of four identical positive high-current driver circuits. Each circuit contains an inverting gate that controls an NPN transistor switch. A low level, at any input, will turn on the switch which is capable of driving loads up to 1.2 amps to ground with external power supply voltages of up to +75 V dc.

APPLICATIONS
The M060 module can be used to drive relays, solenoids, and any similar inductive loads requiring current of up to 1.2 amps.

It is not recommended for lamp-driving tasks; for this application, the M050 module should be utilized.

EXTERNAL POWER SUPPLY
An external power supply must be used to power the loads. This supply may be a maximum of 75 V dc. In connecting the power supply, the positive terminal should be connected to pins S1 and S2, and the negative terminal to ground.

One side of the load device must connect to the external supply and the other side to the driver output.

FUNCTIONS
ON Condition: Each switch activates the load device when the circuit is a logic Low, 0. In this condition, the circuit supplies current which is determined by the external power supply voltage and the load impedance must not exceed 1.2 amps.

OFF Condition: When the input is high, the switch is open and a high impedance exists. In this condition, there is a small amount of leakage current flow which is typically less than 100 μA for an external supply voltage of 75 V dc.

CONNECTIONS and PRECAUTIONS
Note that the emitter and collector on each transistor switch, and the external power supply inputs, each have two pin connections. These dual connections are required because of the high current capability of the circuit. In each case, the pins should be tied together as shown by the dotted lines on the diagram. It should also be mentioned that the emitter connections of each transistor switch must tie to ground, preferably at pin C2 of the logic block.

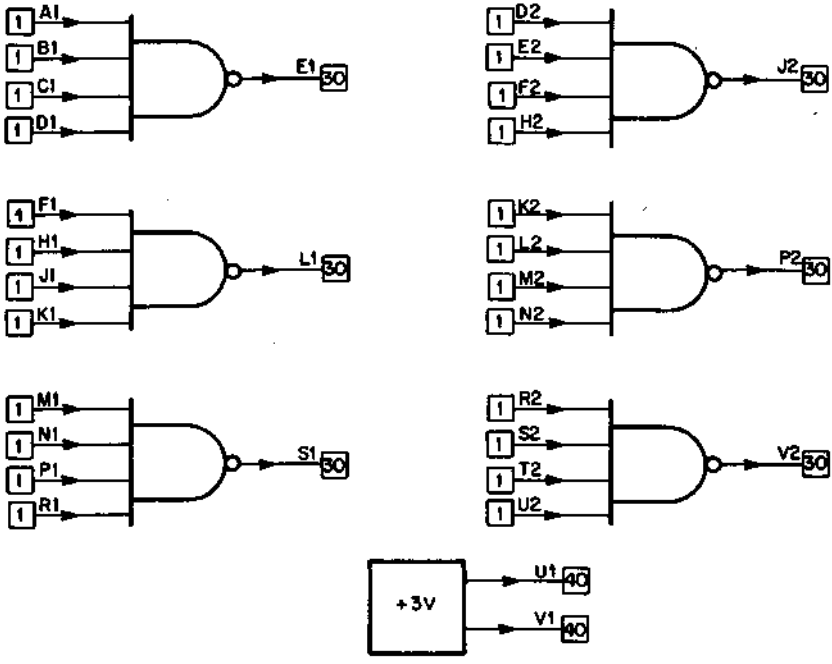
SPECIFICATIONS
Current Capability: 1.2 amps per circuit (max)
External Supply Voltage: 75 V dc (max)
Circuit Delay: 10 μs (typical)—15 μs (max)

M617
FOUR-INPUT POWER NAND GATE

LOGIC AMPLIFIERS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	97	A2
GND		C2, T1

The M617 contains 6 four-input NAND gates each capable of driving up to 30 unit loads.

FUNCTIONS
Physical configuration and logical operation are identical to the M117.

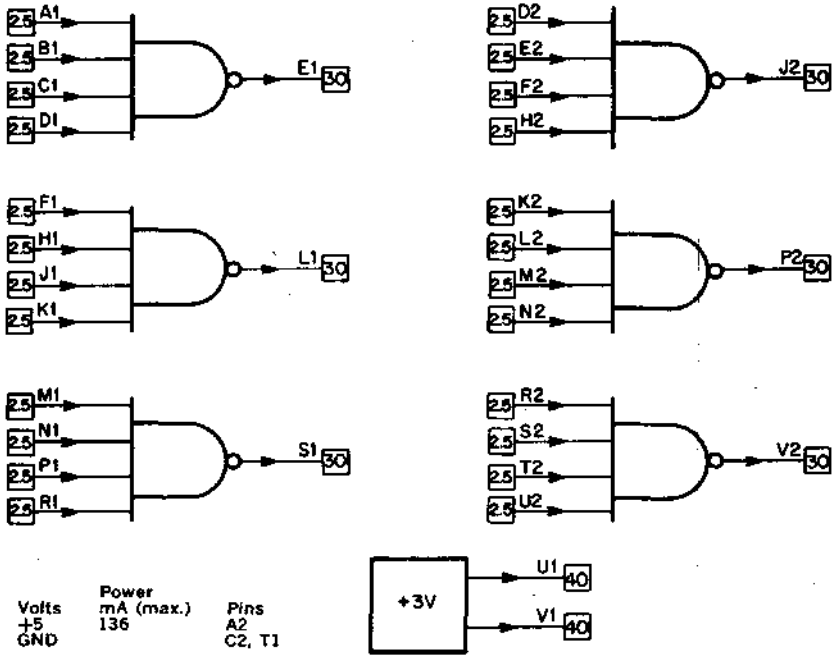
SPECIFICATIONS
Typical gate propagation delay is 15 ns.

M627
NAND POWER AMPLIFIER

LOGIC AMPLIFIERS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	136	A2
GND		C2, T1

The M627 provides six 4-input NAND gates that combine power amplification with high-speed gating.

APPLICATIONS

For high fan-out of clock or shift pulses to expanded counters and shift registers.

PRECAUTIONS

1. In pulse amplifier applications, unused inputs should be connected to the +3 volt pins provided.
2. To utilize the timing accuracy of this module, wire runs of minimum length are recommended.

SPECIFICATIONS

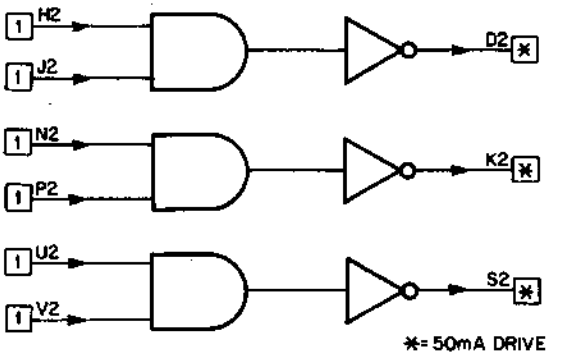
Propagation Time: Typically 6 ns between input and output transitions.

M660
POSITIVE LEVEL CABLE DRIVER

LOGIC AMPLIFIERS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	71	A2
GND		C2

The M660 Cable Driver consists of three NAND gate circuits each of which will drive a 100-ohm terminated cable with M Series levels or pulses of duration greater than 100 ns. The output is not open-collector.

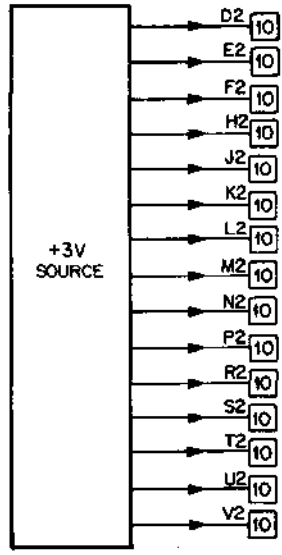
SPECIFICATIONS
Outputs: Can sink 50 mA at a logic LOW, and can source 50 mA at a logic HIGH.

M002
LOGIC HIGH SOURCE

MISCELLA-NEOUS

M SERIES

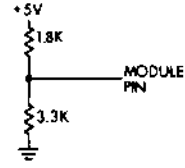
Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	16	A2
GND		C2, T1

To hold unused M Series TTL gate inputs HIGH, the M002 provides 15 outputs at +3 volts (logic HIGH) on pins D2 through V2. Up to 10 unused M Series gate inputs may be connected to any one output. If an M002 circuit is driven by a gate, it appears as two TTL unit loads or 3.2 mA at ground.

The M002 can also be used as pull-ups for open-collector outputs in a wired-OR situation. The following diagram shows one of the 15 identical circuits.

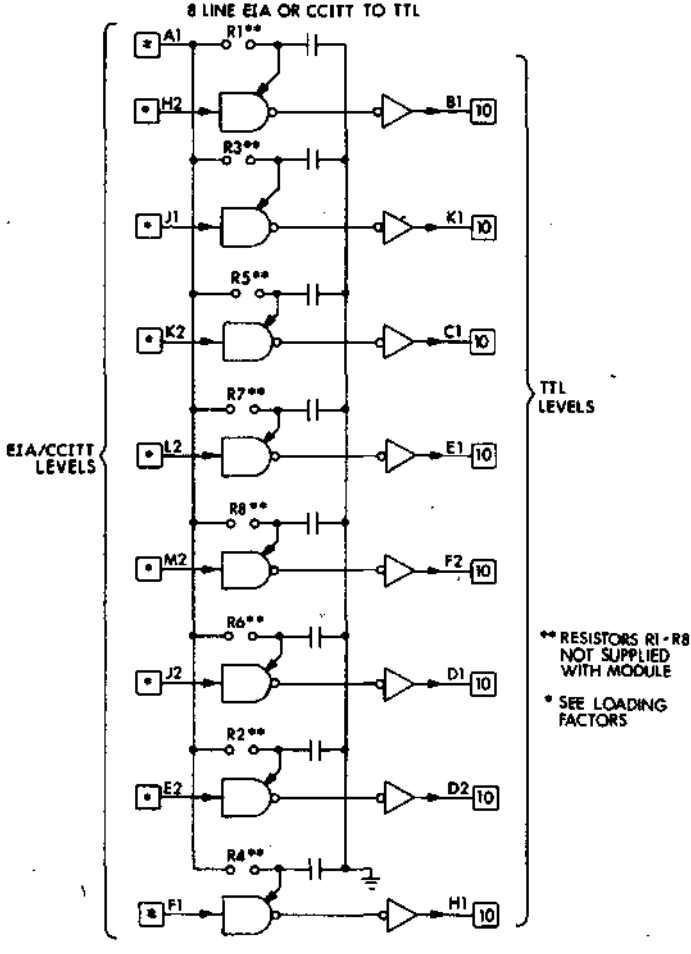


M594
EIA/CCITT LEVEL CONVERTER

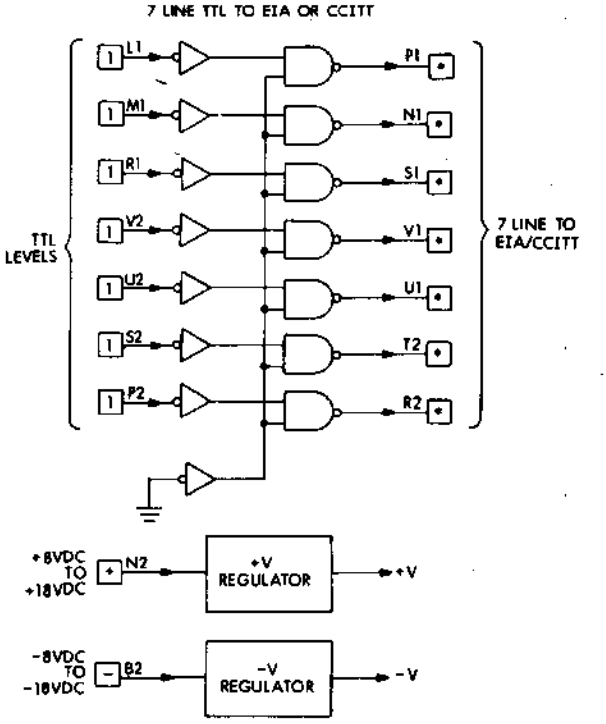
MISCELLANEOUS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5V	125	A2
GND		C2, T1
+15V	25	
−15V	25	



The M594 Module is used to convert the signal voltage levels between DIGITAL data processing terminal equipment such as the DF11 Modem and data communications equipment such as a Bell data set. The M594 provides circuits to convert a maximum of eight EIA or CCITT signal levels to eight DTL or TTL signals that are compatible with DIGITAL logic, and circuits to convert a maximum of seven DIGITAL, TTL, or DTL logic signal outputs to seven signals compatible with EIA or CCITT signal devices. Refer to EIA Standard RS-232-C for description of the selected signals.

FUNCTION

The eight-line EIA or CCITT to TTL converter receives input signals which can vary between +30 Vdc and −30 Vdc. Each input operates on a hysteresis curve or double threshold to prevent noise triggering. The threshold level is determined by the external bias voltage applied to pin A1 of the module and by the value of resistors R1 through R8. A LOW (mark) EIA/CCITT input voltage produces a LOW (0) TTL compatible level output and a HIGH (space) input level results in a HIGH (1) TTL compatible level output.

The seven-line TTL to EIA or CCITT circuits contain inverters and line drivers and can provide output signals which vary between a maximum of +10 Vdc and −10 Vdc from standard DTL or TTL logic inputs. Power to the line drivers is from two voltage regulator circuits contained on the M594. The positive external voltage supplied to the regulators can be any value between +8 Vdc

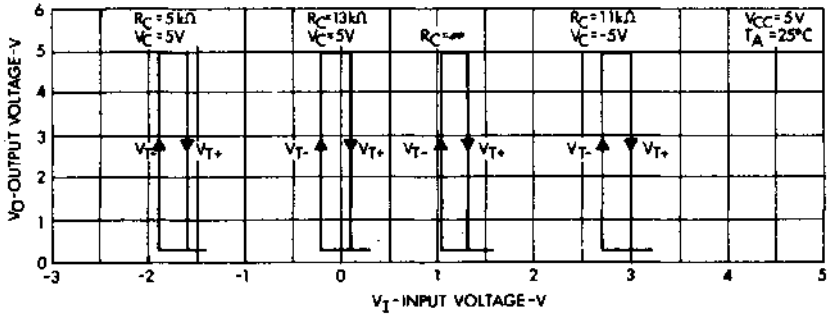
and +18 Vdc, and minus external voltage can be any value between −8 Vdc and −18 Vdc. A LOW (0) TTL compatible level input produces a LOW (mark) EIA/CCITT −10 Vdc level output and a HIGH (1) TTL compatible level input produces a HIGH (space) EIA/CCITT +10 Vdc output.

APPLICATIONS

Convert EIA or CCITT levels from Bell or Western Union Modems to TTL or DTL levels for data communications equipment.

Convert TTL or DTL compatible levels to Bell or Western Union modem signals.

Refer to the following curve for determining the value of resistors R1 through R8 which vary the input voltage threshold of the 8-line EIA/CCITT to DTL level converter. The input voltage threshold, without resistors R1 through R8 recounted, is ±1.0 V. With a V_{CC} of −15 V on pin A1 and a resistor value of 33K ohms in R1 through R8, the input voltage threshold is approx. ±2.5 V..



V_C applied to pin A1

LOADING FACTORS

EIA to TTL (Pins H2, J1, K2, L2, M2, J2, E2, F1)

Input Voltage (V_I)	High Level Input Current (I_{IH})
+25 V	8.3 mA (max.)
+3 V	0.43 mA (min.)
	Low Level Input Current (I_{IL})
−25 V	−8.3 mA (max.)
−3 V	−0.43 mA (min.)

TTL to EIA (Pins P1, N1, S1, V1, U1, T2, R2)
(Low level input voltage V_{IL} = 0.8V, Load Resistor R_L = 3KΩ)

V_{CC}+	V_{CC}−	High level output voltage V_{OH}
+9 V	−9 V	6 V (min.)
+13.2 V	−13.2 V	9 V (min.)

(High level input voltage V_{HL} = 1.9 V, Load Resistor 3KΩ

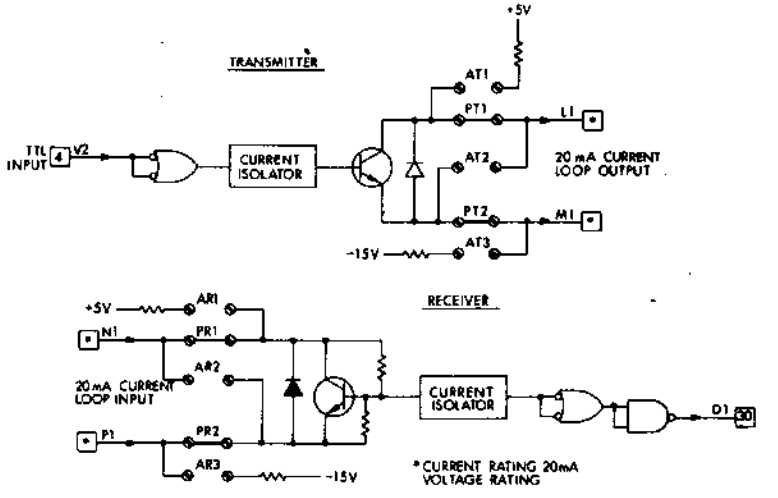
V_{CC}+	V_{CC}−	Low level output voltage V_{OL}
+9 V	−9 V	−6 V (max.)
+13.2 V	−13.2 V	−9 V (max.)

M598
1-CHANNEL TRANSMIT/RECEIVE OPTIC-COUPLED CURRENT ISOLATOR

MISCELLANEOUS

M SERIES

Length: Extended
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5V	100	A2
GND	60	C2, T1
−15V	40	B2

The M598 module contains a single-channel transmit and a single-channel receive circuit capable of converting the data signals between a Teletype ® or similar current loop device and TTL or DTL compatible logic circuits. The data signals transferred through each of the module circuits are optically-coupled to provide a maximum of 1500 V isolation between the current loop and the TTL logic. The transmitter receives serial TTL or DTL compatible levels and controls an output current loop with a maximum current of up to 80 mA.

The receiver circuit responds to input currents of a maximum of 80 mA from a Teletype or similar current loop device and provides serial TTL or DTL compatible signals at the output.

The M598 module is supplied with jumper leads installed to operate as a passive element providing no current to the current loop device. By rewiring the jumper leads on the transmitter and receiver circuits, the module can be an active element and supply current from a +5 Vdc or −15 Vdc source.

APPLICATIONS

Provides up to 1500 V isolation in the data and control lines between TTL or DTL compatible logic and a current loop device such as a TTY. As an active element the M598 performs signal level conversion without isolation.

FUNCTION

A High level at input pin V2 of the transmitter opens the transistor in the output current loop. A Low level causes the transistor to conduct. No current flow at the input of the receive circuit results in a High level at output pin D1 and current flow at the input results in a Low level at pin D1.

SPECIFICATIONS

Signals: The characteristics of the input and output levels and the current and voltage limits of the current loop are listed as follows. The maximum transfer rate of the transmitter or receiver is 4.8 K baud.

PIN	NAME	CHARACTERISTICS		
D1	Received Data, TTL levels	High output level = space = no current flowing in current loop.		
V2	Transmitted Data TTL Levels	High input level = space = no current flowing in current loop.		
			Min	Max
L1	Transmitted Data Most positive	Open circuit voltage	5.0 volts	80 V
		Transmitter voltage drop (marking)	0.5 volts	2.0 V
M1	Transmitted data, Most negative	Marking current	20 mA	80 mA
		Spacing current	0.5 mA	2.0 mA
			Min	Max
N1	Received Data, Most positive	Receiver voltage drop	—	2.5 volts
P1	Received Data Most negative	Marking current	15 mA	80 mA
		Spacing current	—	5.0 mA

Connect the jumpers as indicated on the following table.

CONNECT JUMPERS

	Active**	Passive*
Transmitter	AT1, AT2, AT3	PT1, PT2
Receiver	AR1, AR2, AR3	PR1, PR2

* Jumpers inserted during manufacturing

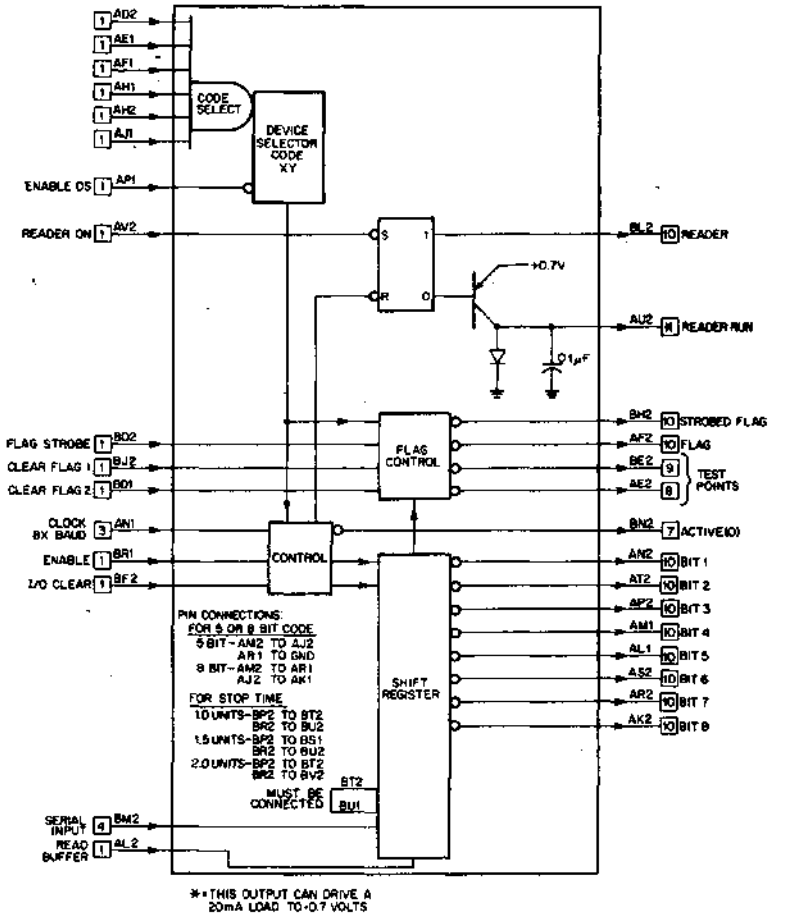
** Requires −15 V in this configuration

M706
TELETYPE RECEIVER

MISCELLA-NEOUS

M SERIES

Length: Standard
Height: Double
Width: Single



*THIS OUTPUT CAN DRIVE A 20mA LOAD TO 0.7 VOLTS

Volts	Power mA (max.)	Pins
+5	400	AA2, BA2
GND		AC2, AT1, BC2, BT1

The M706 Teletype Receiver is a serial-to-parallel teletype code converter self contained on a double height module. This module includes all of the serial-to-parallel conversion, buffering, gating, and timing (excluding only an external clock necessary to transfer information in an asynchronous manner between a serial data line or teletype device and a parallel binary device). Either a 5-bit serial character consisting of 7.0, 7.5, or 8.0 units or an 8-bit serial character of 10.0, 10.5, or 11.0 units can be assembled into parallel form by the M706 through the use of different pin connections on the module. When conversion is complete, the start and stop bits accompanying the serial character are removed. The serial character is expected to be received with the start bit first, followed by bits 1 through 8 in that order, and completed by the stop bits. Coincident with reception of the center of bit eight, the Flag output goes low indicating that a new character is ready for transmission into the parallel device. The parallel data is available at the Bit 1 through Bit 8 outputs until the beginning of the start bit of a new serial character as received on the serial input. See the timing diagram of Figure 1 for additional information.

In addition to the above listed features, the M706 includes the necessary logic to provide rejection of spurious start bits less than one-half unit long, and half-duplex system operation in conjunction with the M707. Device selector gating is also provided so that this module can be used on the positive I/O bus of either the PDP8/I or the PDP8/L.

Inputs: All inputs present one TTL unit load except where noted. When input pulses are required, they must have a width of 50 nsec or greater.

Clock: The clock frequency must be eight times the serial input bit rate (baud rate). This input can be either pulses or a square wave. Input loading on the clock line is three unit loads.

Enable: This input when brought to ground will inhibit reception of new characters. It can be grounded any time during character reception, but returned high only between the time the Flag output goes to ground and a new character start bit is received at the serial input. When not used this input should be tied to a source of +3 Volts.

I/O Clear: A high level or positive pulse at this input clears the Flag and initializes the state of the control. When not used, or during reception, this input should be at ground.

Code Select Inputs: When a positive AND condition occurs at these inputs the following signals can assume their normal control functions—Flag Strobe, Read Buffer, and Clear Flag 1. Frequently these inputs might be used to multiplex receiver modules when a signal like Read Buffer is common to many modules. The inputs can also be used for device Selector inputs when the M706 is used on the positive I/O bus of the PDP8/I or PDP8/L. The code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If it is desired to bypass the code select inputs, they can be left open and the Enable D.S. line tied to ground.

Clear Flag 1: A high level or positive pulse at this input while the code select inputs are all high, will clear the Flag. When not used, this line should be grounded. Propagation delay from input rise until the Flag is cleared is a maximum of 100 nsec. The Flag cannot be set if this input is held high.

Clear Flag 2: A high level or positive pulse at this input, independent of the state of the code select inputs, will clear the Flag. All other characteristics are identical to those of Clear Flag 1.

Flag Strobe: If the Flag is set, and the code select inputs are all high, a positive pulse at this input will generate a negative going pulse at the Strobed Flag output. Propagation delay from the strobe to output is a maximum of 30 nsec.

Read Buffer: A high level or positive pulse at this input while the code select inputs are all high will transfer the state of the shift register to outputs Bit 1 through Bit 8. Final parallel character data can be read by this input as soon as the Flag output goes to ground. Output data will be available a maximum of 100 nsec after the rising edge of this input. See the timing diagram of Figure 1 for additional information.

Reader On: A low level or ground at this input will turn the internal reader flip-flop on. This element is turned off at the beginning of a received character start bit. This input can also be pulsed by tying it to one of the signals derived at output pins AE2 or BE2. A low output will exist at pin BE2 if the M706 is addressed and the clear Flag 1 (pin BJ2) is high. A low output will exist at pin AE2 if the M706 is addressed and the Clear Flag 1 (pin BJ2) is high or if Clear Flag 2 (pin BD1) is high.

Serial Input: Serial data received on this input is expected to have a logical zero (space) equal to +3 Volts and a logical 1 (mark) of ground. The input receiver on the M706 is a schmitt trigger with hysterisis thresholds of nominally 1.0 and 1.7 Volts so that serial input data can be filtered up to 10% of bit width on each transition to remove noise. This input is diode protected from voltage overshoot above +5.9 Volts and undershoot below —0.9 Volts. Input loading is four unit loads.

Outputs: All outputs can drive ten unit loads unless otherwise specified.

Bits 1 through 8: A read Buffer input signal will transfer the present shift register contents to these outputs with a received logical 1 appearing as a ground output. If the Read Buffer input is not present, all outputs are at logical 1. When the M706 is used for reception of 5-bit character codes, the ouput data will appear on output lines Bit 1 through 5 and bits 6, 7, 8 will have received logical zeros.

Active (0): This output goes low at the beginning of the start bit of each received character and returns high at the completion of reception of bit 8 for an 8-bit character or of bit 5 for a 5-bit character. Since this signal uses from ground to +3 Volts one-half bit time after the Flag output goes to ground, it can be used to clear the flag through Clear Flag 2 input while the Flag Output after being inverted can strobe parallel data out when connected to Read Buffer.

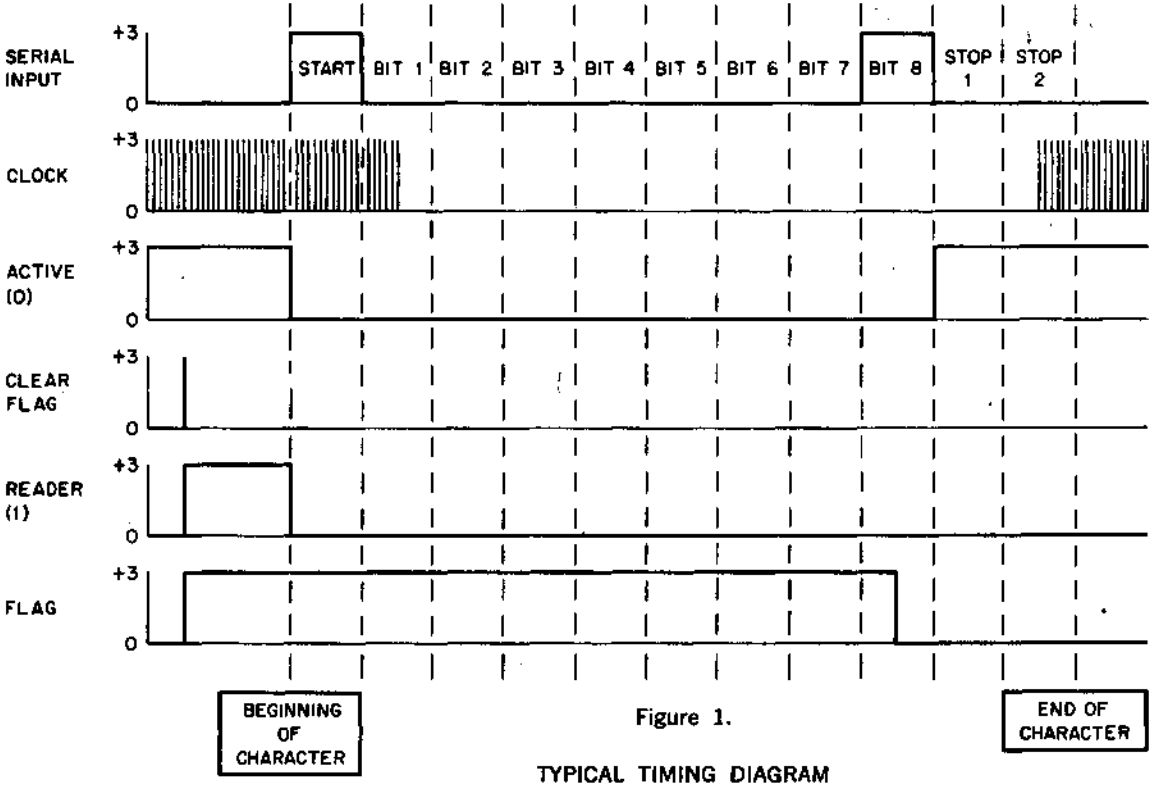


Figure 1.

TYPICAL TIMING DIAGRAM
Serial Input-Parallel Output 8-Bit (01, 111, 111)-2 Unit Stop Time

If an M706 and M707 are to be used in half duplex mode, this output should be tied to the Wait input of the M707 to inhibit M707 transmission during M706 reception. Output drive is eight unit loads.

Flag: This output falls from +3 Volts to ground when the serial character data has been fully converted to parallel form. Relative to serial bit positions, this time occurs during the center of either bit 8 or bit 5 depending respectively on the character length. If the M706 is receiving at a maximum character rate, i.e. one character immediately follows another; the parallel output data is available for transfer from the time the Flag output falls to ground until the beginning of a new start bit. This is Stop bit time plus one-half bit time.

Strobed Flag: This output is the NAND realization of the inverted Flag output and Flag Strobe.

Reader (1): Whenever the internal reader flip-flop is set by the Reader ON input, this output rises to +3 Volts. It is cleared whenever a start bit of a new character received on the serial input.

Reader Run: For use with Digital modified ASR33 and ASR35 teletypes which have relay controlled paper tape readers. This output can drive a 20 ma at +0.7 Volts load. The common end of the load can be returned to any negative voltage not exceeding −20 Volts.

Pin AE2: This output is the logical realization of NOT (Clear Flag 1 or Clear Flag 2 or I/O Clear) and is a +3 Volts to ground output level or pulse depending on the input. This signal can be used to pulse Reader On for control of Reader Run as used in DEC PDP8/I or PDP8/L computers.

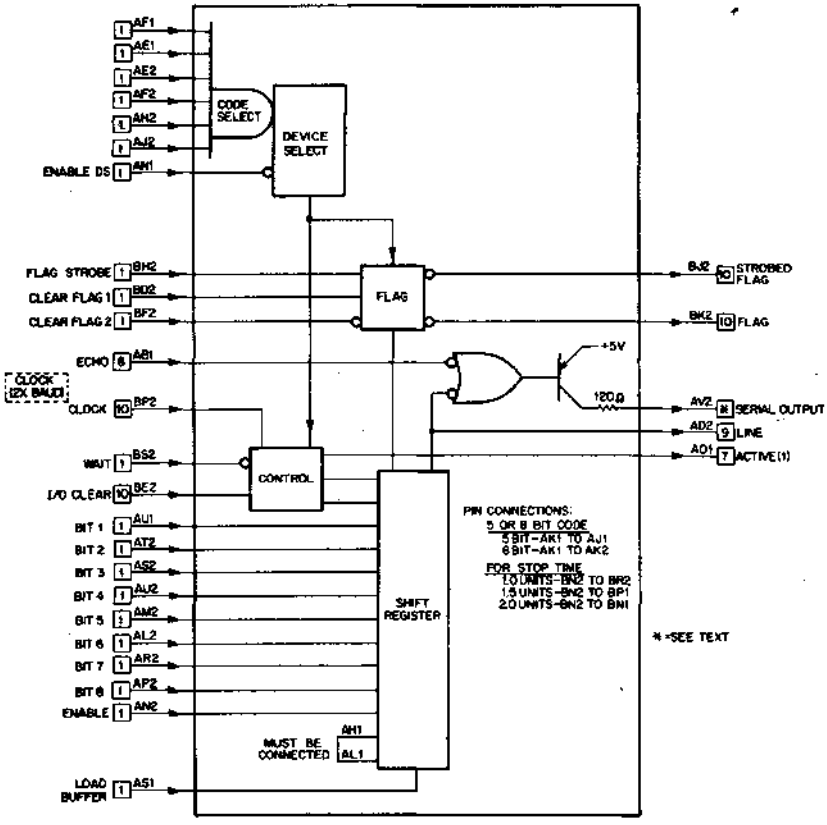
Pin BE2: This output is brought from +3 Volts to ground by an enabled Clear Flag 1 input. It can be connected to Reader On for a different form of control of Reader Run.

M707
TELETYPE TRANSMITTER

MISCELLANEOUS

M SERIES

Length: Standard
Height: Double
Width: Single



Volts	Power mA (max.)	Pins
+5	375	A2
GND		C2, T1

The M707 Teletype Transmitter is a parallel-to-serial teletype code converter self contained on a double height module. This module includes all of the parallel-to-serial conversion, buffering, gating, and timing (excluding only an external clock) necessary tot ransfer information in an asynchronous manner between a parallel binary device and a serial data line or teletype device. Either a 5-bit or an 8-bit parallel character can be assembled into a 7.0, 7.5, or 8.0 unit serial character or a 10.0, 10.5, or 11.0 unit serial character by the M707 through the use of different pin connections on the module. When conversion is complete, the necessary start bit and selected stop bits (1.0, 1.5, or 2.0 units) have been added to the original parallel character and transmitted over the serial line. The serial character is transmitted with the start bit first, followed by bits 1 through 8 in that order, and completed by the stop bits. Coincident with the stop bit being put on the serial line, the Flag output goes low indicating that the previous character has been transmitted and a new parallel character can be loaded into the M707. Transmission of this new character will not occur until the stop bits from the previous character are completed. See the timing diagram of Figure 1 for additional information.

In addition to the above listed features, the M707 includes the necessary gating so that it can be used in a half-duplex system with the M706. Device selector gating is also provided so that this module can be used on the positive bus of either the PDP8/I or the PDP8/L.

Inputs: All inputs present one TTL unit load with the exception of the Clock input which presents ten unit loads. Where the use of input pulses is required, they must have width of 50 nsec or greater.

Clock: The clock frequency must be twice the serial output bit rate. This input can be either pulses or a square wave.

Bits 1 through 8: A high level at these inputs is reflected as a logic 1 or mark in the serial output. When a 5-bit code is used, bit inputs 1 through 5 should contain the parallel data, bit 6 should be considered as an Enable, and bits 7, 8 and Enable should be grounded.

Enable: This input provides the control flexibility necessary for transmitter multiplexing. When grounded during a Load Buffer pulse, this input prevents transmission of a character. It can be driven from the output of an M161 for scanning purposes or in the case of a single transmitter, simply tied to +3 Volts.

Wait: If this input is grounded prior to the stop bits of a transmitted character, it will hold transmission of a succeeding character until it is brought to a high level. A ground on this line will not prevent a new character from being loaded into the shift register. This line is normally connected to Active (0) on a M706 in half duplex two wire systems. When not used, this line should be tied to +3 Volts.

Code Select Inputs: When a positive AND condition occurs at these inputs the following signals can assume their normal control functions—Flag Strobe, Load Buffer, and Clear Flag 1. Frequently these inputs might be used to multiplex transmitter modules when signals like Load Buffer are common to many modules. These inputs can also be used for device selector inputs when the M707 is used on the positive bus of the PDP8/I or PDP8/L. The

code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If it is desired to by-pass the code select inputs, they can be left open and the Enable DS line tied to ground.

Clear Flag 1: A high level or positive pulse at this input while the code select inputs are all high, will clear the Flag. When not used, this line should be grounded. Propagation delay from input rise until the Flag is cleared at the Flag output is a maximum of 100 nsec. The Flag cannot be set if this input is held at logic 1.

Clear Flag 2: A low level or negative pulse at this input will clear the Flag. When not used this input should be tied to +3 Volts. The Flag will remain cleared if this input is grounded. Propagation from input fall to Flag output rise is a maximum of 80 nsec. If it is desired to clear the flag on a load buffer pulse, Clear Flag 2 can be tied to pin AR1 of the module.

Flag Strobe: If the Flag is set, and the code select inputs are all high, a positive pulse at this input will generate a negative going pulse at the Strobed Flag output. Propagation delay from the strobe to output is a maximum of 30 nsec.

I/O Clear: A high level or positive pulse at this input clears the Flag, clears the shift register and initializes the state of the control. This signal is not necessary if the first serial character transmitted after power turn-on need not be correct. When not used, or during transmission, this input should be at ground.

Load Buffer: A high level or positive pulse at this input while the code select inputs are all high will load the shift register buffer with the character to be transmitted. If the Enable input is high when this input occurs, transmission will begin as soon as the stop bits from the previous character are counted out. If a level is used, it must be returned to ground within one bit time (twice the period of the clock).

Outputs: All outputs present TTL logic levels except the serial output driver which is an open collector PNP transistor with emitter returned to +5 Volts.

Serial Output: This open collector PNP transistor output can drive 20 mA into any load returned to a voltage between +4 Volts and —15 Volts. A logical output or mark is +5 Volts and a logical 0 or space is an open circuit. If inductive loads are driven by this output, diode protection must be provided by connecting the cathode of a high speed silicon diode to the output and the diode anode to the coil supply voltage.

Line: This output can drive ten TTL unit loads and presents the serial output signal with a logical 1 as +3 Volts and logical 0 as ground.

Active: During the time period from the occurrence of the serial start bit and the beginning of the stop bits, this output is high. This signal is often used in half duplex systems to obtain special control signals. Output drive is eight TTL unit loads.

Flag: This output falls from +3 Volts to ground at the beginning of the stop bits driving a character transmission. The M707 can now be reloaded and the Flag cleared (set to +3 Volts). This output can drive ten TTL unit loads.

Strobed Flag: This output is the NAND realization of the inverted Flag output and Flag Strobe. Output drive is ten TTL unit loads.
+3 Volts: Pin BJ1 can drive ten TTL unit loads at a +3 Volts level.

Power: +5 Volts at 375 mA. (max.)

Size: Standard, double height, single width FLIP CHIP module.

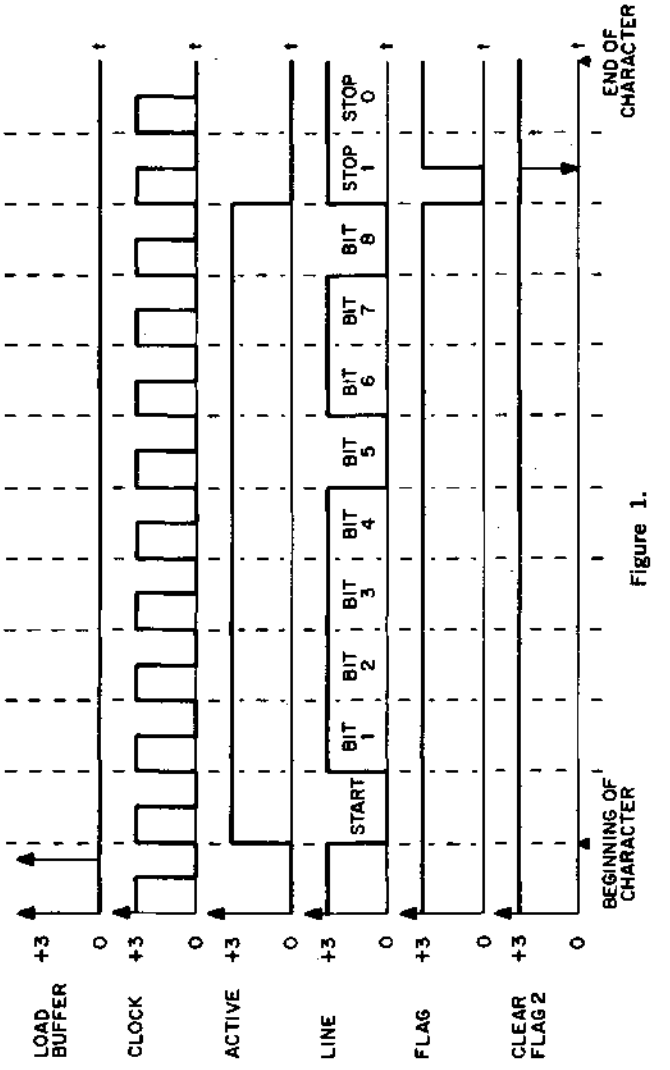


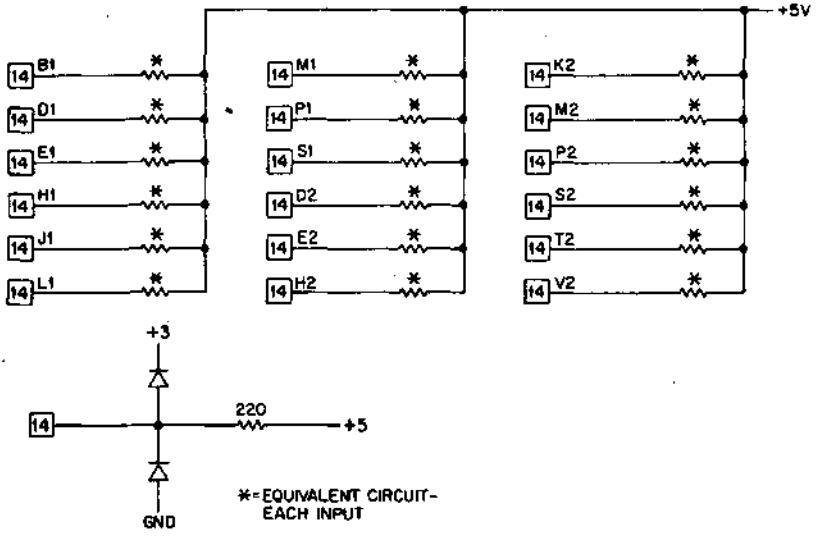
Figure 1.
Typical Timing Diagram, Parallel input, 8-Bit Character (11, 110, 110) With two bit Stop time.

M906
CABLE TERMINATOR

MISCELLANEOUS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	440*	A2
GND**		A1, C1, F1, K1, N1, R1, T1 C2, F2, J2, L2, N2, R2, U2

* all signal lines grounded
** all ground pins must be grounded

The M906 cable terminator module contains 18 load resistors which are clamped to prevent excursions beyond +3 volts and ground. It may be used in conjunction with M623 to provide cable driving ability similar to M661 using fewer module slots.

APPLICATIONS

The M906 may be used to terminate inputs. In this configuration M906 and M111 are a good combination.

This module is normally used with standard M Series levels of 0 and +3 volts to partially terminate 100-ohm cable. It presents a load of 22.5 mA or 14 TTL unit loads at ground and, therefore, must be driven from at least an M116-type circuit or, preferably, a cable driver.

M7389
ASYNCHRONOUS TRANSCEIVER

MISCELLANEOUS

M SERIES

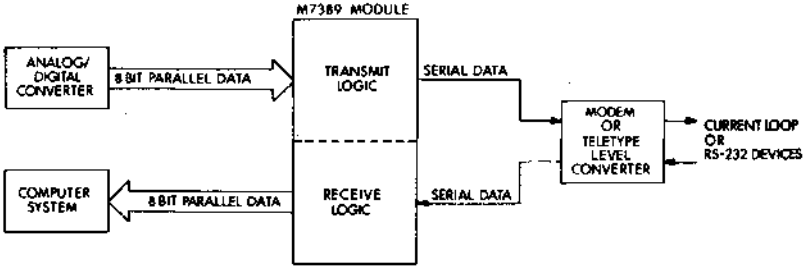
Length: Extended
Height: Double
Width: Single

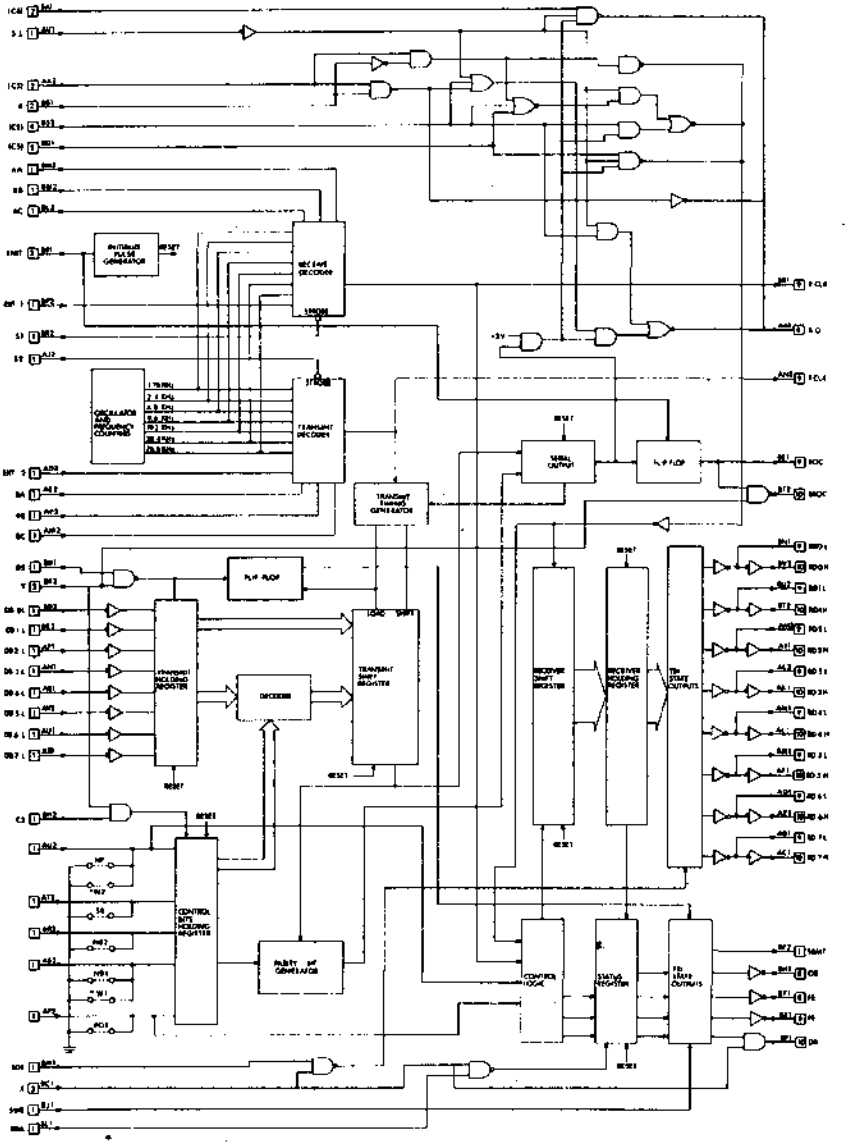
The M7389 Asynchronous Transceiver is a data communications interface module capable of operating in a full-duplex or half-duplex receive and transmit mode. During transmission, the M7389 accepts an 8-bit parallel data word, from a computer or terminal, appends control and error information onto the word, and serially transmits the word at a predetermined rate to an asynchronous serial receiver (Teletype or modem-type interface). In the receive mode, the module accepts serial binary data from a Teletype or modem interface at a predetermined rate, removes the appended control information, monitors the error status, and converts the word to a parallel data word for transmission to a computer or terminal.

The baud rate, bits per character, parity mode, odd or even parity select, and number of stop bits are externally selectable by control signals or by jumper lead connections on the module. The baud rate of the transmitted and received data is determined by the selection of a clock frequency internally generated on the module. A separate clock is provided for both the transmit and receive circuit functions, and the clock frequency is selected by TTL levels applied to the three control lines associated with each clock and frequency divider circuit.

APPLICATIONS

The M7389 Module provides asynchronous serial line compatibility for full- or half-duplex data communications applications. The M7389 can be used to control the level converters associated with modems conforming to EIA Standard RS-232 and Teletypes or similar devices. The M594 module can be used to convert the serial information between the modem and the M7389 and the M598 can be used as a signal interface between a 20 mA current loop device and the M7389.





Power		
Volts	mA (max.)	Pins
+5V	480	AA2, BA2
−15V	28	AB2

FUNCTION

Transmit Mode

A character transmission is initiated when the parallel data on lines DB0-DB7 is loaded into the transmit holding register by an externally generated Data Strobe (DS) pulse. Data bit DB0 is the least significant bit, and the transmitter accepts TTL-compatible inputs with a low voltage as a logic 1 and a high voltage as a logic 0. The corresponding serial data bit at the output will be a HIGH TTL compatible level for a HIGH input.

The DS pulse required is a positive-going pulse with a 250 ns (min.) pulse width and occurring 200 ns (min.) after the data is applied to the DB0-DB7 lines. The data is loaded into the transmit holding register by the leading edge of the DS pulse and transferred from the holding register to the serial shift register by the trailing edge. The word is formatted according to the control information entered into the control bit holding register, and the proper start, stop, and parity bits are appended to the specified number of bits per word. The asynchronous character is transmitted serially by bit, with the least significant bit first, at the clock rate determined by the frequency selected from the transmit decoder. Three control inputs BA, BB, and BC) to the decoder are used to select one of seven frequencies from the internal crystal oscillator or one input externally generated (EXT 2). To enable the decoder, a low level (0) is applied to the (S) input.

The transmitter buffer empty (TBMT) flag becomes high when the transmit holding register is ready to accept a new data word on DB0 to DB7.

When the character generated has been transmitted from the serial output logic, the end of character flag (EOC) becomes a high level to indicate that the transmission is complete. A new character can be loaded into the transmit holding register prior to the transmission of the previous character; however, the TBMT flag should be monitored to prevent loss of data.

The M7389 provides a number of control and error signals that provide convenient integration into logic systems. They may be grouped as follows:

- Receiver control
- Format control
- Error signals
- Transmitter control
- Miscellaneous functions

Receive Mode

In the receive mode, the M7389 receives asynchronous serial characters and assembles the characters for parallel transmission. The serial input is TTL-compatible and requires a low level 0 (Marking) between character transmissions. The receiver accepts a data word according to the format specified by the control information entered into the control bit holding register. The number of data bits, stop bits, and parity bits may be controlled.

A character is assembled when a "start bit" is recognized. A "start bit" is defined as a "mark" (low) to "space" (high) transition with a duration equal to one full bit time (16 clock times). When a mark to space transition is detected at the serial input of the module, a sample mode is initiated. If the input line is still "spacing" eight clock periods after the transition, the bit is recognized as a legal "start bit" and character assembly begins. If, however, the line is "marking," at the 8th bit time the transition is interpreted as a noise spike and is rejected. Once the start bit is recognized, the proper number of data bits and stop bit is accepted. When a full character is assembled, the data available (DA) flag is raised.

The receiver portion of the M7389 is also double buffered. When a serial character is assembled, it is transferred to a parallel output register. This allows the serial input shift register to accept another character while the previous character is available to external equipment.

Additional control and error characters are available as outputs.

Error Signals
Three types of errors can be detected by the error circuits on the module: overrun, framing, and parity.

Overrun: An overrun error flag is generated when the Data Available (DA) flag has not been reset by the Reset Data Available (RDA) before another DA flag is generated.

Framing: A framing error occurs when a received character is missing a stop bit.

Parity: A parity error occurs when the parity of the received character does not conform with programmed parity selection.

Baud Rate Selection
Table 1 lists the TTL-compatible control input levels required by the transmit and receive multiplexer to select the proper frequency associated with a specific Baud rate. In addition, an external frequency can be applied to the multiplexers and selected by the input levels for baud rates not available from the existing clock frequencies.

TABLE 1
BAUD RATE SELECTION

Control Inputs						Clock Frequency KHz	Baud Rate
Receive			Transmit				
AC	AB	AA	BC	BB	BA		
0	0	0	0	0	0	1.76	110
0	0	1	0	0	1	2.4	150
0	1	0	0	1	0	4.8	300
0	1	1	0	1	1	9.6	600
1	0	0	1	0	0	19.2	1200
1	0	1	1	0	1	38.4	2400
1	1	0	1	1	0	76.8	4800
1	1	1	1	1	1	*(External Supplied Clock)	

*Maximum acceptable input frequency is 153.6 KHz (Baud 9600)
0 = low level
1 = high level

Word Formats
The serial data accepted by the module consists of a start bit, from five to eight data bits, a parity bit (optional), and one or two stop bits. The selection of the data formats is controlled by TTL level inputs generated externally from the module or by the connection of jumper leads on the module. Table 2 shows the TTL levels required at the inputs for the various data formats available.

The M7389 is supplied with jumpers connected for a data format of seven bit and for an even parity. Table 4 shows the data format for all combinations of SB, NB1, NB2, NP and POE. When a jumper is present, a logic 1 is selected.

Serial Line Control

The line control levels permit the serial line inputs and outputs to be operated in full-duplex mode (receive and transmit asynchronously), half-duplex mode (receive or transmit at different intervals), local mode (serial output returned to serial input), and internal or external ECHO. The type of mode selected is determined by the TTL levels applied to serial control line inputs as listed on Table II. A high level on each input is the enable level; however, only one high level can be selected on inputs C2, C3, C4, and C5 during the same interval.

Data Line Signals

DB0L-DB7L	**Data Bit 0-7:** Eight input lines that receive the parallel data from a computer or terminal.
RD0H-RD7H	**Receive Data Bit 0-7:** Eight output lines that transmit the parallel data to computer or terminal.
RD0L-RD7L	**Receive Data Bit 0-7:** Eight output lines that transmit the inverse levels of RD0H-RD7H.
SO	**Serial Output:** An output line that transmits the serial data, by bit, to the Teletype or modem-type interface. A low level signal is present on the SO line during the idle state.
SI	**Serial Input:** An input line that receives the serial data, by bit, from the Teletype or modem-type interface. The SI line must be held low in the idle state.

TABLE II

OPERATING MODE SELECTION

Input Signals					Mode Description
C2	C3	C5	C6	R	
1	0	0	0	0	The serial output data from the transmitter logic is gated to the serial input of the receiver logic. The serial input from the Teletype or modem-type interface is gated to the serial output to Teletype or modem interface.
0	1	0	0	0	Specifies a transmit operation in the half-duplex mode.
0	1	0	0	1	Specifies a receive operation in half-duplex mode.
0	0	1	0	0	Internal ECHO. Serial input to module from Teletype or modem-type interface is OR gated with serial output of transmitter logic before transmission to receiver logic.
0	0	0	1	0	External ECHO. Serial input from Teletype or modem-type interface is OR gated with serial output from transmitter logic before output to Teletype or modem-type interface.

Transmitter Control/Status Signal

TBMT **Transmitter Buffer Empty:** A high level on this line indicates that the transmitter holding register is empty and ready to receive a new character.

EOC **End of Character:** A high level on this line indicates that a full serial character, including stop bit, has been transmitted from the module.

BEOC **Buffered End of Character:** The EOC signal gated with the Y enable signal.

DS **Data Strobe:** A positive pulse of 250 ns (min.) duration is required on this line to enter data bits DB0 — DB7 into the transmitter holding register and to serially transfer the data from the transmitter holding register.

TCLK **Transmit Clock:** This line contains the transmitter clock frequency selected by inputs BA, BB, and BC. Refer to Table 1.

Receiver Control and Status Signals

DA — **Data Available:** A high level on this line indicates that an entire input character has been received and transferred to the receiver holding register.

RDE — **Receive Data Enable:** A high level on this line transfers the received data to output lines RD0H — RH7H and RD0L — RD7L.

RDA — **Reset Data Available:** A high level on this line resets the DA status line.

SWE — **Status Word Enable:** A low level on this line transfers the status word bits PE, OR, FE, DA, and TBMT onto the output lines.

OR — **Overrun:** A low level on this line indicates that the character in the receiving holding register has not been read (DA not reset) before the next character is transferred to the receiver holding register.

FE — **Framing Error:** A low level on this line indicates that the received character from the Teletype or modem-type interface has no valid stop bit.

PE — **Receive Parity Error:** A low level on this line indicates that the received character parity does not conform to the parity selected by the POE input.

RCLK — **Receive Clock:** This line contains the receiver clock frequency selected by inputs AA, AB, and AC. Refer to Table 1.

Miscellaneous Inputs

EXT 1 — **External Clock 1:** An input line used to enter an external clock frequency to control the baud rate of the receiver. Refer to Table I for the control input levels required.

EXT 2 — **External Clock 2.** An input line used to enter an external clock frequency to control the baud rate of the transmitter. Refer to Table I for the control input levels required.

S1 — **Receiver Clock Enable:** A low level on this line enables the receiver clock decorder.

S2 — **Transmitter Clock Enable:** A low level on this line enables the transmitter clock decoder.

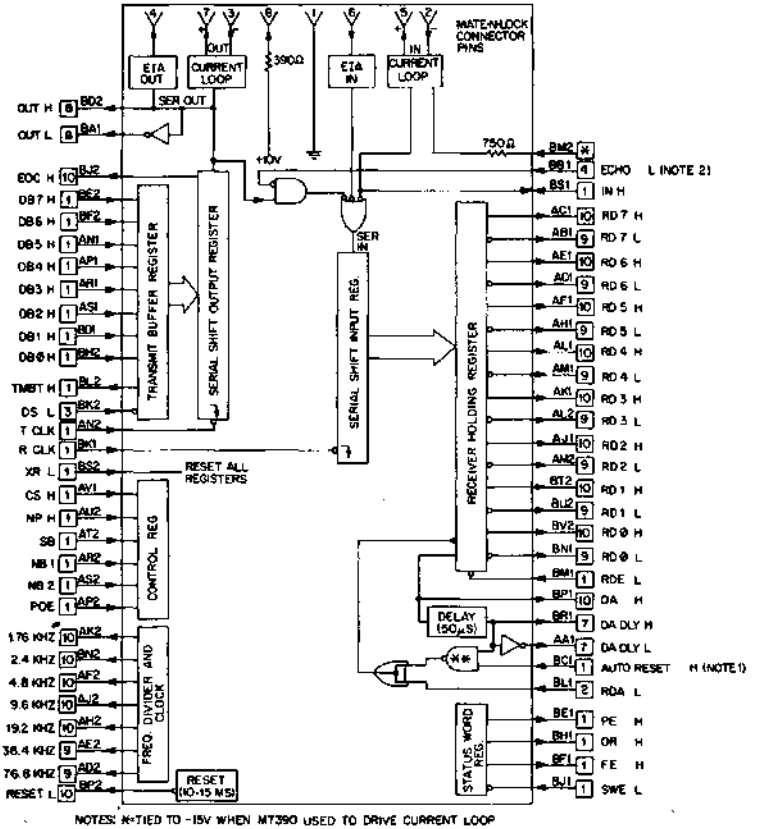
INIT — **Initialize:** A high to low transition on this line resets all registers and flags.

M7390
ASYNCHRONOUS TRANSCEIVER

MISCELLA-NEOUS

M SERIES

Length: Extended
Height: Double
Width: Single



NOTES: *=TIED TO -15V WHEN M7390 USED TO DRIVE CURRENT LOOP
**=OPEN COLLECTOR OUTPUT
1. MUST BE TIED TO GROUND IF RDA L NOT USED
2. MAY BE LEFT OPEN IF ECHO NOT DESIRED

Volts	Power mA (max.)	Pins
+5	700	BA2
+10	3	AV2
GND		BC2
−12*	64	BR2
−15*	80	BB2

*Requires −12 V or −15 V only, not both.

DESCRIPTION

The M7390 asynchronous transceiver is a modular subsystem which provides asynchronous serial line compatibility for data communications applications. The M7390 combines input/output level converters, parallel-to-serial and serial-to-parallel conversion, and a crystal controlled clock, into one module.

APPLICATIONS

The M7390 can be used for computer terminal applications, data entry devices or any system which requires asynchronous serial line compatibility. The M7390 may also be used to drive modems conforming to EIA RS-232C specifications or current-operated devices such as Teletypes.

FUNCTIONS

There are three groups of functions on the M7390—error detection, data, and control.

Error Detection: The error function of the module allows three types of errors to be detected. These are:

1. Parity: If the received parity bit does not agree with the expected parity bit, the parity error flag is set.
2. Overrun: The receiver section of the M7390 is fully double buffered. Therefore, one full character time is allowed to remove the received data from the receiver buffer before a new character is assembled and transferred. If the character is not removed before a new one is loaded, the overrun flag is set.
3. Framing: Since the M7390 is asynchronous, the absence of a stop bit can be detected. For example, an eight bit data character would have one start bit, eight data bits, and one or two stop bits. Therefore, a stop bit is expected as the 10th bit to be received. If the 10th bit is in the logic TRUE (marking) condition no error is detected. However, if the 10th bit is a logic FALSE (spacing) condition, the framing error flag is set. The framing error flag is useful for detecting open lines or null characters.

Data Functions: The M7390 performs serial-to-parallel and parallel-to-serial conversion. The parallel side of the module is TTL compatible. The serial inputs and outputs are available as three signal sources: EIA, current loop or TTL. The current loop and EIA input and output are available only on the eight-pin MATE-N-LOK connector on the front of the module.

The EIA input corresponds to RS-232C specifications. In addition to the EIA signals RECEIVED DATA and TRANSMITTED DATA, the DATA TERMINAL READY signal and SIGNAL GROUND are also provided.

The current loop input/output is designed to operate on a 20 to 100 mA current loop. The M7390 uses optical couplers to provide 1500 volts of isolation between the M7390 ground and power and the driving source. The serial input will respond to a 20 mA current flow. Current flow is a marking condition (binary 1). The external source must not exceed 35 volts dc open circuit voltage or 100 mA current. The serial output is a transistor switch that can turn a current loop on or off. The open circuit voltage of the current source must not exceed 35 volts dc.

The TTL versions of the serial input and output signals are available on the module pins and may be used in place of the level converter signals.

Control: The M7390 provides full control of the receiver and transmitter sections. All control pulses must be greater than 250 ns in width. Data to be loaded into the module must be present 250 ns before the DATA STROBE pulse.

Receiver Control Signals:

DA	Data Available
DA DLY	Delayed Data Available
AUTO RESET	Allows DA to be automatically reset.
RDE	Receiver Data Enable. Places data and control signals on the pins of the module.
RDA	Reset Data Available

Transmitter Control Signals:

TBMT	Transmitter Buffer Empty
ECO	End of Character

Error Control and other Signals:

NP	No Parity
POE	Parity Odd or Even
SWE	Status Word Enable
CS	Control Strobe
NB1, NB2	Number of Bits in data word
SB	Number of Stop Bits (1 or 2)
XR	External Reset (clears all registers)
RESET	Negative pulse used for clearing module during power-up.
RCLK	Receiver Clock Input
TCLK	Transmitter Clock Input

PRECAUTIONS

1. EIA and current loop connections are available on an 8-pin MATE-N-LOK connector located in the handle position on the B half of the board.
2. Provision is made to power this module from either −15 or −12 volts dc. Do not use both simultaneously.
3. Current loop input and output circuits must not have more than 35 volts peak applied or greater than 100 mA current flow.
4. The M7390 contains an MOS LSI chip. Care must be taken in proper handling and grounding of the module to prevent damage to the MOS chip.
5. The +10 volt dc supply is required only if the EIA level converters are used, or if the module is going to be used as a current source.
6. If the M7390 is used as a current source, 20 mA additional current must be supplied by the −15 volt and the +10 volt power supplies.

SPECIFICATIONS

Data Format: Asynchronous, serial by bit, least significant bit first.
Input/Output Level (Serial):

1. EIA RS-232C: Binary 1 = −3 to −25 volts dc
   Binary 0 = +3 to +25 volts dc
2. Current Loop: Mark (Binary 1) = 20 to 100 mA current flow
   Space (Binary 0) = <3 mA current flow
3. TTL: Binary 1 = HIGH
   Binary 0 = LOW

Data Rates: (TTY Mode) 110, 150, 300 Baud
(EIA Mode) 110, 150, 300, 600, 1200, 2400, and 4800 Baud.

Character Format: One start, 5, 6, 7, 8 data, parity (if requested), one or two stop bits.

Clock Frequencies (kHz): 1.76, 2.4, 4.8, 9.6, 19.2, 38.4, 76.8

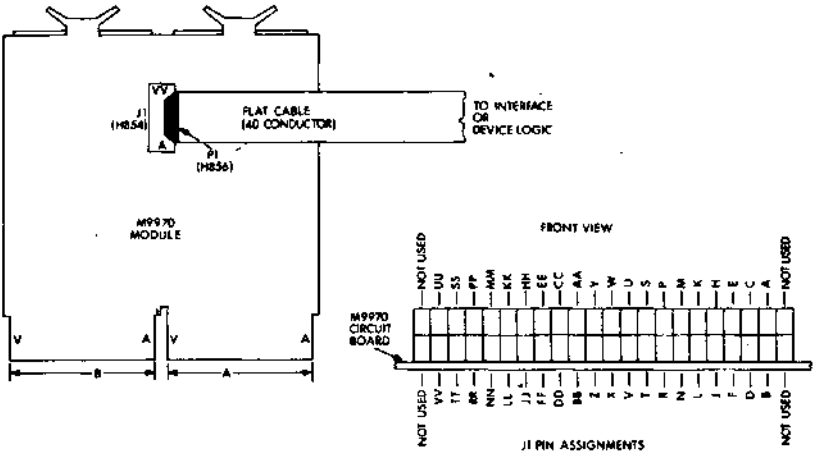
Input/Output Levels (Parallel): All TTL compatible.

M9970
H854-TO-BACKPLANE ADAPTER

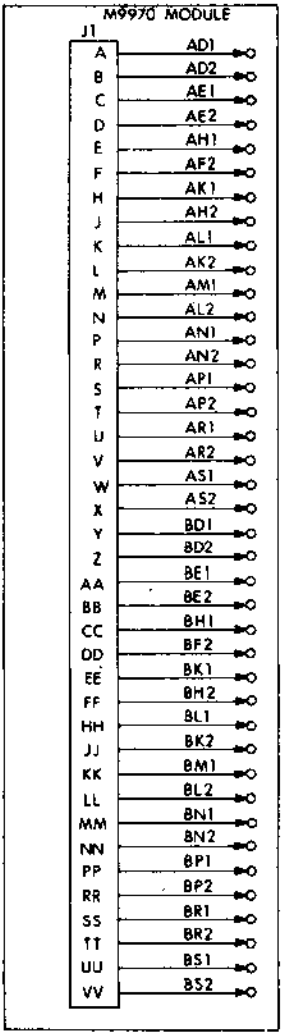
MISCELLA-NEOUS

M SERIES

Length: Extended
Height: Double
Width: Single



The M9970 is a double-height, extended-length module with an H854 Male Connector permanently mounted to the board. Each of the 40 pins of the H854 connect to the edge board contacts of the module through printed circuit wiring. The H854 will accept any standard or special flat cable with an H856 Plug mounted on the cable end. The module can be used as an adapter to transfer signals and levels to or from a device or interface logic and the backplane wiring of a system unit or connector block. To facilitate installation with DIGITAL systems, none of the signal lines of the M9970 Module connect to the standard power or ground pins normally assigned to the FLIP CHIP modules.


M9970 MODULE
J1
A AD1
B AD2
C AE1
D AE2
E AH1
F AF2
H AK1
J AH2
K AL1
L AK2
M AM1
N AL2
P AN1
R AN2
S AP1
T AP2
U AR1
V AR2
W AS1
X AS2
Y BD1
Z BD2
AA BE1
BB BE2
CC BH1
DD BF2
EE BK1
FF BH2
HH BL1
JJ BK2
KK BM1
LL BL2
MM BN1
NN BN2
PP BP1
RR BP2
SS BR1
TT BR2
UU BS1
VV BS2

A SERIES

NOTES ON OPERATIONAL AMPLIFIERS

I. INTRODUCTION

This article describes some of the basic characteristics and uses of operational amplifiers. It is written especially for people with a digital background, but with a limited exposure to analog technology. The equations presented are not exact, but are good engineering approximations, which are accurate enough for most applications. It is hoped that this simplified discussion will provide more insight into the uses and limitations of operational amplifiers than a more rigorous approach.

The operational amplifier is a basic building block in analog work, much the same way as a NAND gate can be a basic building block in a digital computer. An operational amplifier (op amp) together with other components such as resistors and capacitors, can be used to perform addition, subtraction, integration, and many other functions. Op amps can be used to make oscillators, active filters, and even digital circuits such as Schmitt triggers, gates, and flip-flops. When used with A/D and D/A converters in data processing work, op amps perform such functions as scale changing, offsetting, and isolation between source and load.

II. GENERAL CHARACTERISTICS

An operational amplifier can be considered a 3 terminal device, plus a common or ground return, see Fig. 1. Chopper-stabilized op amps, which will not be considered here, have the Plus Input permanently tied to ground. The op amp is really a difference amplifier, in that it amplifies only the difference between the two inputs, and tries to reject any DC or AC signal that is common to both inputs.

Op amps are characterized by high DC gain, high input impedance, low output impedance, and a gain that decreases with increasing frequency. Op amps used without feedback would be operating open loop, a rare situation; but with feedback the operation would be closed loop. The use of properly applied negative feedback stabilizes the operation of the composite circuit against changes in the amplifier, and provides its versatility and usefullness.

When an op amp is working in the linear region, two approximations can be made to help in the analysis of the circuit configuration. First, the voltages of the two inputs are the same; and second, no current flows into or out of the input terminals. Fig. 2 shows a simple inverting amplifier. Assume the Minus Input is 0 volts, the same as the Plus Input, and that no current flows into the Minus Input, called the summing junction. Then $i_i = i_f$, and some simple manipulations show that the gain is equal to $-R_f/R_i$. Similar reasoning applied to the non-inverting amplifier of Fig. 3 shows that the gain is equal to $+\frac{R_1 + R_2}{R_1}$. An easy way to remember this is to think of the two resistors as forming a tapped divider network.

III. SPECIFICATIONS

Specifications are usually given for open loop performance, so that the user has to interpret and calculate how this will affect his particular closed loop circuit. The following section will give some brief descriptions of what some of the specifications mean.

Settling time. This is the time it takes the output to get within and stay within a certain amount of is final value, after the input has received a step input, see Fig. 4. This parameter is important when an amplifier is used in front of an A/D converter, since the A/D should not begin its conversion until the amplifier has settled.

Overload recovery. It takes an overload recovery time for the output to first assume its proper value after an overdriving input signal has been removed. However, the output still has not settled, and this extra time must be waited before the output is valid.

Slew rate. This term is comparable to rise or fall time in a digital circuit. It is a measure of how fast the output can change. If an amplifier output could go from 0 volts to 10 volts in 2 μsec, it would have a slew rate of 5 volts/μsec.

Frequency for full output. This is the maximum frequency at which a full scale sine wave (such as +10 to −10 volts) can be assured at the output, without noticeable distortion. In many ways this is real frequency limitation of an op amp, since up to this frequency there are no other restrictions on the amplitude of the input signal.

Frequency for unity gain. The open loop gain of an amplifier is equal to one at this frequency. But the input signal must be restricted in amplitude such that the maximum rate of change of output (slew rate) is not exceeded. Usually only millivolt signals may be processed at this frequency, therefore the full amplifier bandwidth is not usable for normal data processing systems.

Impedance. The input impedance is simply the resistance between the two inputs. The common mode impedance is the highest resistance attainable with feedback.

Common mode rejection. This is a measure of how well an amplifier will not respond to a signal common to both inputs. If used as a voltage follower, an op amp with a common mode rejection ratio (CMRR) of 10,000 could have error of 1 mv if the input were 10 v. (10/10,000 volts).

Voltage offset. The inability to achieve perfect balance in the input circuit causes the output to respond to an apparent signal when the inputs are tied to ground. For an inverting amplifier, the output error due to the input voltage offset is equal to the offset times the closed loop gain plus one. With an input offset of 3 mv, and a gain of 1, the output error would be 6 mv. Fortunately, initial voltage offset can be trimmed with a potentiometer at the right place in the circuit.

Current offset. Current offset (or bias current) multiplied by the feedback resistor (Fig. 2) produces an output error. This effect can be minimized by using the differential offset (the difference in offset currents for the two inputs) when the resistance seen from both inputs to ground are equal. For Fig. 2, the Plus Input should than be returned to ground through a resistor equal to the parallel combination of R_I and R_F.

Output ratings. The output voltage and current ratings imply a minimum value for the load resistor. 10 volts and 5 ma would correspond to a load resistor of 2 K. In an inverting amplifier, the feedback resistor is a load for the output, and the current through this resistor must be subtracted from

the amount of current still available at the output. All really useful operational amplifiers can be shorted to ground without damage, but shorting to a voltage will usually destroy some of the circuitry.

IV. APPLICATIONS

Some common configurations for operational amplifiers are shown in Figs. 5 through 10. The pin letter assignments correspond to the op amps sold by Digital Equipment Corp. If these op amps are used, the jumper between Pin S and the Minus input should be removed.

The voltage follower, Fig. 5, features high input impedance, but will have an error depending on the CMRR. Large voltages cannot be handled, since common mode voltage ratings should not be exceeded. The inverter configuration, Fig. 7, is very versatile and does not have a common mode voltage problem, since both inputs are near ground. Large input voltages can be handled if the input resistor is made appropriately large. One disadvantage of the inverting configuration is that the input impedance is relatively low, essentially equal to the input resistor. When a gain trim potentiometer is used, the gain accuracy by itself becomes irrelevant. What is important is gain resolution (mostly determined by the potentiometer), and the gain stability (mostly determined by the temperature coefficients of the input and feedback resistors). The ratio of the closed loop gain to the open loop gain gives the suitability of an amplifier as far as static accuracy is concerned. With a closed loop gain of 5, and an open loop gain of 10,000, an amplifier could be used in a system with an allowable error of 1 part in 2,000.

The possibility of oscillation must always be considered when feedback amplifiers are used. Usually the more feedback used, the greater is the tendency to oscillate. Oscillations can always be attributed to phase shift. Therefore, stabilization of operational amplifiers involves phase shifting to oppose oscillation. In Fig. 7, the feedback capacitor allows high frequency signals to be fed back to the inverting input (degenerative feedback) with a phase lead. In the inverting configuration, the output will be 180° out of phase with the input at low frequencies, and the feedback signal will oppose the input signal. At high frequencies, there are additional phase lags in the amplifier and feedback circuitry. If the feedback signal has a total phase shift (lag) of 360° with a gain through the amplifier and feedback network of greater than 1, the amplifier will oscillate, since the input and output are in phase.

V. REFERENCES

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   Analog Devices, Inc., Cambridge, Mass.
2. "Handbook of Operational Amplifier Applications"
   Burr-Brown Research Corp., Tucson, Arizona
3. "Linear Integrated Circuits Applications Handbook"
   Fairchild Semiconductor, Mountain View, California
4. "Applications Manual for Operational Amplifiers"
   Philbrick/Nexus Research, Dedham, Mass.

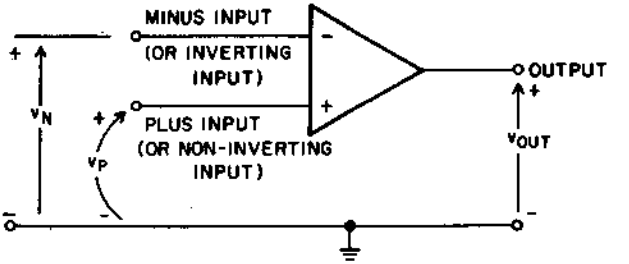
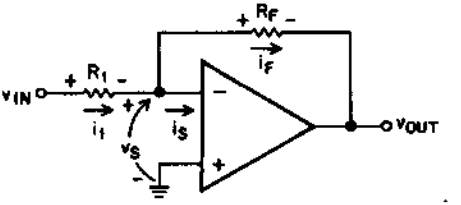


Fig. 1, Basic Operational Amplifier Symbol

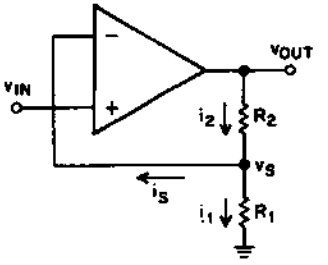


ASSUME: $v_S = 0$ THEN $i_1 = i_F$
$i_S = 0$

$$\frac{v_{IN}}{R_1} = -\frac{v_{OUT}}{R_F}$$

$$\frac{v_{OUT}}{v_{IN}} = -\frac{R_F}{R_1}$$

Fig. 2, Inverting Amplifier



ASSUME: $v_S = v_{IN}$
$i_S = 0$
THEN $i_1 = i_2$

$$\frac{v_S}{R_1} = \frac{v_{OUT} - v_S}{R_2}$$

$$\frac{v_{IN}}{R_1} = \frac{v_{OUT} - v_{IN}}{R_2}$$

$$v_{IN} R_2 = v_{OUT} R_1 - v_{IN} R_1$$

$$\frac{v_{OUT}}{v_{IN}} = +\frac{R_2 + R_1}{R_1}$$

Fig. 3, Non-Inverting Amplifier

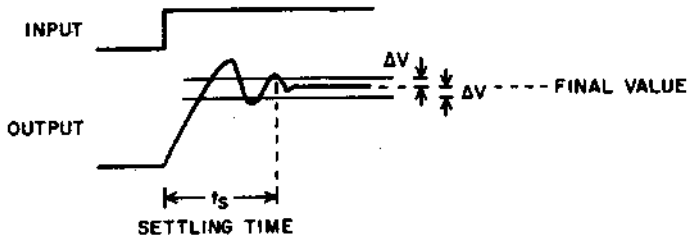
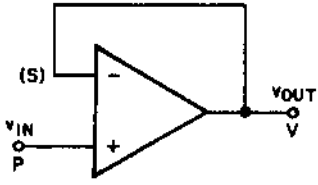


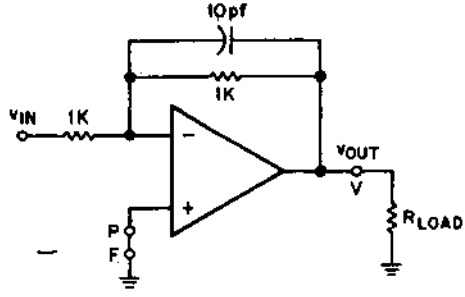
Fig. 4, Settling Time



$$\frac{V_{OUT}}{V_{IN}} = +1$$

$$R_{IN} = R_{COM\ MODE}$$

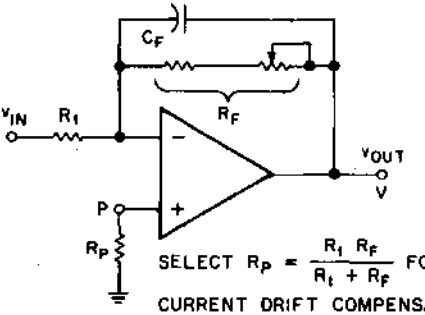
Fig. 5, Voltage Follower



$$\frac{V_{OUT}}{V_{IN}} = -1$$

$$R_{IN} = 1K$$

Fig. 6, Inverter



$\frac{V_{OUT}}{V_{IN}} \approx -\frac{R_F}{R_1}$

$R_{IN} = R_1$

GAIN STABILITY DEPENDS ON THE INPUT AND FEEDBACK RESISTOR, AND GAIN TRIM POTENTIOMETER.

TYP VALUES

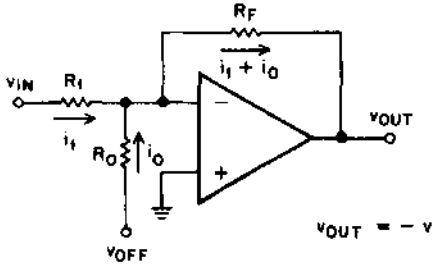
R_1 1K TO 10K

R_F 1K TO 100K

R_P 500Ω TO 5K

THE USE OF C_F REDUCES THE TENDENCY OF THE OP AMP TO OSCILLATE

Fig. 7, Adjustable Gain and Current Compensation



$V_{OUT} = -V_{IN}(\frac{R_F}{R_1}) + \underbrace{\left[-V_{OFF}\ (\frac{R_F}{R_O})\right]}_{\text{OFFSET}}$

Fig. 8, Offsetting

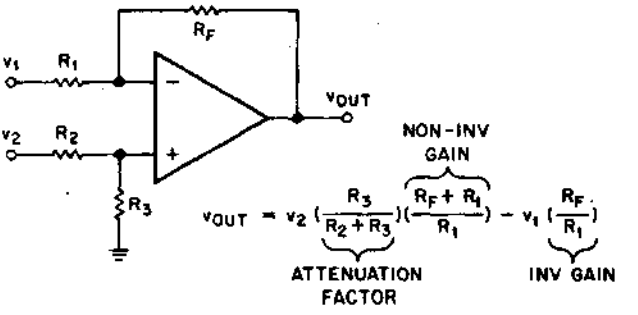


Fig. 9, Differential Gain

2^n and Resolution

2^n	# OF BITS n	RESOLUTION (%)	PPM
1	0	100.0	1,000,000
2	1	50.0	500,00
4	2	25.0	250,000
8	3	12.5	125,000
16	4	6.25	62,500
32	5	3.125	31,250
64	6	1.563	15,625
128	7	0.781	7,812
256	8	0.391	3,906
512	9	0.195	1,953
1 024	10	0.0977	977
2 048	11	0.0488	488
4 096	12	0.0244	244
8 192	13	0.0122	122
16 384	14	0.00610	61
32 768	15	0.00305	31
65 536	16	0.00153	15
131 072	17	0.000763	8

DIGITAL CODES FOR A/D'S, D/A'S AND DATA ACQUISITION SYSTEMS

OFFSET BINARY (BIPOLAR)

+ FULL SCALE −1 LSB	111111111111
+ 3/4 FULL SCALE	111000000000
+ 1/2 FULL SCALE	110000000000
ZERO	100000000000
− 1/2 FULL SCALE	010000000000
− 3/4 FULL SCALE	001000000000
− FULL SCALE +1 LSB	000000000001
− FULL SCALE	000000000000

STRAIGHT BINARY (UNIPOLAR)

+ FULL SCALE −1 LSB	111111111111
+ 3/4 FULL SCALE	110000000000
+ 1/2 FULL SCALE	100000000000
ZERO +1 LSB	000000000001
ZERO	000000000000

TWO'S COMPLEMENT (BIPOLAR)

+ FULL SCALE −1 LSB	011111111111
+ 3/4 FULL SCALE	011000000000
+ 1/2 FULL SCALE	010000000000
ZERO	000000000000
− 1/2 FULL SCALE	110000000000
− 3/4 FULL SCALE	101000000000
− FULL SCALE +1 LSB	100000000001
− FULL SCALE	100000000000

BINARY CODED DECIMAL (UNIPOLAR)

+ FULL SCALE −1 LSD	1001 1001 1001
+ 3/4 FULL SCALE	0111 0101 0000
+ 1/2 FULL SCALE	0101 0000 0000
ZERO + LSD	0000 0000 0001
ZERO	0000 0000 0000

A SERIES MODULES

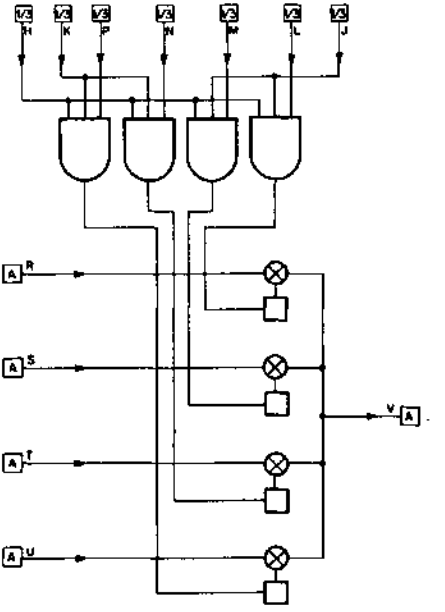
The following A Series Analog Module descriptions are contained in this subsection:

A123
FOUR-INPUT MULTIPLEXER

MULTI-PLEXERS

A SERIES

Length: Standard
Height: Single
Width: Single



A - ANALOG SIGNALS (DO NOT CONNECT TO LOGIC LEVELS)

Volts	Power mA (max.)	Pins
+10	18	D2
+5	45	A2
GND		C2, T1
−20	50	E2

The A123 Multiplexer provides 4 gated analog switches that are controlled by logic levels of 0V and +3V. The module is equivalent to a single-pole, 4-position switch, since one output terminal of each MOS FET switch is tied together. If all three digital inputs of a circuit are at +3V (or not connected) the two output terminals are connected together. If any digital input is at 0V, the switch terminals are disconnected. Two switches should not be on at the same time. The analog switch can handle signals between +10V and −10v, with currents up to 1 mA.

The positive power supply must be between +5V and +15V, and at least equal to or greater than the most positive excursion of the analog signal. The negative power supply must be between −5 and −20v, and at least 10 Volts more negative than the most negative excursion of the analog signal. The voltage difference between the two supplies must not be more than 30V.

SPECIFICATIONS

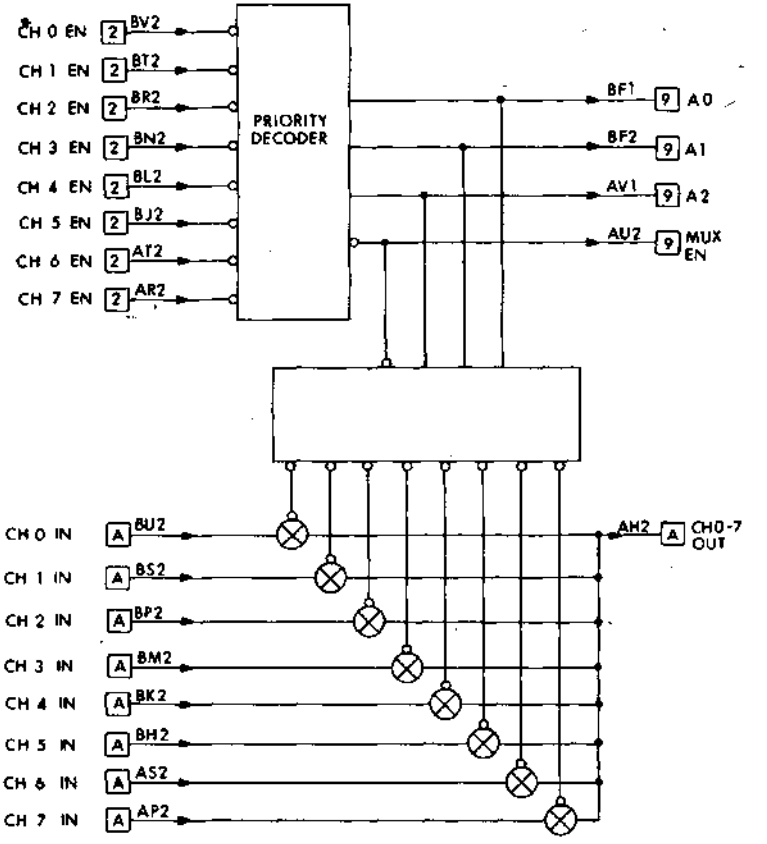
Digital Inputs	
Logic ONE:	+2.4v to +5.0V
Logic ZERO:	0.0v to +0.8V
Input loading:	0.5mA. at 0Volts
Analog Signal	
Voltage range:	+10v to −10v
Current (max.):	1 mA
Output Switch	
On resistance, max.:	1000 ohms
On offset:	0 Volts
Off leakage, capacitance:	10 nA, 10 pF
Turn on delay, max.:	0.2 μsec
Turn off delay, max.:	0.5 μsec

A126
8 CHANNEL HIGH IMPEDENCE MULTIPLEXER

MULTI-PLEXERS

A SERIES

Length: Standard
Height: Double
Width: Single



Volts	Power mA (max.)	Pins
+5V±5%	100	AA2
+15V±5%	17	AD1, AD2
−15V±5%	12	AE1; AE2
*GND	LOGIC	AC2, AT1
*GND	ANALOG	AF1, AF2

*Analog GND must be connected to LOGIC GND

The A126 is an eight-channel, high-impedance multiplexer module with each channel controlled by an associated enable input. The conduction or non-conduction of each channel is controlled by FETs and the channel outputs are connected together to a common terminal. Each channel is capable of switching bipolar (±12 V) analog signals and is protected against random switching in the event of overvoltage and power down or loss of power conditions.

FUNCTIONS

The enable inputs, associated with each channel, are priority encoded to ensure that only one channel is connected to the output at a time. Therefore, more than one Channel enable input can be asserted at one time. Channel 0 is the highest priority and channel 7, the lowest priority. The enable signals required are TTL or DTL compatible levels. Three TTL outputs are provided for identifying the selected channel, and one TTL multiplexer enable output indicates that one of the eight channels has been selected. The selected channel number is specified by an octal code on lines A0-A2.

APPLICATIONS

The A126 can be used to multiplex up to eight signals from the analog inputs into buffer amplifiers or circuits with a minimum input impedance of 10 megohms.

SPECIFICATIONS

Analog Inputs:

CH0 (IN) — CH7 (IN)	8 single-ended channel inputs
Voltage Range	±15 V (max.)
Impedance (ON)	1040 ohms ± 10%
Analog switch turn-on	1.0 μsec (max.)
Analog switch turn-off	0.5 μsec (max.)
Analog switch current	2.0 mA (max.)
Jumper W1	(Not for customer use)

TTL Input Signals

CH0 (EN) — CH7 (EN)	8 enable inputs associated with each channel
Input Voltage	Low (enable) — 0.8 V (max.) High (disable) — 2.0 V (max.)

TTL Output Signals

A0 — A2, MUX EN	Low — 0.4 V (max.) High — 2.4 V (min.)

TRUTH TABLE

TTL ENABLE INPUTS								OUTPUTS				
CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	MUX EN	A2	A1	A0	Analog Channel
H	H	H	H	H	H	H	H	H	H	H	H	NONE
H	H	H	H	H	H	H	L	L	H	H	H	7
H	H	H	H	H	H	L	X	L	H	H	L	6
H	H	H	H	H	L	X	X	L	H	L	H	5
H	H	H	H	L	X	X	X	L	H	L	L	4
H	H	H	L	X	X	X	X	L	L	H	H	3
H	H	L	X	X	X	X	X	L	L	H	L	2
H	L	X	X	X	X	X	X	L	L	L	H	1
L	X	X	X	X	X	X	X	L	L	L	L	0

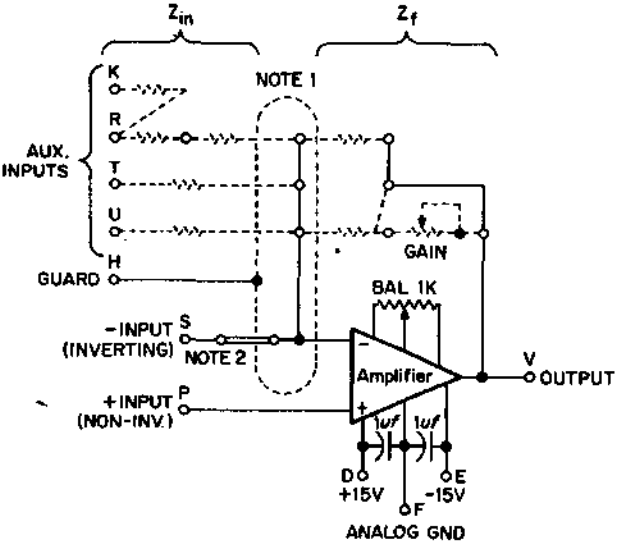
H = High Level L = Low Level X = Either High or Low

A207
OPERATIONAL AMPLIFIER

AMPLIFIERS

A SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+15	6	D2
GND	ANALOG	F2
−15	10	E2

NOTE 1. Mounting holes are provided on the module so that input and feedback components can be added. Components shown with dashed lines are not included with the module.

NOTE 2. This jumper comes with the module. It may be removed to suit circuit requirements.

NOTE 3. Pins L & M can be connected together to improve settling time, but parameters such as drift and open loop gain are degraded.

The A207 is an economical Operational Amplifier featuring fast settling time (5 μs to within 10 mv), making it especially suited for use with Analog-to-Digital Converters. The A207 can be used for buffering, scale-changing, offsetting, and other data-conditioning functions required with A/D Converters. All other normal operational amplifier configurations can be achieved with the A207.

The A207 is supplied with a zero balance potentiometer. Provisions are made on the board for the mounting of input and feedback components, including a gain trim potentiometer. The A207 is pin-compatible with the A200 Operational Amplifier.

SPECIFICATIONS—At 25°C, unless noted otherwise.

		Pins L & M Differences with Pins Connected L & M Not Connected
Settling Time*		
Within 10 mV, 10V step input, typ:	3 μsec	6 μsec
Within 10 mV, 10V step input, max:	5 μsec	8 μsec
Within 1 mV, 10V step input, max:	7 μsec	10 μsec
Frequency Response		
Dc open loop gain, 670 ohm load, min:	15,000	100,000
Unity gain, small signal, min:	3 MHz	
Full output voltage, min:	50 kHz	
Slewing rate, min:	3.5v/μsec	
Overload recovery, max:	8 μsec	
Output		
Voltage, max:	±10V	
Current, max:	±15 mA	
Input Voltage		
Input voltage range, max:	±10 V	
Differential voltage, max:	±10 V	
Common mode rejection, min:	10,000	
Input Impedance		
Between inputs, min:	100 k ohms	
Common mode, min:	5 M ohms	
Input Offset		
Avg. voltage drift vs. temp, max:	60 μV/°C	30 μV/°C
Initial current offset, max:	0.5 μA	
Avg. current drift vs. temp, max:	5 nA/°C	
Temperature Range	0°C to +60°C	

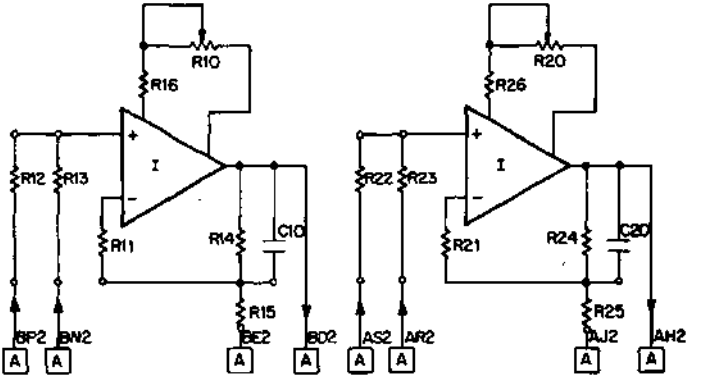
*Gain of 1, inverting or non-inverting configuration.

A260
DUAL AMPLIFIER CARD

AMPLIFIERS

A SERIES

Length: Standard
Height: Double
Width: Double



A = ANALOG SIGNALS (DO NOT CONNECT TO LOGIC LEVELS)

Volts	Power mA (max.)	Pins
+15	20	AD2
GND	ANALOG	AF2
−15	20	AE2

The A260 is a universal dual amplifier card which contains two independent operational amplifiers. Provisions have been made for mounting input and feedback components so that the A260 may be used in a variety of modes.

Some of the configurations in which the A260 may be used are:

1. Voltage follower with a gain of plus one.
2. Voltage follower with positive gain of greater than one.
3. Attenuated follower with positive gain of less than one.
4. Differential amplifier with differential input and single ended output.
5. Inverter with negative gain of one or greater.

The A260 may also be used as the output buffer for the A160 and A164 multiplexer series, as well as the input buffer for the A400 series sample and hold modules. Individual offset adjustments are provided for on each amplifier.

SPECIFICATIONS

Description:	Two differential amplifiers mounted on one board with provision for mounting resistors in a variety of modes.
Offset:	Adjustments provided to adjust offset to zero.

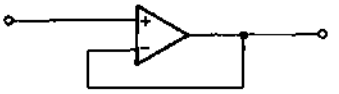
Configurations

A.	Follower	High input impedance, gain of plus one.
	Transfer Accuracy:	±0.01% of FS
	Settling Time (0 to 10v):	1.5 μs to .01%
	Output drive:	20 mA., short circuit proof to ground.
	Input/output range:	±10 Volts
	Input impedance:	1000 megohms
	Temp. Coefficient:	30 μV/°C.
B.	Follower with Gain—	High input impedance, positive gain greater than one.
	Transfer accuracy:	Function of resistors provided.
	Gain:	Determined by $\frac{R14 + R15}{R15}$
	Settling Time:	(Gain) x (1.5 μs) to .01%
	Output Drive:	20 mA. short circuit proof to ground.
	Input/Output range:	±10 Volts
	Input Impedance:	⩾100 megohms
	Temp. Coefficient:	30 μV/° C. (referred to input)
C.	Attenuated follower—	Input attenuator, positive gain less than one.
	Gain:	$\frac{R13}{R12 + R13}$ (see schematic)
	Transfer Accuracy:	Function of resistors provided.
	Settling Time:	1.5μs to .01% if not limited by attenuator.
	Input Range:	0 to ±100 Volts, max.
	Output Range:	±10 Volts

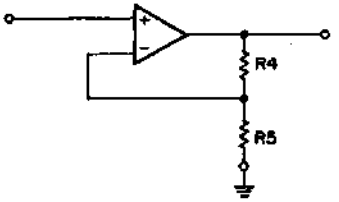
	Output Drive:	20 mA., short circuit proof to ground.
	Input Impedance:	R12 + R13
	Temp. Coefficient:	30 μV/° C. plus input attenuation.
D.	Differential Amplifier:	Differential input, single ended output.
	Gain:	$\frac{R14}{R15}$
	Transfer Accuracy:	Function of resistors provided.
	Settling Time:	(Gain) x (1.5μs)
	Input Voltage (Signal plus common mode):	$(1 + \frac{1}{Gain}) \times$ (10V) max.
	Output Range:	±10 Volts
	Output Drive:	20 mA., short circuit proof to ground.
	Temp. Coefficient:	(30 μV/° C) x (1 + Gain)
	Common Mode Rejection:	Function of resistor matching in each input > 86dB for .01% resistor watch in addition to transfer accuracy of .01%
E.	Inverter	Negative gain of one or greater

Specs same as differential amplifier, except input referenced to ground.

1. FOLLOWER

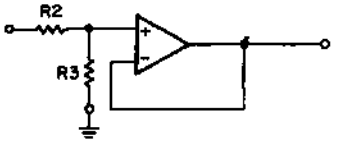


2. PLUS GAIN



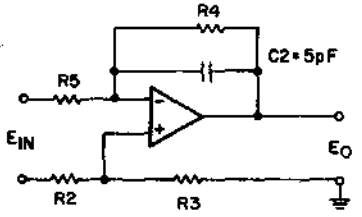
$$\frac{E_O}{E_{IN}} = \frac{R4+R5}{R5}$$

3. POSITIVE GAIN LESS THEN ONE



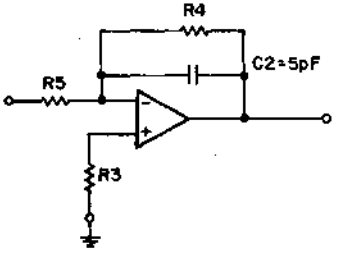
$$\frac{E_O}{E_{IN}} = \frac{R3}{R3+R2}$$

4. DIFF. INPUT



$$\frac{E_O}{E_{IN}} = \frac{R4}{R5}$$

5. INVERTER



$$\frac{E_O}{E_{IN}} = \frac{R3}{R4}$$

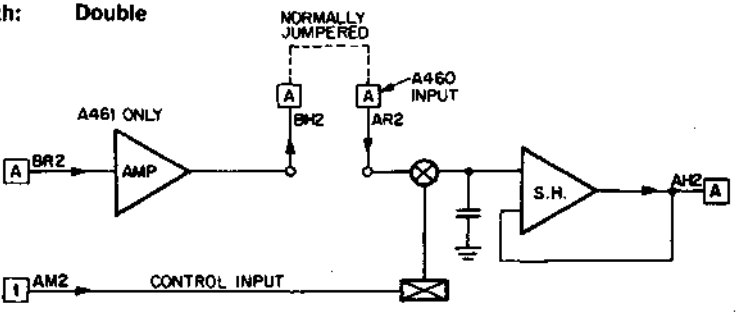
R12 R22	R13 R23	R14 R24	R15 R25
0Ω	∞	0	∞
0Ω	∞	5K G=	5K +2
		9K G=	1K +10
50K G=	50K +1/2	0	∞
20K	20K G=	20K 1	20K
∞	10K G=	20K −1	20K

A460
SAMPLE AND HOLD

SAMPLE & HOLD

A SERIES

Length: Standard
Height: Double
Width: Double



A = ANALOG SIGNALS (DO NOT CONNECT TO LOGIC LEVELS)

Volts	Power mA (max.)	Pins
+15	12, 20*	AD2
GND	ANALOG	AF2
−15	12, 20*	AE2

*with buffer

The A460 is a one-channel sample and hold module used to sample the value of a changing analog signal at a particular point in time and store this information as a stable analog voltage level. The A460 is without input buffering.

Provided on the A460 is a select line which can be used to control the sample or hold operation of the module.

The A460 is DTL and TTL compatible and may be used with standard "M" or "K" Series modules in control and system configurations.

The output circuitry consists of a buffer amplifier with output drive capability of 20 mA. The A460 is compatible with DEC "A" Series high impedance and constant impedance multiplexers and may be used with either to perform various levels of multiplexing.

SPECIFICATIONS

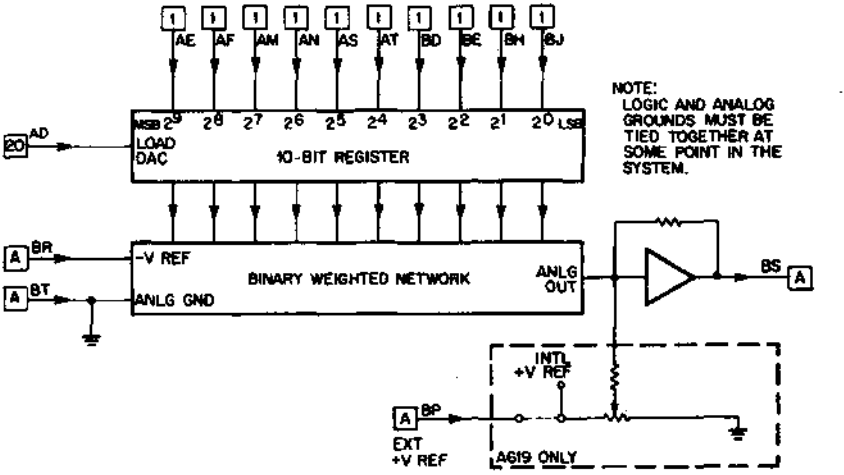
Transfer Accuracy at 23° C.:	±0.01% FS in Hold mode
Input/Output Voltage Range:	±10V Full Scale
Transfer Characteristic:	+1 (non-inverted)
Acquisition Time (to 0.01%):	5 microseconds for −10V to +10V excursion
Aperture Time	Less than 50 nanoseconds
Input Impedance (During Sample Time)—	
(With No Buffer):	100 ohms in series with 0.002 microfarad capacitor
(With Buffer):	1000 megohms in parallel with 10 pF.
Output Drive:	20 mA.
Pedestal in Sample mode:	10 mV max.
Hold Decay:	15 μV per millisecond
Offset:	Adjustable to zero
Temp. Coefficient of Offset:	50 μV per degree C.
Control Input (1 TTL Load)—	
Sample:	Logic Zero
Hold:	Logic One

A619
10-BIT D/A CONVERTER
SINGLE BUFFERED

DIGITAL TO ANALOG

A SERIES

Length: Standard
Height: Double
Width: Double



Power		
Volts	mA (max.)	Pins
+15	25**	BV2
+5	135	AA2
GND	LOGIC	AC2
GND	ANALOG	BT2
−10.05*	60	BR2
−15	35**	BU2
−15	50	AB2

* ref.
** plus output loading

The A619 Digital to Analog Converter (DAC) is double width in the lower (B section) half. The converter is complete with a 10-bit buffer registers, level converters, a precision divider network, and a current summing amplifier capable of driving external loads up to 10 mA. The reference voltage is externally supplied for greatest efficiency and optimum scale factor matching in multi-channel applications.

The A619 DAC output voltage is bi-polar. Binary numbers are represented as shown (right justified) in Table 1:

TABLE 1

Binary Input	Analog Output (Standard) A619
0000_8	−5V
0400_8	−2.5V
1000_8	0 Volts
1400_8	+2.5V
1777_8	+5V

SPECIFICATIONS

OUTPUT:

Voltage: A619	±5 volts
Current:	10 mA. (max)
Impedance:	<0.1 ohm
Settling Time:	
(Full scale step, resistive load)	<5.0 μs
(Full scale step, 1000 pf)	<10.0 μs
Resolution:	1 part in 1024
Linearity:	±0.05% of full scale
Zero Offset:	±5 mV. (max)
Temperature Coefficient:	<0.2 mV/°C
Temperature Range:	0 to 50°C

INPUT

Level: 1 TTL Unit Load	
Pulse: (positive)	
Input loading: 20 TTL Unit load	
Rise and Fall Time:	20 to 100 nsec
Width:	>50 ns
Rate:	10^6 Hz max.

Timing:

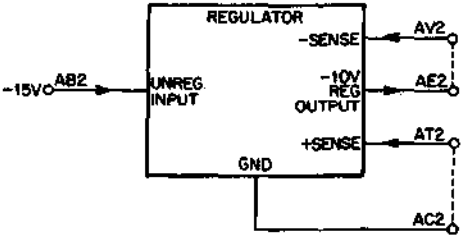
Data lines must be settled 40 ns before the "LOAD DAC" pulse (transition) occurs.

A704
REFERENCE SUPPLY

REFERENCE SOURCES

A SERIES

Length: Standard
Height: Double
Width: Single



Volts	Power mA (max.)	Pins
−15*	250	AB2
GND	ANALOG	AC2

* plus or minus 2 volts

The A704 Reference Supply converts an ordinary −15 volt logic supply voltage into a precisely adjustable regulated −10 volt reference source for A/D and D/A converters of up to 13 binary bits.

FUNCTIONS

Remote Sensing: The input to the regulating circuits of the A704 is connected at sense terminals AT (+) and AV (−). Connection from these points to the load voltage at the most critical location provides maximum regulation at a selected point in a distributed or remote load.

When the sense terminals are connected to the load at a relatively distant location, a capacitor of approximately 100 μF should be connected across the load at the sensing point.

Preloading: The supply may be preloaded to ground or −15 volts to change the amount of current available in either direction. For driving DEC Digital/Analog Converter modules, −125 mA maximum can be obtained by connecting a 270-ohm plus or minus 5%, one-watt resistor from the reference output (pin AE2) to ground (pin AC2).

SPECIFICATIONS

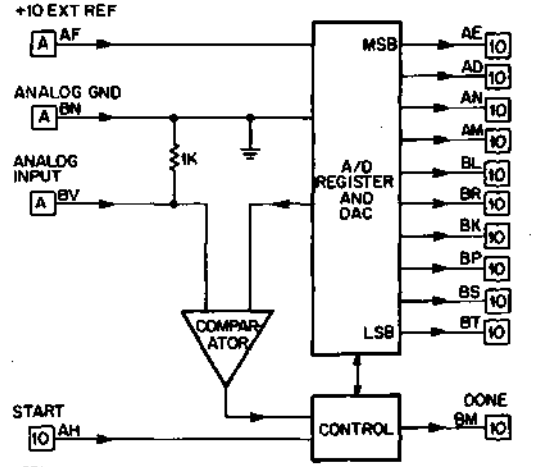
Input Power	−15 V
Use:	See text for sensing and preloading
Output:	−10 V
Current:	−90 to +40 mA
Regulation:	0.1 mV, no load to full load
Temperature Coefficient:	1 mV/8 hrs 1 mV/15 to 35 degrees C 4 mV/0 to 50 degrees C
Peak-to-Peak Ripple:	0.1 mV
Adjustment Resolution:	0.01 mV
Output Impedance:	0.0025 ohms

A811
10-BIT A/D CONVERTER

ANALOG TO DIGITAL

A SERIES

Length: Standard
Height: Double
Width: Double (A Section only)

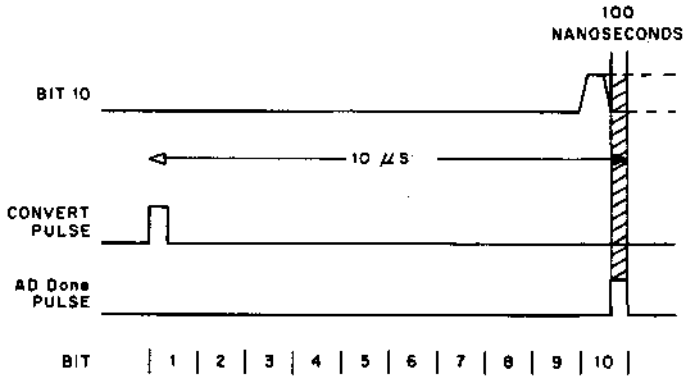


NOTE:
LOGIC AND ANALOG GROUNDS MUST BE TIED TOGETHER AT SOME POINT IN THE SYSTEM.

Volts	Power mA (max.)	Pins
+15*	20	BU2
+5	300	AA2
GND	LOGIC	AC2
GND	ANALOG	BN2
−15*	160	AV2

*Supply voltages must be regulated to within 1%.

The A-811 is a complete, 10-bit successive approximation, analog to digital converter with a built in reference supply. Conversion is initiated by raising the Convert input to logic 1 (+4 volts). The digital result is available at the output within 10 microseconds. An A/D Done Pulse is generated when the result is valid. The A-811 uses monolithic integrated circuits for control logic, output register, and comparator.



Options:
The input impedance of the A/D converter can be raised to greater than 100 megohms by adding an input amplifier module. A sample and hold amplifier module may also be included. The impedance of the converter with sample and hold is 10,000 ohms. Both options may be included simultaneously if high impedance and narrow aperture are both required.

SPECIFICATIONS

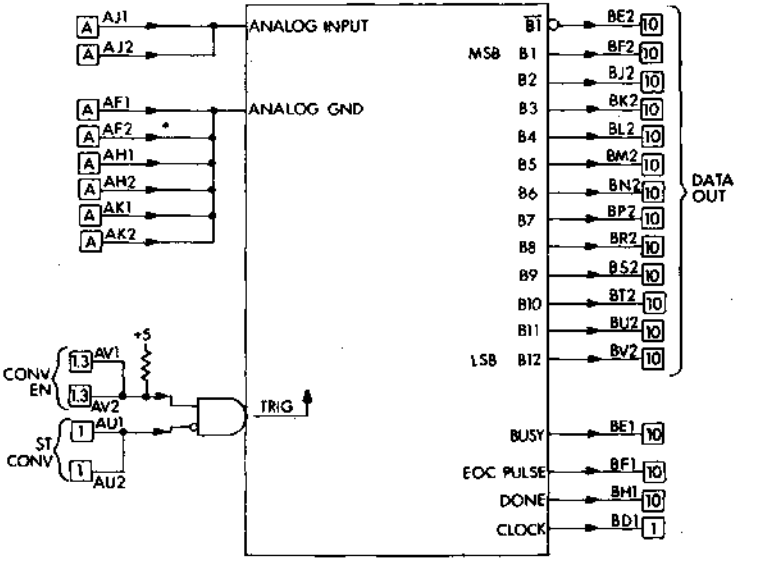
	Max.	Min.
Convert Pulse Input:		
Input loading	10 TTL unit load	
Pulse Width	500 nsec	100 nsec
Pulse Rise Time	250 nsec	—
A/D Done Pulse Output:		
Pulse Width	300 nsec	100 nsec
Digital Output:		
Logical "0"	+0.4V	0V
Logical "1"	+3.6V	+2.4V
Output Current "0"	16 mA	
Output Current "1"	−0.4 mA	
Input:		
Input Voltage	0 to +10V	
Input Impedance	1000 ohms	
Resolution:	10 bits	
Accuracy:	0.1% of full scale	
Temperature:		
Coefficient:	0.5 mV/°C	
Operating Temperature:		
	0°C to 50°C	
Conversion Rate:	100 kHz (max)	
Output Format:	Parallel Binary Uni-polar	

A866
HIGH-SPEED 12-BIT BIPOLAR A/D CONVERTER

ANALOG TO DIGITAL

A SERIES

Length: Standard
Height: Double
Width: Single



Volts	Power mA (nominal)	Pins
+5V±10%	300	AA1, AA2, BA1, BA2
+15V±3%	75	AD1, AD2
−15V±3%	40	AE1, AE2
LOGIC GND		AC1, AC2, AT1, BC1, BC2, BT1

The A866 is a 12-bit general purpose analog-to-digital converter module which uses the successive approximation technique. The A866 is designed to accept unipolar or bipolar single-ended analog voltage as input and convert it to a 12-bit TTL-compatible, coded digital output. The coded digital output is parallel data and is available for application to a computer, terminal, display, or other logic device.

The selection of unipolar or bipolar and voltage range of the analog input is determined by jumper leads mounted on the module circuit board. The module has factory-installed jumpers that permit its use with bipolar, 10-volt full-scale extended-range inputs. By changing the jumper configuration, the user can select bipolar or unipolar, 5-volt or 10-volt full scale extended or nonextended input ranges.

The extended range is particularly useful when the output data is used in computations because the LSB is easily expressed as an integer submultiple of the full scale; i.e., full scale/2000_{10} rather than full scale/2048_{10} for a bipolar configured module and full scale/4000_{10} rather than full scale/4096_{10} for a unipolar configured model. Therefore, less rounding-off error occurs during the computations. In addition, extended range provides some overscale input capability; i.e., +0.2350 Volt and −0.2400 Volt (+10.2350 Volts and −10.2400 Volts full overscale inputs) for a bipolar configured module and +0.2375 Volt (+10.2375 Volts full overscale inputs) for a unipolar configured module. The coded output is 12-bit binary and two's complement using the MSB output and the MSB output respectively.

The A866 can be used wherever fast, accurate analog-to-digital conversions are required.

The high input impedance (100 megohms) at the analog inputs minimizes the signal source loading, and the fast conversion time permits an encoding rate at the output of 16,000 conversions per second.

The digital output data, the output control and status signals, and the input control signals are all TTL-compatible.

APPLICATIONS

The A866 Analog-to-Digital Module is suitable for use in scientific and industrial research applications. It provides fast, accurate analog-to-digital conversion from transducers, bridges, or similar instrumentation.

The A866 Module has factory-installed jumpers that permit its use with bipolar, 10-volt full scale extended range inputs where a change of 5.0 millivolts at the input corresponds to a change of 1 LSB at the output. The A866 Module may be reconfigured with jumpers by the user so that it will accept analog inputs of any of the following:

bipolar ± 10-Volt full scale extended range
bipolar ± 10-Volt full scale nonextended range
bipolar ± 5-Volt full scale extended range
bipolar ± 5-Volt full scale nonextended range
unipolar + 10-Volt full scale extended range
unipolar + 10-Volt full scale nonextended range
unipolar + 5-Volt full scale extended range
unipolar + 5-Volt full scale nonextended range

Table I

Bipolar ± 10 Volt Full Scale, Extended Range
Analog Input Output Code Conversion Chart

Analog Voltage Input	Two's Complement Output Code*		Scale
	Base 10	Base 8	
+10.2350 V	2047	3777	+Full Overscale
+10.2300 V	2046	3776	+Full Overscale — 1 LSB
+10.0000 V	2000	3720	+Full Scale
+ 7.5000 V	1500	2734	+¾ F.S.
+ 5.0000 V	1000	1750	+½ F.S.
+ 2.5000 V	500	0764	+¼ F.S.
+ 0.0050 V	1	0001	+1 LSB
0.0000 V	0	0000	Zero
— 0.0050 V	— 1	7777	—I LSB
— 2.5000 V	— 500	7014	—¼F.S.
— 5.0000 V	—1000	6030	—½ F.S.
— 7.5000 V	—1500	5044	—¾ F.S.
—10.0000 V	—2000	4060	—Full Scale
—10.2350 V	—2047	4001	—Full Overscale — 1 LSB
—10.2400 V	—2048	4000	—Full Overscale

Note: When an A866 module is jumpered to accept ±5 Volt full scale inputs, the inputs are exactly ½ of the input value shown in the above table.

* Using MSB output.

Table II

Bipolar ± 10 Volt Full Scale, Non-extended Range
Analog Input to Output Code Conversion Chart

Analog Voltage Input	Two's Complement Output Code**		Scale
	Base 10	Base 8	
	Not Valid	Not Valid	+Full Scale
+ 9.9951*V	2047	3777	+F.S. — 1 LSB
+ 7.5000 V	1536	3000	+¾ F.S.
+ 5.0000 V	1024	2000	+½
+ 2.5000 V	512	1000	+¼
+ 0.0048*V	1	0001	+1 LSB
0.0000 V	0	0000	Zero
— 0.0048*V	— 1	7777	—1 LSB
— 2.5000 V	— 512	7000	—¼F.S.
— 5.0000 V	—1024	6000	—½ F.S.
— 7.5000 V	—1536	5000	—¾ F.S.
— 9.9951*V	—2047	4001	—F.S. — 1 LSB
—10.0000 V	—2048	4000	—Full Scale

Note: When an A866 module is jumpered to accept ±5 Volt full scale inputs, the inputs are exactly ½ of the input values shown in the above table.

* Rounded off value.
** Using MSB output.

SPECIFICATIONS

Analog Input

Type of Input	Single-ended
Impedance	>100 megohms
Input Bias Current	6 nanoamperes, (max.)
Overvoltage Limit	±18 volts, (max.)
Perturbations	The encoding process does not cause noise at the input

Encoding Process

Technique	Successive approximation
Quantizing Resolution	1 part in 4095 of full range
Encoding Word Time	15 microseconds, max. (includes Op-Amp settling time)
Encoding Word Rate	64,000 conversions/second, min.
Code	Binary and 2's complement (using MSB and complement of MSB)

Measurement Accuracy Uncertainty at 23°C

Warm-up Time	3 minutes
Absolute (Ref. to NBS STDS)	±1 LSB at full scale, max.

Stability

Overall Tempco	±1/20 LSB/°C, max.
Tempco of Clock Period	±0.1 percent/°C, max.
Long Term	±1/2 LSB/6 mos., max.

Sensitivity to Power Supply Voltage Changes

For the ±15 Volt Supply	0.002% % V, max., from dc to 1 MHz
For the ±5 Volt Supply	0.0003% % V, max., from dc to 1 MHz

FUNCTIONS

Analog Inputs

The single-ended dc analog input will accept unipolar or bipolar voltage with a maximum amplitude of 10 V.

Control Inputs

A high to low level change on either of the two ST CONV inputs when the CONV EN input is high or a low to high transition on either of the two CONV EN inputs when the ST CONV input is low will start the conversion process.

Data Outputs

The data outputs are 12 parallel bits plus the complement of B1 (MSB). Bit B12 is the LSB. The output code is available in a binary format when the B1 output is used and in two's complement when B1 output is used. The outputs are TTL-compatible levels.

Status Outputs

Three outputs are provided to indicate the status of the conversion process. The BUSY output becomes high and remains high while the conversion process is active. The BUSY output becomes low 50 ns after the data is available at the output and remains low until the next command to start the conversion.

The DONE output is the complement of the BUSY level.

The EOC PULSE output becomes a high level for 450 ±50 ns after the DONE output level goes high.

The CLOCK output is a series of 50 ns pulses (min.) generated when the A866 Module is performing an analog-to-digital conversion.

Detailed information on the module is available on the A866 A/D Converter Module (12-Bit, 15-Microsecond) data sheet available from the Logic Products Group of DIGITAL.

K SERIES
CONTROL MODULES

Computer-oriented logic, by its very nature, is high speed (1 MHz and above), and provides noise immunity far below that required in a process control environment. The upper frequency range of the K Series modules is 100 KHz, with provision for reduction to 5 KHz for maximum noise immunity. These modules incorporate all silicon diodes, transistors, and integrated circuits, deliberately slowed through the use of descrete components.

Either English (non-inverting) logic or NAND/NOR logic is compatible with K Series. The hardware for this series is specifically designed for standard NEMA enclosures. FLIP CHIP mounting hardware can likewise be used for rack-mounting, inasmuch as K Series modules fit standard DEC sockets.

Proven FLIP CHIP connectors, used for years in applications from steel mills to lathe controls, provide modularity. Even the connection between terminal strips and electronics can be plugged for installing the logic after field wiring is complete, and removing it quickly for modifications or additions.

Checkout and trouble shooting is easy with K Series logic. Wherever possible, every system input and output has an indicator light at its screw terminal. A special test probe provides its own local illumination and built-in indication of transients, as well as steady states. Every point in the system is a test point, and consistent pin assignments reduce the need to consult prints.

Construction materials and methods are the same as for other high-production FLIP CHIP modules, including a computer-controlled operating test of each complete module. K Series modules further offer the size reduction, reliability, flexibility, and low cost of solid state logic, with an added bonus of easy interconnection. FLIP CHIP industrial modules are ideal for interfacing high speed M Series or computer-systems to machinery and processes. Sensing and output circuits can operate at 120 vac for full electromechanical capability. Inputs from contact devices see a moderate reactive load to assure normal contact life. Solid state ac switches are fully protected against false triggering. Voltages from the external environment are excluded from the wire-wrap connections within the logic.

K SERIES SPECIFICATIONS

SUMMARY

Frequency range: DC to 100 KHz. Control points on the modules allow reduction to 5 KHz for maximum noise immunity for critical functions.

Signal levels: 0v and +5v, regardless of fanout used.

Fan-out: 15 ma available from all outputs; typical inputs 1-4 ma.

Waveforms: Trapezoidal. No fast transients to cause cross talk. External capacitive loading affects speed only; no risetime dependence.

Temperature range: −20°C to +65°C, using all-silicon diodes, transistors, and monolithic integrated circuits (0° to 150°F). (Limited to 0°C on the module types: K201, K202, K210, K211, K220, K230).

Noise immunity: False "1":30 ma at 1.6v for 1.5 μsec typical. False "0":3 ma at 3v for 1.5 μsec typical. Time thresholds can be increased by a factor of 20 for critical points by wiring the slowdown control pins.

Simple power requirements: Single voltage supply, +5v ± 10%. Dissipation typically 200 mw per counting or shifting flip-flop, 30 mw per control flip-flop. 10 mw per two-stage diode gate.

Control system voltage: 120 VAC, 50 or 60 hertz.

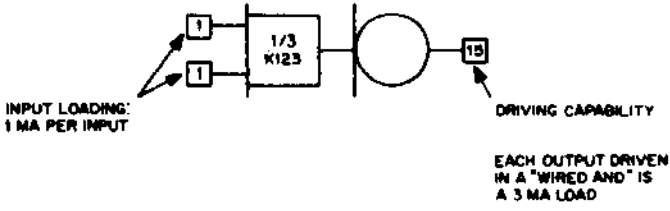
Mounting provisions: Standard NEMA industrial enclosures. May also be used in 19" electronics cabinets.

Logic Signals

There are no ultra-fast transients at any K Series output. Logic signal "1" and "0" levels are essentially independent of fanout. Rise and fall transitions have controlled slopes which are not strongly influenced by normal changes in fanout, lead length, temperature, or repetition rate. The fastest K Series trapezoidal logic signal can be fully analyzed with a 500KC oscilloscope. Logic "1" or "true" is +5 volts and logic "0" or "false" is zero volts except where redefined by logic designer. Counters and shift registers advance at the "1" to "0" transition and are cleared by a "0" level. Any unused input may be left open.

Loading

Input Loading (Fanin)—Each K Series input requires a certain amount of drive to operate, thus imposing a load on the output driving it. The amount of load imposed by an input is defined in terms of the amount of current required to pull that input to ground. Logic gate inputs consume 1 milliampere per input. Other loadings range from 1 to 4 milliamperes as indicated by the loading numbers enclosed in squares on each specification diagram.



FANIN AND FANOUT

Output Loading (Fanout)—Each K Series output is capable of sinking a certain maximum amount of current to ground in the low state. The standard K Series output can sink 15 milliamperes to ground and can therefore handle a maximum of 15 inputs, each requiring 1 milliampere of drive.

If K Series outputs are paralleled to obtain the wired AND logic function, each gate output is effectively driving the other and therefore, each output must be considered as a load on the others. To pull a typical output to ground requires 3 milliamperes of drive. When two or more K Series outputs are tied together, they produce a 3 milliampere load on each other. If, for

example, the outputs of three K123 gates are connected, the combined fanout is reduced by 6 milliamperes, leaving 9 milliamperes of drive capability. A maximum limit of five outputs can be tied together reducing the fanout capability to three milliamperes.

M Series Compatibility

Interfacing M Series with K Series modules requires adherence to all timing constraints of both the input and output devices. As a minimum, M Series signals driving K Series circuits must last long enough (at least 4 μs even if no propagation within the K Series is required) so that the K Series module will not reject it as noise. K Series signals driving M Series circuits must be received by M Series inputs that will not be affected by ultra-slow rise times.

To convert from K Series to M Series, the trapezoidal K Series waveform must be reshaped to provide fast rise times. There are two ways to accomplish this task. The first method is simple, but there are some constraints. When these constraints cannot be complied with, the second method is required.

Method one converts K to M levels simply by connecting the K Series level through two M Series gates. This method is simple and effective; however, the total lead length from the K Series output to the M Series input must be kept less than 6 inches to prevent oscillation of the M Series output as the waveform traverses the unstable areas in the input gate response curve. When the input waveform is in this area, the gate is extremely susceptible to noise. "Slowed" K Series waveforms must not be used. If noise persists in this configuration, an 0.001 microfarad capacitor may be connected from the M Series input to ground.

The second method of converting K Series to M Series levels involves the use of one-shots. The one-shot is triggered by the K Series level transition and provides a pulse of predetermined length to the M Series circuitry. Refer to the M521 K-to-M Converter module description contained elsewhere in this section.

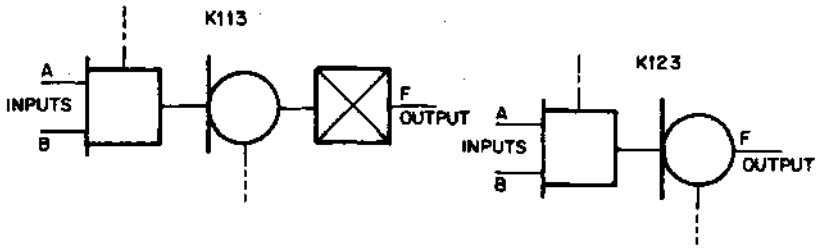
Converting M Series levels to K Series levels is not as complicated. The M671 module contains four M-to-K level converters designed especially for this purpose. (The M671 module is described elsewhere in this section.) The use of the M671 is recommended; however, some K Series inputs can be driven directly, although the capacitive loading will slow the transitions.

K Series modules which cannot be driven directly from M Series gates include K303, K220, K230, K135, K161, as well as the clear inputs to K202, K210, K220, and K230. When driving other K Series gates with M Series signals, care should be taken to ensure that the M Series signal occurs long enough so that the K Series signal will not ignore it as noise.

GATING

K Series gating modules combined with K Series gate expanders provide an extremely versatile method of implementing logic functions. Functions of high complexity can be implemented inexpensively using these gates and expanders.

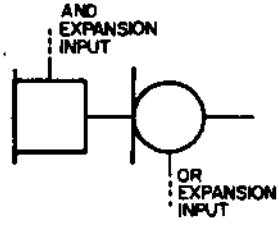
The basic K Series gates are the K113 Inverting gate and the K123 Non-inverting gate.



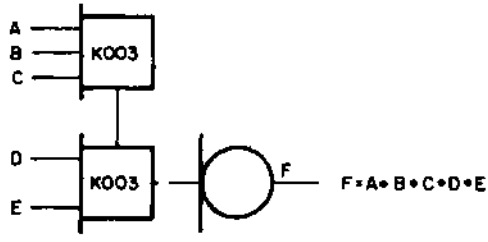
The K113 performs the NAND function
$F = \overline{(A \cdot B)}$

The K123 performs the AND function
$F = (A \cdot B)$

Notice that each basic K Series gate shows two inputs with dotted lines. These are the expansion inputs, which allow functions other than NAND or AND to be implemented.

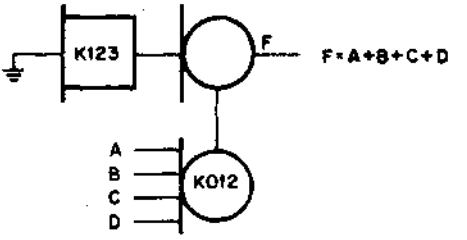


The "AND" expansion input is used with the K003 AND Expander, to provide the AND or NAND function for more than 2 inputs. For example, with one K003 AND Expander connected to a K123 Non-inverting gate we create a five input AND gate.



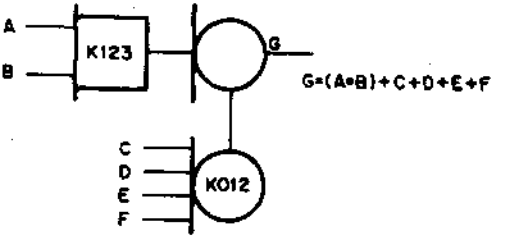
Up to 100 inputs may be connected to the AND Expansion input.

The "OR" expansion input is used with the K026 "AND/OR" expansion gate, or the K028 "AND/OR" expansion gate. Used with the K012, the K123 (or K113) becomes a 4 input "OR" (or Nor) gate.



Up to 9 "OR" inputs can be connected to the OR expansion input.

When the OR expansion input is used, and the AND inputs are also used, the output of the AND gate is "ORed" with the OR expansion input.



The following K Series modules are described in this subsection. Additional information can be obtained by contacting the Logic Products Sales Support Group of DIGITAL, Marlboro, Mass.

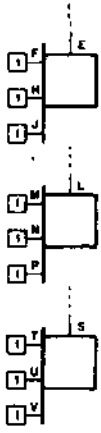
K003 Gate Expanders
K012 Gate Expanders
K026 Gate Expanders
K028 Gate Expanders
K113 Logic Gates
K123 Logic Gates
K124 Logic Gates
K134 Inverters
K135 Inverters
K138 Inverters
K161 Binary to Octal Decoder
K174 Digital Comparator
K201 Flip-Flop
K202 Flip-Flop
K206 Flip-Flop
K207 Flip-Flop
K210 Counter
K211 Programmable Divider
K220 Up/Down Counter
K230 Shift Register
K265 Reed Relay Drivers
K281 Fixed Memory
K282 Diode Memory
K302 Dual Timers
K303 Timer
K323 One-Shots
K501 Schmitt Triggers
K564 DC Input Converters
K579 Isolated AC Input Converters
K580 Dry Contact Filters
K581 Dry Contact Filters
K616 Isolated AC Switches
K657 DC Drivers
K658 DC Driver
K675 5-Digit Display
K681 Lamp Drivers
K683 Lamp Drivers
K716 Interface Block
K724 Interface Shell
K990 Timer Component Board

GATE EXPANDERS

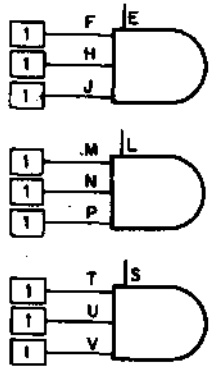
K003, K012, K026, K028

K SERIES

NEMA



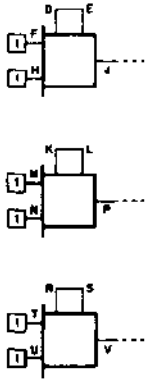
MIL



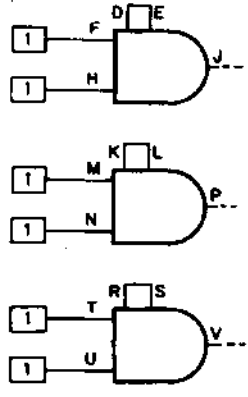
K003

K003 AND expander: May be connected to the AND expansion node of any K Series module.

NEMA

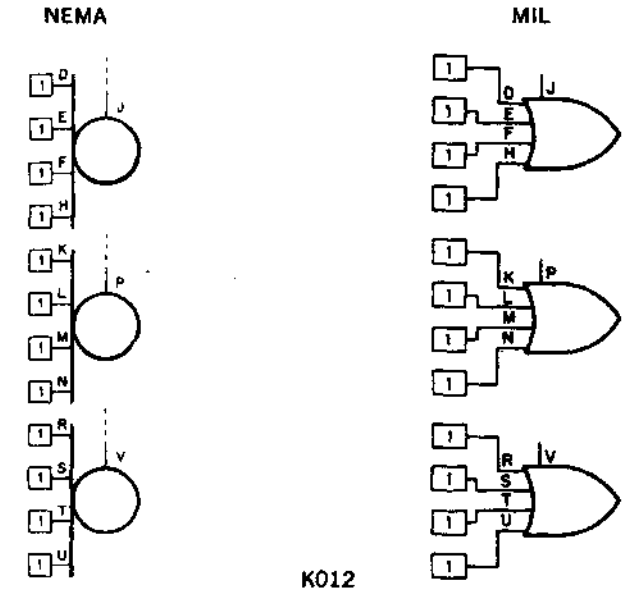


MIL

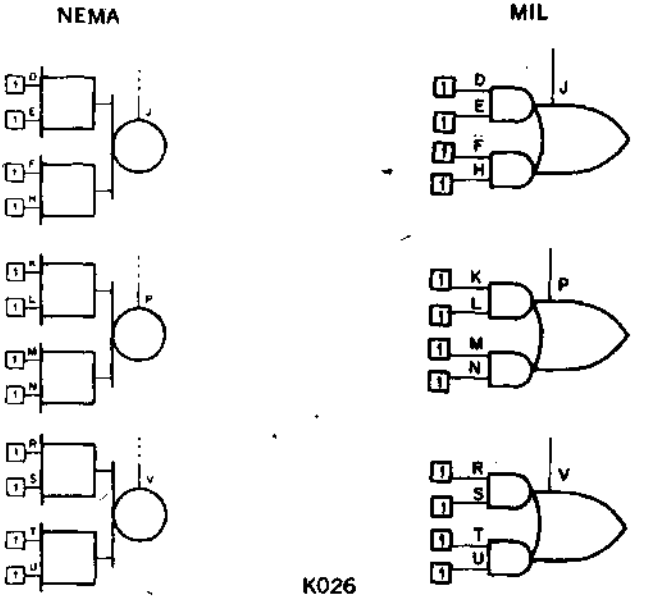


K003

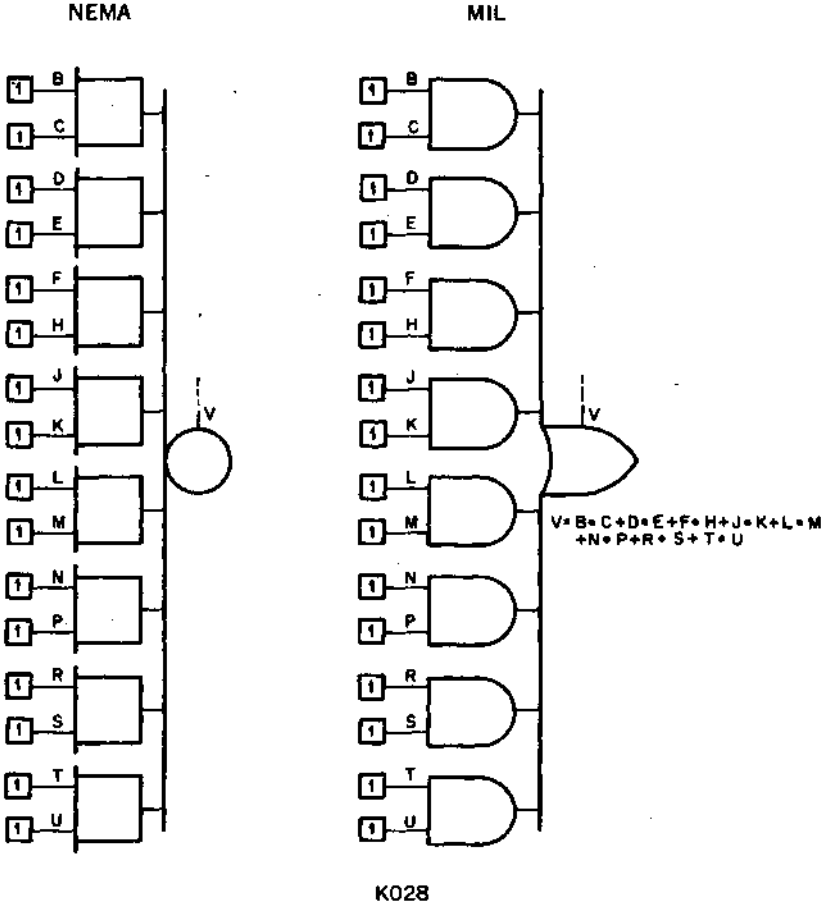
K003 AND/OR expander: May be connected to the OR expansion node of any K Series module.



K012 OR expander: May be connected to the OR expansion node of any K Series module.



K026 AND/OR expander: May be connected to the OR expansion node of any K Series module.



K028

K028 AND/OR expander: May be connected to the OR expansion node of any K Series Gate.

These inexpensive gate expanders offer great logic flexibility and versatility without a proliferation of module types. Logic functions performed by expanders are illustrated in combination with the K113 and K123 gates in several pages that follow the data sheet for the gates themselves.

It must be clearly understood that the gate expanders above are merely expansions for other K Series gates and can never be used as separate AND or OR functions.

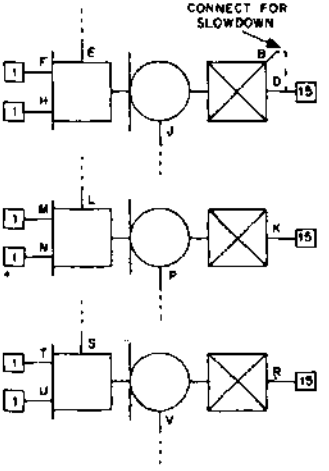
Each K003 expander module has a .01 uf capacitor available at pin B which may be used to implement logic delays or to further reduce the speed of a K Series output.

Caution: Pin C on K028 expanders should not be bussed to ground unless function B-C is not used.

LOGIC GATES
K113, K123, K124

K SERIES

NEMA



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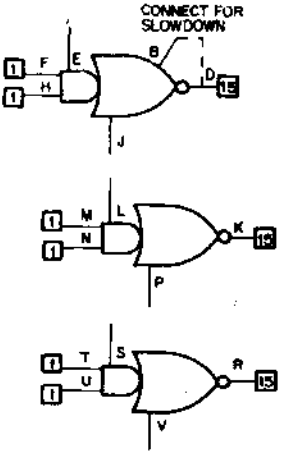
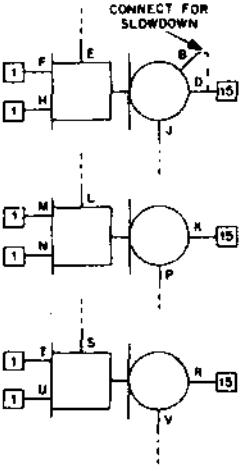


K113
INVERTING GATE

NEMA



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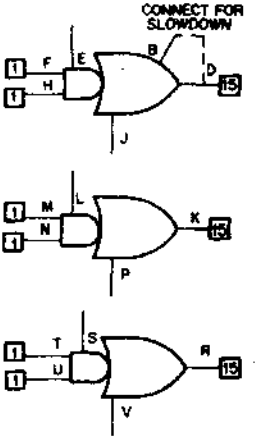
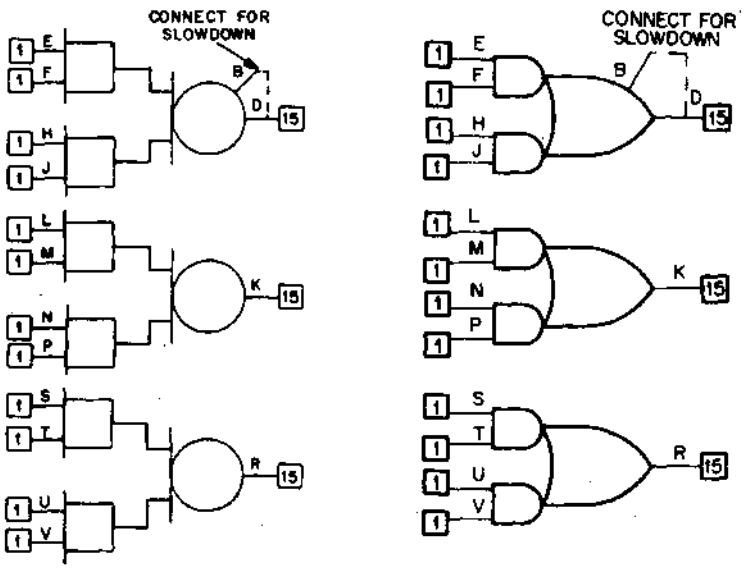


K123
NON-INVERTING GATE



K124
AND/OR GATE

Together with the K003, K012, K026 or K028 expanders, these gates perform any desired logic function, including AND, OR, AND/OR, NAND, NOR, exclusive OR, and wired AND.

Logic gate type K123 is an AND/OR non-inverting gate subject to expansion at either the AND or the OR node.

The AND input can be expanded up to 100 AND inputs total using pins E,L, and S. Up to 9 OR expansion inputs can be connected to the OR expansion pin (J,P,V). More OR expansion inputs can be added if faster fall times are acceptable. Both AND and OR functions can be expanded at the same time.

Expansion of the K113 inverting gate is identical. The equivalent circuit is the same except for inversion in the output amplifier.

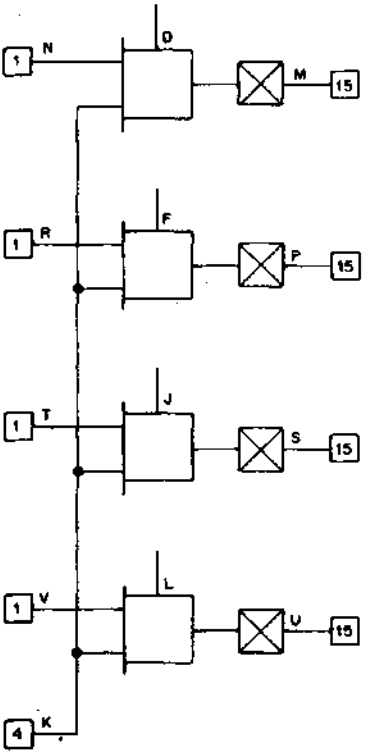
The K124 provides a convenient way to implement non-inverting gate control flip-flops, exclusive ORs, and two term OR logic equations without the need for expanders. The module is electrically the same as a K123 gate with a K003 expander.

Of the three circuits on each module only one has a slowdown capacitor that can be connected to the output to increase noise rejection when the gates are interconnected to make control flip-flops. Use of this capacitor increases rise and fall time by approximately a factor of 20. The maximum speed of each unslowed gate is 100KHz and the maximum speed of a slowed gate is 5KHz.

INVERTERS
K134

K SERIES

NEMA



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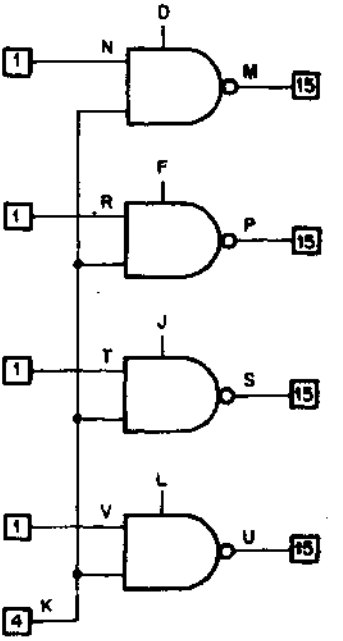


K134 INVERTERS

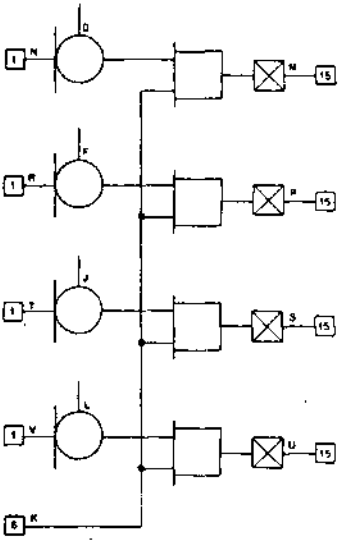
Four flip-flop functional modules such as K210, K220, K230 can conveniently be augmented by a K134 to get "0" as well as "1" outputs. The K134 is also provided with expansion and inhibit inputs for use as the readout element of ready-only memories using K281 diode memories. A common input at pin K can force all four outputs high, a helpful feature for building large K281 memories or very large K161 decoders.

K134 inverters may also be AND expanded by K003 gate expanders, providing an efficient way to obtain 4-input NAND or inverted NOR gates.

INVERTERS
K135

K SERIES

NEMA



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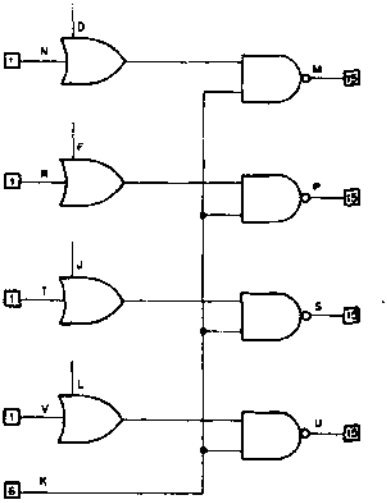


K135 INVERTERS

The K135 module was designed primarily for use in applications that require inverters with "OR" expandability. A common input at pin K can force all four outputs high regardless of the "OR" gate inputs. This feature is useful if a K161 decoder is used for multiplexing K135 modules, since all outputs for the same bit can be wire "AND"ed together.

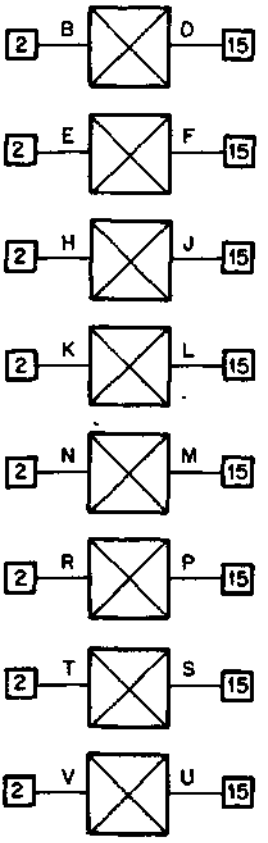
The loading on pin K is initially 6 with no "OR" expansions and increases by "1" unit load for each "OR" input that is added to the module. For example, if a K012 expander was added to each of the four inverters, the total pin K load would be 22 unit loads.

K003 expanders can be used for AND/OR expandability. The number of AND inputs on a given OR input does not affect the loading of pin K.

INVERTERS
K138

K SERIES

NEMA



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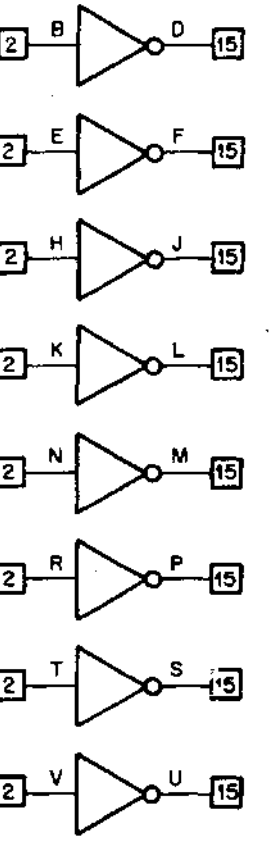
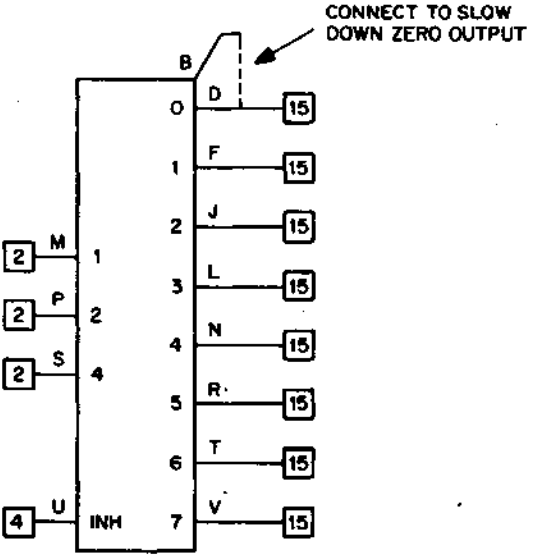


The K138 has eight inverter circuits on each module. These circuits can be used to invert other K Series outputs to obtain both a high (+5V) level as well as a low (0v) level. The K138 is pin compatible with the K134 and K135 and may be substituted for them if a higher density of inverters is desired.

BINARY TO OCTAL DECODER

K161

K SERIES



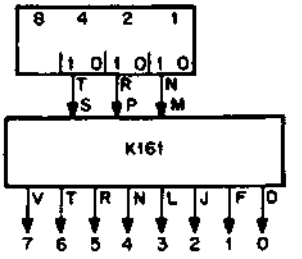
K161 DECODER

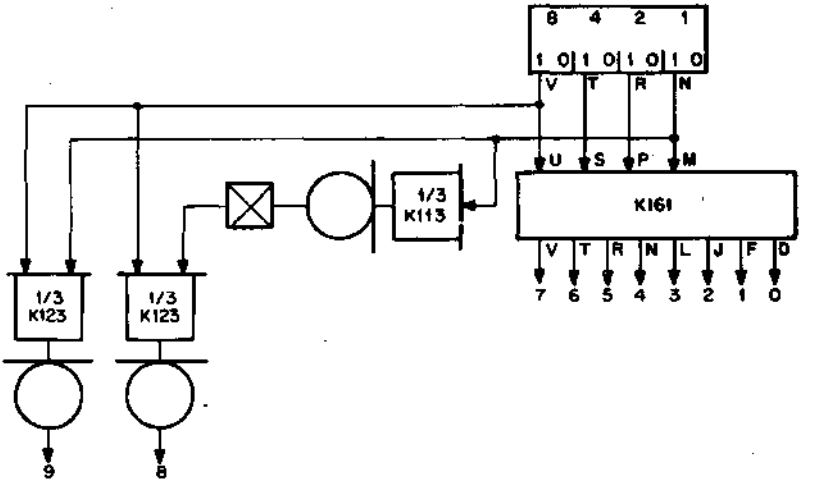
Three-bit binary numbers at the input to the K161 will be decoded into eight one-at-a-time outputs. Both inputs and outputs are high for assertion. The inhibit input allows BCD to ten line decoders to be built, or permits several decoders to be interconnected for sixteen, twenty-four, thirty-two outputs, etc. The inhibit may be left open if unused, even though high is the inhibit state. When the K161 is being used with M series, all input signals must be buffered with K series gates. This is necessary due to the 3 volt thresholds in the K161.

Standard K Series slowdown circuits on each output minimize and for most purposes nullify the splinter pulses that all decoders emit during input transitions. Additional slowdown available on the zero output can usually suppress the larger splinter that may occur there. But since splinter size is ultimately determined by input timing tolerances, it is cleanest to avoid logic designs in which a decoder output is used as a source of pulses.

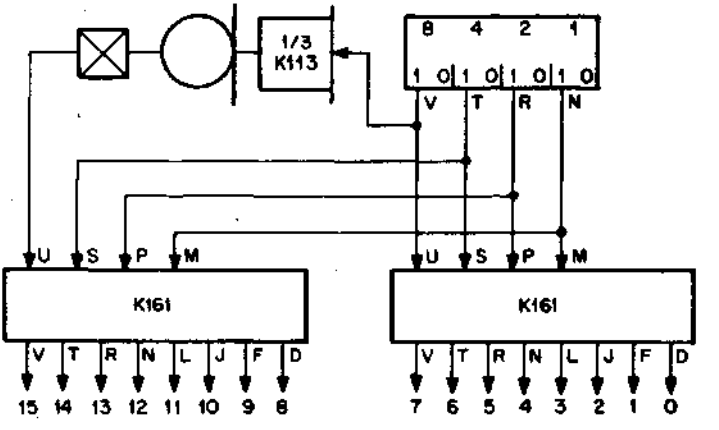
The diagrams below show how to connect decoders for 8, 10, 16 and 32 outputs. Much larger decoders are possible, and in fact up to 256 outputs or even more can be obtained by inhibiting all but one of several decoders.

8 STATE DECODER

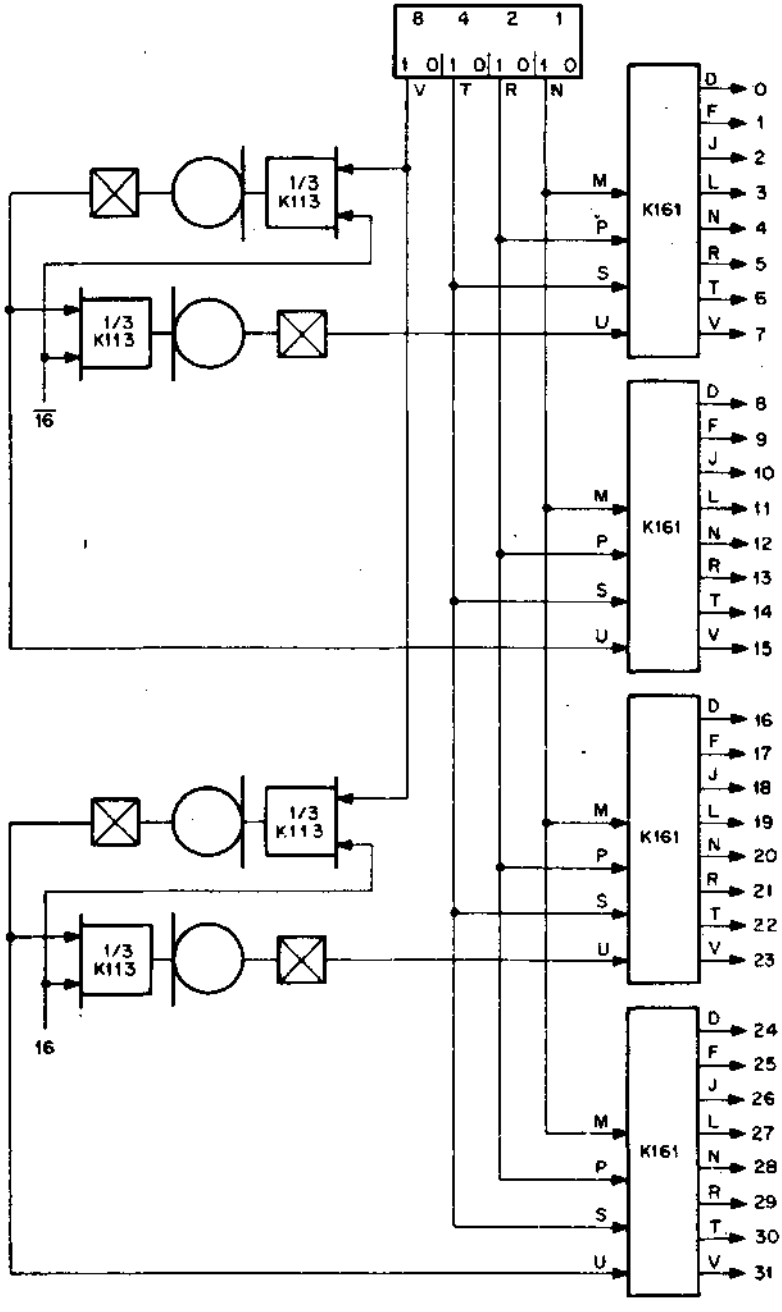




BINARY-CODED-DECIMAL (BCD) DECODER



16 STATE DECODER

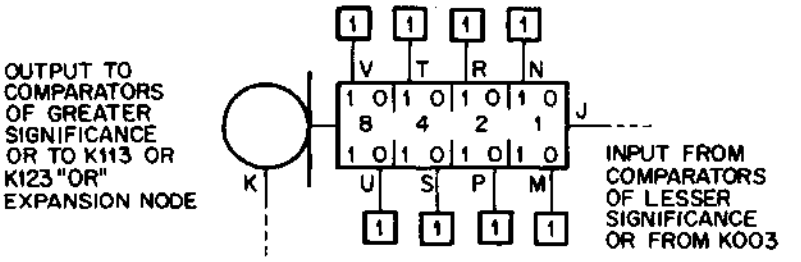


32 STATE DECODER

DIGITAL COMPARATOR
K174

K SERIES

NEMA



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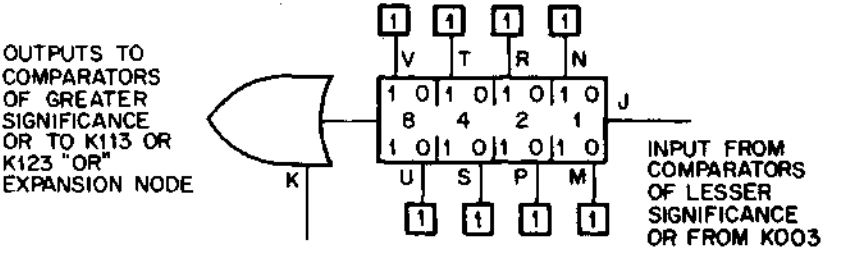


K174 DIGITAL COMPARATOR

Numerical comparisons such as those required in digital positioning controls are facilitated by the K174. Performing the same function as the comparator in closed-loop analog systems, the K174 tells which of two quantities is larger.

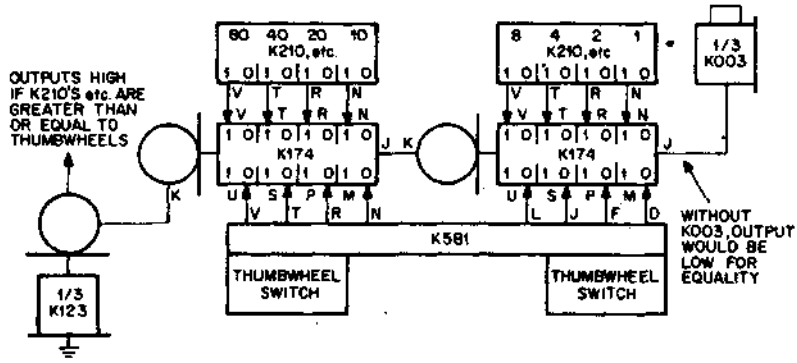
Fundamentally, the K174 performs a subtraction to determine whether a "borrow" would be needed to obtain a positive result. The magnitude of the difference is not available; only the sign.

Note in the example below that the output on pin K will be low only if the magnitude of the number in the K210's is less than the thumbwheels.

If more than four bits are to be compared, several comparators may be cascaded as shown below. Note use of K003 as if expanding an "OR" to control the state of the output for the case of equal input numbers.

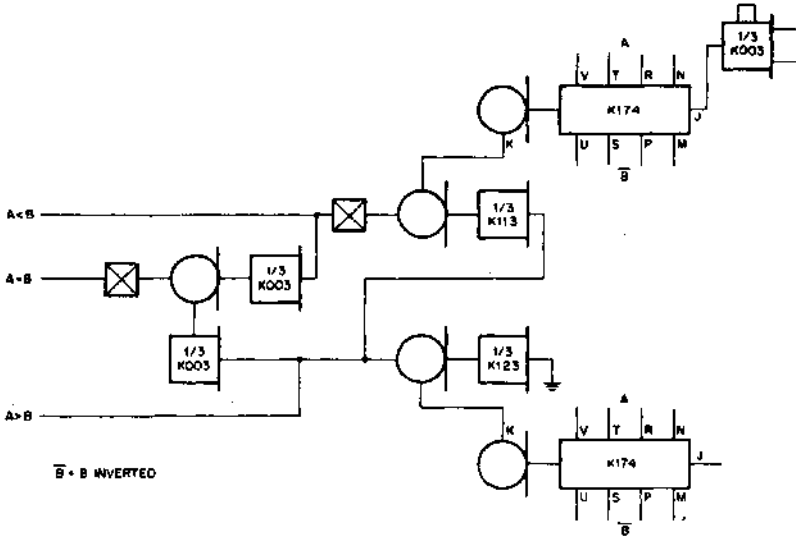
The output at Pin K would normally be low for equality without the K003 connected to Pin J, but with it connected, Pin K is high for equality as shown below.

TWO DIGIT COMPARISON OF THUMBWHEELS AGAINST K210, ETC.



If the numbers being compared are not multiples of 4 bits then one of the inputs on each unused comparitor position must be connected to +5 and the other one to the ground.

The K174 can also be used to obtain three independent outputs for full greater-than, equal-to, less-than capability. The application below takes advantage of the fact that if A is equal to B, K will go high if J goes high and K will go low if J goes low.

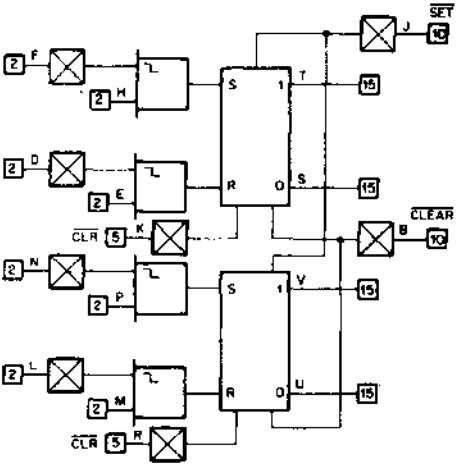


In certain applications, it is possible to make a single K174 oscillate if A=B. This is done by inverting the output at pin K and feeding it back to pin J.

FLIP-FLOP
K201

K SERIES

NEMA



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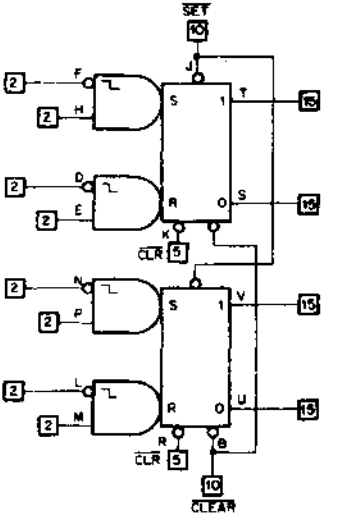


This superslow memory simplifies sequencing of machine motions, and finds other applications where the ultimate in noise isolation is needed and speed is no problem. Its 1 KHz maximum repetition rate makes this flip-flop noticeably more resistant to extremely noisy surroundings than faster types like K202, K210, etc. So noise immune, in fact, that several yards of wire may be connected to K201 outputs even in severely noisy areas without errors.

The K201 flip-flop input gating is designed to respond to the time sequence of two inputs rather than to their simple AND function. Level inputs E, H, M, and P must be high at least 400 µs before the pulse inputs D, F, L, and N make a high to low transition. The flip-flop will compliment if the S and R inputs are pulsed at the same time. The input minimum noise rejecting time thresholds are 100 µs. Successive input transitions must not be closer than 400 µs.

Grounding pin J causes pins T and V to go high and pins S and U to go low, regardless of the state of any other input except clear inputs.

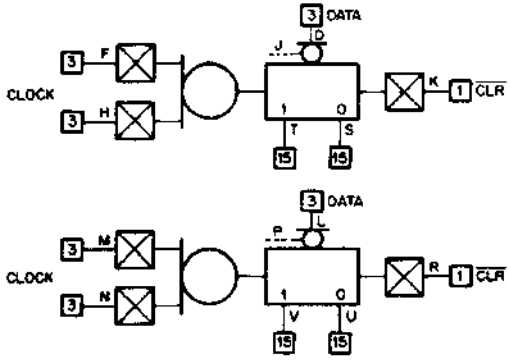
Each flip-flop circuit on this module has a separate clear input (pin K and R). If either of these inputs is grounded the ZERO output of that specific flip-flop will go high and the ONE output will go low unless the set input is grounded.

There is also a common clear, Pin B, which when grounded, forces pins S and U high and pins T and V low, except when pin J is grounded.
If any clear input and the SET input pin J are grounded at the same time, the outputs will be undefined.

FLIP-FLOP
K202

K SERIES

NEMA



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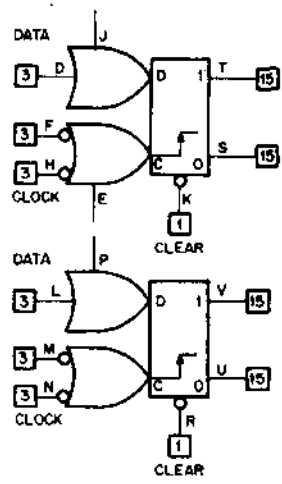


K202 flip-flops do shifting, complementing, counting, and other functions beyond the capabilities of simple set-reset flip-flops built up from logic gates. They also may be used to extend K210 counters or K230 shift registers.

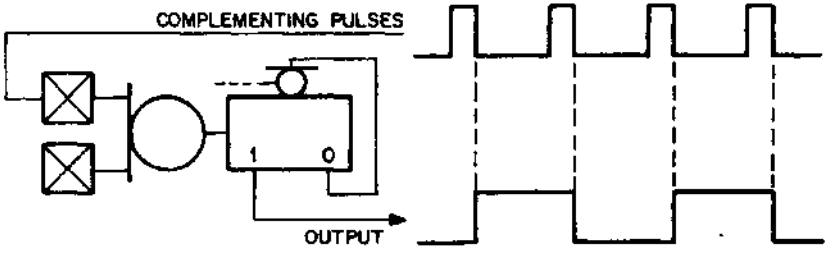
When the output of the clock gate falls from high to low, the information at the OR input (pins D-J, L-P) is transferred into the flip-flop. Pin J (or P) is ORed with the pin D (or L) input. Like pins J and P of a logic gate, these pins can be driven only from a K003, K012, K028, or K026 expander.

Time is required for flip-flops and delayed inputs to adjust to new signals. The clock gate output must not fall to zero sooner than 4 μsec after its own rise, the end of a clear signal, or a change on associated data input pins.

A K202 flip-flop is cleared by grounding the clear input pin. The flip-flop is held in the zero state as long as the clear input is zero volts, regardless of other inputs.

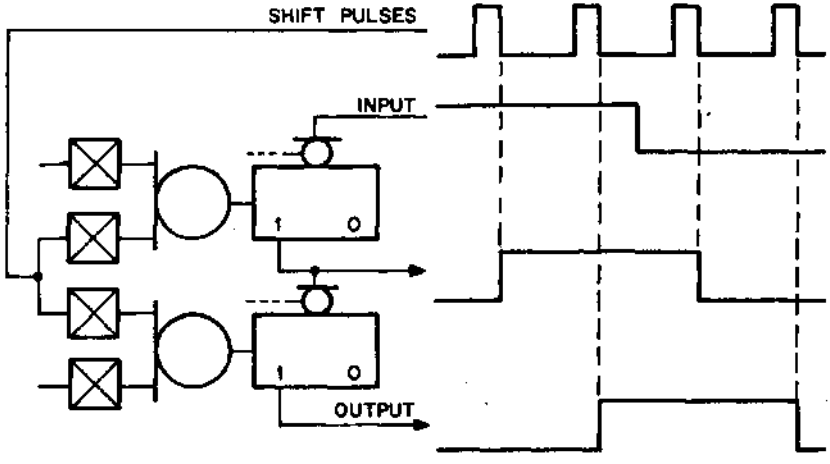
When using a K202 flip-flop to extend the length of a K230 shift register, pins B on both modules must be left open (unslowed). Pin B slows the clock inputs of the K202 for complementing correctly at slow speeds in very noisy surroundings; but the data inputs are not affected by pin B.

Complementing: Below is shown a complementing application. Here the information stored at the data input is the opposite of the flip-flop's present state. Each time the clock gate output changes from "1" to "0", the opposite of the current state is read in.



K202 COMPLEMENTING

Shift Register: The diagram below shows two flip-flops connected as a two-stage shift register. At each step the incoming signal, whether high or low, is set into the first stage of the register, and the original content of the first stage is set into the second stage. The input to each flip-flop must be stable for at least 4 microseconds before another shift pulse occurs, for reliable shifting.



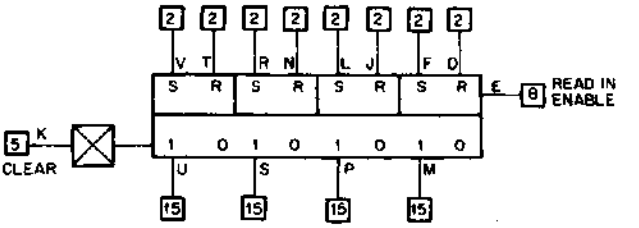
K202 2-STAGE SHIFT REGISTER

Note: In older systems of logic, most flip-flop functions had to be performed by general-purpose flip-flops like the K202. The K Series, however, includes functional types K210, K211, K220, and K230 which are both less expensive and easier to use than the K202 for most applications. Think of the K202 primarily as a complementing control flip-flop and register extender.

FLIP-FLOP REGISTER
K206

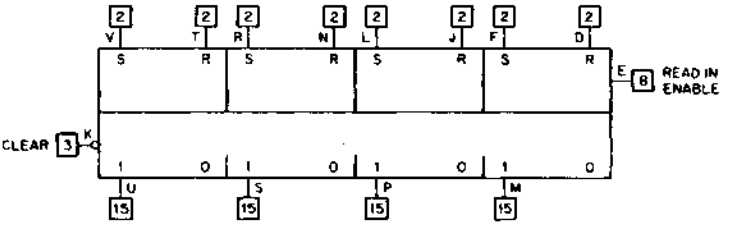
K SERIES

NEMA



K206 FLIP-FLOP REGISTER

MIL



K206 FLIP-FLOP REGISTER

The four set-reset flip-flops in the K206 are arranged for convenient addressing from the outputs of a K161 Binary to Octal Decoder. The flip-flop outputs can then be wired to control and maintain the state of corresponding output drivers, providing addressable output conditioning from teletypes, computers, or fixed-memory sequence controllers.

In addition, the same decoder may be used to address a particular K578 input sampler by grounding the K206 enable input when flip-flop changes are not desired. Pin E enable fanin on the K206 is reduced to 2 milliamperes when K161 addressing is used.

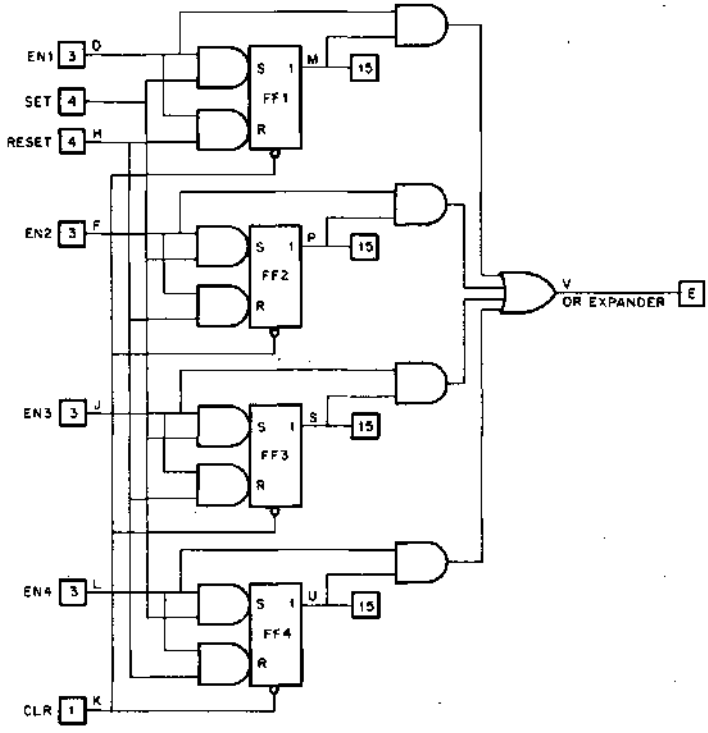
Since most control systems have about half as many digital outputs as inputs, it is convenient to use the least significant bit of the K161 address to determine which flip-flop state is wanted. Odd addresses allow for setting; even addresses, resetting. All flip-flops may be reset together by grounding the clear input, pin K. This clear input takes precedence over all other inputs.

When pin E is high, a logic "1" at an S input will set the output to a logic "1" and a logic "1" at an R input will reset the output to a logic "0." S and R inputs should not be allowed to go high at the same time while the flip-flop is enabled. Any one or all flip-flops may be changed when pin E is high.

FLIP-FLOPS
K207

K SERIES

MIL



The K207 is a 4-bit, set/reset, flip-flop buffer which can be used to manipulate or store data. The module has common set and reset lines with an enable input for each stage. Each stage may be set or reset independently with the use of the enable line.

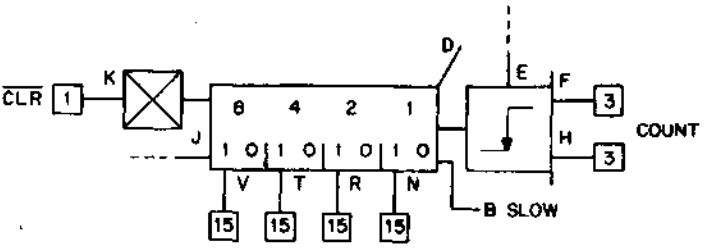
To set a flip-flop, its enable input (pins D, F, J, L) must be at +5 V and the common set input must be brought to +5 V for at least 5 μs. To reset a flip-flop, the enable pin must be at +5 V and the common reset line brought to +5 V for 5 μs. The K207 has a common clear line which, when brought to 0 V, will clear all the flip-flops in the buffer.

The K207 contains an output expander network which allows the state of each stage to be examined. The selected flip-flop will cause an output at pin V if it is set. Pin V must be connected to the OR expander node of any K-series module. To read a stage, the enable for that stage must be at +5 V. If the stage is set, a logic 1 will be presented to pin V.

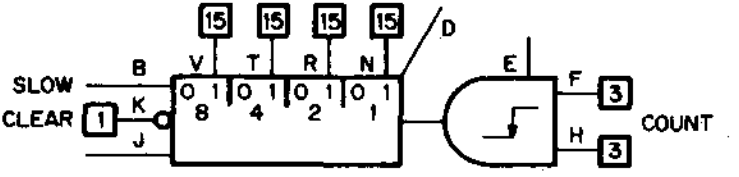
COUNTER
K210

K SERIES

NEMA



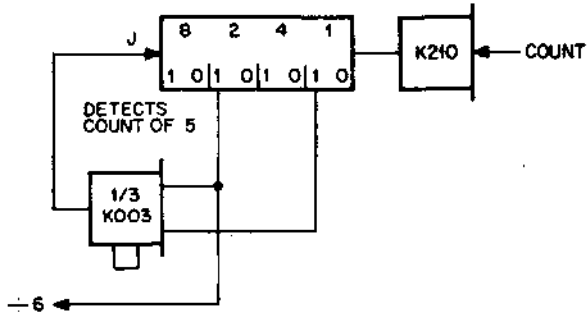
MIL



The K210 is a binary or BCD counter that can be wired to return to zero after any number of input cycles from 2 to 6. Count-up occurs when the COUNT gate output steps to zero. Decimal counting logic is built in; when pin D is unused, the counter resets to zero on the next count after nine. When pin D is grounded, the counter overflows to zero, after a count of 15. (Pin D is not intended for dynamic switching between binary and BCD counting.)

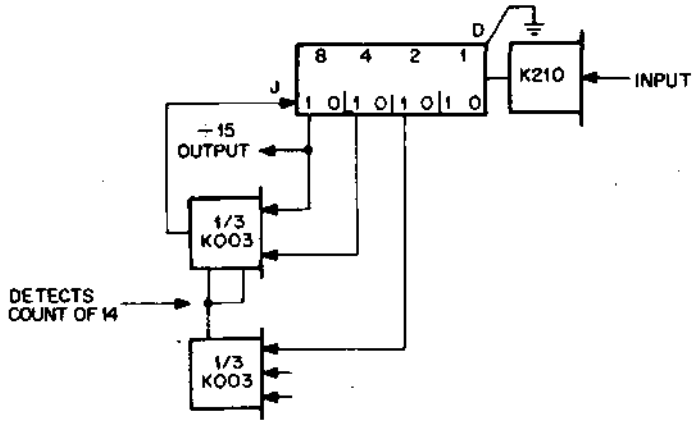
The counter is reset by grounding the clear input for 4 microseconds or more. A positive level at the J input from a K003 expander also resets the counter on the next high to low transition of the COUNT gate output. Counts of 10 or 16 DO NOT require the use of a K003 expander since they can be obtained with pin D.

Wire the K003 as a decoder to detect one count less than the desired modulus. (Detect 5 for a count-of-6 counter, etc.). Use the K424 Thumbwheel Decoder if manual reset control is desired.



K210 CONNECTED FOR COUNT OF 6

To count above 10, ground pin D. Combine two K003 expanders as shown below, where three counter outputs must be sensed (to divide by 8, 12, 14 or 15).

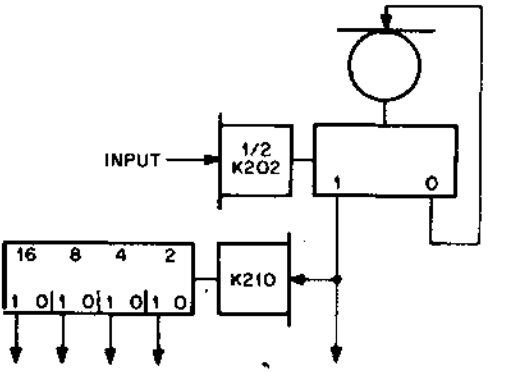


K210 CONNECTED FOR COUNT OF 15

Time is required for flip-flops and pin J reset logic to adjust to new inputs. The count gate output must not step to zero sooner than 4.0 μsec after its own rise, a change at pin J, or the end of a clearing signal at pin K. **When pin B is grounded for slowdown, allow 50 μsec.**

Larger counters are obtained by cascading K210's or adding K202 flip-flops. To cascade K210 modules, wire the most significant output of one counter to the input gate of the next. Inputs to the least significant stage can be either pulses or logic transition to ground; risetime is not important.

Any transducer such as a switch, photocell, pulse tachometer, or thermistor probe, can generate the signal which is to be counted. The lack of input risetime restrictions may allow transducer outputs to drive K210 counters directly if damaging transients can be avoided, as when the transducer shares the logic system environment.

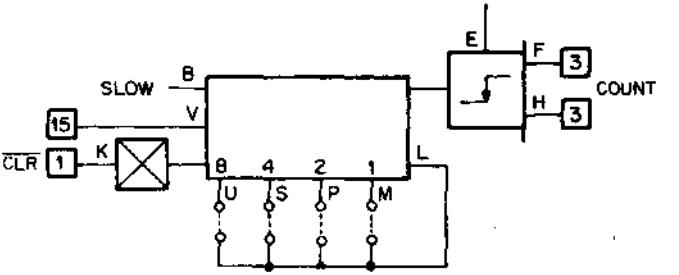


K210 AUGMENTED WITH K202 FOR COUNT OF 32

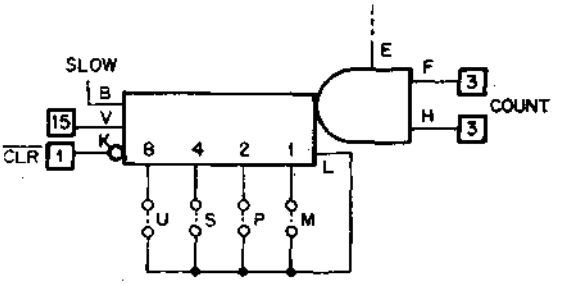
PROGRAMABLE DIVIDER
K211

K SERIES

NEMA

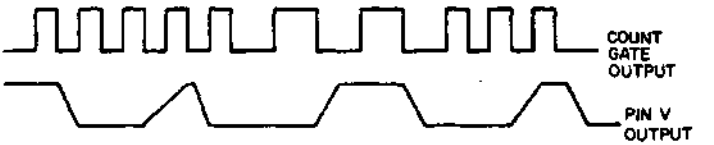


MIL



The K211 is a binary counter that can be wired to produce a high to low output transition on pin V after any number of input cycles from 2 to 16. Count-up occurs on the high to low transition of the count gate output.

The counter is programmed by connecting pin L to pins M,P,S, and U to select the binary number that is one count less than the desired modulus. (Detect 2 for a count-of-3 counter, etc).



Modulo 3 counter

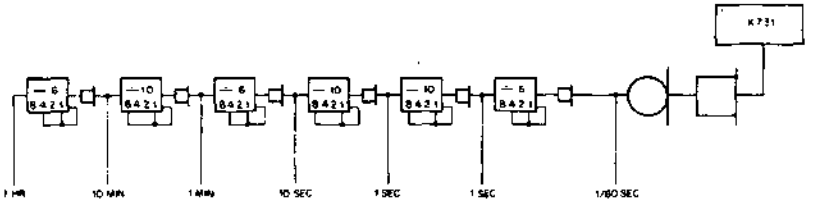
Pin L is connected to pin P only.

The counter is reset by grounding pin K for 4 microseconds or more.

Time is required for flip-flops to adjust to new inputs. The count gate output must not step to zero sooner than 4.0 μsec after its own rise or at the end of a clearing signal at pin K. When pin B is grounded for slowdown, allow 50 μsec.

Larger dividers can be obtained by cascading K210's, K211's or adding K202 flip-flops. To cascade K211 modules, wire pin V to the input gate of the next module. Inputs to the least significant stage can be either pulses or logic transitions to ground; risetime is not important. Any transducer such as a switch, photocell, pulse tachometer, or thermistor probe, can generate the signal which is to be counted. The lack of input risetime restrictions may allow transducer outputs to drive K211 modules directly if damaging transients can be avoided, as when the transducer shares the logic system environment.

K211 modules can be used to build real time clocks and frequency dividers when only the most significant output is required.

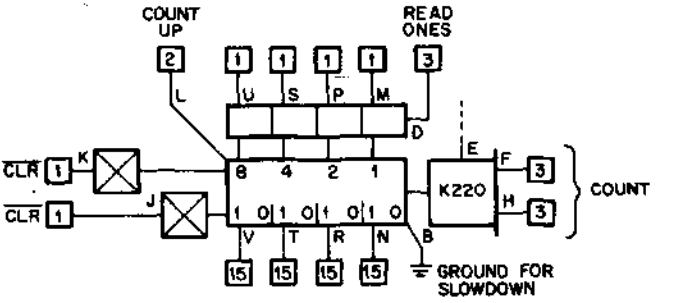


REAL TIME CLOCK

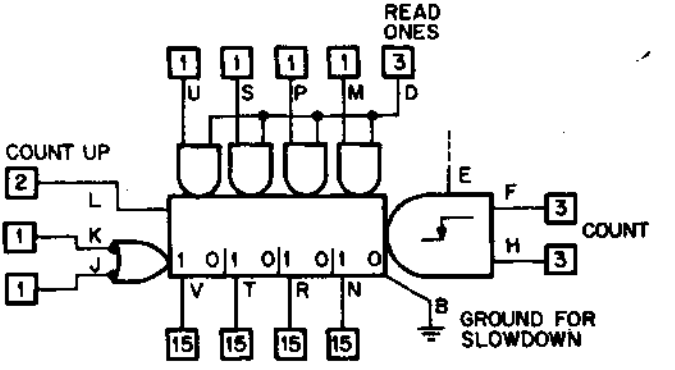
UP/DOWN COUNTER
K220

K SERIES

NEMA



MIL



(DOUBLE HEIGHT BOARD)

The K220 Counter module provides all the circuitry necessary for binary and binary coded decimal up counting, down counting, presetting and clearing. This module is useful in many digital position readout and feedback applications.

The K220 is a double height module with all but two pin connections made on the upper connector (pins D and E on the lower connector must be grounded for binary UP/DOWN counting).

The direction of counting is established by the signal at pin L, high for up counting and low for down counting. Pin L count direction changes should finish no later than 4.0 μsec. before the next count input. Up counts occur when the count (AND) gate output makes a transition from high to low (+5v to 0v). Down counts take place on the count gates output transition from low to high (0v to 5v).

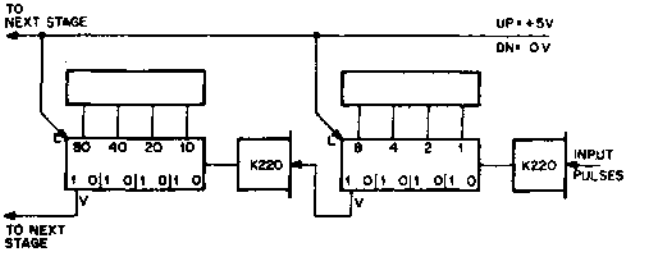
To preset the outputs of a K220, four read-in flip-flops with a common enable have been provided in the circuit. High logic levels (+5v) present at the read-in gate pins (U,S,P, or M) are read into their respective flip-flops when the common enable pin D, makes a low to high transition (0v to 5v). These preset flip-flops will not read low levels (0v) into the K220. All unused read-in gate inputs should be grounded to prevent the read-in of undesired ONE's.

The K220 outputs can be cleared to zero by grounding pin J or K. During this clearing process, no count or preset input can be read into the module; clearing inputs take precedence over all others.

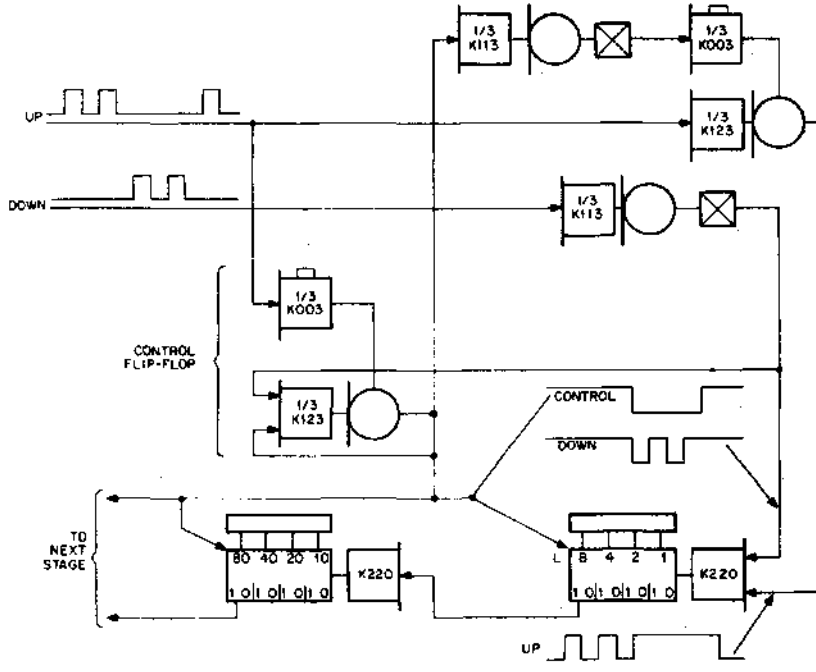
With the exception of the clear inputs, time is required for flip-flops, counting logic, and read-in gates to adjust to new inputs. To prevent counting errors, neither the count gate output nor any other counter input should change within 4.0 microseconds of a transition at any other input.

For slowdown operation, pin B of the K220 must be grounded. If slowdown is used, 50 microseconds must be allowed between one counter input transition and an input transition at any other input.

When K220 counters are cascaded, a single connection from pin V of one K220 to the count input gate of the next, establishes both carry and borrow propagation.

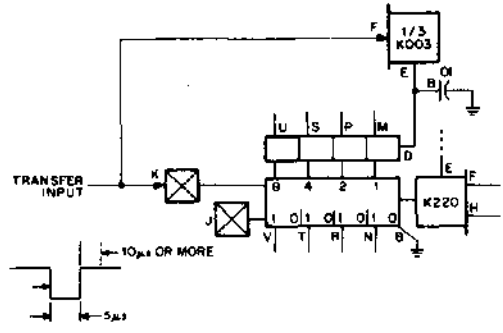


Shown below is a means of acception up and down pulse-trains from two separate sources. For this application, input pulse spacing should be at least 20 microseconds and input pulse widths should be at least 10 microseconds.



UP/DOWN COUNTER
FOR SEPARATE PULSE SOURCES TO 50Kc

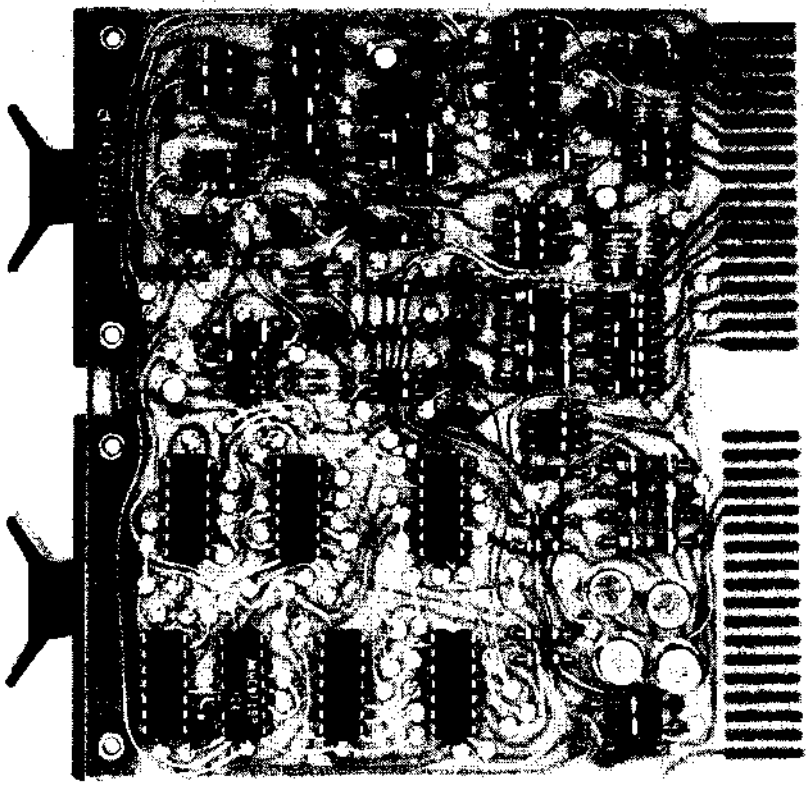
The "clear" and "read ones" inputs on the K220 module may be combined to transfer completely new data into the module in a single operation. Timing requirements in the K220 demand that a low to high transition on the "read ones" (PIN B) input wait until at least 4 microseconds after the clear input rises. A simple method of accomplishing this delay follows.



This circuit gives approximately 10 microseconds of rise delay. The delay may be reduced to about 5 microseconds if desired, by connection another one milliampere pull-up (pin D to pin E on the K003).

Several "read ones" inputs may be driven from a single K003 section, provided the capacitance is multiplied by the number of inputs driven. Heavy capactive loading may cause slow falltimes on the transfer input line. Pin D inputs on the K220 may be regarded as 1 milliampere loads in this application.

The transfer input rise time must be from an unslowed K Series output. Slow signals from K580, K581 or K578 modules must be accelerated by a K501, Schmitt Trigger.

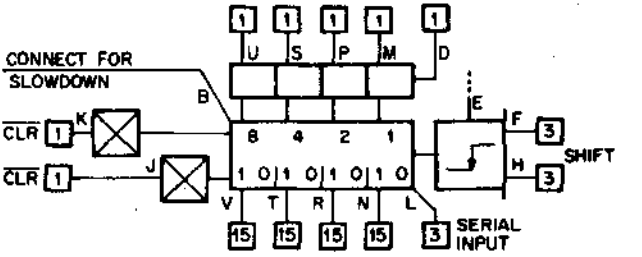


K220 UP/DOWN COUNTER

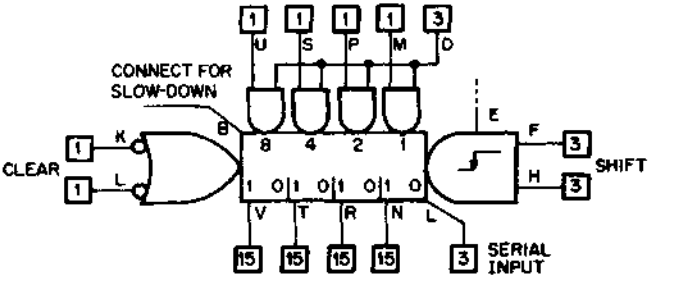
SHIFT REGISTER
K230

K SERIES

NEMA



MIL



(DOUBLE HEIGHT BOARD)

Information presented at pin L of this four stage flip-flop register is shifted toward pin V with each high to low transition (5v to 0v) at the shift input gate.

To preset the outputs of a K230, four read-in flip-flops with a common enable have been provided in the circuit. High logic levels (+5v) present at the read-in gate pins (U,S,P, or M) are read into their respective flip-flops when the common enable pin D, makes a low to high transition (0v to 5v). These preset flip-flops will not read low logic levels (0v) into the K230. All unused read-in gate inputs should be grounded to prevent the read-in of undesired ONE's.

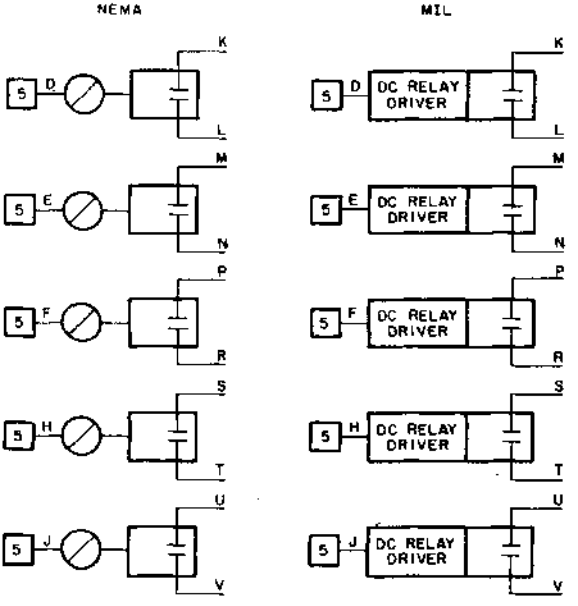
The K230 outputs can be cleared to zero by grounding pin J or K. During this clearing process, no count or preset input can be read into the module; clearing inputs take precedence over all others.

Shift registers of any length can be formed by tying pin V of one K230 to pin L of the next, and operating all shift gates together. Supply all shift pulses from the same device to maintain synchronism. The propagation delay of even one gate is too large a difference between two shift inputs on the same register. For every 20 bits that are required, duplicate the last stage of the shift-generating logic and tie the outputs in parallel to all K230 shift gate inputs.

Time is required for flip-flops, shifting logic, or read-in gates to adjust to new inputs. Except clear inputs, neither the shift gate output nor any other register input may be changed within 4 μsec. after a transition at any other input. When pin B is grounded for slowdown, allow 50 μsec.

K265
REED RELAY DRIVERS

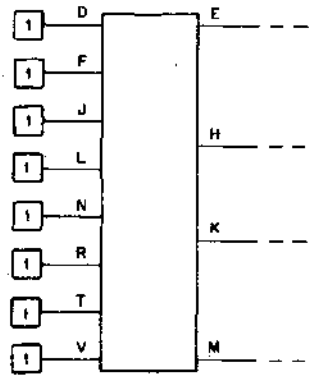
K SERIES



REAL TIME CLOCK

The K265 Reed Relay Driver has drive circuits for customer mounted relays. Up to five relays with Form A contacts can be mounted on the single height card. A logic 1 at each input energizes the relay to provide isolated contact outputs for special interfacing applications.

There are two mounting configurations: split lugs for axial lead relays, and mounting holes for certain printed circuit mounting relays. Typical reed relay closure speed is 1 ms to 2.5 ms.

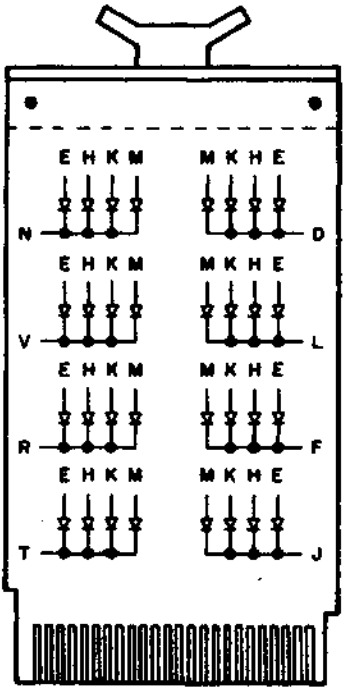


K281 FIXED MEMORY

The K281 is designed to be used with the K161 (Binary to Octal Decoder), the K681 (8-30 ma drivers) and the K134 (4 inverters), to build a read-only memory. Each K281 initially contains eight four-bit words consisting of only "1's". The user selects the codes he desires by cutting out diodes in the bit positions that are to be "0's". Additional K281 and K134 modules may be added to the system to generate more words and longer words.

CODING THE K281 DIODE MEMORY

When the K281 is used to build a K Series Read Only Memory, the codes are stored by cutting out diodes where zeros are desired. The diode map below shows the physical location of the diodes on the K281 and how they are connected to the module pins.



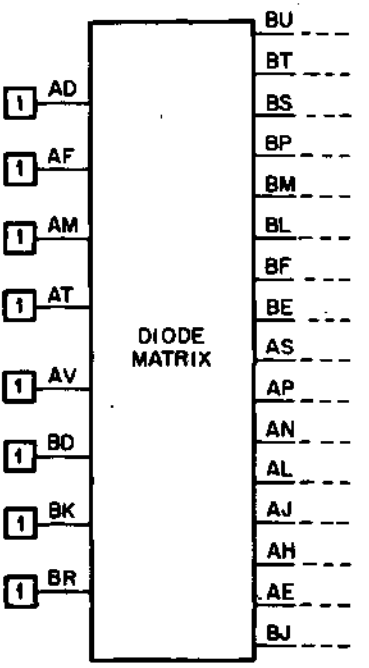
E,H,K,M are the four output pins.

D,F,J,L,N,R,T,V, are the eight drive lines.

Component side

DIODE MEMORY
K282

K SERIES

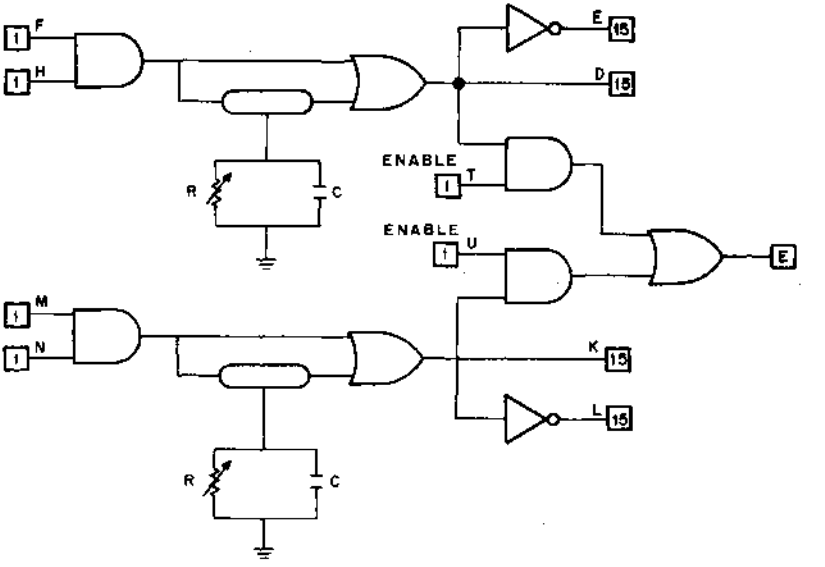


K282

The K282 is a diode matrix module which initially contains eight, 16-bit words. This matrix was designed to be used with K134 modules to obtain read-only memories. The user selects the codes he desires by cutting out diodes in the bit positions. More bits may be added by using additional K281 or K282 modules.

DUAL TIMERS
K302

K SERIES



The K302 module contains two independent timer circuits. Each circuit provides three delay ranges:

Range one:0.01 to 0.3 seconds
Range two: 0.1 to 3.0 seconds
Range three: 1.0 to 30 seconds

A range of up to three minutes can be obtained with a modification to the K302. A single wire jumper on each timer circuit can be removed and a resistor substituted.

The potentiometer on the module is adjusted clockwise for maximum and counterclockwise for minimum delay for each range.

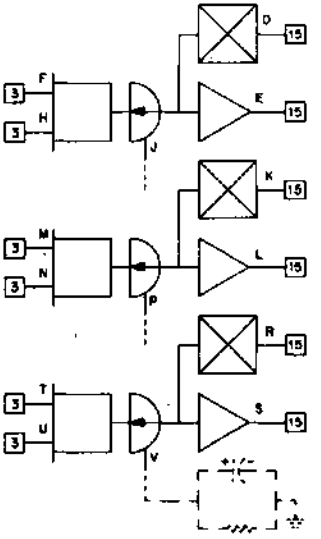
The time delay begins when either AND gate output goes to a logic 1 (pins F and H high, or pins M and N high); i.e., enable gates are provided to gate the individual delays to the expander output. The expander output, pin V, has no drive capability and must be connected to the OR expander input of a K113 or K123 module.

When the AND gate output steps to a logic 1 the delay is triggered. The non-inverted output rises after the time delay, while the inverted output falls. These outputs will remain in this state until the input steps to zero. At this time the outputs will revert to their initial state.

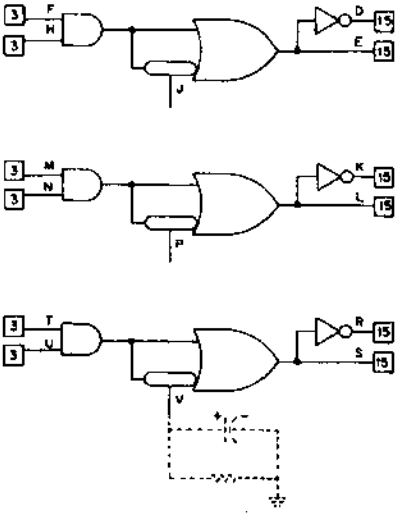
TIMER
K303

K SERIES

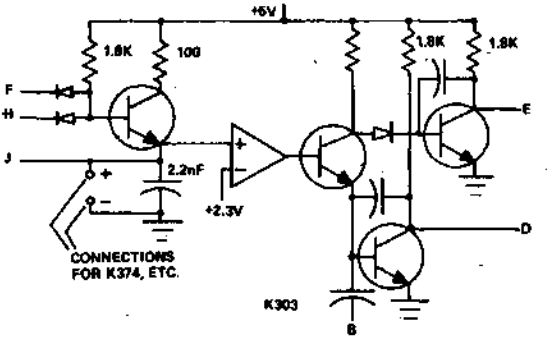
NEMA



MIL



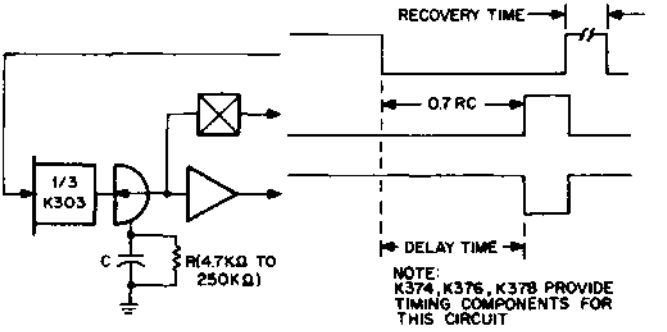
K303 timers provide time delays from 10 microseconds to 30 seconds and can be interconnected to form clocks with periods covering the same intervals. Fixed or adjustable delays and frequencies are obtainable. Calibrated controls are available (K371 through K378) for mounting directly on the K303. Remote controls can be added, if desired. A simplified schematic of the K303 is shown below. Note that the comparator has hysteresis, increasing the rejection of false "1" noise peaks at the input.



K303 TIMER SIMPLIFIED SCHEMATIC

When a K303 input gate steps to zero, the uninverted output falls after a controlled interval, while the inverted output rises. The interval can be as little as 10 μsec or as long as 30 seconds depending on the size of the R and C connected to pin J, P, or V. Recovery begins when the input gate output rises to a logic "1". In order to guarantee 95% repeat accuracy in the delay time, a recovery time of at least 300 C should be used, (C is in Farads, Time is in seconds). Be sure to include the 2.2 nf capacitor as part of the value for C. The delay interval in seconds is equal to .7RC (R in ohms, C in farads).

Any value of C may be used as long as R remains between 1 K and 250 K ohms.



1/3 K303 AS OFF DELAY

A positive step at the input gate output resets the K303 timer outputs. If the step occurs before a timeout is complete, the timeout is terminated and no change appears at the outputs. This property is sometimes convenient for establishing a pulse repetition rate threshold (Frequency Setpoint) .

A built-in 2.2 nanofarad timing capacitor assures adequate noise rejection when external capacitors are mounted several inches from the timer. Time threshold for resetting is always several percent of rated recovery time, so that noise rejection time increases in proportion to the size of the timing capacitor. Remote rheostats and timing capacitors may be used, but noise rejection will be degraded. If several timing capacitors will be switch selected, wire in the smallest near the module and switch the others in parallel with it.

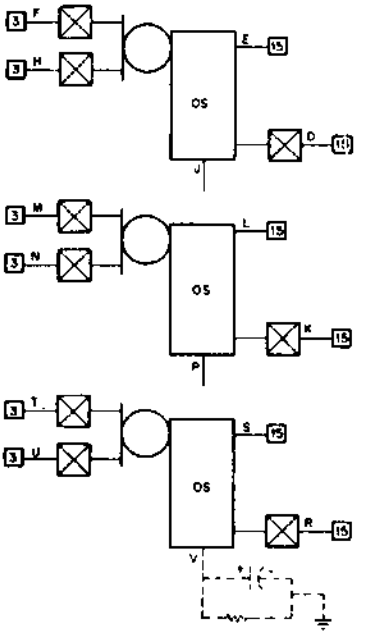
Variable or fixed timing resistors used with K303 timers may be any carbon composition, film, or wirewound rheostat or potentiometer. Delay time is linearly proportioned to resistance from 250KΩ down to a few thousand ohms, falling to zero (reset inhibited) below a few hundred ohms. Momentary shorting to ground of control pins will not cause damage, but a padding resistor of at least 300Ω in series with variable controls is advisable both to prevent continuous grounding and to avoid confusion which may arise if resetting in inhibited.

Timing capacitors may be any ordinary mica, paper, ceramic, or low leakage electrolytic type. For delays above a few seconds, wet slug tantalum electrolytic capacitors are advisable to avoid leakage-induced drift at high temperatures. Temperature coefficient of delay has been optimized for the carbon composition potentiometers and tantalum electrolytic capacitors used in the controls described below, and is typically less than ±1% in 5°C (9°F) using K731 and K732 regulators for power.

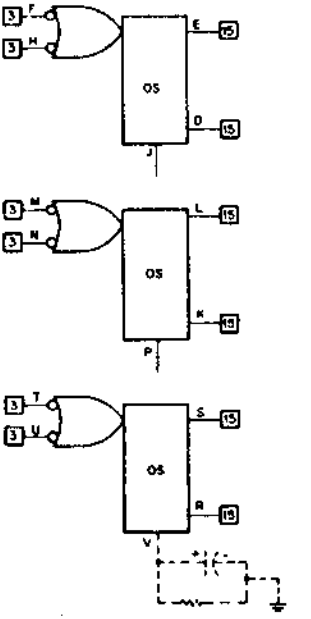
ONE SHOTS
K323

K SERIES

NEMA



MIL



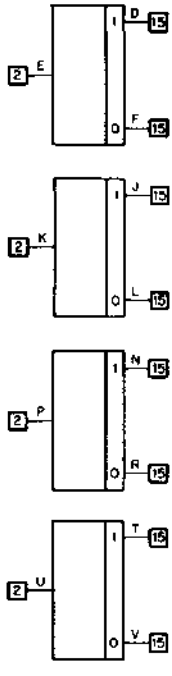
K323 one-shots provide output pulse widths from 10 μs to 30 seconds with either fixed, or adjustable delays. Calibrated controls K374, K376, and K378 are available for mounting directly on the K323. Remote controls can be mounted on a K990 Timer Component Board.

When either input to the K323 gate steps to 0, the uninverted output rises and stays positive for a time equal to 0.7 RC. The pulse width is controlled by the value of R and C connected to pin J, P, or V. The one-shot recovery begins when both signals at the input gate rise to logic 1.

SCHMITT TRIGGERS
K501

K SERIES

NEMA



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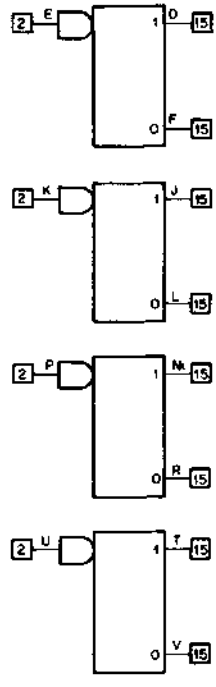


The K501 can be used with the K580, K581, or K578 to provide simultaneous true and complementary signals with full K series drive. Built in hysteresis and slowed outputs insure reliable operation in noisy signal environments.

Schmitt Triggers can also be used to speed up signals with very slow rise or fall times for input into pulse formers or logic circuits where timing considerations are critical.

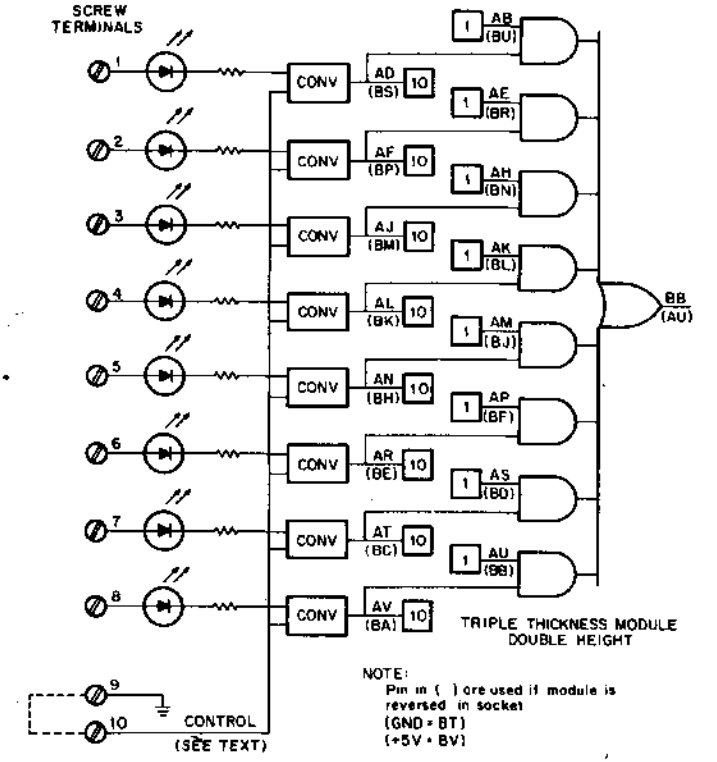
The K501 is not designed to be connected directly to unfiltered contacts or other noisy signal sources. The Schmitt Triggers have standard K-Series outputs and their rise time is on the order of 7μs. Minimum hysteresis between upper and lower Thresholds is 1 volt.

A logic "1" level at pins E, K, P and U forces pins D, J, N, and T high and pins F, L, R, and V low. A logic "0" level at pins E, K, P, and U forces pins D, J, N, and T low and pins F, L, R, and V high.

DC INPUT CONVERTERS
K564

K SERIES

MIL



Pins in parentheses are used when module is reversed in socket.

The K564 provides conversion of eight dc signals in the 10 to 55 Vdc range to K-series logic levels. A light-emitting diode (LED) indicator is provided for each input circuit and will light with a 10-55 V input. Clamp type input terminals will accept two wires up to # 14 AWG.

Control terminals 9 and 10 are provided to control the input current for all circuits on the module. Terminal 9 is to be connected to the negative reference of the external supply which should be tied to both chassis and logic ground.

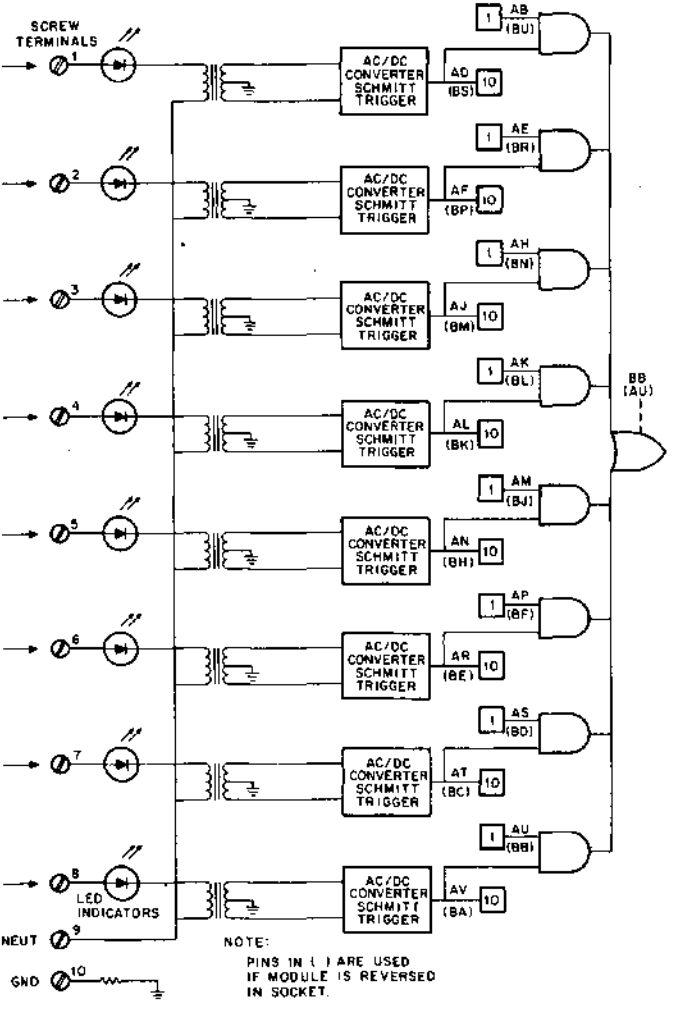
Each circuit of the K564 contains an RC input noise filter to provide switch bounce rejection.

Gating circuits equivalent to four K026 sections are included for contact scanning applications using the K161 or to facilitate forming the logical OR of many inputs. Direct outputs are from active circuits and may not be wired together. The OR expander output (if used) must be connected to the OR expansion node of a K-series gate.

K579
ISOLATED AC INPUT CONVERTERS

K SERIES

MIL



The K579 is an isolated ac input converter module containing eight 120 Vac input circuits. The input circuits are transformer isolated and have LED indicators which indicate voltage present on the input screw terminals. Schmitt triggers are provided on each input for bounce rejection. A 120 Vac input will cause the corresponding output to be at +5 V. A gatable expander output is provided which may be connected to the OR expansion input of a K-series gate.

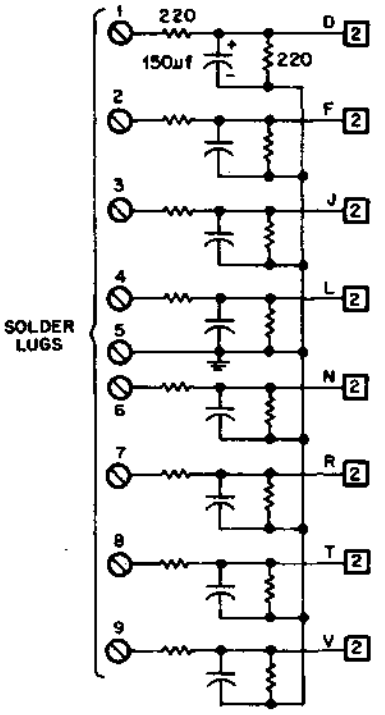
Either the K724 Interface Shell or K943 Mounting Rack will provide suitable mounting of the K579.

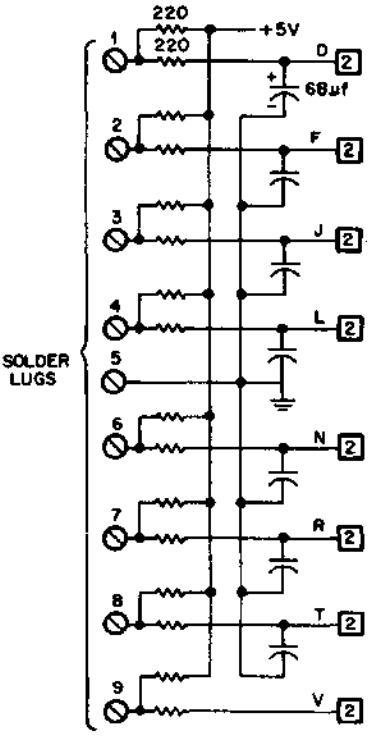
A 10-terminal, nylon strip is provided for connection to 120 Vac field wiring. The strip has 3/8 terminal spacing, captive screws with wire clamps, and is color coded red for ac. The terminal strip meets NEMA and JIC specifications regarding barrier height and voltage breakdown. Each terminal is marked according to its function: Input (→), Neutral (NEUT), and Chassis Ground (GND).

DRY CONTACT FILTERS

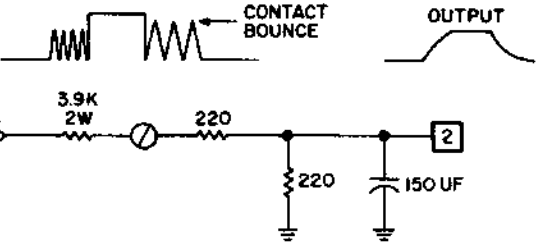
K580, K581

K SERIES





K580 **K581**



These filters convert signals from dry or wiping contacts to logic levels. Primarily they are used with gold contacts such as the new encapsulated reed limit switches, thumbwheel switches, and the like. Those push-buttons or slide switches that provide good wiping action will also operate reliably with these filters, but silver contacts designed for long life on heavy duty loads are likely to give trouble. For them, use interfaces designed for such application like K508-K716 or K578, or at least switch a high voltage. (see K580 voltage table.)

Schmitt Triggers should be used on the outputs of both the K580 and K581 when they are used for one shot or timer inputs.

Access to K580 and K581 inputs is by solder lugs only. Strain relief holes are provided in the board (near handle) for a 9-wire cable. The avoidance of contact connectors on the logic wiring panel combined with heavy filtering guarantees noise isolation and protects modules by preventing accidental short circuits. Below is a summary of other characteristics.

	Contact Current	Contact Voltage	Output for Contact Closed	Time Delay on Closure	Time Delay on Opening
K580	22ma	See Table	high	10msec	30msec
K581	22ma	5V	low	20msec	20msec

(Time delay figures above are nominal, and assume connection to the input of a standard gate such as K113 or K123.)

The contact current for the K581 comes from the logic supply, making it very important to assure freedom from accidental high voltages on K581 inputs which could damage many logic modules by getting through to the system power supply. This hazard is not present with the K580, which uses an external source of +10 volts or more. The table below shows how external dropping resistors may be added to provide higher voltage operation.

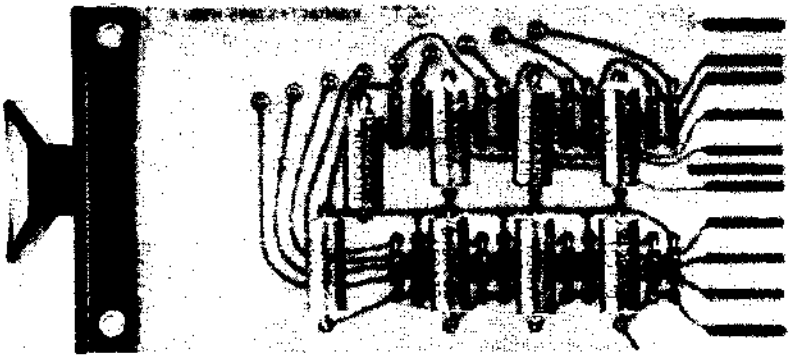
TABLE OF K580 VOLTAGE DROPPING RESISTANCES

CONTACT SUPPLY VOLTAGE	10	12	15	24	28	48	90	100	120
Dropping Resistance	0	82Ω	220Ω	620Ω	820Ω	1.8KΩ	3.6KΩ	3.9KΩ	4.7Ω
Dissipation	—	0.05W	0.11W	0.3W	0.4W	0.85W	1.8W	2.0W	2.5W

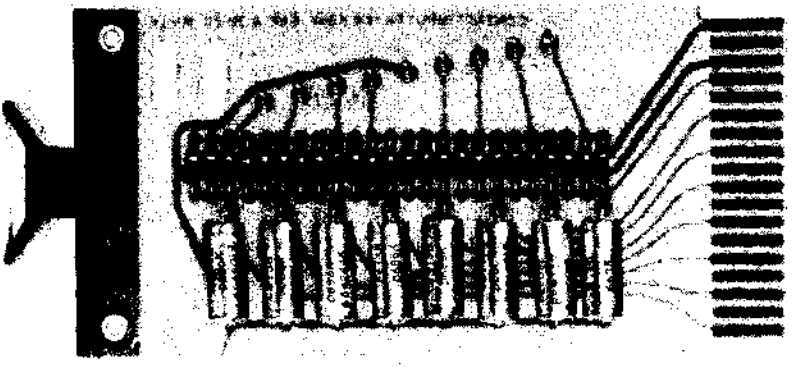
When using dropping resistors and higher voltage supplies, total tolerance of resistors and supply should be ±10% to insure high levels between +4 V and +6 V at the logic. Also observe that a handful of dropping resistors in 90 V or 120 V systems may dissipate more power than the entire logic system, and must be located so as not to cause excessive temperature rise in the K series environment.

Note that these circuits may not be paralleled to obtain the wired OR or wired AND function, and that fanout is limited to 2 milliampers in order to maintain the low (zero) output voltage within normal K-Series specifications. Fanout to ordinary logic gates and diode expanders may be raised to 4 milliampers if some noise and contact bounce rejection can be traded off; but hysteresis inputs such as those at counter inputs, rate multiplier, etc., may not switch properly if the logic zero is allowed to rise much above +0.5 V.

Looking at the component side of both the K580 and K851, the solder lug connections are numbered 1 to 9 from pin end to handle end.



K580

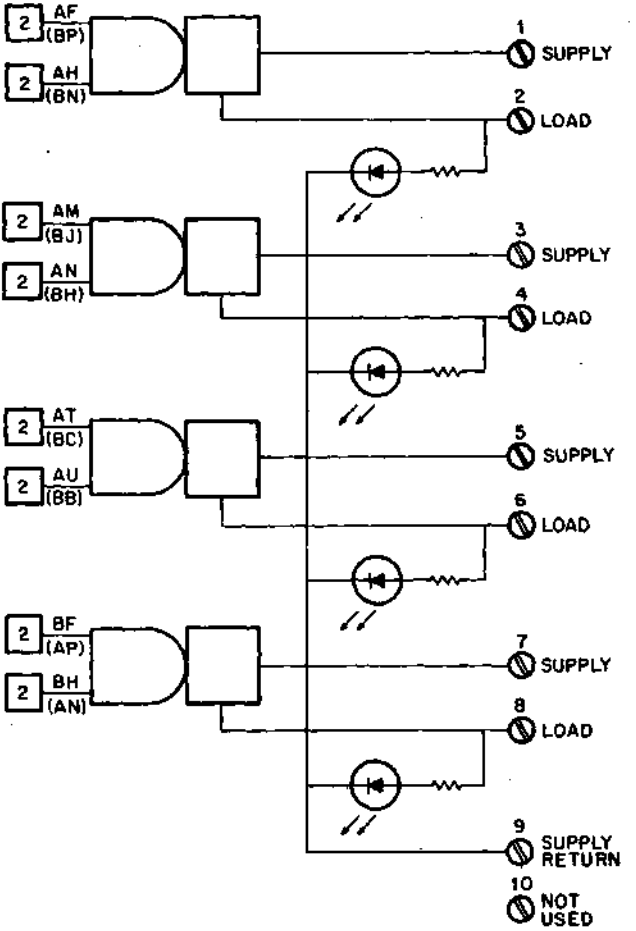


K581

ISOLATED AC SWITCHES
K616

K SERIES

MIL

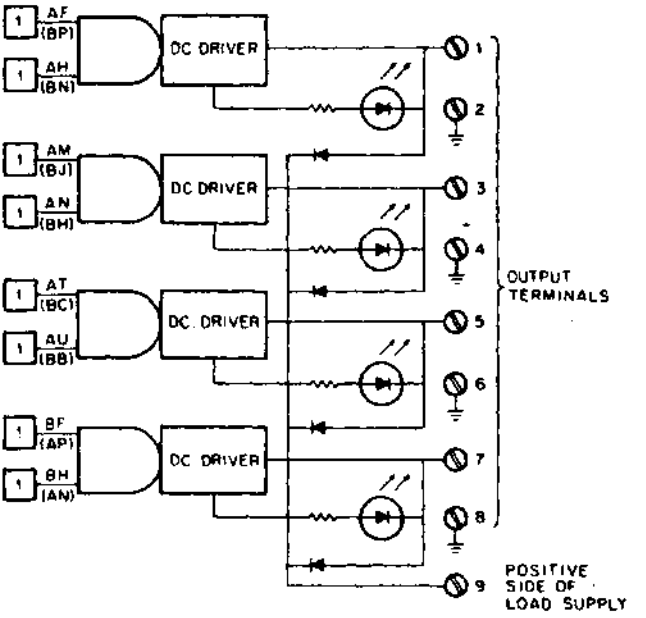


The K616 isolated ac switch module contains four isolated 120 Vac TRIAC output circuits. Each output is fused and has a light-emitting diode to indicate when the output is ON. The fuses can be changed from the terminal strip side of the module without removing field wiring or removing the module from the system. Either the K724 Interface Shell or K943 Mounting Rack will provide suitable mounting for the K616.

The K616 is a new version of the K614 featuring improved operation under light output loads, lower input loading, and a new 10-terminal nylon strip with 3/8 spacing between terminals. The terminal strip meets NEMA and JIC specifications regarding barrier height and voltage breakdown. It has captive screws with wire clamps to accept 2-14 AWG wires and is color coded red for ac. Each terminal is marked according to its function: Supply (LINE), Switched Output (→) AC Return (NEUT), and Chassis Ground (GND).

DC DRIVERS
K657

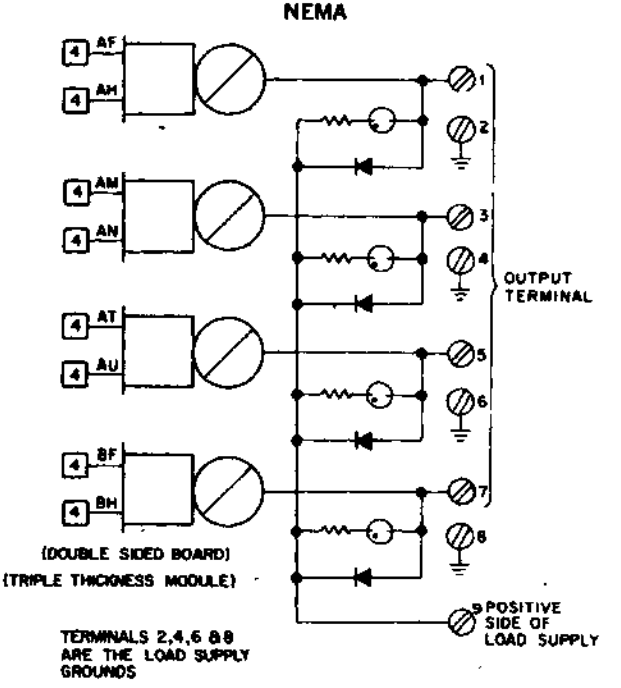
K SERIES



The K657 DC Driver module contains four 250 Vdc drivers. Each circuit of this driver can switch to ground up to 1.0A at up to 250V. The outputs will switch to ground whenever both AND gate inputs are high (logic 1).

DC DRIVER
K658

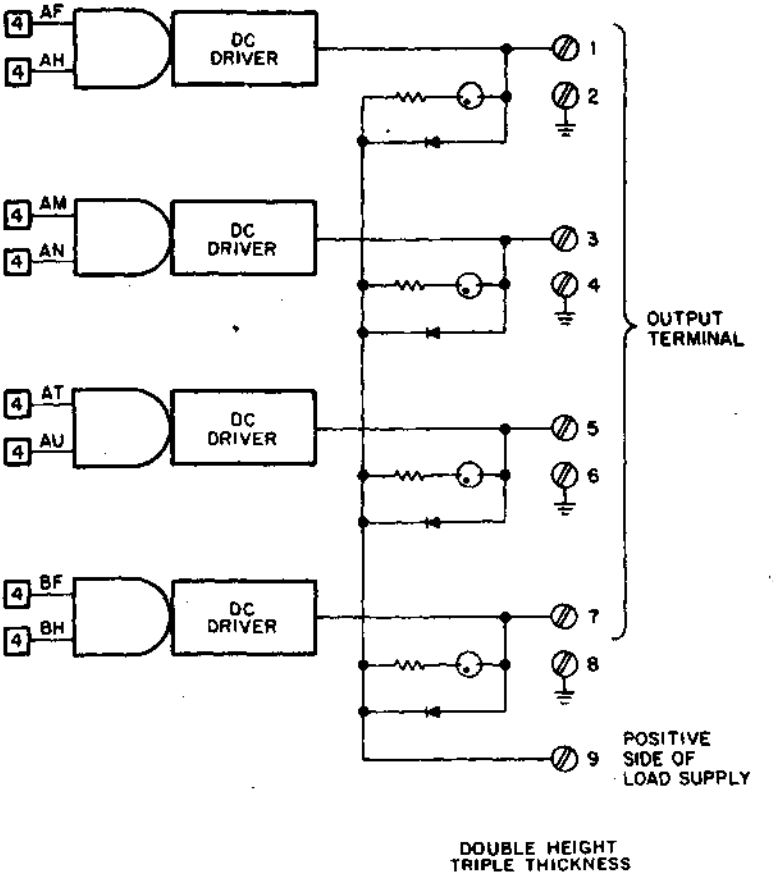
K
SERIES



K658 4 AMP DRIVER

Each circuit of this versatile driver can deliver up to 4 amperes at up to 125 volts. This module has integral clamp-type terminals and neon indicator lamps. (Lamps are effective only at 90 volts and above.) This driver module is designed to be used with K724 interface shells. Positive side of load supply must be connected to protect output transistors from damage during turnoff transient.

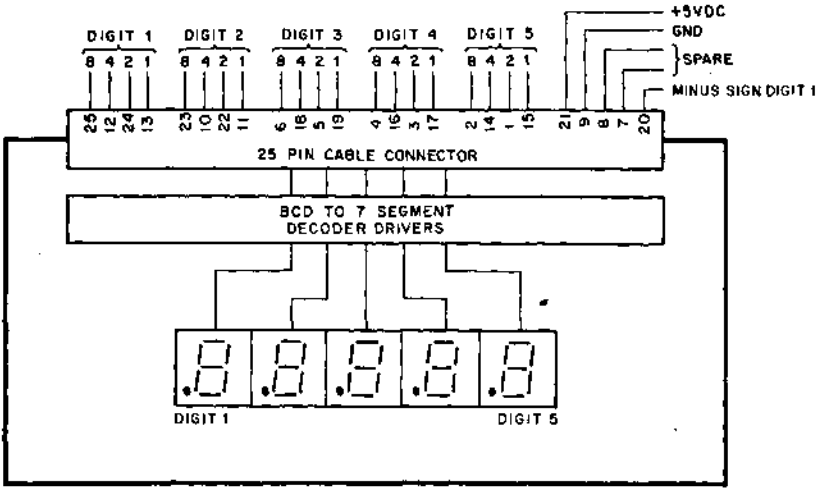
MIL



Terminals 2, 4, 6 and 8 must be connected directly to the negative terminal of the load power supply or damage to the module will result from high currents.

5-DIGIT DISPLAY
K675

K SERIES

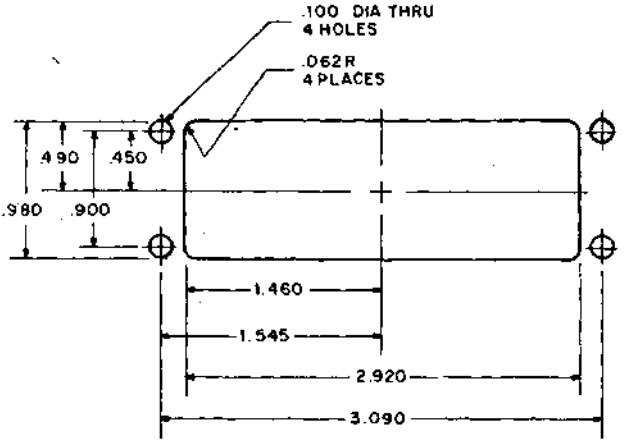


The K675 is a 5-digit display module designed to be panel mounted. Five digits of 7-segment LED readouts are housed in a plastic bezel with a lucite window which can be mounted through a panel cutout. The display is connected to the logic backplane wiring by a 10 foot, 25-conductor cable (BC14F) and a double height cable connector module, K783. Five digits of BCD-coded data, presented to the K783, will be displayed by the K675.

A blanking feature to suppress zeroes to the left of the last non-zero digit is controlled by a wire jumper on the display module. The display is pre-enabled for blanking but can be disabled by removing a wire jumper. If disabled, the K675 will display all BCD digits, including zeroes.

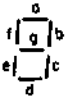
A decimal point is located to the left of each digit and can be controlled by jumpers W2 through W6. Removing a jumper will extinguish the corresponding decimal point.

Digit 1 can be used for a minus sign when displaying 4-digit negative numbers. When the minus sign is used, digit 1 is not available for displaying other numbers. The minus sign is illuminated by groundng pin 20 directly, or with a K-series NAND gate or inverter.



Panel Cutout Dimensions

DISPLAY SEGMENTS



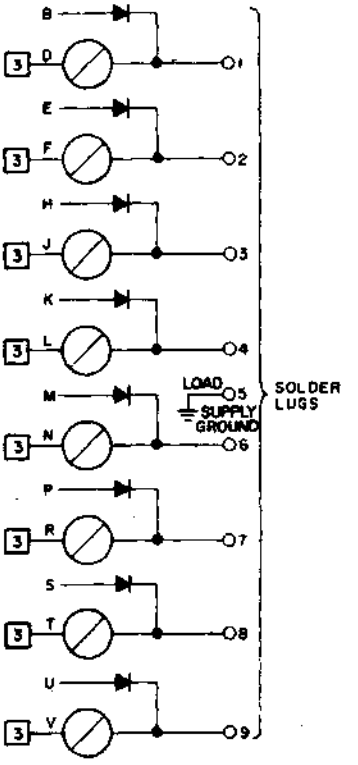
DECIMAL VALUE	BCD INPUTS 8	4	2	1	5082-7730/7731 SEGMENT OUTPUTS a	b	c	d	e	f	g	FONT
0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	1	0	1	1	0	0	0	0	1
2	0	0	1	0	1	1	0	1	1	0	1	2
3	0	0	1	1	1	1	1	1	0	0	1	3
4	0	1	0	0	0	1	1	0	0	1	1	4
5	0	1	0	1	1	0	1	1	0	1	1	5
6	0	1	1	0	0	0	1	1	1	1	1	6
7	0	1	1	1	1	1	1	0	0	0	0	7
8	1	0	0	0	1	1	1	1	1	1	1	8
9	1	0	0	1	1	1	1	0	0	1	1	9
10	1	0	1	0	0	0	0	1	1	0	1	
11	1	0	1	1	0	0	1	1	0	0	1	
12	1	1	0	0	0	0	1	1	1	0	0	
13	1	1	0	1	1	0	0	1	0	1	1	
14	1	1	1	0	0	0	0	1	1	1	1	
15	1	1	1	1	0	0	0	0	0	0	0	

NOTE: 1 = Segment ON
0 = Segment OFF

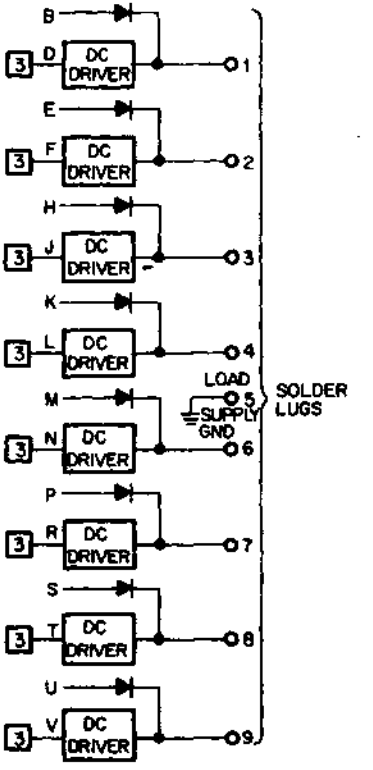
LAMP DRIVERS
K681

K SERIES

NEMA



MIL



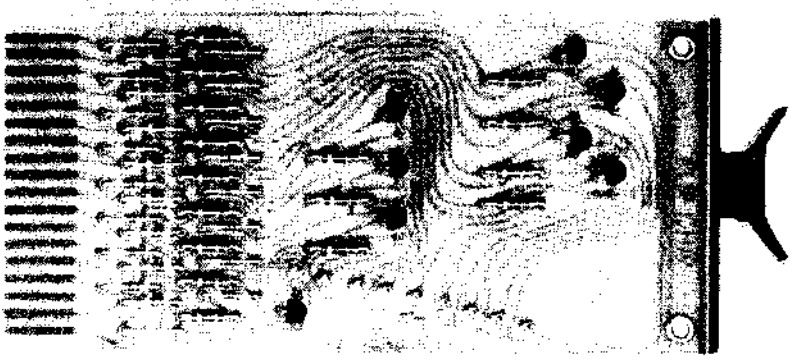
K681 LAMP DRIVER

These eight-circuit modules drive external loads through 9-conductor cable soldered to split lugs at the handle end by the user. Strain relief holes are prepunched in the board. Logic "0" turns the driver off, logic "1" turns it on.

Pin connections via diodes to outputs facilitate production automatic module testing while isolating system wiring from high voltages. Circuits are not slowed, and these connections are not recommended as output tiepoints unless exceptional care is taken to prevent noise and damaging voltages from degrading system reliability.

MODULE TYPE	OUTPUT RATINGS		
	RESISTIVE	INDUCTIVE	INCANDESCENT LAMPS
K681	18V, 30ma	18V, 30ma with added suppression diodes (K784)	Lamps rated 18V, 40ma operated at 12V to reduce current to 30 milliamperes.

Note greatly reduced ratings on tungsten loads. Lamp filaments draw typically ten times more current at turnoff than when hot, resulting in very high transistor dissipation if supply voltage is high. Series current limiting resistors or shunt preheat resistors could be used to limit surge in certain cases, but ratings above assume this would be awkward or impractical.

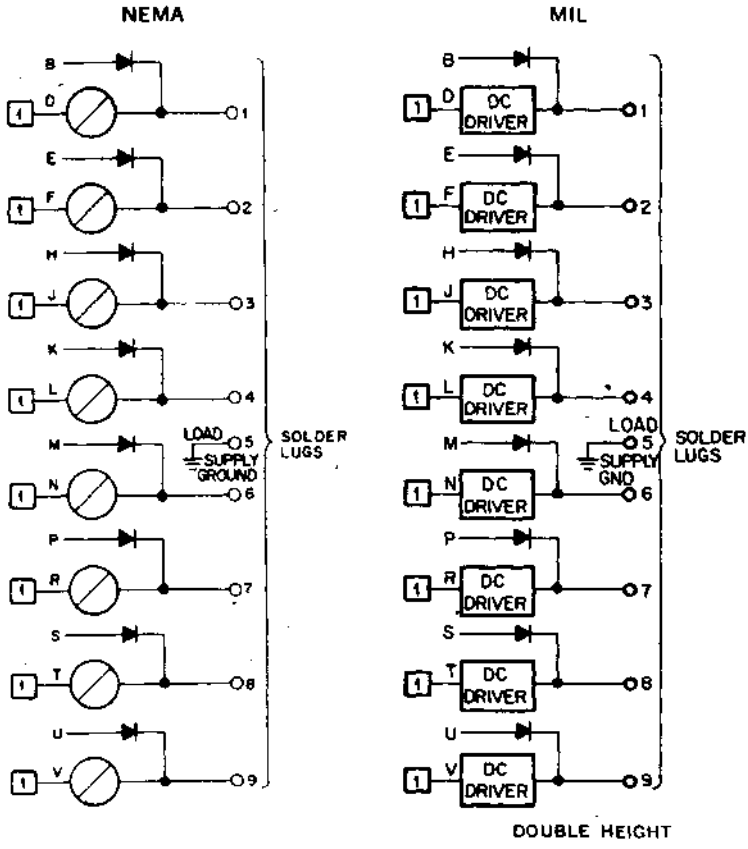


K681

Solder lugs on the K681 shown above are numbered 1 to 9 from left to right.

LAMP DRIVERS
K683

K SERIES



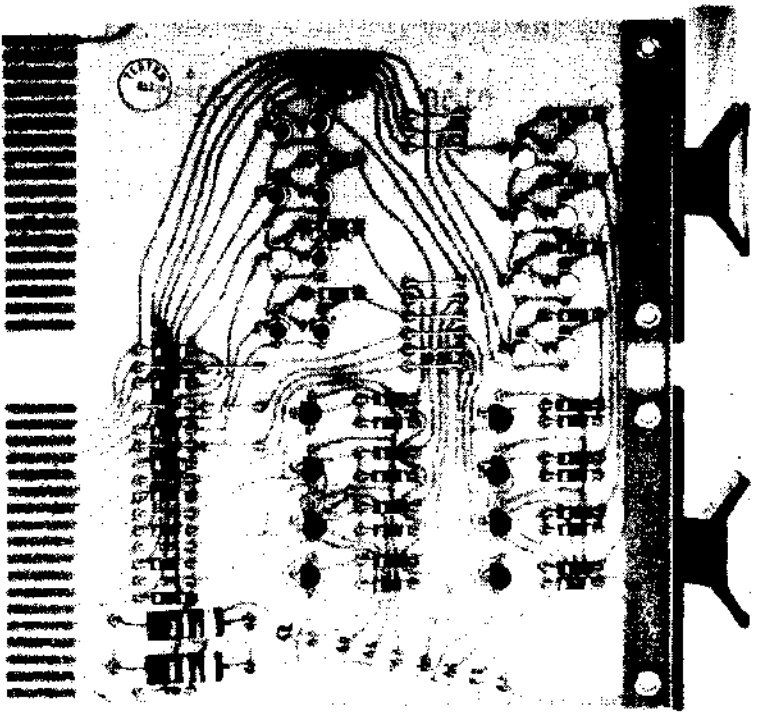
K683 LAMP DRIVER

These eight-circuit modules drive external loads through 9-conductor cable soldered to split lugs at the handle end by the user. Strain relief holes are prepunched in the board. Logic "0" turns the driver off, logic "1" turns it on.

Pin connections via diodes to outputs facilitate production automatic module testing while isolating system wiring from high voltages. Circuits are not slowed, and these connections are not recommended as output tiepoints unless exceptional care is taken to prevent noise and damaging voltages from degrading system reliability.

MODULE TYPE	OUTPUT RATINGS		
	RESISTIVE	INDUCTIVE	INCANDESCENT LAMPS
K683	55V, 250ma	55V, 250ma with added suppression diodes (K784)	Lamps rated 40ma, to 48V; Lamps rated 60ma, to 28V; Lamps rated 80ma, to 18V; Lamps rated 100ma, to 12V

Note greatly reduced ratings on tungsten loads. Lamp filaments draw typically ten times more current at turnon than when hot, resulting in very high transistor dissipation if supply voltage is high. Series current limiting resistors or shunt preheat resistors could be used to limit urge in certain cases, but ratings above assume this would be awkward or impractical.



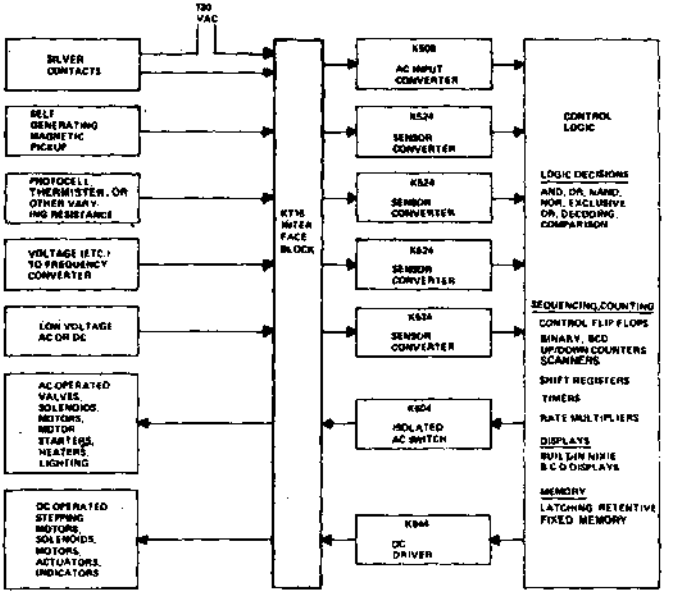
K683

Solder lugs on the K683 shown above are numbered 1 to 9 from left to right.

INTERFACE BLOCK
K716

K SERIES

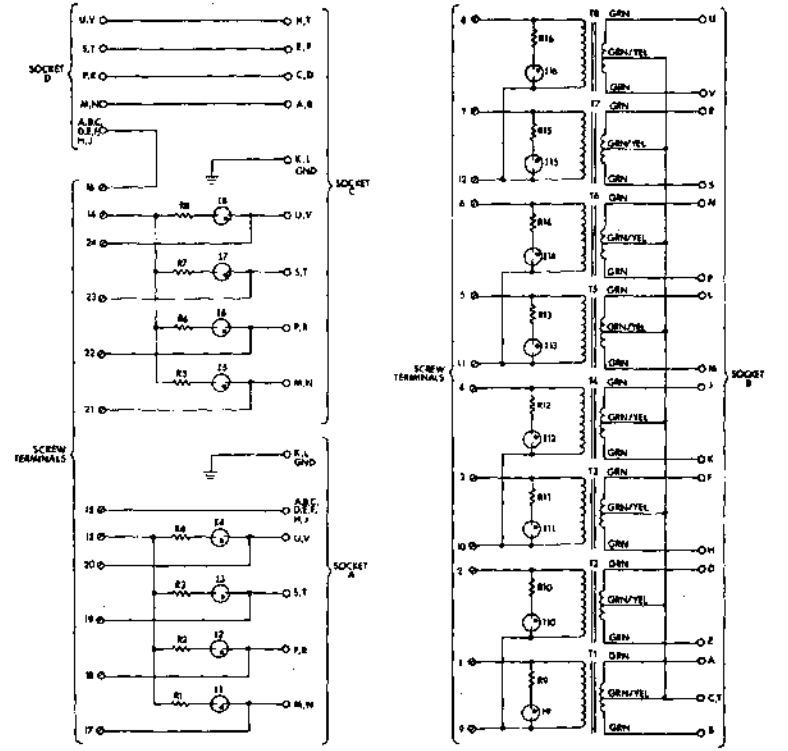
An important hardware feature of the K Series system is the K716 Interface by electricians. The logic modules interconnect to the K716 by plug-in ribbon cables.



TYPICAL CONTROL APPLICATIONS FOR K SERIES MODULES INTERFACED BY K716

Contacts: Ordinary silver contacts of the kind found in limit switches, pressure switches, and pushbuttons work best when operated with healthy levels of both line voltage and load current. The sparking that results prevents buildup of contact surface contamination. To assure reliable switching, isolation transformers in the K716 provide a reactive load for switched 120 vac pilot voltages. The K508 AC Input Converter ignores contact bounce. Hash filters in the module, and attenuation in the isolation transformer built into the K716, reduce electrical noise. Built-in indicators permit quick maintenance checks.

The K716 Interface Block serves as an interconnection interface for those K Series modules that communicate with external equipment. External field wiring terminates at a 24-terminal screw connection block that accepts plain stripped wire up to 14 guage. No separate crimped or soldered terminals are required.



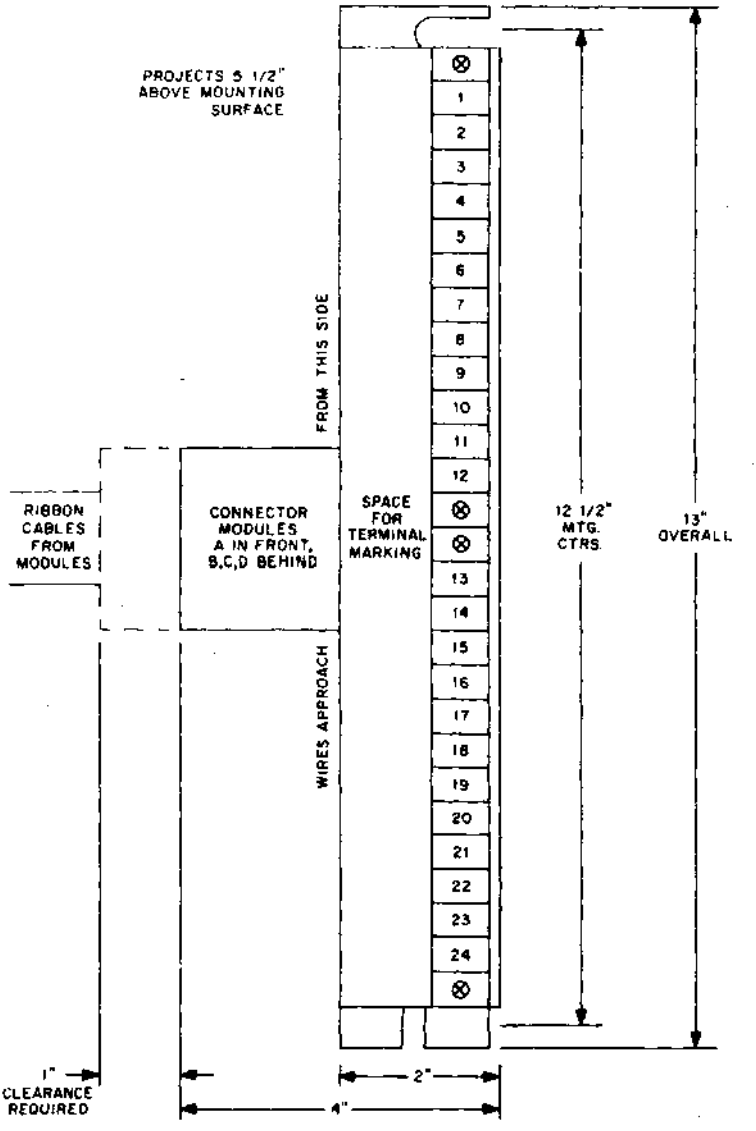
K716 INTERFACE BLOCK SCHEMATIC

Ribbon cables from the K Series interface modules connect to printed circuit board sockets on the K716. This allows the K716 terminal block to mount on the rear panel of a NEMA enclosure for the convenience of electricians, while the digital system itself mounts on the door for easy access to both modules and logic wiring. The ribbon cable makes neat, simple wiring layouts and easy flexing at the hinge.

The three sockets in the K716 terminal block contain the same module-connector system used for the modules themselves, permitting quick disconnect of the entire logic system without affecting reliability. This arrangement, together with the K940-K941 bolt-on mounting hardware, allows initial check-out of control systems away from the site, as well as minimizing downtime in case of failure. The cable sockets have the same reliable gold contacts as K Series module sockets.

Socket B, for use with the K508 AC input converter, is fed by eight isolation, stepdown and contact loading transformers contained within the aluminum shell of the K716. The transformer primaries receive 120-volt pilot signals from external contact closures. Each input is monitored by a neon indicator.

Sockets A and C are for use with K524, K604, and K644. Neon indicators are provided to monitor the outputs of the K604 Isolated AC Switch module.



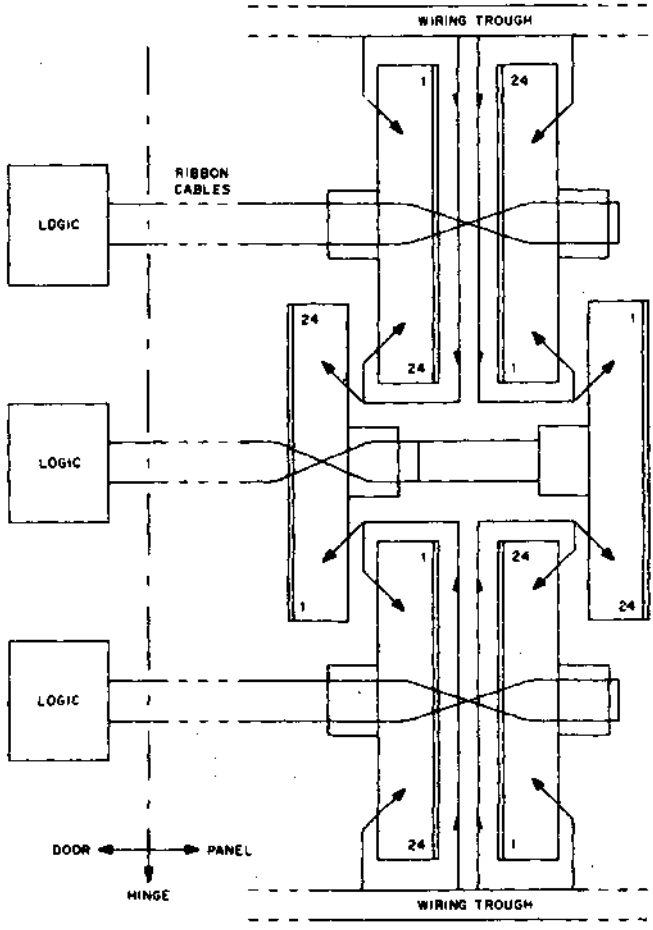
K716 INTERFACE BLOCK
FRONT VIEW

The drawing above shows approximate dimensions of the K716. Mounting slots clear no. 10 screws and allow compensation for mounting screw location tolerances.

All neon indicators are located within the K716 shell, visible at the rear of associated screw terminals.

Socket D, normally terminated by a shoting plug, runs all return lines from connector C to a common point. If the shorting plug is removed, independent wiring of connector C return leads for K524 or K604 modules is possible. A W033-06F-W033 cable connector ($15) must be installed between socket D and socket A. An extra 2-inch clearance is required by this connector board. Independent wiring provides connections for four two-wire circuits instead of 8 circuits with bussed returns.

Below is a recommended mounting pattern for combining many interface blocks. This pattern can be extended provided the 30" reach of ribbon is not exceeded.



K716'S IN INDIVIDUAL ENCLOSURE

INTERFACE SHELL
K724

K SERIES

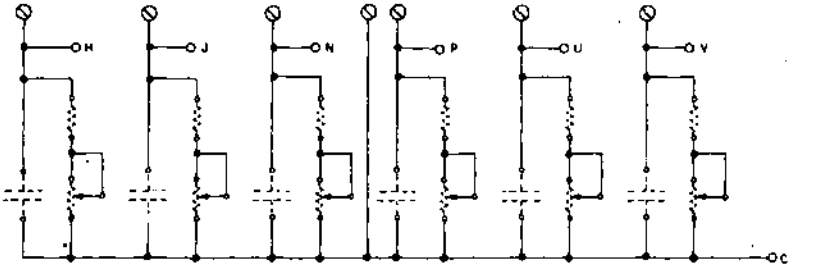
Unlike the K716 Interface Block, the K724 Interface Shell does not contain any electronic components. Instead, it provides the connectors and the mechanical support for self-contained interface modules K578, K614, K615, K650, K652, K656 and K658. Up to four K578, K614 or K615 modules or two K650, K652, K656 or K658 modules may be installed, with eight module sockets remaining for decoding or gating modules. The limit of two DC Driver modules is due to the fact that they cannot be reversed in their connector sockets.

Convenient wiring channels are obtained between units if they are mounted on 12" centers vertically and 6" centers horizontally. This way a total of up to 32 input converters and 16 output converters fit in one square foot of panel space, along with up to 16 logic modules.

The K724 provides only logic power and ground connections between all but two sockets. It is primarily intended for very simple logic systems or for large systems where all input and output logic levels are connected to a separate logic unit by connector cables.

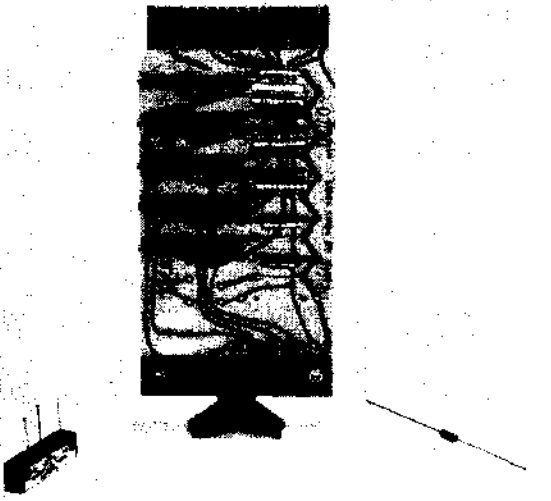
TIMER COMPONENT BOARD
K990

K SERIES



The K990 is a predrilled etched module for mounting up to six RC networks for K301, K303, or K323 timer controls. Any capacitor size up to a "D" case tantalum can be mounted in the space provided. A trimpot and series resistor can be mounted in the remaining space. Trimpot adjustments are accessible from the edge of the module. If the module is not mounted in the top row of modules in the system, a W980 extender module will be required to make trimpot adjustments. Etch layout is for trimpots with a staggered center pin. Connections to the module can be made either through the pins or through a cable soldered to split lugs.

Dimensions for trimpot mounting are:



MODULES NOT RECOMMENDED FOR NEW DESIGN

The M, W, R, and B Series modules described in this subsection are modules from earlier Logic Handbooks that are outmoded and are not recommended for new design. However, these modules are perfectly functional for use as spares or replacements in systems that previously utilized these circuits. Detailed descriptions of these modules are contained in earlier versions of the Logic Handbook. For ordering information, contact the Sales Support Manager at the address listed in the front of this Handbook.

M SERIES

M152 Dual 1-of-8 Decoder
The M152 consists of two identical binary-to-octal decoders, each requiring complementary inputs. This module may be used for applications such as memory address decoding.

M160 AND/NOR Gate
The M160 contains three general purpose AND/NOR gates which perform functions similar to those of the M121.

M169 Gating Module
The M169 contains groups of 4-input AND/NOR gates prewired as four stages of a 4-input, 1-output multiplexer or similar gating function.

M208 8-Bit Buffer/Shift Register
The M208 is an internally-connected 8-bit buffer/shift register. Provisions are made for gated single-ended parallel load, bipolar parallel output, and serial input.

M253 16-Word x 12-Bit RAM
The M253 is a 192-bit read/write random access bipolar semiconductor memory organized in a 16-word by 12-bit array. This module may be used as a scratchpad memory of 16 words by 12 bits with other modules of the same type, or may be used to construct larger memory arrays where fast reading and writing are required.

M260 4-Word x 12-Bit Associative Memory
The M260 is a high-speed 48-bit associative random access memory that may be used for comparing and locating data. It is a 4-word by 12-bit array in which the equality search is performed on all bits in parallel. All inputs and outputs are TTL-compatible.

M261 Four-State Motor Translator
The M261 develops the sequence of patterns necessary to step a Sigma or Superior Electric type stepping motor (4 winding).

M262 Ten-State Motor Translator
The M262 generates the sequence of patterns required to step a Fujitso type stepping motor (5 winding).

M302 Dual Delay Multivibrator
The M302 contains two delays (one-shot multivibrators) which are triggered by a level change from High to Low or a Low-going pulse whose duration is ≥50 ns. When the input is triggered, the output changes from Low to High for a predetermined length of time and then returns Low. This delay time is adjustable from 50 ns to 7.5 ms using the internal capacitors and can be extended by adding an external capacitor. This module is replaced by the M3020 described elsewhere in this Handbook.

M410 Reed Clock
The M410 is a free-running contactless resonant-reed-tuned clock which provides stable timing signals for a system using the M706 and M707 teletypewriter converter modules.

M452 Variable Clock
The M452 is a free-running clock which generates the necessary timing signals for the PDP-8/I teletypewriter control.

M606 Pulse Generator
The M606 contains six pulse generators which may be used for setting or clearing of flip-flops by applying the output of the M606 to the direct Clear or Set inputs of up to 14 flip-flops.

M610 Open Collector Two-Input NAND Gate
The M610 contains six 2-input NAND gates with open collector outputs. Also contained on the module is a pulse amplifier which does not have an open collector output.

M661 Positive Level Driver
The M661 contains three 3-input AND circuits which may be used to drive low-impedance, unterminated cables with M Series logic levels or pulses of duration greater than 100 ns.

B SERIES

B Series FLIP CHIP modules operate at frequencies from dc to 10 MHz. They are electrically and mechanically compatible with all other R and W Series modules.

B104, B105, B123, B124 Inverters
Each inverter is analogous to a switch. If the inverter base is at −3 v and the inverter emitter is at ground, the transistor is saturated and a conducting path is established between the emitter and the collector of the inverter. If the base is at ground, or if both base and emitter are at −3 v, the emitter-collector path is open circuited (i.e., will not allow current to flow).

Delay through the inverter is approximately 12 nsec for lightly loaded inverters driven by a pulse.

The B104 contains three standard 10-mA clamped loads and four transistor inverters, each with its base, emitter, and collector brought to connector pins.

The B105 has five standard 10-mA clamped loads and five transistor inverters, with each emitter grounded, and with each base and collector brought out.

The B123 has three standard 10-mA clamped loads and eight transistor inverters. The inverters are tied together in series groups of two.

The B124 has three standard 10-mA clamped loads and nine transistor inverters, each with emitter grounded, and with each base and collector brought to terminals. The collectors are tied together in groups of three.

B113, B115, B117, B171 NAND/NOR Gates
The B113, B115, B117, and B171 are positive NOR diode gates; they form NOR gates for ground inputs and NAND gates for −3 v inputs. The outputs of the diode gates drive inverters similar to the B105, for power amplification. The typical total transition time is 40 nsec for output fall and 60 nsec for output rise.

The B113 provides three standard 10-mA clamped loads and four diode gates, each with two diode inputs and the collector brought out.

The B115 has three standard 10-mA clamped loads and three diode gates, each with two diode inputs and the collector brought out.

The B117 has two diode gates, each with six diode inputs and the collector brought out. In addition, the emitter of one of the inverters is available.

The B171 is a single gate with twelve diode inputs. In addition to the positive NOR output, another inverter has been added at the output; using the inverted output makes the B171 an OR gate for ground inputs and an AND gate for −3 v inputs.

B130 Three-Bit Parity Circuit
This special logic module has two levels of high-speed logic and complementary outputs. It is designed to compute the parity (odd or even) of the contents of a flip-flop register with a minimum of time delay, but it can be used wherever there is a need for four 3-input negative diode AND gates feeding a 4-input OR gate.

B155 Half Binary-to-Octal Decoder
The B155 module is used alone as a 2-bit decoder with two enable inputs, or it is used with another B155 to form a full 3-bit (binary-to-octal) decoder, using one combined enable line. Either way, each binary input combination results in one selected output held at ground if the decoder is enabled. No output will be selected if an enable input is held at ground. The decoder consists of four 4-input diode gates with appropriate input interconnections.

B201 Flip-Flop
The B201 has nine built-in inverters for accomplishing such operations as set, clear, jam-transfer, shift, and complement without the need for additional gating. The B201 can also be used in counters.

B204 Quadruple Flip-Flop
Module B204 contains four bits of unbuffered flip-flop memory. Each flip-flop comprises two B105-type inverters, two 10-mA clamped loads, a common clear input, and an indicator driver resistor.

B301 Delay
The B301 is a one-shot delay that contains three capacitors for delay range selection, and a screwdriver-adjustable rheostat for fine control. Typical level output duration ranges are 60 to 700 nsec, 0.5 to 10 μsec, and 7 to 150 μsec. By connecting an external capacitor, the range can be further increased.

B360 Delay with Pulse Amplifier
The B360 contains a delay line which may be varied from 25 nsec to 250 nsec, and a standardizing pulse amplifier similar to one half of a B602. The length of the delay is adjusted by means of a slotted screw accessible from the handle-end of the module. The high resolution of the delay line (approximately ¼ nsec) makes it ideal for high-speed timing chains.

B401, B405 Clocks
The B401 Variable Clock produces standard pulses from a stable, RC-coupled oscillator with a wide range of frequencies. The variable clock is often used as a primary source of timing for large systems. The frequency is variable from 10 KHz to 10 MHz.

The B405 contains a series resonant crystal oscillator circuit and a pulse-shaping buffer amplifier which produces standard 40-nsec pulses. The frequency, specified by the customer, can be between 2 and 10 mc. The frequency is stamped on the crystal.

B602 Pulse Amplifier
The B602 contains two pulse amplifiers which are used for power amplification, for standardizing pulses in amplitude and width, and for transforming a level change to a pulse.

B681 Power Inverter
The B681 Power Inverter contains four high current inverters, each with separate emitter connections. A 20-mA clamped load is permanently connected to each collector. Four additional 10-mA clamped loads are supplied.

B684 Bus Driver
The B684 contains two dual-purpose, non-inverting bus drivers and a —3 v supply. Each bus driver provides standard levels either to a large number of inverter base and diode loads, or to a terminated 90-ohm cable. All logic terminals are available at the connector. Delay through a bus driver is approximately 30 nsec.

R SERIES

R Series FLIP CHIP modules operate at frequencies from dc to 2 MHz. These modules utilize the diode gate as the basic element of digital logic.

R001, R002 Diode Networks
Diode networks can expand the logic capability of any R-Series, W-Series, or A-Series module which has one or more node inputs, such as the R111 diode gate. They can also make it possible to OR into an R-Series flip-flop output terminal for setting or clearing from several sources.

R107 Inverter
The R107 Inverter contains seven inverter circuits with single-input diode gates. Six of the circuits are used for single-input inversion; the seventh

circuit can be used for gating by tying additional diode input networks to its node terminal. Clamped load resistors of 2 mA are a permanent part of each inverter.

R111 Expandable NAND/NOR Gate
The R111 contains three diode gates, each connected to a transistor inverter. The gate operates as a NAND for negative inputs, and as a NOR for ground inputs. Each gate has three input terminals: two are connected to diodes, a third is connected directly to the node point of the diode gate. The third terminal allows the number of input diodes to be increased by adding external diode networks such as the R001 or R002.

R113, R121 NAND/NOR Gate
The R113 contains five diode gates, each connected to a transistor inverter. The gate operates as a NAND for negative inputs, and as a NOR for ground levels.

The R121 contains four R111-type circuits with 2-mA loads internally connected to each output. This module increases density at the expense of flexibility, since gate expanders R001 and R002 cannot be used.

R122 NOR/NAND Gate
Provides the logical complement to the R121 NAND Gate at some sacrifice of speed and economy.

R123 Input Bus Gate
This module contains six R111-type diode gates arrayed for convenient driving of the PDP-8 computer input bus, and for other matrix-like applications. Clamped loads are not provided on this module, and must be obtained from some module in the associated logic.

R131 Exclusive-OR Gate
This module provides a convenient way to compare two binary numbers or patterns. The output of each circuit is negative if its inputs are the same, and ground if they are different. If the outputs of several circuits are tied together, the common output line will be negative if every input pair matches, ground if any pair doesn't match.

R141 AND/NOR Gate
The R141 AND/NOR Gate performs two levels of gating. The module contains a multiple-input diode gate with a transistor inverter for signal amplification. For negative input signals the R141 is seven 2-input AND gates which are NORed together. For ground inputs, it is seven 2-input OR gates NANDed together. This module is frequently used to mix multiple inputs to a pulse amplifier, or to compare the contents of the two flip-flop registers.

R151 Binary-to-Octal Decoder
The R151 decodes binary information from three flip-flops into octal form. When the enable input is at ground, the selected output line is at ground and the other seven outputs are at −3 v. When the enable input is at −3 v, all outputs are at −3 v. The internal gates are similar to those in the R111. The enable input is the common emitter connection of the output inverters.

R181 DC Carry Chain
The R181 DC Carry module is designed for building counters with no carry propagation delay. A 2-mc counter of any size, with all flip-flops switching simultaneously, can be constructed using dc carry modules.

R200 Flip-Flop
The R200 is a basic flip-flop for use in set-reset applications. It can be set and cleared at any frequency up to 2 mc. A set input makes the 1 output go to −3 v and the 0 output to ground; a clear input makes the 0 output go to −3 v and the 1 output to ground.

R201 Flip-Flop
The R201 Flip-Flop has direct set and clear inputs and five diode-capacitor-diode (DCD) gates.

R202 Dual Flip-Flop
The R202 Dual Flip-Flop contains two identical flip-flops. Each has a direct clear input, a common set input, and two DCD gates. The R202 can perform in any one of the following applications without additional gating: up counter, down counter, shift register, ring counter, jam transfer buffer, and switch tail ring counter.

R203 Triple Flip-Flop
The R203 Triple Flip-Flop contains three identical flip-flops. Each flip-flop has a direct clear input and a DCD gate for conditional read-in.

R204 Quadruple Flip-Flop
The R204 Quadruple Flip-Flop contains four flip-flops. Each has direct set and direct clear inputs. Two of the flip-flops share a common direct clear input. The R204 is used in general control applications.

R205 Dual Flip-Flop
The R205 contains two identical flip-flops with a common direct clear input. Each has three DCD gates, and can be collector-triggered at either output by a diode-transistor gate or a diode network. The R205 can be used in any of the following applications without additional gating: up counter, down counter, shift register, ring counter, or jam transfer register.

R302 Delay
The R302 contains two delays (one-shot multivibrators) which are triggered by DCD gates. Each delay is independent and can be externally or internally controlled. When the input is triggered, the output changes from its normal ground level to −3v for a predetermined, adjustable period of time and then returns to ground.

R303 Integrating One-Shot
The R303 contains a zero recovery time multivibrator and complementary output buffers. Its unusual characteristics include the ability to respond to inputs even while in the ONE state, so that successive inputs above a preset frequency can postpone the return to ZERO indefinitely. This characteristic can be used, for example, to detect gaps in an otherwise continuous pulse, train, or to determine whether an input pulse rate is above or below a preset frequency threshold. If the delay setting of this module exceeds the time it takes +10 and −15 to reach 90% of their final values on power turn-on, this module will initially go to the ONE state. The above conditions allow the R303 to be used for system initialization on power turn-on.

R401 Variable Clock
The R401 Variable Clock is a gateback clock that produces standard 100-or 400-nsec pulses from a stable RC-coupled oscillator. The variable clock is often used as a primary source of timing for large systems.

The frequency of the R401 Clock is variable from 30 cps to 2.0 mc. Five capacitors provide coarse frequency control, and a built-in 20,000 ohm po-

tentiometer permits fine adjustment. Terminals for an external potentiometer or capacitor are available. The maximum size of the external potentiometer to be used is 20,000 ohms.

R405 Crystal Clock
The Type R405 employs a series resonant crystal oscillator, squaring circuit, and output pulse amplifier. The crystal clock's output frequency remains within 0.01% of specified value between 0°C and +55°C. The clock frequency is specified anywhere in the 5 kc to 2 mc range by the customer and is stamped on the crystal can.

R601 Pulse Amplifier
The R601 is a pulse amplifier that standardizes pulses in amplitude and width. Outputs may be either standard 100- or 400-nsec pulses (—3v to ground). It has six DCD gates so that inputs from as many as six sources may be mixed. Input pulses can occur at any frequency up to 2 mc for 100-nsec pulse outputs and up to 1 mc for 400-nsec outputs. Delay through the pulse amplifier is approximately 50 nsec.

R602, R603 Pulse Amplifiers
The R602 and R603 contain pulse amplifiers for power amplification and for standardizing pulses in amplitude and width. Each amplifier produces standard 100-nsec pulses and one section of the R602 can also produce 400 nsec pulses. DCD gates and a single diode input permit inputs from many sources to be mixed. Input pulses can occur at any frequency up to 2 mc for 100 nsec pulses, and up to 1 mc for 400 nsec pulses. Delay through the pulse amplifier is approximately 50 nsec.

R650 Bus Driver
The R650 contains two inverting bus drivers for driving heavy current loads to either ground or negative voltages. The four input terminals make the R650 a versatile logic element as well. The diode inputs D and E (N and P) are the principal inputs. They form a NAND gate for negative inputs or a NOR gate for ground inputs.

W SERIES

The W Series provides input/output compatibility between FLIP CHIP modules and other digital devices.

W002, W005 Clamp Loads
The W002 contains 15, 2-mA clamped loads. These can be used for clamping voltages at the output of inverter collectors in R-Series modules, or for converting B-Series modules to work with R-Series.

The W005 contains 15, 5-mA clamped loads. These can be used for clamping voltages at the output of inverter collectors in B-Series modules, or for converting R-Series modules to work with B-Series. Two of these clamped loads in parallel are equivalent to one B-Series clamped load.

W040, W043 Solenoid Drivers
These high current drivers can drive relays, solenoids, stepping motor windings, or other similar loads. The output levels are −2 volts and a more negative voltage determined by an external power supply. One terminal of the load device should be connected to the external power source, the other to the

driver output. There are two drivers per module and both modules use the same pin connections.

W042 10 Amp Driver
This module has four germanium transistor drivers each capable of providing up to ten amperes of DC drive at ambients up to 40°C for heavy loads such as paper tape punches, card punches, hydraulic servo valves, or high-torque stepping motors like Responsyn (T.M. United Shoe) or Slo-Syn (T.M. Superior Electric). In 55°C ambients up to 8 amps total current may be obtained. AMP "Faston" tabs at the handle end of the module provide high current connections for ground, ES, and the four outputs and external ground.

W050 30 mA Indicator Driver
The W050 contains seven transistor amplifiers that can drive miniature incandescent bulbs, such as those on an indicator panel. It is used to provide remote indicators for R- or B- Series flip-flops. If the input is at −3v, the output is at −1v.

W051 100 mA Indicator and Relay Driver
The W051 contains seven inverter amplifiers suitable for driving indicators, relays and other medium power devices. The amplifiers can supply up to 100 mA at ground, and each output is diode clamped to 15 v to prevent overvoltage when the current is interrupted in an inductive load. If the input is at −3v, the output is at ground. Typical delay for circuit alone: 1 microsecond.

W061 Relay Driver
The W061 Relay Driver has four all-silicon 250 mA drivers with gateable inputs; it can drive relays and solenoids with positive voltage supplies up to 55v. Typical delay for circuit alone: 1 microsecond.

W500 High Impedance Follower
High impedance signal sources such as photocells and low current instrumentation amplifiers can drive Schmitt Trigger W501 or logic gates through a W500 circuit. The module contains 7 fault-protected circuits, each comprising two cascaded emitter-follower amplifiers. Input voltage excursions up to ±30v or short-circuits from output to ground are harmless. Outputs can go as negative as −15v with very light loading, but will not exceed −10v when driving a W501 input.

W501 Negative Input Converter and Schmitt Trigger
The W501 contains a Schmitt trigger circuit which produces standard levels as a result of some outside activity such as the closure of a switch or relay. A ground level input produces a −3v level output, and a negative level input produces a ground level output.

W510 Positive Input Converter
The type W510 Positive Level Converter contains three circuits that convert positive levels to DEC standard levels of ground and −3v. Each circuit consists of a grounded-emitter inverter with a diode string between its input and the base of the inverter.

W511 Negative Input Converter
The type W511 Negative Level Converter contains two circuits that convert negative levels to DEC standard levels of ground and −3v. Each circuit consists of a grounded emitter inverter with a string of bias diodes between its base and the input pins.

W512 Positive Level Converter
Positive logic systems, such as those being monolithic integrated circuits, can use the W512 to make available standard accessory modules in the W and A Series.

W520 Comparator
This module is useful as an inexpensive comparator for A/D work, or as a general-purpose input level converter. The W520 contains three four-transistor difference amplifiers which give DEC standard levels at the output. The state of the output is determined by the relative polarity of the input voltages.

W532 Dual AC-Coupled Difference Amplifiers
The W532 contains two AC-coupled differential amplifiers for use with many magnetic sense systems, including the H201 core memory. These amplifiers provide the high differential gain and common mode noise rejection necessary to amplify information signals in a system using a single sense line per plane for a memory or per channel for a tape system.

W533 Dual Rectifying Slicer
This module is used to detect amplified magnetic system sense signals from a W532 and convert them to positive DEC pulses. Detection of signals as narrow as 100 nsec is possible over a wide range of detection thresholds. There are two slicer circuits on each W533. Two input terminals per circuit permit rectification so that bipolar difference signals can be sliced and standardized.

W600 Negative Output Converter
The W600 contains three inverting amplifiers that convert standard levels to outputs of ground and an externally supplied negative voltage. The external clamp voltage is applied to terminal F (M, T) and must be between −1 and −15v. Additional inputs may be added by tying diode networks, such as those contained on the R001 or R002, to the node terminal.

W601 Positive Output Converter
The W601 contains three amplifiers for converting DEC standard levels to outputs of ground and an externally supplied clamp voltage level, E_c. This external clamp voltage is applied to terminal F (M) and must be between +1 and +20v. Additional inputs can be added by tying diode networks, such as the R001 or the R002, to the node terminal.

W602 Bipolar Output Converter
For driving EIA standard communication lines and other applications demanding levels both positive and negative with respect to ground the W602 provides up to 15 mA at up to 6 v. There are three inverting amplifiers on the module.

W603 Positive Level Amplifier
Positive logic systems such as those using RTL, DTL, or TTL monolithic integrated circuits can be driven from FLIP CHIP systems through the W603. Clamped load resistors at the output of each circuit permit output levels to be adjusted to the type of circuit being driven.

W607, W640 Pulse Output Converters
These pulse converters were designed primarily to facilitate the use of FLIP CHIP modules in conjunction with Digital Laboratory and System Modules. In addition, the W607 can be useful in setting or clearing B Series unbuffered flip-flops via inverters such as B104 or gates such as B113.

W690 DEC to IBM N Line Converter
Each of the four inverting drivers on this module provides outputs compatible with the three types of IBM N lines, depending upon what output currents are programmed by grounds or open circuits at pins T and U. Node points are provided at each input. Maximum delay: 100 nanoseconds driving N transmission lines.

W700 Switch Filter
The W700 contains six switch filters for reducing contact closures to standard levels. The output drive of the switch filter is determined by the voltage to which the switch contact is returned.

W705 +3.6V Power Supply
This inexpensive power supply is of primary use in conjunction with the W706 and W707 teletype modules. The output can supply up to 1.5 amps at a nominal voltage of 3.6 volts. Voltage regulation for variable loading is provided and output ripple is less than 40 mv.

W706 Teletype Receiver
The W706 Teletype Receiver is an integrated-circuit, serial-to-parallel Teletype code converter, self contained on a double-height module. This unit includes all of the serial to parallel conversion, buffering, gating and synchronizing necessary to transfer information between an incoming asynchronous serial teletype line and a parallel binary device. Either a 5 bit serial character consisting of 7.0, 7.5 or 8.0 units or an 8 bit serial character of 10.0, 10.5 or 11.0 units can be assembled into parallel form by the W706 through the use of selective jumpers on the module.

W707 Teletype Transmitter
The W707 Teletype Transmitter is an integrated circuit parallel to serial teletype code converter, self contained on a double-height module. This unit includes all of the parallel to serial conversion, buffering, gating, and timing necessary to transfer information in an asynchronous manner between a parallel binary device and a serial teletype line. Either a 5 bit or 8 bit parallel character can be assembled into a 7.0, 7.5 or 8.0 unit serial character or a 10.0, 10.5 or 11.0 unit serial character, respectively, by the W707 through the use of selective jumpers on the module.

W708 Teletype Interface
The W708 provides special gating controls and clock synchronization for teletype and data communications systems when used with the W706 and W707 teletype modules. Such system features as half duplex operation, half unit start bit spike rejection and single clock operation are possible when W706, W707 and W708 modules are used in a system.

W800 Relay
The W800 Relay consists of two separate Form A reed relays, each with an optional protecting circuit. The type W800 is used to drive heavy loads on computer or logic command. The frequency limit is 100 cps. Maximum relay operating time is 2 msec.

W802 Relay Multiplexer
The W802 Relay Multiplexer contains eight double-pole, normally open reed relays. One of its uses is to address memory lines in memory testers. It can also be used as a low-speed multiplex switch where the grounded, low-noise performance of the A111 multiplexer is not required. Maximum closing time: 1.5 msec; typical opening time: 500 μsec.

computer interfacing modules

M SERIES MODULES FOR COMPUTER INTERFACING

INTRODUCTION

Design and support of interfaces for PDP computers is a major function of M Series modules. This edition of the Logic Handbook emphasizes a collection of modules for interfacing to the following processors:

—PDP-8 Family
- PDP-8/A, 8/E, 8/F, 8/M (OMNIBUS) and External Bus
- PDP-8, 8/I, 8/L, 8/S (Non-OMNIBUS)

—PDP-11 Family
—PDP-12
—PDP-15

This section consists of a separate subsection for each processor. Within each subsection there is a brief overview of interfacing theory, followed by individual descriptions of related modules.

PDP-8 FAMILY COMPUTER INTERFACING

The PDP-8 family of computers remains the undisputed leader in the minicomputer industry with over 20,000 installations to date. Since its inception in 1964, the PDP-8 has been continually improved. Each model has become more powerful, more efficient, and faster. At the same time, system cost and size have been reduced to less than 25 percent of original figures. More importantly, these improvements have been made without sacrificing software and hardware compatibility. Programs written for the earliest PDP-8 can be run on the newest PDP-8; peripheral devices that operated with earlier PDP-8s can be made to operate with the latest PDP-8.

This section contains hardware interfacing information and related I/O module descriptions for all PDP-8 models. For ease in reading, this section is organized into two main subgroups:

—OMNIBUS—PDP-8/A, 8/E, 8/F, 8/M, and External Bus
—Non-OMNIBUS—PDP-8, 8/I, 8/L, 8/S

For historical references, the non-OMNIBUS-related processors preceded the OMNIBUS-structured processors.

PDP-8/A, 8/E, 8/F, 8/M (OMNIBUS) Interfacing

This subsection consists of general interfacing information for the PDP-8/A, 8/E, 8/F, and 8/M processors, followed by detailed descriptions of related modules. In addition, a description is provided for the External Bus option which allows non-OMNIBUS-related devices to operate with the OMNIBUS.

General OMNIBUS Interfacing Principles

The PDP-8/A, 8/E, 8/F, and 8/M are the newest 12-bit word length processors offered by DIGITAL. These processors utilize the OMNIBUS concept for transferring commands and signals among modules within a system.

Physically, the OMNIBUS is an etched board with rows of module connectors soldered to the board. The pin assignment is the same on all connectors. The OMNIBUS consists of 96 signals which feed to 96 pins on the connectors. The user is generally only concerned with those signals that control data transfers, address memory, or contain the data to be transferred. However, the additional signals, such as timing, are readily available on the OMNIBUS to accommodate any tailor-made requirement in the event that the user

should design and build his own interface module. A single OMNIBUS assembly accommodates 20 PDP-8/A, 8/E, 8/F, or 8/M modules.

The OMNIBUS bus structure employs bidirectional data and control lines plus a few undirectional control signals. Each bus line is a matched and terminated transmission line that must be received and driven with devices designed for that specific application. All M Series modules designed for interconnections to the OMNIBUS employ special high-impedance bus driver and bus receiver circuits appropriate for such bus lines. All drivers (identified by a "D" in the logic symbol) are open-collector gates that control the bus through a wired-OR connection. All receivers (identified by the "R" in the logic symbol) are high-impedance gates that present a minimum of loading to the bus line.

A module may have unused bus driver or bus receiver circuits that can be used with TTL devices, provided the following loading rules are observed:

Receiver Loading: The bus receiver input presents two TTL unit loads (in the High state) to a TTL output and has a normal fan-out of 10.

Driver Sink Capability: The open-collector bus drivers are capable of sinking at least 50 mA, with a collector voltage of 0.8 volts or less. The collector voltage, when not sinking current, must be less than +6 volts. Leakage current (in the High state) is less than 25 μA. The input of a bus driver presents a single TTL unit load to a TTL output.

There are three types of data transfer: programmed data transfers, program interrupt transfers, and direct memory access transfers. Programmed data transfer is the easiest and most direct method of handling data I/O. Program interrupt transfers provide an extension of programmed I/O capabilities by allowing the peripheral device to initiate a data transfer. The data break system uses direct memory access for applications involving the fastest data transfer rates.

Table 1 lists and describes the signals on the OMNIBUS-related processors that are used for programmed and interrupt I/O control. More complete descriptions for these and data break transfer signals are contained in the SMALL COMPUTER HANDBOOK.

Table 1. OMNIBUS I/O Signal Summary

SIGNAL	DEFINITION
MDO-11	Contains the device select code for an I/O instruction. Bits 3-8 contain the device select code; bits 9-11 specify the operation select code within that device.
I/O PAUSE L	Asserted by the processor when the instruction is an I/O instruction ($6XXX_8$).
TP3H	TP3H is normally used to clock data into the output buffer of an output interface.
INTERNAL I/O L	INTERNAL I/O is asserted by the interface to indicate to the processor that the selected device is not on the External I/O Bus.

Table 1. OMNIBUS I/O Signal Summary (Continued)

SIGNAL	DEFINITION
DATA0-11	The 12 DATA lines called DATA BUS serve as a bidirectional bus for both input and output data between the AC register in the processor and the interface buffer register.
C lines C0, C1, C2	Signals C0, C1, C2 are asserted by the interface during I/O instructions to notify the processor whether data is to be placed onto the DATA BUS or received from the DATA BUS by the processor.
INT RQST L	INT RQST is the method by which the device signals the processor that it must be serviced. The processor will then branch to a subroutine which issues a skip IOT to each device to identify the one that is interrupting.
SKIP L	Asserted by the interface as the result of a skip IOT if an interrupt is being requested. Used to identify the interrupting device by causing the processor to skip the next instruction.
BUS STROBE L	BUS STROBE is used to load the AC and PC registers. Unless special I/O operations are being performed, the designer of an interface need not concern himself with BUS STROBE.
NOT LAST XFER L	A ground level on this line indicates to the processor that the next BUS STROBE does not terminate the I/O transaction. Typical I/O tranfers will not use this signal.
RUN L	When low, RUN indicates that the machine is executing instructions. Can be used to notify an interface that the processor has stopped.
TS1 L TS2 L TS3 L TS4 L TP1 H TP2 H TP3 H TP4 H	These are the internal machine cycle time states and time pulses. Each time state precedes its corresponding time pulse. Time states are always 200 ns or more in duration, and change 50 ns after the leading edge of the time pulse. Time pulses are 100-ns positive-going pulses. The exact spacing of the timing pulses is a function of fast or slow cycle. Only TP3H is used in the typical interface.
INITIALIZE H	INITIALIZE is a positive-going 600-ns pulse used to clear AC, LINK, and flags in peripherals. It is generated when power is first applied to the processor, by the Clear key on the console and by IOT 6007.

The following is a brief summary of the basic sequence of I/O transactions for programmed data transfers and interrupt data transfers. This information is provided here as a general reference aid; detailed descriptions are contained in the SMALL COMPUTER HANDBOOK.

For programmed data transfers, the computer program issues an input/output instruction to, first, select the desired peripheral and, second, direct the peripheral to generate certain operating control signals called IOTs. The input/output instructions are transmitted to the peripheral via the MD (Memory Data) lines 00 through 11. Each peripheral contains circuitry that monitors the MD lines. MD03 through MD08 carry a device selection code which is unique for each peripheral. Lines MD09 through MD11 carry command operate signals that the selected peripheral must translate into one of eight IOT functions for that device. Signal I/O PAUSE is also generated by the processor at this time. I/O PAUSE notifies all peripherals that the MD lines contain an I/O instruction. Note that the interface does not have to monitor MD lines 0-2 to detect a 6₈. I/O PAUSE occurs after the MD lines have settled and is used to actually gate the device select and the operation codes into the interface.

The IOT functions vary depending upon the type of peripheral but generally, they consist of sampling and clearing status flags and reading, loading, and clearing data buffers. For data inputs into the processor, the interface bus drivers are enabled by the appropriate IOT. For data outputs from the processor, the IOT is gated with TP3 H and the resulting signal is used to load the desired output register. The Control lines (C0, C1, C2) must be configured by the device interface during an I/O instruction to notify the processor of the type of transfer that will occur between the device and the processor. These lines control the data path within the processor and determine if data is to be placed onto the data lines (output) or received from the data lines (input). The INTERNAL I/O signal must also be generated to notify the processor that an extended cycle is not needed.

The interrupt facility is a more efficient method of I/O transfer. This method includes all of the above elements of programmed data transfers except the time of transfer. Instead of waiting for the processor to check the peripheral, the peripheral signals the processor that it has data to be serviced by asserting the INT RQST line. The processor interrupt system detects the INT RQST signal and enters a subroutine to determine the identity of the requesting device by sending an I/O instruction to each peripheral which causes the SKIP line to be asserted if the peripheral is asserting the interrupt signal. When this identity has been established, a servicing subroutine causes the peripheral to enter a normal programmed data transfer sequence.

External Bus

The External Bus provides an extension of the OMNIBUS system which allows interfacing non-OMNIBUS PDP-8 family *positive-bus* equipment with the PDP-8/A, 8/E, 8/F, or 8/M. The external bus was specially designed to make the OMNIBUS operate like the positive-bus PDP-8/I and PDP-8/L computers. Many modules and peripheral controllers developed for this positive-bus structure are in demand and are fully supported by DIGITAL.

The external bus consists of a number of signal lines (88 excluding grounds) that enable data transfers between the CP and peripherals. These lines carry data and control signals between the peripheral and two interface boards—the Positive I/O Bus interface (KA8-A) and the Data Break interface (KD8-E)—that plug into the OMNIBUS. These two boards convert the internal OMNIBUS signals into PDP-8/I and PDP-8/L *type bus* signals. For instance, PDP-8/I peripherals need IOP pulses to perform instructions. The PDP-8/E does not generate internal IOP pulses, but it does provide signals (MD bits 09, 10, and 11) that can be converted into IOP pulses by the Positive I/O Bus interface. Other signals normally required by these peripherals are, in essence,

available on the OMNIBUS. For example, BAC (buffered accumulator) bits must be supplied for the PDP-8/I peripherals. The PDP-8/E Data lines carry the necessary accumulator information. The Positive I/O Bus interface merely buffers the DATA bits and, thus, provides the external bus BAC signals.

Although the external bus consists of signal lines from both the positive I/O Bus interface and the Data Break interface, it is not always necessary to use both boards. When only programmed I/O transfer peripherals are used, the Positive I/O Bus interface provides all the necessary signals. However, if data break peripherals are to be connected, both interfaces must be used. Because each data break peripheral requires its own data break interface board, the number of signal lines comprising the bus may vary. There may be as many as 12 of these data break peripherals connected in the system, each contributing 36 signal lines to the external bus. Figure 1 illustrates the details of an external bus interface. The signals of the external bus are defined in Table 2. Descriptions of general purpose interfacing modules that can be used with the external bus are provided in the non-OMNIBUS-related modules section (positive bus).

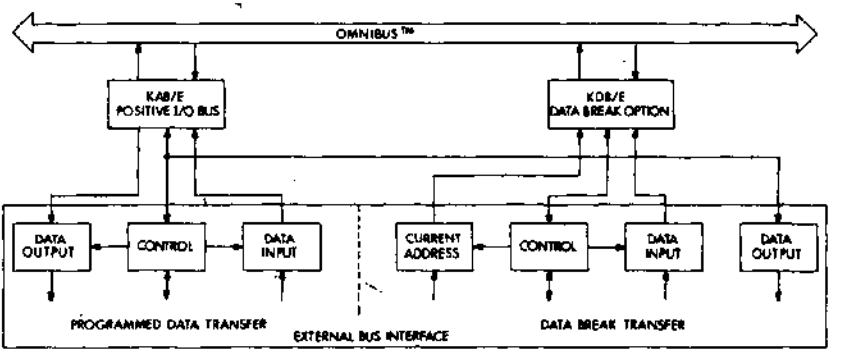


Figure 1. External Bus Interfacing

Table 2. External I/O Bus Signal Summary.

SIGNAL	DEFINITION
B Initialize	This line is asserted when the processor is initially powered up or when the start key is depressed. Usually performs housekeeping on all peripheral devices—for example, resets all flip-flops on power up.
AC00-11	These lines carry information from the peripheral device to the accumulator. (Input)
BAC 00-11	These lines carry information from the accumulator to the peripheral devices. (Output)
BMB 00-11	These lines carry the device identifier code, a unique address to which only one device will respond.
INTERRUPT REQUEST	This line is activated by the device flag and, when asserted, causes the processor to JMS to location 0 of memory field 0 and disables the interrupt system. (Input)
BIOP 1	This line, when active, is ordinarily used to test device flags. (Output)
SKIP	This line, when active during an IOP, will cause the processor to skip the next instruction.
BIOP 2	This line, when active, is ordinarily used to clear the device flag and/or cause the device to operate. (Output)
CLEAR AC	This control line, when asserted, changes the mode of I/O input transfer to a jam transfer. (Input)
BIOP 4	When active, is ordinarily used to effect data transfers to or from the peripheral devices. (Output)
B Run	When active, signals peripheral devices that the processor is executing instructions. (Output)
BTS1 and BTS3	These lines are used to sync peripheral devices to the processor. (Output)

OMNIBUS-Related Interface Modules
Detailed descriptions for the following modules are contained here:

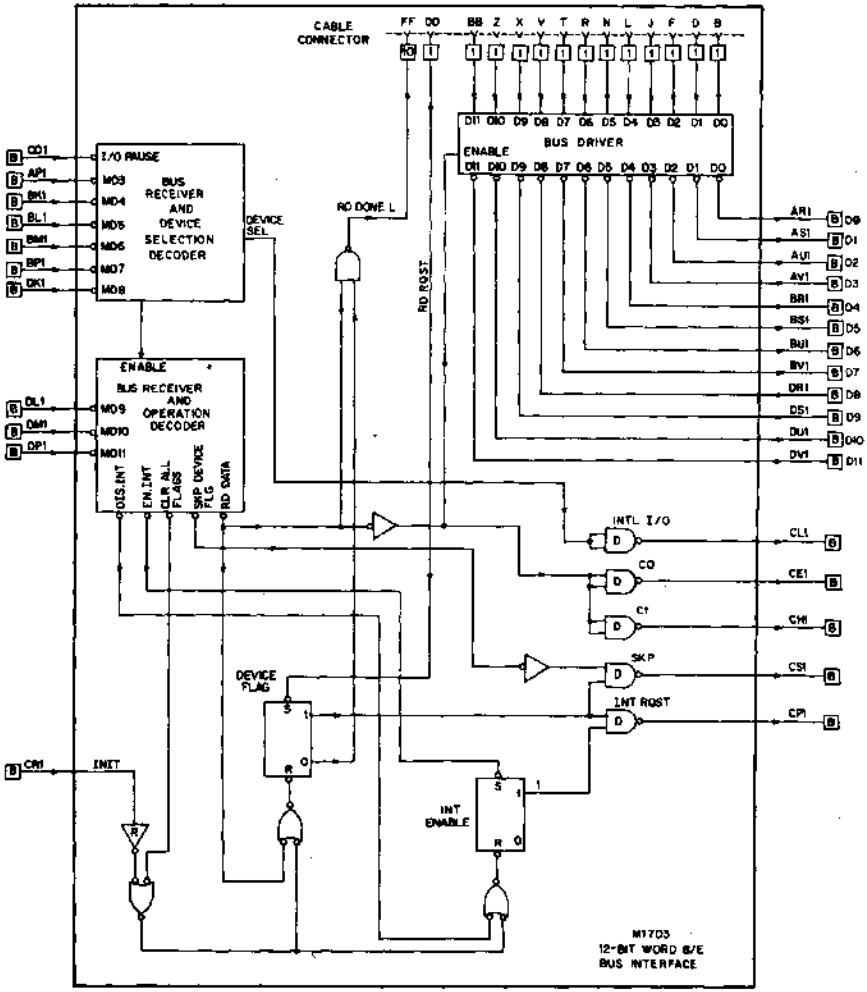
M1703 Input Interface Module
M1705 Output Interface Module
M1709 Interface Foundation Module
W966 Wire Wrappable Module
W967 Wire Wrappable Module (w/IC sockets)

M1703
OMNIBUS INPUT INTERFACE

PDP-8/E, 8/M OMNIBUS

M SERIES

Length: Extended
Height: Quad
Width: Single



Volts	Power mA (max.)	Pins
+5	555	AA2, BA2, CA2
GND		AC2, BC1, BC2, CC1, CC2, DC1, DC2
		AN1, AN2, BN1, BN2, CN1, CN2, DN1, DN2
		AT1, AT2, BT1, BT2, CT1, CT2, DT1, DT2
		AF1, AF2, BF1, BF2, CF1, CF2, DF1, DF2

DESCRIPTION

The M1703 provides, on a single quad-height module, a complete, self-contained interface that will input 12 bits of parallel TTL-level data to the PDP-8/A, 8/F, 8/E or 8/M OMNIBUS, under interrupt or programmed I/O control. The M1703 plugs directly into the OMNIBUS connector assembly, and the external device plugs into a 40-pin flat cable connector on the module itself. The module includes a device selector, an operation decoder, flags, and all control logic needed to request interrupt and respond to programmed I/O commands on the OMNIBUS. Command codes assigned to this module include:

ENABLE AND DISABLE INTERRUPT
CLEAR FLAGS
SKIP IF DEVICE FLAG SET
READ DATA

A device selection code of 14 (octal) is assigned to this module but the code can be changed by moving wire jumpers.

FUNCTIONS

Device Selection Decoder: The device is addressed through this decoder when I/O PAUSE is asserted and the octal device code for the decoder is received through <MD03:08>. The decoder output asserts the INT. I/O line and enables the operation decoder.

Operation Decoder: The select bits (MD09, 10 and 11) determine the type of operation to be performed when the operation decoder is enabled by the device selection decoder.

DATA <00:11>: Data from the external device is applied to the bus drivers on these lines. A READ DATA command enables the bus drivers and asserts C0 and C1, thereby entering the data into AC0-11 via corresponding OMNIBUS data lines.

READ RQST: When the external device is ready to input stable data, it applies a logic LOW for at least 50 ns on this control line, to set the DEVICE FLAG. READ DONE goes HIGH within 60 ns after READ RSQT goes LOW.

DEVICE FLAG: After being set by a LOW on the RD RQST line, this flag initiates an interrupt request (if INTERRUPT is enabled). This flag is sensed by the SKIP control line.

INTERRUPT RQST: When this line is asserted by the DEVICE FLAG, an interrupt request is sent to the computer which responds by executing a JMS0 instruction.

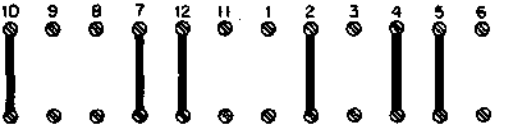
INTERRUPT ENABLE: This flip-flop is set to enable and cleared to disable the interrupt request function.

SKIP Control Line: If the device flag is set, the instruction SKIP ON DEVICE FLAG asserts the SKIP line, incrementing the contents of the computer's program counter.

READ DONE: This line stays HIGH as long as the DEVICE FLAG is set, and signals the end of a data transfer by going LOW after the end of a RD DATA pulse.

Changing the Device Code: The device selection decoder is preset for a device code of 14 octal. However, split lugs on this module permit the code to be changed by the user to any octal number from 00 to 77. To obtain the

desired octal number, jumper the split lug pairs that select the binary equivalent of the device code, as shown below:



A. PHYSICAL LAYOUT OF SPLIT LUGS (SHOWING JUMPERS FOR DEVICE CODE 14 OCTAL)

ADD JUMPER AT:	DEVICE CODE					
	8^1			8^0		
	2^2	2^1	2^0	2^2	2^1	2^0
BIT = 1	1	3	5	7	9	11
BIT = 0	2	4	6	8	10	12

EXAMPLE

0	0	1	1	0	0	BINARY EQUIV. OF 14 OCTAL CODE
2	4	5	7	10	12	REQUIRED JUMPERS

B. DETERMINING JUMPERS FOR NEW CODE ASSIGNMENTS

IOT INSTRUCTION ASSIGNMENTS

Octal Code	Instruction	Purpose
6140	Disable Interrupt	Clears the INTERRUPT ENABLE flag to disable the *INT* RQST line
6141	Enable Interrupt	Sets the INTERRUPT ENABLE flag to enable the INT RQST line
6142	Clear Flags	Clears the DEVICE FLAG, asserts READ DONE and clears INTERRUPT ENABLE flag
6143	Skip if Device Flag Set	Asserts the SKIP line if the DEVICE FLAG is set. The computer responds by incrementing the program counter so that the next instruction is skipped.
6144	Read Data	Transfers input data bits <00:11> to <AC00:11> through the OMNIBUS data lines. Also clears the DEVICE FLAG, allowing the RD DONE output to go LOW when the data transfer is complete.

SPECIFICATIONS

Propagation Time:

FROM	TO	ns (max.)
LOW on RD RQST input	RD DONE going HIGH	60

M1705
OMNIBUS OUTPUT INTERFACE

OMNIBUS

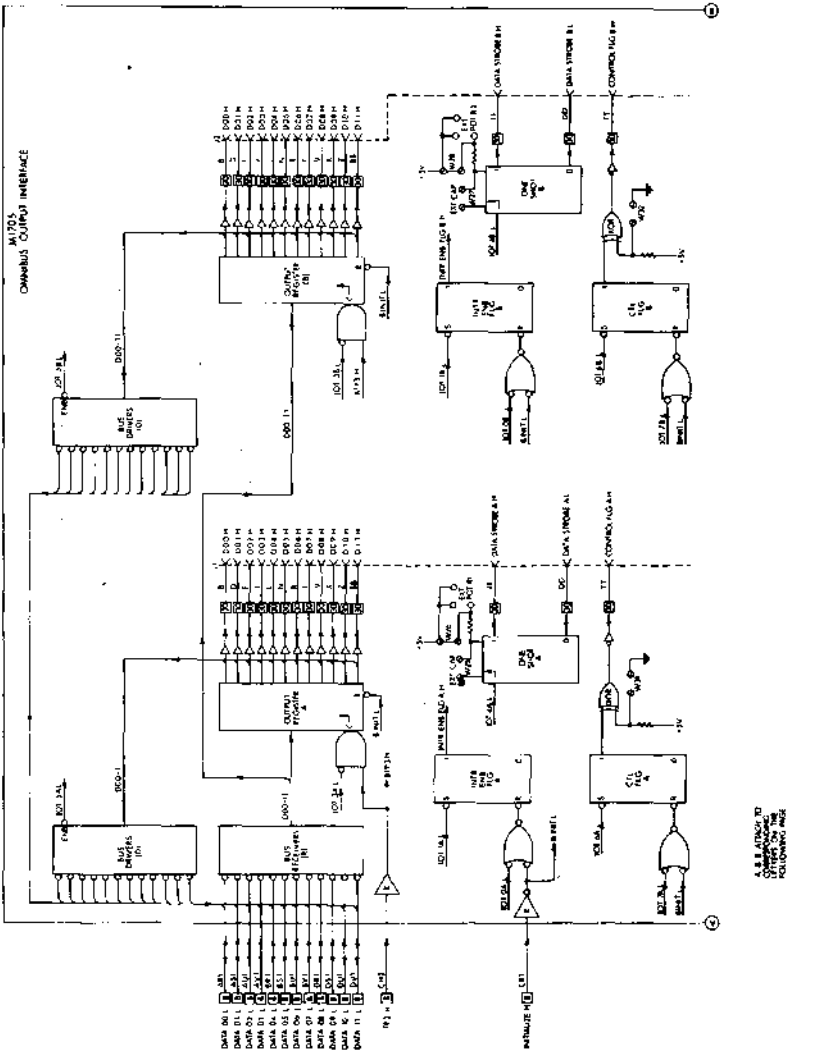
M SERIES

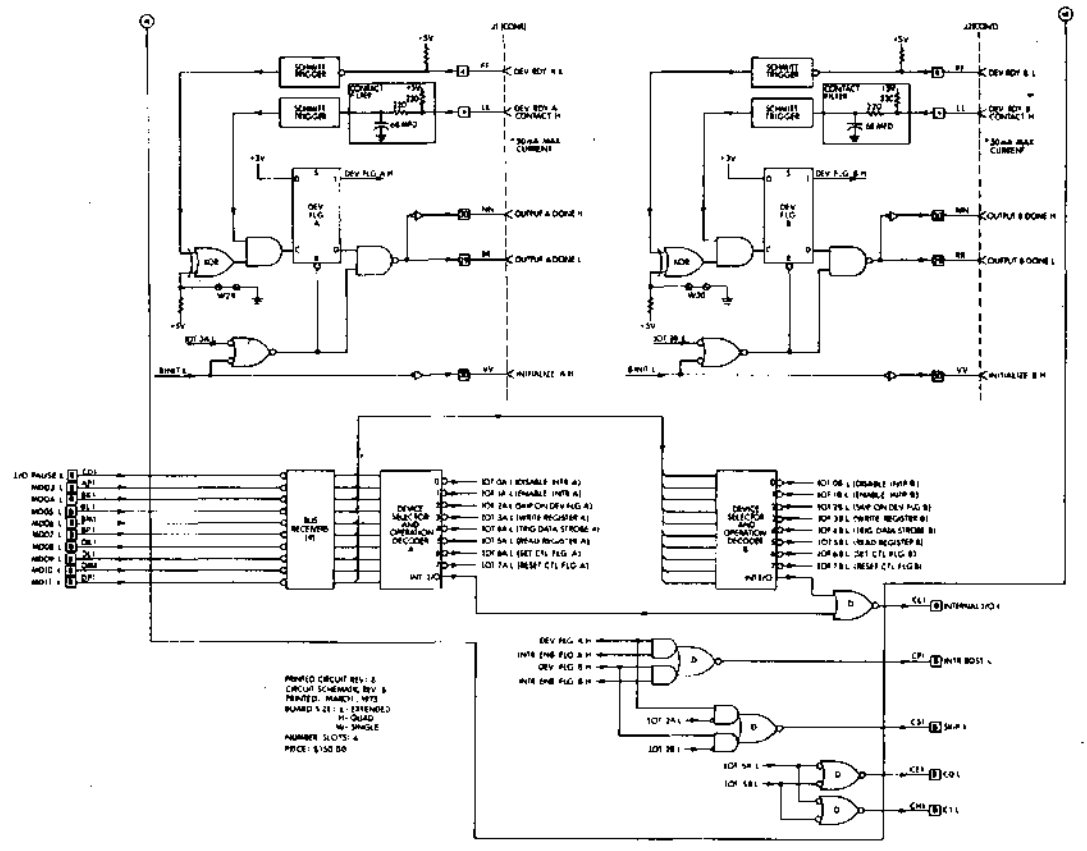
Length: Extended
Height: Quad
Width: Single

Volts
+5
GND

Power
mA (max.)
1.15A

Pins
AA2, BA2, CA2
All pins F, T, N, AC2, BC1, BC2, CC1, CC2, DC1, DC2




SCHMITT TRIGGER
DEV RDY A L
DEV RDY A CONTACT H
DEV FLG A H
OUTPUT A DONE H
OUTPUT A DONE L
INITIALIZE A H
DEV RDY B L
DEV RDY B CONTACT H
DEV FLG B H
OUTPUT B DONE H
OUTPUT B DONE L
INITIALIZE B H
I/O PAUSE L
BUS RECEIVERS (H)
DEVICE SELECTOR AND OPERATION DECODER A
DEVICE SELECTOR AND OPERATION DECODER B
INTERNAL I/O L
INTR BOOST L
SKIP L
CLR L
CTL L
PRINTED CIRCUIT REV: E
CIRCUIT SCHEMATIC, REV. B
PRINTED: MARCH, 1973
BOARD TYPE: E - EXTENDED
H - QUAD
M - SINGLE
NUMBER SLOTS: 4
PRICE: $150.00

DESCRIPTION

The M1705 is an output interface module that allows the PDP-8 computer to transfer data to, and control the operation of, remotely programmable instruments or similar digital devices. The function is to perform parallel transfers, under program or interrupt control, of 12-bit data words from the computer to peripheral devices.

The M1705 consists of duplicate logic sections. Each section includes device selection logic to address an external device, an operations decoder to determine the type of interface operation, a 12-bit storage register to buffer the output data, interrupt control logic, and bus drivers/receivers to allow operation on the OMNIBUS. Connection to the device(s) is made via standard cables that plug into a pair of connectors on the M1705 module board.

FEATURES

- Complete single-card OMNIBUS output interface
- Data storage registers
- Program interrupt capability
- Cable drivers on all output signals, diode-protected
- Compatible with M1703 OMNIBUS Input Interface
- TTL-compatible signals
- Diode-protection/pulse-shaping on all input signals
- Peripheral I/O cables plug directly onto M1705 card
- Variable pulse width control signals
- User-assigned device codes—jumper selected
- Many user-selected control functions—assertion levels, both TTL and contact closures.

APPLICATIONS

The M1705 OMNIBUS Output Interface is suitable for a variety of scientific and industrial applications which require parallel TTL-compatible data to be output from a PDP-8/E family computer. Its dual word (24-bit) digital output and data storage capability make it a natural for the remote programming of instruments such as digital voltmeters (DVMs), digital multimeters (DMMs), RLC bridges, programmable power supplies and many more.

The M1705 finds application in the scientific and industrial laboratory as a general-purpose digital (TTL) output interface. The control of experimental equipment and the driving of strip chart recorders are only two of the many possible laboratory uses.

Its cable-driving capabilities make the M1705 a fine choice for interprocessor communication. When used with the M1703 OMNIBUS Input Interface, the M1705 provides the capability of communicating at high speed with one or more PDP-8/E family computers. Additionally, the M1703 Input and M1705 Output Interfaces may be combined at one computer to form a general-purpose digital input/output interface system. The result is a very flexible, low-cost system that may be readily expanded. This type of system is often required for the control of, and collection of data from, programmable instruments, production line machinery, lab experiments, and custom peripheral devices (X-Y recorders, card readers, mag tape drivers, etc.).

FUNCTIONS

Device Selection Decoder (A, B)
External devices are addressed through one of two identical Device Selection Decoders. This allows external devices to be handled separately if desired. Each decoder is activated when I/O PAUSE is asserted by the processor and the octal device code for that decoder is received through bits MD03-MD08. Decoders A and B are factory-assigned octal device codes 15 and 16 respectively. However, any octal code from 01 to 77 is selectable by the user via split lug jumpers. The decoder output asserts the INTERNAL I/O line and enables an operation decoder.

Operation Decoder (A, B)
The Operation Decoder decodes the three operation bits MD09-MD11 from the OMNIBUS to determine the type of operation to be performed. The appropriate operation decoder (A or B) is enabled by its respective Device Selection Decoder (A or B).

Output Register (A, B)
The data from the processor accumulator (AC) is transferred to one of the two output registers (A or B) via OMNIBUS lines DATA-00-DATA-11. A binary 1 in the accumulator corresponds to a binary 1 in the output register and to a logic HIGH at the register's output. The register output (D00-D11) may be transferred, in parallel, to the device by a Data Strobe pulse. All bits of both output registers are reset to a logic LOW by assertion of the OMNIBUS signal INITIALIZE.

Device Flag (A, B)
This is a flip-flop which is set by the external device signal DEV RDY or DEV RDY CONTACT and reset by the INITIALIZE signal from the processor or by the appropriate IOT 3 (WRITE REGISTER) command). The status of the Device Flag can be interrogated by the IOT 2 (SKP ON DEV FLG) command. Setting this flip-flop initiates the interrupt request if the Interrupt Enable Flag flip-flop is set.

Interrupt Enable Flag (A, B)
This is a flip-flop which is set under program control to enable or disable the interrupt request function on the M1705 module.

Control Flag (A, B)
This is a spare flip-flop which may be used to perform any additional control function at the external device.

I/O Bus Drivers and Receivers
The OMNIBUS receivers and drivers contain special high-impedance circuitry to minimize bus loading.

PROGRAMMING

The following is a list of instructions that are available for use by the programmer.

Octal Code*	Name	Function
6150	Disable Interrupt A	Resets INTR ENB FLG A to disable the Interrupt Request function for Section A.
6151	Enable Interrupt A	Sets the INTR ENB FLG A to enable the Interrupt Request function for Section A.
6152	Skip on Device Flag A	Asserts the SKIP line if DEV FLG A is set.
6153	Write Register A	Clocks the contents of AC00-AC11 into Output Register A. Also, OUTPUT A DONE H becomes a logic HIGH and OUTPUT A DONE L becomes a logic LOW following completion of this instruction.
6154	Trigger Data Strobe A	The trailing edge of the pulse generated by this IOT initiates DATA STROBE A H and DATA STROBE A L pulses.
6155	Read Register A	Transfers the contents of Output Register A to AC00-AC11.
6156	Set Control Flag A	Sets the CTL FLG A flip-flop.
6157	Reset Control Flag A	Resets the CTL FLG A flip-flop.
6160	Disable Interrupt B	Resets INTR ENB FLG B to disable the Interrupt Request function for Section B.
6161	Enable Interrupt B	Sets the INTR ENB FLG B to enable the Interrupt Request function for Section B.
6162	Skip on Device Flag B	Asserts the SKIP line if DEV FLG B is set.
6163	Write Register B	Clocks the contents of AC00-AC11 into Output Register B. Also, OUTPUT B DONE H becomes a logic HIGH and OUTPUT B DONE L becomes a LOW following completion of this instruction.
6164	Trigger Data Strobe B	The trailing edge of the pulse generated by this IOT initiates DATA STROBE B H and DATA STROBE B L pulses.
6165	Read Register B	Transfers the content of Output Register B to AC00-AC11.
6166	Set Control Flag B	Sets the CTL FLG B flip-flop.
6167	Reset Control Flag B	Resets the CTL FLG B flip-Flop.

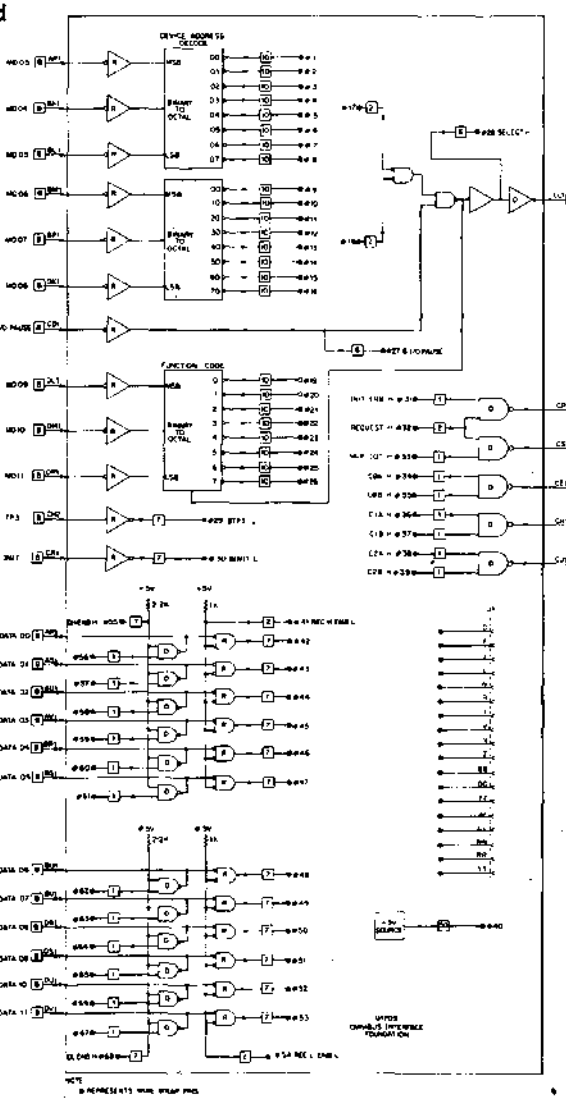
*Device codes 15_8 and 16_8 are factory-selected. Other codes may be chosen by changing jumpers on the M1705 module.

M1709
OMNIBUS INTERFACE
FOUNDATION MODULE

OMNIBUS

M SERIES

Length: Extended
Height: Quad
Width: Single



Printed Ckt. Rev.: B
Ckt. Schem. Rev.: A
Printed: August 1972

Board Size:
L—Extended
H—Quad
W—Single
No. Slots: 4

Volts	Power mA (max.)	Pins
+5	830	AA2, BA2, CA2
GND		All pins C, N, F, and T

DESCRIPTION

The M1709 OMNIBUS Interface Foundation module is a generalized OMNIBUS interface card that is constructed to allow the user to build a custom design using integrated circuits (ICs). All required OMNIBUS interface logic, i.e., bus drivers/receivers, device selectors, and interrupt/skip circuitry is provided. IC mounting pads with wire wrappable pins are made available for custom circuitry. Pads accommodate all common types of Dual-In-Line Pack (DIP) ICs with up to forty pins.

Connection to user-equipment is made via standard cables (BC08R or BC04Z) that plug directly into the M1709 module board. The module cable connector allows several M1709 modules or W966/W967 wire wrappable modules to be strapped together to accommodate more extensive designs.

APPLICATIONS

Since both analog and digital circuitry are available in DIP form, quite complex systems may be built. Some of the typical applications for the M1709 module are:

- Multiword input and/or output
- Instrument interfaces
- Interprocessor communication
- Oscilloscope controller (D/A)
- Peripheral control (data terminals, etc.)
- Interfacing of:
  - A/D converters
  - Multiplexers
  - Counters
  - Shift registers
  - Read-Only Memories (ROMs)
  - Arithmetic Logic Units (ALU)

FUNCTIONS

The preassembled circuitry of the M1709 module can be classified into four categories: Device and Function Selection, Data Bus Interface, Interrupt and Skip Interface, and Control Line Interface.

Device and Function Selection: Device address decoding is performed with a pair of binary-to-octal decoders (3 to 8 line). OMNIBUS lines MD03 through MD08 are decoded and one output of each decoder is ANDed (by wire wrapping) to sense a "device selected" condition. Any code from 01_8 to 77_8 is selectable via wire wrap jumper selection.

The "device selected" condition is, in turn, ANDed with the I/O PAUSE signal to drive the OMNIBUS signal INTERNAL I/O. This signal is also made available at a wire wrap pin as SELECT H.

Function decoding is performed by a binary-to-octal decoder (3 to 8 line). OMNIBUS signals MD09 through MD11 are decoded to form the eight IOT 0 through IOT 7 signals. These TTL signals are made available at numbered wire wrap pins for ease of connection to user-installed IC logic.

Data Bus Interface: The 12 OMNIBUS Data Lines, DATA 00 through DATA 11, are received with special high-impedance circuitry and TTL signals are made available at wire wrap pins. In addition, each data line has a special BUS driver circuit assigned to it. Input to these drivers is available at wire wrap pins and is TTL-compatible for direct connection to user-installed IC logic.

Enabling inputs are provided for both data line receivers and drivers.

Interrupt and Skip Interface: BUS driver circuits are available for driving the OMNIBUS INT RQST and SKIP lines. The INT RQST driver has an enabling input which can be used to inhibit the interrupt request while maintaining the ability to test the interrupt condition via the SKIP facility. Input to these drivers is TTL-compatible and made via wire wrap pins.

Control Line Interface: BUS driver circuits are connected for asserting the three OMNIBUS data transfer mode signal lines—C_0, C_1, C_2. Input to these drivers is TTL-compatible and made via wire wrap pins.

Miscellaneous Interface Signals: OMNIBUS signals TP3 and INITIALIZE are received with high impedance circuits. These signals are made available in TTL-compatible form at wire wrap pins as BTP3 and BINIT, respectively. A source of +3 volts is made available at a wire wrap pin.

OMNIBUS Signals made Available to the User*
In addition to those OMNIBUS signals mentioned previously, the following 40 OMNIBUS signals are made available to the user at wire wrap pins. The complete set of signals available is sufficient to allow the user to accomplish all program transfer and data break interface operations.

OMNIBUS Signal Name	Pin
MA0	AD1
MA1	AE1
MA2	AH1
MA3	AJ1
MD0	AK1
MD1	AL1
MD	AM1
MD DIR	AK2
MA4	BD1
MA5	BE1
MA6	BH1
MA7	BJ1
MD6	BM1
MD7	BP1
INT STROBE	BD2
BRK IN PROG	BE2
MA, MS LOAD CONT	BH2
OVERFLOW	BJ2
BREAK DATA CONT	BK2
BREAK CYCLE	BL2
BUS STROBE	CK1

* These OMNIBUS signals (except ± 15 V) require high impedance/low leakage current driving and receiving circuitry. (Use DEC 8640 and 8881 ICs).

OMNIBUS Signal Name	Pin
NOT LAST XFER	CM1
CPMA DISABLE	CU1
MS, IR DISABLE	CV1
TP1	CD2
TP2	CE2
TP3	CH2
TP4	CJ2
TS1	CK2
TS2	CL2
TS3	CM2
TS4	CP2
LINK DATA	CR2
LINK LOAD	CS2
MA8	DD1
MA9	DE1
MA10	DH1
MA11	DJ1
+15 V	DA2
−15 V	DB2

SPECIFICATIONS

Signals to and from the OMNIBUS are received or driven with special high impedance circuitry to minimize bus loading.

CAUTION

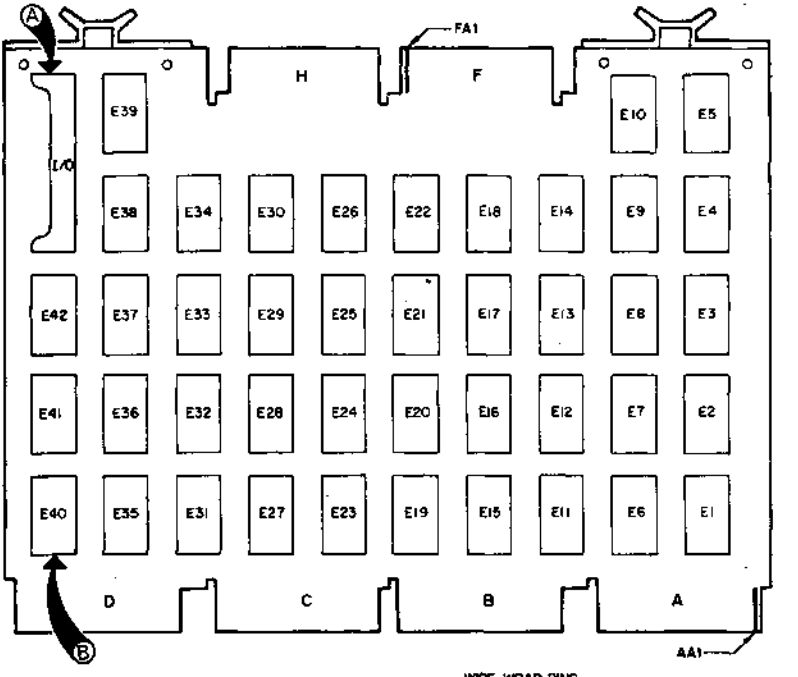
All requirements for timing should be in accordance with the PDP-8/e and -8/m Small Computer Handbook.

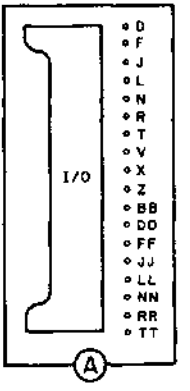
W966
WIRE WRAPPABLE MODULE

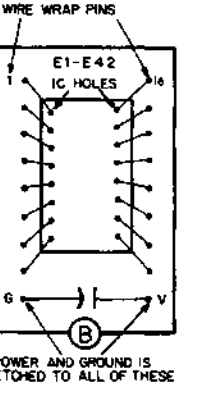
OMNIBUS

W SERIES

Length: Extended
Height: Quad
Width: Single







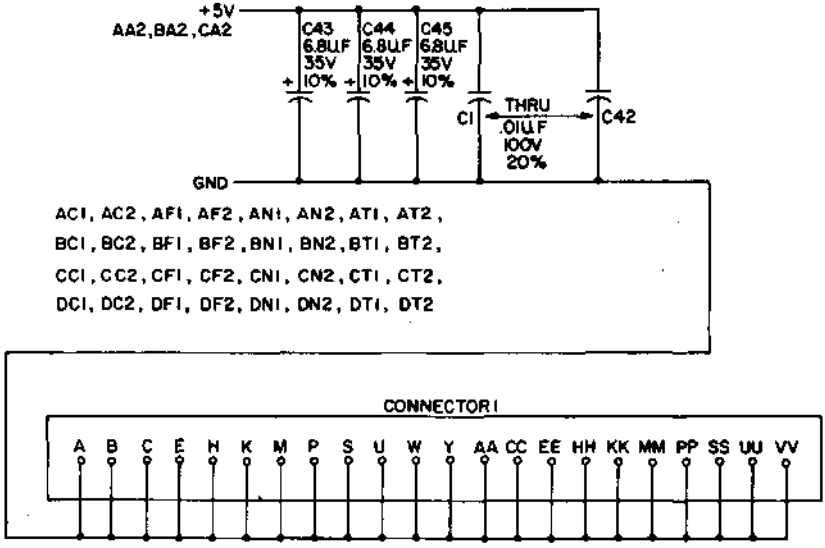
W966 Wire Wrappable Module

DESCRIPTION

The W966 Wire Wrappable Module is a PDP-8/E, 8/F, 8/M general-purpose module that provides for the construction of custom interface designs using integrated circuits (ICs) and wire wrapped interconnections. Up to 42 of 14- and/or 16-pin ICs can be easily mounted (with or without 16-pin sockets) onto the etched IC pads. (Sockets are not supplied.) Each wire wrap pin can accommodate two separate leads of 30-gauge wire. Discrete components may also be directly soldered onto the IC pads. Position E39 features a pad that can be used for mounting a potentiometer.

The W966 has 72 etched contact fingers at the handle end, with a wire wrap pin connected to each finger. When a W966 is located adjacent to another W966, signals can be bused from one module to the other via these contact fingers by using an H851 edge connector. One H851 can bus 36 signals; therefore, two H851s are required to bus all 72 signals. In addition, the standard 144 contact fingers at the connector end of the module are also connected to wire wrap pins.

An H854 40-pin I/O connector (male) is contained on the module to provide access to the "outside world"; it can accept any cable equipped with an H856 connector. Eighteen of these connector pins are connected to wire wrap pins.



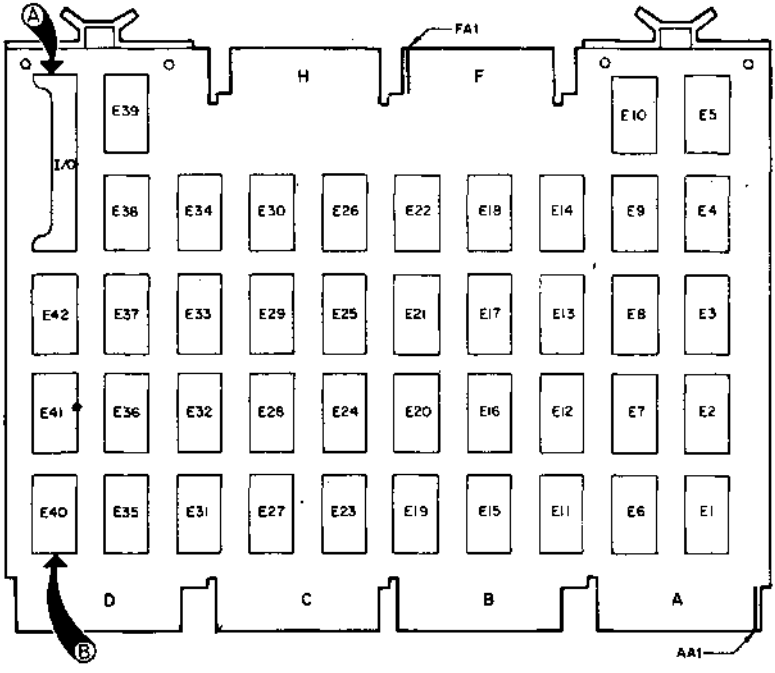
W966 Circuit Schematic

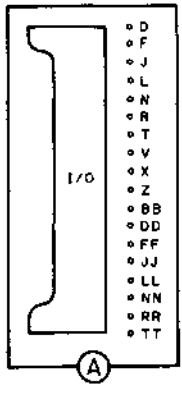
W967
WIRE WRAPPABLE MODULE

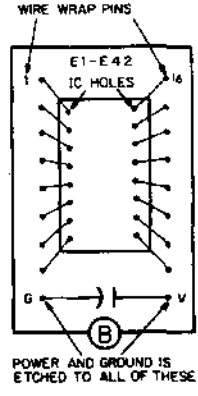
OMNIBUS

W SERIES

Length: Extended
Height: Quad
Width: Single







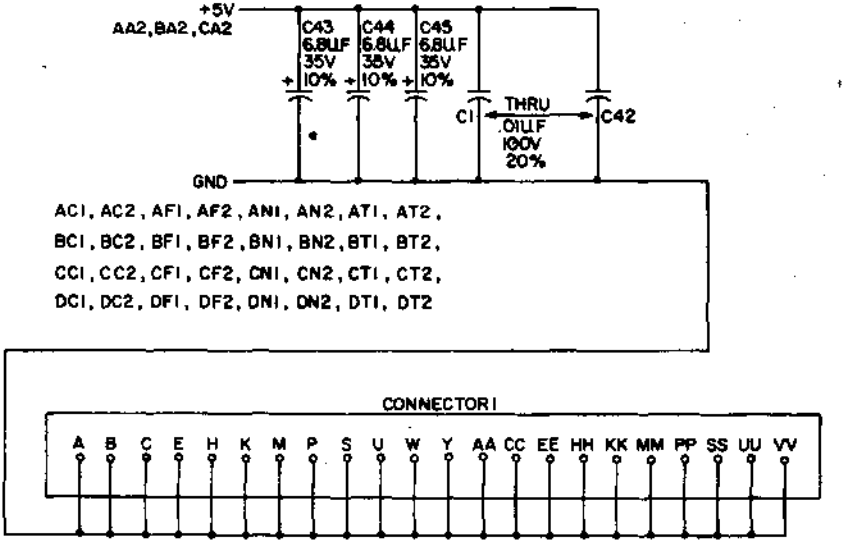
W967 Wire Wrappable Module

DESCRIPTION

The W967 Wire Wrappable Module is a PDP-8/E, 8/F, 8/M general-purpose module that provides for the construction of custom interface designs using intergrated circuits (ICs). Featured on the board are 42 low-profile IC sockets which easily accommodate 14- and/or 16-pin ICs. Each wire wrap pin can accommodate two separate leads of 30-gauge wire. Discrete components may also be directly inserted into the sockets. Position E39 features a pad that can be used for mounting a potentiometer by removing the socket.

The W967 has 72 etched contact fingers at the handle end, with a wire wrap pin connected to each finger. When a W967 is located adjacent to another W967, signals can be bused from one module to the other via these contact fingers by using an H851 edge connector. One H851 can bus 36 signals; therefore, two H851s are required to bus all 72 signals. In addition, the standard 144 contact fingers at the connector end of the module are also connected to wire wrap pins.

An H854 40-pin I/O connector (male) is contained on the module to provide access to the "outside world"; it can accept any cable equipped with an H856 connector. Eighteen of these connector pins are connected to wire wrap pins.



W967 Circuit Schematic

PDP-8, 8/I, 8/L, 8/S (Non-OMNIBUS) Interfacing
This subsection is organized into two groups:

(1) Positive Bus—PDP-8I/ and PDP-8/L
(2) Negative Bus—PDP-8 and PDP-8/S

The I/O signals for the positive and negative buses are identical; refer to Table 2 for descriptions.

Positive Bus—is utilized on most PDP-8/I and all PDP-8/L processors. This means all logic signals passing between these processors and I/O equipment are positive voltage levels or positive signals which allow direct TTL logic interface with appropriate diode clamp protection. The positive levels and pulses change from ground potential (0 V to 0.4 V) to (+2.4 V to +3.6 V) and vice-versa.

The M Series functional modules for use with the positive bus PDP-8 processors are listed below and described on the following pages.

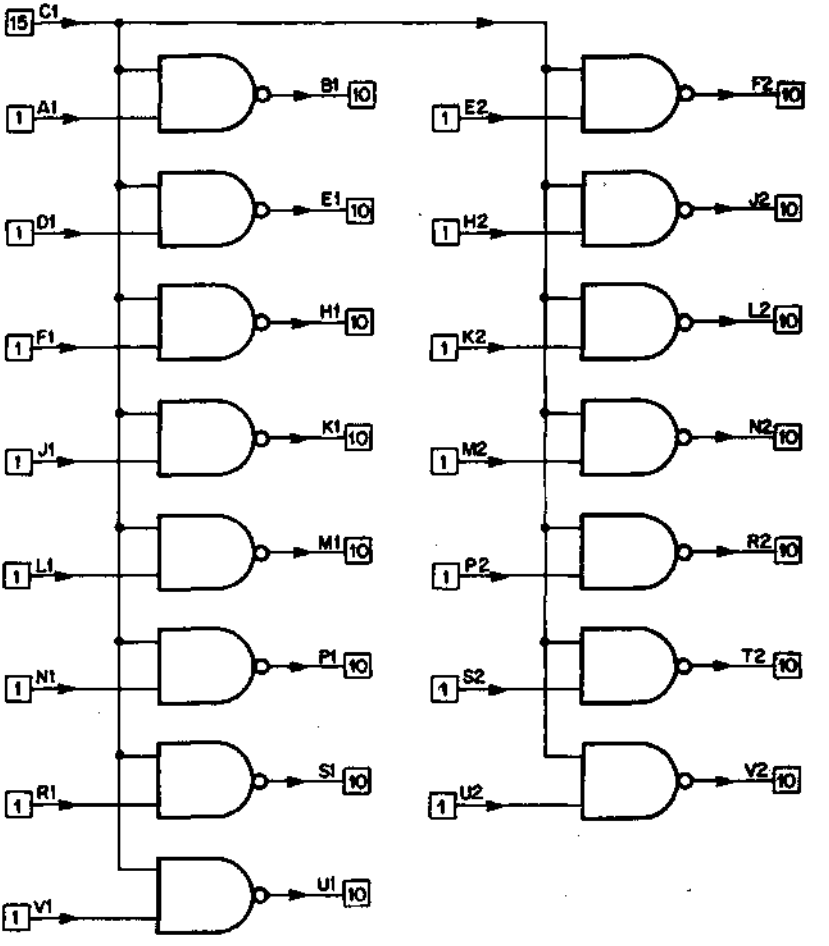
M101	Bus Receivers (data output)
M103 M107	Device Selectors
M108	Flags
M623 M624	Bus Drivers (data input)
M730	Bus Output Interface (positive logic output)
M731	Bus Output Interface (negative logic output)
M732	Bus Input Interface (positive logic input)
M733	Bus Input Interface (negative logic input)
M734	3-Word Input Multiplexer
M735	Input/Output Interface
M736	Priority Interrupt Control
M737	Bus Receiver Interface
M738	Counter-Buffer Interface
M970	Diode Clamping for Bus Lines

M101
BUS DATA INTERFACE

8-FAMILY POS. I/O BUS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	82	A2
GND		C2, T1

The M101 contains fifteen, two-input TTL NAND gates with input ground clamps arranged for convenient data strobing from the PDP8/I or PDP8/L positive bus.

APPLICATIONS

- PDP8/I, PDP-8/L Positive Bus Output Expansion
- Can also be used as inverters or a data multiplexer

FUNCTIONS

Inputs are NAND gated to the output by the common ENABLE input (€I).

SPECIFICATIONS

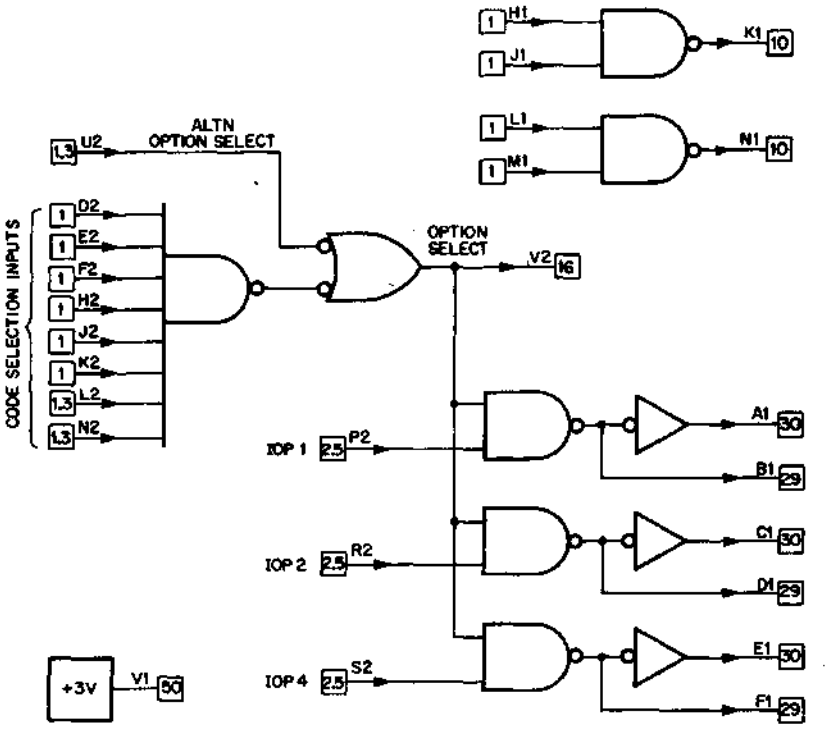
Inputs and outputs have standard M Series levels and propagation time. All data inputs are protected from a negative voltage of more than −0.8 volts.

M103
DEVICE SELECTOR

8-FAMILY POS. I/O BUS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	110	A2
GND		C2, T1

The M103 is used to decode the six device bits transmitted in complement pairs on the positive bus of the PDP8/I and PDP8/L. Selection codes are obtained by selective wiring of the bus signals to the code select inputs D2, E2, F2, H2, J2, and K2. This module also includes pulse buffering gates for the IOP signals found on the positive bus of the above computers. Two two-input NAND gates are also provided for any additional buffering that is required.

APPLICATIONS

- Special-purpose M Series Interfaces for positive bus PDP-8/I, PDP-8/L

FUNCTIONS

OPTION SELECT: The OPTION SELECT output is HIGH when all code inputs (D2-N2) are HIGH. The OPTION SELECT ENABLE input is able to override the code input.

IOP ENABLE: When the OPTION SELECT output is enabled, IOP pulses from the computer are gated to output pins A1-F1. Buffered and unbuffered outputs are provided (of opposite polarity).

Unused Inputs: Unused code inputs should be connected to a source of logic HIGH. Inputs U2, L2, and N2 need not be tied to logic HIGH.

SPECIFICATIONS

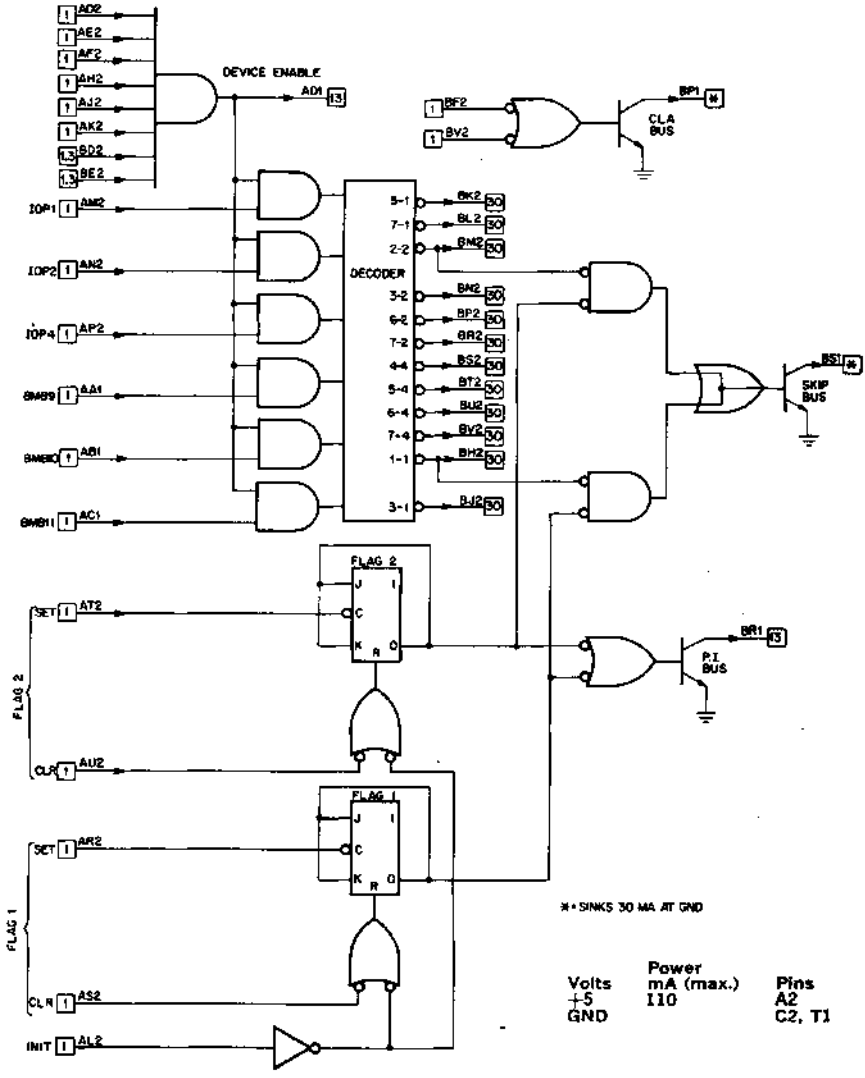
Input Protection: All inputs which receive positive bus signals are protected from negative voltage undershoot of more than 0.8V.

M107
DEVICE SELECTOR

8-FAMILY POS. I/O BUS

M SERIES

Length: Standard
Height: Double
Width: Single



Volts	Power mA (max.)	Pins
+5	110	A2
GND		C2, T1

The M107 is a device selector which, by the use of extended decoding of the BMB lines 9 through 11, will provide seven discrete IOT pulses. Five additional IOT pulse outputs are provided to allow the user to reduce software requirements by the combining of IOT codes. The IOT instruction and the IOP times at which the various IOT pulses occur at the module pins are outlined in the following chart:

Module Pin	IOT	AT IOP TIME		
		1	2	4
BH2	1 – 1	X		
BM2	2 – 2		X	
BJ2	3 – 1	X		
BN2	3 – 2		X	
BS2	4 – 4			X
BK2	5 – 1	X		
BT2	5 – 4			X
BP2	6 – 2		X	
BU2	6 – 4			X
BL2	7 – 1	X		
BR2	7 – 2		X	
BV2	7 – 4			X

Example: If an IOP-7 is issued, IOT pulses will exist only at output pins BL2 (7-1), BR2 (7-2) and BV2 (7-4). IOT pulses will not exist at any other output pin.

The M107 also contains two flag flip-flops which may be directly cleared or set. The outputs of the flag flip-flops are connected to the skip and program interrupt lines. Interrogation of the flags is accomplished by IOT 1 – 1 for flag 1 and IOT 2 – 2 for flag 2.

The M107 also provides two inputs to accomplish the "clear the accumulator" function.

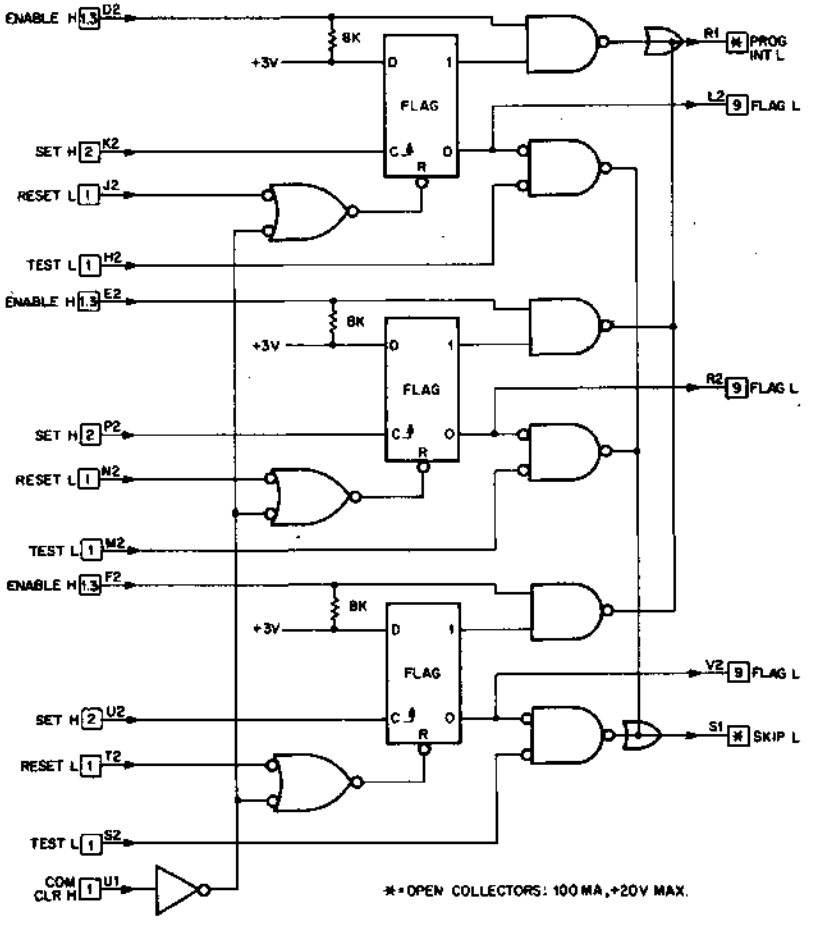
Outputs: Option Select Pin AD1 can drive 13 TTL loads. Bus driver outputs pins BP1, BS1, and BR1 are open collector NPN transistors and can sink 30 ma. at ground. The maximum voltage applied to these outputs must not exceed +20 Volts and each output is diode protected against negative undershoot in excess of −0.9 Volts.

M108
FLAG MODULE

8-FAMILY POS. I/O BUS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	137	A2
GND		C2, T1

The M108 contains three general-purpose clocked flip-flops for use in flag applications in I/O interfaces, etc. Gating is provided so that the flags can be individually set or gated to the program interrupt inputs of a positive-bus PDP-8 computer.

APPLICATIONS

- Device Ready logic in custom device interfaces for positive-bus PDP-8 computers

FUNCTIONS

CLEAR Inputs: Each flag flip-flop may be independently cleared or all flip-flops may be cleared simultaneously.

Flag Outputs: The output of each flag flip-flop is gateable and is open collector ORed to the Program Interrupt bus.

The output of each flag flip-flop is passed through a gate and open collector to the skip bus. This facility allows the user to test for a flag.

The 0 side of each flip-flop has been extended to module pins for peripheral control.

SET Inputs: Each flip-flop may be independently set by the application of the leading (positive going voltage) edge of a pulse or level to the clock inputs.

Disabling PI Feature: If use of the Program Interrupt feature is not desired, the ENABLE inputs (D2, E2, F2) must be connected to ground. If Program Interrupt is desired, no connections to the ENABLE inputs are required.

SPECIFICATIONS

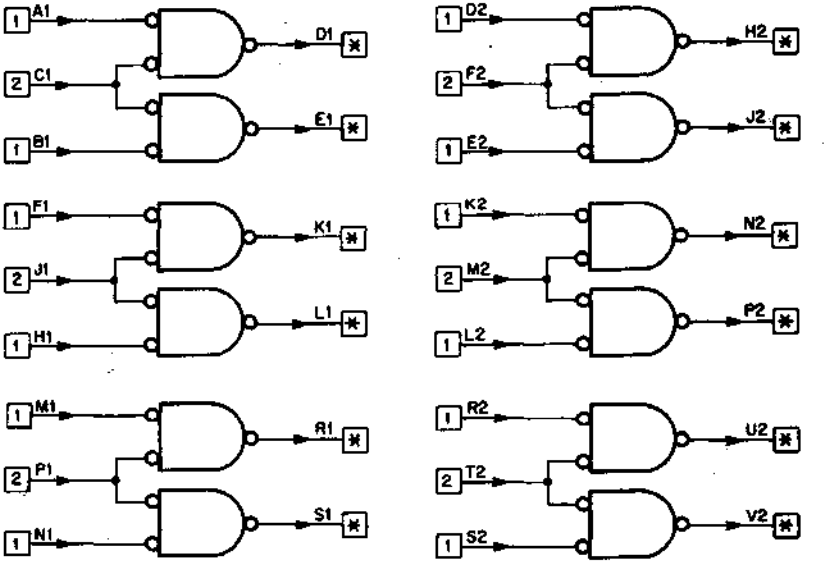
Pin R1, (PI Function) and S1 (Skip Function) are open collector NPN Transistors and will sink 100mA to ground. The voltage applied to these outputs must not exceed +20 volts.

M623
BUS DRIVER

8-FAMILY POS. I/O BUS

M SERIES

Length: Standard
Height: Single
Width: Single



*= SINKS 100 MA TO GROUND, +20V MAX.

Volts	Power mA (max.)	Pins
+5	71*	A2
GND		C2, T1 U1, V1

* does not include output current

The M623 contains 12 two-input AND gate bus drivers for convenient driving of the positive input bus of either the PDP-8/I or PDP-8/L. The output consists of an open collector NPN transistor.

APPLICATIONS

- Driving PDP-8/I or PDP-8/L positive input bus

FUNCTIONS

A driver output will be at ground when both inputs are at ground.

SPECIFICATIONS

Output Drive: Each driver can sink 100 mA at ground and can withstand a maximum output voltage of +20 volts.

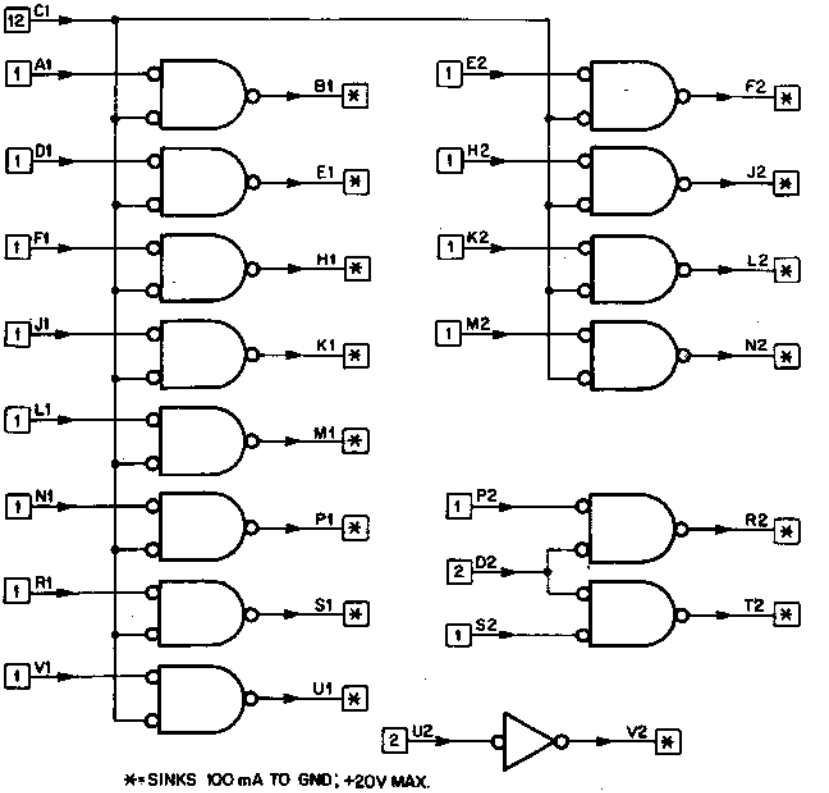
Output Rise and Fall Times: Typically 30 ns when a 100 mA resistive load is connected to a driver output.

M624
BUS DRIVER

8-FAMILY POS. I/O BUS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	89*	A2
GND		C2, T1

* driver outputs not connected

The M624 contains 15 bus drivers intended for convenient driving of the positive input bus of either the PDP-8/I or PDP-8/L. Twelve of the drivers have a common gate line for selecting data. There are three additional drivers, two sharing a common gate line and the third without a gate line. These three additional drivers were intended to accommodate the functions of PROGRAM INTERRUPT, IO SKIP and CLEAR AC.

Each output consists of an open collector NPN transistor.

APPLICATIONS

- PDP-8/I or PDP-8/L positive input bus driving

SPECIFICATIONS

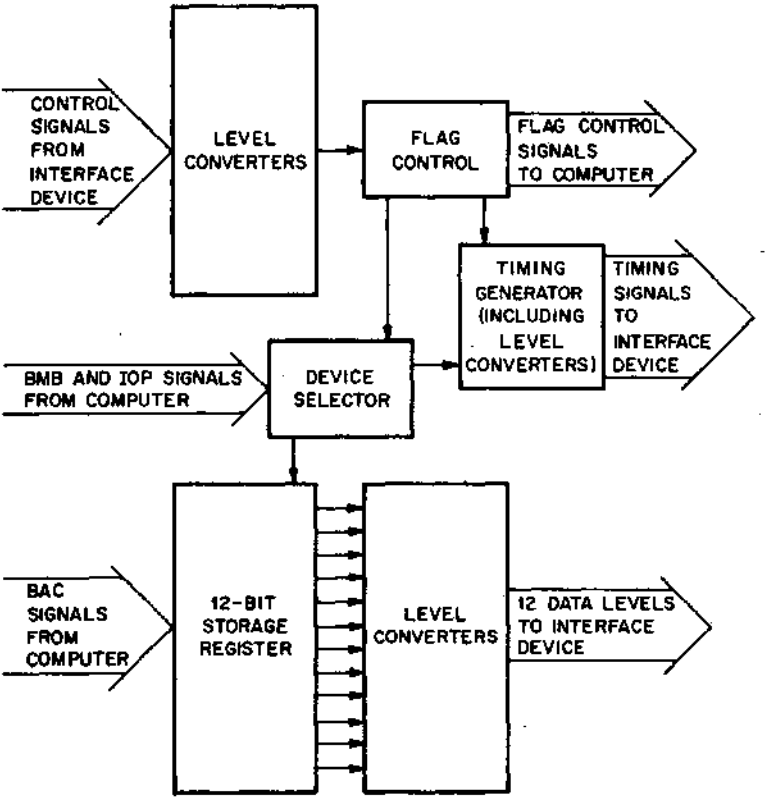
All outputs can sink 100 mA to ground. Voltage applied to the output should be equal to or less than +20 volts. Output rise and fall times are typically 30 ns when a 100 mA resistive load to +5 volts is connected to a driver output.

M730 & M731
BUS INTERFACES

8-FAMILY POS. I/O BUS

M SERIES

Length: Standard
Height: Double
Width: Single

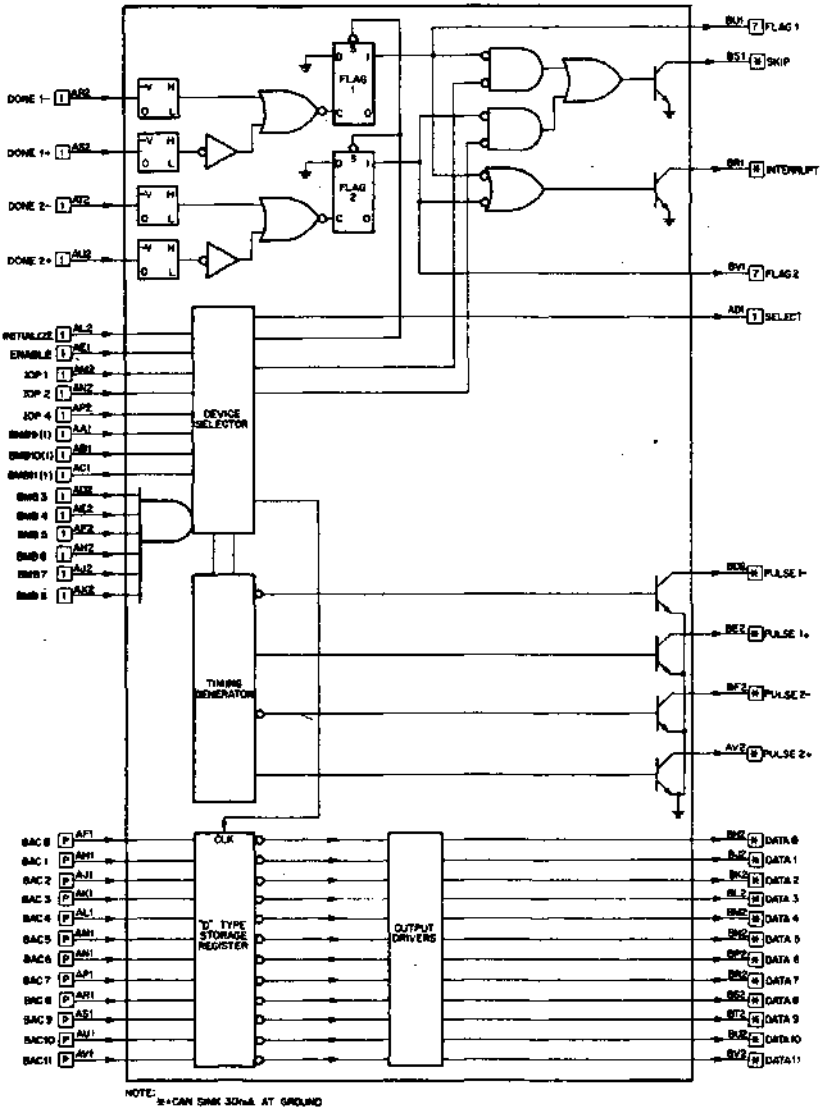


Volts	Power mA (max.)	Pins
+5	400	AA2, BA2
GND		AC2, AT1, BC2, BT1
−15	90*	AB2, BB2

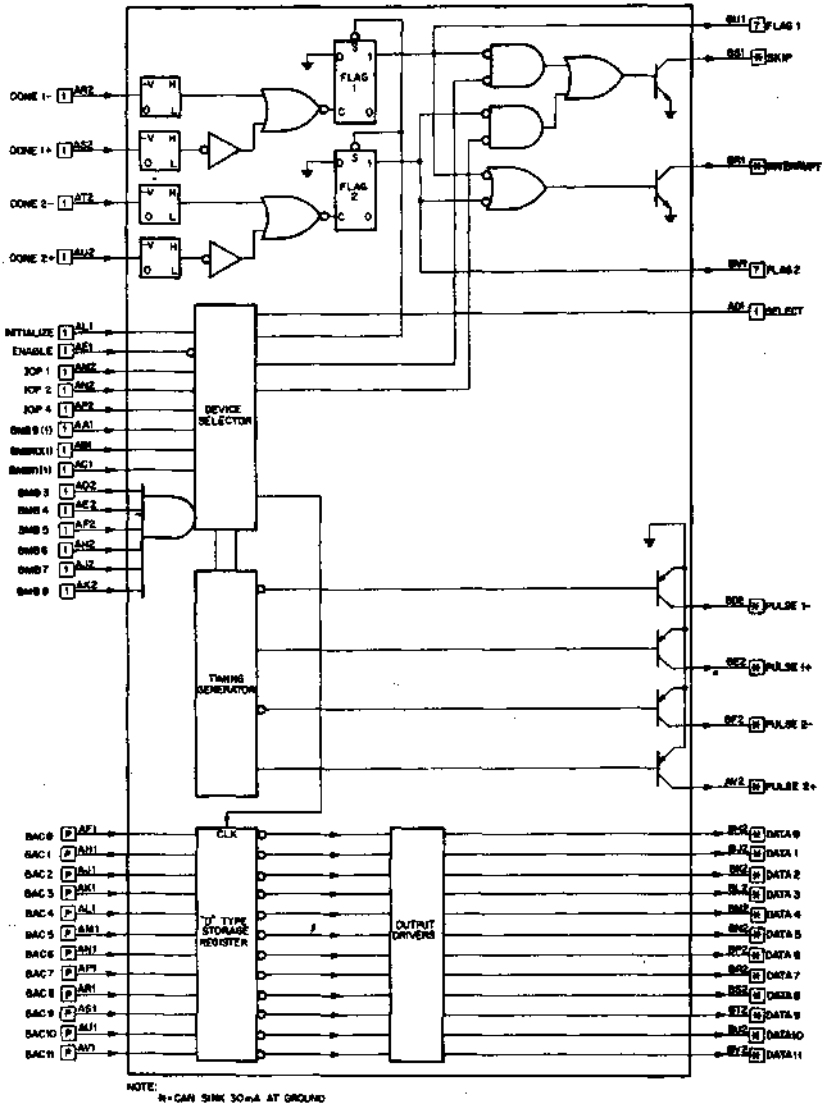
* M731 only

The M730 and M731 interface modules provide extremely flexible interface control logic to connect devices, systems, and instruments to the output half of the programmed I/O transfer bus of either a PDP8/I or a PDP8/L positive bus computer. Peripheral equipment which operates either asynchronously or synchronously to a computer and expects to receive data from that computer, can to a large degree be interfaced by either the M730 or M731. Basic restrictions on the device or system to be interfaced are simply that it receive data in parallel, provide one or more control lines, and operate at a data transfer rate of less than 20 KHz. Complete interfaces to such peripheral gear as card punches and other repetitive devices is possible using the M730 and M731; however part of the controlling functions, such as counting etc. must be performed by computer software.

The M730 provides an output interface for positive voltage level devices and the M731 provides an output interface for systems using negative voltages. A detailed description of the M730 follows; the M731 is essentially the same except for the negative outputs.



BUS INTERFACE — M730 (POSITIVE OUTPUT)



BUS INTERFACE — M731 (NEGATIVE OUTPUT)

GENERAL

The M730 provides a complete positive (TTL compatible) output interface for the positive bus PDP-8/I or PDP-8/L. It accepts from the positive bus computer 12 bits of data from the BAC bus, the device selection code from the MB bus, and IOP pulses from the IOP bus. It will send information from 2 flags to the computer via the skip bus, and will send 12 bits of data plus two pulses (pulse 1 and pulse 2) to the external device. The pulses are variable from 5 to 25 microseconds by the use of potentiometers. The module will also accept Done signals from the external device to control the flags.

FLAG CONTROL

Setting Flag 1 or Flag 2 causes an interrupt which comes from an open collector NPN transistor to the positive bus computer in the form of a ground signal. IOT 6XY1 will cause a skip if Flag 1 is set. IOT 6XY3 will cause a skip if Flag 2 is set. The skip output is also an open collector NPN transistor which, when asserted, sends a ground signal to the positive bus computer. Both skip and interrupt outputs are open collector NPN transistors that can be tied directly to the skip and interrupt bus of the positive bus computer. Flag 1 and Flag 2 outputs are available as M Series TTL outputs and are ground when true. Flag 1 is set by Done 1— and Done 1+ from the external device. In order to set Flag 1, Done 1— must go to ground and Done 1+ must go to at least +2.5 V. If desired, one can tie Done 1+ to +3VDC and set Flag 1 by issuing a negative pulse or level at Done 1—. To set Flag 2 use Done 2— and Done 2+, the same as Flag 1— and Flag 1+. Flag 1 and Flag 2 can be cleared by Initialize or by IOT 6XY2.

DEVICE SELECTOR CONTROL

The code selector accepts signals from bus lines BMB 3-8. When the AND gate conditions are met (depending on the code wired in) the Device Selector will become active. The code selected by BMB 3-8 can be bypassed by putting a ground on the enable line. The Select output can be used as an enable to allow external gating of pulses IOP 1, 2, and 4 and levels BMB 9 (1), BMB 10 (1), and BMB 11 (1) to issue the IOTs listed below depending on which gates are met.

Mnemonic	ON IOP	OPERATION
6XY1	1	Skip on Flag 1
6XY2	2	Clear Flags 1 and 2
6XY3	1	Skip on Flag 2
6XY4	4	Issue Pulse 1
6XY5	4	Clear Pulse 1— and Pulse 1+ when jumper A & C are in
6XY6	4	Load the BAC into the 12 Bit Storage Register
6XY7	4	Issue Pulse 2

TIMING GENERATOR CONTROL

Upon issuing IOT 6XY4, Pulse 1— and Pulse 1+ outputs will issue a pulse. Note that Pulse 1— and Pulse 1+ are the inverse of each other. Pulse duration can be from 5 μs to 25 μs depending on the setting of the potentiometer mounted on the board. The amplitude of the pulse out can be from 0 V. to +20 V., depending on the voltage applied to the open collector NPN transistor output on the Data Lines.

SPECIFICATIONS

Inputs: Done 1—, Done 1+, Done 2—, and Done 2+ present one TTL unit load at ground and are protected for input voltage between —20 to +20 volts and have an input threshold at +1.5 volts.

Code Select, Initialize, and BMB 9-11 are TTL compatible inputs and each represents 1 unit load (1.6 ma). All other inputs are M Series inputs and draw 2 unit loads each.

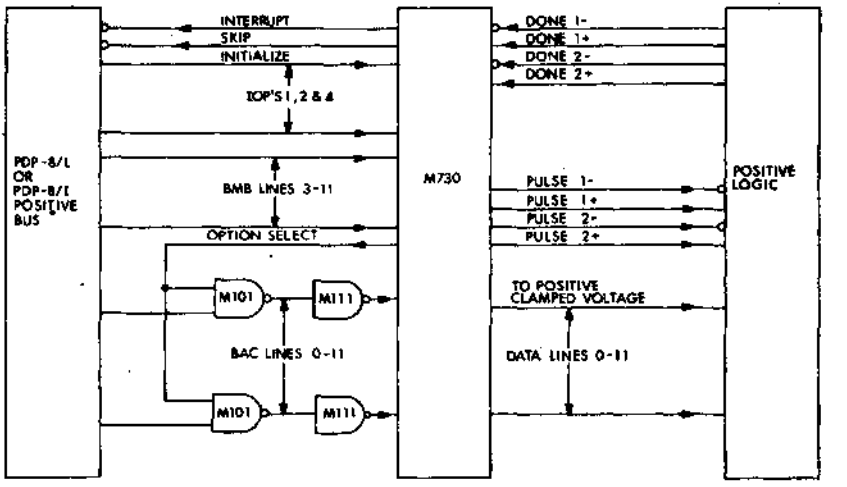
Outputs: All open collector outputs including computer inputs drive 30 ma non-inductive at ground with a maximum positive output voltage of +20 volts. The outputs are driven by an open collector NPN transistor. Pulse 1 and Pulse 2 outputs are adjustable from 5 μs to 25 μs with a recovery time of 40 μs to 250 μs. Note that data lines and pulse output lines have to be diode protected if driving an inductive load.

POWER	**CURRENT**
+5v Pin AA2, BA2	500 ma (max.)
Gnd Pin AC2, AT1	
BC2, BT1	

Some care must be taken when using the M730 to avoid overloading the bus. Normally, the bus can drive 64 devices or ports. An unbuffered M730 presents to the bus a load which is equivalent to ten normal ports.

A large port capability, using the M730, can be realized by buffering it with the M101, using the Select Line as the enable for the M101. In this configuration each M730 and M101 combination looks to the bus like 2.6 ports. Use of this method allows 25 M730s on the bus, rather than six. A configuration for this method is shown in the following figure.

Use of M730 Using M101 & M111



JUMPER NOTES

A & C in — Outputs BD2, BE2 at asserted levels from IOTXY4 until IOTXY5.

A & B in — Outputs BD2, BE2 at asserted levels from IOTXY4 until Flag 1 is set by AND of data on inputs AR2, AS2.

D & F — Outputs BF2, AV2 at asserted levels from IOTXY7 until Flag 2 is set by AND of data on inputs AT2, AU2.

D & E — Outputs BF2, AV2 at asserted levels as using D & F until Flag 1 is set.

Pulse widths presently 5 μs — 25 μs recovery time 40 μs — 250 μs.

All units when used on I/O bus require M907 or equivalent diode undershoot protection.

M732 & M733 BUS INTERFACES

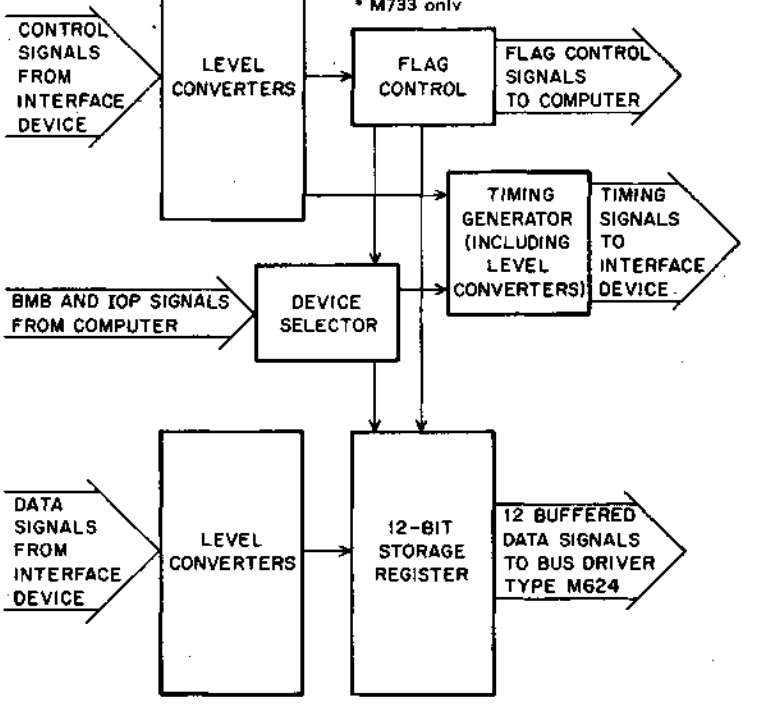
8-FAMILY POS. I/O BUS

M SERIES

Length: Standard
Height: Double
Width: Single

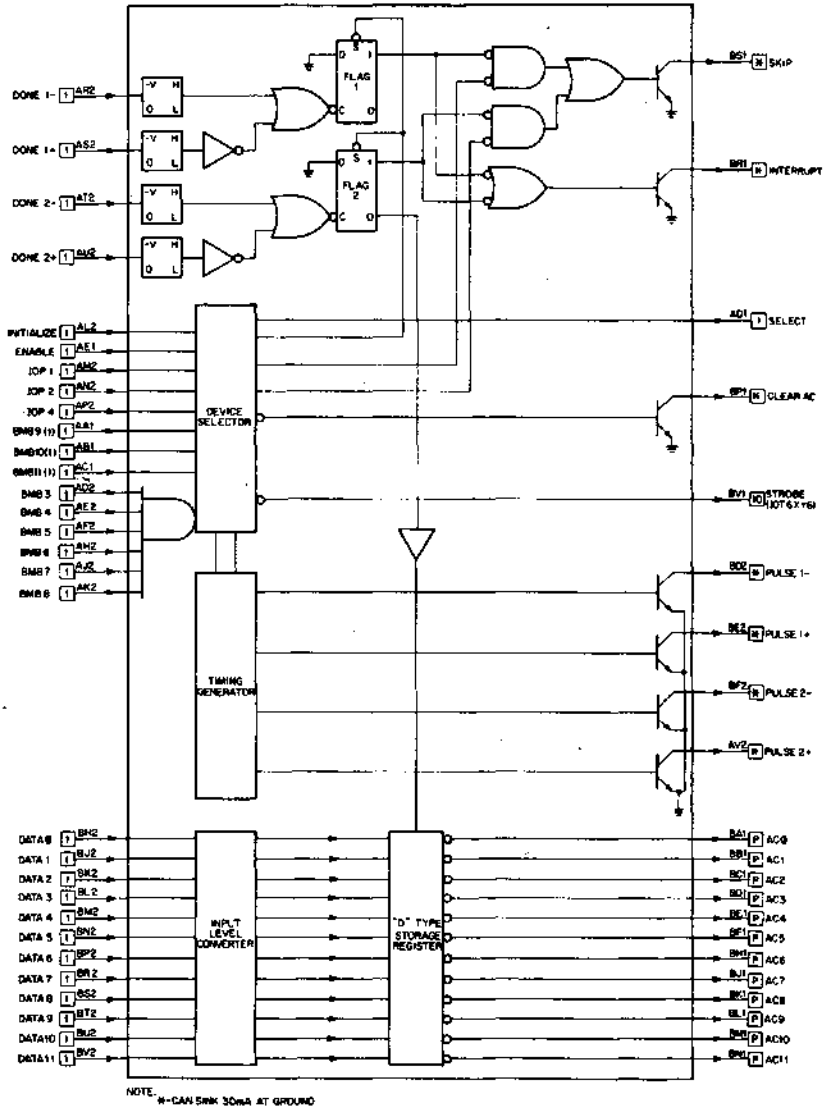
Volts	Power mA (max.)	Pins
+5	400	AA2, BA2
GND		AC2, AT1, BC2, BT1
−15	125*	AB2, BB2

* M733 only

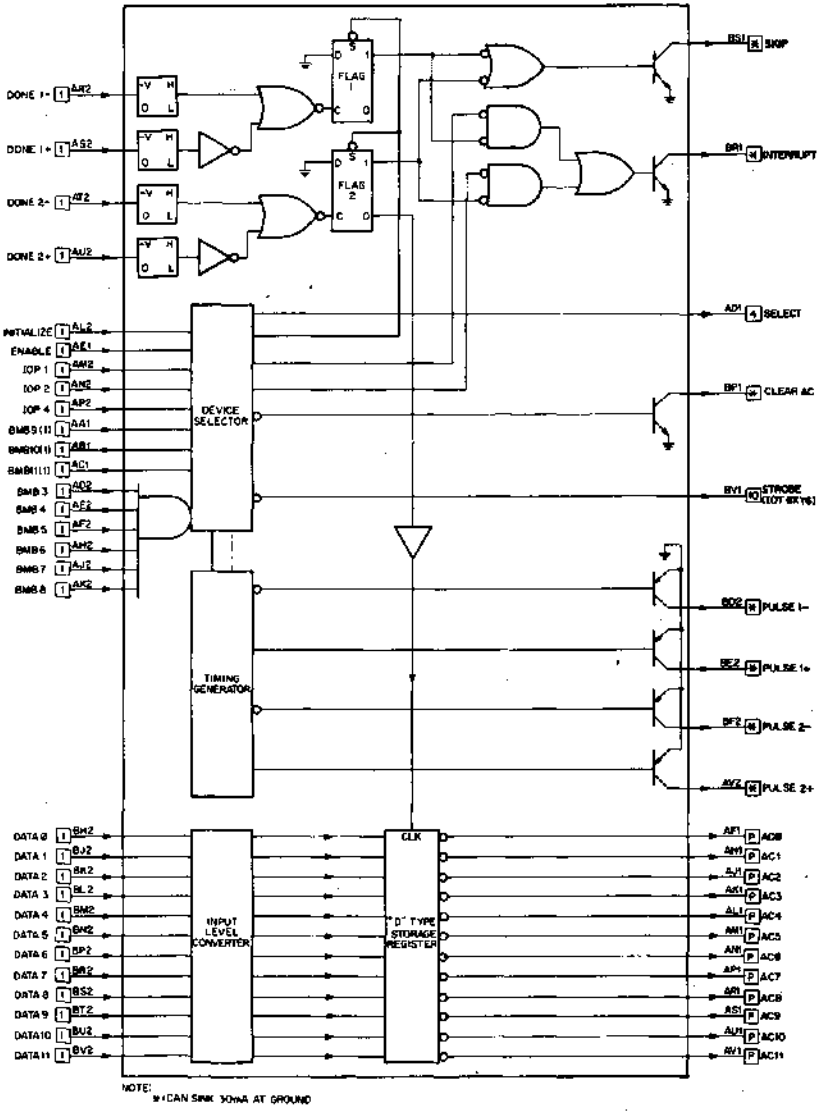


The M732 and M733 interface modules provide extremely flexible interface control logic to connect devices, systems, and instruments to the input half of the programmed I/O transfer bus of either a positive bus PDP8/I or PDP8/L computer. Peripheral equipment which operates either asynchronously or synchronously to a computer and expects to transmit data to that computer, can to a large degree be interfaced by either the M732 or M733. Basic restrictions on the device or system to be interfaced are simply that it transmit data in parallel, provide one or more control lines, and operate at a data transfer rate of less than 20KHZ. Complete interfaces to such peripheral gear as card readers and other repetitive devices is possible using the M732 and M733; however, part of the controlling functions such as counting, etc., must be performed by computer software.

The M732 provides an input interface for positive voltage level devices and the M733 provides an input interface for systems using negative voltages. A detailed description of the M732 follows; the M733 is essentially the same except for the negative inputs.



BUS INTERFACE — M732 (POSITIVE INPUT)



BUS INTERFACE — M733 (NEGATIVE INPUT)

GENERAL

The M732 provides a complete positive (TTL compatible) input interface for the positive bus PDP-8/I or PDP-8/L. It receives 12 parallel bits of data from the external device and transmits 12 bits of data from the storage register to the computer via the BAC bus under computer control. It accepts from the positive bus computer the device selection code from the MB bus, and IOP pulses from the IOP bus. Two separate flags can be generated and sent to the computer via the skip bus. Also, two timing pulses (pulse 1 and pulse 2) can be sent to the external device. The timing pulses are variable from 5 to 25 microseconds by the use of potentiometers mounted on the module. Done signals are accepted from the external device to control the flags. The basic restriction on the device or system to be interfaced is that it must have a data transfer rate of less than 20 KHz.

FLAG CONTROL

Setting Flag 1 or Flag 2 causes an interrupt which comes from an open collector NPN transistor to the positive bus computer in the form of a ground signal. IOT 6XY1 will cause a skip if Flag 1 is set. IOT 6XY3 will cause a skip if Flag 2 is set. The skip output is also an open collector NPN transistor which, when asserted, sends a ground signal to the positive bus computer. Both skip and interrupt outputs are open collector NPN transistors that can be tied directly to the skip and interrupt bus of the positive bus computer. Flag 1 and Flag 2 outputs are available as M Series TTL outputs and are ground when true. Flag 1 is set by Done 1— and Done 1+ from the external device. In order to set Flag 1, Done 1— must go to ground and Done 1+ must go to at least +2.5V. If desired, one can tie Done 1+ to +3V. and set Flag 1 by issuing a negative pulse or level at Done 1—. To set Flag 2, use Done 2— and Done 2+, the same as Flag 1— and Flag 1+. Flag 1 and Flag 2 can be cleared by Initialize or by IOT 6XY2.

DEVICE SELECTOR CONTROL

The code selector accepts signals from bus lines BMB bits 3-8. When the AND gate conditions are met (depending on the code wired in) the Device Selector will become active. The code selected by BMB 3-8 can be bypassed by inserting a ground on the enable line. The Select output can be used as an enable to allow external gating of IOP pulses 1, 2, & 4 with BMB 9 (1), BMB 10 (1), and BMB 11 (1) to issue the IOTs listed below depending on which gates are conditioned.

Mnemonic	On IOP	Operation
6XY1	1	Skip on Flag 1
6XY2	2	Clear Flags 1 and 2
6XY3	1	Skip on Flag 2
6XY4	4	Issue Pulse 1
6XY5	4	Clear Pulse 1— and Pulse 1+ when jumpers A & C are inserted
6XY6	2	Clear AC
6XY6	4	Read AC0-AC11 from the M624 into the accumulator of the computer.
6XY7	4	Issues pulse 2

TIMING GENERATOR CONTROL

Upon issuing IOT 6XY4 Pulse 1— and Pulse 1+ outputs will issue a pulse. Note that Pulse 1— and Pulse 1+ are the inverse of each other. Pulse duration can be from 5 μs to 25 μs, depending on the setting of the potentiometer mounted on the board. The amplitude of the pulse out can be from 0 V. to +20 V. depending on the voltage applied to the open collector NPN transistor output. Issuing IOT 6XY7 will cause Pulse 2— and Pulse 2+ to receive a pulse. The same characteristics hold true here as for Pulse 1— and Pulse 1+.

12-BIT STORAGE REGISTER CONTROL

Upon setting the Flag 2 by the Done 2 signal, Data 0 through Data 11 is read into the storage register. The positive logic signals being interfaced on the data lines can be from 0 V. to +20 V. levels. A ground or 0 V. level on the data line read into the storage register input yields a +3V. level on the output (AC). A +3V. signal or larger up to +20 V. read into the storage register input from the data lines will yield a ground level out of the storage register on the AC lines. For assertion of a one into the computer, the appropriate data lines has to be at least +2.5 or greater, up to +20 V. The storage register output AC0 through AC11 can be read into the accumulator using an M624 Bus Driver module and the data out strobe IOT 6XY6.

SPECIFICATIONS

Inputs: All inputs appear as TTL loads. Inputs present 2 unit loads except for the following inputs, which present only one unit load: Code Select, Initialize, BMB 9-11, and Data 0-11. Data inputs expect a logical 0 of 0, +1, −3 and a logical 1 of 3, +17, −1 volts.

Outputs: All outputs drive 30 ma. at ground through NPN transistors except AC0—AC11, Select (1), Flag (0), and Flag 2 (0). AC0—AC11 must be connected to the M624 module and then will be capable of driving 100 ma. at ground. Select (1), Flag 1 (0), and Flag 2 (0) outputs are normal TTL levels with output drive capability in unit loads of respectively 1, 7, and 7.

POWER	PIN	CURRENT
+5 V. ±5%	AA2, BA2	500 ma. (max.)
GND	AC2, BC2 AT1, BT1	

JUMPER NOTES

A & C in—Outputs BD2, BE2 at asserted levels from IOTXY4 until IOTXY5.

A & B in—Outputs BD2, BE2 at asserted levels from IOTXY4 until Flag 1 is set by AND of data on inputs AR2, AS2.

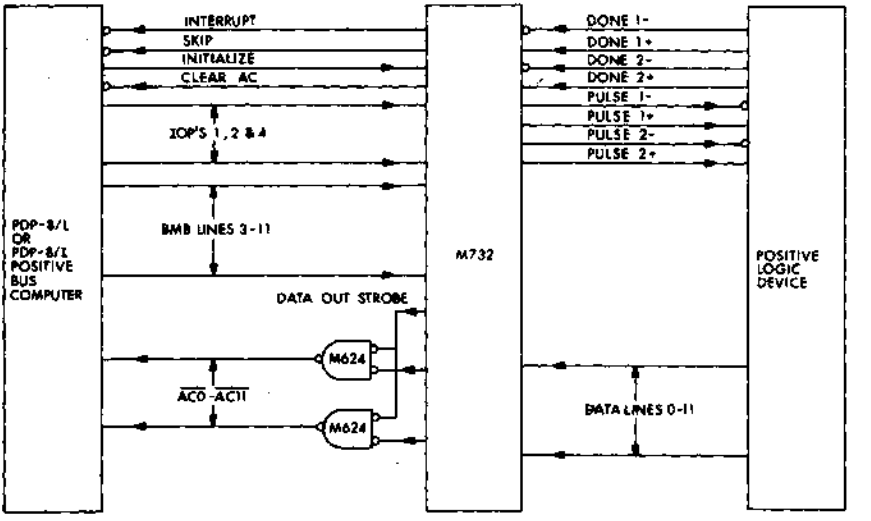
D & F —Outputs BF2, AV2 at asserted levels from IOTXY7 until Flag 2 is set by AND of data on inputs AT2, AU2.

D & E —Outputs BF2, AV at asserted levels as using D & F until Flag 1 is set.

Pulse widths presently 5 μs—25 μs recovery time 40 μs—25 μs.

All units when used on I/O bus require M907 or equivalent diode undershoot protection.

INTERFACE EXAMPLE

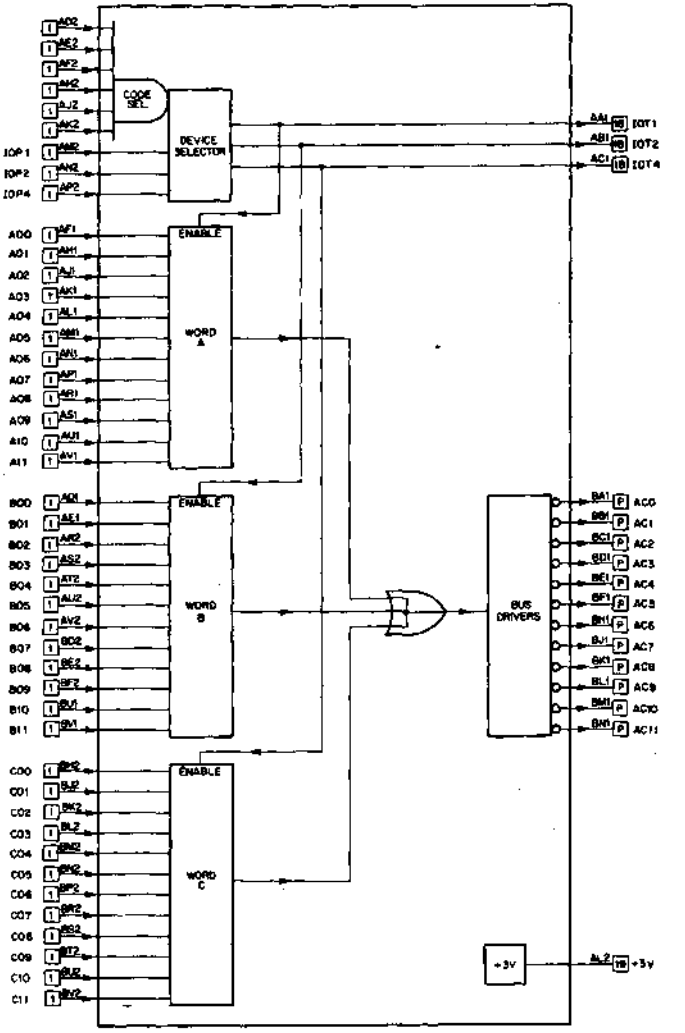


M734
I/O BUS INPUT MULTIPLEXER

8-FAMILY POS. I/O BUS

M SERIES

Length: Standard
Height: Double
Width: Single



Volts	Power mA (max.)	Pins
+5	325	AA2, BA2
GND		AC2, AT1, BC2, BT1

The M734 is a three-word multiplexer used for strobing 12-bit words on a positive voltage input bus, usually the input of the PDP-8/I or the PDP-8/L. Device selector gating is provided. The data outputs of the M734 Multiplexer consist of open collector NPN transistors which allow these outputs to be directly connected to the bus.

FUNCTIONS

Code Select Inputs: When a positive AND condition occurs at these inputs, the pulse inputs IOP1, IOP2, and IOP4 are enabled for use in strobing input data. The code select inputs must be present at least 50 ns prior to any of the three signals that they enable. If all select inputs are not required, unused inputs must be tied to a source of +3 volts (pin AL2). These inputs are all clamped so that no input can go more negative than −0.9 volts.

IOP1, 2, 4: These 50 ns (or longer) positive pulse inputs strobe 12-bit words A, B, and C to the bus driver. All three lines are clamped so that no pulse input can go more negative than −0.9 volts.

Data Inputs: Bits 0-11 on words A, B, and C are strobed 12 bits at a time. Bus driver output lines (0-11) correspond to the selected word input lines (0-11). A HIGH data input forces a bus driver output to ground during a data strobe. Data signals must be present at least 30 ns prior to issuance of IOP 1, 2, or 4.

Bus Driver: These open collector NPN transistor bus driver outputs can sink 100 mA at ground. Each driver output is protected from negative undershoot by a diode clamp. When this module is used with the PDP-8/I or PDP-8/L, these outputs would be connected to the accumulator input lines of the I/O bus. Typical rise and fall times at these outputs with a 100 mA resistive load are 100 ns.

Data Strobes: Pins AA1, AB1, and AC1 appear coincident with IOP1, IOP2, and IOP4 respectively only if the code select inputs are all HIGH.

+3 Volts—Pin AL2: Can hold 19 inputs at a logic HIGH level.

PRECAUTIONS

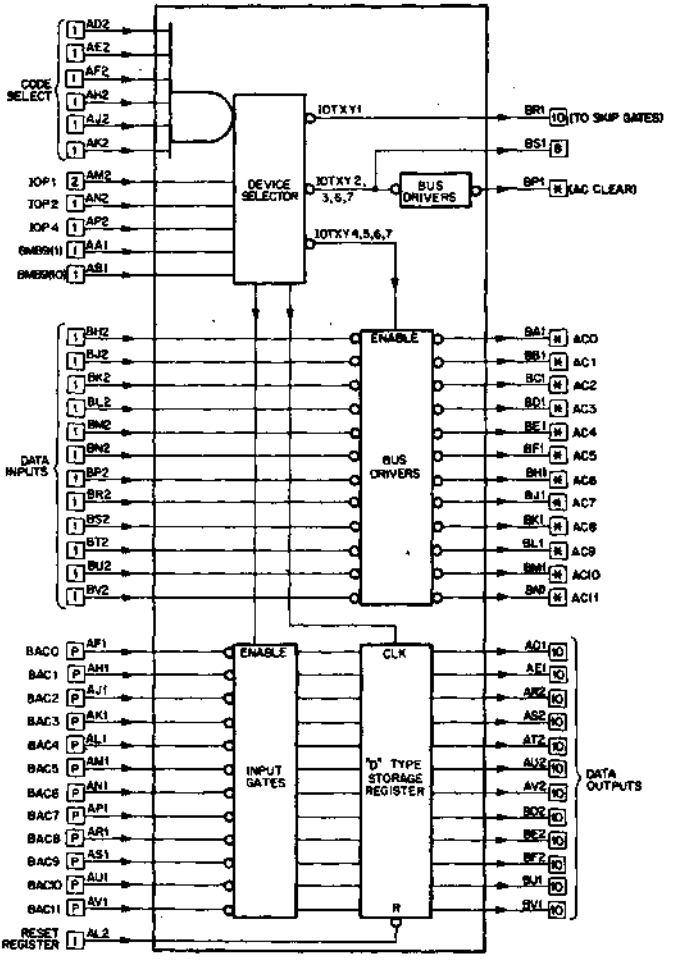
Bus driver maximum output voltage must not exceed +20 volts.

M735
I/O BUS TRANSFER REGISTER

8-FAMILY POS. I/O BUS

M SERIES

Length: Standard
Height: Double
Width: Single



NOTE:
**CAN SINK 100 mA TO GROUND

Volts	Power mA (max.)	Pins
+5	425	AA2, BA2
GND		AC2, AT1, BC2, BT1

The M735 provides one 12-bit input bus driver and one 12-bit output buffer register for input and output data transfers on the positive I/O bus of either a PDP8/I or a PDP8/L. Device selector gating plus additional signal lines provide the flexibility necessary for a complete interface with the exception of flag sense signals. Use of the M735 is not restricted to a computer, as it can be used in many systems to provide reception and transmission of data over cables.

Inputs:
All inputs present one TTL unit load with few exceptions as noted in the functional descriptions below:

Code Select Inputs: When a positive AND condition occurs at these inputs, the pulse input gates for IOP1, IOP2, and IOP4 are enabled for use as detailed below. The code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If all select inputs are not required, unused inputs must be tied to a source of +3 Volts. These inputs are all clamped so that no input can go more negative than —0.9 Volts. When this module is used with the PDP8/I or PDP8/L these inputs would be connected to BMB outputs 3-8 to generate a device code. Where required in discussions below, this 6-bit device code will be referred to as code XY.

IOP1, 2, 4, BMB9(1) and BMB10(1): These three IOP's 50 nsec or longer positive pulse inputs, in conjunction with control level inputs BMB9(1) (Pin AA) and BMB10(1) (Pin AB1) provide all of the necessary signals for operation of this module. Table 1 below indicates the recommended use of these pulses and levels. A"1" or "0" in this table indicates the presence or absence respectively of a pulse (an IOP) or the logic level at pins AA1 or AB1.

IOP 4	IOP 2	IOP 1	BMB 9(1)	BMB 10(1)	PDP/8 Mnemonic	Module Operation
0	0	1	0	0	IOTXY1	+3V → 0V output pulse on pin BR1 used for skip function.
0	1	0	0	1	IOTXY2	+3V → 0V output pulse on pin BS1, bus driver output on BP1 pulsed to ground and is used for the AC clear function.
0	1	1	0	1	IOTXY3	Load output register from accumulator outputs on IOP1 execute IOTXY2.
1	0	0	1	0	IOTXY4	Data inputs strobed onto accumulator inputs.
1	0	1	1	0	IOTXY5	Load output register on IOP1, Execute IOTXY4.
1	1	0	1	1	IOTXY6	Execute IOTXY2, and IOTXY4.
1	1	1	1	1	IOTXY7	Execute IOTXY3, and IOTXY4.

The M735 module operation as associated with the various mnemonic IOT codes is quite explicit with the exception of IOTXY5. This code (IOTXY5) would be used to load zeros into the M735 with IOTXY1 and then to load into the AC the data present at the data inputs of the bus driver when IOTXY4 occurs. In this particular operation the AC has been effectively cleared as the content of the AC was zero during IOTXY1 thereby allowing the transfer of data into the AC without the use of the AC clear command usually generated by IOT2.

Although it is not implicit from Table 1, BMB9(1) and BMB10(1) inputs are gated in a positive OR circuit, so that when the M735 is not used on a PDP8/I or PDP8/L I/O bus one of these inputs can be grounded and the other used for control. They must appear at least 50 nsec prior to an IOP pulse. If the M735 is used with one of the above computers, these inputs must be tied to the corresponding I/O bus lines. The input load on IOP1 is two TTL unit loads. All five inputs are clamped so that no input can go more negative than —0.9 Volts.

Data Inputs: Each data input when at ground, enables the corresponding bus driver output to be pulsed to ground during IOTXY4. A high input will inhibit the bus driver from being strobed. Since each input is ANDed with IOTXY4, any change of data after this strobe begins will change the bus driver output.

Accumulator Inputs: The input level presented to these inputs will be the same as that assumed by the buffer outputs after executing inputs strobes IOTXY, 5, or 7. Input data must be present at least 50 nsec prior to an IOP. Each input is protected from negative undershoot by a diode clamp.

Reset Register Pin AL2: A positive pulse of 50 nsec or longer at this input sets all buffer outputs to ground. When high, this input overrides any data loading from the accumulator inputs. The output register will be cleared within 70 nsec from the rising edge of this input. Diode input clamping is provided to limit negative undershoot to —0.9 Volts.

Outputs:
Pin BR1: This output can drive ten TTL unit loads and has a propogation delay of less than 20 nsec. See Table 1.

Bus Driver: These open collector npn transistor bus driver outputs, including pin BP1, can sink 100 ma. at ground. The maximum output voltage cannot exceed +20 Volts and each driver output is protected from negative undershoot by a diode clamp. When this module is used with the PDP8/I or PDP8/L, output pins BA1—BN1 would be connected to the accumulator input lines and pin BP1 to the clear accumulator line of the I/O bus. Typical rise and fall TTT of these outputs with a 100 mA. resistive load are 100 nsec.

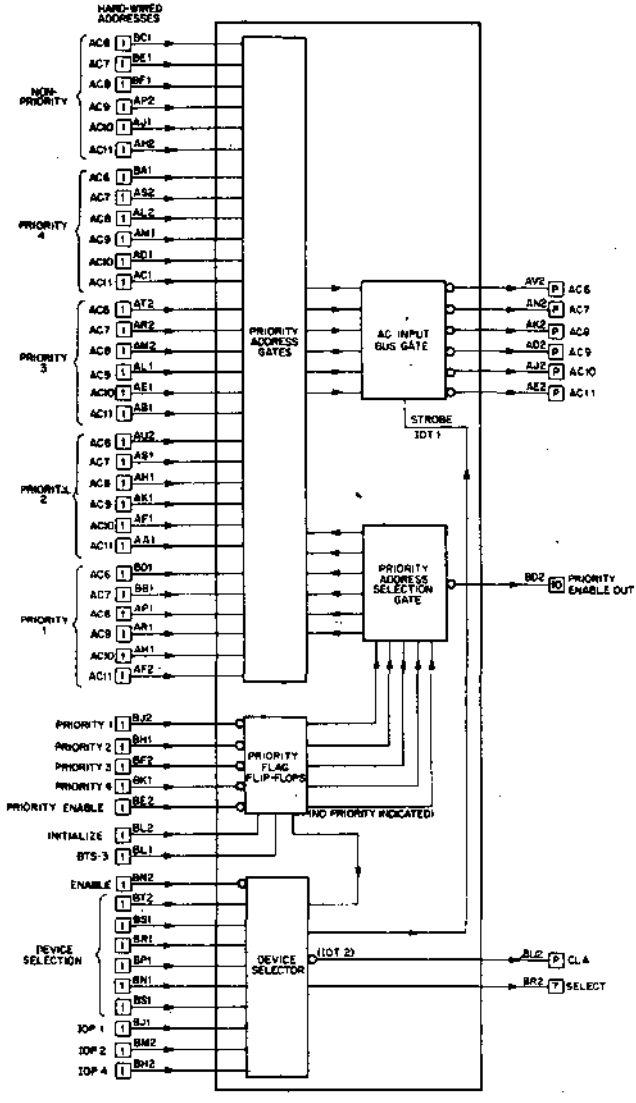
Buffer Outputs: Each output can drive ten TTL unit loads.

M736
PRIORITY INTERRUPT MODULE

8-FAMILY POS. I/O BUS

M SERIES

		Volts	Power mA (max.)	Pins
Length:	**Standard**			
Height:	**Double**	+5	400	A2
Width:	**Single**	GND		C2, T1



The M736 is used in conjunction with the PDP8/I or 8/L to provide the capability of assigning priorities to various I/O devices connected to the I/O bus of the computer. The M736 can be used to assign priorities for one thru four external devices. Priority assignment may be provided for more than four devices by using additional M736 modules for each additional group of four devices. All M736's in a particular priority system would utilize the same device code.

THEORY OF OPERATION

Basically the M736 module consists of the following:

1. The M103 device selector function.
2. A Bit Time State-3 (BTS-3) input.
3. Four priority input lines.
4. Priority enable line, input and output.
5. Five groups of six gates, each of which is capable of being hard wired to provide address information to locate subroutines to service the various devices associated with the priority interrupt system. The output of each of these gates is strobed onto the accumulator input bus on lines AC(6) thru AC(11).

SEQUENCE OF OPERATION

The external device activates its skip and/or interrupt FLAG flip-flop. The activation of the FLAG causes two things to happen; (a) The computer's interrupt request line is pulled to ground. This tells the computer that an external devices requires service and requests the computer to jump to an I/O priority interrupt service subroutine as soon as the computer completes its present cycle. (b) The external device FLAG pulls to ground the appropriate hard wired priority line connected to a "D" flip-flop in the M736.

A Bit Time State-3 (BTS-3) pulse from the computer is applied to the clock input of the "D" flip-flop to which the activating device flag is connected, as mentioned in section 1b above, and causes this flip-flop in the M736 to set. If more than one priority devices called to be serviced at the same time, all of the associated priority "D" flip-flops in the M736 would be set at this time. The outputs of the priority flip-flops in the M736 are connected to a priority gate structure which is arranged in such a manner that only one output line will be activated and that line will be associated with the external device with the highest priority.

This activated output of the priority gate structure is applied to one group of six two-input gates which make up the address gate. The other input of each of the six two-input gates of the address gate is hard wired to provide a discrete address which will correspond to the starting location of the particular subroutine associated with that priority request. Each of the six output lines of the activated address gates is applied to one input of a two-input gate of the AC input strobe gate.

The computer now has had time to jump to the priority interrupt service routine and now issues a device selection code corresponding to the hard wired device selection code assigned to the M736 priority interrupt modules. This device selection code will pre-enable the IOP gates of the M736 of M736's.

The computer now issues an IOP-2 pulse to the IOP-2 gate of the M736 module. The output of the IOP-2 gate now produces an IOT-2 pulse which causes the "Clear the AC" line of the I/O bus to be pulled to ground, and thereby clears the AC.

The computer issues an IOP-1 pulse to the IOP-1 gate of the M736 module. The output of the IOP-1 gate produces an IOT-1 pulse which is applied to the strobe inputs of the AC input bus gate. As the other inputs of the AC input bus gate are connected to the outputs of the address gate, appropriate lines of the AC input bus (AC 6 thru AC 11) will be pulled to ground thereby loading into the AC the starting address of the subroutine associated with the particular priority I/O device to be serviced.

The computer now refuses to accept any further interrupt requests and jumps to the subroutine with the particular starting address which was loaded into the AC. The service routine of the particular priority device contains an instruction to clear the interrupt flag flip-flop of the particular I/O device and at the end of the subroutine issues the M736 device selector code with an IOP-4 which clears the priority flag flip-flops of the M736. The computer now turns on the priority interrupt system capability which allows the computer to service any future interrupt requests.

USING THE M736 PRIORITY INTERRUPT MODULES

1. Assign a device selection code to the M736 priority system and connect the device selection inputs of the M736 to the proper device selection lines to assure decoding for that code. If more than one M736 is used connect the device selection lines for each M736 in exactly the same manner. Each M736 will use the same device selection code.
   These inputs are: BT2, BS1, BR1, BP1, BN1 and BS2.
2. Connect the enable input, BN2, of each M736 to +3V.
3. Connect the IOP-1 input, BJ1, to the IOP-1 bus line.
4. Connect the IOP-2 input, BM2, to the IOP-2 bus line.
5. Connect the IOP-4 input, BH2, to the IOP-4 bus line.
6. Connect the BTS-3 input, BL1, to the BTS-3 bus line.
7. Connect the outputs of the external I/O device flag flip-flops to the priority

NOTE: In normal operation, IOP-4, is not required as the flag flip-flop in the external priority I/O device is cleared by the subroutine servicing that device. When the flag in the I/O device is cleared, the next BTSO3 pulse will load the disabled flag outpu tinto its respective priority flag flip-flop in the M736 effectively clearing the priority flag flip-flop. flip-flop.

inputs in such a manner as to pull the corresponding priority input line of the M736 to GRD when the device flag is activated. These inputs are as follows:

1st priority	BJ2	1st	M736 Module
2nd priority	BH1	"	"
3rd priority	BF2	"	"
4th priority	BK1	"	"
5th priority	BJ2	2nd	"
6th priority	BH1	"	"

Carry on for additional priority interrupt devices.

8. Assign starting address to the subroutines which will service each priority interrupt device attached to the priority interrupt system. Also assign a starting address for the subroutine to service non-priority devices. Hardwire the various starting address of the service routines as follows:

	AC(6)	AC(7)	AC(8)	AC(9)	AC(10)	AC(11)
Priority 1	BD1	BB1	AP1	AR1	AH1	AF2
Priority 2	AU2	AS1	AN1	AK1	AF1	AA1
Priority 3	AT2	AR2	AM2	AL2	AE1	AB1
Priority 4	BA1	AS2	AL2	AM1	AD1	AC1
NON-Priority	BC1	BE1	BF1	AP2	AJ1	AH2

NOTE: If more than four external I/O devices require priority assignments, the NON-priority address inputs BC1, BE1, BF1, AP2, AJ1 and AH2 of the M736 module used for the first four highest priorities, *must* be connected to GRD. If more than two M736 modules are required all of the NON-priority address lines of each module except the last M736 containing the lowest priorities, must be connected to GRD. The NON-Priority address is hardwired to the NON-Priority address inputs of only the lowest priority M736 module. All un-used priority address inputs must be grounded. Logic 1 level for address may be obtained from module pin BV2 of each M736 module. Lower priority addresses would be hardwired on succeeding M736 modules in the same order hard wired to the second M736 module as follows:

	AC(6)	AC(7)	AC(8)	AC(9)	AC(10)	AC(11)
Priority 5	BD1	BB1	AP1	AR1	AH1	AF2
Priority 6	AU2	AH2	AK2	AD2	AJ2	AE2

9. Connect the AC input bus gate outputs to the AC bus as follows:

	AC(6)	AC(7)	AC(8)	AC(9)	AC(10)	AC(11)
Module Pins	AV2	AH2	AK2	AD2	AJ2	AE2

10. Connect the *Priority Enable* input line BE2, of the M736 with the highest priorities, or the only priorities, to ground.

11. If lower priorities of 5 or more are assigned, connect the Priority output of the module with the higher priorities, Pin BD2, to the next M736 module (with the next following four lesser priorities) Priority enable input pin BE2.

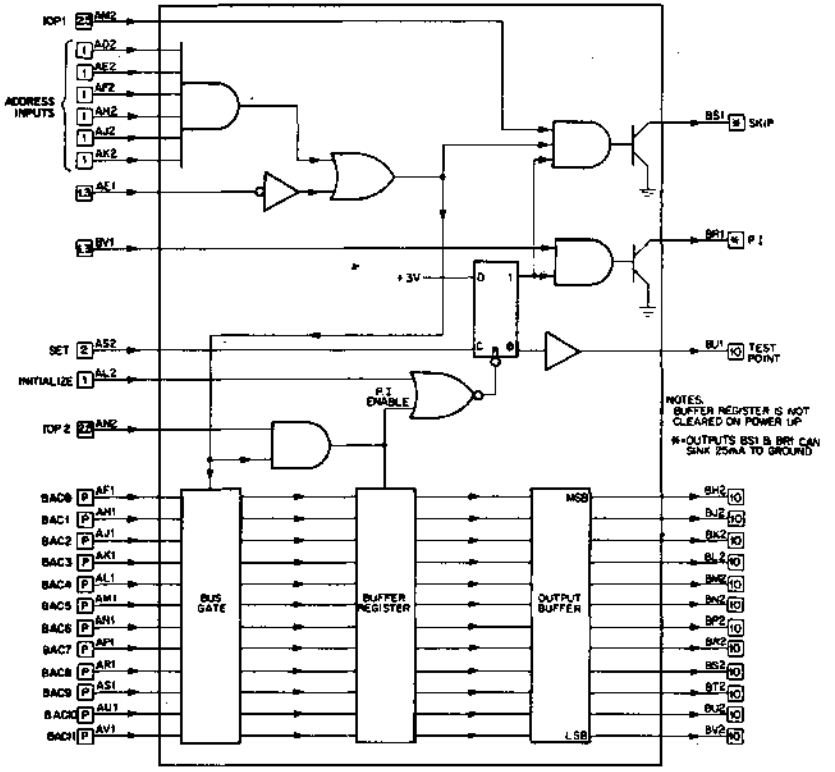
12. Connect the INITIALIZE input, BL2 to the Initialize line of the computer I/O bus.

M737
12-BIT BUS RECEIVER INTERFACE

8-FAMILY POS. I/O BUS

M SERIES

Length: Standard
Height: Double
Width: Single



Volts	Power mA (max.)	Pins
+5	300	AA2, BA2
GND		AC2, AT1, BC2, BT1

The M737 12-Bit Bus Receiver Interface is completely contained on a double height, single width module.

The M737 was designed primarily to receive and store in a buffer register twelve parallel data bits from the positive bus of the PDP-8/I or PDP-8/L. The M737 is pin compatible with the B738 Counter-Buffer Interface, the M107 Device Selector and the M108 Flag Module. The 12-Bit Bus Receiver Interface, M737, consists of three basic sections: device selector, flag, and buffer register section.

Device Selector Section
The device selector section contains six address inputs which are to be connected to the proper BMB bits for address selection. IOP 1 input is used to generate an IOT 1 which is used internally to test the flag. The output of flag test gate is connected directly to the skip bus with an NPN transistor. The output of the address selection gate is connected to the bus gate of the buffer register section and functions as an option select level. IOP 2 is used for two purposes. It is internally connected in such a manner as to clear the flag and to load the buffer register with the contents of the BAC lines.

The Flag Section
The flag section is used to generate a programmed interrupt. The flag flip-flop may be set by a level shift from low to high (a positive going voltage) applied to the set input at pin AS2. The output of the flag is connected to the P. I. line by way of a P. I. enable gate and an open collector NPN transistor. The output of the flag is also connected to pin BU1. The flag is reset by IOP2 applied to pin AN2 or by initialize pulses applied to Pin AL2.

Buffer Register Section
Data from the bus is applied to the inputs of the bus gate. The bus gate prevents the buffer register from loading the bus when M737 is not addressed. The bus gate is enabled by the option select level derived internally from the output of the device selector section. The buffer register is loaded by jam transfer upon the command of an IOT2 instruction. The output of the buffer register is buffered by the use of TTL circuitry.

Inputs: All inputs which receive positive bus signals are protected against negative voltage undershoot. AE1, BV1 represent 1.25 TTL unit loads. These two inputs need not be tied to a logic 1 source when not used.

AM2, AN2 represent 2.5 TTL unit loads.

AS2 represents 2 TTL unit loads.

All other inputs represent 1 TTL unit load.

Outputs: BS1, BR1 will sink 25 MA to ground. Voltage applied to these outputs must not be allowed to exceed +20 Volts. These outputs are protected against negative voltage undershoot and consist of open collector NPN transistors.

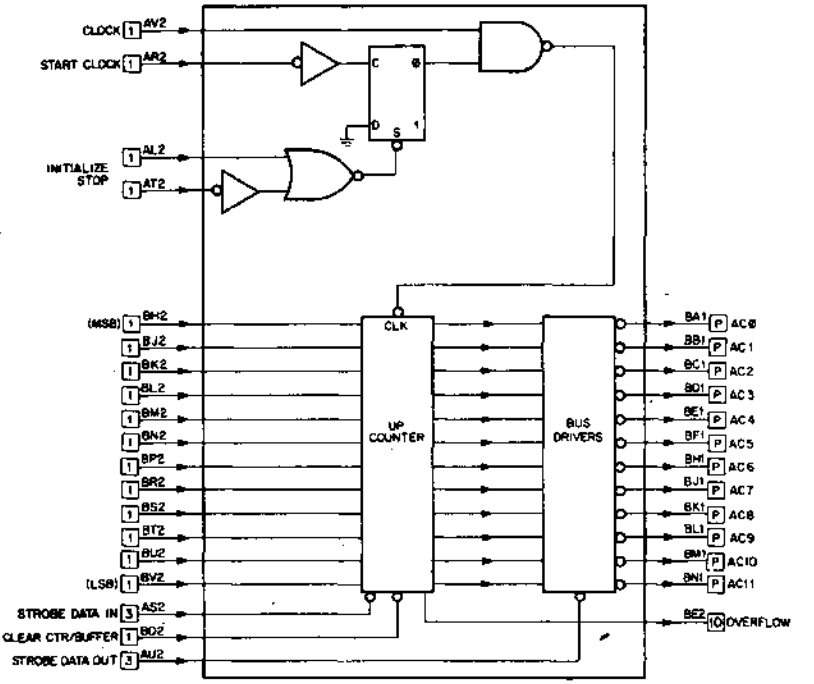
All other outputs will drive 10 TTL unit loads.

M738
COUNTER-BUFFER INTERFACE

8-FAMILY
POS. I/O BUS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	*	AA2, BA2
GND		AC2, AT1, BC2, BT1

*250 mA—no strobe onto bus
370 mA—during bus strobe

The M738 provides a 12-bit binary up-counter that can be read to the positive external I/O bus of a PDP-8/I or PDP-8/L. The counter can be cleared or preset to a starting value by a jam transfer from an external device. When a count enable flag is set, the counter operates as an up-counter in response to external clock pulses. The content of the counter can be strobed to the I/O bus through data gates under program control.

APPLICATIONS

- Interfacing a counting register to I/O bus
- Parallel buffered data transfer to I/O bus

FUNCTIONS

Loading Counter/Buffer: The 12-bit counter/buffer consists of three MSI, 4-bit presetable counters connected in tandem. Twelve parallel bits of data may be applied to the data inputs and then transferred into the counter by the application of a LOW level (250 ns or longer) to the STROBE DATA IN pin AS2. This input could be an IOT pulse from an M102 or M107.

Clearing Counter/Buffer: The counter may be cleared by a logic LOW at least 3 μs in duration applied to the CLEAR COUNTER/BUFFER input pin BD2. The requirement of a 3 μs pulse precludes the direct use of an IOT pulse for clearing the counter. If it is *required* to clear the counter by an IOT pulse, an M302 dual delay multivibrator could be used to stretch the IOT pulse length.

Bus Driver: The 12-bit bus driver strobes the contents of the buffer counter onto the bus when a logic LOW is applied to the STROBE DATA OUT pin AU2. The input to the STROBE DATA OUT pin AU2 would normally be an IOT pulse derived from an M103 or M107.

All bus driver outputs consist of open collector NPN transistors which are capable of sinking 25 mA to ground. Voltage applied to these outputs must not exceed +20 volts. The outputs are diode-protected against negative voltage undershoot in excess of −0.9 volts.

CLOCK ENABLE Flip-Flop: The clock enable flip-flop gates clock pulses to the counter/buffer. This flip-flop may be cleared by a logic HIGH pulse to pin AL2 or by a logic LOW to the STOP input AT2. When the flip-flop is cleared, clock pulses applied to the clock input, pin AV2, are not counted.

Counting: Clock pulses may be counted by setting the COUNT ENABLE flip-flop with the application of a logic LOW pulse to the START CLOCK input AR2. The four inputs—CLOCK, START CLOCK, STOP and INITIALIZE—require a minimum pulse width of 50 ns and, therefore, could use IOT pulses derived from the device selectors M103 or M107.

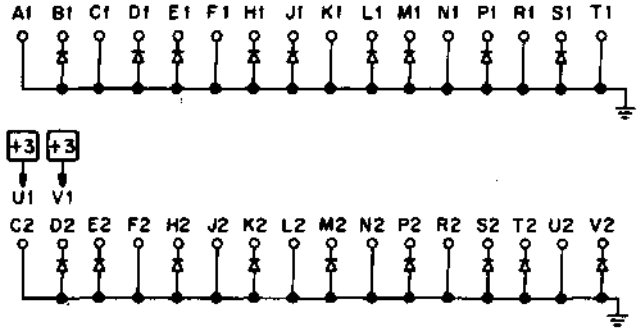
Tandem Operation: At times, it may be desirable to connect two or more M738 module counters in tandem. This may be accomplished by connecting the "overflow" output pin BE2 of the first M738 to the START CLOCK input pin AR2 of the next M738. Also, the signal on pin AR2 must be connected to CLOCK pin AV2. The clear pulse time duration should be an additional 3 μs for each M738 added in tandem: i.e., 24 bits would require a 6 μs clear pulse.

M907
DIODE CLAMP CONNECTOR

8-FAMILY POS. I/O BUS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	10	A2
GND		A1, C1, F1, K1, N1, R1, T1 C2, F2, J2, L2, N2, R2, U2

The M907 is used to provide proper undershoot ground clamps for devices receiving PDP-8/I and PDP-8/L positive I/O bus signals that are not so protected.

The M907 also provides +3 volts for clamping 25 unused inputs. Diode clamps appear on signal leads used in double-sided alternate-ground I/O cables.

Negative Bus: The PDP-8 and PDP-8/S (and some models of the PDP-8/I) employ an I/O bus structure that is logically identical to the positive-logic I/O bus except for the logic levels which are ground and −3 volts. The following M Series functional modules simplify adapting negative-bus computer I/O signals to controllers using positive TTL logic:

M100	Data Output from Negative Bus (pin compatible with M101 which does the same function for the positive bus)
M102	Device Selector (pin compatible with the M103 positive-bus device selector)
M632	Drives negative bus input lines
M633	Drives negative bus input lines (pin compatible with the M623 positive bus driver)

In addition, there is a wide assortment of level converters for two-way compatibility between the negative bus and M Series modules:

M051 M650 M652	Positive in, negative out
M500 M502 M506 M507	Negative in, positive out

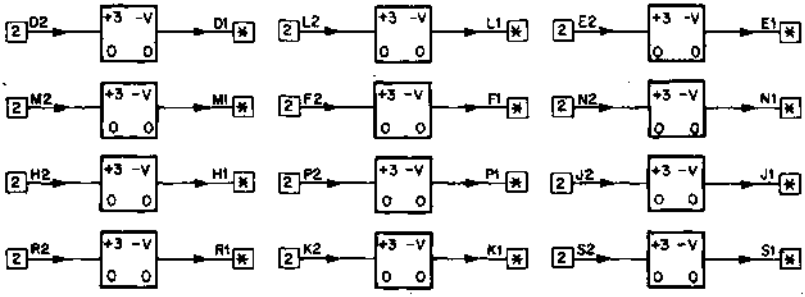
For detailed electrical characteristics and timing on the negative I/O bus, refer to a 1970 (or earlier) edition of the SMALL COMPUTER Handbook.

M051
POSITIVE TO NEGATIVE LOGIC LEVEL CONVERTER

LEVEL CONVERTERS

M SERIES

Length: Standard
Height: Single
Width: Single



*=50 MA, -6V MAX.

Volts	Power mA (max.)	Pin
+5	47	A2
GND		C2
−15	16	B2

The M051 contains twelve level converters that can be used to shift M and K Series logic levels to negative logic levels of ground and −3 volts.

APPLICATIONS
- Interfacing to negative bus PDP computers
- Interfacing to R/B/W Series Logic Systems

Restrictions: Do not use for indicator drive or current sinking.

FUNCTIONS
A grounded input on the driver causes the output to be grounded.

SPECIFICATIONS
The output circuit consists of an open collector PNP transistor that can drive 20 mA to ground. −6 volts maximum may be applied to the output.

M100
BUS DATA INTERFACE

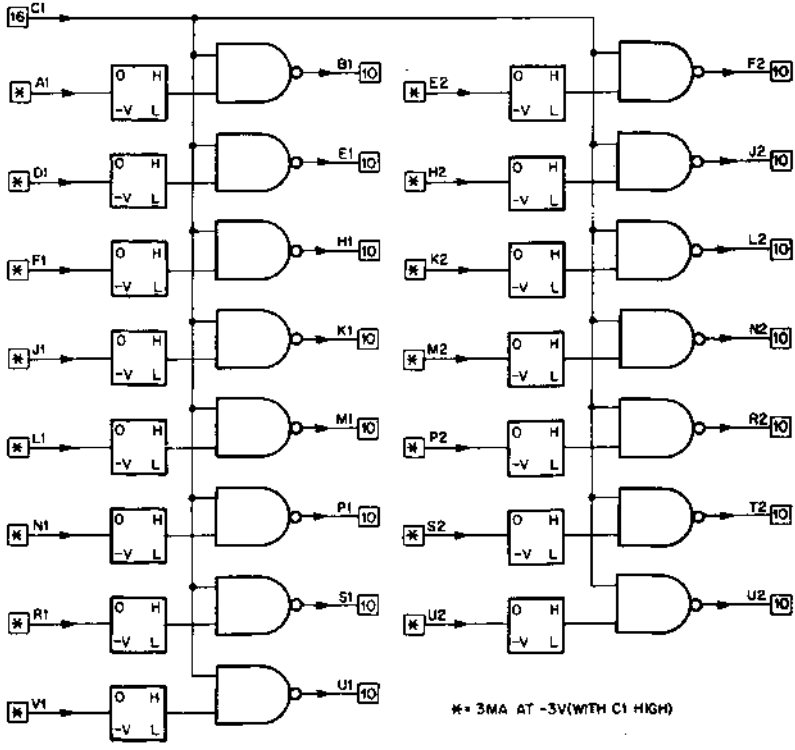
8-FAMILY NEG. I/O BUS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$50



Volts	Power mA (max.)	Pin
+5	60	A2
GND		C2
−15	10	B2

The M100 Bus Data Interface contains fifteen circuits for convenient reception of data from the PDP-8, PDP-8/I negative voltage bus. It is pin compatible with the M101 Positive Bus Data Interface.

APPLICATIONS

- Output data transfer expansion for PDP-8, PDP-8/I

FUNCTIONS

Each input line is connected to M Series levels and gated to the output by the ENABLE signal. Each circuit has the following function:

INPUT	ENABLE	OUTPUT
0V	L	H
0V	H	L
—V	L	H
—V	H	H

(L and H refer to standard M Series Levels of 0 and +3V. —V refers to negative input. (See Threshold Switching Level.)

PRECAUTIONS

The enable line of the M100 cannot be used as a strobe line. The output signals are indeterminate for a period of 200 ns after the enabling line has become true. The enable is intended to be controlled by the option select output of the M102.

SPECIFICATIONS

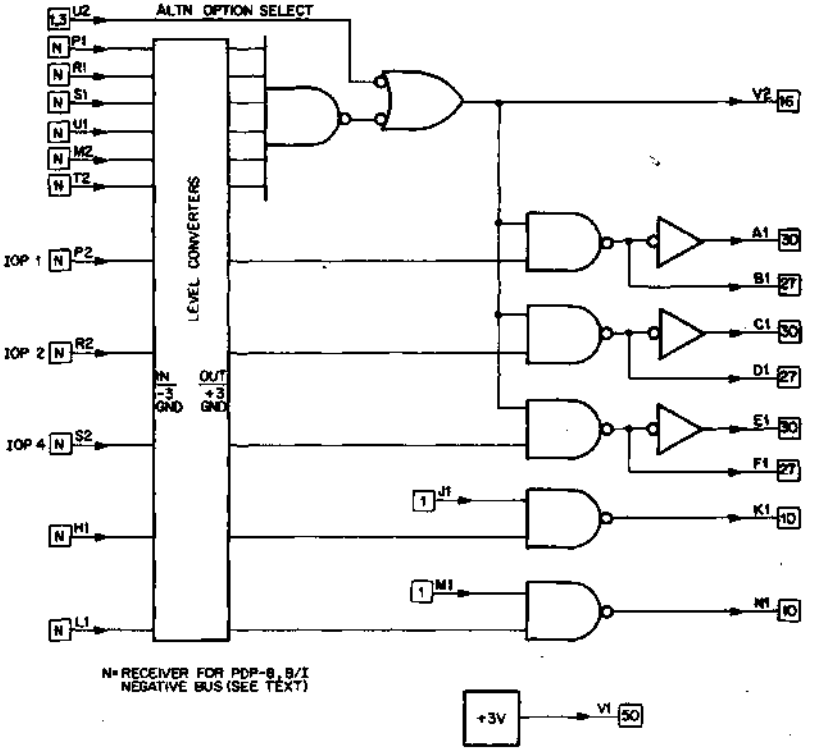
Input Loading: The loading presented to the negative voltage bus differs from the loading using the standard bus modules (i.e., R107, R111) in that the data lines are loaded only if the device is selected.
Threshold Switching Level: —1.5 volts typ.
Propagation Delay: 40 ns typ.

M102
DEVICE SELECTOR

8-FAMILY
NEG. I/O BUS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	130	A2
GND		C2, T1
−15	40	B2

The M102 is used to decode the six device address bits transmitted in complementary pairs on the negative BMB bus of the PDP-8, PDP-8/I. The outputs of the M102 are compatible with M Series TTL logic. The M102 is pin compatible with the M103 Positive bus device selector with the exception of the address inputs.

APPLICATIONS

- Design of custom M Series interfaces for negative bus PDP-8, PDP-8/I.

FUNCTIONS

OPTION SELECT: The OPTION SELECT output is HIGH when all negative-bus code inputs (P1-T2) are at ground. (Note: PDP-8, PDP-8/I BMB outputs are asserted at ground.) The OPTION SELECT ENABLE input is an M Series level that can override the code input.

IOP ENABLE: When the OPTION SELECT output is enabled, IOP pulses from the computer are gated to output pins A1-F1. Both LOW to HIGH and HIGH to LOW pulse output polarities are provided.

Gated Inverters: Two single-input inverters are provided which function as follows:

Neg. Input (H1, L1)	Gating Input	Output
0V	L	H
0V	H	H
−V	L	H
−V	H	L

SPECIFICATIONS

Negative Input Levels: Negative inputs (−V) are nominally −3V and ground. Threshold Switching Level is −1.5V typ.

Negative Input Loading: BMB input loading is 1 mA, shared among the inputs that are at ground.

IOP Input Loading: P2, R2, S2, H1 and L1

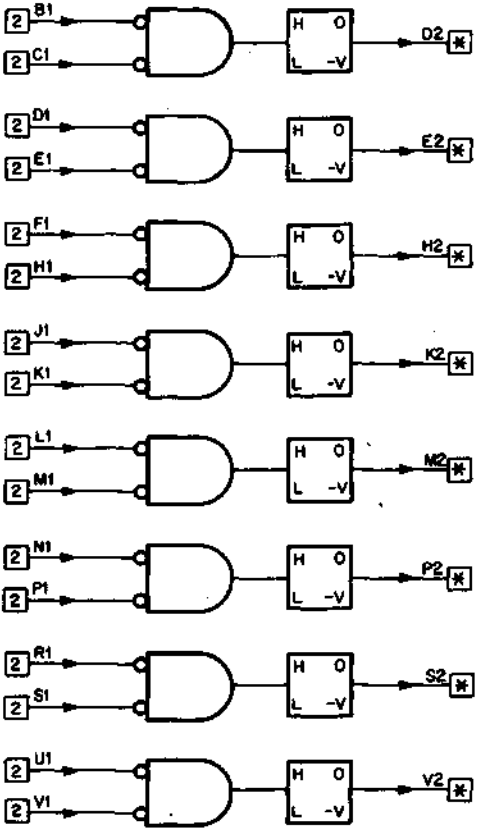
0.2 mA, when V in = 0 volts
0.0 mA, when V in = −3 volts

Propagation Delay: 40 ns typ.

M632
POSITIVE INPUT NEGATIVE OUTPUT BUS DRIVER

8-FAMILY NEG. I/O BUS

Length: Standard
Height: Single
Width: Single



* = SINKS 100 mA AT GND

Volts	Power mA (max.)	Pins
+5	175	A2
GND		C2, T1, F2, J2, L2, N2, R2, U2,
−15	40*	B2

* excluding output current

The M632 contains eight two-input AND gate bus drivers for convenient driving of the negative bus of the PDP-8/I or PDP-8/L.

FUNCTIONS

Each stage operates according to the following truth table:

INPUTS	OUTPUT
LL	0V
LH	−V
HL	−V
HH	−V

SPECIFICATIONS

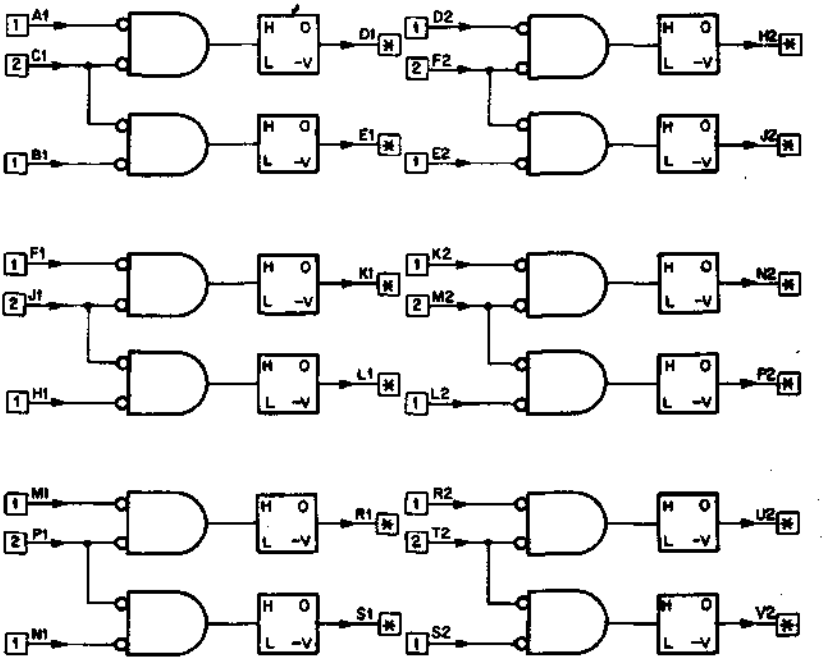
Output Drive: The output is internally clamped to keep it between −3 volts and ground. The output current must not exceed 100 mA.

Propagation Delay: 50 ns max.

M633
NEGATIVE BUS DRIVER

8-FAMILY NEG. I/O BUS

Length: Standard
Height: Single
Width: Single



* = DRIVES PDP-8, PDP-8/I NEGATIVE BUS

Volts	Power mA (max.)	Pins
+5	100	A2
GND		C2, T1
−15	40	B2

The M633 contains 12 bus drivers intended for convenient driving of the negative bus of the PDP-8, PDP-8/I. Each driver consists of an open collector PNP transistor. It is pin-compatible with the M623 positive voltage bus driver.

FUNCTIONS
Each stage operates according to the following truth table:

INPUTS	OUTPUT
LL	0
LH	—V
HL	—V
HH	—V

SPECIFICATIONS:
Output Drive: Each output is an open collector PNP transistor capable of supplying 20 mA from ground. Voltage applied to the output should not exceed —6 volts.

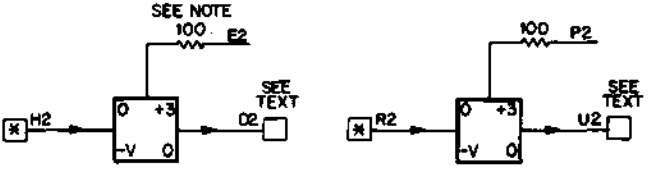
Propagation Delay: Typically 40 ns.

M502
HIGH SPEED
NEGATIVE INPUT CONVERTER

LEVEL CONVERTERS

M SERIES

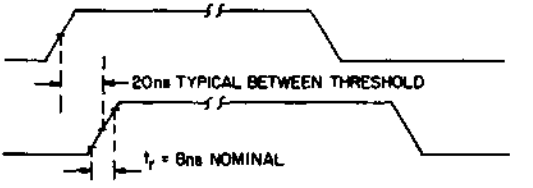
Length: Standard
Height: Single
Width: Single



*=EQUIV. OF 3 MA CLAMPED LOAD

Volts	Power mA (max.)	Pins	NOTE
+5	49*	A2	CONNECT TO OUTPUT WHEN
GND		C2, T1	NOT DRIVING 92Ω COAX.
−15	92	B2	

* Add 44 mA for each 100 ohm resistor connected to outputs.



The M502 contains two non-inverting high-speed signal converters which interface standard negative (−3 volts and ground) logic levels or pulses with M and K Series positive logic modules. These converters provide sufficient current drive at a low output impedance for system interconnections by means of terminated 92-ohm coaxial cable.

FUNCTIONS

Outputs: Each output can drive a terminated 92-ohm coaxial cable and supply an additional 30 mA at +3 volts or sink an additional 30 mA at ground.

SPECIFICATIONS

The converters operate at frequencies up to 10 MHz with typical output rise and fall times of 8 ns. Propagation times for output rise and fall are typically 20 ns.

Input loading is equivalent to a 3 mA clamped load.

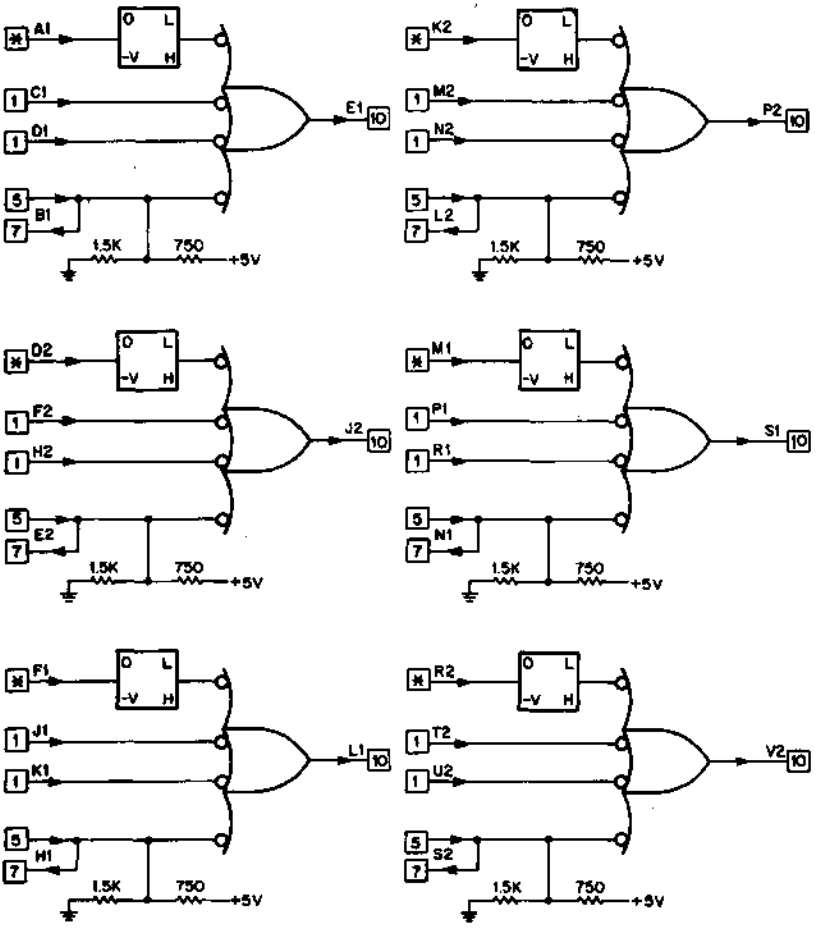
Output rise and fall times depend on the length of coaxial cable driven. When coaxial cable is not driven, switching speeds are increased by connecting the 100-ohm resistor to the output.

M506
MEDIUM SPEED
NEGATIVE INPUT CONVERTER

LEVEL CONVERTERS

M SERIES

Length: Standard
Height: Single
Width: Single



*=10mA AT GND, DIODE CLAMPED

Volts	Power mA (max.)	Pins
+5	81	A2
GND		C2, T1
−15	115	B2

The M506 contains six noninverting signal converters which can be used to interface the negative logic levels or pulses of duration greater than 100 ns to M and K Series positive logic levels of +3 volts and ground.

In addition to the negative level inputs, each converter circuit has three additional NOR inputs for positive logic levels of +3 volts and ground. A source of logic HIGH for unused inputs is provided at each gate.

FUNCTIONS

(Pins A1, etc.)	IN	OUT
	−3V	0V
	0V	+3V

SPECIFICATIONS

These converters operate at frequencies up to 2 MHz with typical rise and fall propagation times of 70 ns and 40 ns respectively.

All negative level inputs (A1, D2, . . . R2) present a 10 mA load at ground.

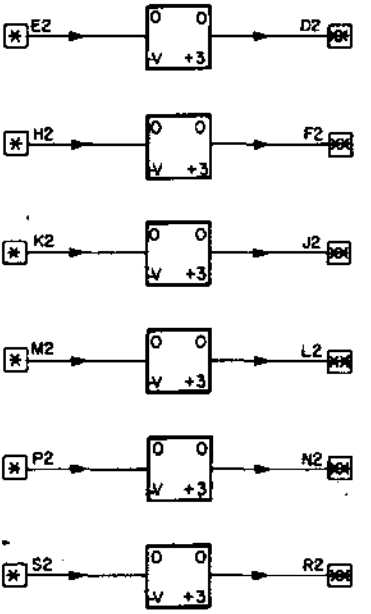
> **Caution:** These inputs are diode-clamped to −3 volts; input voltages greater than −3 volts may draw excessive current.

M507
MEDIUM SPEED
NEGATIVE BUS CONVERTER

LEVEL CONVERTERS

M SERIES

Length: Standard
Height: Single
Width: Single



* = 10 mA CLAMPED LOAD
** = SINKS 100 mA TO GND; +20V MAX.

Volts	Power mA (max.)	Pins
+5	42	A2
GND		C2, T1
−15	115	B2

The M507 contains six inverting level shifters which will accept −3V and GND as inputs. The input to each level shifter consists of a 10 mA clamped load and is diode protected against positive voltage excursions.

The output consists of an open collector NPN transistor. The output of each level shifter will sink 100 mA to GND.

The output transistor is protected against negative voltage excursions by a diode connected between the collector and GND. The output rise is delayed by 100 ns for pulse spreading.

APPLICATIONS

The M507 is used to convert negative voltage logic levels or pulses of duration greater than 100 ns to M Series levels (or pulses).

FUNCTIONS

INPUT	OUTPUT
GND	GND
−3V	+3V

SPECIFICATIONS

Input loading is equivalent to a 3 mA clamped load.

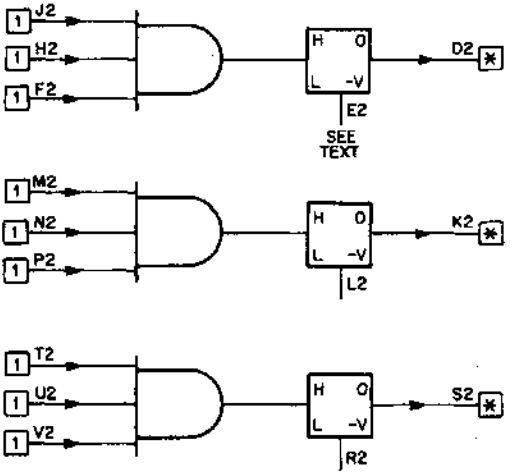
Each output can sink 100 mA to GND. Maximum voltage applied to any output is +20 volts.

M650
NEGATIVE OUTPUT CONVERTER

LEVEL CONVERTERS

M SERIES

Length: Standard
Height: Single
Width: Single



*=20 MA AT GND OR -3V

Volts	Power mA (max.)	Pins
+5	37	A2
GND		C2, T1
−15	29	B2

The M650 contains three noninverting signal converters which can be used to interface the positive logic levels or pulses (of duration greater than 100 ns) of K and M Series to digital negative logic levels of −3 volts and ground. These converters provide current drive at a low output impedance so that unterminated cables or wires can be driven with a minimum of ringing and reflections.

FUNCTIONS
A positive AND condition at the input gate produces a ground output. If any input is at ground, the converter output is at −3 volts.

SPECIFICATIONS
The converters operate at frequencies up to 2 MHz with maximum rise and fall total transition of respectively 75 ns and 115 ns. By grounding pin E2 (L2 or R2) the rise and fall total transition times can be increased to avoid ringing on exceptionally long lines. The converter then operates at frequencies up to 500 kHz with typical rise and fall total transition times of 500 ns.

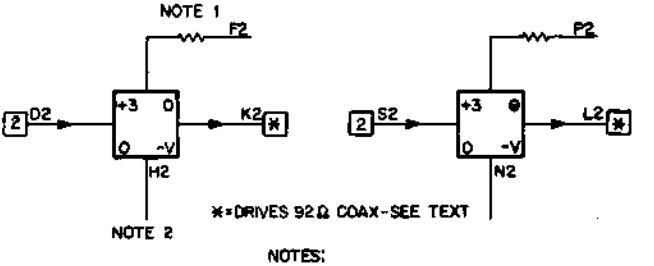
Each output is capable of driving 20 mA at ground and at −3 volts.

M652
NEGATIVE OUTPUT CONVERTER

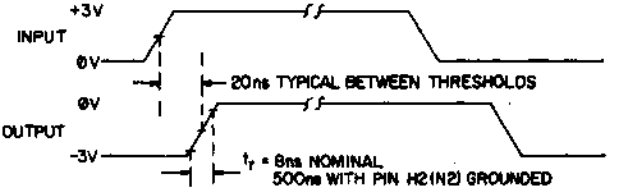
LEVEL CONVERTERS

M SERIES

Length: Standard
Height: Single
Width: Single



NOTES:
1. CONNECT TO OUTPUT WHEN NOT DRIVING 92Ω COAX.
2. CONNECT TO GROUND PIN FOR 500ns RISE TIME



Volts	Power mA (max.)	Pins
+5	122	A2
GND		C2, M2
−15	202	B2

The M652 contains two noninverting high-speed signal converters which can be used to interface the positive logic levels or pulses of the K and M Series to digital negative logic levels of −3 volts and ground. These converters provide current drive at a low output impedance so that system interconnections can be made using terminated 92-ohm coaxial cable.

FUNCTIONS
Each section:

INPUT	OUTPUT
L	−3V
H	0V

SPECIFICATIONS

Timing: The converters operate at frequencies up to 10 MHz with typical output rise and fall times of 8 ns. Propagation times for output rise and fall are typically 20 ns. The slope of the output transition can be decreased by grounding an internal RC network, to avoid ringing on exceptionally long lines. The converter then operates at frequencies up to 1 MHz.

Inputs: Positive logic levels of 0 and +3 volts (nominal). Input signals more positive than +6 volts will damage the circuit.

Outputs: Each output can drive terminated 92-ohm coaxial cable and supply an additional 20 mA at ground or sink an additional 20 mA at −3 volts. Output rise and fall times are dependent on the length of coaxial cable driven. When coaxial cable is not driven, switching speeds will be increased by connecting the 100-ohm resistor to the output.

PDP-11 INTERFACING

The PDP-11 family of computers are the most popular medium-sized systems in the industry. PDP-11s can be found in hundreds of applications, from real-time data acquisition and control to management information systems. All models of the PDP-11 family share one common feature: all signals between the processor, memory, and peripherals are transferred via the UNIBUS. This section is presented in two parts: (1) Basic UNIBUS Interfacing and (2) PDP-11 I/O Modules.

Basic UNIBUS Interfacing

The UNIBUS is a single, common path that connects the processor, memory, and peripherals. (See Figure 1.) Each register (data source or data destination) in each peripheral device is assigned an address to distinguish among the individual peripherals connected to the UNIBUS. This address is analogous to a memory location and permits instructions to act upon device registers as memory locations. There may be only one controlling device on the UNIBUS at any given time because of the system architectural configuration. This device is termed the Master and devices controlled by the Master are termed the Slaves. Devices may request Mastership by asserting either a Bus Request or a Non-processor Request to the Priority Arbitration Logic of the Processor. The request is honored if it is of a higher priority than any other request. The new Master assumes control of the bus when the current Master relinguishes Bus Mastership. The new Master may then request either to have the processor service the peripheral (BR only) or may initiate a data transfer without processor intervention (NPR or BR).

Interface Types

PDP-11 interfaces can be categorized into three distinct types:

1. Slave—This interface has no provision in its control logic to become Master. It will only transfer data onto and off the UNIBUS by command of a Master device.
2. Interrupt—This interface has the ability to gain Mastership of the bus (BR level) in order to give the Central Processor the address of a subroutine which the processor will use to service the peripheral.
3. DMA—This interface has the ability to gain Mastership of the Bus (NPR level) in order to transfer data between itself and some other peripheral.

A single interface may employ all three of the above types.

Signals on the UNIBUS that are used for programmed and interrupt I/O control are defined in Table 1. For complete information on UNIBUS interfacing, refer to the PDP-11 Peripheral Handbook.

Table 1. UNIBUS I/O Signal Summary

SIGNAL	DEFINITION
A <17:00>*	Address Lines. The 18 address lines are used by the master device to select the slave (a unique memory or device register address) with which it will communicate. Lines A <17:01> specify a unique 17-bit word and A00 specifies the byte being referenced. Peripheral devices are normally assigned an address from within the bus address allocations from 760000-777777 (program addresses, 160000-177777).

*Angle brackets enclose groups of lines; A <17:00> = A17 through A00 inclusive.

SIGNAL	DEFINITION

D <15:00> Data Lines. The 16 data lines are used to transfer information between bus master and slave.

C <1:0> Control Lines. These two bus signals are coded by the master device to control the slave in one of four possible data transfer operations.

C1	C0	Operation
0	0	DATI—Data in
0	1	DATIP—Data In, Pause
1	0	DATO—Data Out
1	1	DATOB—Data Out, Byte

MSYN Master Synchronization. A control signal used by the master to indicate to the slave that address and control information is present.

SSYN Slave Synchronization. The slave's response to the master (response to MSYN).

PA, PB Parity Bit Low (PA) and Parity Bit High (PB). These signals are for devices on the UNIBUS that use parity checks. PB is the parity line for the high-order byte (on D <15:08>) and PA is the parity line for the low-order byte (D <07:00>).

BR <7:4> Bus Request Lines. These four bus signals are used by peripheral devices to request control of the bus.

BG <7:4> Bus Grant Lines. These signals are the processor's response to a bus request. They are asserted only at the end of instruction execution, and in accordance with the priority determination.

NPR Non-Processor Request. This signal is a bus request from a peripheral device to the processor, usually for a DMA transfer.

NPG Non-Processor Grant. This signal is the processor's response to an NPR. It occurs at the end of a bus cycle.

SACK Selection Acknowledge. SACK is asserted by a bus-requesting device that has received a bus grant. Bus control passes to this device when the current bus master completes its operation.

INTR Interrupt. This signal is asserted by a peripheral device once it has become the bus master to start a program interrupt in the processor.

BBSY Bus Busy. This signal is asserted by the master device to indicate bus is being used.

SIGNAL	DEFINITION
INIT	Initialization. This signal is asserted by the processor when power is first applied, when the START key on the console is depressed, when a RESET instruction is executed, or when the power fail sequence occurs. INIT may also be used to clear and initialize peripheral devices by means of the RESET instruction.
AC LO	AC Line Low. This signal starts the power fail trap sequence, and may also be used in peripheral devices to terminate operations in preparation for power loss.
DC LO	DC Line Low. This signal remains cleared as long as all dc voltages are within specified limits. If an out-of-voltage condition occurs, DC LO is asserted by the power supply.

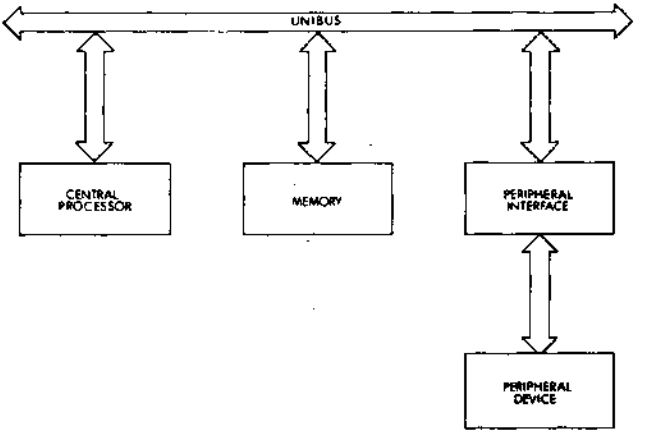


Figure 1. UNIBUS Connections

PDP-11 Input/Output Modules

Detailed description for the following modules are contained here.

M105	Address Selector Module
M1500	Bidirectional Bus Interfacing Gates Module
M1501	Bus Input Interface
M1502	Bus Output Interface
M1621	DVM Data Input Interface
M1623	Instrument Remote Control Interface
M1710	Interface Foundation Module
M1801	16-Bit Relay Output Interface
AR11	Analog Real-Time Module
M7281	Interrupt Control
M783	UNIBUS Drivers
M784	UNIBUS Receivers
M785	UNIBUS Transceiver
M786	Device Interface
M795	Word Count and Bus Address Module
M796	UNIBUS Master Control Module
M798	UNIBUS Drivers

NOTE

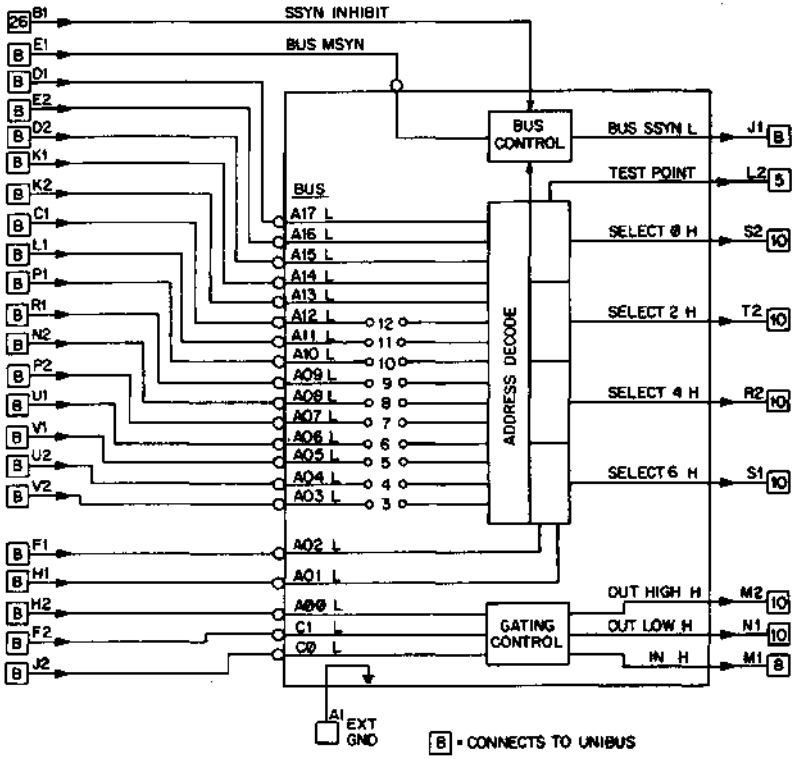
The DECkit11 series of PDP-11 input/output kits offer an added dimension to PDP-11 interfacing. These kits consist of a group of modules (including some of the above) that are installed by the user into a prewired system unit. Additional information on DECkits is contained elsewhere in this Handbook.

M105
ADDRESS SELECTOR

PDP-11
UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	338	A2
GND		C2, T1

The M105 is used in PDP-11 device interfaces to decode the UNIBUS Address and Control lines. It provides gating signals for up to four device registers that indicate a register is being referenced and three control signals that indicate the direction for data flow.

The selector decodes the 18-bit adress A <17:00> as follows: A <17:13> defines the section of the address map that is assigned to peripheral devices and must all be asserted. A <12.03> are determined by jumpers on the card.

When the jumper is "in" the selector will look for a zero in the binary equivalent of the register address on that address line. A02 and A01 are decoded to provide one of the four SELECT outputs. A00 is for byte control.

Signals for gating control are determined by decoding A00, C1, and C0. The signals obtained are: IN, OUT LOW, and OUT HIGH.

Instruction*	Corresponding M105 Output
DATI or DATIP	IN
DATO	OUT HIGH and OUT LOW
DATOB with A00 = 0	OUT LOW
DATOB with A00 = 1	OUT HIGH

*DATI, DATO, DATOB, DATIP are not PDP-11 instructions. They are names given to the various C-line combinations which are automatically configured by the processor for each instruction.

IN is used to gate data from a device register onto the bus. OUT LOW is used to gate D <07:00> from the bus into the low byte of a device register. OUT HIGH is used to gate D <15:08> into the high byte of a device register.

With respect to the bus master, the M105 is actually the "slave" in the relationship when a data transfer occurs on the UNIBUS.

SSYN is asserted whenever it sees its address being referenced and MSYN is asserted. SSYN is negated when MSYN is negated. There is an approximate 100 nsec delay between receiving MSYN and the assertion of SSYN to allow for decoding. Additional capacitance can be added to the delay circuit to increase this time, if desired. A practical maximum is a 1000 pf capacitor which will produce approximately 400 nsec of delay. If a longer delay is needed, the SSYN INHIBIT line can be grounded, which will prevent SSYN from being issued at all from the M105. The SSYN signal would then be generated from another source after the desired delay. SSYN INHIBIT can be left open when not used.

EXT GND is used for testing purposes and should be tied to ground in normal operation.

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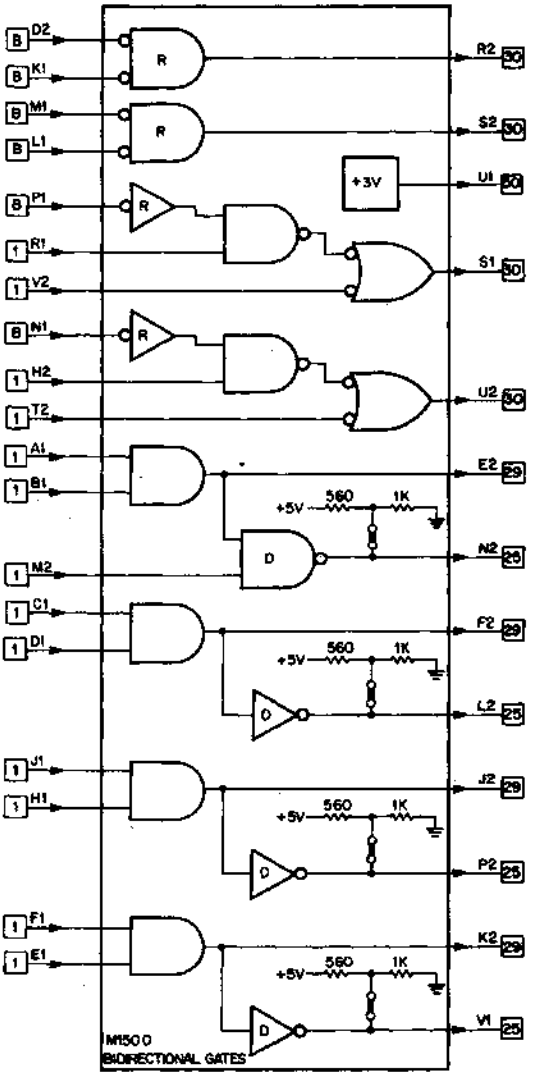
M1500
BIDIRECTIONAL BUS INTERFACING GATES

UNIBUS

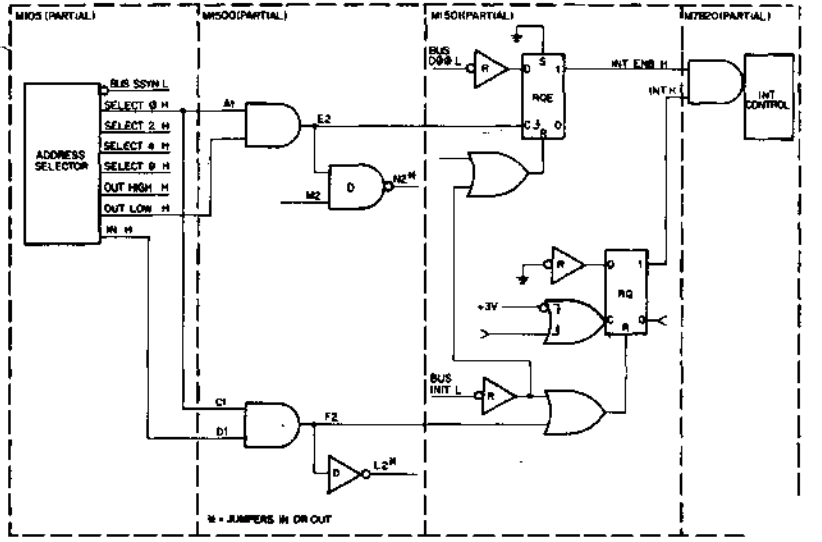
M SERIES

Length: Extended
Height: Single
Width: Single

Volts	Power mA (max.)	Pins
+5	300	A2
GND		C2, T1



This module provides gating arrangements useful for interfacing to the PDP-11 computer. It is designed specifically to provide additional gating and output drive when using the M1501-M1502 Input/Output modules. An example is shown in the following figure.



Using M1500 AND Gates with M1501 in PDP-11 Interfacing.

APPLICATIONS
PDP-11 Interfacing:

1. ANDing SELECT signals with direction signals (OUT HIGH, OUT LOW) to load registers
2. ANDing SELECT signals with direction signals (OUT HIGH, OUT LOW) to form set or reset pulses
3. Receiving the INIT (initialize) signal from the UNIBUS and distributing it via high-power drivers

General-Purpose Use:

1. Providing general-purpose high fan-out drivers
2. Providing a stage of inversion with high fan-out capability

FUNCTIONS
Inputs marked B present one bus receiver load to the UNIBUS. All other inputs are standard TTL; unit loads are shown on the logic diagram.

Output drivers marked D provide open collector outputs with jumpered-in pull-up resistors to enable their use in general logic applications. These outputs may be used to drive UNIBUS lines if the associated jumpers are cut by the user.

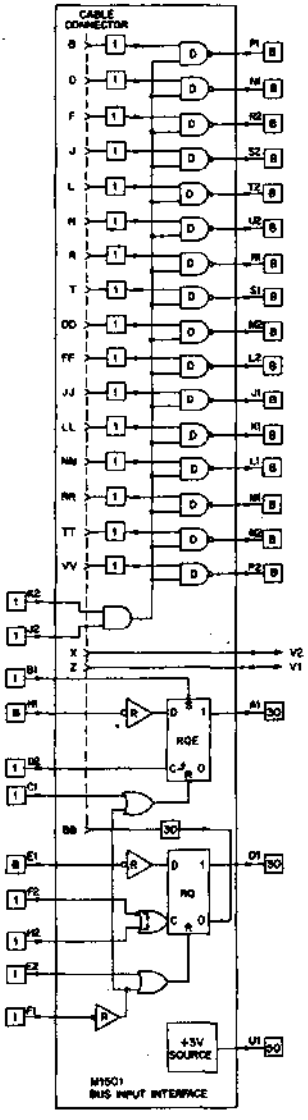
All other outputs provide standard TTL drive as shown on the logic diagram.

M1501
BUS INPUT INTERFACE

UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	300	A2
GND		C2, T1

The M1501 contains 16 bus drivers for interfacing parallel input data to the PDP-11 UNIBUS. The module includes two control flags that can be used for interrupt request and enable. Data inputs from an external device enter a 40-pin flat cable connector mounted on the module itself. All inputs are diode-clamped to ground and +5 volts.

APPLICATIONS

Up to four M1501 modules (64 bits) can be controlled by one M105 Address Selector module, one M7821 Interrupt Control module, and one M1500 Bus Gates module.

FUNCTIONS

Input from Cable: Data is gated from the input connector to the bus when both enabling inputs (K2, J2) are HIGH.

Send/Receive Control Signal: Two additional lines are provided from the cable connector (Pins X and Z) to the module to allow communications between the device and the computer.

Flags: A request flag ($\dot{R}Q$) and a request enable flag (RQE) are included on the M1501. Both flags can be cleared on start-up directly from the PDP-11 INITIALIZE bus line through pin F1. Both flag clock inputs are transition sensitive. The data input to each flag is buffered by a bus receiver; thus, status data can be entered directly from a bus line if desired. The request enable flag clock input responds to a HIGH going transition. The request flag has an input that is sensitive to a LOW going transition and an input that is sensitive to a HIGH going transition. (Whichever input is not used should be connected to the proper logic level to unassert it.) The user is given the maximum degree of freedom to use the request enable flag as a D flop or as an RS flop because all inputs are accessible.

The output of each flag is fully buffered (not shown in diagram) to protect the flag data as well as to provide high output drive.

SPECIFICATIONS

Propagation Time:

FROM	TO	ns (max.)
40-Pin Connector Inputs	Bus Data Outputs	50
Flag Clock Inputs	Flag Outputs	75

M1502
BUS OUTPUT INTERFACE

UNIBUS

M SERIES

Length: Extended
Height: Double
Width: Single

Volts	Power mA (max.)	Pins
+5	750	A2
GND		C2, T1

The M1502 is a versatile buffered output interface for up to 16 data bits, arranged in two 8-bit bytes. The module accepts data from the UNIBUS Data lines and stores it in a 16-bit register. Outputs are supplied both to a 40-pin flat ribbon connector and to the backplane. Open-collector output drivers with pull-up resistors are included on the module. Three flip-flops with type D as well as type RS inputs are provided as flags or synchronizing devices.

APPLICATIONS

Although intended for parallel data output this module may be used to drive indicators or small relays provided the voltage and current limits are not exceeded.

Up to four M1502 modules (64 bits) can be controlled by one M105 Address Selector module, one M7821 Interrupt Control module, and one M1500 Bus Gates module.

FUNCTIONS

Input from Bus: Data is loaded from the bus to the storage register on a positive transition of the loading inputs (AB1 and AA1), which loads the upper and lower bytes respectively providing the enabling input (AM1) is high.

Flags: Three edge-triggered flip-flops are provided. Two of the flags may be triggered by either negative or positive transitions; these supply buffered drive to 40-pin connector outputs. The third flag is triggered by positive-going transitions only. This flag provides an output to the blackplane only.

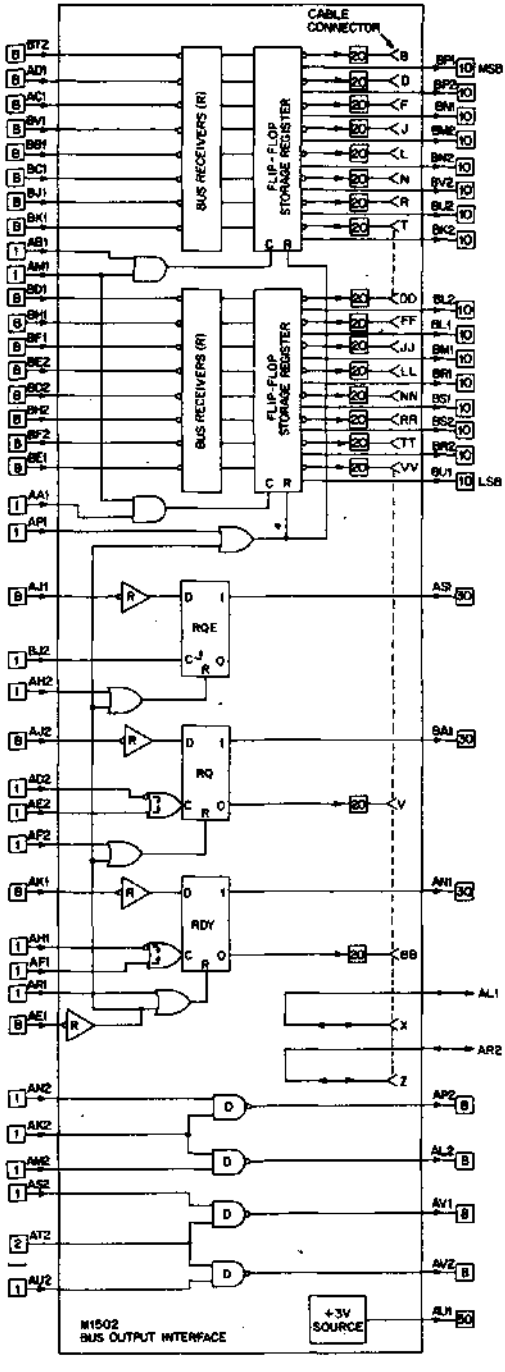
All flags have separate reset inputs and may also be cleared by a common reset line. The set and reset functions occur on logic HIGH levels. Unused inputs should be connected to a logic level that will unassert them. Spare bus drivers are also provided.

Spare Lines: Two additional lines are provided between the cable connector and the module for additional communication between the module and the external device. These lines are diode protected against voltage over shoot below —0.75 volts or above +5.75 volts.

SPECIFICATIONS

Propagation Time:

FROM	TO	ns (max.)
BUS DATA Input	40-Pin Output	100
FLAG CLOCK Input	40-Pin Output	150
FLAG SET or CLEAR Input	Backplane Output	100


CABLE CONNECTOR
BUS RECEIVERS (R)
FLIP-FLOP STORAGE REGISTER
MSB
LSB
RQ-E
RQ
RDY
+3V SOURCE
M1502
BUS OUTPUT INTERFACE

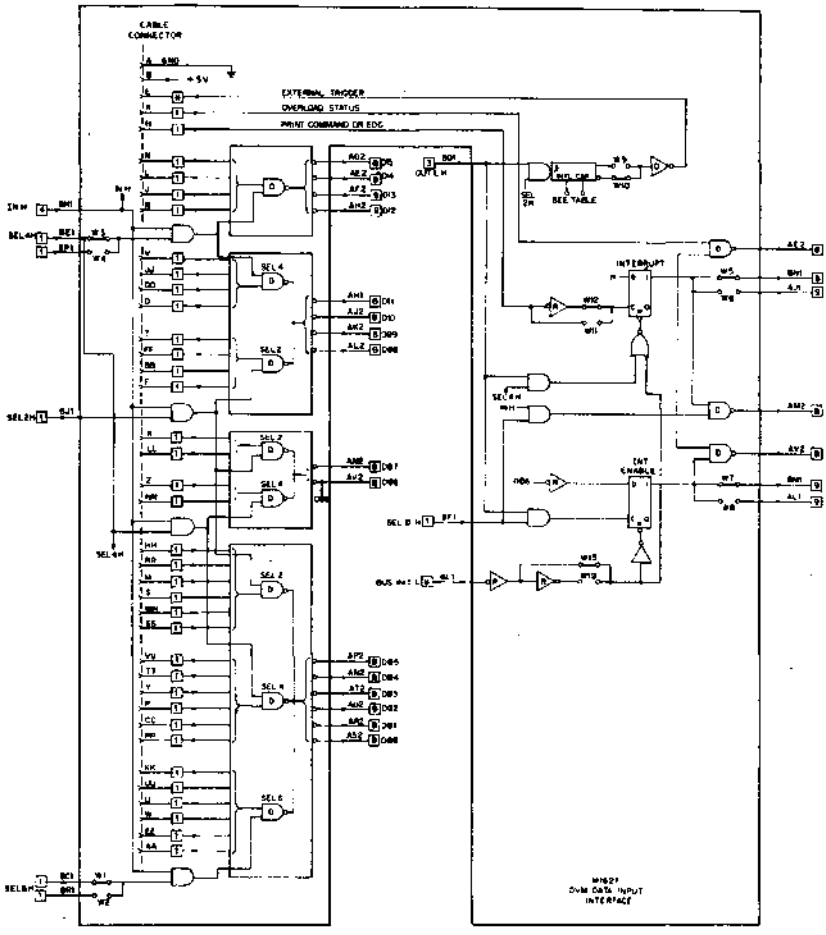
Output Drive: Oututs to the 40-pin connector are supplied by open-collector high-voltage drivers. Resistors (1K ohm) included on the module provide pull-up or current sinking for up to 20 TTL unit loads. If the supplied resistors are removed, the output stages will sink up to 40 mA at logic LOW and will withstand a HIGH level of up to +30 volts. These outputs may therefore be used to drive many types of indicators and even relays. However, if inductive loads are driven, diodes should be wired across each load to bypass inductive kickback.

M1621
DVM DATA INPUT INTERFACE

UNIBUS

M SERIES

Length: Extended
Height: Quad
Width: Single



Volts	Power mA (max.)	Pins
+5	777*	A2
GND		C2, T1

* plus current required by instrument

The M1621 is a PDP-11 interface module containing all the bus drivers and control logic needed to input TTL-level information from several types of digital voltmeters and multimeters. All inputs from the instruments enter a 40-pin cable connector mounted on the module.

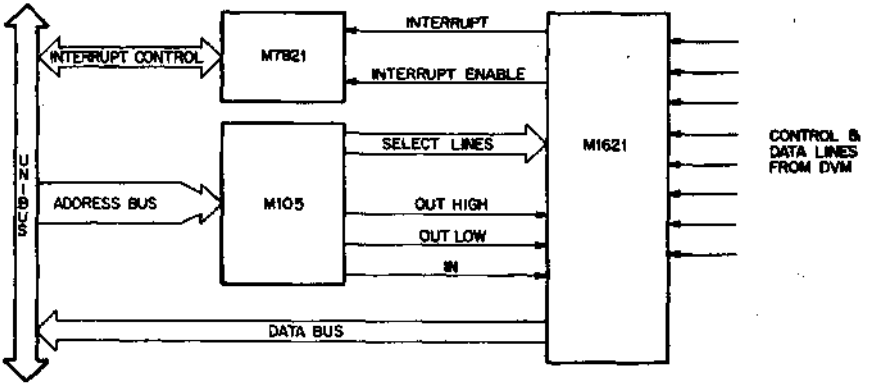
Some of the digital voltmeters and multimeters that can be interfaced by the M1621 are:

Fluke	Model 8200A, 8400A
Hewlett-Packard	Model 3450A, 3480A
Data Precision	Series 2000
Systron-Donner	Model 7110
Dana	Model 4800

The user should first compare the interfacing requirements of his particular instrument with the capabilities of this module. Many instrument manufacturers have various control options which should be chosen carefully for compatibility with the M1621.

APPLICATIONS

For interfacing to the PDP-11, the M1621 must be used with the M105 Address Selector (or equivalent). The M105 decodes the UNIBUS address lines and causes transfer of information through the M1621 under program control. Interrupt circuitry is also built into the M1621 and can be used in conjunction with the M7821 or equivalent. An example of a typical PDP-11 interface using the M1621 is illustrated below.



Used in DECkit 11-M

FUNCTIONS

Bus Drivers: The bus drivers on the M1621 are arranged in separately enabled groups of input words. A 12-bit word normally transfers the DVM's range and function data outputs. Another 16-bit word transfers the first four digits of data output. The third six-bit word might represent the fifth digit of data output plus the overrange and polarity outputs. Each word can be strobed to the computer bus by signals created by the M105. Note that input lines from the DVM are protected by clamping diodes to prevent input signal swings above or below the normal TTL levels.

Flags: The INTERRUPT flag can be set by the PRINT COMMAND or END OF CONVERSION signal from the instrument. Jumpers (W11, W12) are provided which allow the user to select whether the positive or negative transition will set the flag. Interrupt capability is enabled by a second flag INTERRUPT ENABLE, which can be set under program control. Both the INTERRUPT and INTERRUPT ENABLE flag outputs are applied to an M7821 (or equivalent) for computer interrupt. The INTERRUPT flag can be cleared by signals from the M105; both flags can be cleared by computer power up if pin BL1 is connected to the INITIALIZE line.

Jumper pair W5-W6 selects one of two Interrupt signals (INTR or INTR B). With W5 in place and W6 removed, INTR A is selected. With jumpers reversed, INTR B is selected.

Jumper pair W7-W8 selects one of two Interrupt Enable signals (INTR ENB A or INTR ENB B). With W7 in place and W8 removed, INTR ENB A is selected. The reverse selects INTR ENB B.

Status Gates: Status gates on the M1621 give the programmer the ability to check the states of the INTERRUPT and INTERRUPT ENABLE flags and the overload status of the external instrument. These gates are software enabled through the address selector (M105).

Trigger Pulse Generator: For triggering or external equipment, the M1621 contains a one-shot circuit that can be triggered from the device selector (M105). The output pulse width is adjustable from 2 to 12 μs by a trimpot on the module. Longer pulses can be obtained by adding a capacitor at the split lugs on the module. The following equation can be used to determine added capacitance:

$$Tpw = 0.32(RC)$$

where Tpw is in milliseconds, R is in ohms, and C is in microfarads. (The internal trimpot varies from 5.2K to 50 K ohms.)

M1623
INSTRUMENT REMOTE CONTROL INTERFACE

UNIBUS

M SERIES

Length: Extended
Height: Quad
Width: Single

The M1623 is a PDP-11 interface module containing the bus receivers and control logic needed to remotely program several types of digital voltmeters and programmable power supplies. All outputs to the instrument are through a 40-pin cable connector mounted on the module.

Some of the digital voltmeters and power supplies that can be interfaced by the M1623 are:

DIGITAL VOLTMETERS

Fluke	Model 8200A, 8400A
Hewlett-Packard	Models 3450A, 3480A
Data Precision	Series 2000
Systron-Donner	Model 7110
Dana	Model 4800

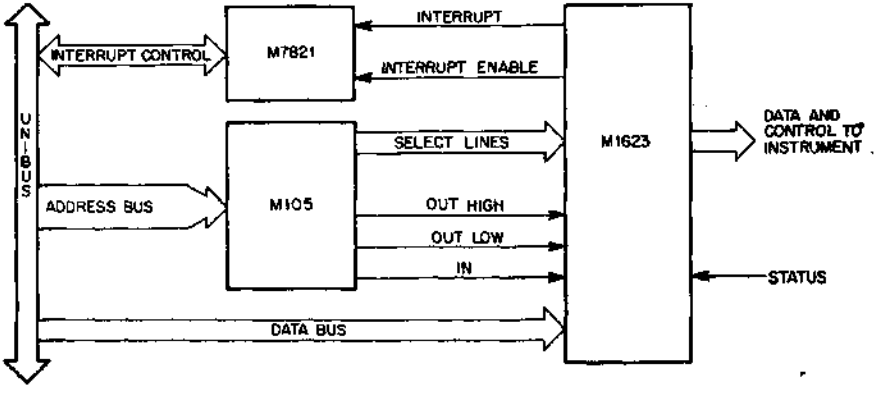
PROGRAMMABLE POWER SUPPLIES

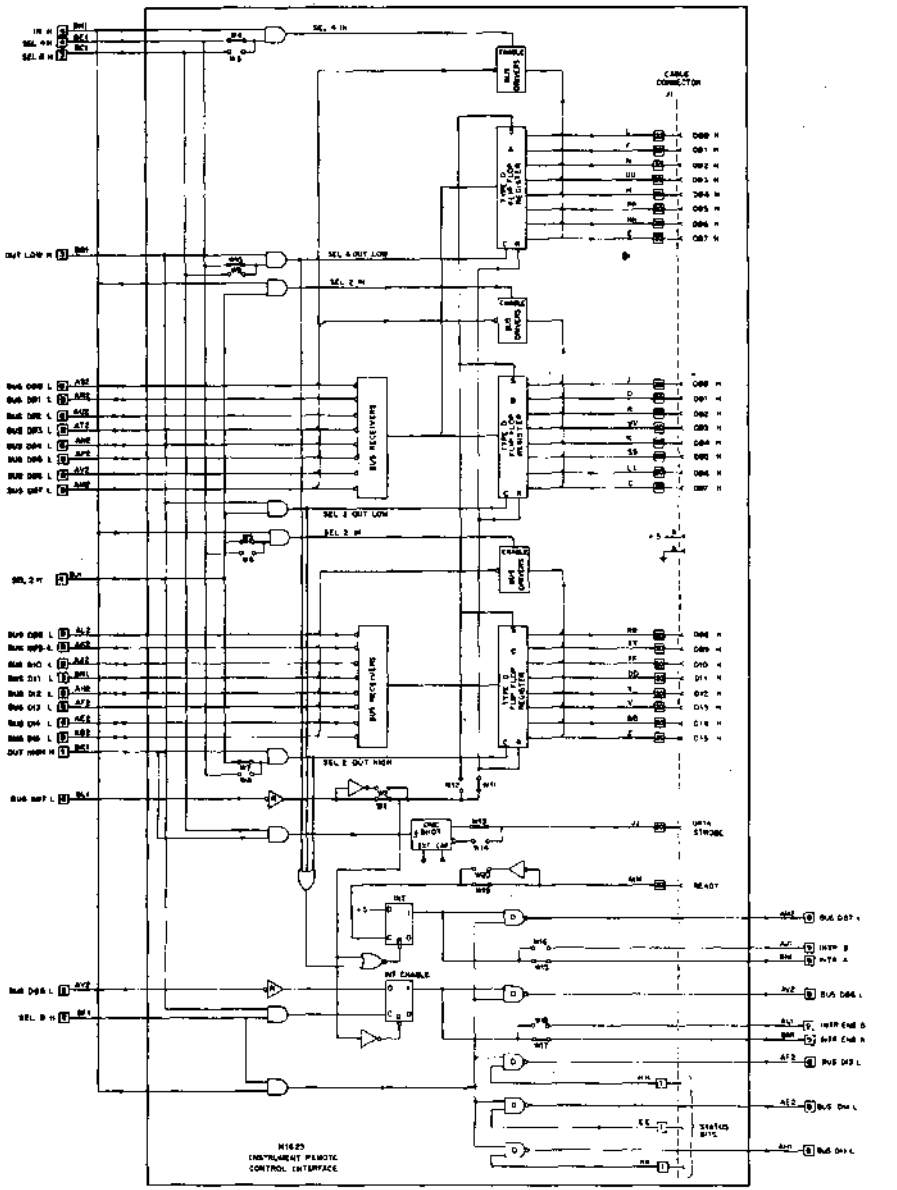
Fluke	Models 4210A, 4216A, 4250A, 4265A
Hewlett-Packard	Model 6130B, 6129B, 6131B

The user should first compare the interfacing requirements of his particular instrument with the capabilities of this module. Many instrument manufacturers have various control options which should be chosen carefully for compatibility with the M1623.

APPLICATIONS

For interfacing to the PDP-11, the M1623 must be used with the M105 Address Selector (or equivalent). The M105 decodes the UNIBUS address lines and causes transfer of information through the M1623 under program control. Interrupt circuitry is also built into the M1623 and can be used in conjunction with the M7821 or equivalent. An example of a typical PDP-11 interface using the M1623 is illustrated below.





FUNCTIONS

Registers: The M1623 contains two registers, one 8-bit and one 16-bit, both interfaced to the computer bus data lines by bus receivers. Data from the computer is clocked into the registers by strobing signals derived from an M105. The user has the option of strobing whole words or 8-bit bytes. All register outputs go to the 40-pin connector and can also be read back by the processor.

Flags: The INTERRUPT flag can be set by the CONVERSION COMPLETE or READY signal from the instrument. Jumpers (W19, W20) are provided which allow the user to select whether the positive or negative transition will set the flag. Interrupt capability is enabled by a second flag, INTERRUPT ENABLE, which can be set under program control. Both the INTERRUPT and INTERRUPT ENABLE flags are applied to an M782 (or equivalent) for computer interrupt. The INTERRUPT flag can be cleared by register-load signals from the M105; both flags can be cleared by computer power-up if pin BLI is connected to the INITIALIZE line.

Jumper pair W17-W18 selects one of two interrupt enable signals (INTR ENB A or INTR ENB B). With jumper W18 in place and W17 removed, INTR ENB B is selected, and the reverse of the jumpers selects INTR ENB A.

Jumper pair W15-W16 selects one of two interrupt signals (INTR A or INTR B). With jumper W16 in place and W15 removed, INTR B is selected, and the reverse of the jumpers selects INTR A.

Register Preset Jumpers: The M1623 also has the option of either setting or clearing the registers during computer power-up. Jumper W11 will cause all register bits to clear on power-up. If W11 is removed and W12 inserted, all register bits will set on power-up.

Status Gates: Status gates on the M1623 give the programmer the ability to check the states of the INTERRUPT and INTERRUPT ENABLE flags and the status of the external-instrument (overflow, remote enable, and latch status, for example). These gates are software enabled through the address selector M105).

Trigger Pulse Generator: For triggering of external equipment, the M1623 contains a one-shot circuit that can be triggered from the device selector (M105). The output pulse width is adjustable from 2 to 12 μs by a trimpot on the module. Longer pulses can be obtained by adding a capacitor at the split lugs on the module. The following equation can be used to determine added capacitance:

$$Tpw=0.32(RC)$$

where Tpw is in milliseconds, R is in ohms, and C is in microfarads. (The internal trimpot varies from 5.2K to 50K ohms.) Jumpers (W13, W14) are provided which allow the user to select either a positive or negative output pulse.

SPECIFICATIONS

Output Drive: Outputs to the 40-pin connector are supplied by open-collector high-voltage drivers. Resistors (1K ohm) included on the module provide pull-up or current sinking for up to 20 TTL unit loads. If the supplied resistors are removed, the output stages will sink up to 40 mA at logic LOW and will withstand a HIGH level of up to +30 volts. These outputs may therefore be used to drive many type of indicators and even relays. However, if inductive loads are driven, diodes should be wider across each load to bypass inductive kickback.

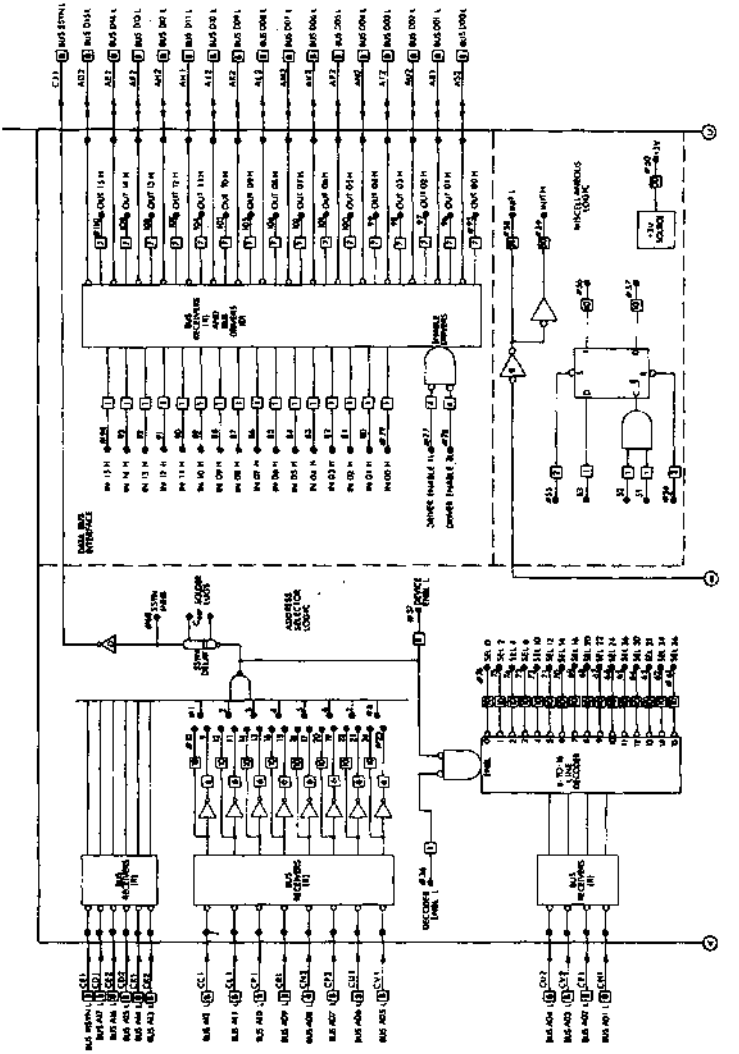
M1710
UNIBUS INTERFACE
FOUNDATION MODULE

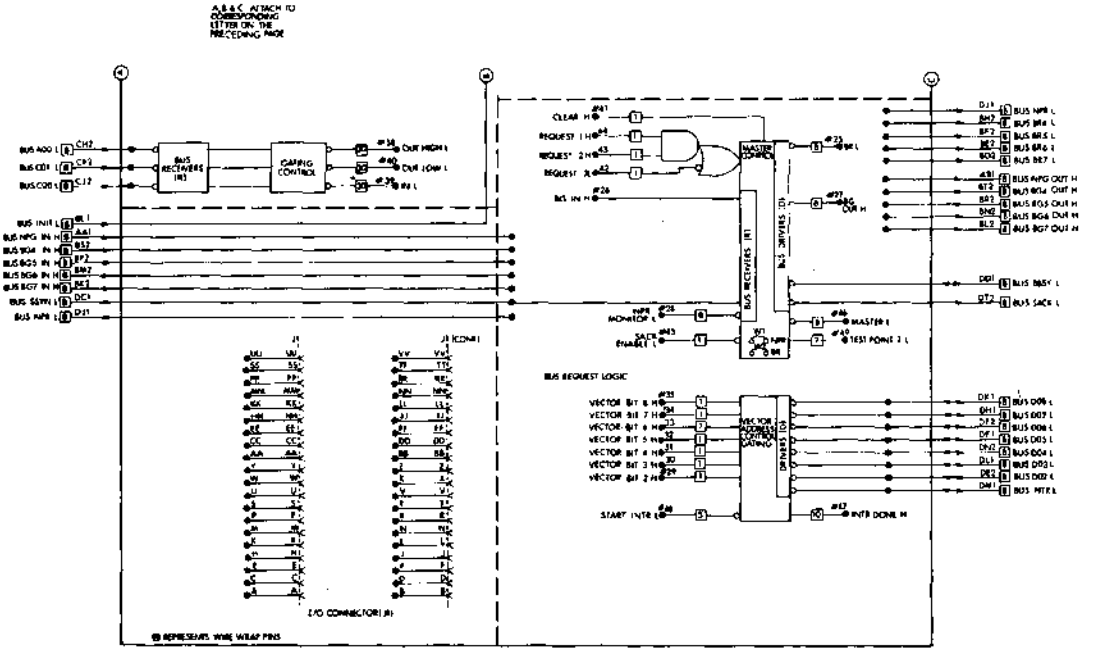
UNIBUS

M SERIES

Length: Extended
Height: Quad
Width: Single

VOLTS	mA TYP	PIN
+5 V @ ± 5%	790	AA2, BA2, CA2
GND		All Pins C, T




A, B & C ATTACH TO CORRESPONDING LETTER ON THE PRECEDING PAGE
BUS RECEIVERS (8X)
GATING CONTROL
BUS RECEIVERS (8X)
BUS DRIVERS (8)
MASTER CONTROL
BUS REQUEST LOGIC
VECTOR ADDRESS CONTROL LATCH
DRIVERS (8X)
I/O CONNECTOR J1
J1 (CONT.)
REPRESENTS WIRE WRAP PINS

DESCRIPTION

The M1710 UNIBUS® Interface Foundation Module is a general-purpose board that provides for the construction of custom interface designs using integrated circuits (ICs). The M1710 lets users build their own interfaces between a wide variety of peripheral equipment and any PDP-11 processor. All essential UNIBUS logic, such as device address selection, interrupt circuitry, and bus receivers and drivers, is provided on the lower portion of the module. The remainder of the board contains IC mounting pads with wire-wrappable pins for custom logic designs. These pads accommodate combinations of all common type of DIP (dual-in-line-package) integrated circuits with up to 40 pins.

The M1710 is a versatile module, ideal for any type of application. The end user, such as a university laboratory familiar with ICs, will appreciate both the capabilities and cost-effectiveness of the module; no additional mounting panel or power supply is required. These features, coupled with the fact that the M1710 is capable of automatic wire wrapping, also should prove valuable to the Original Equipment Manufacturer (OEM) who requires many custom interfaces. And, in all cases, the module is easily adaptable to accommodate any changes in interface design.

The M1710 plugs into any Small Peripheral Controller (SPC) slot of a DECkit11-M Instrument Interface or DD11 Peripheral Mounting Panel. Additionally, it may be used in a system unit such as the BB11-A. Connection to user equipment is made via a cable connector mounted on the M1710 module.

FEATURES

- "Do-it-yourself" interfacing.
- Complete single-card interface.
- Plugs directly into Small Peripheral Controller (SPC) slot.
- Can be used with DECkit11-M Instrument Interface Kit.
- Saves hardware and building costs.
- Preassembled/pretested UNIBUS circuitry eliminates need to build the required bus interfacing functions.
- Wire-wrappable interconnections—compact, 30-gauge wiring used for all IC lead interconnections.
- I/O connection directly to module board—standard 40-conductor cables available.
- All accessories and tools available.
- Accepts all common Dual-in-Line Packages (DIPs); mounts up to 16 of the 14- or 16-pin type plus a multi-use pad set that mounts two 40-pin types, three 24-pin types, four 14- or 16-pin types, or combinations of these.
- Additional bus driver and bus receiver ICs available—special high-impedance devices: DEC 8881, DEC 8640.
- Includes source of +3 V—convenient for tying unused TTL inputs high, etc.

APPLICATIONS

Since more and more devices are becoming available in DIP form, quite complex systems can be built on the M1710. Some typical applications include:

- Multiword input and/or output.
- Programmable instrument interfaces.
- Interprocessor buffers.
- Custom peripheral controllers.
- Interfacing of:
  - Microprocessors
  - A/D converters
  - Multiplexers
  - Counters
  - Shift registers
  - ROM and RAM memories
  - Arithmetic logic units
  - Programmable logic arrays (PLA)

FUNCTIONS

The M1710 can be divided into four functional sections: address selector logic, bus request logic, data bus interface, and miscellaneous logic.

Address Selector Logic

The address selector logic provides gating signals for up to 16 full 16-bit device registers. Addresses which can be chosen by the user range from 760000$_8$ to 777777$_8$. The basic M1710 address selection is similar in function to the M105 Address Selector Module. The input signals for the address selector logic consist of: 18 address lines BUS A<17:00>; two bus control lines, BUS C<1:0>; and a master synchronization lines, BUS MSYN. The address selector decodes the 18-bit address on lines BUS A<17:00>; receives MSYN and issues SSYN.

Bus Request Logic

The M1710 contains the circuitry required to make a bus request and gain control of the bus at either the NPR level or at one of the BR levels. The module also includes circuitry required for transferring a vector address during an interrupt operation.

Data Bus Interface

The M1710 contains standard UNIBUS receivers which provide a buffered bus signal output for each of the 16 data lines OUT 00 H through OUT 15 H. Output drive capability of these receivers is seven TTL unit loads.

The module also includes 16 bus drivers which drive data lines IN 00 H through IN 15 H. Input loading to each driver is one standard TTL load. All 16 drivers have two common gate line enables (DRIVER ENABLE 1 and DRIVER ENABLE 2) which require a logic Low for assertion. Each enable represents four TTL unit loads.

Miscellaneous Logic

The following additional circuitry is also provided on the M1710:

- Inverted and noninverted buffered initialize outputs (pins 58 and 59) capable of driving 28 and 30 TTL unit loads respectively.
- A general-purpose flip-flop with all input and output pins available for wire wrap (pins 51 through 57).
- A +3-volt source (in 50) capable of driving 30 TTL unit loads.

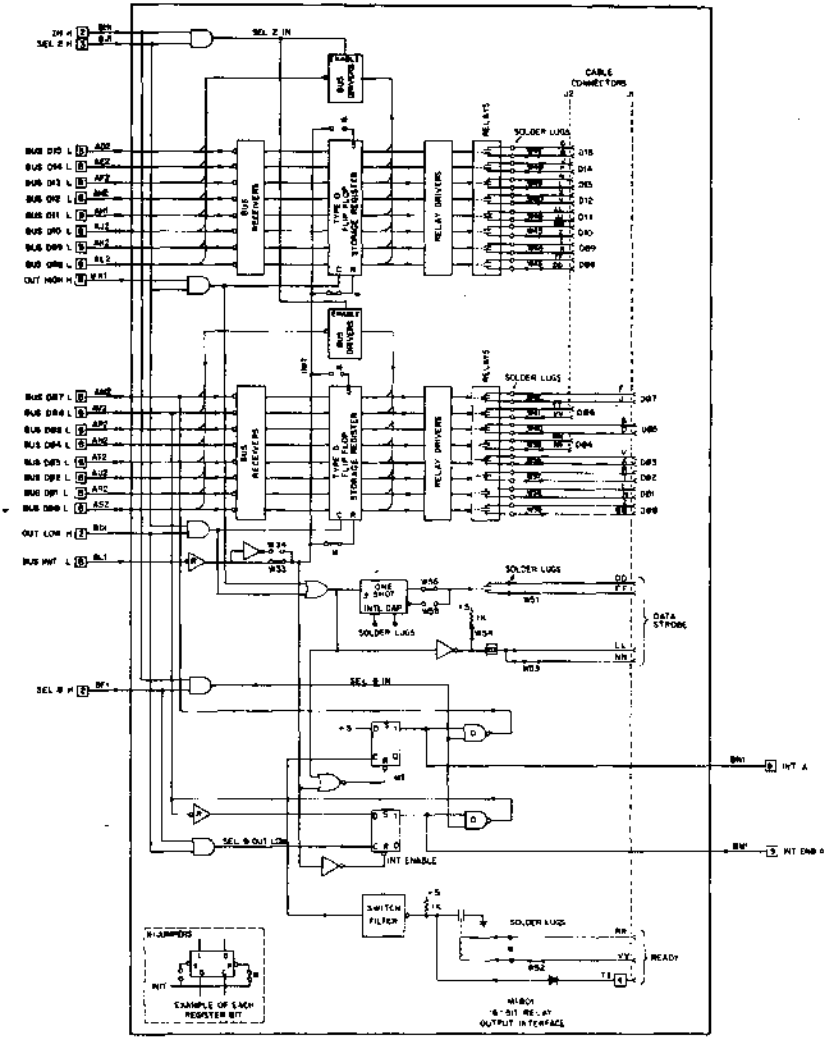
M1801
16-BIT RELAY
OUTPUT INTERFACE

UNIBUS

M SERIES

Length: Extended
Height: Quad
Width: Single

	Power	
Volts	mA (max.)	Pins
+5	1450	A2
GND		C2, T1



The M1801 is a PDP-11 interface module containing the bus receivers, relay drivers, and control logic needed to program 16 isolated single-pole relay contacts. The relay contact outputs are available at two 40-pin cable connectors mounted on the module.

APPLICATIONS

For interfacing to the PDP-11, the M1801 must be used with the M105 Address Selector (or equivalent). The M105 decodes the UNIBUS address lines and causes transfer of information through the M1801 under program control. Interrupt circuitry is also built into the M1801 and can be used in conjunction with the M7821 or equivalent. An example of a typical PDP-11 interface is shown in the M1623 description.

FUNCTIONS

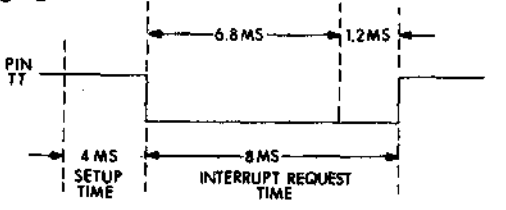
Registers: The M1801 contains two 8-bit read-write registers, both interfaced to the computer bus data lines by bus receivers. Data from the computer is clocked into the registers by strobing signals derived from an M105. The registers have read-back capability for PDP-11 instructions that require a DATIP-DATO sequence. The user has the option of strobing a single 16-bit word or two 8-bit bytes. A logic HIGH (binary ONE) loaded into a register bit activates the corresponding relay output. Each relay output has a jumper and split lugs which allow the user to insert contact filter circuits.

Data Strobe Outputs: Either of the register-loading input pulses will trigger the two DATA STROBE output circuits. One of these outputs is a transistor driver circuit capable of sinking 100 mA (clamped to +5 volts). If jumper W54 is removed, the user can switch up to 20 volts at this output.

The second DATA STROBE circuit contains a one-shot which drives a relay to provide a momentary contact closure. The one-shot has an internal potentiometer for pulse-width adjustment from 5 to 20 ms. External capacitance can be added to split lugs on the module to increase the contact closure time. Jumpers (W56 and W55) are provided which allow the user to choose whether the relay output will be energized on a HIGH or LOW logic level. Both DATA STROBE outputs are available at the 40-pin connector.

READY Relay and Level Inputs: When the interfaced device has received data, it can signal the M1801 that it is ready for another transfer by either energizing the READY relay or by applying a TTL low signal at pin TT of the edge connector J1. The relay has a 5-volt coil rating and pulls in at 4.2 volts. A jumper (W52) and split lugs are provided for users who want to add a voltage divider circuit.

The signal on pin TT must be in the form of a HIGH-to-LOW transition: must be HIGH for min. of 4 ms then go LOW for min. of 8 ms. Contact filtering (6.8 ms min.) is provided for either READY input to prevent false triggering due to contact bounce. The switch filter output sets the INTERRUPT flag, the output of which can be used to request an interrupt. Therefore, continuous interrupts can be made at 12 ms intervals. This timing relationship is shown in the following figure.



Flags: The INTERRUPT flag can be set by the READY signal from the external equipment. Interrupt capability is enabled by a second flag, INTERRUPT ENABLE, which can be set under program control. Both the INTERRUPT and INTERRUPT ENABLE flags can be applied to an M7821 (or equivalent) for computer interrupt. The INTERRUPT flag is cleared by the register-loading signals from the M105; both flags are always cleared by computer power-ups.

Register Preset Jumpers: Each register bit on the M1801 has a jumper which causes that particular bit to clear on power-on. If the user wishes to have a particular bit set on power-on, he must remove the jumper provided and install the particular jumper which sets that bit. Care should be taken to insure that both the set and clear jumpers are not inserted simultaneously.

DATA Bit	Jumper to CLEAR	Jumper to SET
D00	W1	W2
D01	W3	W4
D02	W5	W6
D03	W7	W8
D04	W9	W10
D05	W11	W12
D06	W13	W14
D07	W15	W16
D08	W17	W18
D09	W19	W20
D10	W21	W22
D11	W23	W24
D12	W31	W32
D13	W29	W30
D14	W27	W28
D15	W25	W26

Status Gates: Status gates on the M1801 give the programmer the ability to check the states of hte INTERRUPT and INTERRUPT ENABLE flags. These gates are software-enabled through the address selector (M105).

CAUTION
When the high output voltage or current capabilities of the M1801 are used, the M1801 should be shielded from all computer circuitry.

SPECIFICATIONS
Relay Contact Ratings:

Voltage:	100 V max.
Current:	0.5 A max.
Power:	10 W max. resistive load
Insulation resistance:	1,000 megohms

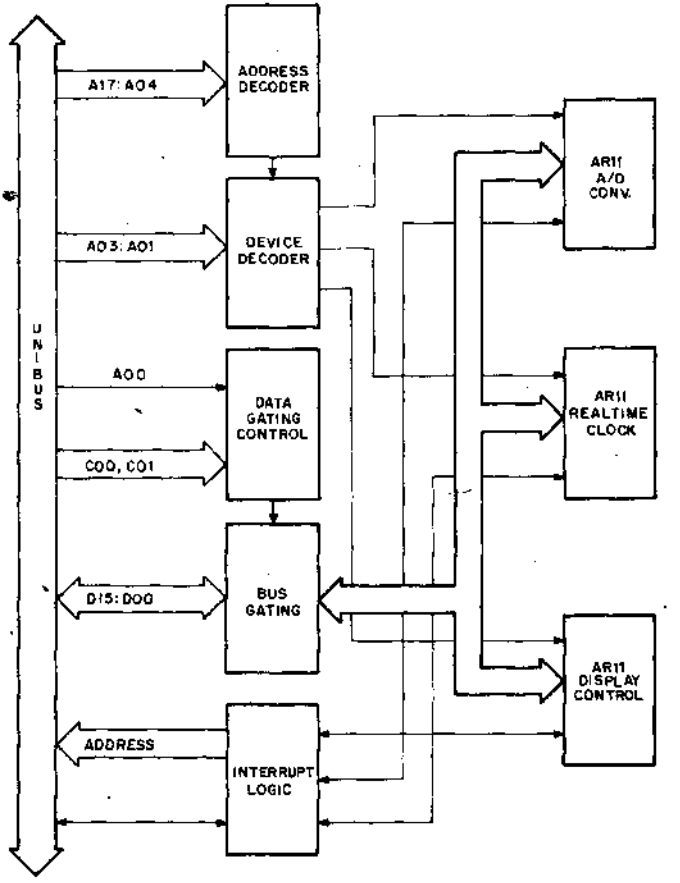
Data Strobe Output:

Current Sinking:	100 mA max.
Voltage:	20 V max.

AR11
ANALOG REAL-TIME
MODULE

UNIBUS

M SERIES



AR11 Block Diagram

DESCRIPTION

The AR11 is a compact analog real-time module for use with the PDP-11 family of computers. Included on the module are a 10-bit analog/digital converted, two 10-bit digital/analog converters, a crystal controlled clock, scope control, a 16-channel multiplexer, and a sample and hold circuit. Operation and selection of functions is under software control.

A/D Converter System

The 10-bit A/D Converter samples analog data at specified rates and allows the program to store the equivalent digital value for subsequent processing. Sample and hold circuitry ensures accurate conversions, even on rapidly changing signals, by holding the input voltage constant until the process is completed. The maximum throughput rate for a single channel is approximately 35 kHz. A 16-channel single-ended multiplexer is included. The input voltage range is program selectable for unipolar (0V to +5V), or bipolar (−2.5 to +2.5V) operation.

Display Control

The display control displays data in the form of a 1024 by 1024 dot array. Under program control, a bright dot may be produced at any point in this array. A series of these dots may be programmed to produce graphical output. The display control is primarily used with DIGITAL's VR14 display. However, it has the capabilities to operate with the Tektronix 602 and 604 display scopes and the 603, 611, and 613 storage scopes. It can also drive an X-Y analog recorder. The display control offers four program-controlled modes in which the scope can intensify a point. There are two 10-bit D/A converters with either a ±5V or a ±0.5V full scale output and all the necessary circuitry for scope control.

Programmable Clock

The programmable clock offers several methods for accurately measuring and counting time intervals or events. It can be used to synchronize the central processor to external events, count external events, measure intervals of time between events, or provide interrupts at programmable intervals. It can be used to start the A/D converter at predetermined intervals or from an external logic input.

The clock operates in one of two program modes: single interval or repeated interval. There are seven programmable frequencies: 1 MHz to 100 Hz, an external input, and an auxiliary input (on the backplane wiring).

An 8-bit counter can be preset for a number of time pulses or events to occur before an interrupt (or A/D counter start) is initiated. This counter can be read from the processor at any time to determine timing status.

PACKAGING

The complete AR11 subsystem electronics are contained on one single hex module that can mount in either of the two center slots of a DD11-B system unit, or within the CPU mainframe assembly. All external connections are made via a Berg connector (supplied with mating plug) which is mounted on an outside corner of the module.

No external analog supply voltages are required. A unique DC to DC converter without transformer uses the +5V logic power to generate the high-quality positive and negative voltages needed by the AR11.

PROGRAMMING

There are 8 registers used for control and data. The address of the first register is selectable in increments of 20, between 770 000 and 777 760. With a starting address of 770 400, the arrangement is:

Register	Address
A/D Status	770 400
A/D Buffer	770 402
Clock Status	770 404
Clock Buffer	770 406
Display Status	770 410
X Buffer	770 412
Y Buffer	770 414
Clock Counter	770 416

There are three interrupt vectors, with the address of the first address vector selectable in increments of 20. If the first vector is at 300, the arrangement is:

Vector	Address	Priority Level
A/D	300	BR6
Clock	304	BR6
Scope Control	310	BR4

SPECIFICATIONS

A/D Converter System

Input voltage range:	0 to +5V, or −2.5V to +2.5V, program selectable
Resolution:	10 bits (1 part in 1024)
Accuracy at 25°C:	±0.1% of full scale
Linearity:	½ LSB
Conversion time:	22 to 24 μsec
Number of input channels:	16
Input impedance:	10M ohms, min.
Settling time; (MUX plus S & H):	8 μsec, max. (5-volt step)

Scope Control

D/A Output voltage range:	−5V to +5V, or −5V to +0.5V, jumper selectable (2 D/A's)
Resolution:	10 bits
Accuracy at 25°C:	±0.1% of 10V full scale, or ±2% of 1V full scale
Scopes controlled:	VR14, Tektronix scopes including storage scopes

Programmable Clock

Clock rates:	1MHz 100 kHz 10 kHz 1 kHz 100 Hz } crystal controlled external logic input auxiliary frequency input
Operating Modes:	single interval repeated interval
Counter size:	8 bits
Preset register size:	8 bits
Accuracy:	±0.005%
External input:	TTL logic
Aux. freq. input:	TTL logic, accessible on backplane

Mechanical

Mounting:	1 hex module slot
User Interface:	Berg connector on the module

Power 4A at +5V

Environment

Operating temperature:	15°C to 52°C, system ambient
Relative humidity:	10% to 90%

SOFTWARE

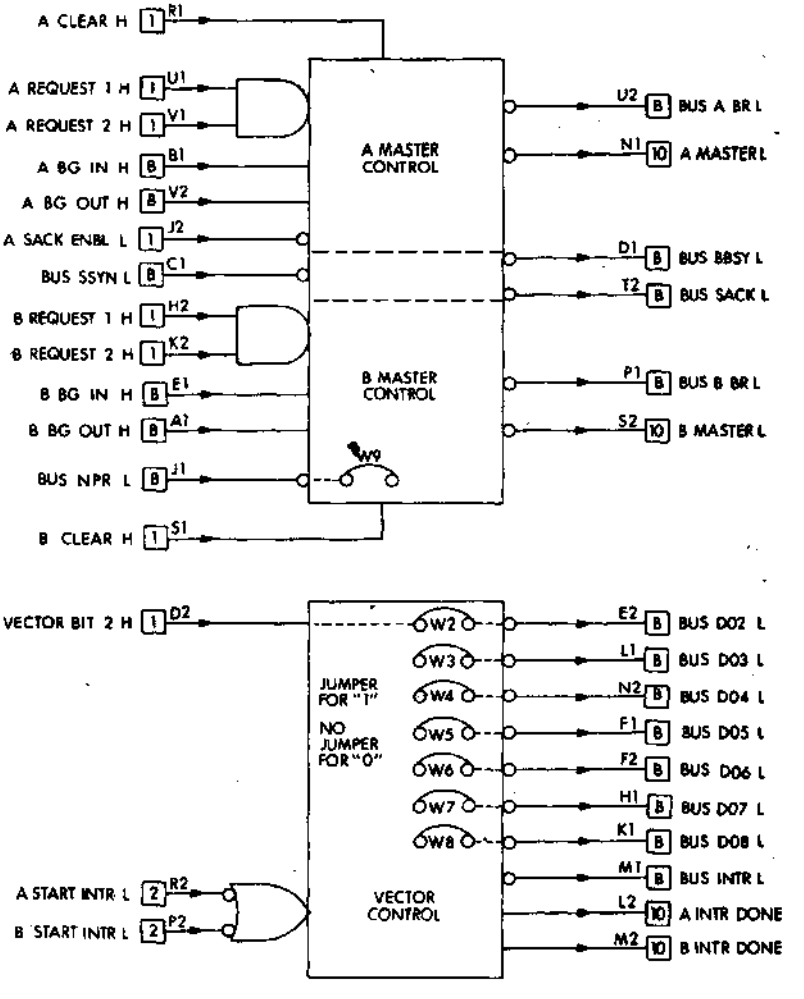
RT11/BASIC
FORTRAN IV
RSX11-M,-D

M7821
INTERRUPT CONTROL MODULE

PDP-11 UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	550	A2
GND		C2, T1

The M7821 Interrupt Control Module is used with the interface logic of a device in the PDP-11 systems. The M7821 allows one or two devices that request an interrupt to gain access to the UNIBUS and become bus master for one or more data transfers. It also provides a vector control circuit to enable the selection of an address in memory at which the device subroutine is stored.

The module consists of an A Master Control, B Master Control, and Vector Control logic. Either of the two master control circuits can be used to generate a Non-Processor Request (NPR) for direct data transfers to memory (DMA) or a Bus Request (BR) which interrupts the current processor program. The A Master Control, however, is normally used for generating the NPR and the B Master Control for the BR. When used as a DMA control, the A Master Control has the ability to perform a burst mode block transfer which allows more than one data cycle to be performed each time the device becomes bus master.

The B Master Control contains logic which can be implemented to allow the monitoring of the bus NPR line. This capability permits an NPR initiated by a device to be honored under certain conditions and the device to gain access to the bus even though a BR from another device has occurred prior to the NPR. A jumper lead can be removed from the module to disable this feature if the B half is used for NPR transfers.

The sequence of interrupt control signals between the M7821 and processor is similar for both the NPR and BR; however, an interrupt signal and vector address is generated after the device becomes master during a BR. The interrupt signal halts the operating program in the processor and the vector address specifies a location in memory where the starting address of the interrupt status routine and a status word is stored.

FUNCTION

The interrupt request generated by a device is received as a High level on either A REQUEST 1 or B REQUEST 1 input. The associated A REQUEST 2 and B REQUEST 2 inputs must be enabled with a High level to generate a bus request. A non-processor request is initiated by the A Master Control and the BUS A BR output is wired to the NPR bus line. The BUS A BR output becomes Low during the request interval. The processor responds to the NPR by issuing a high level to the A BG IN input. The A Master control issues a Low BUS SACK signal to the processor to acknowledge the A BG IN signal and the BUS BBSY signal is asserted Low as soon as the current bus master releases control of the bus to indicate the requesting device is bus master.

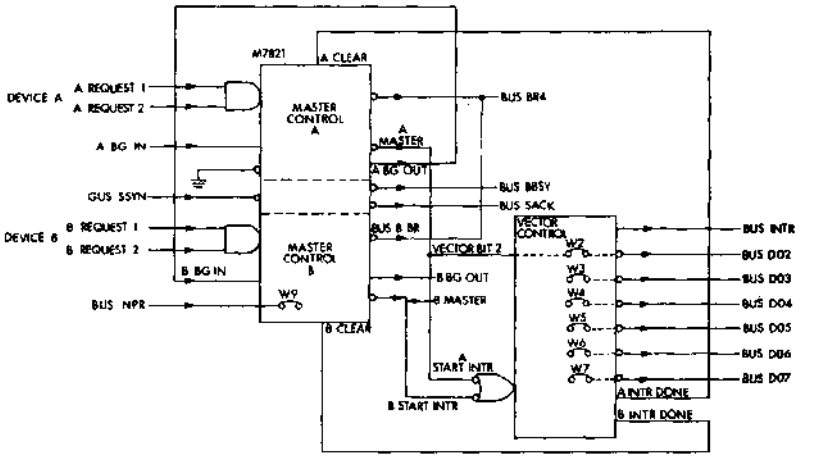
Normally, the BUS SACK signal is returned to a High level after BBSY becomes Low. If more than one data transfer (bus cycle) is required during the period that the device is bus master, the A SACK ENBL input can be connected to a level which remains High until just before the last bus cycle of the burst transfer is started. This level will prevent the processor from issuing a bus grant requesting device until the data transfers have been completed. This insures that the bus will be given to the highest priority requesting device at the end of the burst.

A bus request (BR) is issued by the B Master Control in a similar manner as the NPR. The BUS B BR output of the B Master Control connects to the assigned bus request priority line, BR4 through BR7. After the A Master Control issues a Low to the BUS BBSY line, the vector logic issues a Low BUS INTR signal to the bus interrupt line and transmits the vector address,

as preset by the jumper leads W2 through W7, to the data bus lines BUS D03 through D08. The data from the device which initiated the interrupt request is transferred to memory after the BUS BBSY has been issued by the processor.

APPLICATION

The following diagram shows a typical wiring configuration of the M7821 module. An interrupt request can be initiated from Device A to the A Master Control or by Device B to the B Master Control. The outputs of both master controls can be wired together as shown and connected to the BUS BR4 line; therefore, an interrupt request from either Device A or B will initiate a bus request at the same priority level. The A SACK ENBL input is connected to ground indicating that only one data transfer will be performed each time the device becomes bus master. The bus grant (A BG OUT) connects to the bus grant (B BG IN) where both master controls are connected to the same priority level of bus requests (BUS BR4).



TYPICAL M7821 APPLICATION

All jumpers W2 through W7 are connected on the Vector Control section of the module. The A MASTER output connects to the VECTOR 2 input of the Vector Control circuit. When the A Master Control section of the module becomes bus master, the A MASTER output will be low and the resulting vector address on lines BUS D02 through BUS D08 will contain an octal 100. If the B Master Control is selected, the A MASTER output will be high, producing a vector address of an octal 104. The A MASTER output and the B MASTER output connect to the START INTR inputs of the Vector Control

or gate to initiate the interrupt request on the BUS INTR line. When the data transfer is complete, the INT DONE output of the Vector Control will clear the appropriate master control section previously selected.

WIRING CONFIGURATION

During a BR, the vector address is specified by the information on lines BUS D02 through BUS D08. The address format is indicated below:

JUMPERS	ADDRESS BITS
W2	D02*
W3	D03
W4	D04
W5	D05
W6	D06
W7	D07
W8	D08

*CONTROLLED BY VECTOR BIT 2 INPUT

When a jumper is present between the designated lugs W3 through W8 on the module, a logic ONE will result and when the jumper is removed, a logic ZERO will be present on the corresponding vector address bit. With jumper W2 installed, the state of address bit D02 is determined by the logic level present on the VECTOR BIT 2 input.

Jumper W9 is installed during manufacturing and must be removed when used with early PDP-11/15 and PDP-11/20 without the KH11 option.

M7821 SIGNALS

Inputs (X = A or B Master Controls)

X REQUEST 1 H, X REQUEST 2 H — Both signals must be asserted High to initiate a BR or NPR and remain High until the requesting device is through being bus master. Lowering either of these lines will cause BBSY to be removed. Prior to a new bus request, one signal must become Low before being reasserted.

X BG IN H — Asserted High by the processor in response to a request when the requesting device has the highest priority.

X SACK ENBL L — Connect to ground (Low) when only one data transfer by a device will be performed each time the device becomes bus master. When a burst mode block transfer is done, this line should be held High until just before the last transfer of the block.

BUS NPR L	With jumper W9 connected, a Low on the BUS NPR line from the processor will prevent the B Master Control from transferring a bus grant to another requesting device. Remove this jumper if this section is used for an NPR device.
X CLEAR H	A High transition causes the associated master control to remove the BUS BBSY signal and terminate bus mastership.
VECTOR BIT 2 H	A High input specifies an octal 4 in the least significant digit of the vector address. A Low specifies an octal 0.
X START INT L	A Low transition initiates an interrupt by loading the vector address onto the UNIBUS and producing a (Low) BUS INTR signal.

Outputs

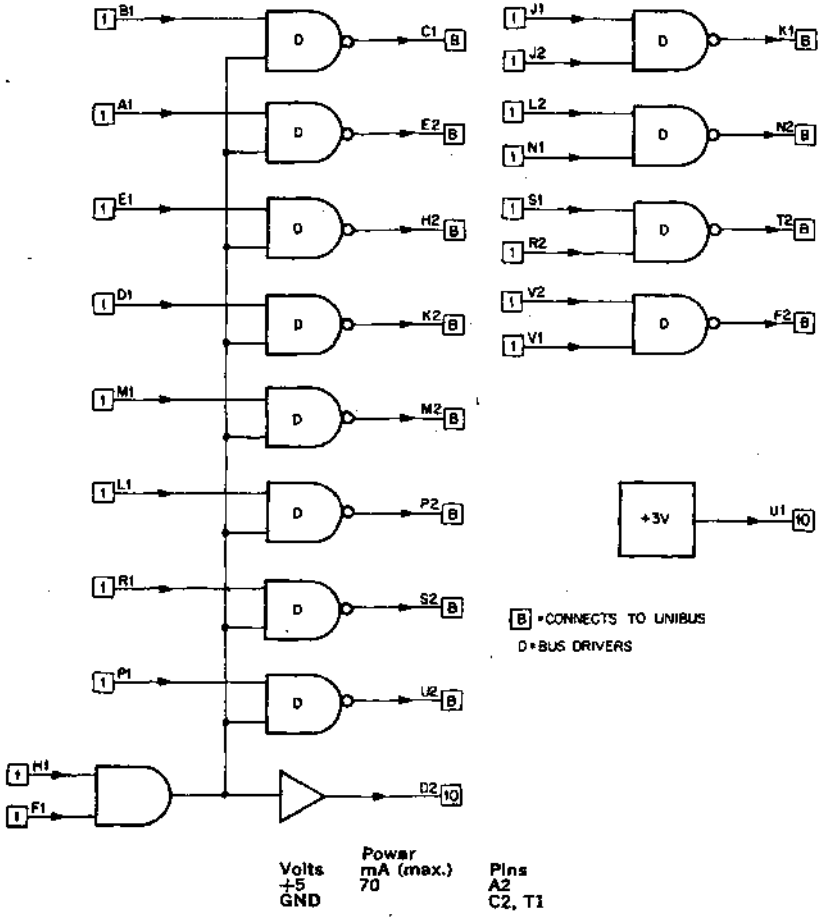
BUS X BR L	Asserted Low when X REQUEST 1 and X REQUEST 2 are asserted to indicate that a device has initiated a BR or NPR. Connect to desired UNIBUS BR or NPR line.
X BG OUT H	Asserted High to transmit the bus grant to the next device on the same priority level.
BUS SACK L	Asserted Low to acknowledge to the processor that the requesting device has received the grant signal and is prepared to become the bus master when the current master releases the BUS BBSY signal.
BUS BBSY L	Asserted Low to indicate that the requesting device is bus master.
X MASTER L	Asserted Low when the associated master control has become bus master.
X INT DONE H	Asserted High at the completion of the interrupt (when BUS SSYN is received).
BUS D02—D08L	Specifies the vector address to the UNIBUS.
BUS INTR L	Asserted Low by the requesting device after it has become bus master to notify the processor that the data lines contain a vector address.

M783
UNIBUS DRIVERS

UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	70	A2
GND		C2, T1

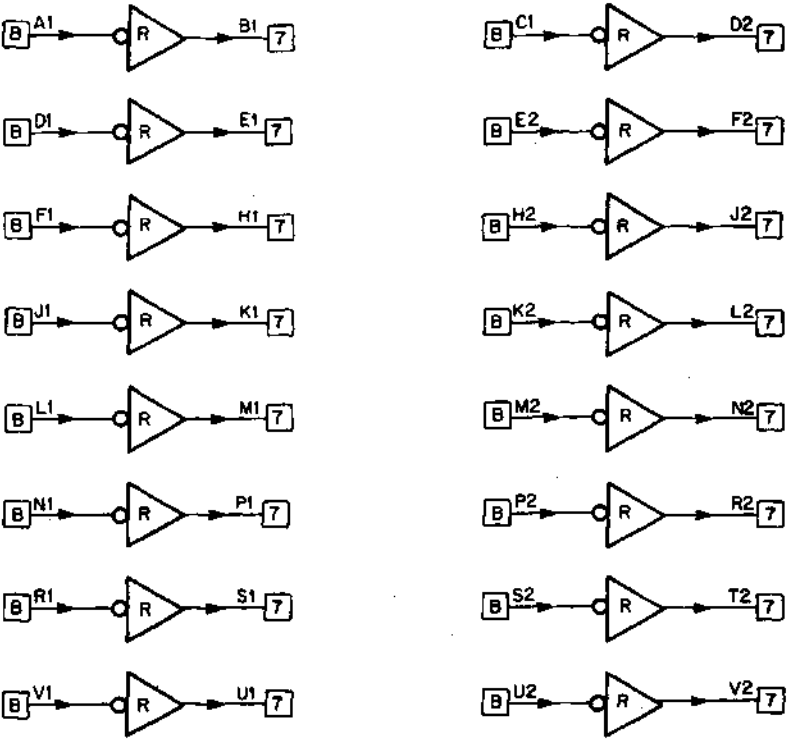
The M783 consists of 12 low-leakage bus drivers to be used as an input interface to the UNIBUS of the PDP-11. Each driver is open-collector and is capable of sinking 50 mA with a collector voltage of less than 0.8 volts. The output high leakage current is 25 microamperes maximum. Pin D2 is a TTL output that allows additional drivers to be controlled by the single enabling gate (inputs H1 and F1). Pin U1 provides +3 volts as a source of logic HIGH for 10 TTL loads.

M784
UNIBUS RECEIVERS

UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	200	A2
GND		C2, T1

R = BUS RECEIVER
B = CONNECTS TO UNIBUS

The M784 consists of 16 high-impedance inverting bus receivers that are used as an output interface from the UNIBUS of the PDP-11.

SPECIFICATIONS

Input Loading: All inputs present one UNIBUS receiver load. (See UNIBUS description.)

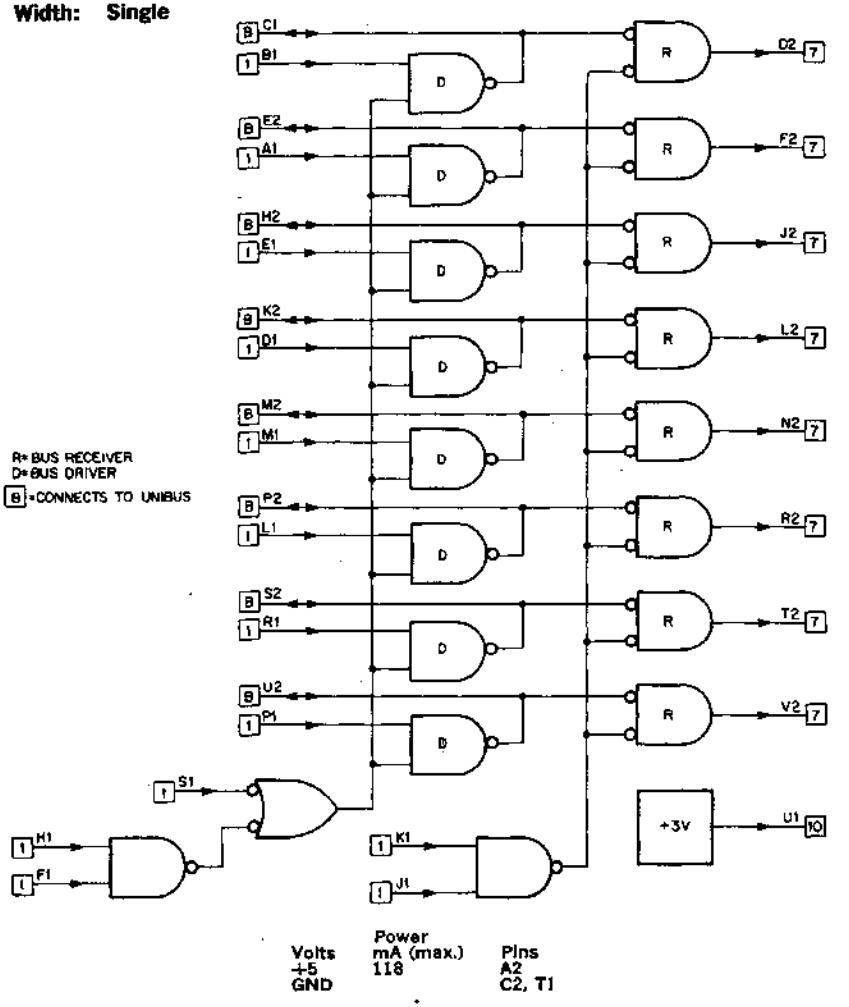
Output Drive: Each output has a fan-out capability of 7 standard TTL loads.

M785
UNIBUS TRANSCEIVER

UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	118	A2
GND		C2, T1

The M785 consists of eight drivers and eight receivers for use as a device interface with the PDP-11 UNIBUS. Pin U1 provides +3 volts and has an output capability of 10 TTL loads. Driver gates have open collectors and are capable of sinking 50 mA with a collector voltage of less than 0.8 volts. The output high leakage current is 2.5 microamperes maximum.

Interrupt: Each I/O connector also has an additional request line (REQUEST A on connector No. 1, REQUEST B on connector No. 2) which may be asserted High by the external device to initiate an interrupt or to generate a flag that may be tested as part of a peripheral status-checking program. Whether these two request lines cause an interrupt is determined by two Interrupt Enable flip-flops (INTR ENB A, INTR ENB B) which may be set under program control to enable interrupt capability for either an A or B interrupt or both if dual interrupts are required.

For interrupt capability, an INTR ENB and a REQUEST signal are applied to an M7821 module or equivalent. These two signals must be both A or B signals; for example INTR ENB A and REQUEST A.

The priority level of both interrupts on the M786 module must be the same, with the interrupt which is back panel-wired closest to the proccessor having the highest sublevel priority. The M786 module contains a priority jumper plug which is normally set at BR5. If other priorities are desired, different plugs may be purchased; part numbers are as follows:

Priority Plug	Part No.
Priority plug, level #7	54-08782
Priority plug, level #6	54-08780
Priority plug, level #5	54-08778
Priority plug, level #4	54-08776
Priority plug, No Request	54-10341

Status Gates: Status gates on the M786 module give the programmer the ability to check the states of the REQUEST and INTR ENBL signals. These gates are software-enabled through the address selector (M105 module) signals SEL 0 and IN H.

SPECIFICATIONS

Propagation Time:

FROM	TO	ns (max)
Bus DATA	I/O Connector	100
I/O connector	Bus DATA	35
Flag Clock inputs	Flag output	40

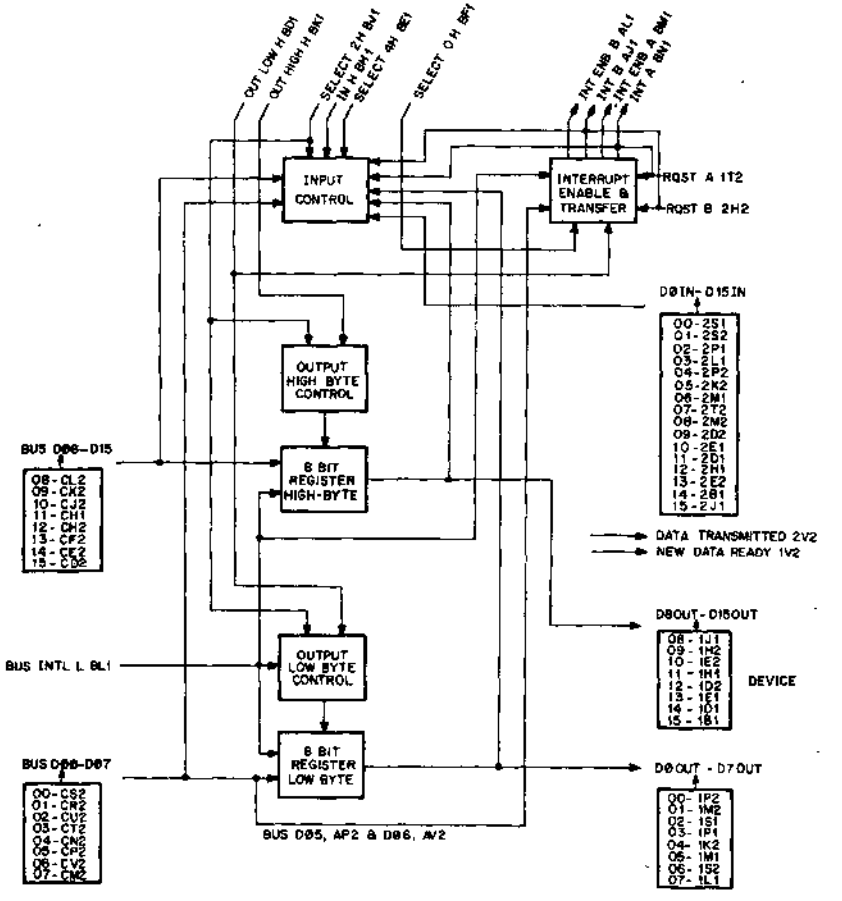
I/O Connector Cables:
The I/O connector accepts the M904 and M927 Cable Connectors which contain solder lugs and can be used with ribbon cable, twisted pair cable, or open wire.

M786
DEVICE REGISTER INTERFACE

UNIBUS

M SERIES

Length: Extended
Height: Double
Width: Single



Volts	Power mA (max.)	Pins
+5	600	AA2, BA2
GND		AC2, BC2
		AT1, BT1

The M786 is a PDP-11 interface module containing all the logic necessary for transfers of 16-bit input and output data between a PDP-11 system and an external device. All I/O connections are made using the connector blocks mounted on the module.

APPLICATIONS

For interfacing to the PDP-11, the M786 must be used with the M105 Address Selector. The M105 decodes the UNIBUS address lines and causes transfer of information through the M786 under program control. Interrupt request circuitry is also built into the M786 module and can be used in conjunction with the M7821 module or equivalent. An example of a typical PDP-11 interface using the M786 module is illustrated below.

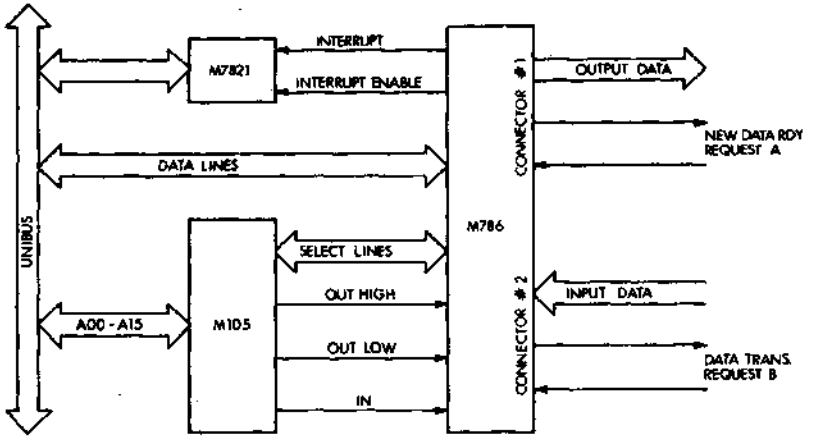


Figure 1. Typical PDP-11 Interface

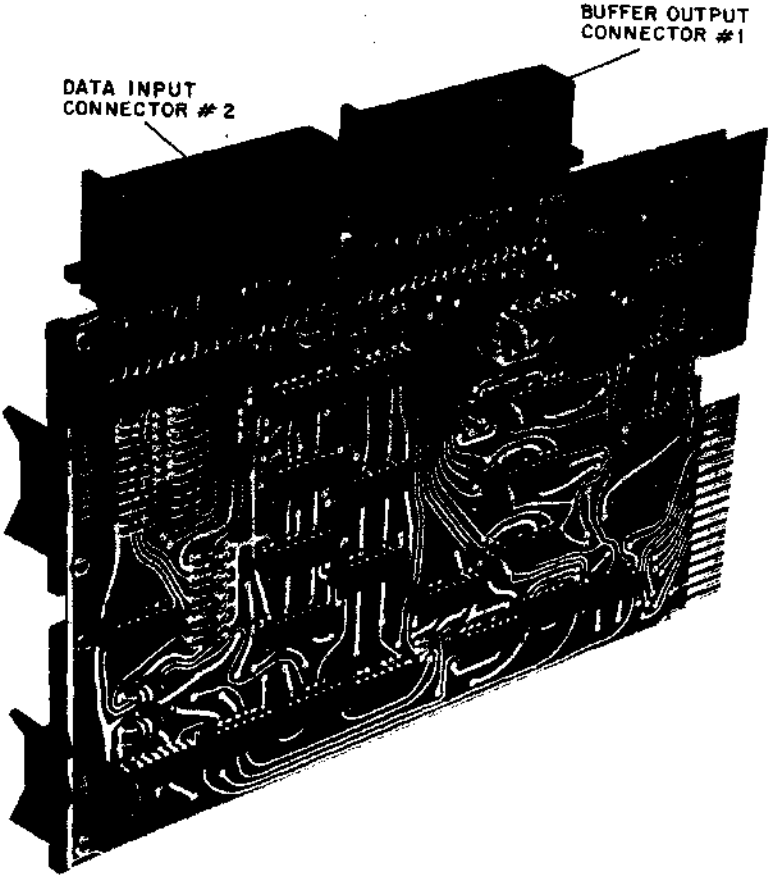
FUNCTIONS

Registers: The M786 module contains a 16-bit register interfaced to the computer bus data lines by ungated receivers. Data from the computer is clocked into the registers by strobing signals OUT LOW with SEL 2 and OUT HIGH with SEL 2 derived from the M105 module. The user has the option of reading whole words (OUT LOW with SEL 2 and OUT HIGH with SEL 2) or 8-bit bytes (OUT LOW with SEL 2 for a low byte and OUT HIGH with SEL 2 for a high byte). All register outputs go to I/O connector No. 1 where cables from an external device can be attached.

The M786 module signals the external device through the NEW DATA signal each time new data is loaded into the 16-bit register. Register outputs may be read back onto the computer bus by program-enabling the IN H and SEL 2 signals from the M105 module.

Drivers: Sixteen bits of TTL data may be received from an external device via cables attached to I/O connector No. 2. These input lines are protected by clamping diodes to prevent input signal swings above or below the normal TTL levels. Each of these input signals can be read onto the computer bus by means of bus drivers which are enabled by the IN H and SEL 4 signals from the M105 module.

The M786 module signals the external device through the DATA TRANSMITTED signal that data has been read onto the computer bus.



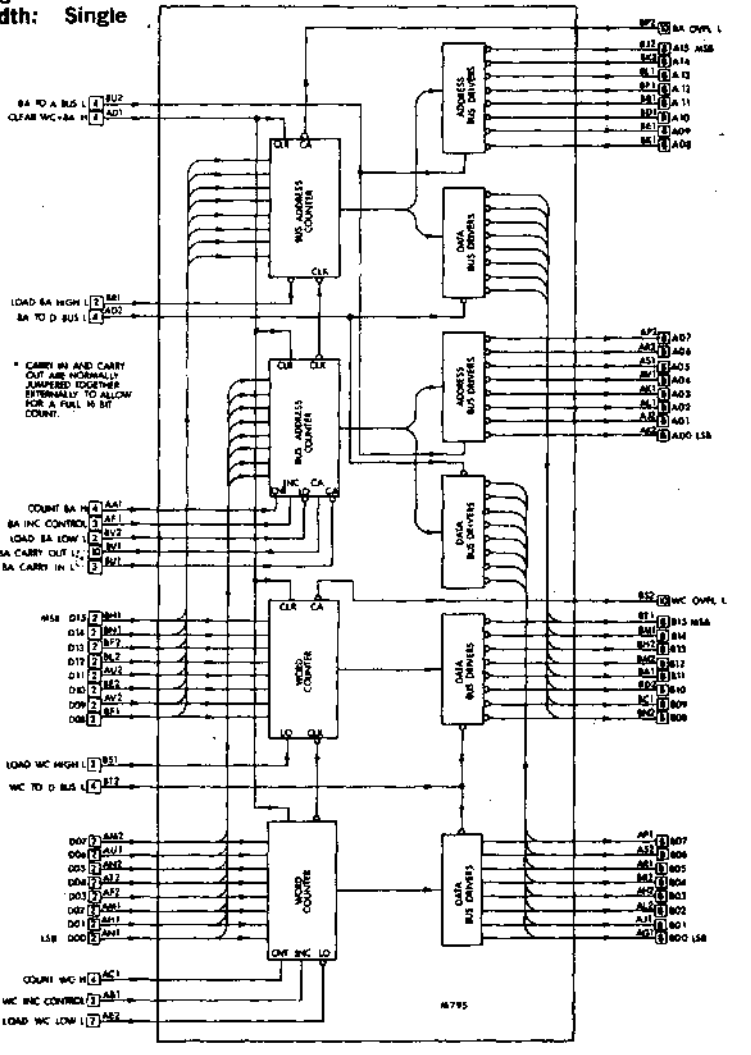
M786 Device Register Interface

M795
WORD COUNT AND BUS ADDRESS MODULE

UNIBUS

M SERIES

Length: Extended
Height: Double
Width: Single



Volts	Power mA (max.)	Pins
+5	600	AA2, BA2
GND		AC2, AT1, BC2, BT1

The M795 Word Count and Bus Address Module can be used to provide two of the essential elements of an interface which connects Direct Memory Access (DMA) devices to the UNIBUS. This module contains two 16-bit counters. One counter is used to count the number of data transfers that occur. The other counter is used to specify sequential bus addresses for the sources and/or destinations of the data to be transferred.

FUNCTION

Word Counter

Block transfer devices that function as bus master during data transfers usually require two registers to hold the parameters of the transfer. One parameter is the transfer word count. Initially, this register (WC) is loaded by the computer with the 2's complement of the number of words to be transferred to or from memory. This number is clocked into the WORD COUNT register in two 8-bit bytes or one 16-bit word using the LOAD WC L (low byte) and LOAD WC + 1 L (high byte) inputs. After each data transfer is complete, the WC register is incremented by clocking the COUNT WC H input. When the new value of the WC register reaches 0, an overflow signal is generated at the WC OVFL L output, which would be used to inhibit further transfers and to signal that the transfer is complete. Information can be transferred in either words (16 bits each) or bytes (8 bits each), because the WC register may also be used as a byte counter.

Address Counter

The second parameter used in block transfers is the transfer address. Initially, a bus address register (BA Counter) is loaded by the computer with an address that specifies the memory location to or from which data is to be transferred. This address is loaded from the BUS DATA lines (D00-D15) in two 8-bit bytes or one 16-bit word using the LOAD BA L (low byte) and LOAD BA+1 L (high byte) inputs. The BA register is incremented after each transfer by clocking the CLOCK BA H input. The register continually "points" to sequential memory locations for block transfers.

BUS Drivers

Outputs of both the Word Counter and BA Counter are connected to a set of UNIBUS drivers so that the counter contents can be gated to the DATA BUS when the appropriate enable signals (BA TO BUS L and WC TO D BUS L) are asserted. In addition, the BA register has a set of drivers with independent outputs to allow it to drive the ADDRESS BUS when the BA TO BUS L input is asserted.

Counter Increments

The BA register can be incremented by either 1 or 2 as a function of the BA INC CONTROL input (High=1, Low=2). This incrementation capability allows addressing of either sequential bytes or words. The register is incremented on the trailing edge of a positive pulse applied to the COUNT BA H input of the register. The carry between bits 03 and 04 is broken and brought out to pins BV1 (BA CARRY OUT L) and BU1 (BA CARRY IN L). Normally these pins are connected together externally to allow for a full 16-bit count. They can, however, be controlled to inhibit the carry and to force repeated addressing of 16 sequential byte addresses. This feature can be used in device-to-device transfers. An overflow pulse (BA OVFL L) is provided as an output whenever the register is incremented from all 1's to all 0's.

The WC register is incremented by either 1 or 2 as a function of the WC INC CONTROL input (High=1, Low=2). The register increments on the trailing edge of a positive pulse applied to the COUNT WC H input of the register.

An overflow pulse is also available at pin BS2 (WC OVFL L). Both registers reset to 0's whenever the CLEAR WC+BA H signal is asserted.

The storage elements on the M795 module are not edge triggered devices. Data must be established and held for the duration of the loading pulse.

The data inputs to the registers are not bus receivers and can not be connected directly to the UNIBUS. Use the M784 or equivalent.

APPLICATIONS

This module is used to interface direct memory access (DMA) devices to the UNIBUS.

SPECIFICATIONS

Propagation Time:

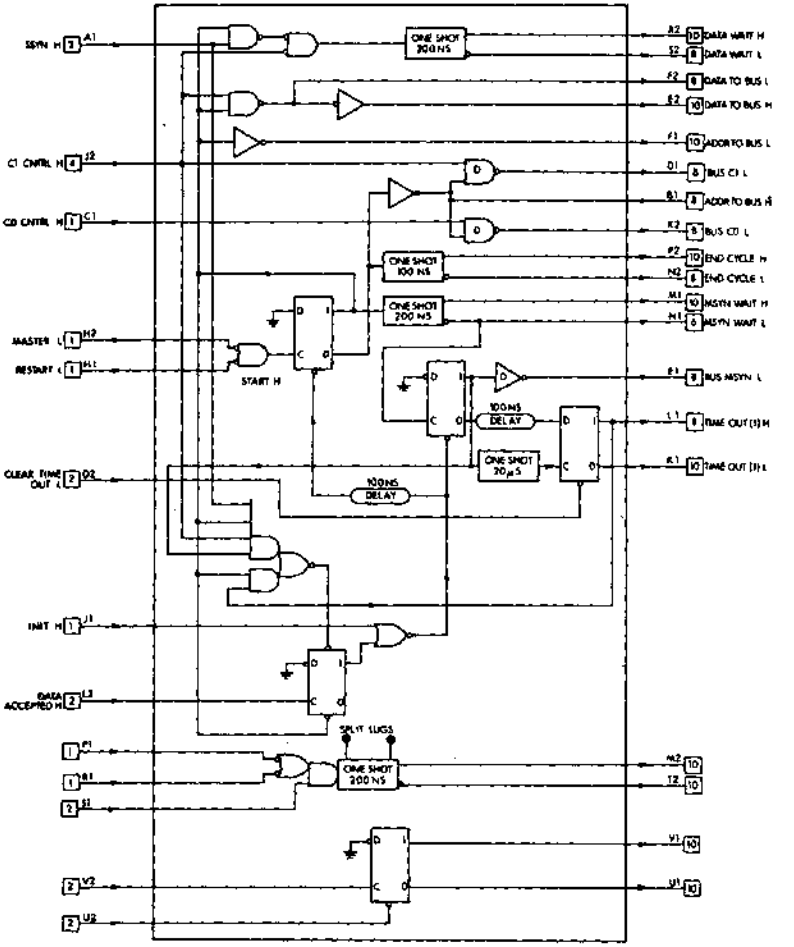
FROM	TO	ns (max.)
CLEAR WC+BA	WC+BA Outputs	125
LOAD WC L	WC Outputs	75
LOAD WX+1 L	WC Outputs	75
COUNT WC H	WC Outputs	60
LOAD BA L	BA Outputs	75
LOAD BA+1 L	BA Outputs	75
COUNT BA H	BA Outputs	60

M796
UNIBUS MASTER CONTROL

UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	130	A2
GND		C2, T1

The M796 UNIBUS Master Control Module provides the necessary logic to enable a peripheral device to perform a bus cycle on the UNIBUS to transfer data. In addition to controlling the four transfer operations (DATI, DATIP, DATA, and DATOB), the M796 module generates strobe and gating signals which transfer both addresses and data to and from the bus; handles deskewing of data received from the bus; protects against data transfers to nonexistent devices by the use of time-out circuits; and provides a flip-flop and integrating one-shot that can be used by the customer for special control functions.

Any device in the PDP-11 system may have the capability of gaining control of the bus and, as bus master, of transferring data to and from other slave devices on the bus. This operation is performed independently of processor control and is usually referred to as Direct Memory Access (DMA). The logic necessary to gain control of the UNIBUS is provided by the M7821 Interrupt Control module.

Upon becoming bus master, the device is free to conduct a data transfer. A DATI cycle is performed if the device needs data (either a word or byte) from memory or from another peripheral; a DATO cycle is performed if the device is storing a word of data in memory (DATOB cycle for byte storage) or is sending data to another peripheral; a two-cycle DATIP, DATO(B) operation is performed if data held in memory is to be modified as in the case of increment memory or add to memory functions.

In order to execute one of these transfer cycles, the M796 must set Bus C0 and Bus C1 for the required type of data transfer, assert the MSYN signal, and then wait for the SSYN repsonse from the slave. Data must either be gated to the Bus data lines on a DATO cycle or be received and strobed at the proper time on a DATI cycle.

The Bus C1 and Bus C0 outputs of the M796 can directly drive the UNIBUS and are asserted as a function of the control inputs C1 CNTRL H and C0 CNTRL H. Table 1 lists the states of the control inputs for the four possible bus cycles. Note that for DATI or DATO, only C1 has to be varied while holding C0 low.

Table 1. Control Line Input States for M796

C1	C0	Bus Cycle
L	L	DATI
L	H	DATIP
H	L	DATO
H	H	DATOB

The data transfer sequence is triggered by meeting the AND condition of the low state of both MASTER L (H2) and RESTART L (H1). Usually these two inputs are tied together and are connected to the MASTER L signal produced by the M7821 Interrupt Control Module. When the AND condition is met, it produces the START signal, which is an internal signal in the M796 module. At the transition of the START signal, both Bus C1 and Bus C0 are asserted as determined by their respective control inputs. The ADRS to Bus signals are also asserted and are used to gate the address of the slave onto the bus address lines (Bus A 17:00). If an output cycle is specified (C1 = 1), the DATA TO BUS signals (both H and L) are also asserted and are used to gate data to

be transferred to the slave onto the bus data lines (Bus D 15:00). When the MSYN WAIT one-shot times out after 200ns, the BUS MYSN L signal is asserted. The master device then waits for a response from the slave.

In a data output cycle (DATO), assertion of SSYN by the slave causes BUS MYSN to be negated immediately. After a 100-nanosecond delay, BUS C1, BUS C0, ADRS TO BUS and DATA TO BUS are negated. When these signals drop, the END CYCLE pulse appears and is usually used to release control of the bus.

In a data input cycle (DATI), the assertion of the SSYN input produces a 200-nanosecond pulse that appears as DATA WAIT. This delay allows time for the incoming data to deskew and settle. The trailing edge of the DATA WAIT pulse can be used to clock data from the slave into the master device. If a strobe pulse is necssary, the trailing edge of DATA WAIT can be used to trigger the one-shot provided on the module. In either case, once data is received, a positive-going edge is applied to DATA ACCEPTED L causing BUS MSYN to be negated initially, followed by negation of ADDR TO BUS, BUS C1, and BUS C0 100 nanoseconds later.

A TIME-OUT flip-flop is set if a SSYN response fails to occur within 20 microseconds after BUS MSYN is asserted. When this flip-flop is set, the bus cycle is terminated and END CYCLE is issued. The TIME OUT signals are used to indicate an error condition. The TIME-OUT flip-flop is cleared by asserting the CLEAR TIME OUT L input.

The M796 module provides an extra flip-flop that has the clock (V2), reset (U2), 1 side (V1) and 0 side (U1) available to the customer. The flip-flop is clocked by a positive transition on the clock input.

An integrating one-shot is also provided on the module. This one-shot is triggered whenever the output of the gating input becomes true. The output pulse width at pins T2 and M2 is 150 nanoseconds but can be lengthened by adding capacitance across the pair of split lugs on the module. The following equation can be used to determine the approximate value of the added capacitance:

$$T_{pw} - 0.32\ (RC$$

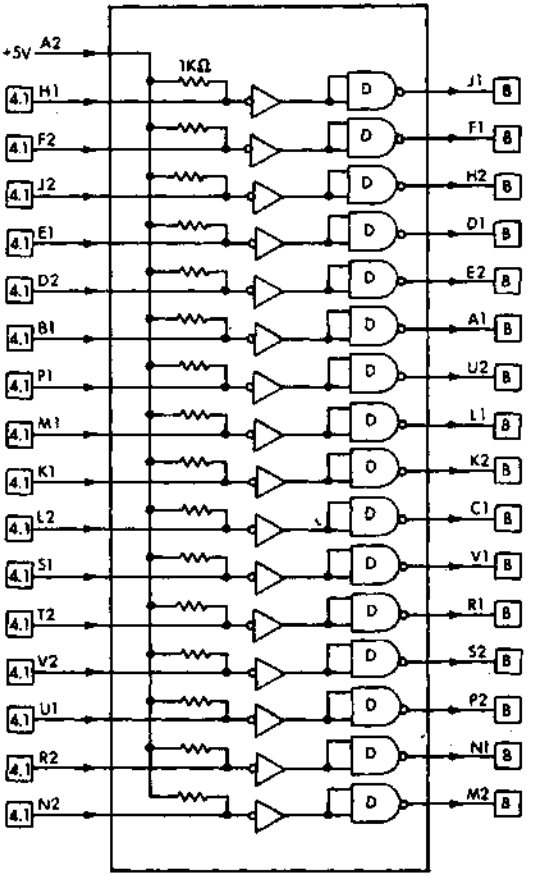
where T_{pw} is in milliseconds, R is in ohms, and C is in microfarads. (The internal resistance is 5.6 kilohms.)

Note that all times mentioned above represent nominal values with a tolerance of ± 25%. The delays and pulses provided by the module are controlled by simple RC circuits: therefore, if the user has any special requirements, part substitutions can be made to alter these time constants.

M798
UNIBUS DRIVERS

UNIBUS

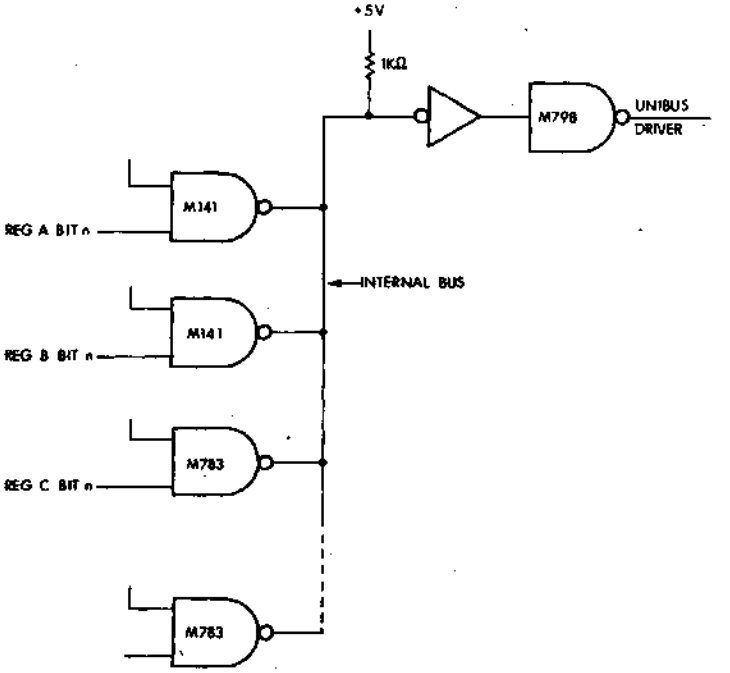
Length: Extended
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	320	A2
GND		C2, T1

This module consists of 16 noninverting UNIBUS drivers with pull-up resistors on the inputs. The module is used in device interfaces to minimize the loading effect caused by attaching several drivers to the same UNIBUS signal line, as in the case of a device containing multiple registers. Loading of signal lines on the UNIBUS is restricted to the equivalent of one UNIBUS receiver input and two UNIBUS driver outputs per device.

In addition, the M798 module allows the UNIBUS to be driven by standard open-collector TTL gates. The inputs to each M798 driver circuit are pulled up to +5 V through a 1-kilohm resistor. As shown below, an internal wired-OR multiplexer is created that is driven from standard open-collector gates or from UNIBUS drivers (such as the M1501 or M783).



Typical Use of M798

SPECIFICATIONS

Output Driver: The output Low voltage for each of the 16 outputs is 0.8 volts maximum with 50 mA current sink. The output High leakage current is 25 microamperes maximum.

Propagation Delay: The propagation delay between the 16 inputs and the driver outputs is 60 nanoseconds maximum.

PDP-12 Interfacing
The PDP-12 is a general-purpose 12-bit computer system that is interfaced identically to the non-OMNIBUS positive bus PDP-8s. Therefore, the interfacing criteria and related module descriptions listed for PDP-8 positive bus operation apply to the PDP-12.

PDP-15 Interfacing
The PDP-15 is an 18-bit word length general-purpose computer that utilizes a positive bus structure. The following modules were developed specifically for interfacing with the PDP-15 I/O Bus, but may be used in many other positive logic applications.

M500 Negative Input/Positive Output Receiver

M510 Positive Bus Receiver

M622 Positive Bus Driver

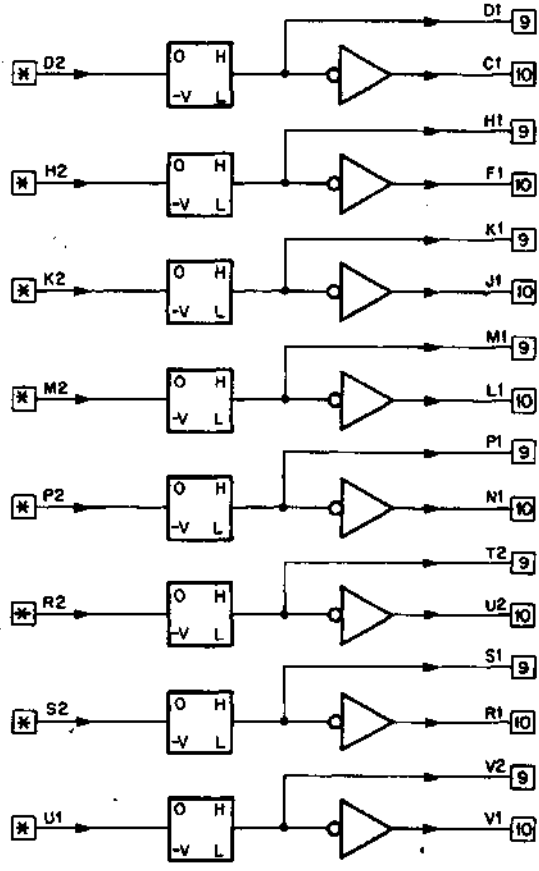
M909, M910 } Bus Line Terminators

M500
NEGATIVE INPUT POSITIVE OUTPUT RECEIVER

PDP-15 BUS

M SERIES

Length: Standard
Height: Single
Width: Single



*=1mA AT GROUND

Volts	Power mA (max.)	Pins
+5	160	A2
GND		C2, T1
−15	64	B2

The M500 module is used to convert negative input signals to positive output signals. Each card contains eight converters and is pin compatible with the PDP-15 positive receiver card (M510).

FUNCTIONS

A ground input at D2 will yield a +3 at D1 and ground at C1. Do not connect to pin E2 (used for manuf. test only).

SPECIFICATIONS

Propagation time (each circuit):

FROM	TO	ns (max.)
Input	Output	40

M510
I/O BUS RECEIVER

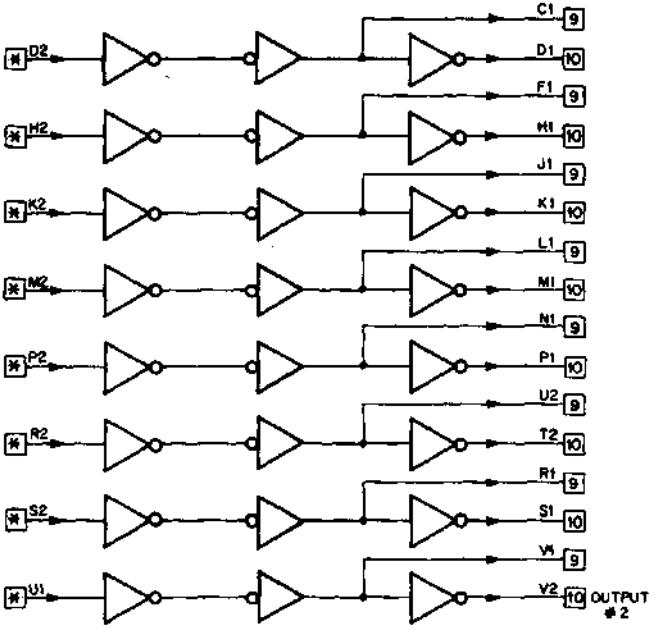
PDP-15 BUS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$51



* = 80 μA AT HIGH(+3V)

Volts	Power mA (max.)	Pins
+5	170	A2
GND		C2, T1, F2 J2, L2, N2

The M510 is a positive input/output receiver card for use with the PDP-15. It contains 8 high-impedance input circuits of at least 27K ohms and input switching thresholds of about +1.5 V. Each receiver has two outputs, one of the same polarity as the input, the other, the complement of the input. The receiver card can be used anywhere on the PDP-15 I/O Bus.

PRECAUTIONS

Do not connect to pin E2 (used for manuf. test only). Power (B+) must be applied at all times since the input impedance drops to 1K ohm when power is off.

Inputs: The input impedance is 27K ohms (min.). Each input load current is 80 μA (max.) and the threshold switching level is 1.4 to 1.6 volts.

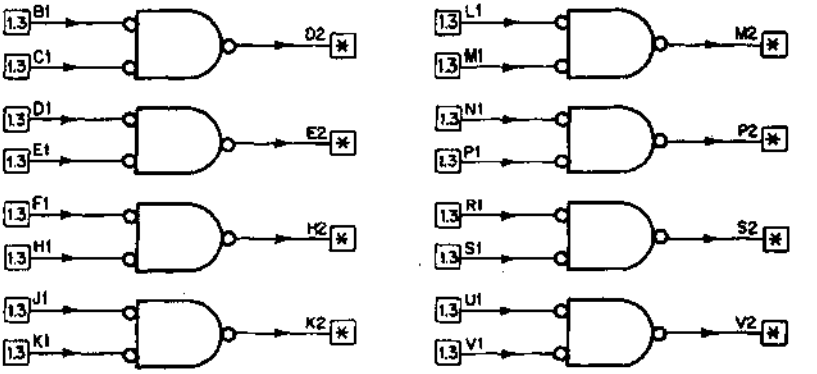
Outputs: Output no. 2 delay ≃ 50 ns (from input).

M622
EIGHT-BIT POSITIVE INPUT/OUTPUT BUS DRIVER

PDP-15 BUS

M SERIES

Length: Standard
Height: Single
Width: Single

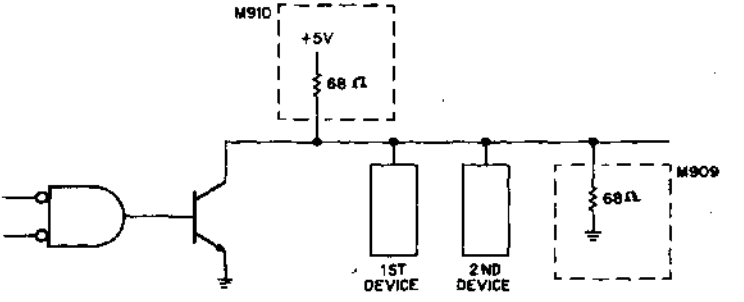


* = DRIVES PDP-15 POSITIVE BUS

Volts	Power mA (max.)	Pins
+5	210*	A2
GND		C2, T1, F2, J2, L2, N2, R2, U2

* excluding output current

The M622 contains 8 two-input AND gate bus drivers for convenient driving of the positive input bus of the PDP-15. The output consists of an open collector NPN transistor.



Pull-up resistors of 68 ohms to +5.0 V (supplied on M910) must be tied to the output and the last device should terminate all lines to ground with a 68-ohm resistor (supplied on M909).

PRECAUTIONS

Outputs: The maximum voltage applied to the output transistor must not exceed +20 volts and the collector current must not exceed 100 mA.

SPECIFICATIONS

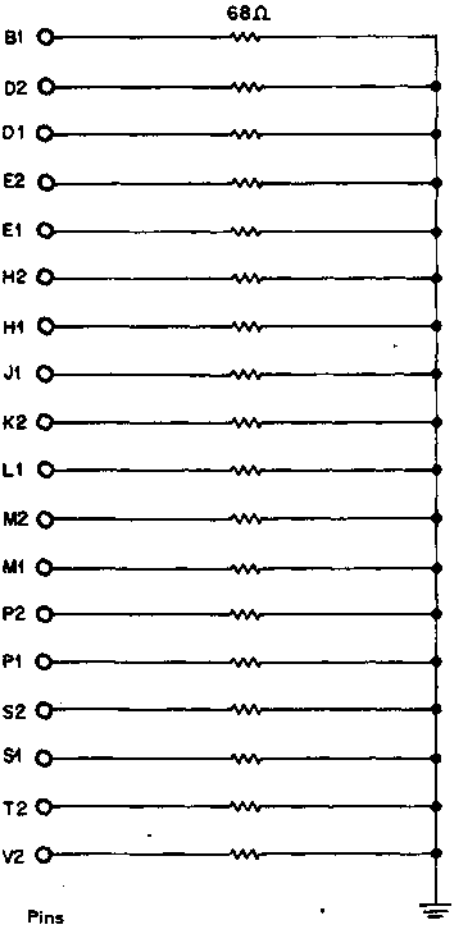
Propagation Time: Typically 25 ns.

M909
TERMINATOR

PDP-15 BUS

M SERIES

Length: Standard
Height: Single
Width: Single



Volts	Power mA (max.)	Pins
+5	NONE	
GND		A1, C1, C2, F1, J2, K1 L2, N1, N2, R1, R2, T1, U2

The M909 module contains eighteen 68-ohm resistors tied to ground through a common bus.

APPLICATIONS

This module is intended to be used with the M910 to form half of the biasing circuit used in the driving network of the M622.

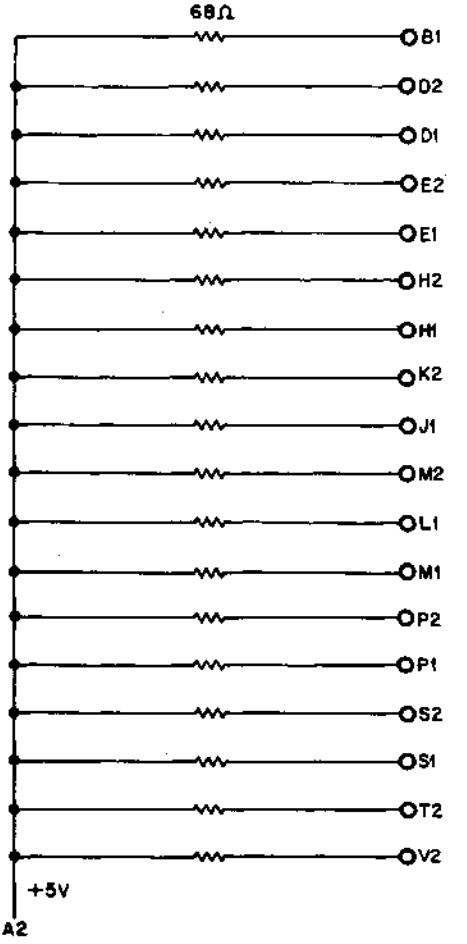
M910
TERMINATOR

PDP-15
BUS

M SERIES

Length: Standard
Height: Single
Width: Single

Volts	Power mA (max.)	Pins
+5	1350	A2
GND		A1, C1, C2, F1, F2, J2, K1 L2, N1, N2, R1, R2, T1, U2



The M910 module contains eighteen 68-ohm resistors tied to a common +5 volt bus.

APPLICATIONS

This module is intended to be used with the M909 to form half of the biasing circuit used in the driving network of the M622.

deckits

modular computer interfacing

DECkits

INTRODUCTION

M Series Logic Modules have been developed over a period of time, from a collection of fundamental logic components (gates and flip-flops) to complex MSI- and LSI-implemented logic arrays. In some instances, full-scale digital subsystems are available, such as the M1710 UNIBUS Interface Foundation Module, which allows the user to interface a wide variety of equipment to PDP-11 computers.

In a continuing effort to offer greater interfacing capability for the lowest cost possible, the complex logic module building block concept is being expanded to greater limits of versatility in kit form.

A kit is basically a collection of logic modules assembled by the user to a prewired system unit, capable of performing a highly complex computer interface at low cost to the user.

The following kits are described in this handbook:

DECkit11-H PDP-11 I/O Interface (4 Words In/4 Words Out)

DECkit11-F PDP-11 I/O Interface (3 Words In/1 Word Out)

DECkit11-K PDP-11 I/O Interface (8 Words In)

Deckit11-M PDP-11 I/O Interface (34 Bits In/24 Bits Out)

DECkit11-D PDP-11 Direct Memory Access Interface

DECkit01-A Remote Analog Data Concentrator

Five of the six kits listed above are DECkit11 Series PDP-11 Input/Output Kits which allow the processor to communicate with a variety of peripheral devices by either receiving and/or transmitting the appropriate number of 16-bit data words via the computer. Provisions are included which will enable computer interrupts to be made at preassigned (hardwired) priority levels.

The kits are defined in full or maximum configuration; i.e., the system unit wiring and the recommended complement of modules define the maximum I/O capability. If the user wishes, a lesser capability may be achieved by removing the appropriate modules.

The sixth kit, designated DECkit01-A, provides a convenient method of monitoring analog voltages at a remote location. The analog voltages are converted to numerical data and transmitted as an ASCII-coded message over a serial communication line.

DECkit11 Series General Description

DECkit11 Series is a set of complete PDP-11 UNIBUS interfaces that are configured with Digital Equipment Corporation parts and assembled by the user. The kits consist of M Series modules, cables, and prewired backplane (standard system unit). No additional wiring or design is required by the user for standard configurations. For any other variation, refer to KIT VARIATIONS section in the appropriate data sheets and/or option manuals.

FEATURES

- Low cost
- Expandable—variable number of I/O channels; several kits may be stacked to make larger arrays
- Complete interface packages that are directly compatible with the PDP-11 UNIBUS
- User-selected register addresses
- Full 16-bit storage for data outputs
- High-voltage, high-fan-out, open-collector data output capability for directly driving cables, instruments, etc.
- Interrupt capability (DECkit11-F, H, M, D)
- Multiple 8-bit byte or 16-bit output capability
- Multiple 16-bit word input capability
- External input/output connections via convenient connectors
- One I/O cable for every input or output word
- User-defined variations are possible

INDIVIDUAL KIT DESCRIPTIONS

DECkit11-H

The DECkit11-H, when fully configured, is capable of reading four 16-bit words from a peripheral device into a PDP-11. See Figure 1. It is also capable of writing four 16-bit words, or eight 8-bit bytes, from a PDP-11 to a peripheral device. Each input word is supplied with an interrupt capability to signal the processor that the word should be read. Two interrupts are serviced on level 5 and two on level 6. Figure 2 is a module utilization diagram of a fully configured DECkit11-H.

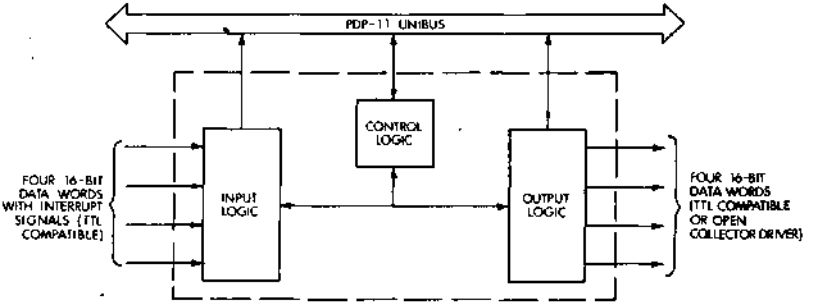


Figure 1. DECkit11-H Functional Block Diagram.

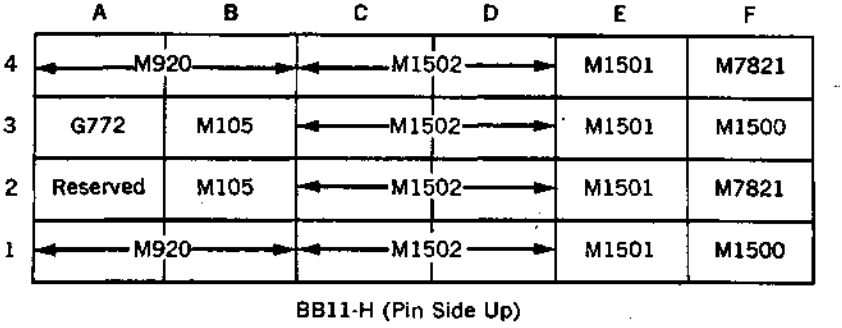


Figure 2. Module Utilization Diagram of a Fully Configured DECkit11-H Backplane.

TABLE 1

Parts List DECkit11-H

ITEM	STOCK NO.	DESCRIPTION	MAX. QTY.
1	BB11-H	Pre-wired Backplane for DECkit11-H	1
2	M105	Address Selector Module	2
3	M7821	Interrupt Control—UNIBUS	2
4	M1500	Bus Gates Module	2
5	M1501	Bus Input Interface Module	4
6	M1502	Bus Output Interface Module	4
7[1]	M920	Internal Bus Connector	1
8[1]	BC11A-XX*	PDP-11 UNIBUS Cable	1
9[2]	BC08R-XX*	Cable, H856-H856	8
10[2]	BC04Z-XX	Cable, H856—Open End	8
11[2]	BC07A or D-XX	Cable, H856-Open End	8

Items 1-6 comprise basic kit.
Items 7-11 are required accessories. Refer to notes for appropriate usage.

[1] Order either Item 7 or Item 8, not both.
[2] Order any combination up to eight of Items 9, 10, 11.
* XX is length in feet.

DECkit11-F

The DECkit11-F when fully configured is capable of reading three 16-bit words from a peripheral device into a PDP-11. See Figure 3. It is also capable of transferring one 16-bit word, or two 8-bit bytes, from a PDP-11 to a peripheral device. Each word, both input and output, is supplied with an interrupt capability on priority level 7. Figure 4 shows a module utilization diagram of a fully configured kit.

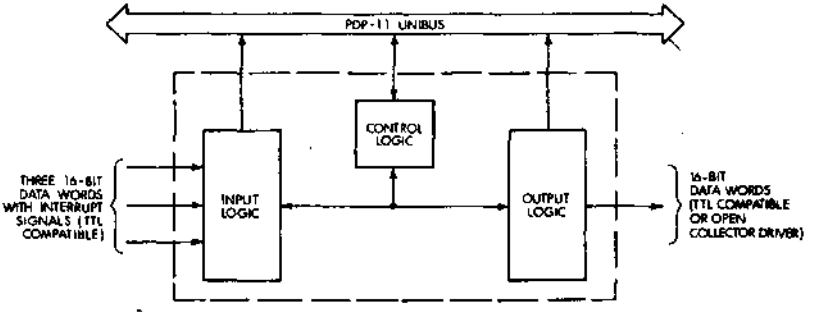


Figure 3. DECkit11-F Functional Block Diagram

	A	B	C	D	E	F
4	← M920 →					M7821
3	G772		See Note 1		M1501	M1500
2	Reserved	M105			M1501	M7821
1	← M920 →		← M1502 →		M1501	M1500

BB11-F (Pin Side Up)

Notes: 1. Shaded slots represent those unused by the Kit. These may be used for additional M, A, W or K Series modules.

Figure 4. Module Utilization Diagram of a Fully Configured DECkit11-F Backplane.

TABLE II

Parts List DECkit11-F

ITEM	STOCK NO.	DESCRIPTION	MAX. QTY.
1	BB11-F	Pre-wired Backplane for DECkit11-F	1
2	M105	Address Selector Module	1
3	M7821	Interrupt Control—UNIBUS	2
4	M1500	Bus Gates Module	2
5	M1501	Bus Input Interface Module	3
6	M1502	Bus Output Interface Module	1
7[1]	M920	Internal Bus Connector	1
8[1]	BC11A-XX*	PDP-11 UNIBUS Cable	1
9[2]	BC08R-XX*	Cable, H856-H856	4
10[2]	BC04Z-XX	Cable, H856—Open End	4
11[2]	BC07A or D-XX	Cable, H856-Open End	4

Items 1-6 comprise basic kit.

Items 7-11 are required accessories. Refer to notes for appropriate usage.

[1] Order either Item 7 or Item 8, not both.

[2] Order any combination up to four of Items 9, 10, 11.

* XX is length in feet.

DECkit11-K

The DECkit11-K when fully configured, is capable of reading eight 16-bit words from a peripheral device into a PDP-11. See Figure 5. It does not have any output or interrupt capability. Figure 6 shows a module utilization diagram of a fully configured kit.

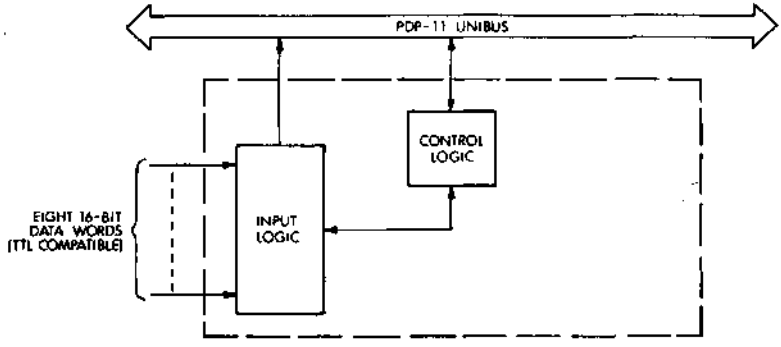
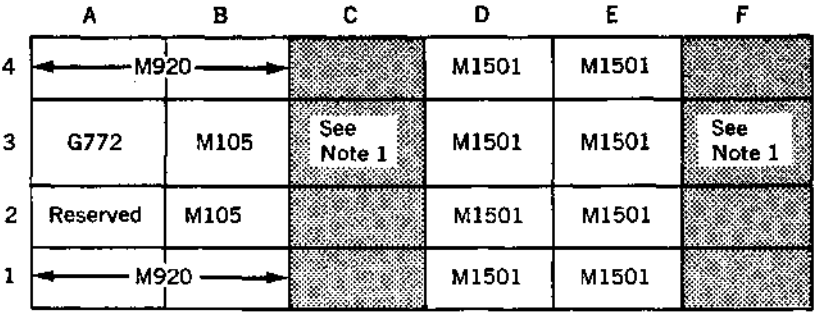


Figure 5. DECkit11-K Functional Block Diagram.



BB11-K (Pin Side Up)

Notes: 1. Shaded slots represent those unused by the Kit. These may be used for additional M, A, W or K Series modules.

Figure 6. Module Utilization Diagram of a Fully Configured DECkit11-K Backplane.

TABLE III

Parts List DECkit11-K

ITEM	STOCK NO.	DESCRIPTION	MAX. QTY.
1	BB11-K	Pre-wired Backplane for DECkit11-K	1
2	M105	Address Selector Module	2
3	M1501	Bus Input Interface Module	8
4[1]	M920	Internal Bus Connector	1
5[1]	BC11A-XX*	PDP-11 UNIBUS Cable	1
6[2]	BC08R-XX*	Cable, H856-H856	8
7[2]	BC04Z-XX*	Cable, H856—Open End	8
8[2]	BC07A or D-XX*	Cable, H856-Open End	8

Items 1-3 comprise basic kit.
Items 4-8 are required accessories. Refer to notes for appropriate usage.

[1] Order either Item 4 or Item 5, not both.
[2] Order any combination up to eight of Items 6, 7, 8.
* XX is length in feet.

DECkit11-H, F, K SELECTION GUIDE

Table IV may be used to determine which kit will fulfill the user's data transfer requirements.

Table V may be used to determine which fully configured kit will fulfill the user's interrupt requirements.

If the user's requirements are less than a fully configured kit, refer to the Data Sheet for the kit that most closely fulfills the requirements.

Table IV. Data Transfer Needs vs. Kit Number

Number of 16-Bit INPUT Words Required per Kit.	Number of 16-Bit OUPUT Words Required Per Kit.				
	0	1	2	3	4
0		11-H 11-F	11-H	11-H	11-H
1	11-H 11-F 11-K	11-H 11-F	11-H	11-H	11-H
2	11-H 11-F 11-K	11-H 11-F	11-H	11-H	11-H
3	11-H 11-F 11-K	11-H 11-F*	11-H	11-H	11-H
4	11-H 11-K	11-H	11-H	11-H	11-H*
5	11-K				
6	11-K				
7	11-K				
8	11-K*				

* Indicates a fully configured kit.

Table V. Interrupt Needs vs. Kit Number

Number of **INTERRUPTS** Associated with **INPUT** Words **Required** per Kit.	Number of **INTERRUPTS** Associated with **OUTPUT** Words **Required** per Kit.	
	0	1
0	11-H 11-F 11-K	11-F
1	11-H 11-F	11-F
2	11-H 11-F	11-F
3	11-H 11-F	11-F*
4	11-H*	

* Indicates a fully configured kit.

8

Items 1-10 comprise basic kit.
Items 2-5 are required accessories. Refer to notes for appropriate usage.

DECkit11-M

A fully configured DECkit11-M is capable of reading 34 bits of data from peripheral instrumentation into any model PDP-11 processor, writing 24 bits of control data from a PDP-11 to peripheral instrumentation, and accommodating one Small Peripheral Controller (SPC) option. Interrupt capability is supplied that informs the processor that input data should be read or that the peripheral instrument is ready to accept data. The full interrupt capabilities of the Small Peripheral Controller are maintained. If the complete DECkit11-M is not required, or if additional input/output capabilities are desired, individual modules and accessories may be ordered to create custom variations.

DECkit11-M is comprised of two Address Selector Modules, one Data Input Interface Module, one Data Output Interface Module, one UNIBUS Interrupt Control Module, various priority jumpers, and a completely wired BB11-M Systems Unit. See Figure 7.

The data and interrupt signals are applied to the kit via two 40-conductor cables. The specific length and termination of these two input/output cables are selected by the user to suit his custom application.

DECkit11-M is well suited to a variety of PDP-11 UNIBUS interfacing applications. Its input and output capabilities are particularly oriented toward data acquisition from and the programming of remotely located laboratory instruments, the control of production equipment, and the accommodation of custom peripheral design. The 34-bit input multiplexing capability makes possible the acquisition of TTL-compatible data from such devices as digital voltmeters, frequency counters, resistance/capacitance bridges, thumbwheel swithes, A/D converters, limit switches, and similar devices.

The DECkit11-M utilizes a 24-bit output storage register which has the ability to provide TTL-compatible or open-collector, high-drive output signals. This makes it possible to perform remote programming of such devices as programmable power supplies and digital voltmeters, and the control of D/A converters, small relays, displays, X-Y recorders, and similar devices.

In addition, by employing a 16-bit relay output module, type M1801, applications that require electrical isolation of the TTL-compatible computer signals or which require conversion from TTL to large positive or negative voltages, can be accommodated. The M1801 allows a PDP-11 to control single-pole, normally open, relay contacts which can be used to operate other equipment such as instruments, lamps, etc. Each bit of the data word from the processor controls one relay contact at switching rates of up to 80 actuations per second.

Figure 8 shows a module utilization diagram of a fully configured kit.

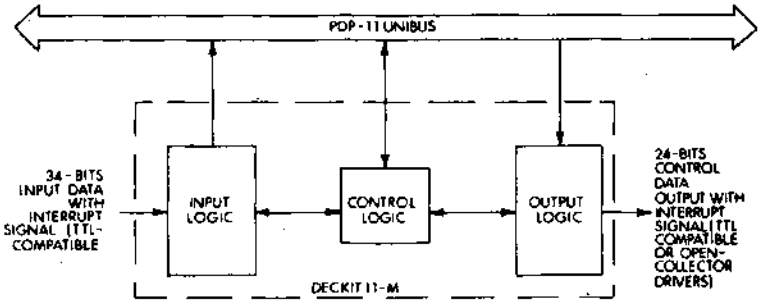


Figure 7. DECkit11-M, Simplified Block Diagram

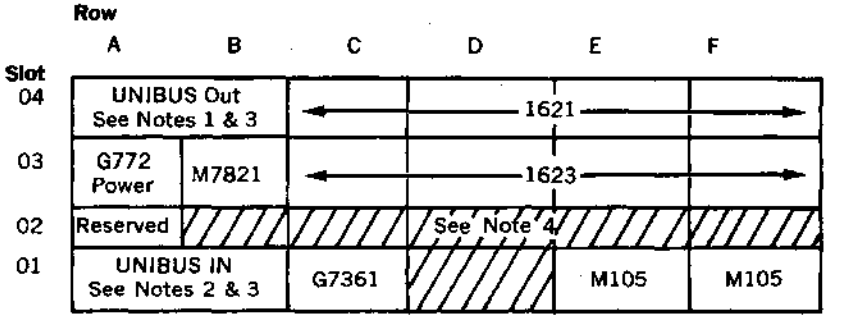


Figure 8. DECkit11-M Module Utilization Diagram (Pin Side)

Notes for Figure 8:

[1] UNIBUS Terminator M930, supplied with the PDP-11, is required at slots A04-B04 when DECkit11-M is the last unit on the UNIBUS.

[2] UNIBUS Cable BC11A-xx is required at slots A01-B01 when DECkit11-M is the first unit in an expansion box.

[3] UNIBUS Connector M920 or UNIBUS Cable BC11A-xx is not supplied as part of DECkit11-M. Refer to HOW TO ORDER paragraph.

[4] Shaded slots represent those unused by DECkit11-M. These are prewired to accommodate an additional I/O module set or an SPC.

TABLE VI

KIT 11-M Parts List

ITEM	STOCK NUMBER	DESCRIPTION	QUANTITY
1	BB11-M	Prewired System Unit (Includes Print Set)	1
2	M105	Address Selector Module	2
3	M7821	UNIBUS Interrupt Control Module	1
4	M1621	DVM Input Interface Module	1
5	M1623	Instrument Remote Control Interface Module	1
6	G7361	Priority Select Module	1
7	5410341	Priority Jumper No Request	2
8	5408776	Priority Jumper level #4	2

In addition to the items included in DECkit11-M, an input cable, an output cable, and a UNIBUS cable are required. Figure 8 shows equipment layout. Expansion boxes (BA11-ES and BA11-EC), cabinets (Cab-A through K), and power supplies (H720-E or -F) are also available.

DECkit11-D

This kit is designed specifically for the PDP-11 owner who requires high I/O data transfer rates. Full 16-bit data words can be transferred between the PDP-11 memory and an external device at UNIBUS speeds. See Figure 9. The DECkit11-D interface kit is physically and electronically compatible with all PDP-11 Family computers.

Parallel digital data is cabled directly to and from the interface kit; no additional logic or hardware is required to handle TTL-compatible data. External devices, such as lab instruments, mass storage units, displays, pre-processors, and other CPUs can communicate conveniently with the PDP-11 memory.

The prewired backplane includes five unused module slots that can be used for custom logic such as level shifters and counters. Even modules for simple processing logic can be utilized in these unused slots. Figure 10 is a module utilization diagram of a DECkit11-D.

DECkit11-D is valuable to the OEM and the end-user. The predesigned interface concept frees the system designer from the complex problems usually associated with UNIBUS interfacing and the end-user has available the flexibility and speed of the UNIBUS for data transfers.

SPECIFICATIONS

Transfer Types:	Direct Memory Access (DMA) via NPR programmed control
Data input to PDP-11 memory:	16-bit word Parallel TTL-compatible Up to 100 ft I/O cable Up to ½ million words/second*
Data output from PDP-11 memory:	16-bit word Parallel TTL-compatible, high-drive capability Up to 100 ft I/O cable Up to 2/5 million words/second*
Control and Status:	16-bit Control and Status Register (CSR) Handshaking control signals— Data Available Out Data Available In Data Accepted Out Data Accepted In Last Transfer External Overflow Status signals—Function/Out Status/In
Interrupts:	Word count overflow Nonexistent memory External overflow Input demand } Set by Priority Interrupt Plug; shipped at level 5. Interrupt enable/disable—CSR bit 06

Register assignments:	Word Count Register (WCR) 76xxx0** Bus Address Register (BAR) 76xxx2** Control and Status Register (CSR) 76xxx4** Data Buffer Register (DBR) 76xxx6**
I/O connection:	Several stranded cables available (BC08R, BC08S)
Power:	+5V, ±5% @ 3 A; normally available from system power supplies
Size:	One system unit
Weight:	4½ pounds (approximately)

* Depending on memory and other options chosen.
** User-selectable addresses.

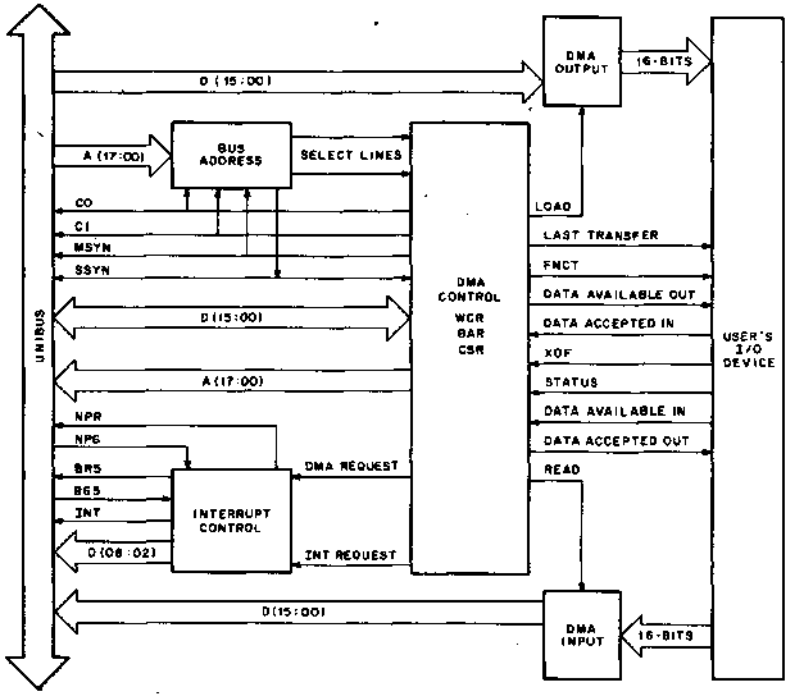


Figure 9 DECkit11-D Block Diagram

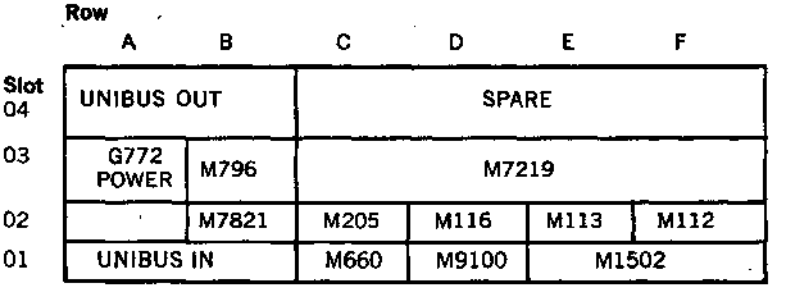


Figure 10. DECkit11-D Module Utilization Diagram (Pin Side)

Hardware/Accessories For DECkit11 Series

If mounting space is available in the existing PDP-11 processor mounting box, the DECkit can be installed there and jumpered to the existing panels by a UNIBUS Connector Module, M920. Power is supplied from the processor power supply, or from an additional H720 C or D Power Supply.

If the Interface Kit is installed in a separate mounting rack, the UNIBUS is extended to that rack with a BC11A cable. This cable is available in various standard lengths from 2 ft to 35 ft.

Input/Output Cables

Type	Connectors
BC08R-XX[1]	H856 to H856[2]
BC04Z-XX[1]	H856 to open-ended[2]
BC07A-XX[1]	H856 to open-ended[2]
BC07D-XX[1]	H856 to open-ended[2]

Notes: 1. XX is length in feet
2. H856 is a female connector

DECkit01-A

Description

DECkit01-A Remote Analog Data Concentrator Kit is a prewired package of standard Digital Equipment Corporation products which provides a convenient method of monitoring analog voltages at a remote location. The analog voltages are converted to numerical data and transmitted as an ASCII-coded message over a serial communication line. The transmitted information can be displayed directly through a terminal or can be processed on-line by a computer. Because of the full-duplex (two-way) communication line, DECkit01-A can be remotely controlled from the device with which it is communicating.

Single ASCII character codes will command the DECkit01-A to scan up to eight channels continuously, scan up to eight channels one time, or sample an individual channel. There are switch or TTL inputs to the DECkit01-A which allow the user to select the baud rate, skip over unused channels, enter an identification character into the output message (batch number, experiment number, etc.). Outputs are provided where unused ASCII characters can be decoded to perform some task at the remote site. An external trigger input is available which will cause all active channels to be examined one time. To allow DECkit01-A to be custom-tailored for a specific application, spare module slots are available. These spare slots, along with the timing pulses, time states, and control signals which are present on the prewired backplane, offer the user a great deal of design flexibility.

DECkit01-A can be used as a *remote* A/D front-end for a computer or as a *stand-alone* system with a terminal. In either case, this product lends itself to applications such as monitoring industrial processes, laboratory experiments, or environmental conditions.

FEATURES

- Complete asynchronous serial line interface
- Full duplex operation
- Programmable from terminal keyboard or computer
- Seven selectable data receive/transmit baud rates—110 to 4800 baud
- Provisions for an external baud rate clock—up to 9600 baud
- Selectable parity options
- Up to eight analog channel inputs—bipolar (±10V) single-ended, high impedance
- 2.4% overrange capability
- Up to 48 samples per second (or 96 with external clock)
- Fast analog-to-digital conversion with 5 mV resolution
- Flexible operation modes—program control plus external trigger
- Serial, 10-character ASCII-coded output message compatible with any ASCII terminal or computer with ASCII interface
- Compatible with Teletype current loop or EIA RS-232-C serial lines
- Digital and analog power supplies included in the kit
- Spare slots available for custom logic additions

SPECIFICATIONS

ANALOG

Number of Channels:	8, single-ended
Input Range:	+10V to −10V
Input Impedance:	>10 megohms
Source Impedance:	≤1K ohms
Resolution:	12 bits (LSB = 5 mV)
Accuracy:	±3.5 mV
Temperature Coefficient:	280μV/°C

DIGITAL

All logic input and output control lines to DECkit01-A are TTL-compatible.

External Trigger:	A High to Low transition causes a single scan of all enabled channels.
Channel Enable:	When one of these eight lines is connected, that respective channel will be enabled. Any number of channels, up to eight, may be enabled at the same time.
External User Code:	These six lines represent the least significant bits of the 7-bit ASCII code. Any of the normally High lines may be pulled Low for character coding.
Read Data Lines:	These eight lines can be used to decode any unused ASCII character.
External Clock:	This input can be used to select transmit/receive baud rates other than the seven jumper selectable rates.

SERIAL I/O

Levels:	TTY 20-mA current loop or EIA RS-232-C available.
Baud Rates:	Jumper Selectable 110 150 300 600 1200 2400 4800 External Clock Up to 9600
Character Format:	7-level Asynchronous Serial ASCII code with even parity. 2 stop bits (110 baud). 1 stop bit (all baud rates except 110).

Serial Output Message Format:

Character	Information
1	Line feed (↑)
2	User-defined ASCII character
3	Channel number (0-7)
4	Voltage Polarity (±)
5, 6, 7, 8, 9	Voltage—in millivolts
10	Carriage return (↵)

GENERAL

Line Voltage:	
DECkit01-AA	115 V, 47-63 Hz
DECkit01-AB	230 V, 47-63 Hz
Power:	170 W (maximum)
Weight:	15 pounds (approximately)
Size:	19 inches wide x 5¼ inches high x 13 inches deep

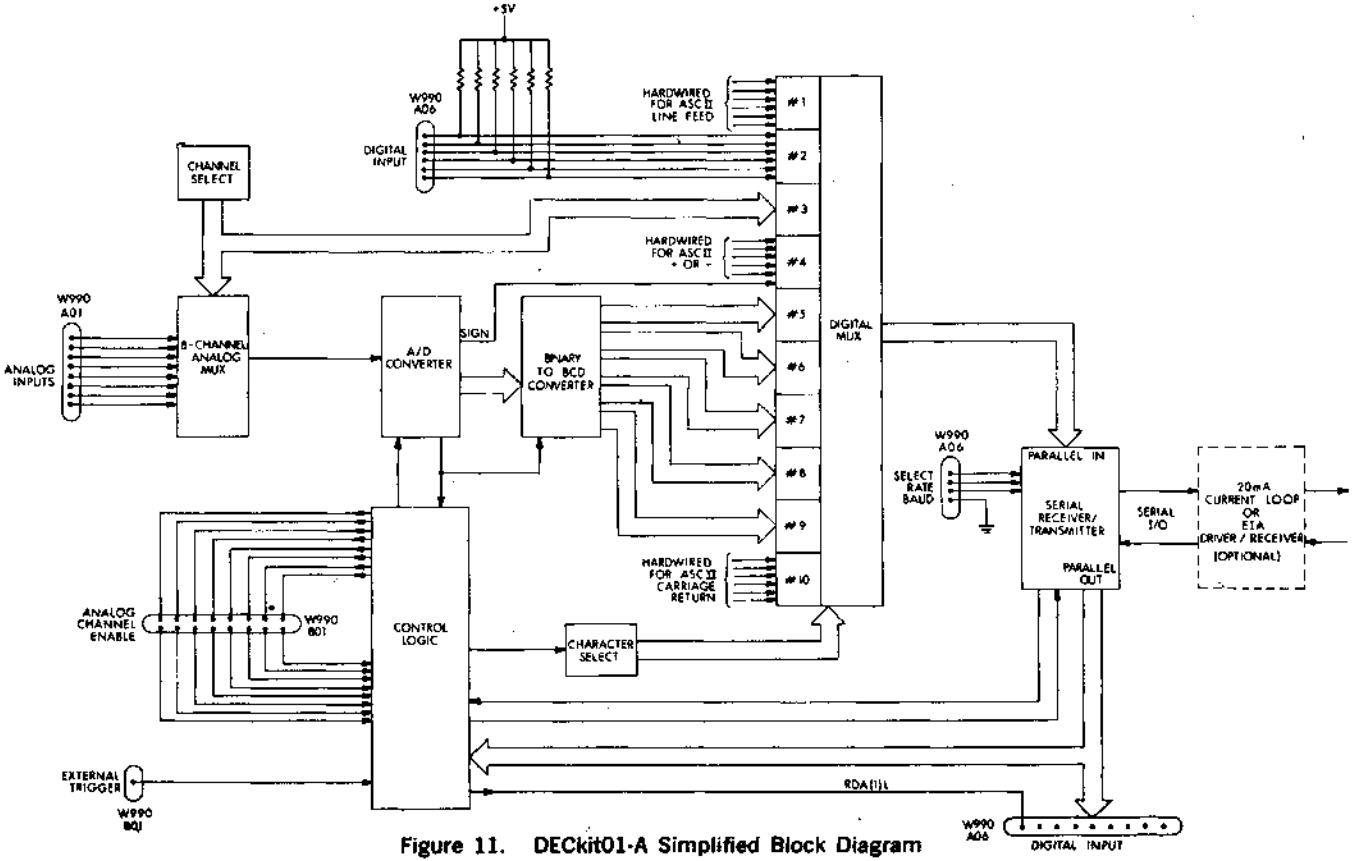
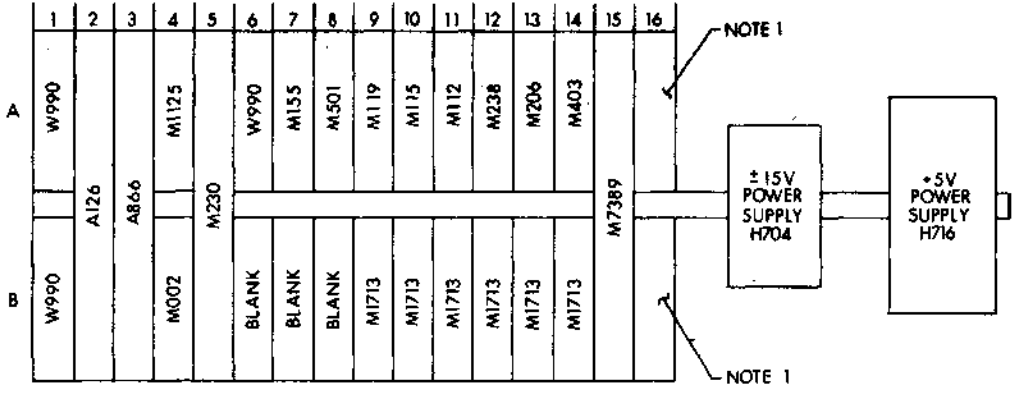


Figure 11. DECkit01-A Simplified Block Diagram



NOTE 1. When 20 mA current loop compatibility is required, module M598 occupies slot A16 and module M973 occupies slot B16. When EIA compatibility is required, module M594 occupies slot A16 and module M970 occupies slot B16. Modules M598 and M973 and modules M594 and M970 are not part of DECkit01-A; they must be ordered separately.

Figure 12. DECkit01-A Equipment Layout Diagram (Pin Side)

TABLE VII DECkit01-A Parts List

ITEM	STOCK NO.	DESCRIPTION	Quantity used in	
			DECkit01-AB	DECkit01-AA
1	7009441-1	Logic Assembly; includes print set, power supplies, wired assembly (115 V)	1	
2	7009441-2	Logic Assembly; includes print set, power supplies, and wired assembly (230 V)		1
3	9107673-9	Ac Power Cord	1	
4	9008853	Ac Power Connector (male)		1
5	9008855	Ac Power Connector (female)		1
6	A126	8-Channel Multiplexer Module	1	1
7	A866	12-Bit A/D Converter Module	1	1
8	M002	Logic HIGH Source Module	1	1
9	M112	6 4-Input NOR Gates Module	1	1
10	M115	8 3-Input NAND Gates Module	1	1
11	M119	3 8-Input NAND Gates Module	1	1
12	M155	4-Line to 16-Line Decoder Module	1	1
13	M206	6 D-Type Flip-flop Module	1	1
14	M230	Binary-to-BCD & BCD-to-Binary Module	1	1
15	M238	Dual 4-Bit Input Synchronous Up/Down Counter Module	1	1
16	M403	RC Multivibrator Clock Module	1	1
17	M501	Schmitt Trigger Module	1	1
18	M1125	10 Exclusive OR Gates Module	1	1
19	M1713	16-Line to 1-Line Data Selector Module	6	6
20	M7389	Asynchronous Transceiver Module	1	1
21	W990	Jumper Module	3	3

HOW TO ORDER

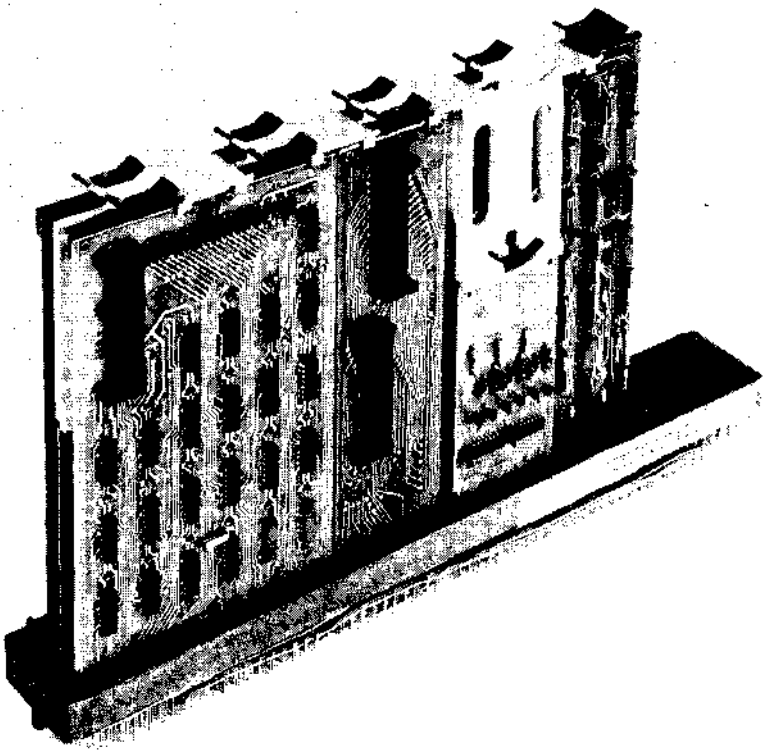
Fully configured Kits may be ordered by specifying the appropriate Kit letter designation, as follows:

Description	Order
DECkit11-H	KIT11-H
DECkit11-F	KIT11-F
DECkit11-K	KIT11-K
DECkit11-M	KIT11-M
DECkit11-D	KIT11-D
DECkit01-A	KIT01-A

Less than fully configured Kits must be ordered as individual parts; refer to the individual Interface Kit Data Sheet.

SERVICE

Field Service is available on a time-and-materials basis. For full information, contact your local DIGITAL Field Service office.



DECkit11-D

microprocessors

MICROPROCESSORS

Once again, for the third time in two decades, the computer industry is experiencing the beginnings of another revolution in computing technology which will offer the uses of computer processing/control concepts to a market more than a magnitude larger, and at costs an order of magnitude lower, than at present.

This revolution has been brought about by the commercial availability of MOS-LSI techniques used both in general logic and memory technologies, culminating in the much-touted "computer-on-a-chip." Just as minicomputers opened new market areas in data communications, laboratory automation, and process control, the microcomputer will open up the largely unsaturated industrial and professional markets where specialized computing power is required on a local basis. Typical of these areas are:

"Smart" instruments and terminals
Medical instrumentation
Machine tool automation
Traffic light control
Optical character recognition
Automatic banking
Environmental control of buildings
Process control
Conveyor systems

Digital Equipment Corporation offers the power and versatility of this emerging concept in the form of the Microprocessor Series (MPS). The MPS is a set of modules that reflect the latest LSI and MSI technology, thus yielding more numerous and more useful built-in design solutions per module. This set of modules may be regarded as a logical extension of the M Series modules described throughout this handbook. Although the internal circuitry is MOS-LSI, all external interfacing remains M Series TTL-compatible.

The following modules and associated products are described in this section.

M7341	Processor Module
M7344-YA, YB, YC	Read/Write Memory Modules
M7345	Programmable Read-Only Memory Module
M7346	External Event Detection Module
KC341	Monitor/Control Panel
MR873-A	Read-Only Memory Programmer
KMP01	Prewired System Backplane
QF500-AB	Software Package

M7341
PROCESSOR MODULE

MICRO-
PROCESSOR
SERIES

DESCRIPTION

The M7341 Processor Module (PM) contains a single chip MOS/LSI microprocessor along with the integrated logic and control circuitry necessary to operate as a parallel 8-bit central processing unit. This microprocessor support logic consists of a clock; a four-channel input multiplexer; data, memory, and address bus gating; I/O control logic; interrupt recognition logic; and a universal asynchronous receiver/transmitter.

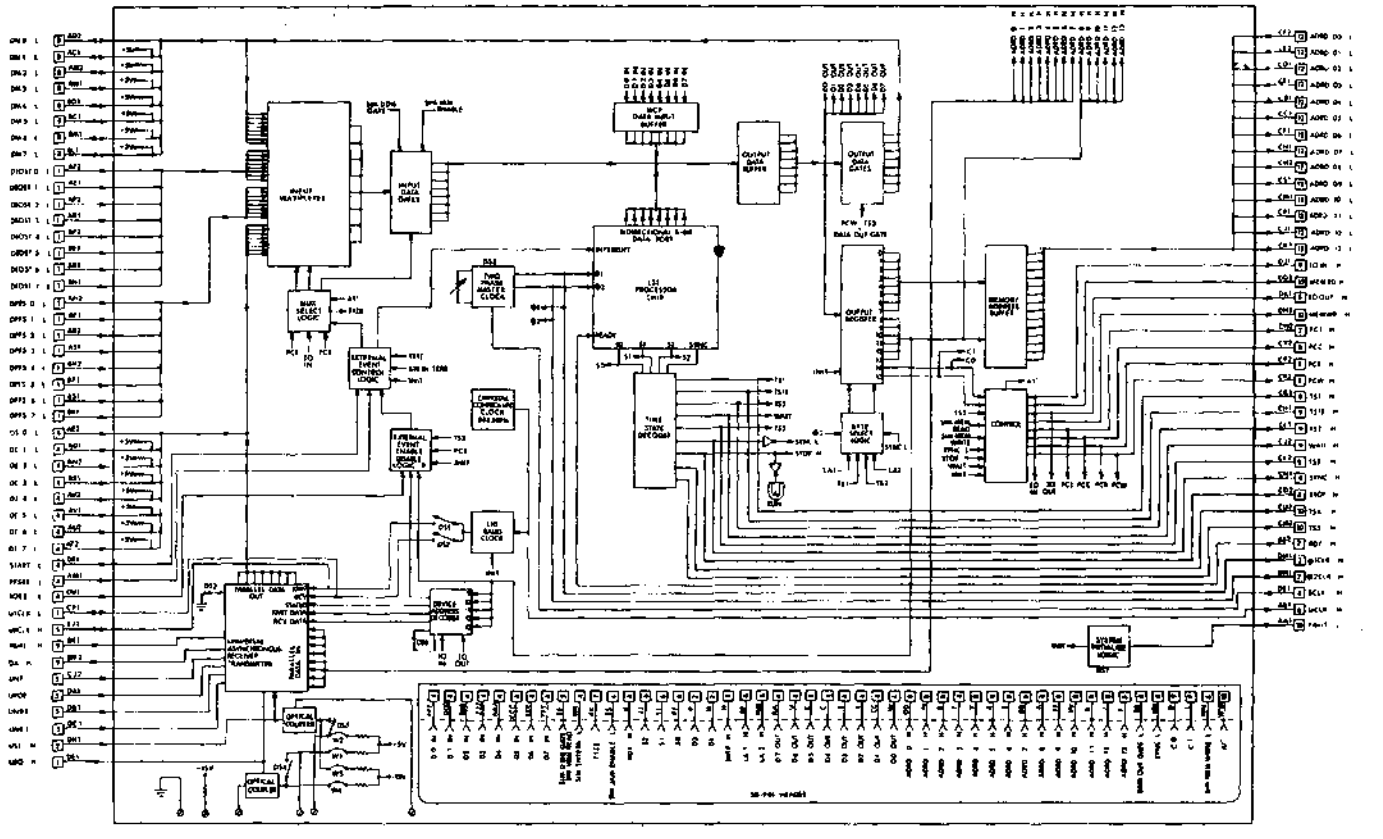
The single-chip microprocessor contains seven general-purpose registers, four condition flip-flops, instruction control and decoding logic, and a memory stack. All communication between internal registers and logic and other MPS modules and peripheral devices is conducted through an 8-bit bidirectional data port integral to the processor chip. The internal stack contains the 14-bit program counter and seven other 14-bit registers for nesting up to seven levels of subroutines. This 14-bit addressing capability permits accessing up to 16K memory locations that can be any mixture of RAM or ROM.

The processor chip is also equipped with an interrupt line which allows the enabling or disabling of interrupts. Input to this interrupt recognition logic is generated by the external event detection module which implements the detection of, and response to, application-defined events or power failure conditions. Enabling and disabling interrupts is performed under program control.

Serial communication between the processor and external equipment is furnished by an integral universal asynchronous receiver/transmitter. Through this interface, programs can be loaded from an external peripheral device such as a paper-tape loader and MPS systems communicating directly with external data bases.

The Processor Module executes 48 basic instructions which can be functionally grouped into five categories:

- Register operations
- Accumulator operations
- Program counter and stack control operations
- Input/output operations
- Machine operations



FEATURES

- 8-bit parallel microprocessor completely contained on a single quad module.
- Uses proven commercially-available LSI microprocessor chip.
- Complete instruction decoding and control.
- Instruction execution time ranges from 12 to 44 μs.
- User program development supported by comprehensive software tools package.
- Contains full duplex universal asynchronous receiver/transmitter for serial communication with external data sources.
- Separate internal clock for 110-baud receiver/transmitter operation.
- Receiver/transmitter switchable to external clock for operation at up to 9600 baud.
- Serial data communication in either TTL or current-loop mode.
- Register complement includes seven general purpose registers including two memory address pointers and an accumulator.
- Contains a stack to implement seven-level subroutine nesting.
- Executes 48 arithmetic, logical, register transfer, and memory reference instructions.
- Arithmetic unit capable of multiple precision arithmetic.
- Module can access an address space of up to 16K words.
- External event interrupts can be enabled and disabled under program control.
- Four multiplexed input ports for memory and I/O data, external event restart and power-fail addresses, and halt instructions.
- Module can directly address eight input peripheral devices and 24 output peripheral devices.
- TTL-compatible inputs and outputs.
- Module plugs into standard DEC H863 wire-wrap connector block backplanes.

SPECIFICATIONS SUMMARY

Performance Specifications

OPERATING SPEED @ 500 kHz
Two-Phase Clock Period: 2μs
State Time: 4μs
Instruction Time: 12 to 44μs

Power Consumption: 1.6 A @ +5 V, 150 mA @ −15 V; 10.25 W

WORD SIZE
Data: 8-bit Word
Instruction: 1, 2, or 3 8-bit Words
Address: 14 bits

INPUT DATA PORTS
Memory Data: 8 bits
Peripheral Data: 8 bits
Power Fail/Stop: 8 bits Multiplexed
I/O External Event Interrupt/Start: 8 bits

INPUT/OUTPUT LINES
- Memory Data: 8 bits bidirectional
- Memory Address: 14 bits, output only
- Peripheral Data: 8 bits input and output
- Peripheral Address: 5 bits, output only
- Communication Lines: 2, TTL or 20 mA current loop, active or passive
- Baud Rate
  - With Internal Clock: 110 baud (1.76 kHz)
  - With External Clock: 9600 baud (153.6 kHz), maximum (TTL)

INSTRUCTION REPERTOIRE
- Number of Basic Instructions: 48
- Instruction Categories
- Register Operation Instructions
- Accumulator Operation Instructions
- PC and Stack Control Instructions
- I/O Instructions
- Machine Instructions

ELECTRICAL SPECIFICATIONS

Input Logic Levels
- Logical Low: 0.8 Vdc max.
- Logical High: 2.0 Vdc min.

Output Logic Levels
- Logical Low: 0.4 Vdc max.
- Logical High: 2.4 Vdc min.

Power Consumption: 1.6A +5V, 150 mA @ −15V, 10.25 W

MECHANICAL SPECIFICATIONS

Board Type: Quad-height, extended-length, single-width

Dimensions: 10.436 x 8.50 x 0.50 inches
(26.5 x 21.6 x 1.27 cm)

ENVIRONMENTAL SPECIFICATIONS

Ambient Temperature
- Operating: 41 to 122°F, (5 to 50°C)
- Nonoperating: −40 to 150°F, (−40 to 66°C)

Humidity: 10 to 95%, noncondensing

Altitude
- Operating: 0 to 8,000 ft. (2.4 km)
- Nonoperating: 0 to 30,000 ft. (9.1 km)

M7344-YA,-YB,-YC READ/WRITE MEMORY

MICRO-PROCESSOR SERIES

DESCRIPTION

The M7344 Read/Write Memory Module provides a 1K, 2K, or 4K x 8-bit random access memory capacity along with all necessary timing, control, and decoding logic. This module is completely contained on a single quad, extended-length PC board. The module memory matrix is formed by up to 32 1024 x 1-bit static MOS MSI memory circuits. The nature of these MOS circuits precludes the need for external refresh logic.

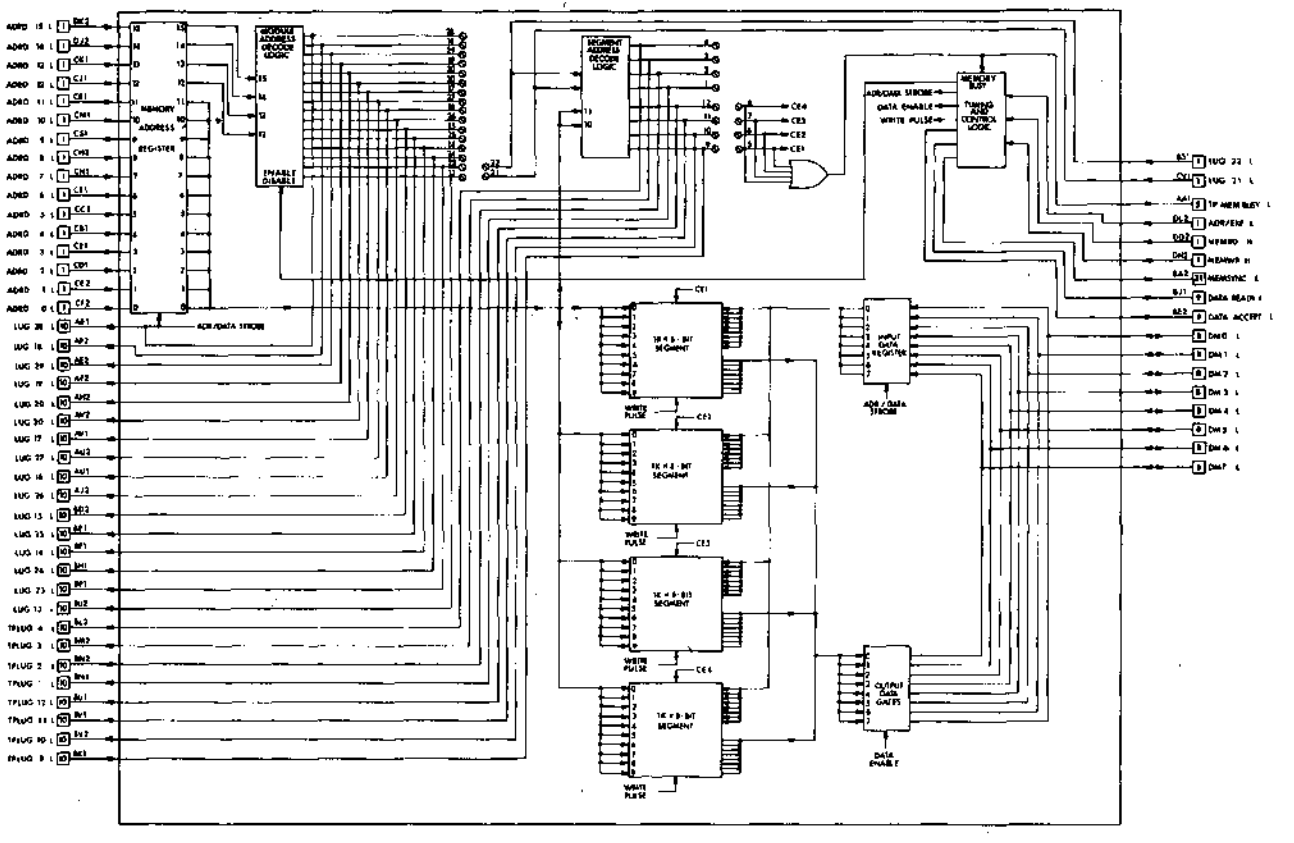
The M7344 Read/Write Memory Module is available in three versions to satisfy varying memory capacity requirements:

- M7344-YA 1K x 8-bit capacity
- M7344-YB 2K x 8-bit capacity
- M7344-YC 4K x 8-bit capacity

All versions of the M7344 can be accessed by up to 16-bits of address data and are equipped with an address expansion line to implement multi-module memory systems having potential capacities of up to 128K 8-bit words. M7344 Read/Write Memory Modules also contain a jumper network which can be configured to permit assignment of a module within an application-defined address space.

FEATURES

- Completely self-contained, fully decoded 8-bit read-write memory contained on standard quad, extended-length module.
- 16-bit memory address register plus dedicated address expansion line.
- Jumper network on module allows assignment of address space in 1K or 4K increments within 64K locations.
- All jumper lugs also brought out to module connector for alternative wire-wrap address space assignment.
- Memory cycle time (read cycle or write cycle) 1.15μs.
- Data ready, data accepted, and memory synchronization signals brought out on module connector for external use.
- A general-purpose memory module, the M7344 can be used with most any 8-bit minicomputer, microprocessor, or logic design.
- Power requirement is +5Vdc only.
- Memory module completely compatible with M7341 Processor Module 14-bit address.
- All inputs and outputs are TTL compatible.
- Module plugs into standard DEC H863 wire-wrap connector block backplane or equivent.
- Memory is designed for both asynchronous and synchronous operation.
- All M7344 versions are pin-for-pin compatible with M7345 Programmable Read-Only Memory modules.


MEMORY ADDRESS REGISTER
MEMORY BUSY CONTROL LOGIC
ADR/DATA STROBE
DATA ENABLE
WRITE PULSE
INPUT DATA REGISTER
OUTPUT DATA GATES
DATA ENABLE

SPECIFICATION SUMMARY

PERFORMANCE

Memory Type: N-channel static MOS
Data Word Size: 8 bits
Address Word Size: 16 bits plus address expansion line
Number of Words: 1024, 2048, or 4096
Memory Read or Write Cycle Time: 1.15μs minimum

ELECTRICAL

Input Logic Levels
  TTL Logical Low: 0.8 Vdc maximum
  TTL Logical High: 2.0 Vdc minimum
Output Logic Levels
  TTL Logical Low: 0.4 Vdc maximum
  TTL Logical High: 2.4 Vdc minimum
Data Bus Receivers/Drivers
  Logical Low: 0.7 Vdc maximum
  Logical High: 2.4 Vdc minimum
Address Bus Receivers
  Logical Low: 0.7 Vdc maximum
  Logical High: 2.4 Vdc minimum
Power Consumption
  M7344-YA: 1.2 A @ +5V, 6.0 W
  M7344-YB: 1.5 A @ +5V, 7.5 W
  M7344-YC: 2.2 A @ +5V, 11.0 W

MECHANICAL

Board Type: Quad-height, extended-length, single-width
Dimensions: 10.436 x 8.50 x 0.5 inches (26.5 x 21.6 x 1.27 cm)

ENVIRONMENTAL

Ambient Temperature
  Operating: 41 to 122°F, (5 to 50°C)
  Nonoperating: −40 to +150°F, (−40 to 66°C)
Humidity: 10 to 95 percent, noncondensing

M7345 PROGRAMMABLE READ-ONLY MEMORY

MICRO-PROCESSOR SERIES

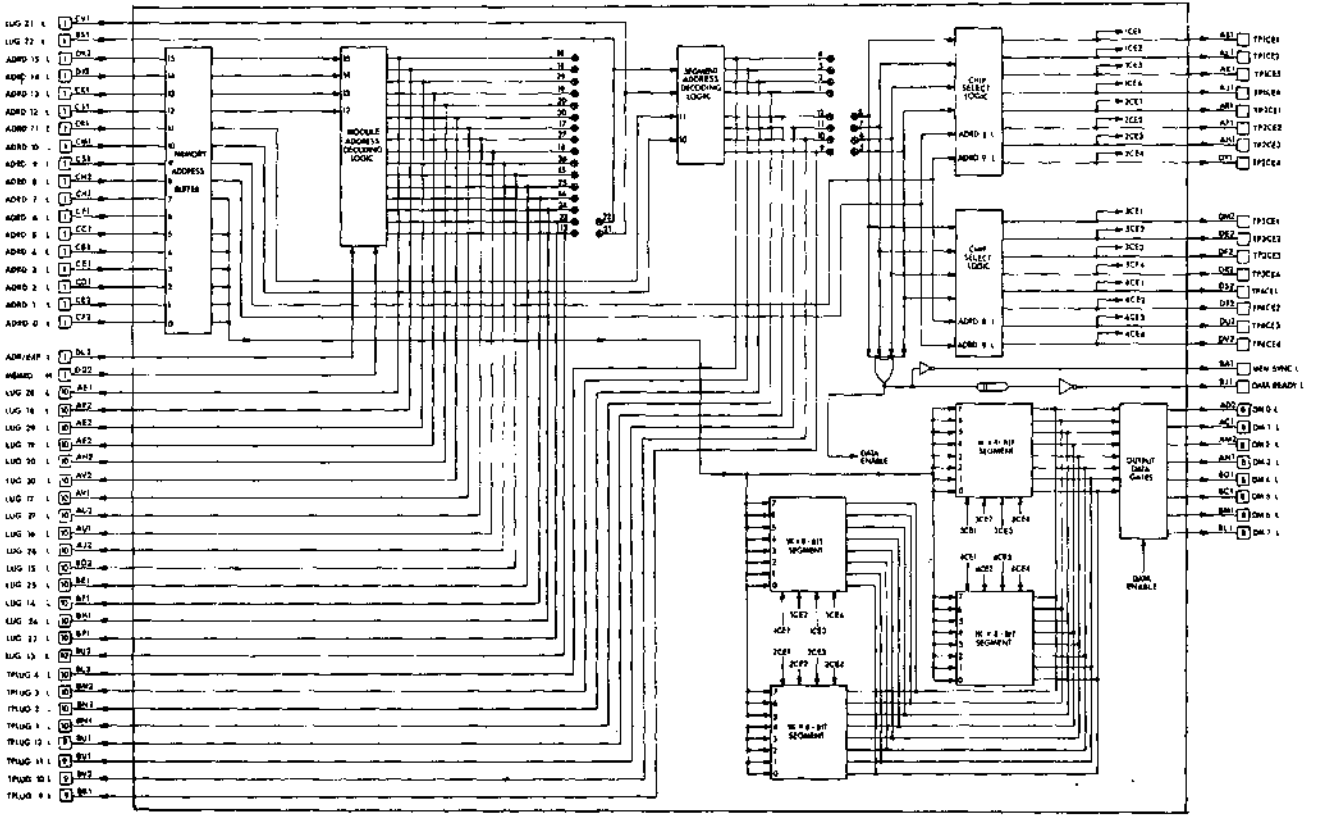
DESCRIPTION

The M7345 Programmable Read-Only Memory module provides a read-only data storage capacity which can vary from 256 8-bit words to 4K 8-bit words in 256-word increments. This read-only memory capacity is formed by static MOS 256 x 8-bit PROM circuits (such as the Intel Corp. 1702A) which are electrically programmable and easily erasable by ultraviolet light. The memory is completely contained on a quad, extended-length module and includes sockets for the memory circuits, and all address decoding, control, and timing logic. The PROM circuits necessary to form the memory matrix are furnished as a separate item apart from the M7345 module.

Maximum PROM capacity is formed by inserting the full complement of 16 circuits into the sockets. These 256 x 8-bit PROM circuits can be added as necessary to satisfy changing system requirements. Socket mounting also permits each circuit to be removed for erasure and reprogramming. A transparent quartz lid on each PROM circuit permits exposure to an ultraviolet light source or erasure of an existing bit pattern. A new bit pattern can then be electrically written.

FEATURES

- Completely self-contained, fully decoded programmable read-only memory contained on standard DIGITAL quad-height module.
- Memory capacity formed by 256 x 8-bit PROM circuits which are electrically programmable and erasible with ultraviolet light.
- Memory circuits are socket-mounted on module for easy insertion and removal.
- Module accepts 16-bit memory address and is equipped with an address expansion line.
- Module memory capacity expandable from 256 to 4K locations in 256-word increments.
- Jumper network on module allows assignment of address space in 1K to 4K increments within 64K locations.
- Jumper network lugs also brought out to module connector for alternative wire-wrap address space assignment.
- Memory read cycle time 1.15 μs.
- Data-ready and memory-synchronizing signals brought out on module connector for external use.
- Memory module logic includes a complete integral general-purpose interface.
- A general-purpose memory module, the M7345 can be used with almost any 8-bit minicomputer or microprocessor, or paralleled for 16 bits.
- Programmable Read-Only Memory Module is pin-for-pin compatible with the M7344 Read/Write Memory Module.
- Input power requirements are +5 Vdc and −15 Vdc.


MEMORY ADDRESS BUFFER
MODULE ADDRESS DECODING LOGIC
SEGMENT ADDRESS DECODING LOGIC
CHIP SELECT LOGIC
CHIP SELECT LOGIC
DATA ENABLE
OUTPUT Data Gates
DATA ENABLE

SPECIFICATION SUMMARY

PERFORMANCE

Memory Type: Static MOS
Data Word Size: 8 bits
Address Word Size: 14 bits, expandable to 16 bits plus address expansion line
Number of Words: Expandable, from 256 words to 4K words
Read Cycle: 1.5μs, nondestructive readout
Erasure Method: Ultraviolet light; 256 words erased per circuit exposed
Erasure Time: 10-minutes
Program Write Time: 2 minutes typical, per 256 words

ELECTRICAL

Input Logic Levels
  TTL Logical Low: 0.8 Vdc maximum
  TTL Logical High: 2.0 Vdc minimum
Output Logic Levels
  TTL Logical Low: 0.4 Vdc maximum
  TTL Logical High: 2.4 Vdc minimum
Data Bus Drivers
  Logical Low: 0.7 Vdc maximum
  Logical High: 2.4 Vdc minimum
Address Bus Receivers
  Logical Low: 0.7 Vdc maximum
  Logical High: 2.4 Vdc minimum
Power Consumption
  M7345 Module without PROMs: 350 mA @ +5V, 100 mA @ −15V; 3.7 W
  23-00-A4-03 256x8-bit PROM Chip: 20 mA @ +5V, 70 mA @ −15V; 1.2 W
  M7345 with 1K Memory: 490 mA @ +5V, 300 mA @ −15V; 6.0 W
  M7345 with 2K Memory: 630 mA @ +5V, 530 mA @ −15V; 11.0 W
  M7345 with 4K Memory: 900 mA @ +5V, 1.0 A @ −15V; 19.5 W

MECHANICAL

Board Type: Quad-height, extended-length, single-width
Dimensions: 10.436 x 8.50 x 0.5 inches (26.5 x 21.6 x 1.27 cm)

ENVIRONMENTAL

Ambient Temperature
  Operating: 41 to 122°F, (5 to 50°C)
  Nonoperating: −40 to +150°F, (−40 to 66°C)
Humidity: 10 to 95 percent, noncondensing

M7346
EXTERNAL EVENT DETECTION

MICRO-PROCESSOR SERIES

DESCRIPTION

The M7346 External Event Detection Module (EEDM) is a multipurpose unit designed for use in conjunction with the M7341 Processor Module to implement interrupt priority schemes, power failure detection, and processor restart and halt control. The M7346 implements nine levels of priority arbitration. These include application-defined six-level priority interrupt schemes, an ac and dc power failure detection capability, and the processor control functions of Halt and Restart. The EEDM is completely contained on a single-height, extended-length PC board.

Separate input lines to the EEDM provide for encoding up to six levels of external application-defined event priority. Each of these lines, when asserted, initiates an attempt to jam a 1-byte unconditional call (RST) instruction into the M7341 Processor Module external event port.

The EEDM priority logic arbitrates all assertions and selects the highest level asserted, then jams the corresponding instruction into the Processor Module. The jammed RST instruction associated with each priority level (zero through five) constitutes an unconditional call on one of six 8-byte subroutines located in the first 48 words on an MPS system memory.

The eight output lines which propagate the instruction being jammed, are connected in common to the processor module external event port and the power-fail port.

To jam an RST instruction, the EEDM asserts a signal to enable multiplexing of the external event port and to initiate an external event interrupt. If interrupts are enabled at the Processor Module, the RST instruction is fetched and executed. If not, the RST instruction is ignored.

The seventh priority level is asserted by either a manually-initiated start signal or automatically as a consequence of power-up. In either of these cases, an RST instruction is generated which makes an unconditional call on eight reserved memory words headed by location 60_8.

Priority level eight is asserted by the power failure detection circuit which monitors ac power inputs to an MPS system. When a power failure condition is detected, an RST instruction is automatically generated which makes an unconditional call on location 56 (70_8). Since level eight is the highest arbitrated priority, a power failure takes precedence over any of the six levels of application-defined event priorities as well as the seventh or start level.

Level nine implements the halt function for MPS systms. This function can be initiated manually or automatically, and overrides all other priorities. When initiated, a halt instruction is placed on the lines to the processor module, and the power fail/stop port is enabled for multiplexing. When fetched, this instruction forces the Processor Module into the stopped state.

FEATURES

- Eight Interrupt priority request lines available to provide eight arbitrated priority levels.
- Power failure detection circuit continuously samples ac voltage levels.
- Inputs for optional external ac and/or dc power failure detection.
- Power failure detection is highest arbitrated priority.
- Halt function has precedent over all arbitrated priorities.
- Module senses power-up condition to initiate an automatic start.
- External event response time 12 to 44 μs.
- Power failure response time 35 ms from ac power loss to power fail interrupt request.
- Real-time clock signal (power line sync signal) available at module connector.
- Power fail indication signal (AC LOW) available at module connector.
- Except for ac sample input, all inputs and outputs are TTL-compatible.
- Module is contained on standard single-height extended-length board and plugs into standard DEC H803 wire-wrap connector block backplanes or equivalents.

SPECIFICATION SUMMARY

PERFORMANCE
Number of Event Detection Input Lines: 8
Priority Encoded: 1—lowest
8—highest
External Event Response Time: 12 to 44 μs
Power Failure Response Time: 35 ms (from ac loss to power-fail interrupt request)
Input Polarity,
External Event Lines: Logic High = False; Logic Low = True
Output Polarity,
Data Lines to Processor Module: Logic High = False; Logic Low = True

ELECTRICAL
Power Supply: +5 Vdc,
Input Logic Levels
Logical Low: 0.8 Vdc maximum
Logical High: 2.0 Vdc minimum
Output Logic Levels
Logical Low: 0.4 Vdc maximum
Logical High: 2.4 Vdc minimum
Noise Immunity: 400 mV
Power Fail Sense Input: 6.3 Vac
Power Consumption: 250 mA @ +5 V
50 mA @ 6.3 V ac, 1.6 W

MECHANICAL
Board Type: Single height extended-length, single-width
Dimensions: 2.4375 X 8.50 X 0.50 inches
6.191 X 21.590 X 1.270 cm

ENVIRONMENTAL
Ambient Temperature
Operating: 41 to 122°F, (5 to 50°C)
Nonoperating: —40 to 150°F, (—40 to 66°C)
Humidity: 10 to 95% noncondensing

KC341-B MONITOR/CONTROL PANEL

MICRO-PROCESSOR SERIES

The KC341-B Monitor/Control Panel (MCP) serves as an operator's panel to provide an on-line control and program diagnostic capability for systems configured from Microprocessor Series modules. In addition to the conventional panel controls and indicators, the MCP is equipped with controls and visual displays for examining and changing the content of manually-accessed read/write memory locations and for performing single-step instruction execution. These functions are supported by a resident memory consisting of a 256 x 8-bit PROM and a 32 x 8-bit RAM completely contained in the MCP. The PROM and the RAM are directly addressable as system memory, and the RAM can be used as a scratch pad by user diagnostics and by operating programs.

The MCP interfaces directly with the M7341 Processor Module through a dedicated cable (supplied with the MCP). Although normally configured for table mounting, the MCP can be panel-mounted in a suitable EIA rack panel.

FEATURES

- Convenient size (18-inches wide by 8¾-inches deep by 1¾-inches high) for placing on bench, desk top, etc.
- Completely interfaced with CPU Module via cable.
- Allows interrogation of CPU timing signals through an LED array.
- Address data can be loaded into the CPU Module via 14-bit switch register.
- Address and memory data can be displayed.
- Controls supplied:
  - —Address load
  - —Start
  - —Deposit
  - —Continue
  - —Examine
  - —Single cycle
  - —Display data
  - —Display address
- Integral read/write scratch-pad memory for diagnostic use.
- Integral read-only memory bootstrap loader program.

SPECIFICATIONS

ELECTRICAL

Power Consumption	2.43A @ +5V, 60mA @ −15V, 12W

MECHANICAL

Width	18 in. (45.7 cm)
Depth	8.75 in. (22.2 cm)
Height	1.75 in. (4.4 cm) excluding switches 2.50 in. (6.35 cm) including switches

ENVIRONMENTAL

Ambient Temperature	
Operating	41° to 122°F (5° to 50°C)
Nonoperating	−41° to 150°F (−40° to 60°C)
Humidity	10° to 95% noncondensing

MR873-A
READ-ONLY MEMORY PROGRAMMER

MICRO-PROCESSOR SERIES

The MR873-A Microprocessor ROM Programmer is a versatile option for Microprocessor Series (MPS) users, providing a capability for writing programs into chips used on the M7345 Programmable Read-Only Memory (PROM) module. Operating as an on-line peripheral device to the PDP-8/A, PDP-8/E, PDP-8/F, or PDP-8/M system, the MR873-A is a fully self-contained subsystem that will load and verify user-generated MPS routines in individual PROM chips under MRP program control. MRP is a system program, executed on the PDP-8, for controlling all MR873-A operations. Source data for loading PROMs is binary code, previously generated by the MLA assembler or the MDP debugging programs. The code can be in the form of paper tapes or a previously programmed PROM.

MRP software features the following MR873-A operations:

- Read or punch binary paper tapes, using high-speed or low-speed tape peripherals, to or from a 2048-word core buffer in the PDP-8.
- Examine and modify any buffer locations prior to writing into the PROM.
- Load specified memory locations with a constant value.
- Read PROM contents into the core buffer when PROM duplication is desired.
- Verify that all PROM locations are clear prior to writing.
- Write a block or binary data from the buffer into a PROM.
- Verify that PROM contents have been correctly written.
- List PROM contents on terminal console or line printer peripherals.

Each MR873-A hardware option includes the main MR873-A assembly, one M1703 Input Interface module, and one M1705 Output Interface module, which plug directly into the PDP-8 Omnibus, and two Y168 modules into which a PROM chip can be inserted. Three flat data cables, which are attached to the rear of the MR873-A, terminate at the interface modules. Labels are attached to each cable for proper installation. In addition, a standard power cord allows application of operating power (115 Vac, 60 Hz) for the assembly.

Only the Intel 1702A PROM chips (or equiv.) can be used with the MR873-A. Each PROM chip has a capacity for storing up to 256 eight-bit words (one memory block). The PROM chips are supplied with quartz lids, enabling ultraviolet erasure of all stored data. Hence, they are reusable as MPS needs change.

SPECIFICATIONS

OPERATING

Program	2 minutes typical, for all 256 bytes
Erasure time	10 minutes maximum
Control computer	PDP-8/A, PDP-8/E, PDP-8/F, or PDP-8/M

ELECTRICAL	
AC power	105 to 125 Vac, 50—60 Hz
AC current	0.5 A
Internal power supplies	
Continuous	+5 Vdc ± 5% 0.5 A
Continuous	+12 Vdc ± 10% @ 10 mA
Continuous	−9 Vdc ± 5% @ 60 mA
Program controlled	+50 Vdc ± 3% @ 3A
ULTRAVIOLET LIGHT SOURCE	
Lamp	Available from Ultraviolet Products, Inc., San Gabriel, California. Model UVS-54 or Model S-52
MECHANICAL	
Dimensions	10½ in. (26.7 cm) high, 19 in. (48 cm) wide, 7 in. (18 cm) deep
Mounting	Table top or rack mount (bracket supplied)
Weight	20 lb (9 kg)

MPS INTERFACE MODULES

In developing an interface structure for an MPS system, the user can take two approaches: (1) design the interface at the IV level using a wire wrap board, or (2) use available DIGITAL M Series modules. In either case, a wide variety of MPS-compatible modules and accessories are available off-the-shelf from DIGITAL. Typically, the M7328 Device Selector may be used to decode the device address from the M7341 processor. The M1501 and M1502 modules serve as efficient input and output interfaces, respectively. For custom interface circuitry, the W9661 and W9671 wire wrappable modules provide a foundation upon which to build integrated circuit interfaces.

The above modules are just a few of the many hundreds of M Series, A Series, W Series, and K Series available for utilization in a unique interfacing requirement. And, to complete the entire support package, DIGITAL offers many accessories, such as power supplies, mounting hardware, and cabling. Thus, an entire family of support hardware and accessories are available to provide the MPS user with a total system capability. Most of these products are described throughout this Handbook.

KMP01-A SYSTEM UNIT

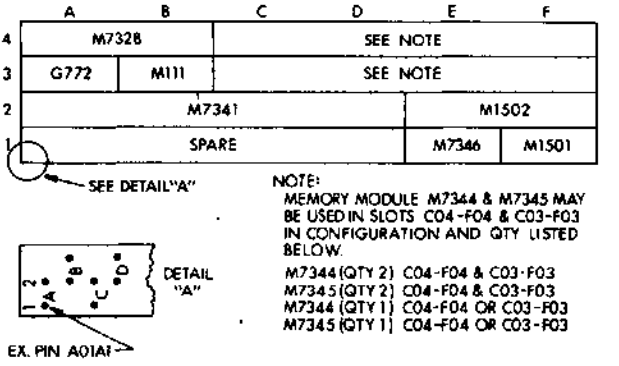
MICRO-PROCESSOR SERIES

The KMP01-A System is a prewired backplane designed to accommodate systems structured from MPS and related support modules. The unit is capable of supporting up to 8K words of memory (12K words if the spare slot is wired as a memory slot), one word out, one word in, TTY, and simulated interrupts and power fail. These features make the KMP01-A ideal for MPS software development and hardware debugging.

The drawing below shows the dedicated slot locations for each MPS and support module in a fully-configured MPS system. The recommended support modules are:

M7328	Device Selector
M111	Inverter
M1501	Input Interface
M1502	Output Interface
G772	Power Connector

These modules are standard DEC M Series available off-the-shelf. The spare slot can be used for either additional MPS memory, M Series interfaces, or W Series wire wrap modules.

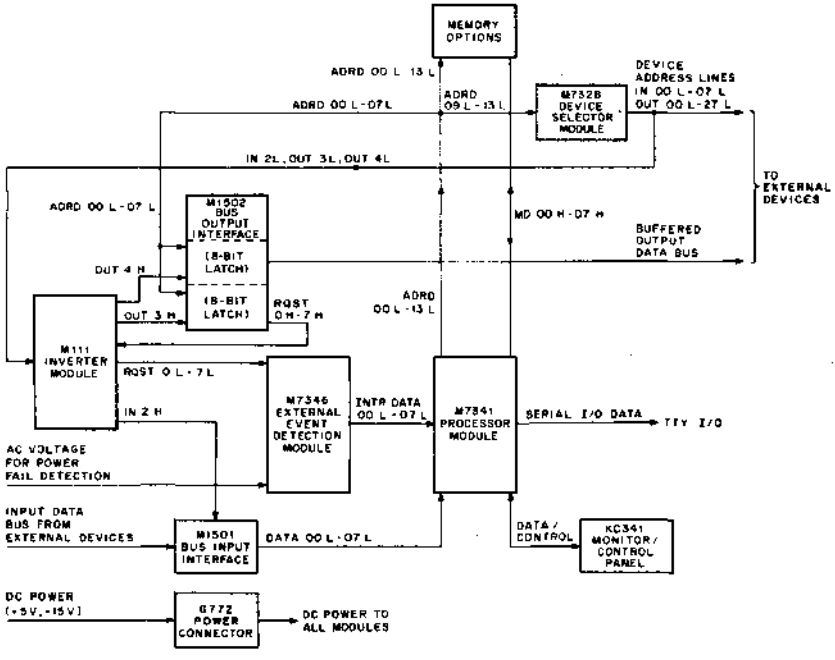


KMP01-A SYSTEM UNIT (PIN SIDE UP)

The KMP01-A can be mounted in a 19-inch rack or cabinet using the H014 Mounting Panel.

SPECIFICATIONS

Length	16.50 in. (41.9 cm)
Width	2.23 in. (5.66 cm)
Height	1.59 in. (4.04 cm)
Mounting Screws	Two #8-32 captive screws spaced 16.10 in. (40.89 cm) center-to-center and located 1.115 in. (2.83 cm) from either side.



KMP01-A/MPS MODULE FUNCTIONS

MPS SOFTWARE TOOLS-QF500-AB

MICRO-PROCESSOR SERIES

MPS SOFTWARE TOOLS—QF500-AB

The QF500-AB MPS Software Tools is a software package available to the user to aid in developing MPS application programs. This package consists of six programs as described below. All programs are provided in paper tape form. Five of the programs run on a PDP-8 minicomputer (except PDP-8/S) with 4K memory, teletypewriter, and paper tape reader/punch; the sixth program (MDP) runs on the MPS itself. The Microprocessor Series User's Handbook (DEC No. DEC-08-UMPHA-A-D) fully describes the operation of these programs and their interaction with the PDP-8.

QF500-AB PROGRAMS

PROGRAM	FUNCTION	DEC NUMBER
Microprocessor Host Loader (MHL)	Loads binary-coded tapes	DEC-08-UMPLA-A-PM
Microprocessor Language Editor (MLE)	Modifies or generates source text from Teletype commands by reading and writing paper tapes	DEC-08-UMPEA-A-PB
Microprocessor Language Assembler (MLA)	Assembles source text into binary format by reading and writing paper tapes and listing at user's option	DEC-08-UMPAA-A-PB
Master Tape Duplicator/ Verifier (MTD)	Copies paper tapes and verifies their contents	DEC-08-UMPDA-A-PB
Microprocessor ROM Programmer (MRP)	Copies and modifies paper tape and PROMs	DEC-08-UMPPA-A-PB
Microprocessor Debugging Program (MDP)	Aids in debugging of binary programs. Runs on MPS.	DEC-08-UMPMA-B-PB

Microprocessor Language Editor (MLE)

The Microprocessor Language Editor is a PDP-8 based editor oriented to paper tape usage. It is interactive and offers an extensive set of commands which can be entered from the Teletype terminal or similar keyboard terminal. It is used primarily as an on-line tool for the creation and modification of source program tapes.

The Editor is the standard PDP-8 PAL Editor and is provided in the form of a binary tape which is loaded into memory by means of the MHL program, using either the low- or high-speed paper tape reader.

The Editor facilitates both program entry and program correction. Source text is entered either directly from the keyboard or via the low-speed (Teletype terminal) or high-speed paper tape reader. Once in memory, the program text can be freely changed, deleted, or reformatted.

Microprocessor Language Assembler (MLA)
The Microprocessor Language Assembler is a powerful paper tape-oriented system which is used to assemble source code on a PDP-8 mini-computer and convert it into binary output which is then loaded and executed on the CPU Module. Input to the MLA is usually prepared with the aid of the MLE program; source text can, however, be generated off-line on a DIGITAL LT33-D Teletype terminal.

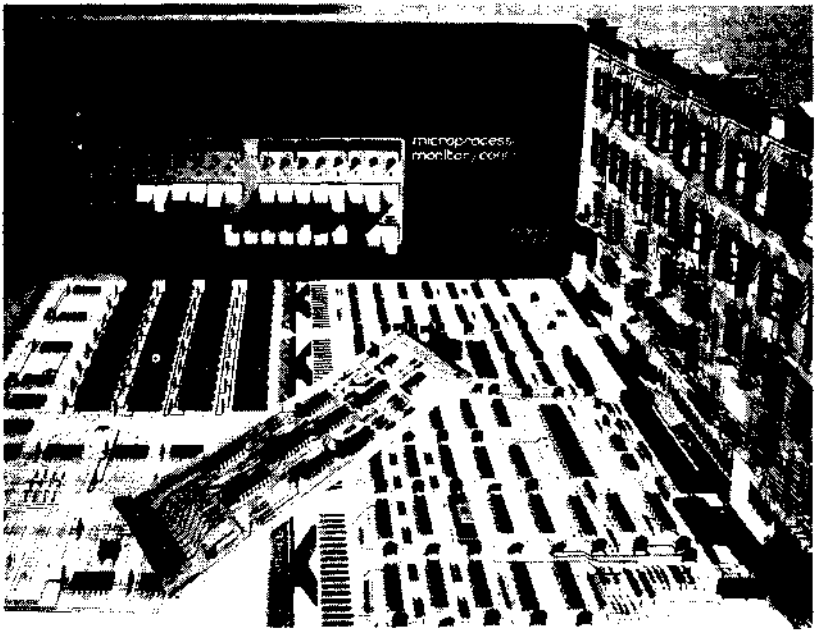
Microprocessor Read-Only Memory Programmer (MRP)
The MRP is a PDP-8 based program which, in conjunction with the PDP-8 and a PROM hardware programming option, allows the user to load, verify and modify programs in a PROM chip. Data can be entered by means of binary paper tapes produced by the MLA, or directly from the Teletype terminal keyboard.

Microprocessor Debugging Program (MDP)
The MDP resides in the Microprocessor Series memory and is used during application program development to assist in debugging. It permits debugging via the Teletype keyboard and others the following capabilities:

- Load a binary paper tape produced by MLA.
- Punch the contents of part or all of MPS memory in MLA binary format.
- Inspect part or all of MPS memory (octal typeout).
- Modify read/write memory (octal type-in).
- Set or move a program breakpoint.
- Start program execution at specified address (octal type-in).

Master Tape Duplicator Program (MTD)
The MTD copies and verifies 8-channel paper tapes. It is provided in the form of a binary paper tape which is loaded into memory by means of the MHL program.

Microprocessor Host Loader Program (MHL)
The MHL is a RIM-formatted tape used to load 8-channel paper tapes that are punched in binary code into the PDP-8 memory.



rtm modules

REGISTER TRANSFER MODULES

Register Transfer Modules (RTM) define the next higher level of computing machine design above sequential and combinatorial logic operations. Digital system design is removed from the realm of the pure logic designer and is made easily achievable by persons such as students, laboratory technicians, researchers, etc.

A standard flowchart, which includes register designations, provides full information for constructing the system. The need for extensive documentation is dramatically reduced and system trouble-shooting is considerably simplified.

RTM systems can be operated in 8-bit or 16-bit register configurations; registers may be linked to form words of 24, 32, or higher numbers of bits.

Existing functions can be expanded simply by adding steps to the flowchart, installing new modules, and making the extra wiring connections.

The modules are especially useful at the university teaching level, in experimental, medical, and research laboratories, industrial control, materials handling and manufacturing.

The concept of RTM is not new; however, this implementation is aimed at providing a powerful and low-cost design tool to digital system engineers. To design a system with these modules, the user need only be familiar with the concept of registers and register operations, and possess a fundamental understanding of the flowchart.

RTM system design and operation are explained in the handbook *Register Transfer Modules*, published by Digital Equipment Corporation.

RTM SYSTEM CONTROL

The control section of an RTM system contains the program by one of two methods: as a hardwired series of logic circuits (evoke module control) or as a list of binary codes in a memory (program control sequence).

This section of the Logic Handbook is organized into these two subsections: Evoke Module Control and Program Control Sequencer Control.

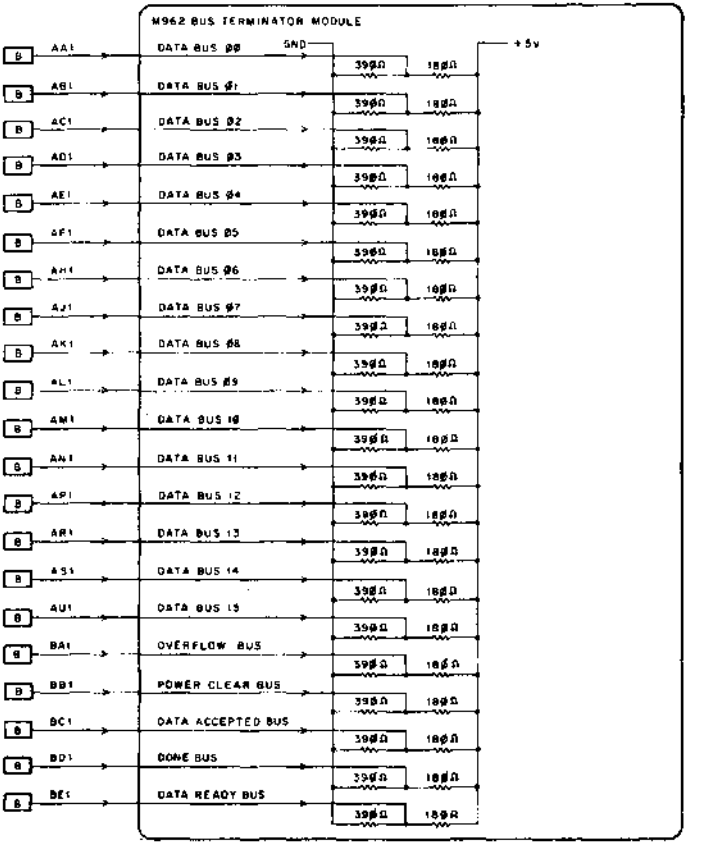
Evoke Module Control

The evoke module control method is best used in a dedicated automatic control system where changes to the program are seldom required because the task that this RTM system performs is expected to remain the same; i.e., the reprogramming flexibility of a minicomputer is not required. The program for this type control system is stored in evoke cricuits that are hardwired together in accordance with specific program requirements. Systems of this type are usually limited to approximately 100 program instructions. This method provides a very fast system because instruction fetching and decoding are not required, i.e., instructions are executed directly. An evoke module control section eliminates the cost of the additional hardware required by a program control sequencer control section. If program changes are ever required for an evoke module control section, wiring changes will probably be required.

M962
BUS TERMINATOR

RTM

Length: Standard
Height: Double
Width: Single



Volts	Power mA (typ)	Pins
+5	380	AA2, BA2
GND		AC2, BC2, AT1, BT1

The M962 Bus Terminator Module contains the pull-up/terminator resistor networks necessary to terminate the 16 Data Bus lines, the Overflow Bus line, the three Control Bus lines, and the Power Clear Bus line of an RTM system. The two resistors in each network form a voltage divider between +5 V and ground that provides a nominal +3 V on each Bus line when all Bus drivers are off (not conducting). Termination impedance is approximately 125 ohms.

This module must always be used in conjunction with an M7304 Bus Sense Register Module. However, an M7332 Bus Monitor and Terminator Module may be used instead of the M7304/M962 pair. An M7304/M962 pair or an M7332 is required in every RTM system to perform system housekeeping functions. A terminator (M962 or M7332) should be located on one end of the RTM Bus. RTM systems with buses more than 19 inches long should have terminators at both ends.

DATA BUS <15:00>—Provides terminating resistance for each of the 16 Data Bus lines <15:00> and a current source for the open-collector bus drivers of all source registers on the functional modules; e.g., M7300, M7301, M7305, M7307, M7311, M7313, M7316, M7317, M7318, M7319, M7320, M7324, M7325, and M7334.

OVERFLOW BUS—Provides terminating resistance for the Overflow Bus line and a current source for the open-collector Overflow Bus driver on the Arithmetic and Logic Function Modules M7300 and M7301. The Overflow Bus line carries the overflow output of M7300 and M7301 modules.

DATA READY BUS—Provides terminating resistance for the Data Ready Control Bus line and a current source for all open-collector Data Ready Bus drivers on the functional modules. The Data Ready Bus line carries the signal indicating that the source has placed data on the Data Bus lines.

DATA ACCEPTED BUS—Provides terminating resistance for the Data Accepted Control Bus line and a current source for all open-collector Data Accepted Bus drivers on the functional modules. The Data Accepted Bus line carries the signal indicating that the destination has received the data from the Data Bus lines.

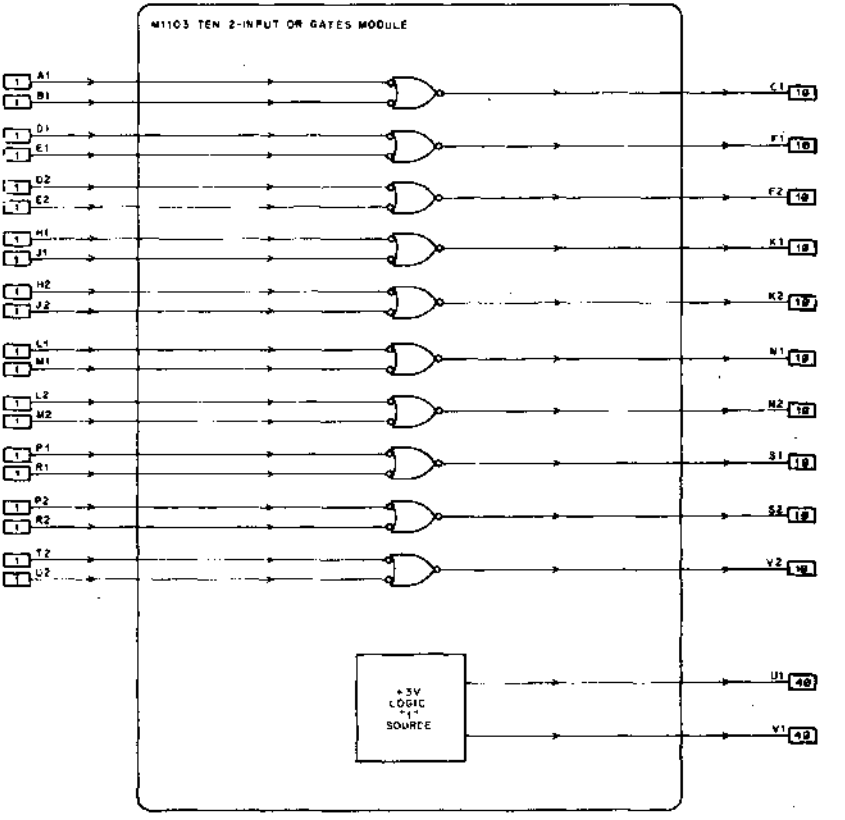
DONE BUS—Provides terminating resistance for the Done Control Bus line and a current source for the open-collector Done Bus Driver. The Done Bus line carries the signal indicating that a data transfer has been completed; i.e., the source has placed data on the Data Bus lines and the destination has received the data. The Done signal is always generated by either the M7304 or the M7332 module, whichever is used.

POWER CLEAR BUS—Provides terminating resistance for the Power Clear Bus line and a current source for the open-collector Power Clear Bus driver. The Power Clear Bus line carries the signal that initializes an RTM system at power on. The Power Clear signal is generated by either the M7304 or the M7332 module, whichever is used.

M1103
TEN 2-INPUT OR GATES

RTM

Length: Standard
Height: Single
Width: Single



Volts	mA (typ)	Pins
+5	80	A2
GND		C2, T1

The M1103 Ten 2-Input OR Gates Module contains ten independent 2-input TTL gates. Each gate performs the OR ($C = A + B$) function; the output is asserted Low when any one or more of its inputs are asserted Low.

Unused inputs on any gate must be tied either to a used input or to a logic High source for maximum noise immunity. Two independent logic High sources are provided on this module.

APPLICATIONS

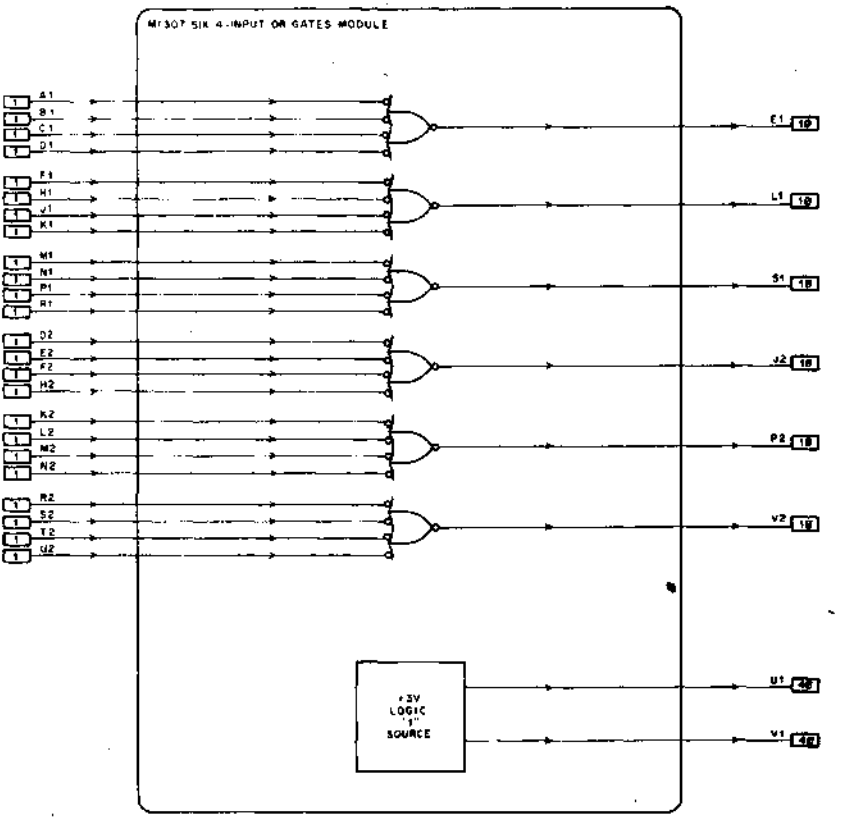
These OR gates can be used to merge Evoke control paths, to expand functional inputs, or as buffers to increase drive capabilities in an RTM system.

These gates can also be used to perform the AND ($C = AB$) function.

M1307
SIX 4-INPUT OR GATES

RTM

Length: Standard
Height: Single
Width: Single



Volts	mA (typ)	Pins
+5	100	A2
GND		C2, T1

The M1307 Six 4-Input OR Gates Module contains six independent 4-input TTL gates. Each gate performs the OR ($E = A+B+C+D$) function; the output is asserted Low when any one or more of its inputs are asserted Low.

Unused inputs on any gate must be tied either to a used input or to a logic High source for maximum noise immunity. Two independent logic High sources are provided on this module.

APPLICATIONS

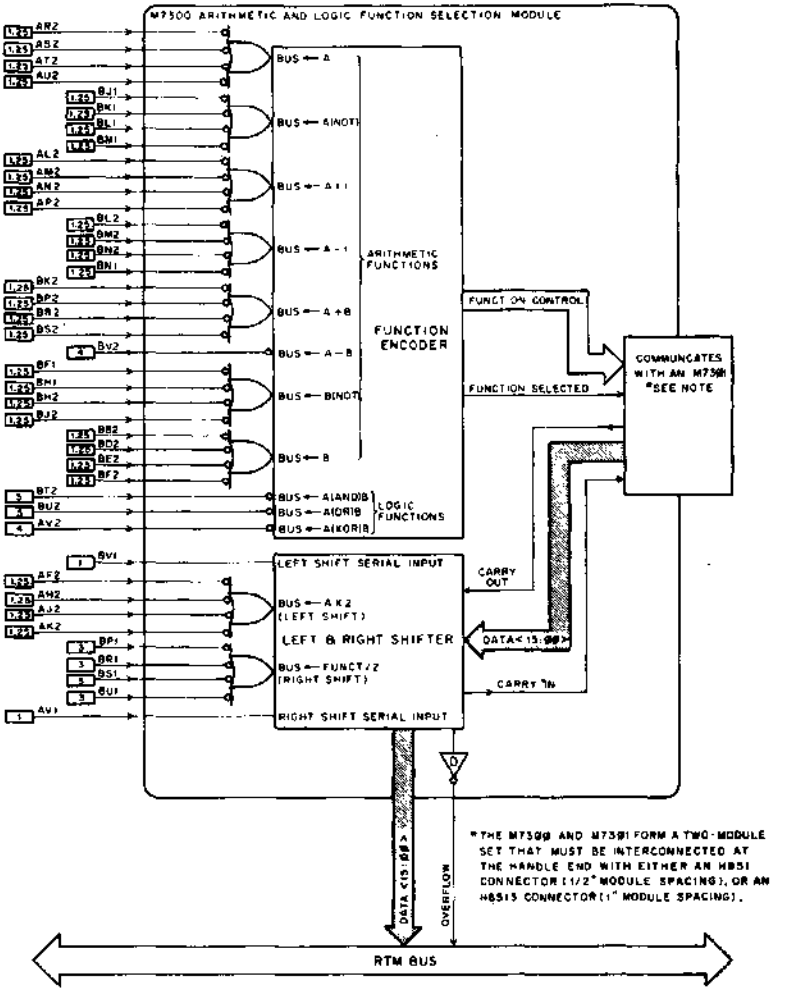
These OR gates can be used to merge Evoke control paths, to expand command inputs, or as buffers to increase drive capabilities in an RTM system.

These gates can also be used to perform the AND ($E = ABCD$) function in systems utilizing positive logic.

M7300
ARITHMETIC AND LOGIC FUNCTION SELECTION MODULE

RTM

Length: Extended
Height: Double
Width: Single

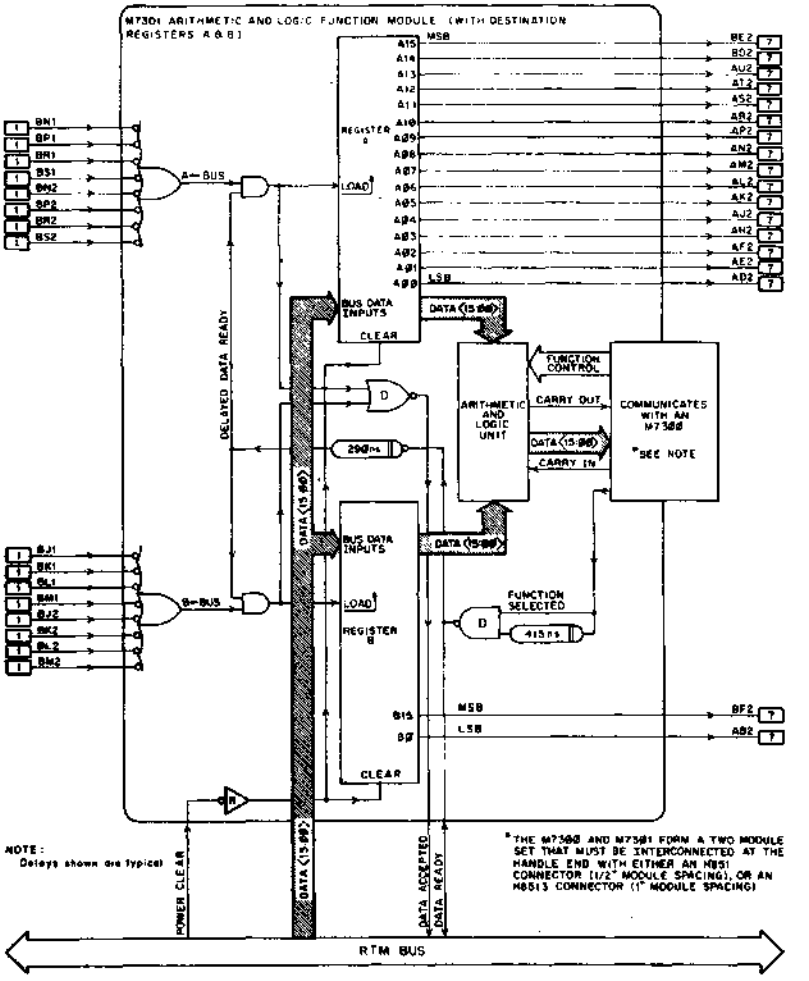


Volts	mA (typ)	Pins
+5	650	AA2, BA2
GND		AC2, BC2, AT1, BT1

M7301
ARITHMETIC AND LOGIC FUNCTION MODULE

RTM

Length: Extended
Height: Double
Width: Single



Volts	mA (typ)	Pins
+5	900	AA2, BA2
GND		AC2, BC2, AT1, BT1

The M7300 Arithmetic and Logic Function Selection Module and the M7301 Arithmetic and Logic Function Module work together to perform arithmetic and logic operations for an RTM system.

The M7301 can accept data from the RTM Bus and place it into either or both of its destination registers. The M7300 can perform operations on the contents of the two registers and place the results on the Bus. The various functional inputs determine what operation(s) will be performed on Registers A and/or B, which serve as the data inputs to the Arithmetic-Logic Unit (ALU) circuitry. Several of the more useful functions of these modules use the same register as both a source and a destination, e.g., A←A+B.

Destination Registers A and B of the M7301 may be loaded from the RTM Bus with the A ← BUS or B ← BUS control inputs, respectively. The ALU receives inputs from Registers A and B. The Function Encoder portion of the M7300 module receives Evoke signals to initiate the arithmetic and logic functions of the ALU. The selected function is coded and communicated to the ALU. Results of operations performed by the ALU are communicated to the Shifter circuit along the data lines DATA<15:00> and via CARRY IN and CARRY OUT signals, and then placed on the RTM (DATA<15:00>) Bus.

The Left and Right Shifter portion of the M7300 module receives Evoke signals to initiate the shifting functions. The left-shift function operates on Register A and shifts the contents of the register one place to the left. This is equivalent to multiplication by two. The right-shift function operates on the results of any one of the other functions. The RIGHT SHIFT, which must be accompanied by a signal for one of the other functions, enables moving the result of the accompanying function one bit to the right (equivalent to dividing by 2). The CARRY IN and CARRY OUT signals indicate when a shift, add, or subtract operation has produced a carry or borrow. The OVERFLOW signal represents the carry of addition, the borrow of subtraction, the MSB after a left shift, or the LSB after a right shift. Because the Overflow Bus is continuously driven by the Overflow circuit, use of more than one M7300/M7301 pair on a single RTM Bus is not recommended.

The Arithmetic and Logic Function Modules are capable of testing the truth of arithmetic conditional statements (A = B, A <B, A> B, A <= B, A> = B, and A ≠ B) or logical statements (A, B, A(NOT), A(AND)B, A(OR)B, A(XOR)B, and A(EQV)B) in a single step. For instance, to determine if A = B, subtract B from A and test the DATA = 0 output of the M7304 Bus Sense Register Module or the M7332 Bus Monitor and Terminator Module.

Inputs
Inputs are organized as Destination Inputs, Source Inputs, and Data Inputs.

Destination **Inputs**
A ← BUS—Register A is loaded from the RTM (DATA<15:00>) Bus.

B ← BUS—Register B is loaded from the RTM (DATA<15:00>) Bus.

Source **Inputs**
BUS ← A—The RTM (DATA<15:00>) Bus gets the contents of Register A.

BUS ← A(NOT)—The RTM (DATA<15:00>) Bus gets the one's complement (all bits inverted) of Register A.

BUS ← A+1—The RTM (DATA<15:00>) Bus gets the contents of Register A incremented by 1.

BUS ← A−1—The RTM (DATA<15:00>) Bus gets the contents of Register A decremented by 1.

BUS ← A+B—The RTM (DATA<15:00>) Bus gets the sum of the contents of Registers A and B.

BUS ← A−B—The RTM (DATA<15:00>) Bus gets the difference between the contents of Registers A and B.

BUS ← B(NOT)—The RTM (DATA<15:00>) Bus gets the one's complement (all bits inverted) of Register B.

BUS ← B—The RTM (DATA<15:00>) Bus gets the contents of Register B.

BUS ← A(AND)B—The RTM (DATA<15:00>) Bus gets the logical AND of Registers A and B.

BUS ← A(OR)B—The RTM (DATA<15:00>) Bus gets the inclusive OR of Registers A and B.

BUS ← A(XOR)B—The RTM (DATA<15:00>) Bus gets the exclusive OR of Registers A and B.

BUS ← AX2—(LEFT SHIFT) The RTM (DATA<15:00>) Bus gets the contents of Register A after all bits have been shifted one place to the left; the MSB is shifted to the OVERFLOW Bus line.

BUS ← FUNCT/2—(RIGHT SHIFT) When this function is used simultaneously with any of the other source functions on this list, the Bus gets the result of that function after all bits have been shifted one place to the right; the LSB is shifted to the OVERFLOW Bus line.

Data Inputs
LEFT-SHIFT SERIAL INPUT—Data is shifted serially into the Shifter via the LSB during a left-shift operation. (Useful for accepting serial data from external devices or flags, or for creating an end-around carry by attaching this input to the MSB of Register A.)

RIGHT-SHIFT SERIAL INPUT—Data is shifted serially into the Shifter via the MSB during a right-shift operation. (Useful for accepting serial data from external devices or flags, or for creating an end-around carry by attaching this input to the LSB of the register that is being shifted.)

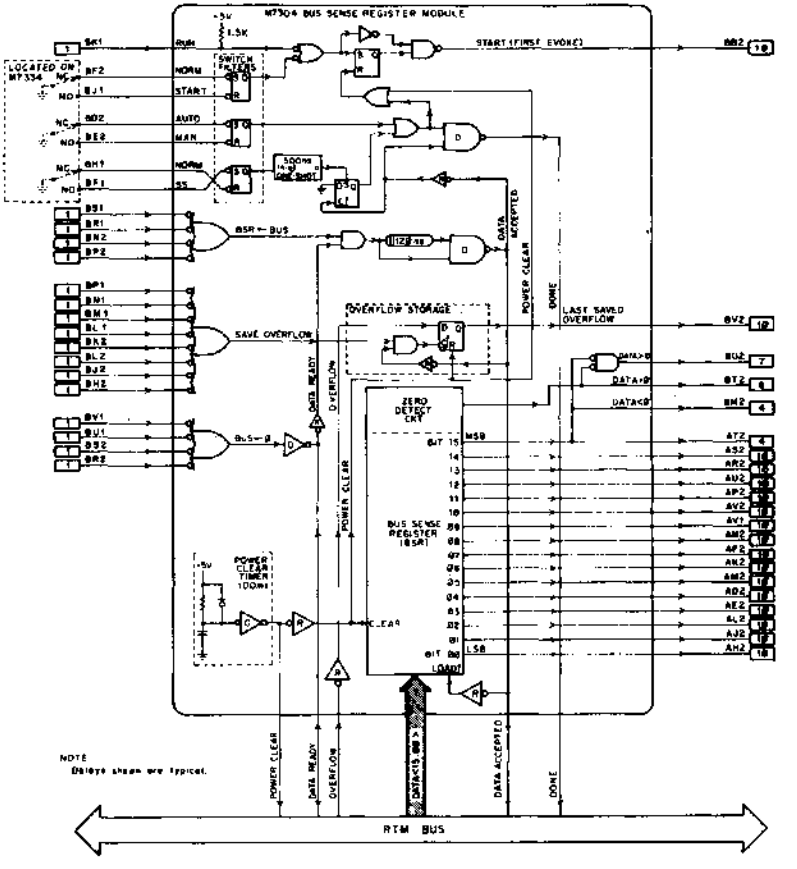
Outputs
A<15:00>, B<15>, and B<0>—These destination register outputs are available as TTL outputs on module pins.

RTM Bus
DATA<15:00>, POWER CLEAR, DATA READY, DATA ACCEPTED, and OVERFLOW are described in the M7332 Bus Monitor and Terminator Module.

M7304
BUS SENSE REGISTER

RTM

Length: Extended
Height: Double
Width: Single



Volts	mA (typ)	Pins
+5	500	AA2, BA2
GND		AC2, BC2, AT1, BT1

The M7304 Bus Sense Register Module contains the circuitry to perform several essential system-level functions that might otherwise have to be included in each RTM module; for example, POWER CLEAR. This module also contains the circuitry that monitors and saves a copy of the data involved in each transfer.

An M962 Bus Terminator Module must always be used in conjunction with the M7304 Module. However, an M7332 Bus Monitor and Terminator Module may be used instead of the M7304/M962 pair and is generally recommended for new designs. An M7304/M962 pair or an M7332 is required in every RTM system to perform system housekeeping functions.

The Bus Sense Register Module can be used as either a source or a destination of data. This module generates the POWER CLEAR signal, which is used to initialize flip-flops and other circuits when power is first applied to the system, and it issues the first EVOKE signal in an evoke-controlled RTM system. It also issues the DONE signal to indicate the completion of each data transfer. This module contains the Bus Sense Register (BSR), which reads the bus each time DATA ACCEPTED appears on the bus. Therefore, the BSR always contains the data that was transferred during the most recent transfer operation between any two registers. The outputs of the BSR are available at the module pins for bit testing or for use as CONDITION inputs to the status signal multiplexer or branch units. Status logic in the Bus Sense Register Module monitors the BSR contents and issues a DATA>0, DATA=0, or DATA<0 signal for each data word that is transferred; each of these signals can be used for CONDITION inputs to branches.

BUS ← 0—The BUS ← 0 functional input is used whenever a source of all binary zeros is desired. DATA READY is issued immediately.

BSR ← BUS—The BSR ← BUS functional input is used to generate a DATA ACCEPTED so that the BSR will be the only destination of a transfer.

SAVE OVERFLOW—The SAVE OVERFLOW functional input is used to load the logic state of the Overflow Bus line into a flip-flop. The overflow operation is used in conjunction with a data transfer between the M7300 and M7301 modules and a destination register to save the overflow bit that resulted from an arithmetic or logic function operation.

RUN—This input allows a TTL level signal to be used to start an RTM system. This input can be from a remote external switch (if debounced) or remote external logic. The RUN signal must be a Low-going pulse at least 100 ns long. The first evoke will be issued on the trailing edge of this pulse.

The M7304 contains three switch filters that allow external switches to be added for manual control of an RTM system. Any single-pole, double-throw switch may be used when connected as shown on the functional diagram. The M7334 Switch and Light Module contains extra switches that may be used for this purpose.

NORM/START—This switch input provides for manually starting an RTM system.

AUTO/MAN—This switch input is especially useful during troubleshooting; it is used in conjunction with the NORM/SS switch input to provide single-stepping capability. With this switch in AUTO, the system will execute the program in the normal manner. With this switch in MAN, the system will halt after executing each instruction.

NORM/SS—This switch input is used in conjunction with the AUTO/MAN switch when that switch is in the MAN position. Each time this switch is moved from NORM to SS then to NORM, one program instruction will be executed and the system will halt.

DATA = 0—A High at this output indicates that the contents of the BSR are equal to zero.

DATA > 0—A High at this output indicates that the contents of the BSR are greater than zero (positive). This assumes that the data is in two's complement form.

DATA < 0—A High at this output indicates that the contents of the BSR are less than zero (negative). This assumes that the data is in two's complement form.

LAST SAVED OVERFLOW—Gives the contents of the Overflow flip-flop.

START (FIRST EVOKE)—The START signal for the PCS module controlled systems or the first EVOKE signal for an evoke module controlled system. This signal goes Low when the START switch is pressed and released, then goes High when DONE is received.

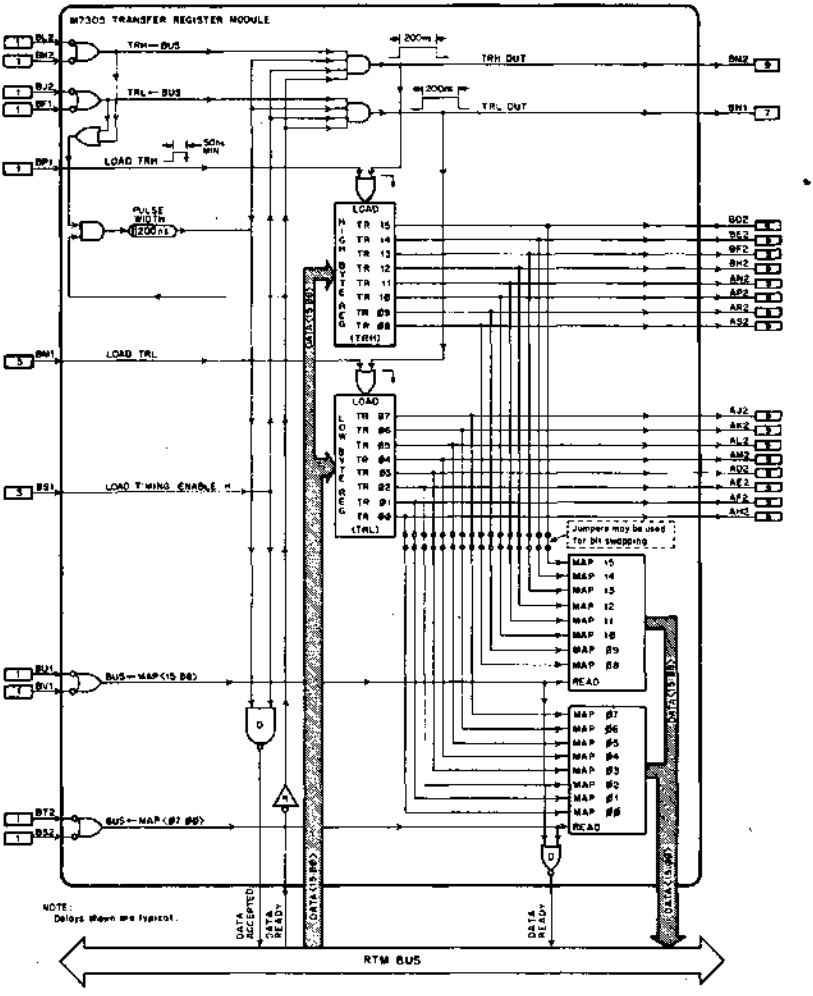
BIT 00 through BIT 15—The contents of the BSR, available at module pins.

POWER CLEAR—This RTM Bus signal is asserted for approximately 100 ms when dc power is first applied to the RTM system.

M7305
TRANSFER REGISTER MODULE

RTM

Length: Extended
Height: Double
Width: Single



Volts	mA (typ)	Pins
+5	400	AA2, BA2
GND		AC2, BC2, AT1, BT1

The M7305 Transfer Register Module is a 16-bit storage register that is both byte and word addressable. The storage register (TRL and TRH) is divided into lower and upper bytes which can be loaded from or read onto the RTM Data Bus either separately (8 bits) or together (16 bits). When data (DATA <15:00>) is loaded into TRL and/or TRH from the RTM Bus, that data (TR<00:07> and/or TR<08:15>) is available at module contact fingers for interfacing or other uses. For example, individual bit outputs from the high-byte and low-byte registers can be used to control CONDITION inputs on other modules, such as branch units and multiplexers.

Jumpers on the module permit bit-swapping when data (DATA<15:00>) is read onto the RTM Bus. Refer to SPECIAL WIRING AND ADJUSTMENTS.

The M7305 contains circuitry for preventing the assertion of DATA ACCEPTED so that two or more transfer registers can be evoked for simultaneous loading. Refer to LOAD TIMING ENABLE signal description. In addition, output signals that correspond to the combination of an Evoke input and the DATA READY signal are available. Refer to TRH OUT and TRL OUT signal descriptions. These outputs allow one or more M7305 modules to be operated as slaves to a single master for simultaneous loading. This feature makes it possible to load several registers simultaneously or each individually.

Inputs

TRH ← BUS—When this input is evoked and when LOAD TIMING ENABLE is High, the high-byte register (TRH) is loaded with parallel data (DATA<15:08>) from the RTM Bus 200 ns (typical) after DATA READY is asserted; 50 ns (typical) after TRH ← BUS is unasserted, TRH OUT and DATA ACCEPTED are asserted.

TRL ← BUS—When this input is evoked and when LOAD TIMING ENABLE is High, the low-byte register (TRL) is loaded with parallel data (DATA <07:00>) from the RTM Bus 200 ns (typical) after DATA READY is asserted; 50 ns (typical) after TRL ← BUS is unasserted, TRL OUT and DATA ACCEPTED are asserted.

Inputs TRH ← BUS and TRL ← BUS may be asserted at the same time, loading the data (DATA<15:00>) on the RTM Bus simultaneously into the high-byte and low-byte registers of the M7305 module.

LOAD TRH—This input is usually used to load the TRH register with parallel data (DATA<15:08>) from the RTM Bus when this M7305 module is in its slave mode (LOAD TIMING ENABLE Low) because DATA ACCEPTED is not asserted. The LOAD TRH input is usually asserted by either the TRH OUT or TRL OUT output of another M7305. To load the register, bring the LOAD TRH line High for at least 50 ns and then Low again. The outputs of the register will follow the inputs as long as the LOAD TRH line is High.

NOTE

LOAD TRH input must be grounded if not used.

LOAD TRL—This input is usually used to load the TRL register with parallel data (DATA<07:00>) from the RTM Bus when this M7305 module is in slave mode (LOAD TIMING ENABLE Low) because DATA ACCEPTED is not asserted. The LOAD TRL input is usually asserted by either the TRH OUT or TRL OUT output of another M7305. To load the register, bring the LOAD TRL line High for at least 50 ns and then Low again. The outputs of the register will follow the inputs as long as the LOAD TRL line is High.

NOTE

LOAD TRL input must be grounded if not used.

LOAD TIMING ENABLE—When High, this input enables the load timing circuit and the DATA ACCEPTED Bus signal circuit. When Low, it disables these circuits so that TRH OUT, TRL OUT, and DATA ACCEPTED are all inhibited.

BUS ← MAP<15:08>—When this input is evoked, the output bits of the storage register that are jumpered to MAP<15:08> are driven to the RTM Bus, and then DATA READY is asserted.

BUS ←MAP<07:00>—When this input is evoked, the output bits of the storage register that are jumpered to MAP<07:00> are driven to the RTM Bus, and then DATA READY is asserted.

Outputs

TRH OUT—This output goes High only when the TRH ← BUS input is evoked and LOAD TIMING ENABLE is High, and DATA READY is received. It is intended to drive the LOAD TRH or LOAD TRL inputs of slaved M7305 modules.

TRL OUT—This output goes High only when the TRL ← BUS input is evoked and LOAD TIMING ENABLE is High, and DATA READY is received. It is intended to drive the LOAD TRH or LOAD TRL inputs of slaved M7305 modules.

TR<15:00>—These are the 16 data output lines from the TRH (TR<15:08>) and TRL (TR<07:00>) registers that make the contents of each byte register continuously available at module pins until the next Evoke signal is issued to that byte register. These output lines are not subject to bit-swapping.

RTM Bus

DATA<15:00>, DATA READY, and DATA ACCEPTED are described in the M7332 Bus Monitor and Terminator Module description.

SPECIAL WIRING

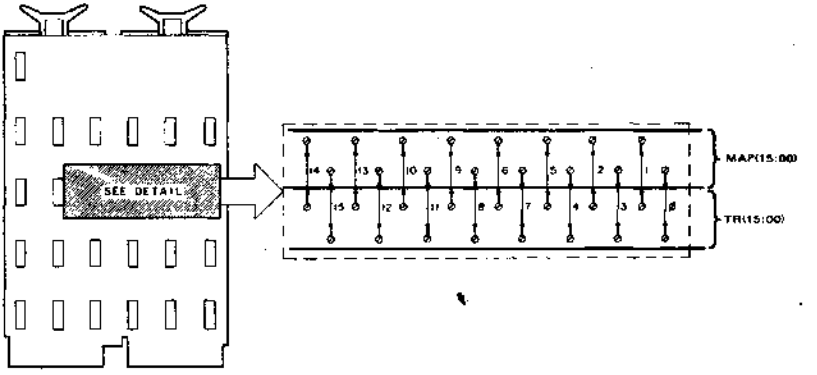
WARNING

Extreme care should be exercised when removing jumpers from the module to avoid lifting or otherwise damaging the printed circuit etching. Clip both ends of the jumper as close as practical to the solder pads and remove the jumper from the module.

NOTE

Split lugs are not positioned in exact numerical order on the module. See the detail drawing of M7305 jumpers.

The jumpers on the M7305 module permit bit-swapping between the Transfer Register and the RTM Data Bus. By clipping the factory-installed jumper wires and connecting jumpers from split lugs in the bottom row (the output of TR<15:00>) to other split lugs in the top row (the input of MAP<15:00>), bits can be swapped either within or between byte registers.

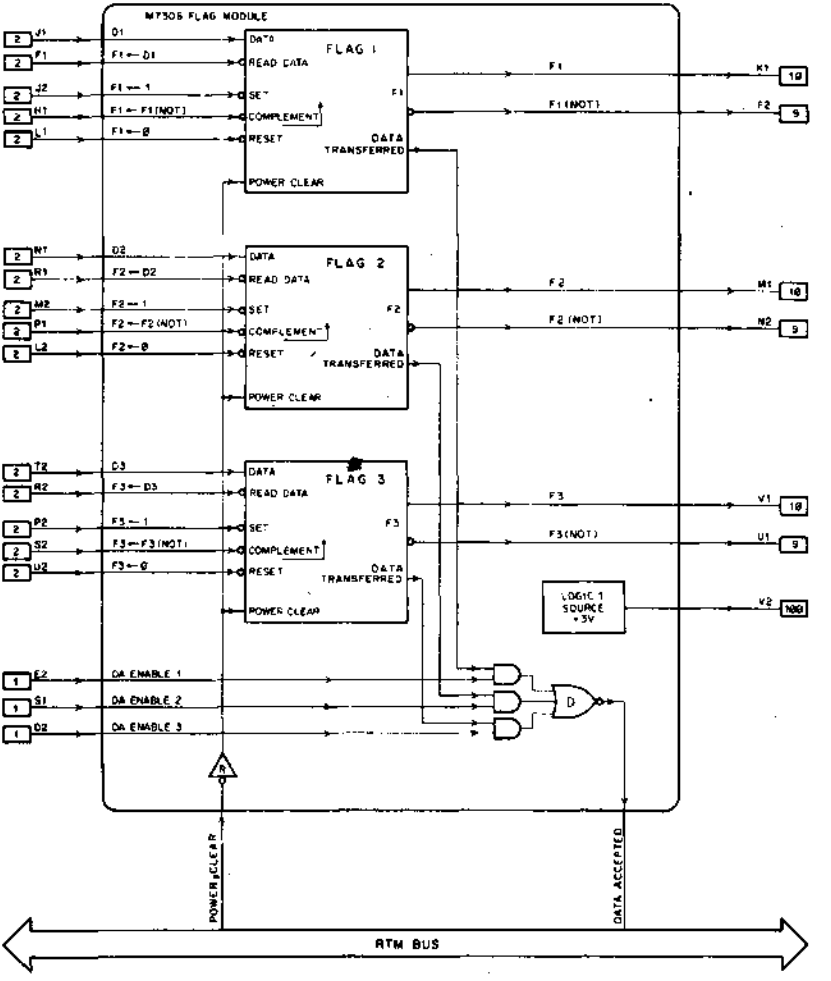


Detail Drawing of M7305 Jumper

M7306
FLAG MODULE

RTM

Length: Extended
Height: Single
Width: Single



Volts	mA (typ)	Pins
+5	160	A2
GND		C2, T1

The M7306 Flag Module is a general purpose flip-flop module containing three flags. Each flag can be set, reset, loaded, or complemented by a High-to-Low signal at the appropriate functional input. The flags perform like RS-type flip-flops when set or reset, like latch-type flip-flops when complemented.

Each flag has the ability to issue DATA ACCEPTED, so that flag functions may be evoked. The DATA ACCEPTED output is controlled by a DA ENABLE input for each flag. When DA ENABLE is High, the assertion of any functional input (F ← D, F ← 1, F ← F(NOT), or F ← 0) will cause DATA ACCEPTED to be issued. When DA ENABLE is Low, DATA ACCEPTED will not be issued. After one of its functional inputs has been asserted, a flag may be used to cause an RTM system to wait for the completion of some event by making the assertion of its DA ENABLE control input contingent upon completion of the event.

Another possible use for a flag is to provide the necessary DATA ACCEPTED signal for a non-RTM register that is being used as the destination in an Evoked operation.

All of the functional input signals are asserted Low, making the flags compatible with the operation of Evoke circuits.

Because the input and output signals of the three flags on this module perform the same function, only Flag 1 inputs and outputs are described.

Inputs

D1—This is the data input line when Flag 1 is used as a latch-type flip-flop. Because this input is not Bus compatible, it should not be connected to a Bus line.

F1 ← D1—When this input is evoked, it causes D1 to be read into Flag 1. The state of Flag 1 will follow the D1 input until this signal goes High. Assertion of F1 ← D1 also asserts DATA TRANSFERRED, which will produce DATA ACCEPTED if DA ENABLE 1 is High.

F1 ← 1—This is the direct Set input. When this input is evoked, the F1 output will go High. Assertion of F1 ← 1 also asserts DATA TRANSFERRED, which will produce DATA ACCEPTED if DA ENABLE 1 is High.

F1 ← F1(NOT)—When this input goes from High to Low, the state of Flag 1 will complement. Assertion of F1 ← F1(NOT) also asserts DATA TRANSFERRED, which will produce DATA ACCEPTED if DA ENABLE 1 is High.

F1 ← 0—This is the direct Reset input. When it is evoked, the Flag 1 output will go Low. Assertion of F1 ← 0 also asserts DATA TRANSFERRED, which will produce DATA ACCEPTED if DA ENABLE 1 is High.

DA ENABLE 1—This input determines whether or not DATA ACCEPTED will be asserted when any of the Flag 1 functional inputs is asserted. It may be tied High, tied Low, or tied to a control signal. This line should NOT be left unconnected.

Outputs

F1—This output is High when Flag 1 is set, and Low when it is reset.

F1(NOT)—This output is the complement of F1.

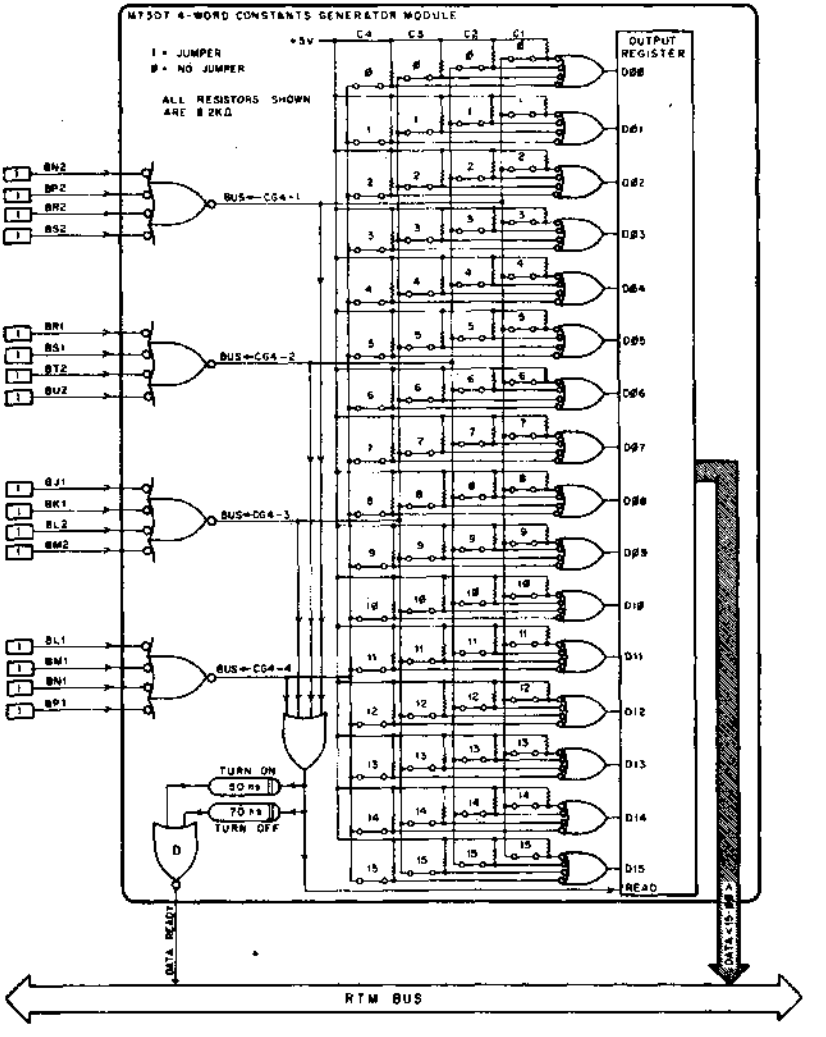
RTM Bus

POWER CLEAR and DATA ACCEPTED are described in the M7332 Bus Monitor and Terminator Module description.

M7307
FOUR-WORD CONSTANTS GENERATOR

RTM

Length: Extended
Height: Double
Width: Single



Volts	mA (typ)	Pins
+5	160	AA2, BA2
GND		AC2, BC2, AT1, BT1

The M7307 4-Word Constants Generator Module provides a convenient way to introduce, into an RTM system, up to four user-defined, hard-wired, 16-bit data word constants. The words are encoded on the module by the user with wire jumpers. Whether a jumper associated with each bit of a constant is installed or removed determines the data bit format that will be obtained when that particular constant is required.

Constants generators can be used wherever there is a need for a numeric, character code, or data mask code constant.

Inputs

BUS ← CG4-#—(Where # represents the number of one of the four data word constants.) When this input is evoked, it causes word # to be driven onto the RTM (DATA<15:00>) Bus. DATA READY is asserted 50 ns (typical) after this input is evoked, and unasserted 70 ns (typical) after the Evoke has been removed.

RTM Bus

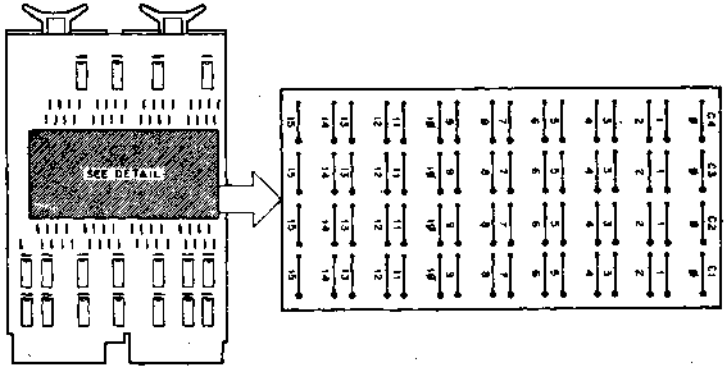
DATA<15:00> and DATA READY are described in the M7332 Bus Monitor and Terminator Module description.

SPECIAL WIRING AND ADJUSTMENTS

WARNING

Extreme care should be exercised when removing jumpers from the module to avoid lifting or otherwise damaging the printed circuit etching. Clip both ends of the jumper as close as practical to the solder pads and remove the jumper from the module.

There are 16 jumpers on the M7307 module associated with each data word. When these factory-installed jumpers remain installed, a binary One is produced at the RTM Data Bus for the associated data bit of that data word. All data bits that are required to be binary Zeros at the RTM Data Bus must have their associated jumpers clipped. See the detail drawing of M7307 jumpers.

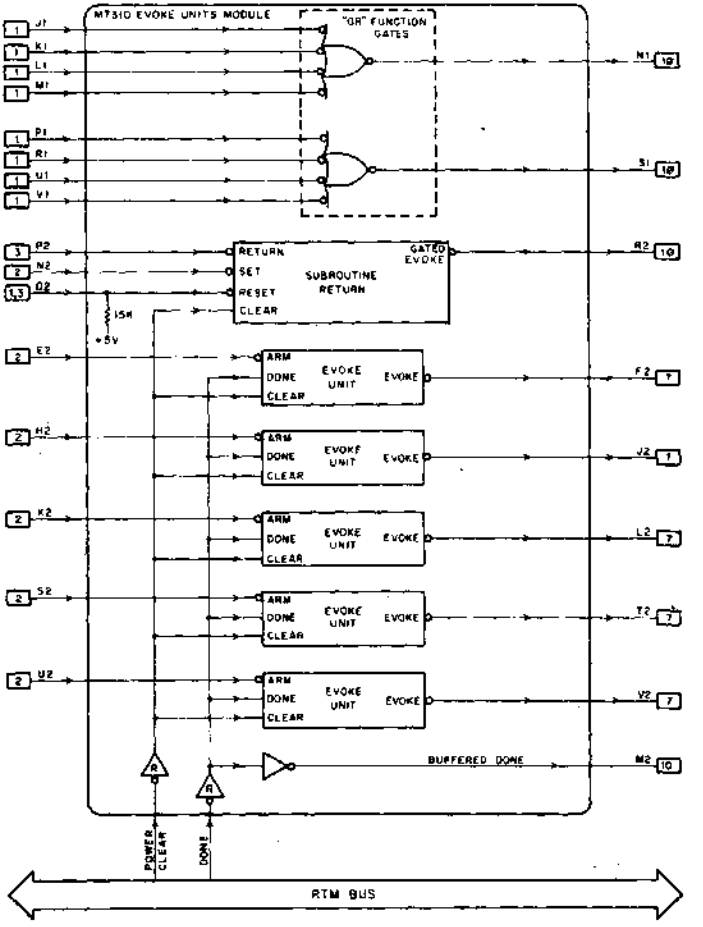


Detail Drawing of M7307 Jumpers

M7310
EVOKE UNITS MODULE

RTM

Length: Extended
Height: Single
Width: Single



Volts	mA (typ)	Pins
+5	150	A2
GND		C2, T1

The M7310 Evoke Units Module is the basic control module in a hard-wired RTM system. Its function is to evoke single register transfer operations in the functional module portion of the system (e.g., B←A, A←A+B). It may also simultaneously evoke an operation that does not require the Bus, such as setting, complementing, or clearing a flag.

Each M7310 module contains five evoke units, one subroutine return unit, and two independent 4-input TTL OR gates.

Evoke Units
An evoke unit is used to cause register transfer operations by means of Evoke signals. The first Evoke signal, which is usually issued by the Bus control module (M7332 Bus Monitor and Terminator Module or M7304 Bus Sense Register Module, and each subsequent Evoke signal serve to evoke a data transfer and also to arm the evoke unit that follows, thus determining the sequence of operations.

The Evoke signal causes the selected source register to perform its function and place its data on the Bus, and then to issue DATA READY, meanwhile also serving as the ARM input for the succeeding evoke unit. The combination of EVOKE and DATA READY causes the selected destination register to read the data from the Bus, issue DATA ACCEPTED, and perform its function. When the M7332 Bus Monitor (or Bus Sense) module receives DATA ACCEPTED, it issues DONE, causing the evoke unit that issued the EVOKE to remove it. This, in turn, unasserts DATA READY and DATA ACCEPTED, thus unasserting DONE. There can be no Evoke signal output from any evoke unit while DONE is present. The unassertion of DONE causes the next armed evoke unit to issue an Evoke signal.

Subroutine Return Unit
The subroutine return unit serves to mark the location in the main program where control is to be returned following the execution of a subroutine. One subroutine return unit is required for each place in a program where the control flow is directed to a subroutine. The return is accomplished by directing the last Evoke signal of the subroutine back to all of the return units, only one of which will gate that Evoke signal through to the main program because only one will be set. In addition to the one on this module, there are six such subroutine return units on the M7315 Hex Subroutine Return Module.

OR Gates
The input lines of the two 4-input TTL OR gates perform an OR($\overline{E} = \overline{A} + \overline{B} + \overline{C} + \overline{D}$)function, and can be used to merge Evoke control paths or as buffer amplifiers.

Inputs
RETURN—The signal at this input of the subroutine return unit is gated to the GATED EVOKE output if the internal flip-flop of the subroutine return unit is set.

SET—This input sets the internal flip-flop of the subroutine return unit; it is usually driven by the same Evoke signal that initiates the subroutine.

RESET—This input resets the internal flip-flop of the subroutine return unit. This input is not used during normal RTM System operation.

ARM—This input arms the internal flip-flop of the evoke unit; it is driven by the prior Evoke signal.

Outputs

GATED EVOKE—If the internal flip-flop of the subroutine return unit is set, the signal at the RETURN input is gated to this output. If the flip-flop is reset, this output remains High.

EVOKE—This output is the EVOKE signal that initiates source-destination transfers. It also arms the succeeding evoke unit.

BUFFERED DONE—This output is the buffered image of the DONE Bus signal.

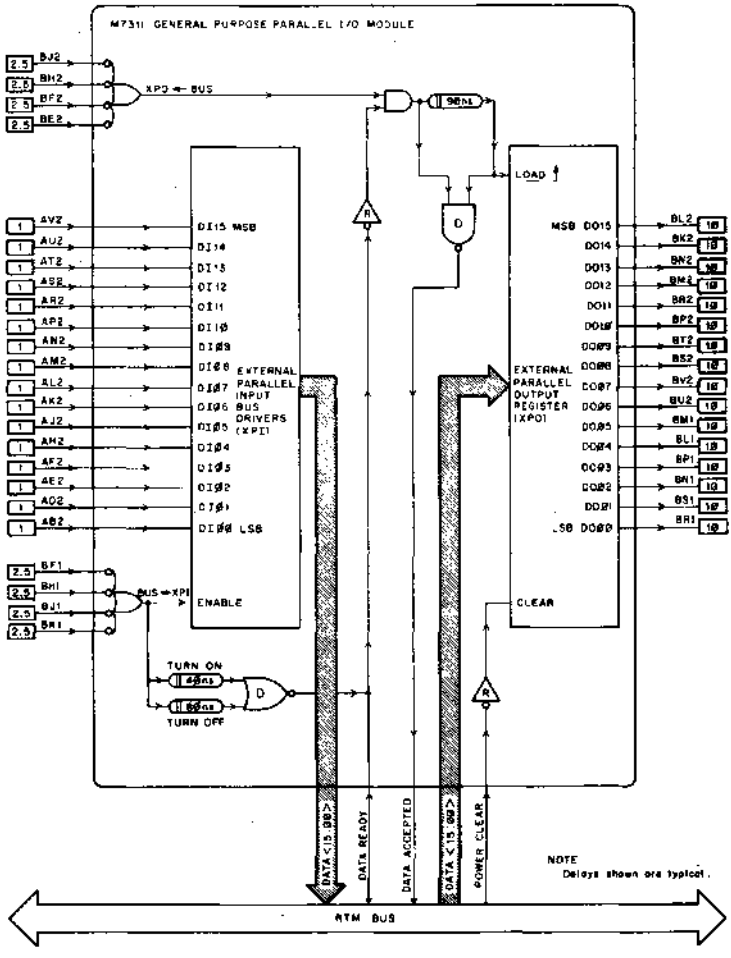
RTM Bus

POWER CLEAR and DONE are described in the M7332 Bus Monitor and Terminator Module description.

M7311
GENERAL PURPOSE PARALLEL I/O

RTM

Length: Extended
Height: Double
Width: Single



Volts	mA (typ)	Pins
+5	400	AA2, BA2
GND		AC2, BC2, AT1, BT1

The M7311 General Purpose Parallel Input/Output Module provides for bi-directional parallel data transfer between the RTM (DATA<15:00>)Bus and external equipment. It contains two functionally separate sections: an input interface section and an output interface section.

The input section contains bus drivers, which drive a 16-bit data word (DI<15:00>) from an external source device to the RTM Data Bus when the External Parallel Input (BUS ← XPI) is evoked.

The output section contains bus receivers and a 16-bit storage register. The bus receivers accept a 16-bit data word (DATA<15:00>) from the RTM Data Bus. When the External Parallel Output (XPO ← BUS) is evoked, the storage register is loaded with the data word (DO<15:00>), making the data word available to an external device. The external device can be informed that data is available from the XPO register by using the Evoke signal for the next data transfer to also set one of the flag circuits of an M7306 Flag Module. The data remains stored in the register until the next Evoke signal is addressed to the register. The two sections of this module operate independently of each other.

Inputs

BUS ← XPI—When the BUS ← XPI is evoked, the XPI bus drivers are enabled and parallel data from an external source is placed on the RTM (DATA <15:00>) Bus lines; then, after a 40 ns (typical) delay DATA READY is asserted.

XPO ← BUS—When the XPO ← BUS input is evoked, the XPO register is loaded with parallel data from the RTM (DATA<15:00>) Bus 90 ns (typical) after DATA READY is asserted. XPO ← BUS and the received DATA READY also cause DATA ACCEPTED to be asserted Low.

DI<15:00>—These are the 16 data input lines to the XPI bus drivers that accept parallel data from an external data source when the BUS ← XPI input is evoked. Data on the input lines must not be changed while being driven onto the Bus. Unused input lines, if left unconnected, will tend to read in as Ones.

Outputs

DO<15:00>—These are the 16 data output lines from the XPO register that make the contents of that register continuously available to the external destination device until the next Evoke signal is issued to the register.

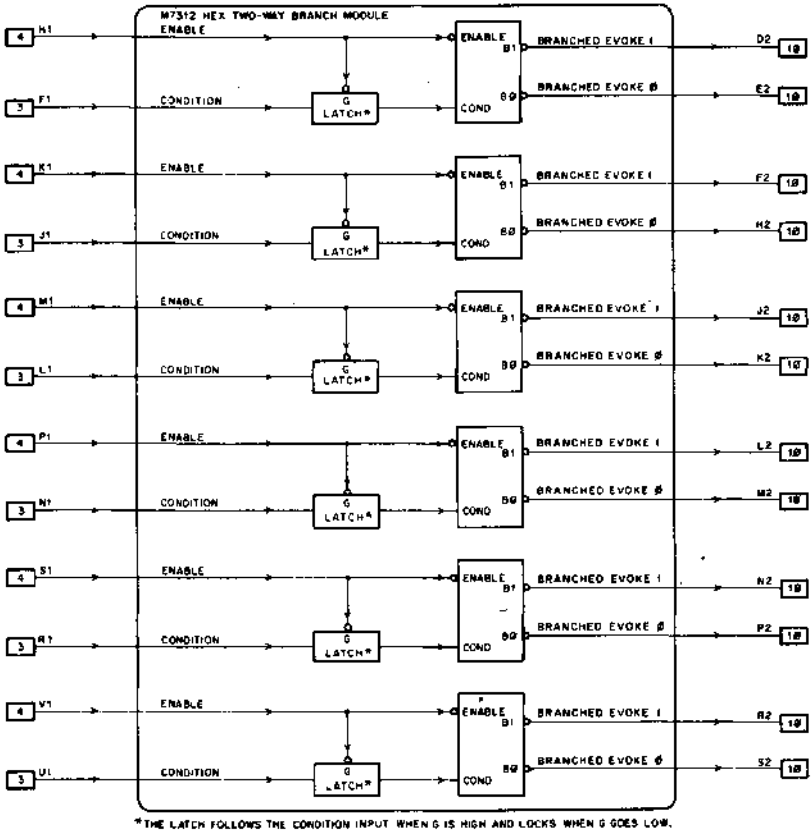
RTM Bus

DATA<15:00>, POWER CLEAR, DATA READY, and DATA ACCEPTED are described in the M7332 Bus Monitor and Terminator Module description.

M7312
HEX TWO-WAY BRANCHES

RTM

Length: Extended
Height: Single
Width: Single



Volts	mA (typ)	Pins
+5	100	A2
GND		C2, T1

The M7312 Hex Two-Way Branch Module contains six two-way branch units that are used in a hard-wired (M7310 Evoke Module controlled) RTM system to branch the control flow to one of two possible directions. Each branch unit operates independent of the other branch units on the module.

Any number or combination of branch units (two-way or eight-way) may be combined to produce any desired degree of branching capability. For example, a 10-way branch may be created by cascading a pair of two-way branch units with an eight-way branch unit (M7314).

Each branch unit on the M7312 module has two input lines, a latch circuit, a decoder, and two output lines. The latch circuit output follows the CONDITION input as long as its G input (ENABLE) remains High. The ENABLE input is usually asserted by an Evoke signal. When ENABLE is asserted (Low), the latch circuit stores the current CONDITION input status so that subsequent changes will not affect the output of the branch unit during the current ENABLE signal. Either the BRANCHED EVOKE 0 or BRANCHED EVOKE 1 output will be asserted whenever the ENABLE input is asserted. The CONDITION input monitors a logic signal, usually a flag output or a register output bit.

Inputs

ENABLE—When this input is evoked, the CONDITION input is decoded and one of the BRANCHED EVOKE outputs is asserted Low. It is also the G input to the latch circuit.

CONDITION—The logic level of this input determines which BRANCHED EVOKE output will be asserted Low when ENABLE is asserted Low. If the CONDITION input is Low, BRANCHED EVOKE 0 will be asserted; if CONDITION is High, BRANCHED EVOKE 1 will be asserted.

Outputs

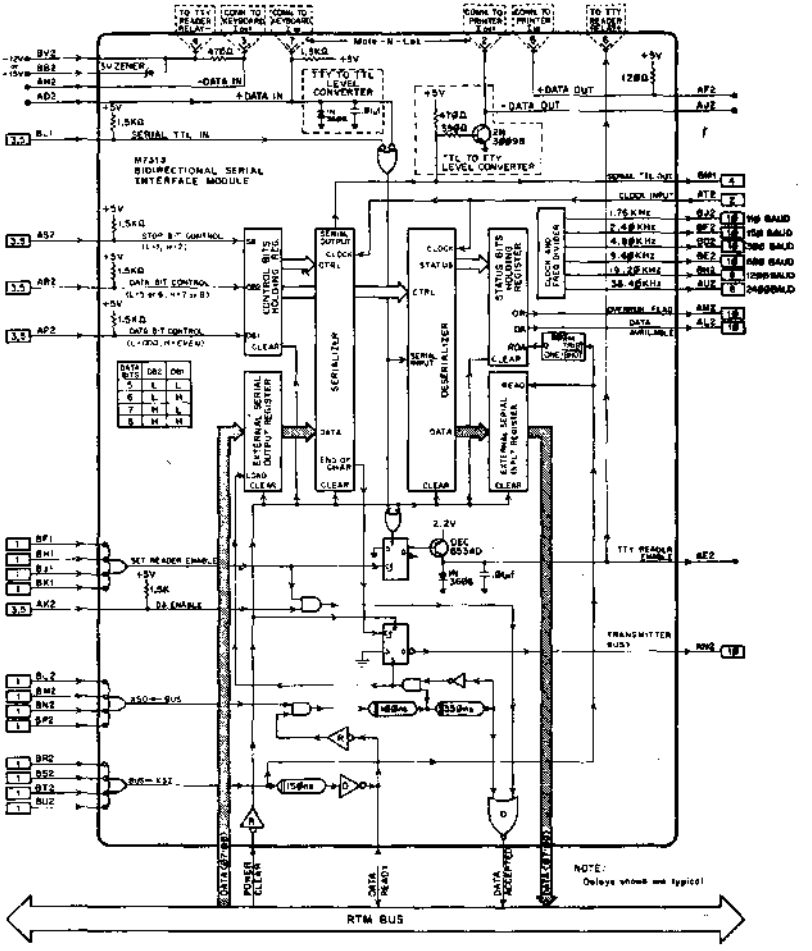
BRANCHED EVOKE 0—This output is asserted Low when CONDITION is Low and ENABLE is asserted Low.

BRANCHED EVOKE 1—This output is asserted Low when CONDITION is High and ENABLE is asserted Low.

M7313
BIDIRECTIONAL SERIAL INTERFACE

RTM

Length: Extended
Height: Double
Width: Single



Volts	mA (typ)	Pins
+5	700	AA2, BA2
−15	80	BB2
GND		AC2, BC2, AT1, BT1

The M7313 Bidirectional Serial Interface Module provides an asynchronous serial transceiver interface for use with data communications equipment. Baud rates of 110, 150, 300, 600, 1200, or 2400 are available when using an internal clock signal. Other baud rates may be obtained by supplying an external clock. The maximum baud rate is 40,000. Inputs provide for selection of from five to eight bits per character and for selection of either one or two stop bits.

The M7313 module can be used only as an active device; i.e., it can transmit and receive a serial line by supplying a current source to a passive external device. The M7313 module cannot be used as a passive device.

The M7313 contains input/output level converters and parallel-to-serial and serial-to-parallel converters for transmitting and receiving asynchronous serial data. The serial input and output may be either a 20 mA current loop or a TTL level signal. The M7313 also contains a 6 pin Mate-N-Lok connector for easy interfacing with a serial device.

All characters received and transmitted serially by this module must contain a start bit, five to eight data bits, and one or two stop bits. The M7313 module accepts parallel data from the RTM (DATA<07:00>) Bus lines, serializes the data, formats it by appending start and stop bits, and transmits this data word serially to an external passive asynchronous serial receiver such as a Teletype, line printer, computer terminal, or serial computer interface.

The M7313 module accepts serial data from an external passive device and places the parallel data word (DATA<07:00>) on the RTM Bus.

The M7313 module can transmit and receive simultaneously or it can transmit or receive independently.

Transmit Function

A character transmission is initiated by evoking the XSO ← BUS input. 100 ns after DATA READY is asserted, data is loaded into the XSO register by a 350 ns pulse at the LOAD input. Data is transferred to the serializer for serialization at the end of the LOAD pulse (Figure 1). The appropriate start and stop bits are appended to the data, and the bits thus assembled are transmitted serially by bit, LSB first, at a rate determined by the baud rate selected. The characters are in the format shown in Figure 1. TRANSMITTER BUSY is asserted Low at the start of transmission (start of transmission is defined as MARK-to-SPACE transition of start bit) and is unasserted when a full character (including stop bit or bits) has been transmitted and remains in the High state until start of transmission of the next character. TRANSMITTER BUSY is unasserted (High) to signal that new data may be loaded into the M7313. TRANSMITTER BUSY must be monitored to prevent loss of data due to a load sequence occurring while TRANSMITTER BUSY is Low (prior to generation of internal END OF CHAR signal). (Figure 1.) The TRANSMITTER BUSY signal can be monitored with an evoke sequence that samples the TRANSMITTER BUSY line prior to loading the serial data and loops back to a previous step if TRANSMITTER BUSY is Low. Or, an M7306 flag unit function may be evoked prior to loading the serial data. If the TRANSMITTER BUSY signal is connected to the DA ENABLE input of the flag, the flag will not issue DATA ACCEPTED and complete the EVOKE cycle until the TRANSMITTER BUSY signal goes High. Serial data may be transmitted by either TTL or current loop type signals, or by both simultaneously. DATA ACCEPTED is generated 450 ns (typical) after DATA READY is received.

Receive Function

The M7313 Deserializer can accept a TTL signal or a current loop signal, but only one at a time because the inputs for these two types of signals are ORed. The M7313 asynchronously receives and assembles, serial-by-bit characters. The number of data bits and stop bits in the received character must be the same as the user has selected; i.e., connected to format control inputs (DB1, DB2, and SB). The baud rate must be the same as the user has selected. A character begins to be assembled when a start bit is recognized. This is always a transition from a marking condition to a spacing condition. A start bit has a duration equal to one full data bit. When a transition is detected and the bit is recognized as a start bit, character assembly begins. When the full character is assembled, it is transferred to the XSI register and DATA AVAILABLE is asserted High. The XSI register should then be read (transferred to a destination via the RTM Data Bus lines). The DATA AVAILABLE signal should be monitored so that each received word can be removed from the input register before the next serial word is fully assembled and is transferred to the XSI register. Data that is still in the XSI register when another serial word is received will be lost. The M7313 will indicate when such a situation has occurred by asserting the OVERRUN FLAG High. When the BUS ← XSI input is evoked, the character (DATA<07:00>) in the XSI register is placed on the RTM Bus; after a 150 ns (typical) delay, DATA READY is asserted Low. (Figure 2.) OVERRUN FLAG High indicates that the previously received character was not read before the present character was transferred to the M7313 Input register.

Inputs

BUS ← XSI—When the BUS ← XSI input is evoked, data (DATA<07:00>) in the External Serial Input register is placed on the RTM Bus; DATA READY is asserted Low after a 150 ns (typical) delay.

XSO ← BUS—When the XSO ← BUS input is evoked, data (DATA<07:00>) is loaded into the External Serial Output register from the RTM Bus 100 ns (typical) after DATA READY is received. BUS ← XSO and DATA READY cause DATA ACCEPTED to be issued. TRANSMITTER BUSY will also be asserted Low; END OF CHAR (an internally generated signal) causes TRANSMITTER BUSY to be unasserted.

DA ENABLE—Refer to the SET READER ENABLE explanation.

SET READER ENABLE—When the SET READER ENABLE input is evoked, the paper tape reader of a Teletype is enabled (current flows and a relay at the Teletype energizes) for one character either via TTY READER ENABLE OR TTY READER RELAY+. When SET READER ENABLE input is evoked, DATA ACCEPTED will be generated if DA ENABLE input is High. The DA ENABLE input is pulled High internally and may be left unconnected if DATA ACCEPTED is desired. DATA ACCEPTED may be inhibited by grounding the DA ENABLE input.

SERIAL TTL IN—This input accepts a TTL-level serial input signal bit stream for input to the Serializer. Low is a MARK or a One; High is a SPACE or a ZERO.

+DATA IN and —DATA IN—These are the two current-sensing serial data input lines. When more than 3 mA current is flowing, the input is MARKING; when less than 3 mA current is flowing, the input is SPACING. It should be noted that —DATA IN is more negative than +DATA IN; —DATA IN does not indicate reference to ground.

STOP BIT CONTROL—A High input causes two stop bits to be appended to the transmitted serial character; a Low input causes one stop bit to be appended to the transmitted serial character. Two stop bits are usually used when the transmit/receive rate is 110 baud; one stop bit is usually used with rates above 110 baud.

DATA BIT CONTROL DB1 and DB2—These inputs are used to select the number of data bits, from five to eight, that the serial characters will contain in addition to the start and stop bits. The number of data bits will be either five or six if DB2 is Low and will be seven or eight if DB2 is High; the number of data bits will be odd if DB1 is Low and will be even if DB1 is High.

CLOCK INPUT—This input accepts the clock signal input to the M7313 circuitry. This input is usually wired to an output of the Clock and Frequency Divider. The clock rate is 16 times the transmit/receive baud rate; e.g., if the 1.76 kHz clock rate is connected to the CLOCK INPUT, the transmit/receive rate will be 110 baud. If an external clock signal is used, it must be TTL-compatible, a square wave, and 16 times the desired baud rate.

Outputs

SERIAL TTL OUT—This TTL-compatible output provides, serially, by bit, the entire transmitted character. This signal remains High when no data is being transmitted. High is a MARK or a One; Low is a SPACE or a Zero.

+DATA OUT and −DATA OUT—These are the two current-sensing serial data output lines. When more than 3 mA of current is flowing, the output is MARKING; when less than 3 mA of current is flowing, the output is SPACING. It should be noted that −DATA OUT is more negative than +DATA OUT; −DATA OUT does not indicate reference to ground.

OVERRUN FLAG—This output is asserted High if a received character is not read from the XSI register before another character is fully assembled and transferred to it.

DATA AVAILABLE—This output is asserted High when a full character has been assembled and transferred to the XSI register; it goes low 800 ns after data is read from the XSI register by evoking the BUS ← XSI input. The DATA AVAILABLE signal indicates that a full character has been assembled and transferred to the XSI register and should be read (transferred to a destination via the RTM Data Bus). (Figure 2.)

READER ENABLE—When the SET READER ENABLE input is evoked, current flows at the TTY READER ENABLE output. Current flow causes a relay at the Teletype to energize and enable the paper tape reader to read one character. TTY READER ENABLE is electrically the same as TTY READER RELAY+.

TRANSMITTER BUSY—This output is asserted Low to indicate that data is being transmitted and that new data should not be loaded into the XSO register. (Figure 1.)

RTM Bus

DATA<07:07>, POWER CLEAR, DATA READY, and DATA ACCEPTED are described in the M7332 Bus Monitor and Terminator Module description.

SPECIAL WIRING AND ADJUSTMENTS

20 mA Current Loop Device Connection

A 20 mA current loop device may be connected to the M7313 module by any one of the three following methods:

1. Direct connection by Mate-N-Lok connector to the M7313.
2. Hardwiring to the equivalent points on the RTM backplane.
3. Through an M7333 Dual Serial Interface Connector Module.

To connect the device by the first method, connect the male Mate-N-Lok plug connector on the device input/output cable to the female Mate-N-Lok receptacle connector on the M7313 module.

To connect the device by the second method, use insulated, stranded, 22 AWG wire, or 6-conductor cable made of this type wire. Connect to the device input/output terminals and to the RTM backplane at the M7313 module socket as follows:

Device I/O Function	M7313 Socket Function	Pin
+DATA INPUT (PRINTER I_{in}) (+RCVD DATA)	+DATA OUT	AF2
−DATA INPUT (PRINTER I_{out}) (−RCVD DATA)	−DATA OUT	AJ2
+DATA OUT (KEYBOARD I_{in}) (+XMIT DATA)	+DATA IN	AD2
−DATA OUT (KEYBOARD I_{out}) (−XMIT DATA)	+DATA IN	AH2
TTY READER RELAY+	TTY READER ENABLE	AE2
TTY READER RELAY−	−12 V*	BV2
TTY READER RELAY−	−15 V*	BB2

* −12 V or −15 V input is required, but not both.

Procedures on how to connect the device by the third method are contained in the M7333 Dual Serial Interface Connector Module description.

SIGNAL SPECIFICATIONS

Inputs must be standard TTL levels except as follows:

Signal Name	Mate-N-Lok Pin	Module Pin
+DATA IN	7	AD2
−DATA IN	3	AH2

These input signals are described in the preceding Inputs paragraph.

Outputs are standard TTL levels except as follows:

Signal Name	Mate-N-Lok Pin	Module Pin
+DATA OUT	5	AF2
−DATA OUT	2	AJ2
TTY READER ENABLE	6	AE2

These output signals are described in the preceding Outputs paragraph.

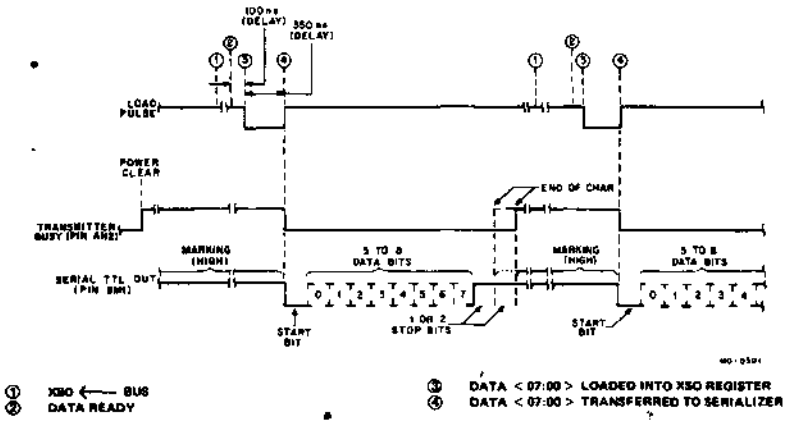


Figure 1. Transmit Mode Timing and Character Format

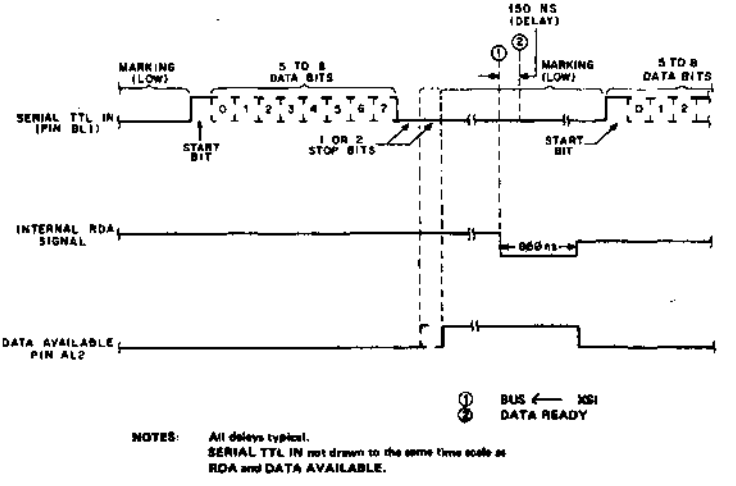
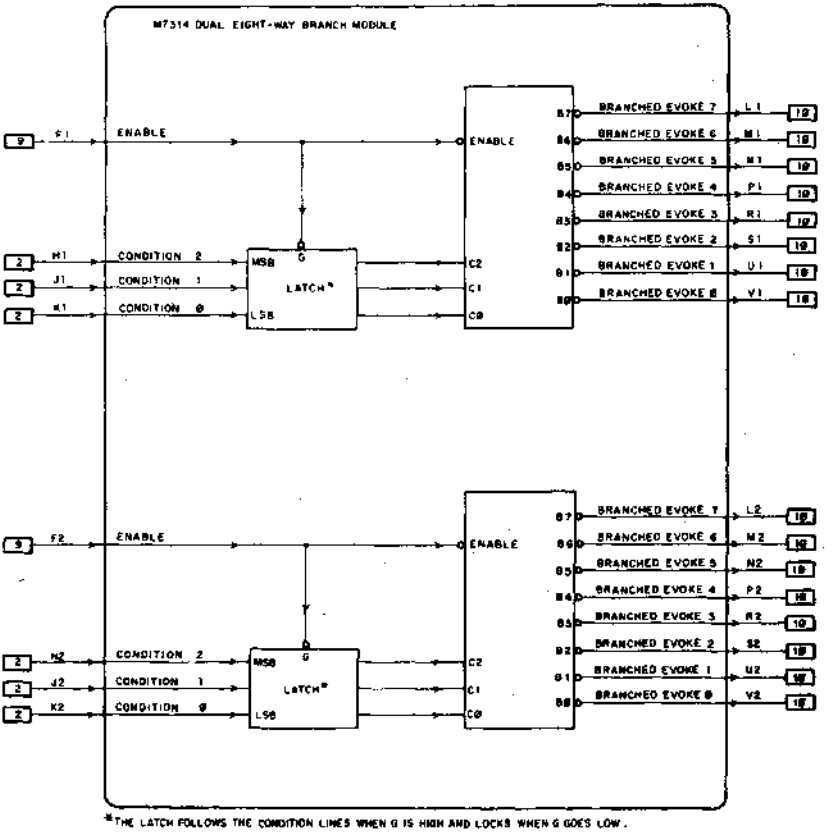


Figure 2. Receive Mode Timing and Character Format

M7314
DUAL EIGHT-WAY BRANCHES

RTM

Length: Extended
Height: Single
Width: Single



Volts	mA (typ)	Pins
+5	120	A2
GND		C2, T1

The M7314 Dual Eight-Way® Branch Module contains two eight-way branch units that are used in a hard-wired (M7310 Evoke Module controlled) RTM system to branch the control flow to one of eight possible directions. Both of the eight-way branch units on the M7314 module operate in the same manner, but are completely independent of one another.

Any number or combination of branch units (two-way or eight-way) may be combined to produce any desired degree of branching capability. For example, a 16-way branch may be created by cascading a pair of eight-way branch units with a two-way branch unit (M7312).

Each of the two eight-way branch units on the M7314 module has four input lines, a latch circuit, a binary-to-octal decoder, and eight output lines. The latch circuit outputs follow the CONDITION inputs, while the G input (ENABLE) remains High. The ENABLE input is usually asserted by an Evoke signal. When ENABLE is asserted (Low), the latch circuit stores the current CONDITION input status so that subsequent changes will not affect the output of the branch unit during the current ENABLE signal.

Inputs

ENABLE—When this input is evoked, the CONDITION inputs are evoked and one of the BRANCHED EVOKE outputs (B0 through B7) is asserted Low. It is also the G input to the latch circuit.

CONDITION 2, 1, and 0—These inputs can be connected to any TTL level signals on which a decision is to be predicated. They constitute a three-bit binary code that corresponds to one of the eight outputs, according to the table below. Input status is latched when ENABLE is asserted.

CONDITION Inputs			BRANCHED EVOKE
2	**1**	**0**	**Selected**
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

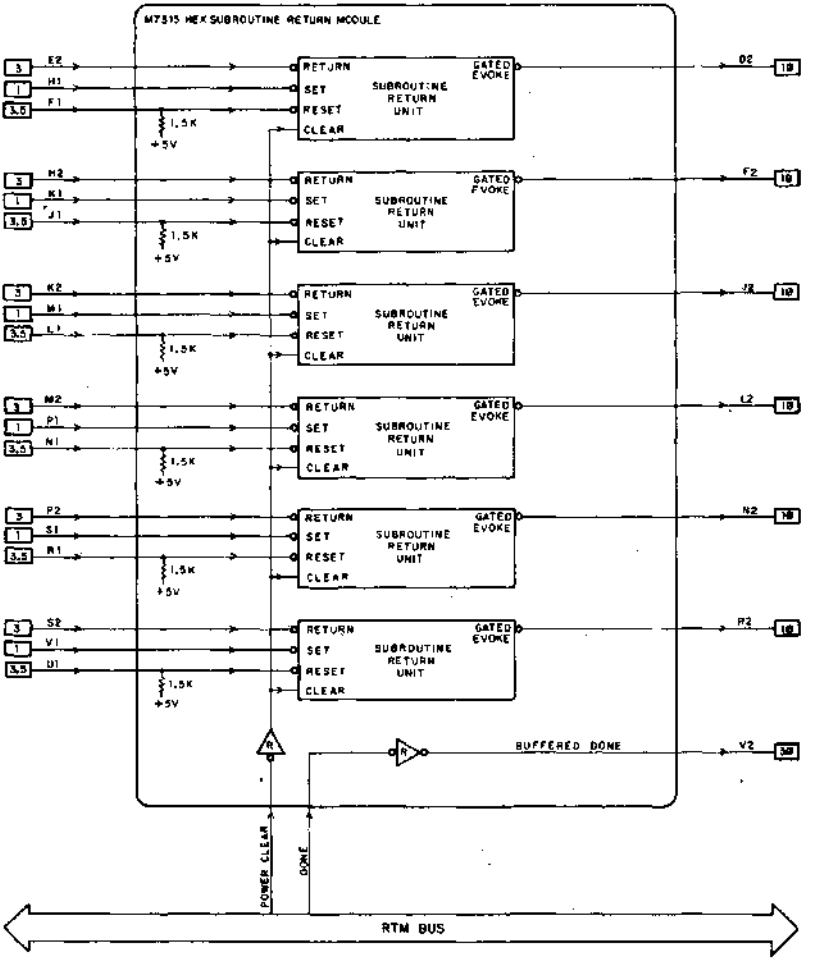
Outputs

BRANCHED EVOKE 0 through BRANCHED EVOKE 7—These signal outputs are selected according to the above table of CONDITION inputs.

M7315
HEX SUBROUTINE RETURNS

RTM

Length: Extended
Height: Single
Width: Single



Volts	mA (typ)	Pins
+5	120	A2
GND		C2, T1

The M7315 Hex Subroutine Return Module contains six independent subroutine return units, each of which can be used in a hard-wired RTM system to mark, or remember, the location in the main program where control is to be returned following the execution of a subroutine.

When a subroutine is entered, a subroutine return unit must be activated to provide a return back to the main program. One subroutine return unit is required for each place in a main program where the control flow is directed to a subroutine. The return is accomplished by directing the last Evoke signal of the subroutine back to all the return units, only one of which will gate that Evoke signal through to the main program.

Figure 1 shows a typical subroutine return unit circuit. The Evoke signal that starts a subroutine also sets the internal flip-flop, which remains set for the duration of the subroutine. If the last Evoke signal in the subroutine is not used to initiate a data transfer, then the GATED EVOKE may be utilized as the next Evoke signal in the main program following the subroutine. If the last Evoke signal in the subroutine is used to initiate a data transfer, then the GATED EVOKE would be used only to arm the following evoke unit.

Inputs

RETURN—The signal at this input is gated to the GATED EVOKE output if the internal flip-flop is set.

SET—This input sets the internal flip-flop; it is driven by the same Evoke signal that initiates the subroutine.

RESET—This input resets the internal flip-flop. This input is not used in normal subroutine return.

Outputs

GATED EVOKE—If the internal flip-flop is set, the signal at the RETURN input is gated to this output. If the internal flip-flop is reset, this output remains High.

BUFFERED DONE—This output is the buffered image of the DONE Bus signal. This output is not used in normal subroutine return operations.

RTM Bus

POWER CLEAR and DONE are described in the M7332 Bus Monitor and Terminator Module description.

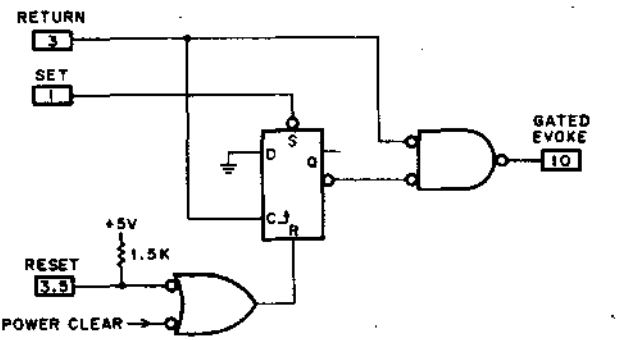
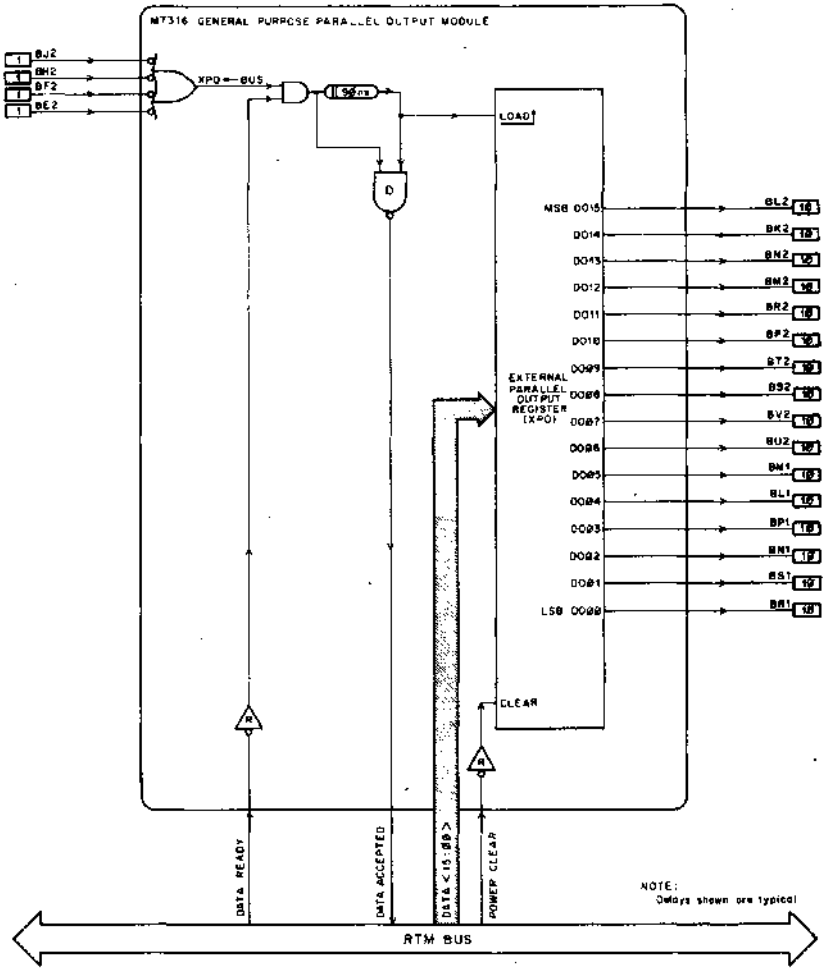


Figure 1. Typical Subroutine Return Unit Circuit

M7316
GENERAL PURPOSE PARALLEL OUTPUT MODULE

RTM



Volts	mA (typ)	Pins
+5	260	AA2, BA2
GND		AC2, BC2, AT1, BT1

The M7316 General Purpose Parallel Output Module contains bus receivers and a 16-bit storage register (XPO). The bus receivers accept a 16-bit data word from the RTM Data Bus. When the module is evoked, register XPO is loaded with the data word (DATA<15:00>), making the data word available to an external device via output lines DO<15:00>.

The external device can be informed that data is available from register XPO by using the Evoke signal for the next data transfer to also set one of the flag circuits of an M7306 Flag Module.

Inputs
XPO ← BUS—When the XPO ← BUS input is evoked, the XPO register is loaded with parallel data (DATA<15:00>) from the RTM Bus 90 ns (typical) after DATA READY is asserted. XPO ← BUS and the received DATA READY also cause DATA ACCEPTED to be asserted Low.

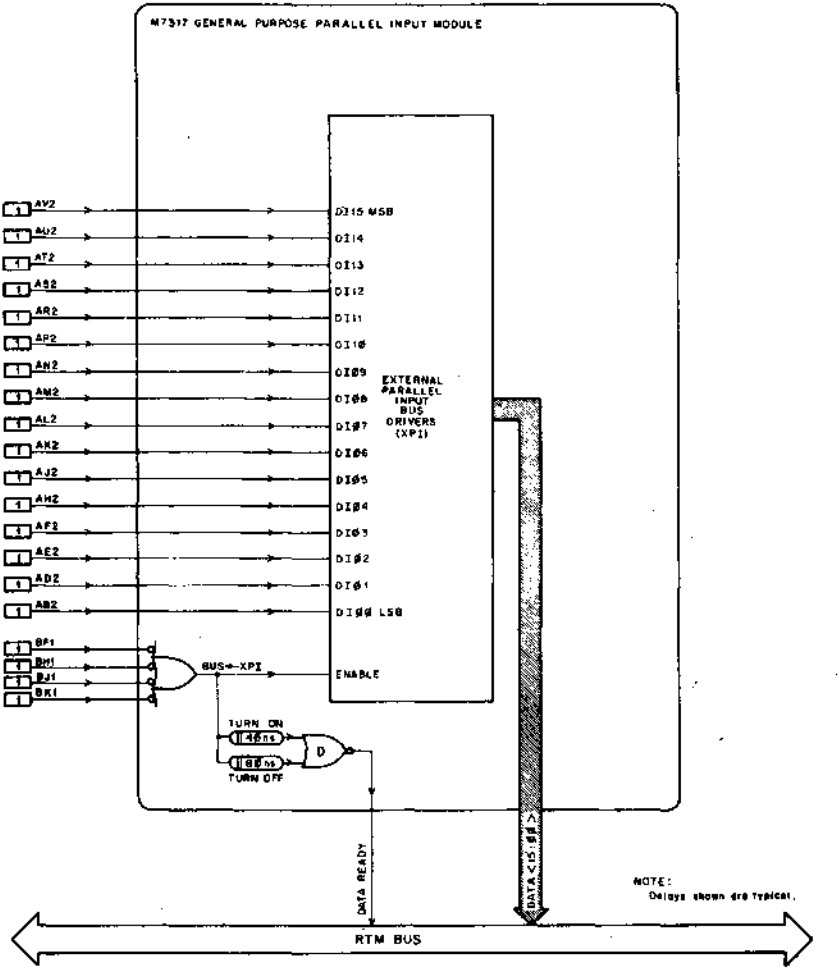
Outputs
DO<15:00>—These are the 16 data output lines from the XPO register that make the contents of that register continuously available to the external destination device until the next Evoke signal is issued to the register.

RTM Bus
DATA<15:00>, POWER CLEAR, DATA READY, and DATA ACCEPTED are described in the M7332 Bus Monitor and Terminator Module description.

M7317
GENERAL PURPOSE PARALLEL INPUT MODULE

RTM

Length: Extended
Height: Double
Width: Single



Volts	mA (typ)	Pins
+5	140	AA2
GND		AC2

The M7317 General Purpose Parallel Input Module contains bus drivers that drive a 16-bit data word from an external device to the RTM Data Bus when enabled by an Evoke signal.

Inputs

BUS ← XPI—When this input is evoked, the External Parallel Input (XPI) bus drivers are enabled and parallel data from an external source is placed on the RTM (DATA<15:00>) Bus; then, after a 40 ns (typical) delay, DATA READY is asserted.

D1<15:00>—These are the 16 data input lines to the XPI bus drivers. Data on the input lines must not be changed while being driven onto the BUS. Unused input lines, if left unconnected, will tend to read in as Ones.

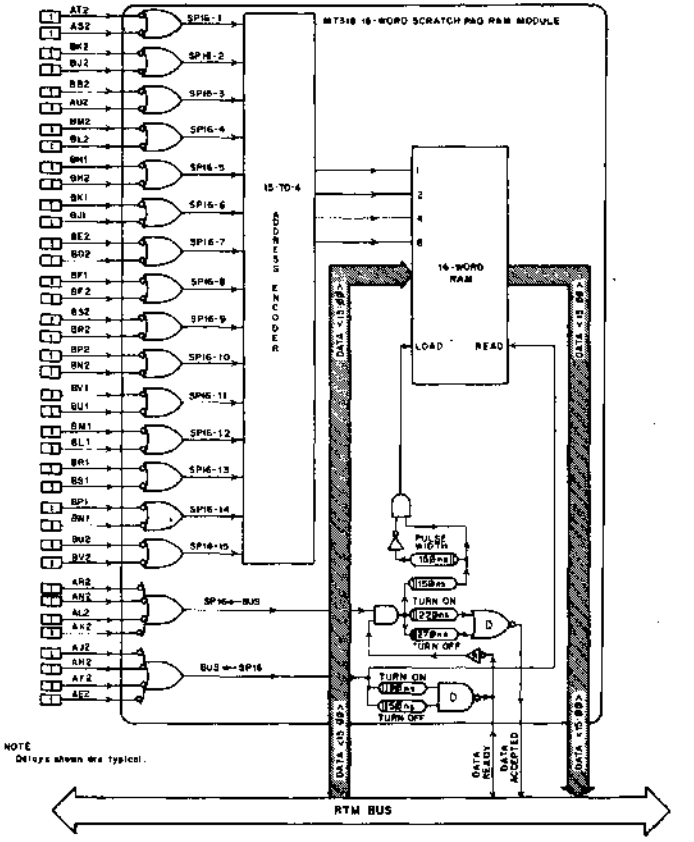
RTM Bus

DATA<15:00> and DATA READY are described in the M7332 Bus Monitor and Terminator Module description.

M7318
16-WORD SCRATCH PAD RAM

RTM

Length: Extended
Height: Double
Width: Single



Volts	mA (typ)	Pins
+5	490	AA2, BA2
GND		AC2, BC2, AT1, BT1

The M7318 16-Word Scratch Pad RAM Module contains a 16-word by 16-bit Random Access Memory (RAM) organized to operate as 16 independent 16-bit registers. This module is used to provide temporary storage for data.

Data (DATA<15:00>) from the RTM Bus lines is loaded into an addressed register when the SP16 ← BUS input is evoked; data (DATA<15:00>) is driven from an addressed register onto the RTM Bus lines when the BUS ← SP16 input is evoked. A register is addressed by asserting any SP16-# input line with the same Evoke signal that asserts either SP16 ← BUS or BUS ← SP16. If no SP input line is addressed when SP16 ← BUS or BUS ← SP16 is evoked, register 0 is addressed.

Inputs

SP16-1 through SP16-15—These are the register select inputs. When any one is asserted Low, it is encoded by the 15-to-4-line address encoder to designate one of the 16 registers. When the SP16 ← BUS input is evoked and when DATA READY is received, data (DATA<15:00>) from the RTM Bus is written into the addressed register. When the BUS ← SP16 input is evoked, data (DATA<15:00>) from the addressed register is placed on the RTM Bus.

SP16 ← BUS—When this input is evoked, it causes the addressed register to be loaded with data (DATA<15:00>) from the RTM Bus 150 ns (typical) after DATA READY is received. 200 ns (typical) after DATA READY is received, DATA ACCEPTED is asserted Low; DATA ACCEPTED remains asserted for 270 ns (typical) after SP16 ← BUS is unasserted.

If no SP input is asserted, the data is loaded into register 0. BUS ← SP16 —90 ns (typical) after this input is evoked, the data (DATA<15:00>) in the addressed register is placed on the RTM Bus and DATA READY is asserted Low; DATA READY remains asserted for 50 ns (typical) after BUS ← SP16 is unasserted.

If no SP16-# is asserted, the data in register 0 is placed on the Bus.

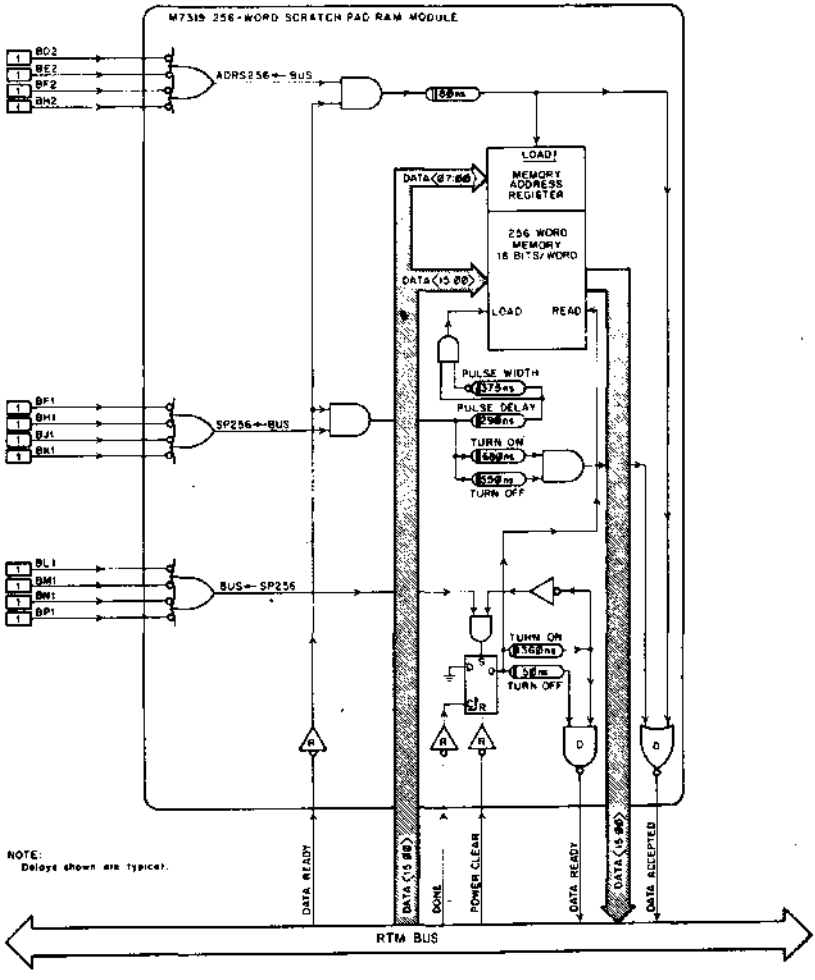
RTM Bus

DATA<15:00>, DATA READY, and DATA ACCEPTED are described in the M7332 Bus Monitor and Terminator Module description.

M7319
256-WORD SCRATCH PAD RAM

RTM

Length: Extended
Height: Double
Width: Single



Volts	mA (typ)	Pins
+5	370	AA2, BA2
−15	40	BU1
GND		AC2, BC2, AT1, BT1

The M7319 256-Word Scratch Pad RAM Module contains a solid-state Random Access Memory (RAM) with a capacity of 256 16-bit words. Word selection is accomplished by a Memory Address Register. The internal timing circuitry on the M7319 protects the user against accessing the information in the register or on the Bus before it has settled.

Transferring data into or out of this memory is a two-step process. The first step identifies the memory location involved in the data transfer by loading the Memory Address Register; the second step transfers the data.

On the M7319 module, POWER CLEAR resets a flip-flop which inhibits the internal READ signal until the flip-flop is set when the BUS ← SP256 input is asserted. The RAM is not cleared when POWER CLEAR is issued.

Inputs

ADRS256 ← BUS—This input is evoked to load the Memory Address Register. The combination of this signal and DATA READY loads the lower 8 bits of the RTM (DATA<07:00>) Bus into the Memory Address Register after a delay of 80 ns (typical). It then asserts DATA ACCEPTED.

SP256 ← BUS—This input is evoked to load data into the memory. When the SP256 ← BUS input is asserted, LOAD is asserted and the RTM (DATA <15:00>) Bus is loaded into the memory location addressed by the Memory Address Register 290 ns (typical) after DATA READY is asserted. LOAD remains asserted for 375 ns (typical). DATA ACCEPTED is asserted 680 ns (typical) after SP256 ← BUS is asserted, and is unasserted 550 ns (typical) after SP256 ← BUS is unasserted.

BUS ← SP256—This input is evoked to read data from the memory and place it onto the RTM Data Bus. This signal causes the contents of the memory location addressed by the Memory Address Register to be driven to the RTM (DATA<15:00>) Bus. DATA READY is asserted 1360 ns (typical) after BUS ← SP256 is asserted, and is unasserted 50 ns (typical) after BUS ← SP256 is unasserted.

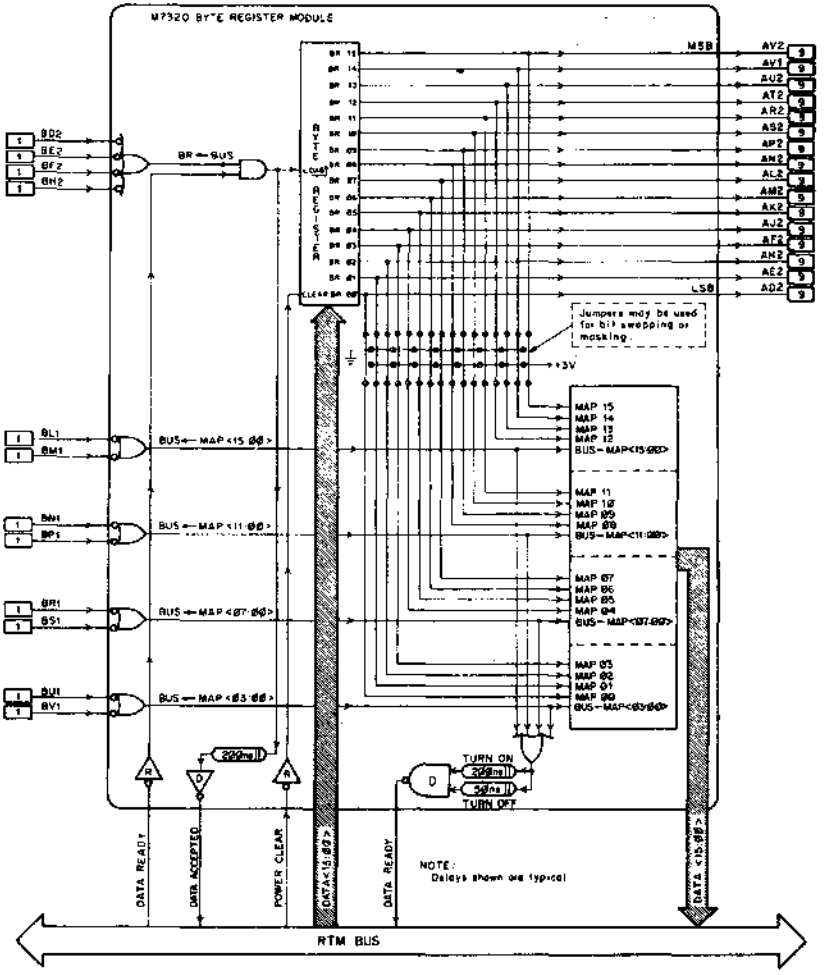
RTM Bus

DATA<15:00>, POWER CLEAR, DATA READY, DATA ACCEPTED, and DONE are described in the M7332 Bus Monitor and Terminator Module description.

M7320
BYTE REGISTER

RTM

Length: Extended
Height: Double
Width: Single



Volts	mA (typ)	Pins
+5	400	AA2, BA2
GND		AC2, BC2, AT1, BT1

The M7320 Byte Register Module is a 16-bit storage register that can be read in bytes of 4, 8, 12, or 16 bits. Loading is always a full 16-bit operation.

When reading the Byte Register, jumpers on all 16 data lines located between the Byte Register and the bus drivers make it possible to swap the bits into a desired pattern before the data is placed on the Bus. This module can also be used to generate a data constant. Outputs from the Byte Register can be monitored (prior to swapping), or used to condition branch units or interface with an external device.

The Byte Register is cleared by POWER CLEAR.

Inputs

BR ← BUS—When this input is evoked, data (DATA<15:00>) from the RTM Bus is loaded into the Byte Register (BR<15:00>) as soon as DATA READY is asserted. After a delay of 200-ns (typical), DATA ACCEPTED is asserted.

BUS ← MAP<15:00>—When this input is evoked, data from MAP<15:00>, the jumpered output of the Byte Register (BR<15:00>), is driven onto the RTM Bus. After a delay of 200 ns (typical), DATA READY is asserted.

BUS ← MAP<11:00>—When this input is evoked, data from MAP<11:00> is driven onto the RTM Bus; the remaining bits (MAP<15:12>) are left unasserted. After a delay of 200 ns (typical), DATA READY is asserted.

BUS ← MAP<07:00>—When this input is evoked, data from MAP<07:00> is driven onto the RTM Bus; the remaining bits (MAP<15:80>) are left unasserted. After a delay of 200 ns (typical), DATA READY is asserted.

BUS ← MAP<03:00>—When this input is evoked, data from MAP<03:00> is driven onto the RTM Bus; the remaining bits (MAP<15:04>) are left unasserted. After a delay of 200 ns (typical), DATA READY is asserted.

Outputs

BR<15:00>—These are the 16 data output lines from the Byte Register that make the contents of the register continuously available for monitoring purposes or to an external device until the next Evoke signal is issued to the register.

RTM Bus

DATA<15:00>, POWER CLEAR, DATA READY, and DATA ACCEPTED are described in the M7332 Bus Monitor and Terminator Module description.

SPECIAL WIRING AND ADJUSTMENTS

WARNING

Extreme care should be exercised when removing jumpers from the module to avoid lifting or otherwise damaging the printed circuit etching. Clip both ends of the jumper as close as practical to the solder pads and remove the jumper from the module.

The jumpers on the M7320 module (see Figure 1) permit bit-swapping between the Byte Register and the RTM Data Bus when this module is used as the source module in a data transfer. By removing the factory-installed jumpers and connecting jumpers from split lugs in the top row (the output of BR<15:00>) to other split lugs in the bottom row (the input of MAP <15:00>), bits may be swapped as desired. Split lugs on this module connected to GROUND and +3 V may be used to connect selected bits Low or High.

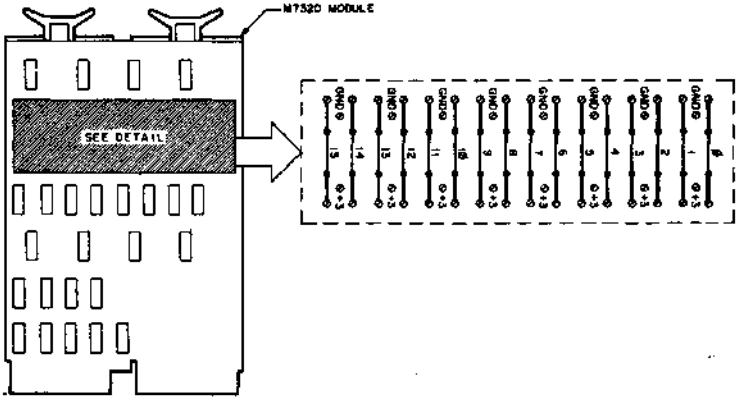
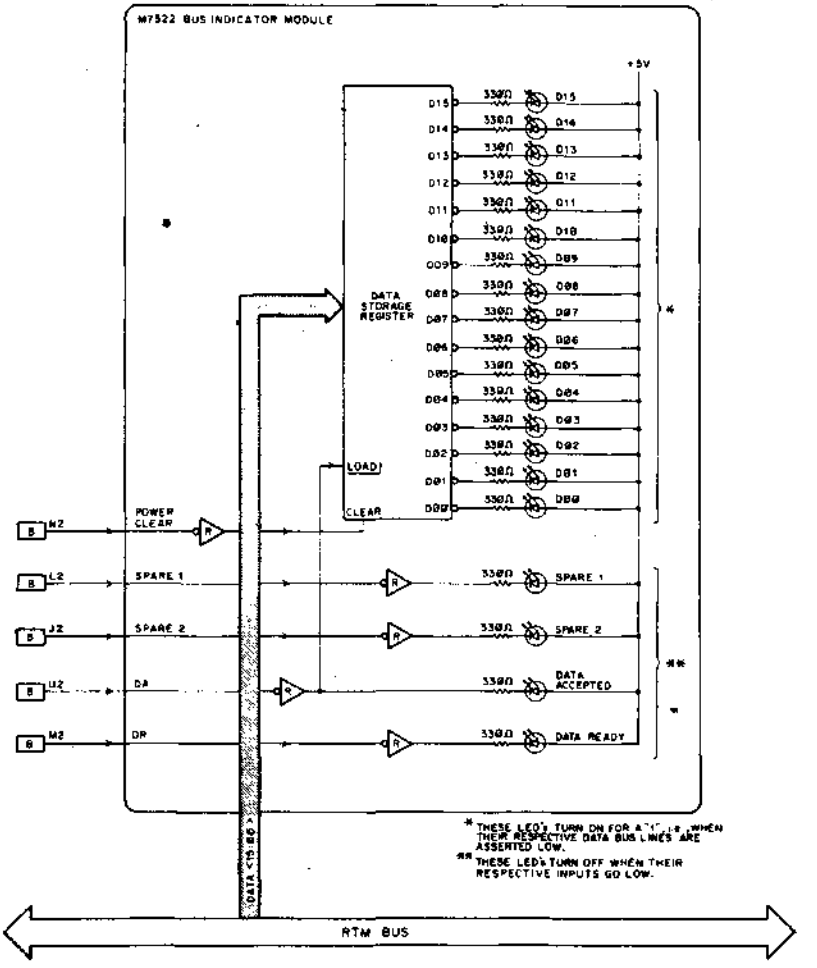


Figure 1

M7322
BUS INDICATOR MODULE

RTM

Length: Extended
Height: Single
Width: Single



Volts	mA (typ)	Pins
+5	200	A2
GND		C2, T1

The M7322 Bus Indicator Module is a Bus readout device that provides a visual indication of the data transferred on the Data Bus. Light Emitting Diode (LED) indicators are used to monitor the 16 Data lines, the DATA READY line, and the DATA ACCEPTED line. Therefore, the status of the Data Bus and of the Control Bus can be easily monitored while single-stepping an RTM system. Two spare LEDs are included for monitoring other TTL or Bus signals.

Inputs

SPARE 1 and SPARE 2—These inputs are connected to high-impedance (27 kΩ) receivers. They may be used to monitor any signal in the system, including Bus lines. The state of these inputs is not stored. Each SPARE LED indicator will be on when its input is High and off when its input is Low.

LED Displays

D<15:00>—These LED indicators display the status of each data bit in the data storage register, which is loaded from the Data Bus lines each time DATA ACCEPTED is asserted. Turned-on indicators represent Data Bus lines asserted Low.

SPARE 1 and SPARE 2—These LED indicators display the status of the signals being monitored by the SPARE 1 and SPARE 2 input lines. Each indicator is turned on when its input line is High.

DATA ACCEPTED—This LED displays the status of the Data Accepted Bus line. The indicator is turned off when this line is asserted Low.

DATA READY—This LED displays the status of the Data Ready Bus line. The indicator is turned off when this line is asserted Low.

RTM Bus

DATA <15:00>, DATA READY, and DATA ACCEPTED are described in the M7332 Bus Monitor and Terminator Module description.

OPERATION

When the system is in manual mode and power is first turned on, the DATA READY and DATA ACCEPTED indicators should be on and the DATA indicators should be off. The data storage register is cleared by POWER CLEAR.

After each data transfer to or from the RTM System Data Bus when single-stepping through a program, LED indicators D<15:00> will be on if their respective data bits were asserted Low; these LED indicators will continue to display this status until another transfer occurs.

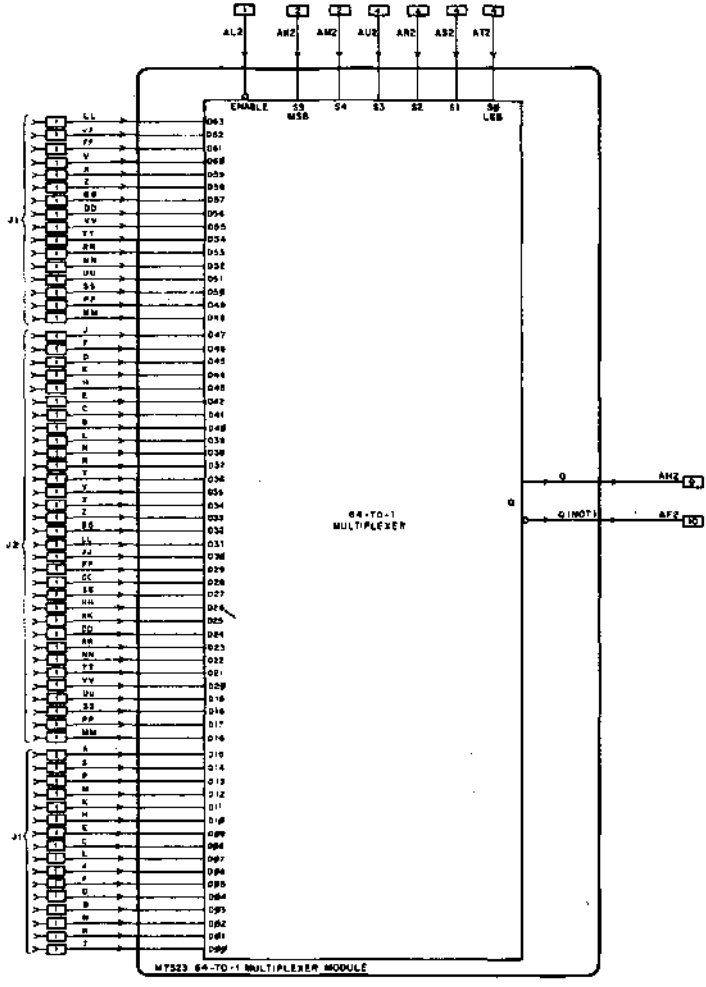
When single-stepping, the system will stop between DATA ACCEPTED and DONE. The LEDs will then display the state of DATA ACCEPTED and DATA READY at that time. Both should be off, indicating that those lines are asserted.

The Bus Indicator Module may be plugged into the RTM Data Bus section in a bused panel and the data LEDs will automatically make contact with the bus lines. However, the DATA READY and DATA ACCEPTED signals will have to be wired to pins M2 and U2 respectively if these signals are to be monitored.

M7323
64-to-1 MULTIPLEXER

RTM

Length: Extended
Height: Double
Width: Single



Volts	mA (typ)	Pins
+5	150	AA2, BA2
GND		AC2, BC2, AT1, BT1

The M7323 64-to-1 Multiplexer Module can be used to monitor up to 64 external condition inputs so that any one may be selected to be presented to the output. If more than 64 condition inputs require monitoring, additional M7323 modules can be used in an RTM system.

The M7323 module decodes a 6-bit binary input to select one of the 64 condition inputs.

To monitor more than 64 condition inputs, one of the following methods may be used. To select between two M7323 modules with one of the flags on an M7306 Flag Module, the ENABLE input of one M7323 should be connected to the F1 output of the flag and the ENABLE input of the second M7323 should be connected to the F1(NOT) output. The desired M7323 will then be selected according to the setting of the flag, while the other M7323 will be deselected. Refer to the M7306 Flag module description.

By using one of the branch units of an M7314 Dual Eight-Way Branch Module, it is possible to select any one of up to eight M7323 modules. The process of enabling the branch unit causes its latch circuit to save the status of its condition inputs, thereby providing the means to monitor and save the condition information. Refer to the M7314 Dual Eight-Way Branch Module description.

Using more than one M7323 module as described above with a flag or a branch requires that an appropriate OR gate be used to OR the outputs of the M7323 modules together. Refer to the M1103 Ten 2-Input OR Gates Module and the M1307 Six 4-Input OR Gates Module descriptions. Only one M7323 module should be enabled at a time.

Inputs

ENABLE—When this input is asserted Low, this 64-to-1 multiplexer is enabled.

S<5:0>—These six inputs receive the binary input that determines which input signal (D<63:00>) will be selected and routed to the output. The selection is based on the following table:

SELECT Inputs						Input Signal Selected
S5	S4	S3	S2	S1	S0	
L	L	L	L	L	L	D00
L	L	L	L	L	H	D01
L	L	L	L	H	L	D02
L	L	L	L	H	H	D03
L	L	L	H	L	L	D04
L	L	L	H	L	H	D05
L	L	L	H	H	L	D06
L	L	L	H	H	H	D07
L	L	H	L	L	L	D08
L	L	H	L	L	H	D09
L	L	H	L	H	L	D10
L	L	H	L	H	H	D11
L	L	H	H	L	L	D12
L	L	H	H	L	H	D13
L	L	H	H	H	L	D14
L	L	H	H	H	H	D15
L	H	L	L	L	L	D16
L	H	L	L	L	H	D17

SELECT Inputs						Input Signal Selected
S5	S4	S3	S2	S1	S0	
L	H	L	L	H	L	D18
L	H	L	L	H	H	D19
L	H	L	H	L	L	D20
L	H	L	H	L	H	D21
L	H	L	H	H	L	D22
L	H	L	H	H	H	D23
L	H	H	L	L	L	D24
L	H	H	L	L	H	D25
L	H	H	L	H	L	D26
L	H	H	L	H	H	D27
L	H	H	H	L	L	D28
L	H	H	H	L	H	D29
L	H	H	H	H	L	D30
L	H	H	H	H	H	D31
H	L	L	L	L	L	D32
H	L	L	L	L	H	D33
H	L	L	L	H	L	D34
H	L	L	L	H	H	D35
H	L	L	H	L	L	D36
H	L	L	H	L	H	D37
H	L	L	H	H	L	D38
H	L	L	H	H	H	D39
H	L	H	L	L	L	D40
H	L	H	L	L	H	D41
H	L	H	L	H	L	D42
H	L	H	L	H	H	D43
H	L	H	H	L	L	D44
H	L	H	H	L	H	D45
H	L	H	H	H	L	D46
H	L	H	H	H	H	D47
H	H	L	L	L	L	D48
H	H	L	L	L	H	D49
H	H	L	L	H	L	D50
H	H	L	L	H	H	D51
H	H	L	H	L	L	D52
H	H	L	H	L	H	D53
H	H	L	H	H	L	D54
H	H	L	H	H	H	D55
H	H	H	L	L	L	D56
H	H	H	L	L	H	D57
H	H	H	L	H	L	D58
H	H	H	L	H	H	D59
H	H	H	H	L	L	D60
H	H	H	H	L	H	D61
H	H	H	H	H	L	D62
H	H	H	H	H	H	D63

MULTIPLEXER INPUTS D<63:00>—These inputs connect to pins on two 40-pin connectors (H854), J1 and J2, for easy interfacing with peripheral equipment. H854 connectors mate with H856 cable connectors.

Outputs

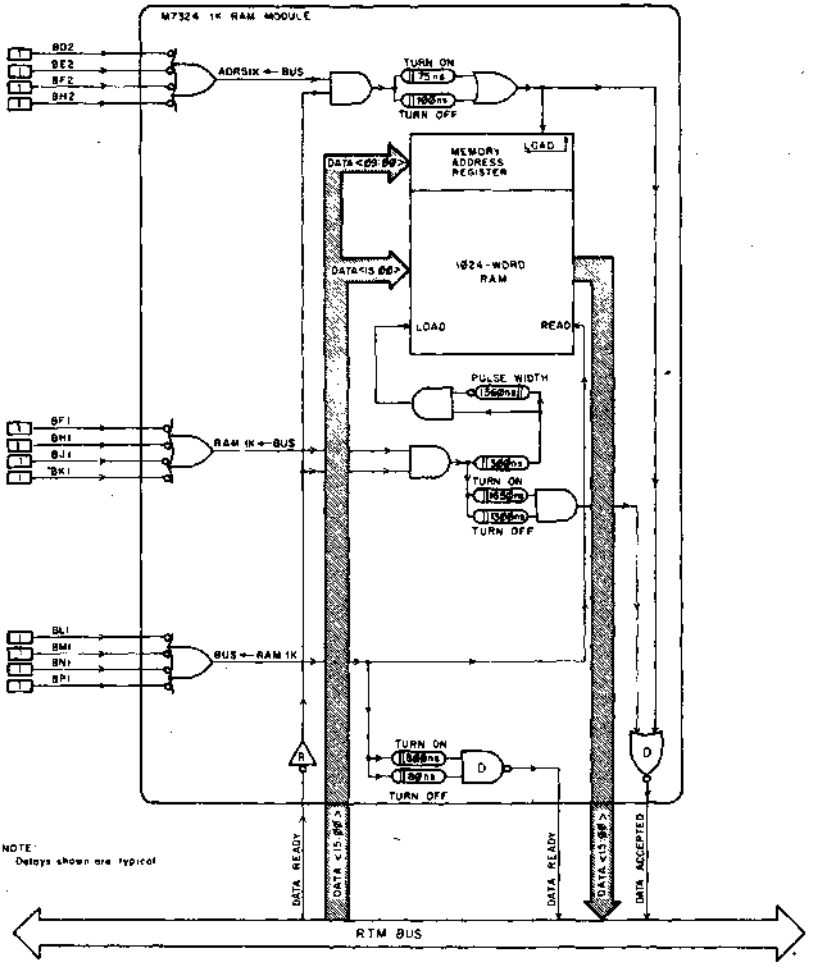
Q—This output follows the selected input.

Q(NOT)—This output is the complement of the Q output.

M7324
1K RAM

RTM

Length: Extended
Height: Double
Width: Single



Volts	mA (typ)	Pins
+5	600	AA2, BA2
GND		AC2, BC2, AT1, BT1

The M7324 1K RAM Module contains a solid-state Random Access Memory (RAM) with a capacity of 1024 16-bit words.

Transferring data into or out of this memory is a two-step process. The first step identifies the memory location involved in the data transfer by loading the Memory Address Register; the second step transfers the data.

Inputs

ADRS1K←BUS—This input is evoked to place the address data from the RTM Data Bus into the M7324 Memory Address Register. 75 ns (typical) after the combination of this signal and DATA READY is asserted, the lower 10 bits (DATA<09:00>) of the RTM M Bus are loaded into the Memory Address Register and DATA ACCEPTED is asserted. DATA ACCEPTED is unasserted 100 ns (typical) after ADRS1K←BUS is unasserted.

RAM1K←BUS—This input is evoked to load data into the addressed memory location. The combination of this signal and DATA READY asserts LOAD after a delay of 300 ns (typical), and it remains asserted for 1360 ns (typical). During that period, the memory location addressed by the Memory Address Register is loaded with data (DATA<15:00>) from the RTM Bus. DATA ACCEPTED is asserted 1650 ns (typical) after the combination of RAM1K← BUS and DATA READY, and is unasserted 1300 ns (typical) after the RAM1K← BUS signal is unasserted.

BUS←RAM1K—This input is evoked to place data (DATA<15:00>), the contents of the memory location addressed by the Memory Address Register, onto the RTM Data Bus. DATA READY is asserted 800 ns (typical) after the assertion of BUS←RAM1K.

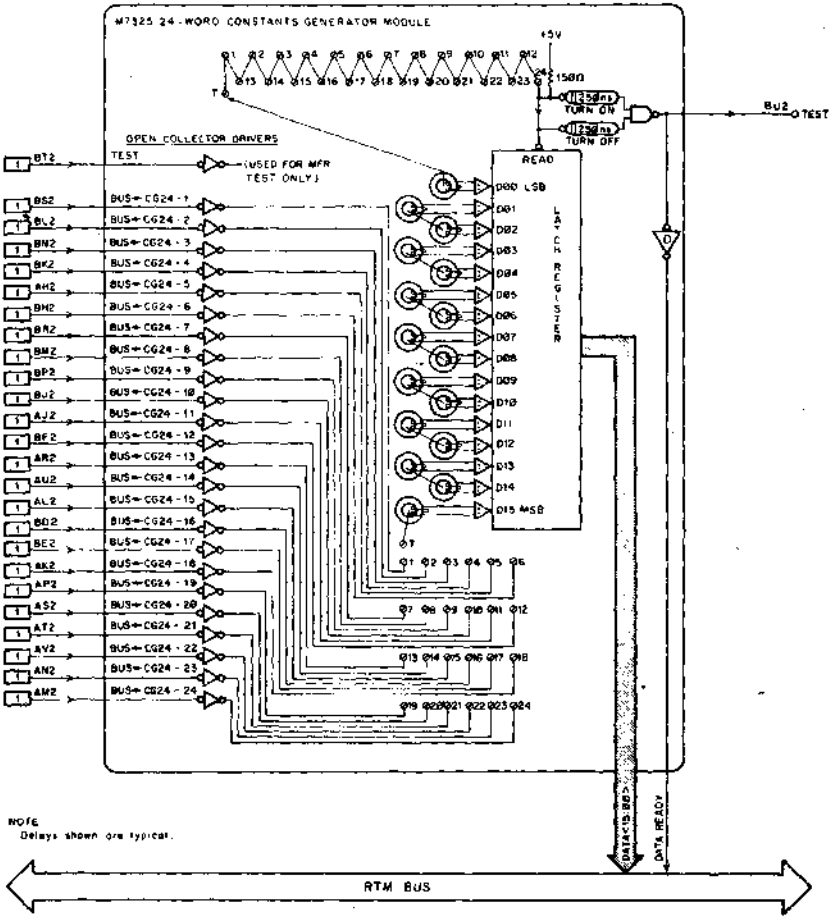
RTM Bus

DATA <15:00>, DATA READY, and DATA ACCEPTED are described in the M7332 Bus Monitor and Terminator Module description.

M7325
24-WORD CONSTANTS GENERATOR

RTM

Length: Extended
Height: Double
Width: Single



Volts	mA (typ)	Pins
+5	400	AA2, BA2
GND		AC2, BC2, AT1, BT1

The M7325 24-Word Constants Generator Module provides Programmable Read-Only Memory (PROM) storage for twenty-four 16-bit constants defined by user hardwiring on the module. This capability is particularly useful in the case of data constants that might have to be changed occasionally. To change a data constant, the user merely has to rethread one wire on the M7325.

Constants generators can be used wherever there is a need for a numeric, character code, or data mask code constant.

The M7325 module contains two groups of 25 split lugs each, separated by a bank of 16 sensing cores. Each group of lugs is numbered from 1 to 24, plus a T to designate the test lugs, so that companion pairs can be easily identified. Constants are defined by connecting a wire between pairs of lugs so that the wire either passes through or around each sensing core, depending on whether a binary One or a binary Zero is desired. To indicate the direction and manner in which the wires representing the constants must be strung, the module is shipped with a test wire woven through all of the cores and connecting the two test lugs. (Refer to SPECIAL WIRING AND ADJUSTMENTS.)

Inputs

TEST—This input is used by Digital Equipment Corporation for testing.

BUS←CG24-#—(Where # represents the number of one of the 24 data word constants.) When one of these inputs is evoked, an open-collector driver causes current to flow through the wire between the lugs associated with the number #. Where the wire passes through one of the current-sensing cores, a binary One is generated. Where it passes outside a core and through the nearby hole in the module, a binary Zero is generated. Sense amplifiers connected to each core amplify the signals and apply them to the latch register (D<15:00>). Assertion of BUS←CG24-# also enables the latch register. Bus drivers drive the selected constant (DATA<15:00>) to the RTM Bus. DATA READY is asserted 250 ns (typical) after BUS←CG24-# is evoked, and is unasserted 250 ns (typical) after the signal is unasserted.

NOTE

No BUS←CG24-# input for which a wire has not been run should ever be evoked in an attempt to generate all Zeroes because DATA READY will not be generated. If a data word constant of all Zeroes is desired, it can be achieved more efficiently by the BUS←0 input of either the M7332 Bus Monitor and Terminator Module or the M7304 Bus Sense Register Module.

Outputs
TEST—This output is used by Digital Equipment Corporation for testing.

RTM Bus
DATA <15:00> and DATA READY are described in the M7332 Bus Monitor and Terminator Module description.

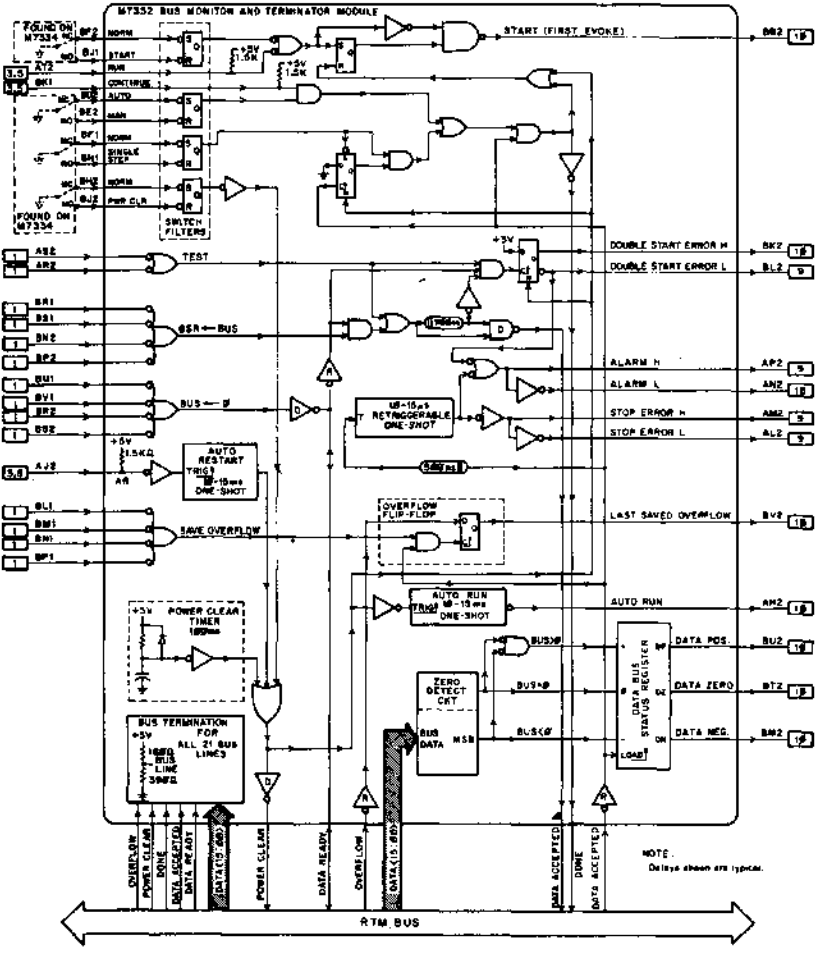
SPECIAL WIRING AND ADJUSTMENTS
To encode a constant, it is only necessary to thread and solder an insulated AWG 30 solid wire between a pair of companion lugs. The pattern followed when threading the wire through or around the cores determines the constant. A wire passing through a core produces a binary One for the bit associated with that particular core; a wire bypassing the core and passing instead through the nearby hole in the module produces a binary Zero for that bit.

NOTE
Wires must pass through the desired cores in the same direction as the test wire.

M7332
BUS MONITOR AND TERMINATOR

RTM

Length: Extended
Height: Double
Width: Single



Volts	mA (typ)	Pins
+5	825	AA2, BA2
GND		AC2, BC2, AT1, BT1

The M7332 Bus Monitor and Terminator Module contains the circuitry to perform several essential system-level functions that might otherwise have to be included in each RT module. The M7332 includes a pull-up/termination resistor network for each RTM Bus Line.

An M7332 module or both an M7304 Bus Sense Register Module and an M962 Bus Terminator Module are required in every RTM system. The M7332 should be placed at one end of the RTM Bus because of the termination networks on the module. If the system contains a Bus that is over 19 inches long, an M962 Bus Terminator Module should be placed at the other end of the Bus.

The M7332 Bus Monitor and Terminator Module generates the POWER CLEAR signal that is used to initialize flip-flops and other circuits when power is first applied to the system. In addition, the M7332 is used to issue the first EVOKE signal in an evoke-controlled RTM system or the START signal in a PCS-controlled RTM system. This module generates the DONE signal to indicate the completion of each data transfer, and it contains the Data Bus arithmetic status circuitry that continually monitors the RTM DATA<15:00> Bus lines and generates the BUS>0, BUS=0, or BUS<0 status signals. Whenever DATA ACCEPTED is issued, the BUS>0, BUS=0, or BUS<0 status signals are loaded into the Data Bus Status Register and placed on the M7332 output lines as DATA POS, DATA ZERO, AND DATA NEG signals; each of these signals can be used for CONDITION inputs to branches.

The Bus Monitor and Terminator Module has three sets of functional signal inputs that allow it to be used as either a source or destination of data. The BUS←0 functional input is used wherever a source of all Binary Zeros is desired. While it is true that the Bus will, by definition, contain all Zeros when no source is specified, a destination cannot read the Bus unless DATA READY is present; the Bus Monitor and Terminator Module provides a DATA READY signal when a BUS←0 input is evoked. Along the same lines, it may be necessary, during the execution of a program, to make the Data Bus Status Register the only destination of a transfer. The Data Bus Status Register will be loaded only when some destination register issues DATA ACCEPTED or when the BSR←BUS functional input is asserted to generate DATA ACCEPTED.

The third functional input causes the logic state of the Overflow Bus line to be loaded into a flip-flop. This operation does not generate a DATA ACCEPTED signal and is, therefore, used in conjunction with a data transfer between the Arithmetic and Logic Function Modules and a destination register to save the overflow bit that resulted from an arithmetic or logic function operation. The output of the Overflow flip-flop can then be used as a status input for a subsequent branch decision.

The M7332 contains four switch filters that allow external switches to be added for manual control of an RTM system. Any single-pole double-throw switch may be used when connected as shown on the functional diagram. The M7334 Switch and Light Module contains extra switches that may be used for this purpose. Refer to the M7334 Switch and Light Module description.

Inputs

BUS←0—When this input is evoked, the M7332 immediately produces a DATA READY signal. DATA READY is asserted Low and is used in an RTM system as a LOAD or ENABLE signal to allow a selected destination register to read the Data Bus. DATA READY remains Low until the current Evoke signal is unasserted.

BSR←BUS—When this input is evoked, it allows the M7332 Bus Status circuitry to be the only destination of a data transfer by generating DATA ACCEPTED after 900 ns (typical).

SAVE OVERFLOW—A Low at this input causes the Overflow flip-flop to store the logic state of the Overflow Bus line when DATA ACCEPTED is issued by a data destination. This input must be evoked in parallel with an arithmetic operation in order to save the Overflow results of that operation for subsequent testing.

RUN—This input allows a TTL level signal to be used for starting an RTM system. The START (FIRST EVOKE) output will be issued at the trailing edge of a Low-going pulse at the RUN input. The pulse width must be at least 100 ns. This can be used to start a remote RTM system with external logic or a filtered pushbutton or toggle switch. It may also be used to provide automatic starting when power is turned on by connecting this input to the AUTO RUN output. This input may be left unconnected if not used.

AR (AUTO RESTART)—A Low pulse at this input causes POWER CLEAR to be generated and placed on the RTM POWER CLEAR Bus line. This input can be used to initialize the RTM system anytime after power-up. It will cause the RTM system to automatically restart at the beginning of the program if the AUTO RUN output is connected to the RUN input.

CONTINUE—This input allows a TTL level signal to be used for switching the system from the auto to the manual mode. A Low applied to this input from either a logic circuit or a filtered switch will place the system in the manual mode, regardless of the position of the AUTO/MAN switch. This input can be used to remotely control the mode of an RTM system.

The CONTINUE input may also be used to provide a breakpoint capability that will halt an RTM system at any desired transfer operation. This is accomplished by connecting a jumper from the CONTINUE input to the evoke signal that causes the transfer operation. Therefore, when the system is started with the AUTO/MAN switch in the AUTO position, it will run until it reaches the breakpoint evoke signal. At that point, the Low on the CONTINUE input will force the system into the manual mode and it will halt with DATA READY and DATA ACCEPTED asserted and the data source bus drivers enabled. The AUTO/MAN switch can then be placed in the MAN position so that single stepping can proceed from that point. Returning the AUTO/MAN switch to the AUTO position will cause the system to continue with the next program instruction after a single step has been performed.

TEST—This input can be evoked at any time during the execution of a program to test for the presence of more than one EVOKE signal in the system. The test circuitry monitors the DATA READY Bus line for 900 ns and, if DATA READY should appear during that interval, the DOUBLE START ERROR signals will be issued. At the end of the 900 ns period DATA ACCEPTED is issued.

NORM/START—This switch input provides for manually starting at RTM system with an external single-pole double-throw switch. The switch normally rests in the NORM position with pin BF2 grounded. Moving the switch to the START position (pin BJ1 grounded) and then back to the NORM position again will cause the START (FIRST EVOKE) signal to be issued. If a START switch is not used, the M7332 input pin BF2 (NORM) must be tied to ground. Refer to SPECIAL WIRING AND ADJUSTMENTS.

AUTO/MAN—This switch input is used in conjunction with the NORM/SS switch input to provide single-stepping capability that is extremely useful for trouble-shooting and for initial system debugging. With this switch in the AUTO position (pin BD2 grounded), automatic mode is enabled and the system will execute the program in the normal manner. With the switch in the MAN position (pin BE2 grounded), manual mode is enabled and the system will halt after executing each instruction. This is accomplished by preventing the assertion of the DONE signal when DATA ACCEPTED is received by the M7332. Thus, the system will halt with the DATA READY and the DATA ACCEPTED signals asserted and with the data source bus drivers enabled. If an AUTO/MAN switch is not utilized, then the M7332 input pin BE2 (AUTO) must be connected to ground. Refer to SPECIAL WIRING AND ADJUSTMENTS.

NORM/SS—This switch input is used in conjunction with the AUTO/MAN switch input when that switch is in the MAN position. When the RTM system is in the manual mode, one instruction will be executed each time the NORM/SS switch is moved from the NORM position (pin BF1 grounded) to the SS position (pin BH1 grounded) and then back to the NORM position again. When staring the system in the manual mode, the NORM/START switch must be activated to execute the first instruction. If a NORM/SS switch is not used in an RTM system, the M7332 input pin BF1 (NORM) must be tied to ground. Refer to SPECIAL WIRING AND ADJUSTMENTS.

NORM/PWR CLR—This switch input provides for initializing the RTM system anytime after power-up with an external single-pole, double-throw switch. The switch normally rests in the NORM position with pin BH2 grounded. Moving the switch to the PWR CLR position will cause the POWER CLEAR signal to be issued. If a PWR-CLR switch is not used, the M7332 input pin BH2 (NORM) must be tied to ground. Refer to SPECIAL WIRING AND ADJUSTMENTS.

Outputs

DATA POS—A high at this output indicates that the last data transferred was positive. This assumes that the data is in two's complement form.

DATA ZERO—A high at this output indicates that the last data transferred was equal to zero.

DATA NEG—A high at this output indicates that the last data transferred was negative (less than zero). This assumes that the data is in two's complement form.

LAST SAVED OVERFLOW—This output provides the status of the Overflow flip-flop.

START (FIRST EVOKE)—This output is the START signal for the PCS module-controlled system or the first EVOKE signal for an evoke module-controlled system. This signal goes Low when the START switch is pressed and released, then goes High when DONE is received.

POWER CLEAR—This RTM Bus signal is asserted for approximately 100 ms when dc power is first applied to the RTM system or for as long as the PWR CLR switch connects BJ2 to ground.

DOUBLE START ERROR H—A High at this output indicates that the TEST input has been evoked and the circuitry has detected the presence of more than one EVOKE signal in the system, which is an undesirable situation. This situation can occur as a result of component failure in an EVOKE unit or if the

START button is pressed while the system is already running. The DOUBLE START ERROR signal can be used to trigger a visual or audible alarm or it can be used as a branch condition that would cause the AUTO RESTART input to be evoked. If the AUTO RUN output is connected to the RUN input, the POWER CLEAR signal will clear all evoke units and the AUTO RUN signal will restart the program at the beginning.

DOUBLE START ERROR L—The complement of DOUBLE START ERROR H.

STOP ERROR H—A High at this output indicates that DATA ACCEPTED was not received from the RTM DATA ACCEPTED Bus line within a 10 μs interval after the previous DATA ACCEPTED. This is interpreted as an indication that the system has stopped.

STOP ERROR L—The complement of STOP ERROR H.

ALARM H—A High at this output indicates that a DOUBLE START ERROR condition or a STOP ERROR condition exists; i.e., an error exists due to multiple EVOKES or DATA ACCEPTED was not received within the last 10 μs.

ALARM L—The complement of ALARM H.

AUTO RUN—A low pulse (10–15 ms) is issued at this output when the system is first turned on. This output may be connected to the RUN input to automatically start program execution when power is first applied or when the AUTO RESTART input is asserted.

RTM BUS SIGNALS AND PIN ASSIGNMENTS

The RTM Bus consists of 21 lines; 16 are used to transfer data from each source to each destination, one is the Overflow Bus, three are used to carry control signals, and one is the Power Clear Bus. All Bus signals are asserted Low.

Data Bus

The 16-bit Data Bus is configured as follows:

Pin	Signal
AA1	Data Bus bit 0 (LSB)
AB1	Data Bus bit 1
AC1	Data Bus bit 2
AD1	Data Bus bit 3
AE1	Data Bus bit 4
AF1	Data Bus bit 5
AH1	Data Bus bit 6
AJ1	Data Bus bit 7
AK1	Data Bus bit 8
AL1	Data Bus bit 9
AM1	Data Bus bit 10
AN1	Data Bus bit 11
AP1	Data Bus bit 12
AR1	Data Bus bit 13
AS1	Data Bus bit 14
AU1	Data Bus bit 15 (MSB)

Overflow Bus
The Overflow Bus is configured as follows:

Pin	Signal	Function
BA1	OVERFLOW	Carries the overflow output of the Arithmetic and Logic Function Modules (M7300 and M7301).

Control Bus
The control bus is configured as follows:

Pin	Signal	Function
BE1	DATA READY	Signifies that the source has placed data on the Data Bus.
BC1	DATA ACCEPTED	Signifies that the destination has received data from the Data Bus.
BD1	DONE	Signifies that a data transfer has been completed.

Power Clear Bus
The Power Clear Bus is configured as follows:

Pin	Signal	Function
BB1	POWER CLEAR	Initializes the system.

SPECIAL WIRING AND ADJUSTMENTS

Switch Filter Inputs
The following table lists the proper switch wiring connections to the switch filter inputs. The START, PWR CLR, and the SINGLE STEP (SS) switches may be single-pole, double-throw pushbutton or toggle switches with momentary contacts. The AUTO/MAN switch should be a single-pole, double-throw toggle or slide switch. Also listed in the following table are the connections that must be made if switches are not used.

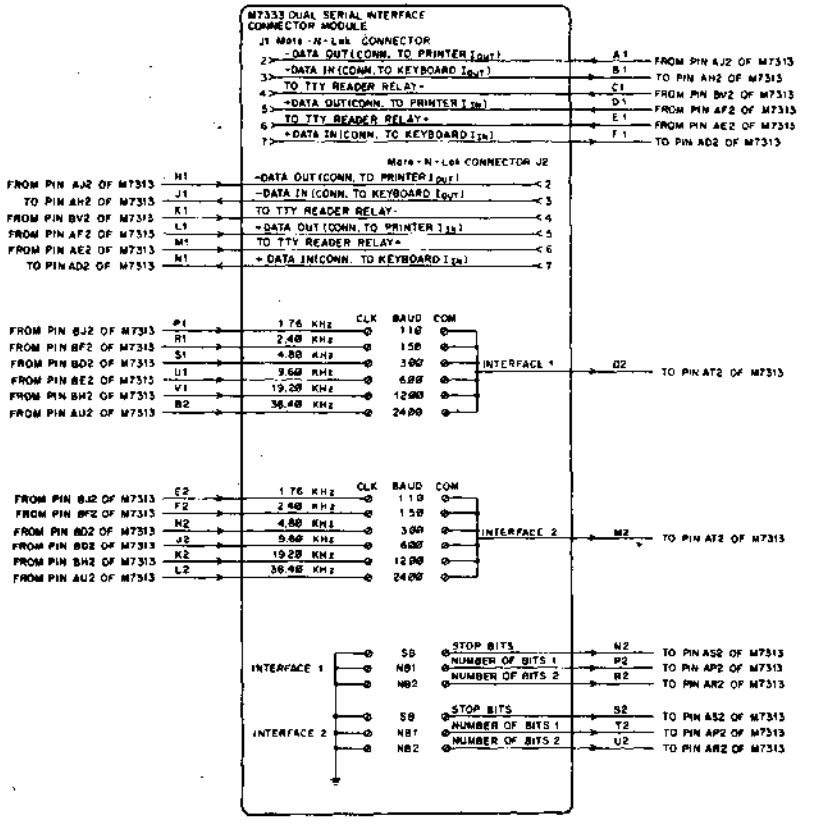
Switch	Switch Contact Connections	Hardwired Connections
START	Normally Closed to pin BF2 Normally Open to pin BJ1 Common to ground	Pin BF2 to ground Pin BJ1 no connection
AUTO/MAN	Normally Closed to pin BD2 Normally Open to pin BE2 Common to ground	Pin BD2 to ground Pin BE2 no connection
SS	Normally Closed to pin BF1 Normally Open to pin BH1 Common to ground	Pin BF1 to ground Pin BH1 no connection
PWR CLR	Normally Closed to pin BH2 Normally Open to pin BJ2 Common to ground	Pin BH2 to ground Pin BJ2 no connection

TEST Inputs
The TEST inputs (pins AS2 and AR2) must be tied to a High source when not being used.

M7333
DUAL SERIAL INTERFACE CONNECTOR

RTM

Length: Extended
Height: Single
Width: Single



The M7333 Dual Serial Interface Connector Module provides interface connections between one or two 20 mA current loop devices and their associated M7313 Bidirectional Serial Interface Modules. An M7333 module is not essential for operation of either one or two M7313 modules; however, it is useful when frequent baud rate and/or word format changes are required.

The M7333 module provides two 12-09340-00 (Mate-N-Lok) connectors, J1 and J2, for connecting the serial current loop devices (Teletype®, LA36, VT50, or other asynchronous serial current loop devices) to their respective M7313 modules. The 12-09340-00 connectors mate with 12-09340-01 (Mate-N-Lok) cable connectors. Split-lug terminals on the M7333 provide easy jumpering capability for setting the transmit/receive baud rate, the number of stop bits to be appended to each character, and the number of data bits in each character. Refer to SPECIAL WIRING AND ADJUSTMENTS.

The M7313 Bidirectional Serial Interface Module description and data sheet provide detailed instructions for selecting clock inputs to obtain the desired receive/transmit baud rates, selecting the number of appended stop bits, and selecting the number of data bits in each character.

SPECIAL WIRING AND ADJUSTMENTS

The transmit/receive baud rate, number of stop bits and number of data bits of the transmitted and received data words must be configured so as to make the M7313 module compatible with the external serial device. The M7333 module allows these adjustments to be made with wire jumpers rather than with backplane wiring.

Clock Input

The serial transmit/receive baud rate depends on the signal applied to the M7313 module CLOCK INPUT. The CLOCK INPUT rate must be 16 times the desired baud rate. The M7333 module contains split-lug terminals that permit easy installation of jumpers to select the desired baud rate. (See the functional diagram.) Use uninsulated, solid, 22 AWG wire and connect a jumper between the two split-lug terminals associated with the desired standard baud rate (110, 150, 300, 600, 1200, or 2400) for INTERFACE 1. Repeat the procedure for INTERFACE 2 as required.

Stop Bit Control

The number of stop bits contained in each transmitted or received serial character depends on the M7313 module stop bit CONTROL input, SB. If this input is High, the word format will contain two stop bits; if it is Low, the word format will contain one stop bit. Refer to the literature for the external serial device to determine the proper format. The M7333 module contains split-lug terminals that permit easy installation of jumpers to select the desired number of stop bits. (See the functional diagram.) If one stop bit is desired, use uninsulated, solid, 22 AWG wire and connect a jumper between the two SB split-lug terminals for INTERFACE 1. If two stop bits are required, do not connect a jumper between these two split-lug terminals. Repeat this procedure for INTERFACE 2 as required.

Data Bit Control

The number of data bits, from 5 to 8, contained in each serial character depends on the M7313 module data bit CONTROL inputs, DB1 and DB2. The M7333 module contains split-lug terminals that permit easy installation of jumpers to select the desired number of data bits. (See the functional diagram.) If 5 data bits are desired for each character, use uninsulated, solid,

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22 AWG wire and connect jumpers between the two DB1 and the two DB2 split-lug terminals for INTERFACE 1. If 6 data bits are desired, connect a jumper between the two DB2 split-lug terminals for INTERFACE 1. If 7 data bits are desired, connect a jumper between the two DB1 split-lug terminals for INTERFACE 1. If 8 data bits are desired, do not connect jumpers between any of the split-lug terminals for INTERFACE 1. Repeat these procedures for INTERFACE 2 as required.

20 mA Current Loop Device Connection

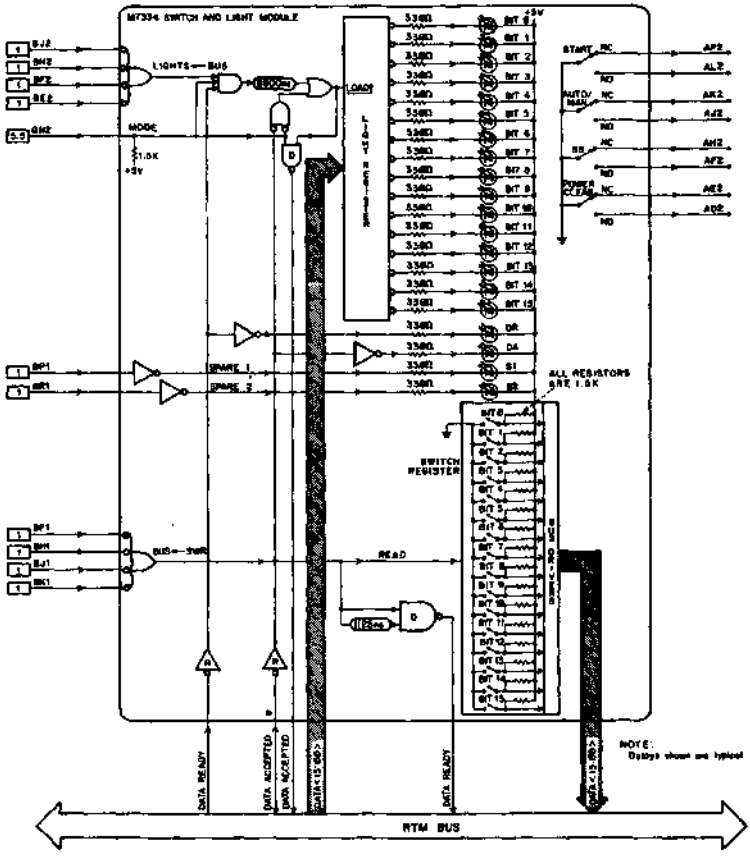
Connect the male 12-09340-01 (Mate-N-Lok) plug connector on the first 20 mA current loop device input/output cable to the female 12-09340-00 (Mate-N-Lok) receptacle connector J1 on the M7333 module. Connect the male 12-09340-01 (Mate-N-Lok) plug connector on the second 20 mA current loop device input/output cable to the female 12-09340-00 (Mate-N-Lok) receptacle connector J2 on the M7333 module as required. (See the functional diagram.)

+DATA IN, —DATA IN, +DATA OUT, —DATA OUT, and READER ENABLE signals are described in the M7313 Bidirectional Serial Interface Module description and data sheet.

M7334
SWITCH AND LIGHT MODULE

RTM

Length: Extended
Height: Double
Width: Single



Volts	mA (typ)	Pins
+5	650	AA2, BA2
GND		AC2, BC2, AT1, BT1

The M7334 Switch and Light Module contains a 16-bit Light register (destination register), 16 Light-Emitting Diode (LED) indicators that display the state of each bit and a 16-bit data source that will place information contained in 16 switches (BIT<15:00>) onto the RTM (DATA<15:00>) Bus. The M7334 module also contains four single-pole, double-throw switches, identified as START, AUTO/MAN, SINGLE STEP (SS), and POWER CLEAR. These switches can be connected to switch inputs on the M7332 Bus Monitor and Terminator Module. The START, AUTO/MAN, and SINGLE STEP (SS) switches can be connected to switch inputs on the M7304 Bus Sense Module. This module can be used as a programmer's console for an RTM system during debugging and maintenance procedures to test for correct data and to identify and isolate inoperative register bits.

Inputs

LIGHTS←BUS—When this input is evoked and when the MODE input is High, the Light register is loaded with parallel data (DATA <15:00>) from the RTM Bus 800 ns (typical) after DATA READY is asserted. The combination of LIGHTS←BUS and MODE, and the received DATA READY cause DATA ACCEPTED to be asserted Low. The contents of the Light register are visually displayed on LED indicators BIT<15:00>. (Refer to LED Displays paragraph.)

MODE—When this input is High, the Light register can be evoked as a data destination with the LIGHTS←BUS input. When the MODE input is Low, the Light register will be automatically loaded each time the DATA ACCEPTED signal appears on the Bus. This automatic loading feature gives a visual indication, on LED indicators BIT<15:00>, of the data that is transferred during each step of a program while single-stepping.

SPARE 1 and SPARE 2—These input lines may be used to monitor additional signals, including Bus lines, within the RTM system.

BUS←SWR—When this input is evoked, the contents (DATA <15:00>) of the Switch register are driven onto the RTM Bus. After a 25 ns (typical) delay, DATA READY is asserted.

LED Displays

BIT<15:00>—These LED indicators display the status of the Light register. A Binary One in the corresponding bit position of the Light register causes an LED to light.

DR—This LED indicator displays the status of the DATA Ready Bus line. The LED is turned on when DATA ACCEPTED is asserted.

DA—This LED indicator displays the status of the Data Accepted Bus line. The LED is turned on when DATA ACCEPTED is asserted.

S1 and S2—These LED indicators display the status of the SPARE 1 and SPARE 2 input lines. The LEDs are turned on when their respective input lines are High.

Switches

BIT<15:00>—Data words can be entered into the RTM system via these switches by making these Switch register switches a data source. When the white dot on a switch is visible, that switch is set to produce a Binary One. The data word (DATA<15:00>) represented by these switches can be driven onto the RTM Bus by evoking the BUS ← SWR input.

START—This switch can be used to provide a START (FIRST EVOKE) signal for an RTM system. This switch is in the START position (pin AL2 grounded)

when the white dot is visible. The switch is generally connected to the NORM/START inputs of an M7304 or the M7332 module. To produce a START (FIRST EVOKE) signal, this switch must be set to START (N.C.) then back to N.O.

A/M (AUTO/MAN)—This switch can be used in conjunction with the AUTO/MAN inputs of an M7304 or M7332 module to put the RTM system into the single-step mode. The white dot is visible when this switch is in the MAN position. When the switch is in the AUTO position (pin AK2 grounded), automatic operation is selected; when it is in the MAN position (pin AJ2 grounded), single-step operation is selected.

SS (SINGLE STEP)—This switch can be used in conjunction with the SINGLE STEP inputs of an M7304 or M7332 module to single-step an RTM program. The white dot is visible when this switch is in the N.O. position. Each time the switch is moved to the N.O. position (pin AF2 grounded) and then back to the N.C. position (pin AH2 grounded), the RTM system will execute one instruction.

PC (POWER CLEAR)—This switch can be used in conjunction with an M7332 module to assert the LOW initializing POWER CLEAR signal anytime after power-up of the RTM system. The POWER CLEAR signal is an RTM Bus signal that sets the logic circuitry components on the RTM modules to a specific, known state. The POWER CLEAR Bus line will go Low when the switch is placed in the N.O. position with the white dot visible (pin AD2 grounded) and will remain Low until the switch is returned to the N.C. position (pin AE2 grounded).

RTM Bus

DATA<15:00>, DATA READY, and DATA ACCEPTED are described in the M7332 Bus Monitor and Terminator Module description.

The M7334 module is supplied with two 3-foot cables (DEC P/N 70-02222-03). These cables allow the module to be located outside of an RTM mounting enclosure to facilitate access to the switches and indicators.

Program Control Sequencer Control

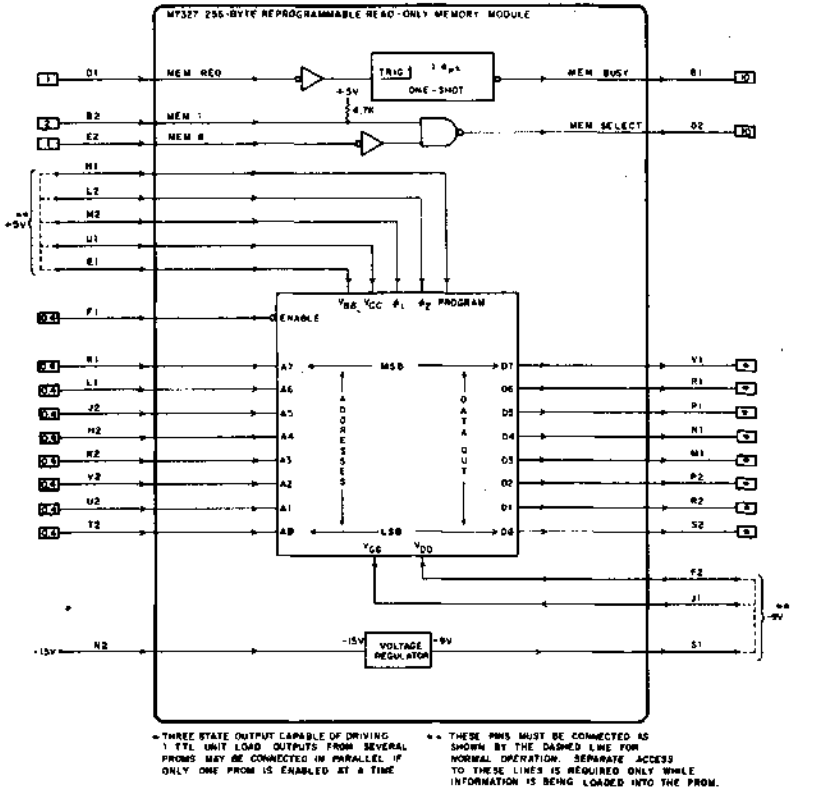
The Program Control Sequencer (PCS) control section is best used in a control system that requires longer programs or periodic, or even frequent, programming changes. This memory-stored program provides reprogramming convenience and, in addition, the advantages of the RTM concept (low-cost, quick design time, and custom-design convenience).

The following module descriptions pertain to PCS-related modules. In addition to these modules, an M7332 Bus Monitor and Terminator Module is required for PCS-based systems.

M7327
256-BYTE REPROGRAMMABLE READ-ONLY MEMORY

RTM

Length: Extended
Height: Single
Width: Single



Volts	mA (typ)	Pins
+5	175	A2
−15	160	N2
GND		C2, T1

The M7327 256-Byte Reprogrammable Read-Only Memory Module is the standard control memory module for a memory-controlled RTM system. It also provides a convenient way to store 8-bit or, with two memories in parallel, 16-bit data constants, such as code conversion tables, text, or numeric data.

A memory-controlled RTM system that uses an M7336 512 PCS module must have an 8-bit code assigned to each source/destination register pair required to perform the desired data transfer operation. A list of these codes stored in the M7327 module constitutes the program that the system will execute. A PCS module fetches, decodes, and executes each instruction in the proper order. Thus, program changes can be made by changing the contents of the control memory, rather than by rewiring.

The contents of the M7327 module memory can be erased with high intensity ultra-violet light and reprogrammed electrically if program changes are desired, but its contents are not affected by noise or power disturbances. This module uses either an INTEL 1702 or an INTEL 1702A Programmable Read-Only Memory (PROM). Programming can be done by Digital Equipment Corporation, and the programmed modules will be factory-tested before shipment. If the user desires to take advantage of this programming service, he should follow the procedures described in the *Register Transfer Modules* handbook for submitting his program to Digital Equipment Corporation. The data sheet for the 1702 PROM, published by INTEL, describes in detail a manual, hand-operated programmer that can be constructed by the user. All of the pins on the PROM are accessible through the module pins.

The M7327 contains a memory select circuit that allows an individual memory to be selectively enabled when two or more of the memories are combined to provide 512 or more control memory locations.

Inputs

MEM REQ—This input comes from the M7336 Program Control Sequencer (PCS) Module and causes the one-shot multivibrator to assert MEM BUSY for 1.4 μs whenever the memory address is changed.

MEM 1—If this M7327 module is designated Memory 1, this input is tied to the memory selection output (PC8) of the M7336 PCS module; the MEM 0 input is tied Low so that a High on MEM 1 will assert MEM SELECT.

MEM 0—If this M7327 module is designated Memory 0, this input is tied to the memory selection output (PC8) of the PCS module; the MEM 1 input may be unconnected (left floating) so that a Low on MEM 0 will assert MEM SELECT.

ENABLE—This input is tied to the MEM SELECT output of this M7327 module and is asserted Low when this M7327 is designated as the addressed memory.

A<7:0>—These inputs from the M7336 PCS module contain the address of a memory location containing the desired information.

−15 V—This input, from a −15 V power supply, may be used to produce the −9 V required by the 1702 or 1702A PROM (i.e., V_{GG} and V_{CC}).

V_{BB}, V_{CC}, $\phi 1$, $\phi 2$, and PROGRAM—During normal operation these inputs must all be tied to +5 V. Individual access is required only while the PROM is being programmed (loaded with data).

Outputs

MEM BUSY—This output is asserted Low when MEM REQ triggers the one-shot, and remains asserted for 1.4 μs to stop the clock in the PCS module for that period, allowing time for the memory data to settle.

MEM SELECT—This output is asserted Low when the MEM 1 and MEM 0 inputs are connected so as to select this M7327 module as the addressed memory. This MEM SELECT output is tied to the ENABLE input of this module.

D<7:0>—These parallel outputs transmit the contents of the addressed memory location to the M7336 PCS module. They are three-state outputs capable of driving 1 TTL unit load, and may be OR-tied in parallel for memory expansion as long as only one M7327 module is enabled at a time.

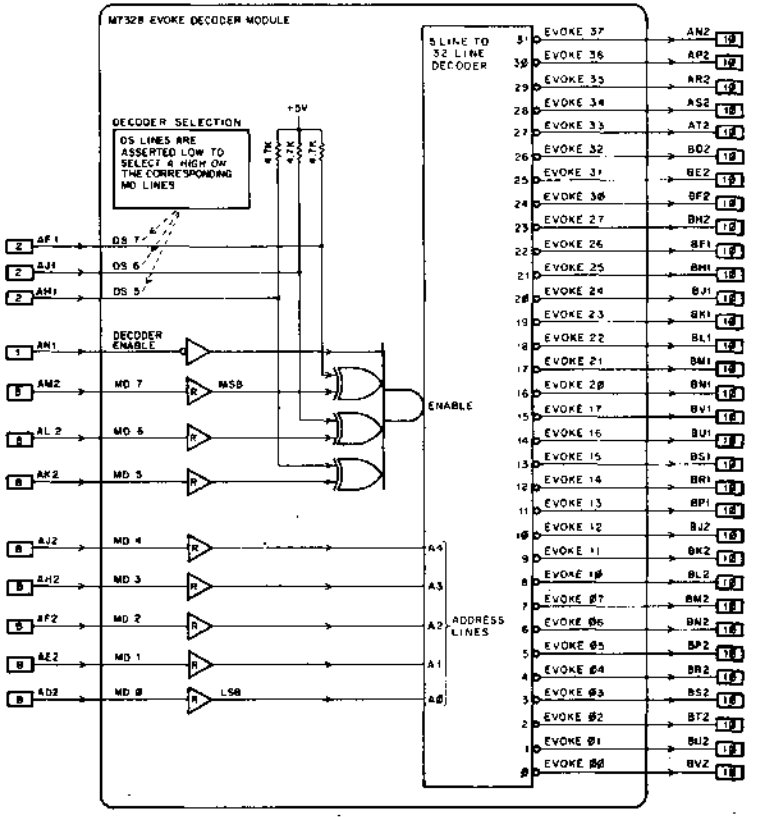
The three-state outputs D<7:0> present either the normal memory contents or go to a third (high-impedance) state. In this state all output transistors are turned off. The output may, therefore, be OR-tied in parallel for memory expansion. Normal TTL outputs cannot be OR-tied because of the excessive output current which one device would have to sink from the others. If, however, all the output transistors in all but one of the connected devices are turned off, then the one remaining device in the normal low-impedance state (normal memory contents) will have to sink from or supply to the other devices only a small amount of leakage current.

−9 V—This output may be used to supply the 1702 or 1702A PROM V_{GG} and V_{DD} inputs when −15 V is supplied to pin N2.

M7328
EVOKE DECODER

RTM

Length: Extended
Height: Double
Width: Single



Volts	mA (typ)	Pins
+5	185	AA2, BA2
GND		AC2, BC2, AT1, BT1

The M7328 Evoke Decoder Module decodes the low 5 bits of the 8-bit evoke operation codes (LET instructions) used in M7336 PCS-controlled RTM systems. The Evoke outputs, like the outputs of the M7310 Evoke Units Module, become the Evoke signals that cause data transfers to occur between source and destination registers in the functional module portion of the system. However, the sequence of the Evoke signals issued by an M7328 module depends upon the data in a control memory. Before an M7328 can issue an Evoke, it must be selected and enabled. Evoke signal capacity can be increased by adding additional M7328 modules.

Each M7328 module contains a 5-line-to-32-line decoder that asserts a discrete output line for each of the 32 possible combinations of the 5 least significant bits of the 8-bit LET instruction code. The remaining 3 bits contain the module selection code that determines which M7328 is selected.

Inputs

DS7, DS6, and DS5—These lines are configured on the backplane by the user to the complement of the desired module selection code. Thus, a Low on one of these lines will select a High on the corresponding MD7, MD6, or MD5 input.

DECODER ENABLE—This signal is asserted Low by the Program Control Sequencer (PCS) module during the execution of a LET instruction. If the code contained in MD7, MD6, and MD5 is the complement of the code configured on the backplane for DS7, DS6, and DS5, the result is ANDed with DECODER ENABLE to enable an EVOKE signal from the selected output of this particular M7328 module.

MD7, MD6, and MD5—These three bits of the LET instruction contain the selection code that identifies the decoder being addressed. They are XORed with DS7, DS6, and DS5 to select the M7328 to be enabled.

MD4, MD3, MD2, MD1, and MD0—These five bits of the LET instruction are decoded by the 5-line-to-32-line decoder to select one of the 32 possible outputs, each of which represents a potential data transfer (Evoke) operation.

Outputs

Signals <31:00>—Each of these outputs (EVOKE $<37:00>_8$) is a discrete EVOKE output capable of initiating a source/destination data transfer.

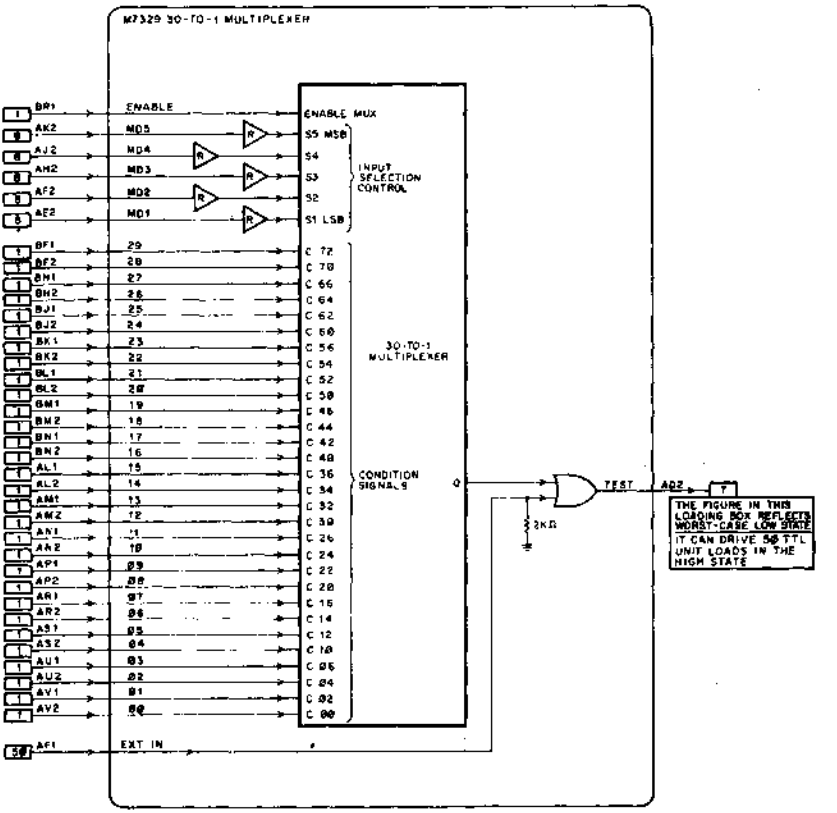
SPECIAL WIRING AND ADJUSTMENTS

When wiring the backplane for DS7, DS6, ano DS5, it is only necessary to ground those lines desired to be Low. Internal resistors will pull the other DS lines High. Wiring the backplane rather than the module itself makes the module selection code socket-dependent, rather than module-dependent, so that any M7328 module placed in a given socket will respond in the same manner as any other M7328. The DS lines must be wired to the complement of the code to which the individual socket is desired to respond. Thus, a Low on one of the DS lines will select a High on the corresponding MD line.

M7329
30-to-1 MULTIPLEXER

RTM

Length: Extended
Height: Double
Width: Single



Volts	mA (typ)	Pins
+5	160	AA2, BA2
GND		AC2, BC2, AT1, BT1

The M7329 30-to-1 Multiplexer Module can be used to monitor up to 30 external condition inputs so that any one may be selected to be applied to the TEST output. A principal RTM system use of the M7329 is in conjunction with an M7336 Program Control Sequencer (PCS) Module to select the condition inputs to the IF instruction of a memory-controled RTM system. IF instructions are the conditional branch codes that cause a branch only if

the associated status condition input is High (True). Tying one of the condition inputs (usually 00) permanently High will cause an effective GOTO instruction to be executed whenever that input is addressed, which provides the useful unconditional jump capability. In this special case, the IF condition will always be True.

If it is desirable to monitor more than 30 condition inputs, two or more additional M7329 modules can be used by selectively enabling only one at a time with either flags or branch units, making it possible for the same LET instructions to apply to different sets of status input signals.

Inputs

ENABLE MUX—When this input is asserted High, this 30-to-1 multiplexer is enabled.

MD<5:1>—These five inputs receive the binary code that determines which condition input signal, 00 through 29 (C<00:72>$_s$), will be selected and routed to the TEST output. The selection is based on the following table:

SELECT Inputs					CONDITION Signal Selected	
MD5	MD4	MD3	MD2	MD1		
0	0	0	0	0	0	(C00$_s$)
0	0	0	0	1	1	(C02$_s$)
0	0	0	1	0	2	(C04$_s$)
0	0	0	1	1	3	(C06$_s$)
0	0	1	0	0	4	(C10$_s$)
0	0	1	0	1	5	(C12$_s$)
0	0	1	1	0	6	(C14$_s$)
0	0	1	1	1	7	(C16$_s$)
0	1	0	0	0	8	(C20$_s$)
0	1	0	0	1	9	(C22$_s$)
0	1	0	1	0	10	(C24$_s$)
0	1	0	1	1	11	(C26$_s$)
0	1	1	0	0	12	(C30$_s$)
0	1	1	0	1	13	(C32$_s$)
0	1	1	1	0	14	(C34$_s$)
0	1	1	1	1	15	(C36$_s$)
1	0	0	0	0	16	(C40$_s$)
1	0	0	0	1	17	(C42$_s$)
1	0	0	1	0	18	(C44$_s$)
1	0	0	1	1	19	(C46$_s$)
1	0	1	0	0	20	(C50$_s$)
1	0	1	0	1	21	(C52$_s$)
1	0	1	1	0	22	(C54$_s$)
1	0	1	1	1	23	(C56$_s$)
1	1	0	0	0	24	(C60$_s$)
1	1	0	0	1	25	(C62$_s$)
1	1	0	1	0	26	(C64$_s$)
1	1	0	1	1	27	(C66$_s$)
1	1	1	0	0	28	(C70$_s$)
1	1	1	0	1	29	(C72$_s$)
1	1	1	1	0	NONE	NONE
1	1	1	1	1	NONE	NONE

CONDITION SIGNALS <00:29> (C<00:72>$_s$)—These inputs receive the condition inputs of individual data sources.

EXT IN—This input allows the output of this M7329 to be ORed with the output of one other M7329 module. Thus, the second one added to an RTM system is ORed with the first, the third is ORed with the second, and so on. This multiple status signal multiplexing technique can be extended to include as many M7329 modules as desired, as long as only one M7329 is enabled at a time. If this input is not used, the user is not required to connect it to ground. An internal 2K pull-down resistor inhibits this input when not used. However, when this input is driven, the driving signal must be able to drive 50 TTL unit loads in the High state. The TEST output from another M7329 module can drive this input.

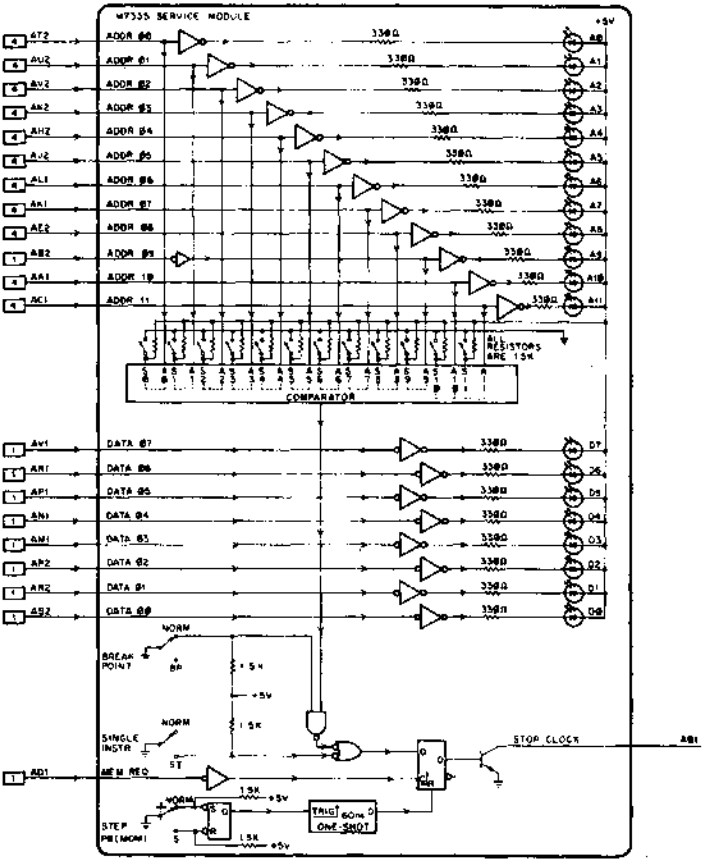
Outputs

TEST—This output carries the status of the selected condition input signal for testing. Although this output can only drive 7 TTL unit loads Low, it can drive 50 TTL unit loads High. This output is usually connected to the CONDITION input of an M7336 PCS Module or the EXT IN input of another M7329.

M7335
SERVICE MODULE

RTM

Length: Extended
Height: Double
Width: Double



Volts	mA (typ)	Pins
+5	500	AA2, BA2
GND		AC2, BC2, AT1, BT1

The M7335 Service Module provides Light-Emitting Diode (LED) indicators for visually monitoring the control memory data in a Programmed Control Sequencer (PCS) controlled RTM system. The module monitors 8 memory data lines and up to 12 address lines and displays the code of the instruction being performed and the contents of that address via LED indicators. There is a LED indicator associated with and dedicated to each memory data line and each address line.

Twelve address switches labeled A0 through A11 provide a break-point capability that allows a program to be stopped at any specific instruction. All switches are asserted to binary Ones when the white dots on the switches are visible.

In addition to the LEDs and address switches, the M7335 module contains a STEP (single-step) switch, an SI (single-instruction) switch, and a BP (break-point) switch.

This module also generates and issues the STOP CLOCK signal to the PCS module when the program has progressed to the specific desired address.

Inputs

ADDR<07:00>—These bits are the memory address of the instruction that is being executed. The LEDs representing these bits display the memory address.

ADDR<11:08>—These bits are not normally used with the M7336 512 Program Control Sequencer Module. Notice that ADDR<09> has an extra inverter.

DATA<07:00>—These bits are the code of the instruction being performed. The LEDs representing these bits display the address location.

BP (BREAK POINT)—This switch can be used to halt the RTM system program at any desired address without having to single-step through the program to that point. When the desired stop address is programmed by setting switches <A11:A0>, the BP switch can be asserted (white dot showing). Then when the system is started the program will automatically run until it reaches the break point, where it will halt. The selected address must contain an instruction being performed by the program. Locations containing jump addresses or HALT commands should not be used as break points.

SI (SINGLE INSTRUCTION)—Asserting this switch (white dot showing) and producing a START (FIRST EVOKE) signal with the M7334 Switch and Light Module START switch permits single-stepping through the program by using the STEP switch. When the SI switch is unasserted and the STEP switch is pressed and released, the program will return to the auto run mode, or may be restarted at the beginning by pressing the START switch of the M7334.

SS (SINGLE STEP)—Pressing and releasing this switch when the SI switch is asserted and a START pulse has been generated (as described above) causes the RTM system to single-step through the program. The LED indicators on the M7335 module will display the address and the instruction code. The data that is transferred during each LET instruction may be observed with an M7322 Bus Indicator Module. Pressing and releasing the STEP switch when the SI switch is unasserted causes the program to return to the auto run mode.

MEM REQ—When this input goes Low the Stop-Clock flip-flop is clocked. If switch S1 is asserted (white dot showing) or if switch BP is asserted (white dot showing) and if the comparator output is High (i.e., program has progressed to switch settings), STOP CLOCK will be asserted Low. The MEM REQ input is usually from the M7336 512 Program Control Sequencer Module.

Outputs

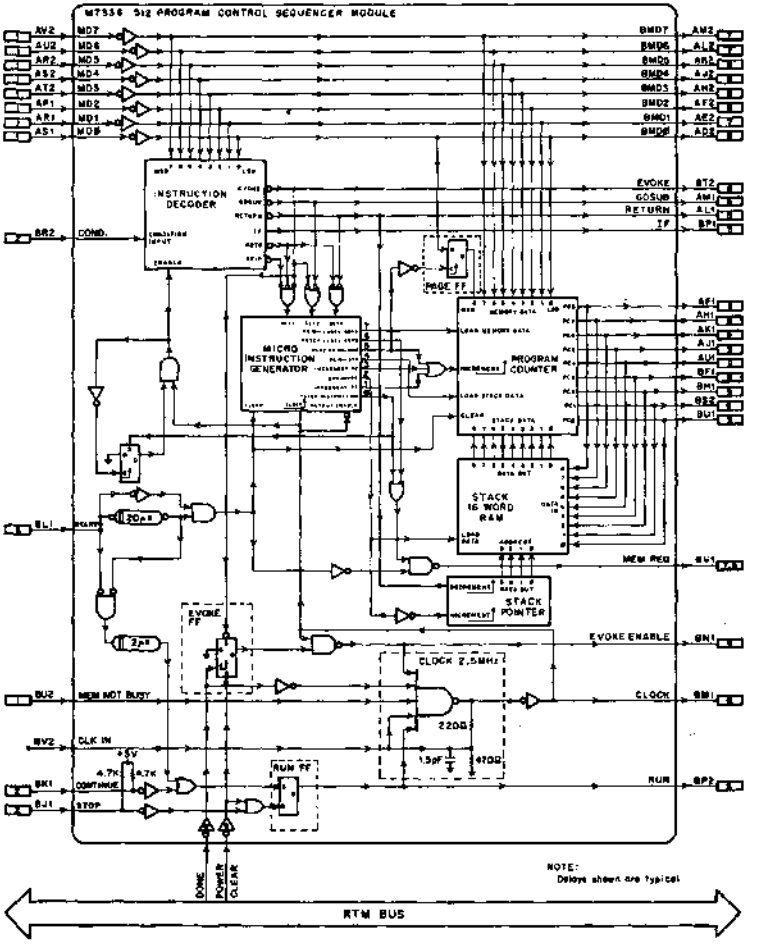
STOP CLOCK—This output is usually applied to the M7336 512 Program Control Sequencer Module. When STOP CLOCK is unasserted High the M7336 Clock runs and the program is automatically stepped through each instruction. When STOP CLOCK is asserted Low (refer to MEM REQ, Input paragraph), the M7336 Clock is stopped.

All other outputs from this module are visually displayed by LED indicators and are described in the Inputs paragraph.

M7336
512 PROGRAM CONTROL SEQUENCER

RTM

Length: Extended
Height: Double
Width: Single



Volts	mA (typ)	Pins
+5	500	AA2, BA2
GND		AC2, BC2, AT1, BT1

The M7336 512 Program Control Sequencer (PCS) Module performs the majority of the system control functions that are required in a memory controlled RTM system. It contains the Program Counter and the logic (the Instruction Decoder, the Microinstruction Generator, the Return Address Stack and Stack Pointer, and a Clock, and Page, Run, and Evoke flip-flops) necessary to decode each instruction and perform all of the intermediate steps that are required to execute it.

Program Counter—The Program Counter has an output of 9 bits and can, therefore, count up to 512, making it possible to address all of the locations on two M7327 256-Byte Reprogrammable Read-Only Memory Modules. If a larger program is desired, the M7336 is able to implement a paging scheme that will permit the use of more control memory modules.

Instruction Decoder—The Instruction Decoder accepts the instruction from the control memory module and determines whether it is a LET (EVOKE), GOSUB, RETURN, IF, or GOTO instruction. It instructs the Microinstruction Generator accordingly as to what microinstructions should be performed.

If the instruction is a LET (EVOKE), the PCS enables the M7328 Evoke Decoder Module(s) so that the proper Evoke signal is issued to the data transfer modules. If the instruction is a GOSUB, RETURN, IF, or GOTO instruction, the PCS performs all of the internal steps required, such as incrementing the Program Counter, fetching the next word to form a branch address, storing the old program count, or testing the status inputs from the status multiplexer module.

Microinstruction Generator—The Microinstruction Generator consists of a 3-bit counter and a decoder which define the chain of operations to be performed by the PCS module to execute an instruction. The 3-bit counter is preset by the Instruction Decoder to determine its starting state according to the type of instruction that has been decoded. The decoder produces control signals (based on counter data) to perform such operations as loading the Program Counter, reading the memory, incrementing the Program Counter, etc. Thus, each type of instruction includes a number and sequence of states. (See Figure 1.) During State 0, the clock halts until the control memory has delivered data, the instruction is decoded, and the appropriate starting state is loaded into the 3-bit counter. During State 1, the Program Counter is incremented. During State 2, the value of the Program Counter is stored in the Stack and the Stack Pointer is incremented. During State 3, the Program Counter is incremented. During State 4, the contents of the Stack are transferred to the Program Counter. During State 5, the Program Counter is incremented. At the end of State 5, the Page flip-flop is loaded with the LSB of the control data. During State 6, control data is requested from the control memory. The control memory halts the PCS clock until it has delivered the new data. During State 7, the Program Counter is loaded with the control memory data and the contents of the Page flip-flop. The Page bit becomes the MSB of the Program Counter.

Sack—The Stack is a small random-access memory used to save the value of the Program Counter when a subroutine is entered. It contains sixteen 9-bit locations, so that it is possible to call up to 16 subroutines before a return is necessary.

Stack Pointer—The Stack Pointer comprises a 4-bit counter that provides the address for writing into or reading from the Stack. It is incremented by the Microinstruction Generator after a return address is loaded into the Stack, so that it indicates (points to) the next empty location. It is decre-

mented before a return address is read, so that it addresses the last return address loaded. Thus, it is a Last In, First Out (LIFO) type of memory.

Clock—The Clock is a free-running multivibrator used to step the Microinstruction Generator through the various states for each instruction. It is stopped during a transfer operation, and also after the Program Counter changes to permit memory data to settle.

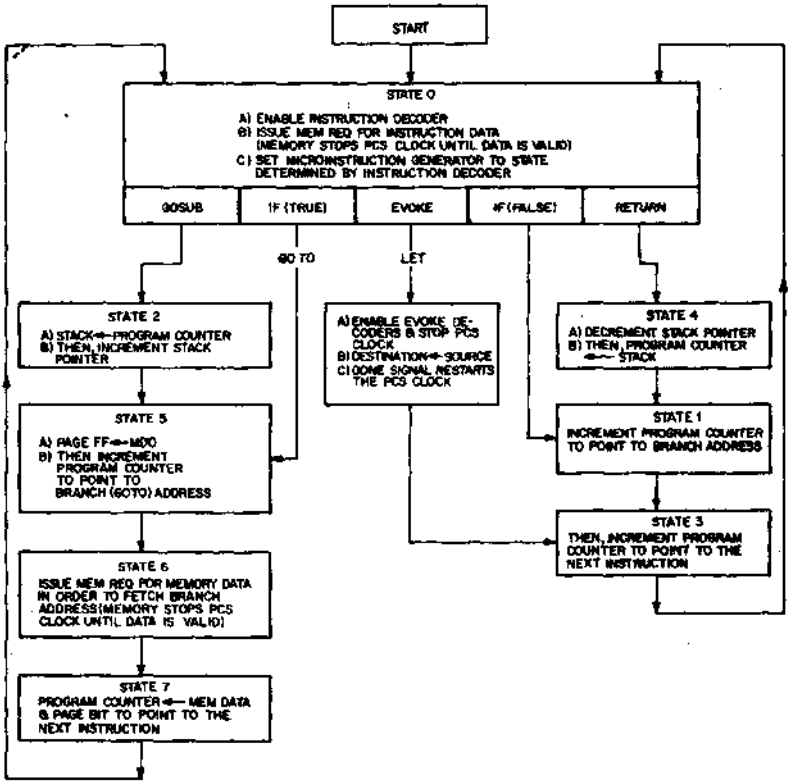


Figure 1. Microinstruction Generator State Diagram

Inputs

MD<7:00>—These are the control memory data lines containing either the instruction code or a branch address.

CONDITION—This input from the M7329 30-to-1 Multiplexer Module indicates whether an IF instruction is True (High) or False (Low). If it is High, the GOTO instruction sequence is performed; if it is Low, the PCS proceeds to the next instruction in the control memory.

START—A Low at this input clears the Microinstruction Generator and the Program Counter and begins program execution by setting the Run flip-flop.

MEM NOT BUSY—This input goes Low when the control memory asserts MEM BUSY, and stops the clock until MEM BUSY is unasserted.

CLK IN—When this input is pulled Low, the clock stops. This input is usually controlled only by the open-collector break-point output (called STOP CLOCK) of the M7335 Service Module. The CLK IN input must be driven by an open-collector output device.

CONTINUE—A Low at this input turns on the Run flip-flop.

STOP—A Low at this input turns off the Run flip-flop.

Outputs

BMD<7:0>—These outputs are the buffered memory data lines used to drive the address inputs of M7328 Evoke Decoder Modules and M7329 30-to-1 Multiplexer Modules. If the instruction is an Evoke, the evoke decoders are enabled. The M7329 modules are constantly enabled and the BMD<5:1> bits contain the binary code used to select the IF condition. The multiplexer output is connected to the M7336 CONDITION input so that it can be tested during the IF instruction execution.

EVOKE—This output is asserted if the instruction received from control memory is an Evoke instruction. This signal is available for test purposes only.

GOSUB—This output is asserted if the instruction received from control memory is a GOSUB instruction; it causes the value of the Program Counter to be saved on the Stack. GOSUB instructions cause a branch to a subroutine. Except for the Program Counter value being saved in the Stack, the microinstruction procedure is the same for a GOSUB and a GOTO. GOSUBs may be nested to a depth of 16. This signal is available for test purposes only.

RETURN—This output is asserted at the end of each subroutine to cause a return to the instruction in the main program at the Program Counter location being saved in the Stack. It also decrements the Stack Pointer before a return address is read from the Stack and loaded into the Program Counter. This signal is available for test purposes only.

IF—This output is asserted if the instruction received from control memory is one of the 29 conditional branch codes, called IF instructions, that will cause a branch only if an associated status condition input signal is True (High). An M7329 module receives and samples the 29 status signals when the instruction is decoded, and uses bits 1—5 of the instruction to identify the input associated with a particular IF instruction. The branch address for the IF instructions is located in the memory location that follows the IF instruction. A true CONDITION input will cause the LSB of the instruction to be combined with the following word to form a 9-bit branch address. This signal is available for test purposes only.

PC8—This output selects Memory 1 when High and Memory 0 when Low (when two control memories are used).

PC<7:0>—These ouputs are the control memory address signals; they should be connected to the eight address inputs of the control memory module (or to both memories, if two are used).

MEM REQ—This output is asserted to request data from the control memory. When connected to the M7327 module, it triggers a 1.4 μs one-shot that generates a pulse that is returned to the M7336 at the MEM NOT BUSY input to stop the clock during the time the memory is fetching the next word to form a branch address and to allow the memory data to settle on the lines.

EVOKE ENABLE—This output is asserted Low when the instruction received by the Instruction Decoder is an Evoke and the Clock has disabled the Instruction Decoder. The EVOKE ENABLE signal is used to enable all evoke decoder modules.

CLOCK—This is the Clock output that is available on a module pin for test purposes only.

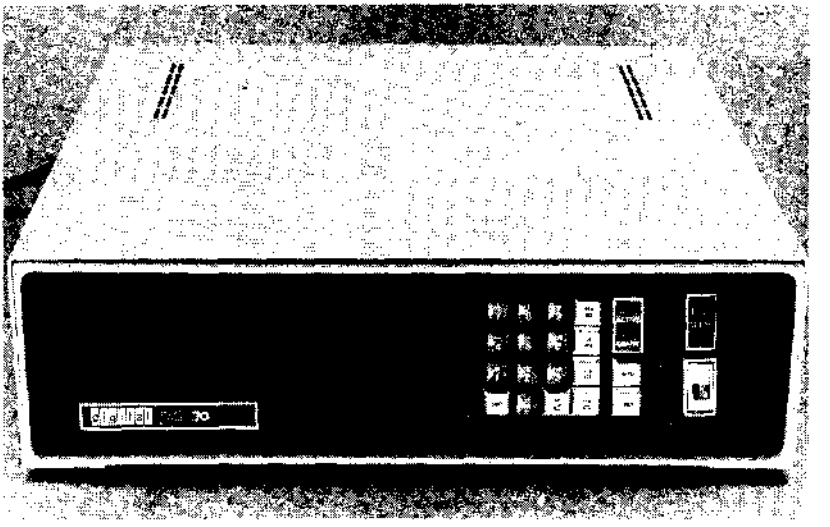
RUN—This output allows the user to monitor the status of the Run flip-flop.

RTM Bus

POWER CLEAR and DONE are described in the M7332 Bus Monitor and Terminator Module description.

data entry terminals

PDM70
PROGRAMMABLE DATA MOVER



The PDM70 Programmable Data Mover is a custom configured, modular data acquisition and transmission device. Capable of either stand-alone or computer-controlled operation, the PDM70 controls the signal conditioning, timing, and sequencing of a wide variety of input and output signals. An optional 16-pad keyboard and 32-character display allow the user to locally input program commands and view displayed data. Programs are simple and may be written and entered by noncomputer-skilled personnel (typical programming time is about 20 minutes).

A library of eight input/output module options is offered which may be plugged into the PDM70 in virtually any configuration to allow custom tailoring to meet a wide range of applications. Two application examples are provided later in this section. The PDM70 is organized as follows:

Basic Unit:

PDM70-A — Provides its own keyboard for entering program commands. Consists of mounting box, power supply, clocks, and a 16-pad keyboard.

PDM70-B — Identical to model PDM70-A, but with added capability of a front-panel-mounted, 32-character, alphanumeric display.

PDM70-C — Features no keyboard or display. Internal program entered by user's keyboard device, PROM read-in module, or by a remote computer. Consists of mounting box, power supply, and clocks.

Control Options:
One of the following two control options is required with PDM70 Models -A, -B, and -C.

Programmable Control (PDM70-P)—Used with stand-alone systems for controlling the internal operations of the PDM70, this option features a 64-character, first-in-first-out (FIFO) buffer which stores the user's program. An additional option offered with this control is the PROM read-in module (PDM70-N) which is used to deposit a fixed program in the PDM70-P at start-up.

Direct Serial Bus Interface (PDM70-R)—Used to provide access to a computer-controlled program, this option contains a 20 mA current loop facility to allow communication with a remote computer.

Input/Output Options:
The following I/O options are truly optional; the customer can order any mix of these options as required. Up to seven I/O options can be plugged into the PDM70-A or PDM70-B. The PDM70-C can accept up to eight I/O options.

Designation	Function	Typical Application
PDM70-D	BCD/Binary Input (32 bits)	DVM or counter input
PDM70-E	BCD/Binary Output (32 bits)	Programmable power supplies or signal generators
PDM70-F	4-Channel Differential Analog Input	RC bridges, thermocouples
PDM70-H	2-Channel Analog Output	X-Y recorders, storage scopes
PDM70-J	Bit Serial Input/Output	20 mA current and EIA levels to or from PDM70
PDM70-M	8-Bit Parallel Input/Output	Tape reader input; parallel printer output
PDM70-JR	Bit Serial Input/Output for unattended, remote operation (includes abort timer)	20 mA and EIA levels; choice of delimiter characters
PDM70-SD	Foundation Module	Allows user to construct unique PDM70 I/O interface, such as a multiplexer for terminals

BCD/Binary Input Option (PDM70-D)—provides the ability to accept eight BCD digits (32 bits) of TTL information from an external source peripheral and transmit the data in an ASCII format to the internal bus. Featured on the module is a 32-bit full flip-flop type register that provides buffering capabilities. The basic operation is to load the eight BCD digits from the peripheral into the register. Here, the digits are transferred one at a time to the UART for parallel-to-serial conversion and transmission. Following transmission of the last digit, as detected by the character counter contained on the module, the ASCII character EOT is transmitted to inform the master controller that the data mode operation has been completed. The module, under program control, can operate with either internal or external synchronization.

BCD/Binary Output Option (PDM70-E)—transfers up to eight parallel, BCD digits (32 bits) from the serial R-Bus out to an external peripheral such as a programmable power supply or signal generator. The BCD digits and module address are taken off the serial R-Bus and converted to parallel data by the UART. The data is then converted to BCD format and stored in a 32-bit full flip-flop-type register where it is strobed out to the peripheral. The message length is determined by the Master Controller recognizing an EOT character. Contained on the module are split lugs and switches for adjusting the strobe pulse width and the address decoder.

Analog Input Option (PDM70-F)—converts voltage levels from four differential analog input channels into ASCII characters for transmission to the serial bus. Through program control, the amount of data this module will transmit can be limited to a single channel or a sequential scan of all channels with either internal or external synchronization. Utilizing the latest C/MOS technology, the true throughput rate is 99 * messages per second (random-access method) or 32 ** messages per second when scanning all four channels (sequential-access method). These throughput rates take into account programming time and other system overhead considerations; input impedance is 100 megohms. Pertinent operation specifications are listed in the chart.

Usable Input Range Full Scale	Gain	System Accuracy at 25° C	Resolution	Common Mode Rejection Ratio (dc to 100 Hz) 1 kΩ R. Imbalance	Temperature Coefficient	Internal Offset	External Offset
±1.999 V ±199.9 mV ±19.99 mV	X1 X10 X100	0.05% of Full Scale plus ± one least significant digit or ±30 μV whichever is greater	1 mV 100 μV 10 μV	≥70 dB ≥86 dB ≥100 dB	0.005%/°C of Full Scale referred to the input	Adjustable to zero	Adjustable to ext. voltage
Input impedance at all gains is 100 megohms. Bias current (either input) ± 50 nanoamperes maximum. Common mode voltage ±10 volt maximum.							

Analog Output Option (PDM70-H)—provides two analog output signals from two 3-digit BCD ASCII messages with a resolution of one part in 1000. Included on the module are two D/A converters capable of 0 V to 10 V outputs at 5 mA. The output accuracy is 0.1 percent of full scale ±1/2 LSB.

The module can operate in one of three basic modes: load X channel; load Y channel; or load X and Y channels. In addition, a 20-μs Data Ready pulse is generated by the EOT character for use in Z-axis control required by such devices as the Tektronix Model 611 storage scope or equivalent. For added convenience and versatility, a program-controlled flop signal is provided for functions such as controlling the pen up/pen down motion in an XY plotter.

Serial Input/Output Option (PDM70-J)—serves as both a destination and a source interface that can receive and transmit serial ASCII characters to and from the R- and T-Buses. Typical applications include usage with Teletypewriters, processor interfaces, acoustic modems, and DIGITAL'S RT02 and VT05 terminals. Accordingly, both a TTL-to-20mA current loop converter and an EIA level converter are provided to make the module compatible with the varying types of equipment.

* A message in this case contains the information from a single channel.

** A message in this case contains the information from four channels.

The module contains separate 64-character first-in-first-out (FIFO) buffers for the receive and transmit operating modes. An address decoder identifies independently the source and destination addresses which enable the transmitter and receiver, respectively. An echo feature is provided whereby a message transmitted from a peripheral device can return to that peripheral by addressing the module with both its source and destination in one command.

8-Bit Parallel Input/Option (PDM70-M)—receives and transmits 8-bit parallel characters to and from the R- and T-Buses. The characters received from the serial R-Bus are converted to parallel information by a UART and stored in a first-in-first-out buffer (FIFO) capable of storing 64 words. When the FIFO output is ready, a Data Strobe pulse is generated which causes the first word stored in the FIFO to be transferred to the peripheral device. The external device responds by asserting its Device Ready output which causes the next sequential word to be read from the FIFO. The message length is determined by the master controller recognizing an EOT character. This module is suitable for any device capable of handling 8-bit bytes such as a line printer, terminal, or computer.

Serial Input/Output Option (PDM70-JR)—represents a powerful systems tool for PDM70 applications requiring remote, unattended operation or for use in terminal concentrator systems. This module includes features such as:

- Remote clear capability.
- 64-character message buffering.
- Choice of two delimiter characters to match various software system needs —one fixed and the other variable.
- User-selectable timer to warn host computer of loss of input data to PDM70.
- Direct interface to Bell 103E modem (or equivalent).
- EIA and 20 mA current loop interfaces.
- Control signals for teletypewriter reader/punch.

Data from terminals is more easily handled with the message-buffered serial input. Up to 64 characters of operator-keyed data can be entered from a terminal before the message terminator is entered. This message buffering permits a number of terminals or other devices to operate with the same PDM70 and thus share a common input line to the computer.

The remote clear and selectable time-out features offer safeguards in applications where the PDM70 is unattended. The remote clear permits the host computer to override the program in the PDM70 and brings up a program contained in the PDM70-N Programmable Read-Only Memory option. In a similar manner, the timer will clear the PDM70 program if there has not been an input from a given option in a preselected time period. These features, plus the direct interface to the Bell 103E, simplify connection to the dial-up phone network for unattended data collection systems.

Foundation Option (PDM70-SD)—is both a source and destination module that provides all required logic for interfacing to the PDM70 serial bus. Typical applications for the Foundation Module include customer-built interfaces to tape cassette drives, semiconductor buffer memories, pulse counters, and automatic dialing circuits.

The rear of the module is notched to accept a 44-pin edge card connector to provide a convenient access to external input and output points. In addition, IC mounting pads with wire wrappable pins are made available for custom logic designs. These pads can accommodate either 23 16-pin, or 18 16-pin and 3 24-pin IC's, or 18 16-pin, 2 40-pin, and 1 24-pin IC's. Pins are also provided to interface with the PDM70 logic on the module, the 44-pin connector on the rear of the module, and +5V, ±15V and ground.

All communications between this option and the PDM70 are accomplished serially, under program control, at the system baud rate. All communications between this option and the external pin connections are accomplished in parallel. Eight data lines in, eight data lines out, and the required control signals are provided to accomplish the data transfers.

APPLICATIONS

Example 1:
Problem: The sulfer dioxide concentration must be measured at four locations remote from the main plant and the results transmitted back to a computer at the plant once every hour. It is desired to control the signal sampling at the remote location as well as from the computer.

Solution: Using sulfur dioxide analyzers providing analog output, a PDM70-B (with keyboard and display) is used with the following option modules:

- One PDM70-F Four Channel Differential Analog Input Option Module to accept signals from sulfur dioxide analyzers.
- One PDM70-P Programmable Control Module to permit local programming of the PDM70.
- One PDM70-JR Serial Input/Output Option Module to allow transmission of data to computer.

Example 2:
Problem: A laboratory has two analytical pH meters and one digital voltmeter. There is no access to a computer, but it is desired to maintain flexibility in the instrumentation to facilitate computerization in the future. For now, the requirement is simply to record voltage vs. time on a strip chart recorder and to print out pH values on a 21-column printer at predetermined time intervals. A fixed program sequence will be utilized most of the time, although it is planned to enter different programs in the future.

Solution: Utilizing pH meters and a digital voltmeter with standard BCD output, a PDM70-B (with keyboard and display) is used with the following option modules:

- Three PDM70-D BCD/Binary Input Modules to accept BCD signals from the pH meters and the digital voltmeter.
- One PDM70-H Two Channel Analog Voltage Output Module to provide analog voltage output to a strip chart recorder to monitor voltage vs. time. One channel remains for future expansion.
- One PDM70-M 8-Bit Parallel Input/Output Option Module to output data showing pH measurements to two 21 column printers.
- One PDM70-P Programmable Control Module to allow local programming of the PDM70.
- One PDM70-N PROM Read-In Option Module to permit "automatic" programming of an often-used program by inserting this permanently preprogrammed module.

The above application examples illustrate the flexibility of the PDM70. Each application was solved by choosing the best basic unit for the user's needs and choosing the proper combination of option modules from the PDM70 module library.

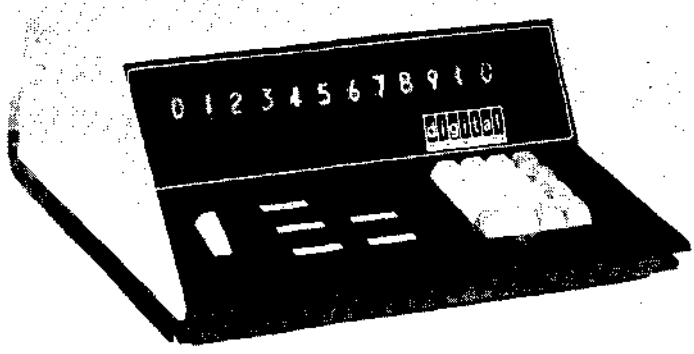
SPECIFICATIONS

Basic System:

Data Format	Standard ASCII asynchronous code format of 7 bits plus even parity
Speed	39,600 baud (internal); also provided are switch-selectable rates of 110, 150, 300, 600, 1200, 1800, 2400, 3600, 4800, and 9600 baud
Input Voltage	PDM70-AA, -BA, -CA: 115 Vac @ 7A, 50/60 Hz PDM70-AB, -BB, -CB: 230 Vac @ 5 A, 50/60 Hz
Power/Heat Dissipation	250 W/858 Btu/hr (12.3 kg—calories/hr)
Mounting	Table-top, standard; rack mount, optional
Length	23 inches (0.58 m)
Width	19 inches (0.48 m)
Height	5¼ inches (0.13 m)
Weight (max.)	55 lbs (25 kg)
Storage Temperature	—40°F to 185°F (—40°C to 85°C)
Operating Temperature	32°F to 104°F (0°C to 40°C)
Relative Humidity	95 percent maximum with no condensation
Keyboard	30 ASCII characters; 16-pad keyboard with shift key
Display	Displays single 32-character line, each character 5 x 7 dot matrix; 64 alphanumeric character set, coding is modified ASCII

RT01
DATA ENTRY TERMINAL

TERMINAL



The RT01 is a compact, portable data entry terminal designed for simple, serial interactive communication with a computer. The terminal consists of a 16-character keyboard, a communications interface module, status indicators, and a power supply. A numeric display is optional.

The 16-character keyboard contains the numeric characters 0 through 9, and the alphabetic characters A through F. The RT01 transmits the key codes and receives at rates of 110 and 300 baud standard.

The RT01 is prewired to accept a numeric display option which enables the RT01 to display numeric data, 0 through 9, and a decimal point. The decimal point is program-controlled; its particular location depends on the data or character codes received. Optional numerical display clusters of 4, 8, and 12 characters are available. A plus-or-minus sign can be substituted for a numeric character.

Communicating with a computer using the RT01 is similar to using a teletypewriter. However, the 16-pad keyboard is not just limited to a 16-character repertoire. There can be virtually countless numbers of functions as determined by the user. By using simple programming techniques, the 16 characters can be software-interpreted as commands, or instructions. For example, in stockroom applications, the keyboard alpha characters might be assigned in the following manner:

Character	Function
A	Employee Number Follows
B	Part Number Follows
C	Cost Center Follows

The RT01 can be connected directly to modems, data phones, acoustic couplers, and other EIA/CCITT compatible devices. Or, it may be connected directly to a computer via its 20 mA current loop interface.

RT01 MODELS

	115 Vac	230 Vac
110 baud	RT01-AA	RT01-AB
300 baud	RT01-BA	RT01-BB

RT01 OPTIONS

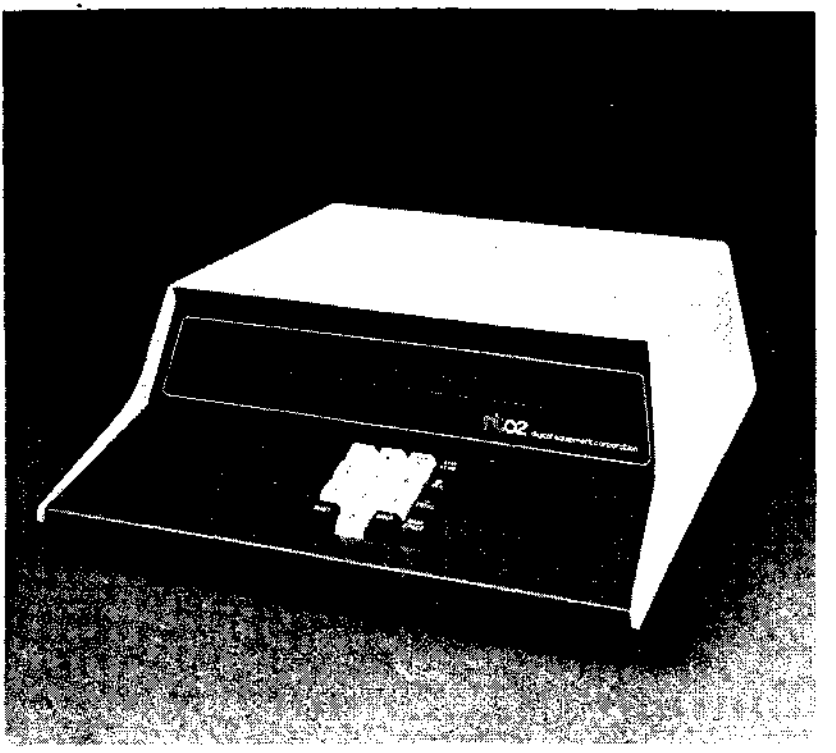
RT01-NA	Four-digit display
RT01-NB	Eight-digit display
RT01-NC	Twelve-digit display

RT01 SPECIFICATIONS

Data Transmission	EIA/CCITT and 20 mA current loop available Jumper selectable transmit/receive rates: 110, 150, 300, 600, 1200, 2400, 4800 baud
Height	6.5 in. (16.5 cm)
Width	12.5 in. (31.98 cm)
Depth	15 in. (38.1 cm)
Weight	12 lb (5.4 kg)
Power Requirements	15 to 125 Vac or 210 to 250 Vac 47 to 63 Hz
Power Dissipation	30 W maximum
Environmental Requirements	
Temperature	30° to 130° F (−1° to 54°C)
Relative Humidity	10 to 90%, without condensation
Optional Display	4-, 8-, or 12-character tube display

RT02-A ALPHANUMERIC DATA ENTRY TERMINAL

TERMINAL



The RTO2-A Alphanumeric Terminal is a low-cost data entry terminal offering both local and remote operation and featuring 20 mA current loop and EIA serial line compatibility. It can receive, store, and display 32 alphanumeric characters on a single line, gas-discharge type readout panel. Character repertoire is a modified 64-ASCII set.

Data is entered via a 16-pad keyboard which includes a shift key to enable entry of a full 30 characters that the monitoring computer may interpret as either numeric data or control functions.

Interfacing to a computer is accomplished via a standard full-duplex, 4-wire data communications interface. Modem interface signals corresponding to EIA RS-232-C specifications are also provided.

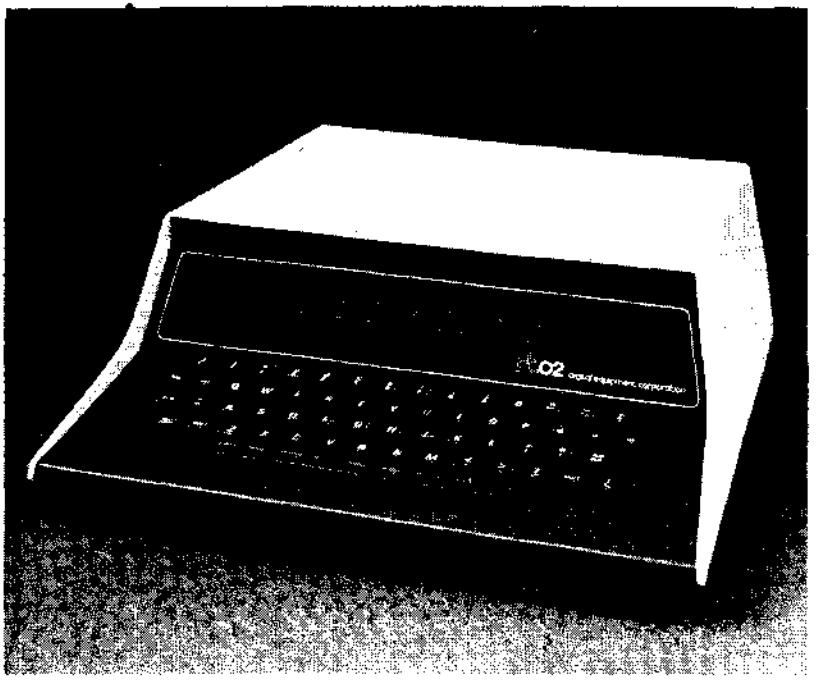
Two RT02-A models are available: The RT02-AA for 115-Vac facilities, and the RT02-AB for 230-Vac facilities.

SPECIFICATIONS

Character Set:	64-character modified ASCII, upper case
Number of Character Screen Positions:	32
Character Generation Method:	5 × 7 dot matrix
Display Color:	Red
Display Viewing Angle:	120°
Character Format:	8 level asynchronous serial ASCII 2 stop bits (110 baud) 1 stop bit (150, 300, 1200 baud)
Data Transmission:	EIA/CCITT and 20 mA current loop available
Transmit/Receive Rates:	Switch-selectable: 110/110 baud, TTY+EIA 150/150 baud, TTY+EIA 300/300 baud, TTY+EIA 1200/1200 baud, EIA 110/1200 baud, EIA 150/1200 baud, EIA
Power Requirements:	RT02-AA: 105-125 Vac, 47-63 Hz RT02-AB: 210-250 Vac, 47-63 Hz
Power Dissipation:	50 W maximum
Operating Temperature:	32° to 104°F (0° to 40°C)
Relative Humidity:	0 to 90%, without condensation
Height:	5.75 in. (14.6 cm)
Width:	14.38 in. (36.5 cm)
Depth:	16.25 in. (41.3 cm)
Weight:	14 lb (6.3 kg)

RT02-B
FULL KEYBOARD
ALPHANUMERIC TERMINAL

TERMINAL



The RT02-B is a compact, lightweight, self-contained alphanumeric display terminal designed to provide interactive communications with a computer in configurations where a limited alphanumeric display storage capability is required. The RT02-B receives, stores, and displays 32 alphanumeric characters on a single-line gas discharge type readout panel from a 64-character repertoire (modified ASCII). Data entry is by means of a full keyboard to furnish a 128- or 96-character input to the computer; input information may be treated by the monitoring computer as either numeric data or control functions. Terminal-to-computer interfacing is via standard 20 mA current loop line units (full duplex, 4-wire interface cable) that are available for all DEC computers. The RT02-B also receives and transmits modem interface signals that comply with Electronic Industries Association (EIA) RS-232-C specifications. Either Teletype or EIA signals are exchanged with data communications devices by means of separate connectors provided as standard equipment on the RT02-B.

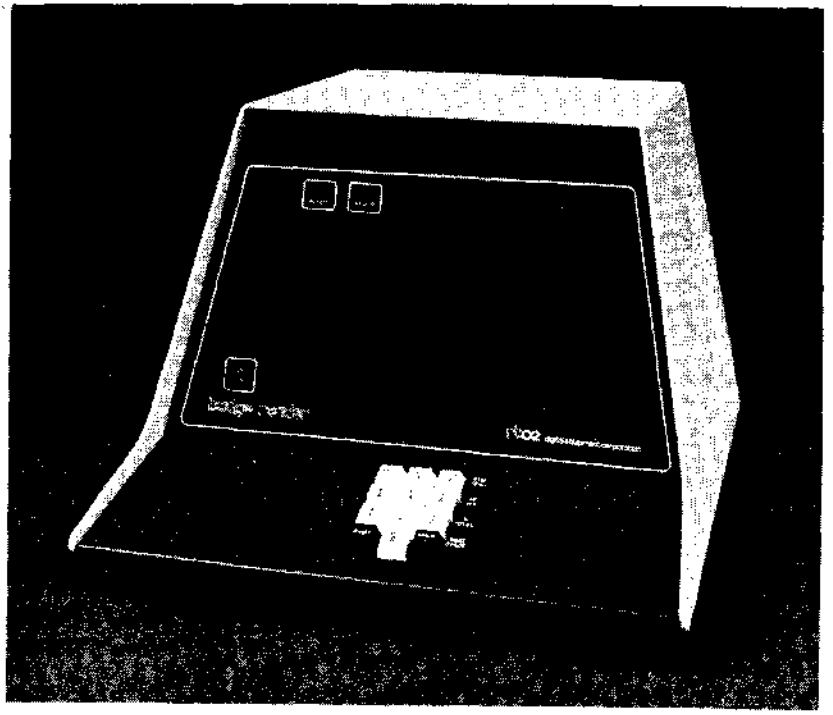
Two RT02-B models are available: The RT02-BA for 115-Vac facilities, and the RT02-BB for 230-VAC facilities.

SPECIFICATIONS

Character Set:	64-character modified ASCII, upper case
Number of Character Screen Positions:	32
Character Generation Method:	5 × 7 dot matrix
Display Color:	Red
Display Viewing Angle:	120°
Character Format:	8 level asynchronous serial ASCII 2 stop bits (110 baud) 1 stop bit (150, 300, 1200 baud)
Data Transmission:	EIA/CCITT and 20 mA current loop available
Transmit/Receive Rates:	Switch-selectable: 110/110 baud, TTY+EIA 150/150 baud, TTY+EIA 300/300 baud, TTY+EIA 1200/1200 baud, EIA 110/1200 baud, EIA 150/1200 baud, EIA
Audible Signal:	Under software control when ASCII bell code received (007). Jumper option for local audible signal when 28th character displayed.
Power Requirements:	RT02-BA: 105-125 Vac, 47-63 Hz RT02-BB: 210-250 Vac, 47-63 Hz
Power Dissipation:	50 W maximum
Operating Temperature:	32° to104°F (0° to 40°C)
Relative Humidity:	0 to 90%, without condensation
Height:	5.75 in. (14.6 cm)
Width:	14.38 in. (36.5 cm)
Depth:	16.25 in. (41.3 cm)
Weight:	15 lb (6.3 kg)

RT02-C
BADGE READER TERMINAL

TERMINAL



The RT02-C Badge Reader is a self-contained, remote data entry terminal. This device offers a reliable method of identifying and controlling access to a computer and a very fast method of entering fixed data. Fixed alphanumeric data entry is accomplished via a 22-column static optical badge reader with no moving contacts; variable alphanumeric data and control entry is accomplished by means of a 16-key, 30-character keyboard. The alphanumeric display permits complete interaction between the computer and the operator; instructions to the operator, therefore, can be tailored to the specific application.

Options are available which allow a combination of controls over the audible signal, function lights, badge ejector, and keyboard lockout. This versatility permits the user to configure the terminal to offer a specific response to a badge input.

The standard terminal contains both EIA and 20 mA interfaces. All communication is ASCII coded.

SPECIFICATIONS

RT02-CA Type III Badge Reader 115 Vac, 47-63 Hz

RT02-CB Type III Badge Reader 230 Vac, 47-63 Hz

Reader Type:	Static optical type utilizing photo diodes
Badge Types:	Type III, plastic punched, 22 columns × 10 rows Hollerith encoded alphanumerics. Maximum 22 characters.
Badge Size:	Type III, 2.43 in. (6.2 cm) × 3.25 in. (8.3 cm); .018 in. (.045 cm) to .030 in. (.076 cm) thick
Badge Removal:	Ejector under program or local control; jumper selectable.
Audible Signal:	0.5 second beeper under program or local control; jumper selectable.
Indicator Lights:	"Accept" and "Reject" under program or local control; jumper selectable.
Badge Reread:	A reread of badge initiated by receipt of "NAK" or "ENQ.."
Keyboard Lockout:	Automatic during badge read cycle. May be also locked out as user jumper option until enabled by computer.
Display:	32-character position, alphanumeric. 64-character modified ASCII set.
Keyboard:	16-key, 30-character (with shift), sealed.
Data Input/Output:	TTY, 20 mA, optically isolated current loop. EIA RS-232C.
Transmit/Receive Rates:	Switch-selectable: 110/110 baud, TTY+EIA 150/150 baud, TTY+EIA 300/300 baud, TTY+EIA 1200/1200 baud, EIA 110/1200 baud EIA 150/1200 baud, EIA
Character Format:	8 level asynchronous serial ASCII 2 stop bits (110 baud) 1 stop bit (150, 300, 1200 baud) Even parity
Height:	12 in. (30.5 cm)
Width:	14.38 in. (36.5 cm)
Depth:	15.88 in. (40.3 cm)
Weight:	20 lb (9 kg)
Power:	65 W maximum
Temperature:	32° to 113°F (0° to 45°C)

The RT02-C can be modified to read the first 22 columns of an 80-column paper card in the same manner it reads Type III plastic badges. The modification requires the installation of a set of card guides internal to the badge reader. Once the modification is installed, Type III badges can no longer be inserted.

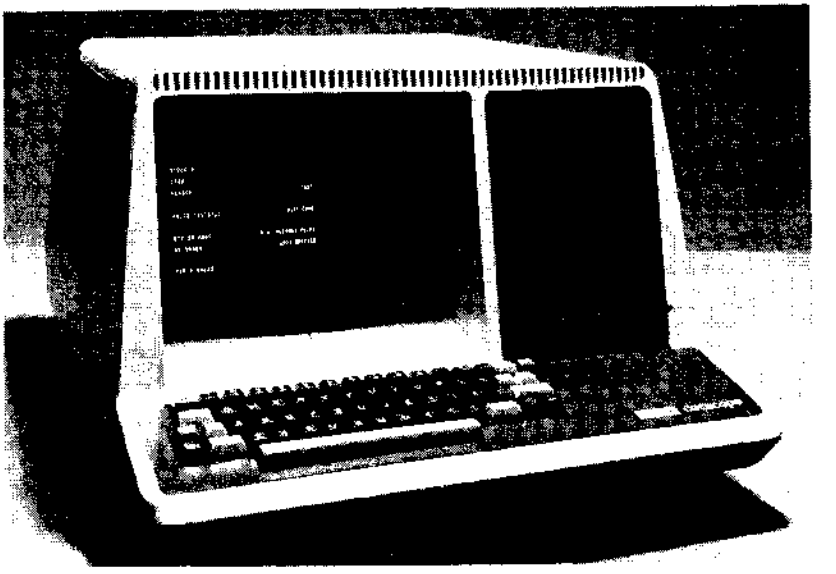
Card guides are available upon request.

CUSTOM TERMINALS

If one of our standard data entry terminals does not meet your needs, you will want to take advantage of our Custom Terminal capabilities. For large volume requirements (typically, more than 50 units), we can supply modified versions of our standard terminals built to your specifications.

VT50
DECscope

TERMINALS



The VT50 DECscope is an alphanumeric video display ideally suited for either quantity usage as remote data terminals in a large timesharing network or as a single station for local I/O applications. The extremely low cost of the VT50 benefits the user by providing a fast video capability at a price comparable to conventional teletypewriters.

The character set consists of the standard 64 ASCII upper case characters. A 20 mA current loop interface is standard equipment; EIA levels conforming to standard RS232-C may be optionally provided. Switch-selectable, full-duplex transmission rates of 75, 110, 150, 300, 600, 1200, 2400, 4800, and 9600 baud are available to satisfy a wide range of transmission facilities. All of these communication features combine to make the VT50 a truly universal and easy-to-interface video terminal.

VT50 operation is simple since all programming commands may be accomplished by nontechnical personnel having no computer or programming skills. Data and control information are easily entered via the keyboard, which is similar to a typewriter in symbol placement. The screen displays up to 960 characters—12 lines, each containing 80 characters. A flashing underline, or cursor, indicates where the next character will appear on the screen. The latest 12 lines of information are always displayed for user reference. Type P4 phosphor is used for maximum character intensity, allowing the VT50 to be used under most room lighting conditions.

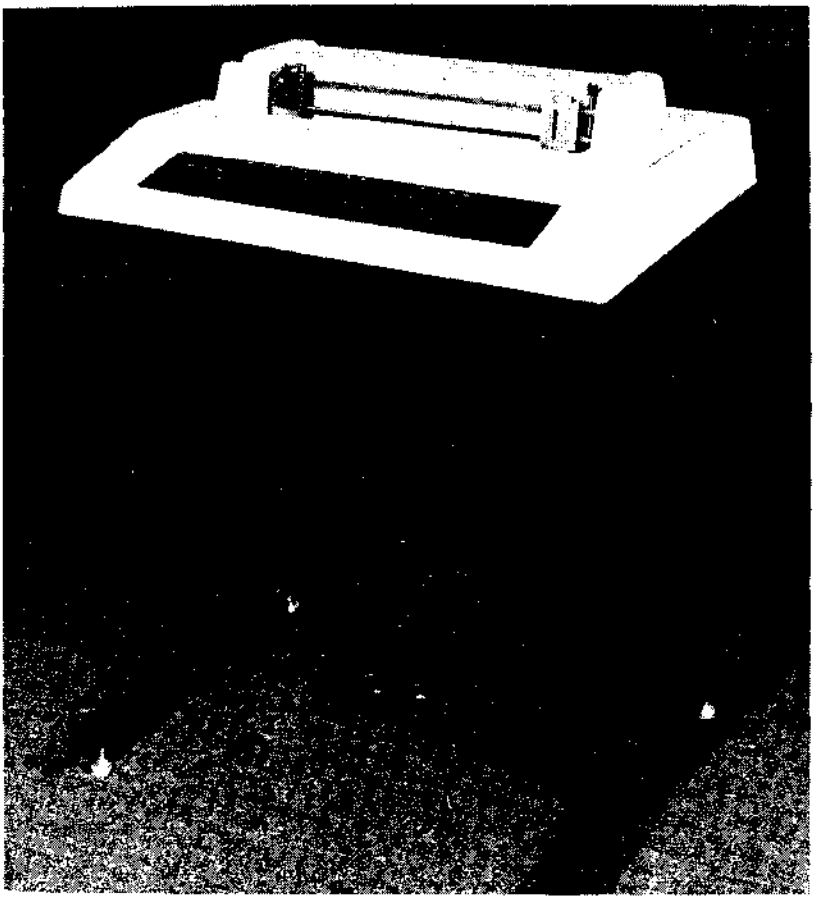
SPECIFICATIONS

Dimensions	Height: 360mm (14.1 in) Width: 530mm (20.9 in) Depth: 690mm (27.2 in)
Weight	19.4 KG (43 lbs)
Environmental	Temperature: 10°C to 40°C (50°F to 104°F) Relative Humidity: 10% to 90% with maximum Wet Bulb 28°C (82°F) and Minimum Dew Point 2°C (36°F)
Case Material	Noryl SE-100 Plastic (Polythenylene Oxide Modified with Polystyrene)
Input Voltage	115 Volts: 100 to 126 Volts @ 60 Hz ±1 Hz European Versions— 200 Volts: 191-238 Volts @ 50 Hz ±1 Hz or 60 Hz ±1 Hz 240 Volts: 209-260 Volts @ 50 Hz ±1 Hz or 60 Hz ±1 Hz Japanese Versions Available
Display	Format: 12 Lines x 80 Characters Character Matrix: 5 x 7 Character Size: 2.7mm x 5.0mm (.11 in x 20 in) Screen Size: 220mm x 110mm (8.7 in x 4.3 in) Capabilities: Control data transmission at high baud rates; will contain FORTRAN or COBOL full-card images; character intensity operator-controlled
Keyboard	Character Set: 64 ASCII Upper Case, Alpha, Numeric, and Punctuation Characters Typewriter Format Keyboard Audio Response Mechanism for Operator Feedback 3-Key Rollover Feature for Minimizing Errors BREAK Key Included for Half Duplex Software
Terminal Modes	Local Mode (Off-Line) Remote Mode (On-Line): Full Duplex or Full Duplex with Local Copy
Page Overflow	Upward Scroll
Parity	Even or Mark (No Parity), Selectable
Cursor	Control: Up or Down One Line, Right or Left One Character, Home Type: Non-Destructive, Underscore
Communications	20 mA Current Loop Standard; EIA Interface Optional
Transmission Code	USASCII Extended Through Escape Sequences
Operator Controls	Power On/Off, Intensity Control, Baud Rate Switch, Full Duplex or Full Duplex with Local Copy Switch, Copier Controls, Data Transmission Controls

Overload Protection	Thermal Switch in Line Transformer
Transmission Rates	Switch-Selectable Full Duplex: 75, 110, 150, 300, 600, 1200, 2400, 4800, and 9600 Baud Full Duplex with Local Copy: 110, 600, 1200, 2400, 4800, and 9600 Baud
Optional Features	For a complete, up-to-date listing of optional features, contact your local DIGITAL sales office.

LA36
DECwriter II

TERMINALS



The LA36 DECwriter II is a fast, reliable, and low-cost data terminal that provides an ideal hard copy capability for both remote and local I/O applications. A true 30-cps throughput rate is provided for full utilization of a 300-baud communications line. This is achieved by eliminating the need for fill characters and storing executable characters in a 16-character buffer during carriage return and line feed. When there is more than one character in the buffer, the LA36 automatically switches to 60-cps operation until all characters stored in the buffer have been printed. In this way, true 30-cps throughput is maintained.

Six-part forms printing is a standard feature of the LA36. This is made possible by using highly reliable tractors such as those found on high-speed computer line printers.

The LA36 makes 132-column printing a standard for keyboard printers. The use of tractors and 132-column printing means that the LA36 can be adjusted to accommodate all form sizes from 3 to 14⅞ inches in width. A simple manual adjustment permits pre-printed forms to be positioned in exact vertical alignment.

Every LA36 includes the ASCII complement of 96 upper and lower case printing characters. With an additional 32 non-printing control characters, the full 128 ASCII set is supported. Characters are printed using a 7x7 wire matrix print head. This field-proven print head is designed to have the longest life in the industry. Horizontal spacing is 10 characters per inch; vertical spacing is 6 lines per inch.

With little training, typists will feel comfortable with the LA36's typewriter-like key layout, and the quiet operation of the LA36 makes it well suited for use in an office environment.

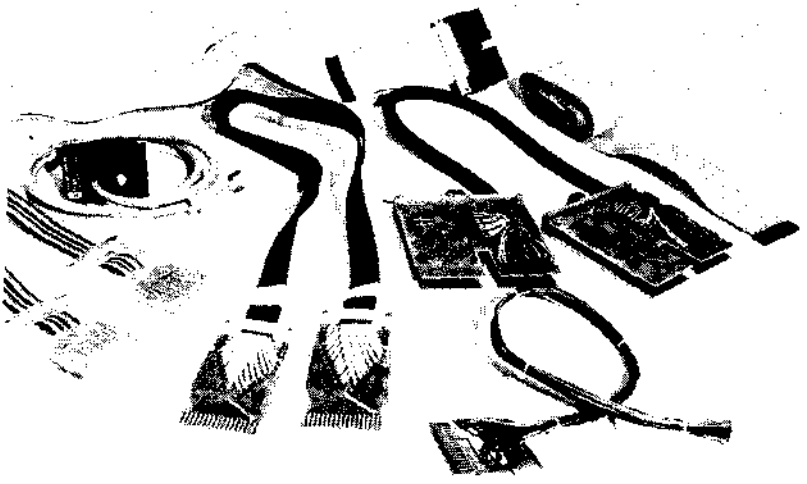
The LA36 incorporates three design features to ensure clear visibility of the printed line. The cabinet top is beveled to permit unobstructed view by a seated operator; the ribbon is positioned away from the paper surface in order to improve readability; the print head automatically moves four spaces to the right during a pause in the printing operation of 800 milliseconds or longer, giving the operator an unobstructed view of the full line being printed.

The LA36 uses an integrated 20 mA current loop interface with a jumper for active or passive mode operation. Other interfaces, such as EIA, are optionally available.

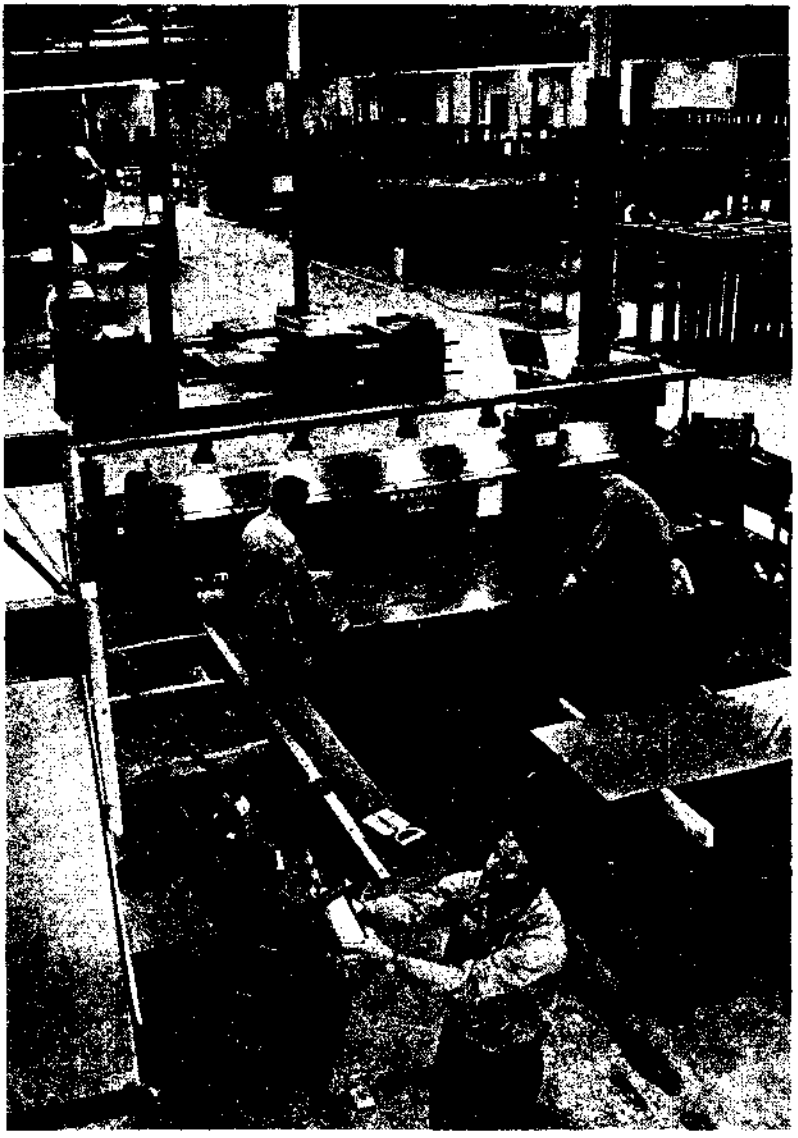
SPECIFICATIONS

Printing	True 30-cps throughput with 60-cps catch-up mode 132-column format Spacing—10-inch horizontal, 6-inch vertical
Characters	Full 96-character upper/lower case ASCII 7x7 dot (wire) matrix (0.070 x 0.100 inches)
Paper	Variable width, 3 to 14⅞ inches (7.6 to 38cm) Up to 6-part forms, 20 mils maximum pack thickness Tractor drive, pin feed
Keyboard	Standard ANSI keyboard layout, N-key roll-over
Interface	Integrated 20 mA current loop
Ribbon	DIGITAL-specified Nylon fabric, spool assembly, 0.5 inches wide x 40 yards
Power Requirements	90-132 Vac or 180-264 Vac, 47-63 Hz 300 W maximum (printing), 160 W non-printing

Temperature	Operating: 50°F (10°C) to 104°F (40°C) Non-operating: –40°F (–40°C) to 151°F (66°C)
Humidity	Operating: 10% to 90% with max. wet bulb 82°F (28°C) and minimum dew point 36°F (2°C) non-condensing Non-operating: 5% to 95% relative humidity non-condensing
Dimensions	27.5 in. (70 cm) wide, 33.2 in. (84 cm) high, 24.0 in. (61 cm) deep
Weight	102 pounds (46 kg)
Optional Features	For a complete, up-to-date listing of optional features, contact your local DIGITAL sales office.



hardware
cable assemblies
power supplies



Cabinets for DEC systems are manufactured in this portion of DEC's recently opened Westfield, Massachusetts production facility.

HARDWARE/CABLE ASSEMBLIES/POWER SUPPLIES

Hardware is subdivided into several subgroups in this publication: cabinets, mounting panels, system units, cable connectors, blank module boards, module extender boards, integrated circuit (IC) sockets, integrated circuits (ICs), wire wrapping tools and accessories, etc. Within each subgroup, the descriptions of the items are arranged in alphanumeric order. Most of the hardware described in this publication is more completely described in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

Cable assemblies are subdivided into several subgroups in this publication according to the type of cable connector(s) and according to the type of cable. For example, 20-conductor, flat ribbon cable with single-sided connectors comprise one subgroup, and 40-conductor, flat mylar cables with double-sided connectors comprise another subgroup. Bulk cables are listed at the beginning of Cable Assembly descriptions. Bulk cable is more completely described in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

Power supplies are subdivided into several subgroups in this publication according to their usual use. For example, +5 Vdc Positive Logic Power Supplies comprise one subgroup, System Power Supplies comprise another subgroup, and Step-Down Transformers and Power Controllers comprise another subgroup. Power supplies are more completely described in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

HARDWARE

CABINETS AND CABINET ACCESSORIES

Digital Equipment Corporation offers two basic cabinet frames, standard size and short size, and a complete line of cabinet accessories and hardware. Both sizes accept panels or equipment designed to mount in standard 19-in. (48.26-cm) electronics cabinets or racks. The standard size cabinet frame provides 63.0 in. (160.0 cm) of vertical mounting space at the front and rear, and the short cabinet frame provides 42.0 in. (106.7 cm). The cabinet frames are rigidly constructed of 12 and 13 gauge steel, either riveted or welded together.

Basic color of cabinet is black. Gray is used for end panels and the inlay of the cover panels.

These cabinet frames offer complete flexibility and expandability to present and future Digital Equipment Corporation customers, single users, multiple users, and original equipment manufacturers. The enclosure area in these cabinets is adaptable to customer-designed hardware, logic module racks, power supplies, computer systems and peripherals.

The cabinets can be placed individually or attached to form a multibay configuration. The accessories and hardware available include front and rear doors, panel mounting door frames and door skins, end panels, bezel and logo panels, blower fans, and power controllers.

Standard Size Cabinets and Accessories

Seven basic cabinet configurations (H960-BC, H960-BD, H960-CA, H960-CB, H961-A, H961-AA, and H961-AB) are available in the standard size cabinet series. The H961-A, -AA, and -AB are intended primarily for add-on configurations. The standard size cabinet is 71.5 in. (181.61 cm) high and provides 63.0 in. (160.0 cm) of vertical mounting space at the front; an additional 63.0 in. of mounting space is available at the rear of the cabinet. These cabinets are configured to meet the requirements of most customer applications.

All standard size cabinets are configured around the basic H950-AA Cabinet Frame. These cabinet frames are drilled with 0.25-in. (0.64-cm) diameter holes at standard EIA spacings to accommodate equipment, panels, or devices which are designed to mount in standard 19-in. (48.26-cm) electronics cabinets or racks. Some of the cabinets contain an 861-A, 861-B, or 861-C Power Controller for distribution and control of the main power to the equipment installed. Six of the cabinet configurations include a rear mounting panel door frame, which is also drilled with 0.25-in. (0.64-cm) diameter holes at standard EIA spacings; this mounting panel door frame allows the equipment and devices mounted on it to be swung out for maintenance or adjustment. Optional accessories as specified by the customer can be added to any of the available configurations. The parts and accessories included with each of the seven standard size cabinet configurations are listed in Table 1, which also lists the optional accessories that are available for use with these cabinets. All cabinets are completely assembled before shipment.

Figure 1 illustrates a typically configured standard size cabinet front. Figure 2 illustrates the installation of typical accessories on a standard size cabinet frame, and Table 2 identifies and describes these accessories. Complete descriptions of the H950-AA Cabinet Frame and the accessories for standard size cabinet frames are contained in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

Table 1
Standard Cabinets
H960-BC, H960-BD, H960-CA, H960-CB, H961-A, H961-AA, and H961-AB

Cabinet Assembly H960-BC	H960-BD	H960-CA	H960-CB	H961-A	H961-AA	H961-AB	Catalog No.	Description
1	1	1	1	1	1	1	H950-AA	Cabinet Frame, 19 in. wide, 69 in. high, 25 in. deep
		1	1				H950-BA	Full Door (RH) (front or rear mounting)
							H950-CA	Full Door (LH) (front or rear mounting)
1	1	1	1		1	1	H950-DA	Mounting Panel Door Frame (RH) (rear mounting)
				1			H950-EA	Mounting Panel Door Frame (LH) (rear mounting)
1	1			1	1	1	H950-FA	Mounting Panel Door Skin
							H950-HA	Short Door (covers 21 in. mounting space)
							H950-HB	Short Door (covers 22¾ in. mounting space)
							H950-HC	Short Door (covers 26¼ in. mounting space)
							H950-HD	Short Door (covers 31½ in. mounting space)
							H950-HE	Short Door (covers 36¾ in. mounting space)
							H950-HF	Short Door (covers 42 in. mounting space)
							H950-HG	Short Door (covers 47¼ in. mounting space)
							H950-HH	Short Door (covers 52½ in. mounting space)
							H950-HJ	Short Door (covers 57¾ in. mounting space)
							H950-HK	Short Door (covers 63 in. mounting space)
							H950-JA	Short Door (covers 21 in. mounting space) (used with H952-BA installed)
							H950-JE	Short Door (covers 63 in. mounting space) (used with H952-BA installed)
							H950-LA	Logo Frame Panel (aluminum)
1	1	1	1	1	1	1	H950-LB	Logo Frame Panel (plastic)
							H950-PA	5¼ in. Bezel Cover Panel
5	5	5	6	6			H950-QA	10½ in. Bezel Cover Panel
1	1	1	1	1	1	1	H950-SA	Filter (for H952-BA or H952-CA)
2	2	2	2				H952-AA	End Panel (require 2 per cabinet)
1	1	1	1				H952-BA	Stabilizer Feet (pair)
1	1	1	1	1	1	1	H952-CA	Fan Assembly (top mounted) (115 Vac)
							H952-CB	Fan Assembly (top mounted) (230 Vac)
1	1	1	1	1	1	1	H952-EA	Caster Set (4 per set, included with H950-AA frame)
1	1	1	1	1	1	1	H952-FA	Leveler Set (4 per set, included with H950-AA frame)
				1	1	1	H952-GA	Filler Strip Set (front and rear) (joining two cabinets)
							H950-G	Cabinet Table
							H952-HA	Free-Standing Table
							H970-BA	Free-Standing Table
							H970-CA	Free-Standing Table
1	1	1	1				74-06782	Kickplate (use with H952-BA)
				1	1	1	74-06793	Kickplate
							12-09154	Drawer Mounting Slides
							12-09703	Drawer Mounting Slides (tilt)
	1		1			1	861-A	Power Controller (90—130 Vac, two phase)
1		1			1		861-B	Power Controller (180—270 Vac, single phase)
							861-C	Power Controller (90—135 Vac, single phase)

Table 2
Standard Cabinet Frame H950-AA and Accessories

Figure 2 Item	Part No.	Description
1	H950-DA	Mounting Panel Door Frame (right hanging)
1	H950-EA	Mounting Panel Door Frame (left hanging)
2	H950-BA	Door, Front or Rear Mounting (right hanging)
2	H950-CA	Door, Front or Rear Mounting (left hanging)
3	H950-SA	Air Filter
4	74-06706	Fan, Cover Plate
5	H952-CA	Fan Assembly (115 Vac)
5	H952-CB	Fan Assembly (230 Vac)
6	H952-AA	End Panel (left or right side)
7	H952GA	Filler Strip Set (front or rear)
8	H950-LB	Frame Panel (plastic)
8	H950-LA	Frame Panel (aluminum)
9	H950-PA	Bezel Cover Panel, 5.25 in. (13.34 cm)
10	H950-QA	Bezel Cover Panel, 10.50 in. (26.67 cm)
11	H950-G	Tabletop Assembly
12	H950-HA	Short Door, covers 21.00 in. (53.34 cm) mounting space
12	H950-HB	Short Door, covers 22.75 in. (57.79 cm) mounting space
12	H950-HC	Short Door, covers 26.25 in. (66.68 cm) mounting space
12	H950-HD	Short Door, covers 31.50 in. (80.01 cm) mounting space
12	H950-HE	Short Door, covers 36.75 in. (93.35 cm) mounting space
12	H950-HF	Short Door, covers 42.00 in. (106.68 cm) mounting space
12	H950-HG	Short Door, covers 47.25 in. (102.02 cm) mounting space
12	H950-HH	Short Door, covers 52.50 in. (133.35 cm) mounting space
12	H950-HJ	Short Door, covers 57.75 in. (146.68 cm) mounting space
12	H950-HK	Short Door, covers 63.00 in. (160.02 cm) mounting space
13	H952-FA	Leveler Set (4)
14	74-06782	Kickplate (used with H952-BA stabilizer feet)
14	74-06793	Kickplate
15	H952-BA	Stabilizer Feet (pair)
16	H952-EA	Caster Set (4)
17	74-11606	Bottom Screen
18	H950-AA	Frame, 19.00 in. (48.26 cm) wide, 69.00 in. (175.26 cm) high, 25.00 in. (63.50 cm) deep

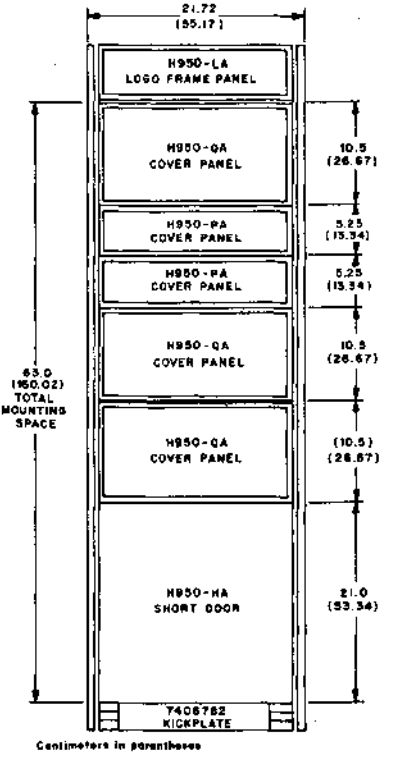


Figure 1. Typical Standard Cabinet Front Cover Panel and Short Door Configuration

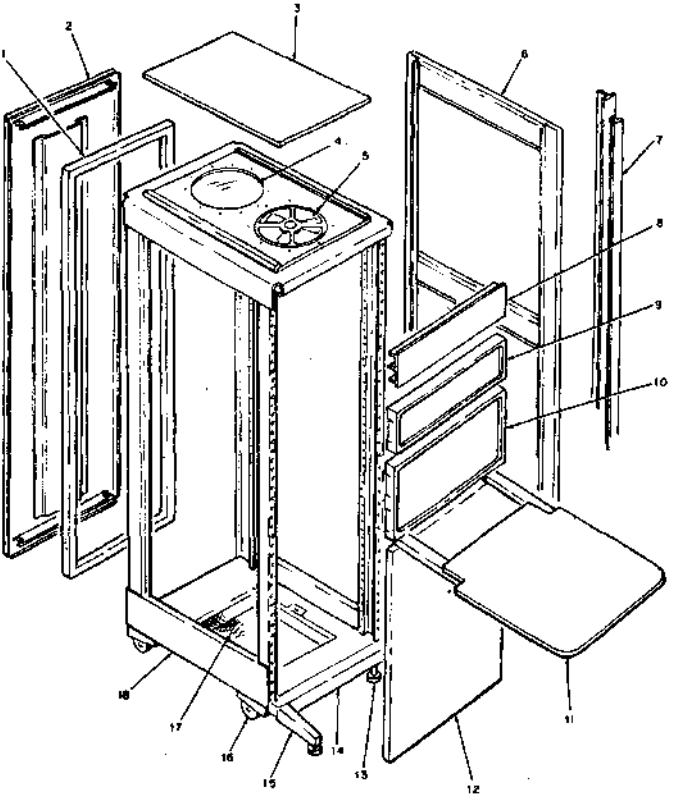
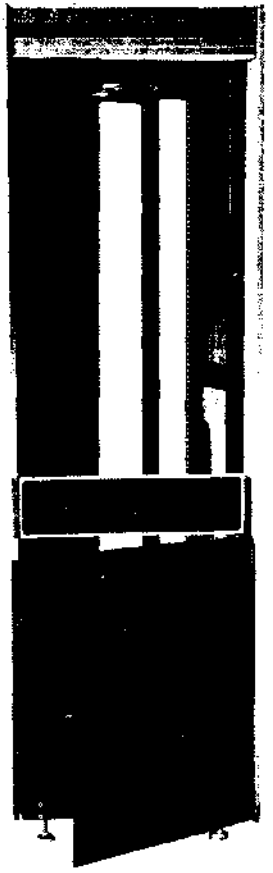
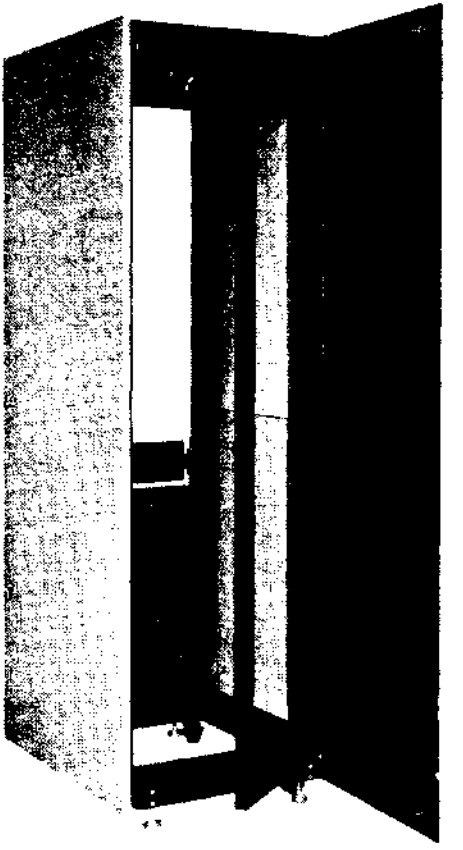


Figure 2. H950-AA Standard Cabinet Frame and Accessories



Front view of H950 frame.



Rear view of H950 frame.

How to Order a Standard Size Cabinet Assembly
Determine if one of the seven basic cabinet assembly configurations (H960-BC, H960-BD, H960-CA, H960-CB, H961-A, H961-AA, or H961-AB) will fulfill your requirements by referring to Table 1 and comparing the items that comprise each configuration.

If one of these basic configurations will satisfy your requirements, you can order the completely assembled cabinet by specifying that cabinet assembly number; e.g., H960-BC, H960-BD, H960-CA, H960-CB, H961-A, H961-AA, or H961-AB. In addition to the accessories included in the seven configurations, optional accessories are available, e.g., short doors, a cabinet table, and drawer mounting slides.

If one of the basic configurations will not fulfill your requirements, you can "build up" and order a cabinet that will suit your specific requirements by ordering an H950-AA standard size frame and the accessories (by specific part numbers) that you require. The frame and the accessories that you select will be shipped completely assembled.

Short Size Cabinets and Accessories
Five basic cabinet configurations (H967-BA, H967-BB, CAB-I, CAB-J, and CAB-K) are available in the short size cabinet series. CAB-K is intended primarily for add-on configurations. The short size cabinet is 50.0 in. (127.0 cm) tall and provides 42.0 in. (106.7 cm) of vertical mounting space at the front; an additional 42.0 in. (106.7 cm) of mounting space is available at the rear of the cabinet. These cabinets are configured to meet the requirements of most customer applications.

All short size cabinets are configured around the basic H957-AA Cabinet Frame. These cabinet frames are drilled with 0.25-in. (0.64-cm) diameter holes at standard EIA spacings to accommodate equipment, panels, or devices that are designed to mount in standard 19-in. (48.26-cm) electronics cabinets or racks. Two of the cabinets contain power controllers for distribution and control of the main power to the equipment installed. Three of the cabinet configurations include a rear mounting panel door frame, which is also drilled with 0.25-in (0.64-cm) diameter holes at standard EIA spacings; this mounting panel door frame allows the equipment and devices mounted on it to be swung out for maintenance or adjustment. Optional accessories as specified by the customer can be added to any of the available configurations. Table 3 lists the parts and accessories included in each of the five short size cabinet configurations; Table 3 also lists the optional accessories that are available for use with these cabinets. All cabinets are completely assembled before shipment.

Figure 3 illustrates a typically configured short size cabinet front. Figure 4 illustrates the installation of typical accessories on a short size cabinet frame, and Table 4 identifies and describes these accessories. Complete descriptions of the H957-AA Cabinet Frame and the accessories for short size cabinet frames are contained in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

Table 3
Short Cabinets
H967-BA, H967-BB, CAB-I, CAB-J, and CAB-K

Cabinet Assembly						
H967-BA	H967-BB	CAB-I	CAB-J	CAB-K	Catalog No.	Description
1	1	1	1	1	H957-AA	Cabinet Frame, 19 in. wide, 47-8/16 in. high, 25 in. deep
1	1	1	1		H957-BA	Full Door (RH) (rear mounting)
				1	H957-CA	Full Door (LH) (rear mounting)
1	1	1			H957-DA	Mounting Panel Door Frame (RH)
					H957-EA	Mounting Panel Door Frame (LH)
					H952-HA	Free-Standing Table
					H970-BA	Free-Standing Table
					H970-CA	Free-Standing Table
					H950-HA	Short Door (covers 21 in. mounting space)
					H950-HB	Short Door (covers 22¾ in. mounting space)
					H950-HC	Short Door (covers 26¼ in. mounting space)
					H950-HD	Short Door (covers 31½ in. mounting space)
					H950-HE	Short Door (covers 36¾ in. mounting space)
					H950-HF	Short Door (covers 42 in. mounting space)
					H950-JA	Short Door (covers 21 in. mounting space) (used with H952-BA installed)
					H950-PA	Bezel Cover Panel, 5¼ in.
					H950-QA	Bezel Cover Panel, 10½ in.
1	1	1			H952-BA	Stabilizer Feet (pair)
1	1	1	1	1	H952-EA	Caster Set (4 per set, included with H957-AA Frame)
1	1	1	1	1	H952-FA	Leveler Set (4 per set, included with H957-AA Frame)
					H950-G	Cabinet Table
1	1	1	1		H957-FA	End Panel (R end)
1	1	1	1		H957-FB	End Panel (L end)
				1	H957-GA	Filler Strip Set (top, front, and rear) (joining two cabinets)
1	1	1	1	1	H957-HA	Fan Assembly (front or rear mounting)
					H957-JA	Bottom Cover Plate
1	1	1	1	1	H957-LA	Logo Frame Panel
1	1	1	1	1	H957-SA	Filter (for H957-HA)
1	1	1			74-06782	Kickplate (use with H952-BA)
			1	1	74-06793	Kickplate
					12-09154	Drawer Mounting Slides
					12-09703	Drawer Mounting Slides (tilt)
					861-A	Power Controller (90—130 Vac, two phase)
	1				861-B	Power Controller (180—270 Vac, single phase)
1					861-C	Power Controller (90—135 Vac, single phase)

Table 4
Short Size Cabinet Frame H957-AA and Accessories

Fig. 4 Item	Part No.	Description
1	H957-BA	Full Rear Door (right hanging)
1	H957-CA	Full Rear Door (left hanging)
2	H957-SA	Air Filter
3	H957-DA	Mounting Panel Door Frame (right hanging)
3	H957-EA	Mounting Panel Door Frame (left hanging)
4	H957-HA	Fan Assembly
5	H957-FA	End Panel (right hanging)
5	H957-FB	End Panel (left hanging)
6	H957-GA	Filler Strip Set (top, front, and rear)
7	H957-LA	Logo Frame Panel (plastic)
8	H950-PA	Bezel Cover Panel, 5.25 in. (13.34 cm)
9	H950-QA	Bezel Cover Panel, 10.50 in. (26.67 cm)
10	H950-HA	Short Door, covers 21.00 in. (53.34 cm) mounting space
10	H950-HB	Short Door, covers 22.75 in. (57.79 cm) mounting space
10	H950-HC	Short Door, covers 26.25 in. (66.68 cm) mounting space
10	H950-HD	Short Door, covers 31.50 in. (80.01 cm) mounting space
11	H952-BA	Stabilizer Feet (pair)
12	74-06782	Kickplate (used with H952-BA Stabilizer Feet)
12	74-06793	Kickplate
13	H952-EA	Caster Set (4)
14	H957-AA	Frame, 19.00 in. (48.26 cm) wide, 47.50 in. (120.65 cm) high, 25.00 in. (63.50 cm) deep

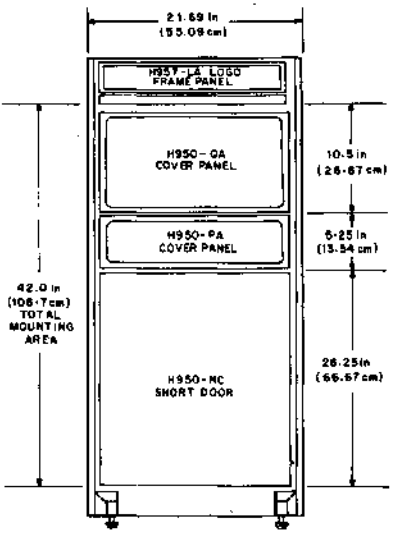


Figure 3. Typical Short Cabinet Front Cover Panel and Short Door Configuration

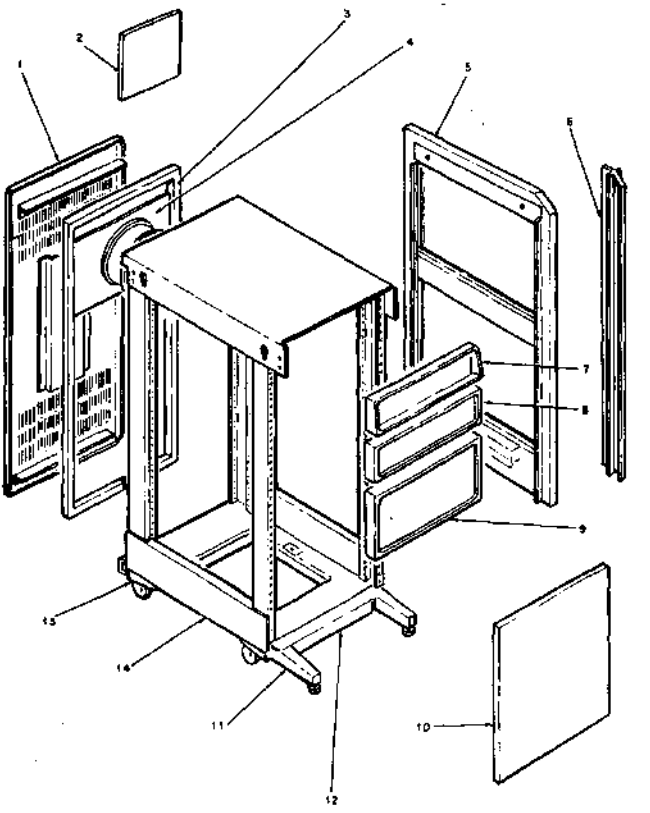


Figure 4. H957-AA Short Cabinet Frame and Accessories

How to Order a Short Size Cabinet Assembly
Determine if one of the five basic cabinet assembly configurations (H967-BA, H967-BB, CAB-I, CAB-J, or CAB-K) will fulfill your requirements by referring to Table 3 and comparing the items that comprise each configuration.

If one of the basic configurations will satisfy your requirements, you can order the completely assembled cabinet by specifying that cabinet assembly number, e.g., H967-BA, H967-BB, CAB-I, CAB-J, or CAB-K. In addition to the accessories included in the five configurations, optional accessories are available, e.g., short doors, a cabinet table, drawer mounting slides, etc.

If one of the basic configurations will not fulfill your requirements, you can "build up" and order a completely assembled cabinet that will suit your specific requirements by ordering an H957-AA short size frame and the accessories (by specific part numbers) that you require. The frame and the accessories that you select will be shipped completely assembled.

Cabinet Hardware
Digital Equipment Corporation offers a variety of cabinet hardware which can be used on existing system cabinets or installed on the basic standard size or short size cabinet configurations. This hardware can also be purchased as replacement parts.

PAINT (TOUCHUP)—29-15201, 29-15202, 29-15205
Paint is available in aerosol cans for touching up Digital Equipment Corporation manufactured cabinets. This paint is available in three colors: black, grey (bezel/68), and grey (end panel/101).

TINNERMAN CLIP NUT AND PHILLIPS PAN HEAD SCREW COLLECTION—90-07786
This is a bagged collection of fifty 10-32 Tinnerman clip nuts, fifty 10-32 × 5/8-in. (1.5875-cm) Phillips pan head screws, and fifty size 10 lock washers.

LATCH—12-09224
The 12-09224 Latch is used to secure H950-PA or H950-QA Bezel Cover Panels to the front of either the standard size or short size cabinet frame (H950-AA or H957-AA).

THICK LATCH—12-11386
The 12-11386 Thick Latch is used to secure H950-PA or H950-QA Bezel Cover Panels to the front of either the standard size or short size cabinet frame (H950-AA or H957-AA).

SPACER—74-07789
The 74-07789 Spacer is used to maintain alignment of H950-PA or H950-QA Bezel Cover Panels on the front of either the standard size or short size cabinet frame (H950-AA or H957-AA).

KEY-LOCK STRIKE PLATE—74-09819
The 74-09819 Key-Lock Strike Plate is used on a short size H957-AA Cabinet Frame as a strike plate for the key lock on the H957-BA or H957-CA Full Door when an H957-DA or H957-EA Mounting Panel Door Frame is not installed. The 74-09819 can be mounted on the left vertical cabinet frame rail to accommodate a right-hanging full door, or it can be mounted on the right vertical rail to accommodate a left-hanging full door. All the required mounting hardware is supplied with the 74-09819 Key-Lock Strike Plate.

CABINET DOOR GROUND STRAP—90-06990

The 90-06990 Cabinet Door Ground Strap is used to electrically connect the cabinet door to the cabinet frame to ensure that the cabinet door is not isolated from earth ground. The cabinet door should be connected to earth ground to prevent operating personnel from electrical shock if a short circuit should occur in the logic system.

The 90-06990 Cabinet Door Ground Strap is a braided-copper bonding jumper; it is 4.875 in. (12.383 cm) long and has a terminal on each end. Each terminal is equipped with a hole sized to accept a No. 10 screw.

One ground strap terminal should be secured to the cabinet frame, at the door hinge side, with a No. 10 screw and nut, and the other terminal should be secured to the cabinet door with a No. 10 screw and nut.

CABINET FRAME GROUND STRAP—90-08887

The 90-08887 Cabinet Frame Ground Strap is used to electrically connect one cabinet frame to another cabinet frame to continue the common earth ground for the logic system cabinets.

The 90-08887 Cabinet Frame Ground Strap is a braided-copper bonding jumper; it is 11.00 in. (27.94 cm) long and has a terminal on each end. Each terminal is equipped with a hole sized to fit over an 0.313-in. (0.794-cm) diameter stud.

Each H950-AA and H957-AA Cabinet Frame is equipped with two threaded (5/16-18) copper studs, one on each side, inside the cabinet near the bottom panel. The ground strap should be installed on the threaded copper studs of two adjacent cabinet frames and a 5/16-18 nut should be used to secure each ground strap terminal. Each cabinet in a logic system should be connected to its adjacent cabinets to form a continuous path to an earth ground.

NINETEEN-INCH (48.26-cm) ELECTRONICS RACK MOUNTING PANELS

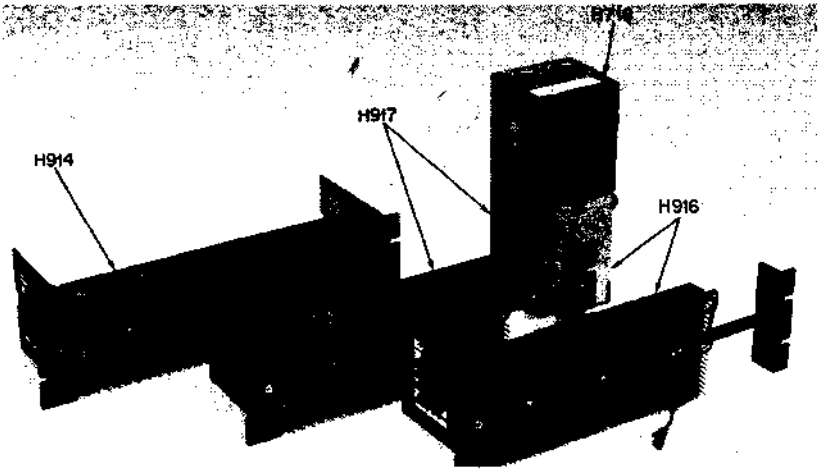
Mounting panels are designed to provide mounting space for module connector blocks and are usually used to expand a logic system. They are designed to mount in standard 19-in. (48.26-cm) electronics racks or cabinets.

One (H020) of these mounting panels is a bare frame for mounting module connector blocks, some (H911-J, H911-K, H911-R, H911-S, K943-R, and K943-S) are equipped with connector blocks and are prebused for power and ground, others (H913, H916, and H917) are equipped with connector blocks and a power supply and are prebused for power and ground, and one (H914) is a frame that is equipped with connector blocks but is not bused or wired for power or ground.

The following table summarizes the mounting panels; individual detailed descriptions of these mounting panels are contained in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

19-In. Rack Mounting Panels

Part Number	Description
H020	Blank mounting panel that accommodates eight connector blocks; mounts in a standard 19-in. (48.26-cm) electronics rack.
H911-J	H020 equipped with eight H803 connector blocks to accommodate 64 single-height or 32 double-height, standard-length modules; bused for power and ground.
H911-K	Same as H911-J except wired and bused for power and ground.
H911-R	Same as H911-J except accommodates extended-length modules.
H911-S	Same as H911-K except accommodates extended-length modules.
H913	H020 equipped with an H710 Power Supply and four H808 connector blocks to accommodate 16 single-height or 8 double-height, standard-length modules; bused for power and ground.
H914	H020 equipped with eight H808 connector blocks to accommodate 32 single-height or 16 double-height, standard-length modules.
H916	H020 equipped with an H716 Power Supply and six H803 connector blocks to accommodate 48 single-height or 24 double-height, standard-length modules; bused for power and ground.
H917	H020 equipped with an H716 Power Supply and four H808 connector blocks to accommodate 24 single-height, standard-length modules; bused for power and ground.
K943-R	H020 equipped with eight H800-W connector blocks to accommodate 64 single-height or 32 double-height modules with contact fingers on only one side; bused for power and ground. Connector blocks equipped with solder-fork pins for 24 AWG wire.
K943-S	Same as K943-R except equipped with eight H800-F connector blocks that have wire wrap pins for 24 AWG wire.


H914
H917
H916

FOUR-SLOT SYSTEM UNITS

Four-slot system units are designed to provide mounting sockets (slots) for logic system modules. They are designed to mount in the various module system enclosures also offered by Digital Equipment Corporation. Module system enclosures are described elsewhere in this section. Four-slot system units accept up to three four-slot module connector blocks mounted end-to-end. Since each of the module connector blocks used with these system units has two rows of slots, a fully complemented four-slot system unit provides mounting facilities for 24 single-height, 12 double-height, or four quad-height and eight single- (or four double-) height modules.

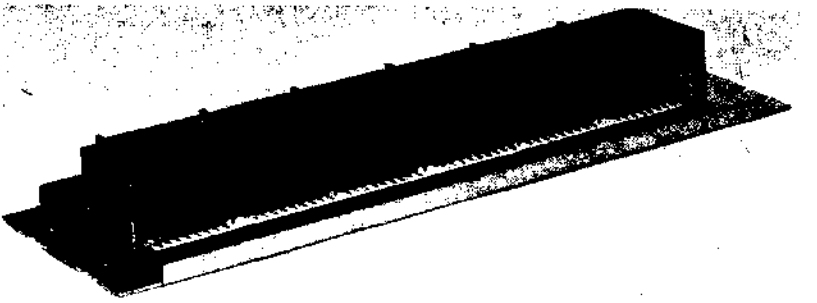
One (H033) of the four-slot system units is a bare frame for mounting connector blocks, some (H933-A, H933-B, H933-CA, H933-CB, and H933-D) of the four-slot system units are equipped with connector blocks, and others (BB11, BB11-A, DD11-A, and DD11-B) are equipped with connector blocks and are prebused for power and ground and are prewired for UNIBUS interfacing.

The following table summarizes the four-slot system units; individual detailed descriptions of these system units are contained in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

Four-Slot System Units

Part Number	Description
BB11	H033 equipped with one H803 and two H863 connector blocks to accommodate 24 single-height, 12 double-height, or four quad-height and four double- (or eight single-) height modules; prewired for UNIBUS, power, and ground; used for general UNIBUS interfacing.
BB11-A	Same as BB11 except equipped with three H803 connector blocks.
DD11-A	H033 equipped with three H803 connector blocks to accommodate four SPCs, a UNIBUS input connector module, a UNIBUS terminator/extender module, and a power connector module, or four UNIBUS interface modules, four address selector modules (M105), four UNIBUS interrupt control modules, a UNIBUS input connector, a UNIBUS terminator/extender module, and a power connector module; prewired for UNIBUS, power, and ground.
DD11-B	H033 equipped with three H803 connector blocks to accommodate four SPCs, two serial line interface signal conditioning modules (DF11), a UNIBUS input connector, and a UNIBUS terminator/extender module; prewired for UNIBUS, power, and ground.
H033	Blank four-slot system unit that accommodates three connector blocks; mounts in various module system enclosures.
H933-A	H033 equipped with three H800-W connector blocks to accommodate 24 single-height or 12 double-height modules with contact fingers on only one side.

H933-B	Same as H933-A except equipped with three H800-F connector blocks.
H933-C	Same as H933-A except equipped with three H803 connector blocks.
H933-CA	Same as H933-A except equipped with one H803 and two H863 connector blocks.
H933-CB	Same as H933-A except equipped with three H863 connector blocks.
H933-D	H033 equipped with three H808 connector blocks to accommodate 12 single-height or 6 double-height modules.



NINE-SLOT SYSTEM UNITS

Nine-slot system units, like four-slot system units, are designed to provide mounting sockets (slots) for logic system modules. They, too, are designed to mount in the various module system enclosures offered by Digital Equipment Corporation. Nine-slot system units accept up to six four-slot and three one-slot module connector blocks mounted in three groups (one four-slot, one one-slot, and one four-slot module) mounted end-to-end. Since each of the module connector blocks used with these system units has two rows of slots, a fully complemented nine-slot system unit provides mounting facilities for 54 single-height, 27 double-height, or nine quad-height and 16 single- (or eight double-) height modules.

One of the nine-slot system units (H034) is a bare frame for mounting connector blocks, one (H934-CB) is equipped with connector blocks, and one (BB11-B) is equipped with connector blocks and is prebused for power and ground and prewired for UNIBUS interfacing.

The following table summarizes the nine-slot system units; individual descriptions of these system units are contained in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

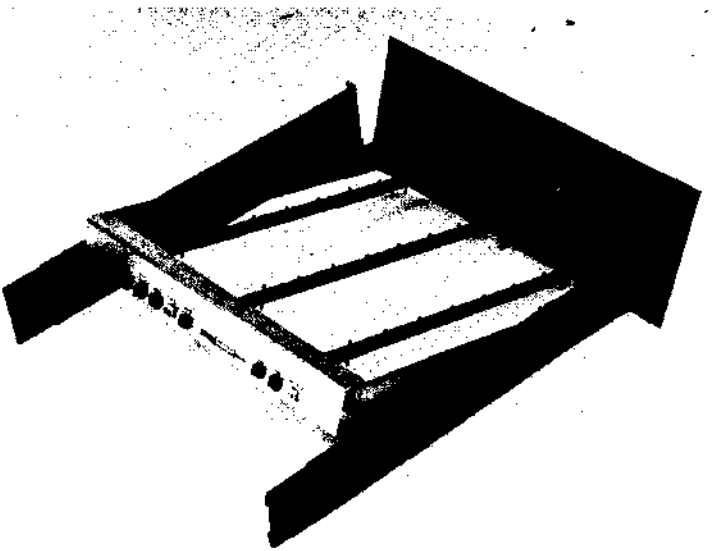
Nine-Slot System Units

Part Number	Description
BB11-B	H034 equipped with six H863 and three H8030 connector blocks to accommodate 54 single-height modules, 27 double-height modules, or nine quad-height and eight double- (or 16 single-) height modules; prewired for UNIBUS, power, and ground. Used for general UNIBUS interfacing.
H034	Blank nine-slot system unit that can accommodate six H863 and three H8030 connector blocks; mounts in various module system enclosures.
H934-CB	Same as BB11-B except not prewired for UNIBUS, power, or ground.

MODULE SYSTEM ENCLOSURES

Module system enclosures are designed to provide mounting space for system units, 19-in. (48.26-cm) rack mounting enclosures, module connector blocks, and power supplies. They provide enough space to accommodate medium-sized systems and offer the convenience of easy access to the system for maintenance and testing.

The following table summarizes the enclosures and associated hardware; individual detailed descriptions of these module system enclosures (except the H909-A and H909-BA) are contained in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation. The H909-A and H909-BA descriptions are included at the end of the following table.



Module System Enclosures

Part Number	Description
BA11-ES	Drawer-type enclosure that accommodates up to six 4-slot system units and an H720 Power Supply. Equipped with four muffin-type cooling fans, tilting chassis slides, and front panel. Accepts extended-length modules; fits 19-in. (48.26-cm) electronics rack.
H035	Vertical system unit mounting frame that accommodates up to six 4-slot or three 9-slot system units. Accepts extended-length modules; mounts in 19-in. (48.26-cm) electronics rack.
H904-A	Horizontal system unit mounting enclosure that accommodates up to two 4-slot or one 9-slot system units. A cooling fan assembly and a rear cover are available. Accepts extended-length modules; mounts in 19-in. (48.26-cm) electronics rack.
H905-A	Similar to H904-A except accommodates up to four 4-slot or two 9-slot system units.
H906	Vertical system unit mounting enclosure that accommodates up to five 4-slot or three 9-slot system units. A cooling fan assembly and a rear cover are available. Accepts extended-length modules; mounts in 19-in. (48.26-cm) electronics rack.
H907-A	Similar to H904-A except accommodates up to eight 4-slot or four 9-slot system units.
H909-A	Drawer-type or table-top enclosure that accommodates one 9-slot system unit and an H755 Power Supply. Equipped with side and top cover plates and a front panel. Equipped with rubber-padded feet for table-top use. Chassis slides are available for mounting the H909-A in a 19-in. (48.26-cm) electronics rack.
H909-BA	Same as H909-A except equipped with an H755 Power Supply.
H920	Drawer-type frame that accommodates up to 24 H800, H803, H808, or H863 module connector blocks or up to 20 Module Connector Blocks and an H710 Power Supply. Equipped with a rear-mounted power distribution panel. Fits in 19-in. (48.26-cm) electronics rack when equipped with H923 Chassis Slides.
H921	Front panel designed to fit the H920 Module Drawer Frame. Occupies 6.9375 in. (17.6213 cm) of vertical space and covers the horizontal space of a 19-in. (48.26 cm) electronics rack.
H923	Chassis slides designed for H920 Module Drawer Frame. Designed to tilt both up and down from the horizontal position. Fits 19-in. (48.26-cm) electronics rack.

Part Number	Description
H925	Drawer-type enclosure that accommodates up to 18 H800, H803, H808, or H863 Module Connector Blocks or up to 14 connector blocks and an H710 Power Supply. Equipped with front panel and non-tilting chassis slides. Accepts extended-length modules; fits 19-in. (48.26-cm) electronics rack.
H930	Drawer-type enclosure that accommodates up to five 4-slot system units and an H750 Power Supply. Equipped with front panel and tilting chassis slides. Accepts extended-length modules; fits 19-in. (48.26-cm) electronics rack.
H941-AA	Mounting panel frame that accommodates up to four 19-in. (48.26-cm) rack mounting panels (H911, H913, H914, H916, H917, or K943). Can be mounted on wall or other convenient surface; has mounting holes on 12 x 22.50 in. (30.48 x 51.15 cm) centers. Two covers, H941-BA and H941-BB, are available.
H941-BA	Cover for H941-AA Mounting Panel Frame. The H941-BA Cover accommodates extended-length modules.
H941-BB	Same as H941-BA except accepts standard-length modules.
12-09154	Chassis slides that provide a 22-in. (55.88-cm) extension for a chassis mounted in an electronics rack. Non-tilting.
12-09703	Chassis slides that provide a 22-in. (55.88-cm) extension for a chassis mounted in an electronics rack. Tilts 90 degrees either up or down.
12-10945	Chassis slides that provide a 19-in. (48.26-cm) extension for a chassis mounted in an electronics rack. The left side of these slides is comprised of two members, one of which can be removed (with the chassis remaining in the rack) to gain access to modules mounted in an H909 enclosure. Non-tilting.

H909-A General Purpose Logic Box

The H909-A General Purpose Logic Box is an enclosure designed to accommodate custom logic subsystems and power supplies and offer the convenience of easy access to the system for maintenance and testing. The box can be used either as a tabletop logic enclosure or, when equipped with optional chassis slides, as a rack mountable unit in any standard 19-inch cabinet. Included with the basic chassis is a top cover, side cover, card guides, cooling fan, cable restraints, and a front bezel.

Additional hardware is available to further increase the versatility of this box: chassis slides, power supply, and a choice of either a nine-slot system unit casting, a nine-slot system unit casting with connector blocks, or a nine-slot prewired unit with UNIBUS busing. These latter items utilize DEC connector blocks (e.g., H863) which, in turn, accommodate single-height through hex-height logic modules. However, the user can mount most any type of logic connector block that meets the dimensions of the H909-A.

Specifications

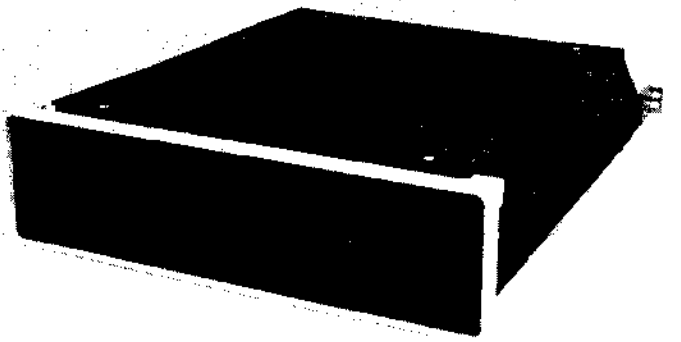
Width: 19 in. (48.26 cm)
Depth: 21 in. (53.34 cm)
Height: 5.25 in. (13.33 cm)
Color: Lamp black

Mounting space available for power supply:
Width —6.25 in. (15.87 cm)
Depth —16 in. (40.64 cm)
Height—4.75 in. (12.06 cm)

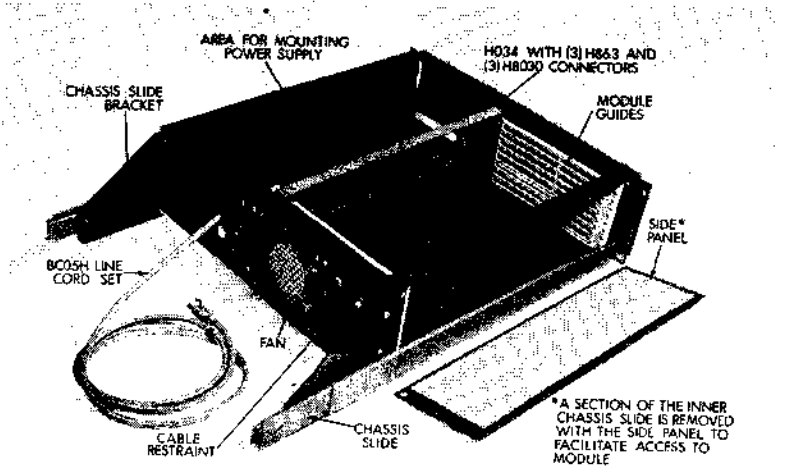
Optional Hardware	DEC Part No.
Chassis slides	12-10945
Required brackets for chassis slides	74-09459 (left) 74-09449 (right)
Nine-slot casting	H034
Nine-slot casting with six H863 and three H8030 Connector Blocks	H934-CB
Nine-slot unit with UNIBUS busing	B811-B
Power Supply, +5 V @ 7 A (mounts on H034 casting, not included)	H726

H909-BA General Purpose Logic Box

The H909-BA General Purpose Logic Box is the same as the H909-A except that it is equipped with an H755 Power Suppy and BCO5H Power Control. The H755 provides +15 Vdc @ 2 A, —15 Vdc @ 2 A, and +5 Vdc @ 17 A. The BCO5H consists of a line cord and circuit breaker.



H909-A


AREA FOR MOUNTING POWER SUPPLY
H034 WITH (3) H863 AND (3) H8030 CONNECTORS
CHASSIS SLIDE BRACKET
MODULE GUIDES
SIDE* PANEL
BC05H LINE CORD SET
FAN
CABLE RESTRAINT
CHASSIS SLIDE
*A SECTION OF THE INNER CHASSIS SLIDE IS REMOVED WITH THE SIDE PANEL TO FACILITATE ACCESS TO MODULE

H909-A

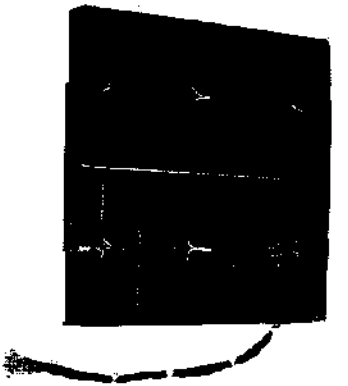
PDP-8/E EXPANSION HARDWARE

An expander frame (H019) and an expander panel (H9190) are available for mounting in a PDP-8/E chassis to provide mounting space for interface or system expansion modules.

The H019 Expander Frame provides mounting facilities for up to 10 module connector blocks of Digital Equipment Corporation types H800, H803, H808, or H863. It is equipped with a power distribution board and a power wiring harness.

The 9190 Expander Panel is the same as the H019 except that it is equipped with ten 288-pin connector blocks (H803) and is prebused for +5 Vdc power and ground.

Individual detailed descriptions of these two items are contained in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.



MODULE CONNECTOR BLOCKS

Digital Equipment Corporation offers a variety of module connector blocks to suit the requirements of almost any logic system. Most M-series systems use H803, 30 AWG, wire wrap blocks for modules with contact fingers on both sides. However, a system requiring 24 AWG interconnections, or using a large number of type 913 Patch Cords, might use H808 Connector Blocks because of the wider spacing of the connector pins. A system using K-series and certain A-series modules (i.e., contact fingers on only one side) can use H800 Connector Blocks. Connector blocks with slotted ends should generally be used in systems where the modules are quad height or larger. The following table summarizes the module connector blocks; individual detailed descriptions of these module connector blocks are contained in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

Module Connector Block Summary

Block Part No.	No. of Slots	Contacts Per Slot	No. of Contact Sides	Wire Wrap Pin Size	Bus Strip No.	Module Type	End
12-10152-1	2	36	2	None*	None	All single-height	Unslotted
H800	8	18	1	24 AWG	932	All single- and double-height; single-sided	Unslotted
H802	1	18	1	24 AWG	932	All single-height single-sided	Unslotted
H803	8	36	2	30 AWG	933	All single- and double-height	Unslotted
H8030	2	36	2	30 AWG	933	All single- and double-height	Slotted
H807	1	36	2	30 AWG	933	All single-height	Unslotted
H808	4	36	2	24 AWG	939	All single- and double-height	Unslotted
H863	8	36	2	30 AWG	933	All single- and double-height	Slotted

* 12-10152-1 is used on a motherboard and the pins are soldered to the printed circuit tracks.

CABLE CONNECTORS

Cable connectors are grouped into eight general classifications according to the type cable they accommodate and their use: flat ribbon cable, flat mylar cable, flat coaxial cable, round coaxial cable, flat shielded cable, round cable, bus interconnection and termination, and miscellaneous connectors. Most of the connectors described in this section are general-purpose connectors; some, however, are specific-use connectors. These connectors are described relative to the specific use. The descriptions of some of the general-purpose connectors cite application examples; the cited examples are popular, widely used applications and are not intended to imply that a particular connector cannot be used with other equipment.

Frequently Digital Equipment Corporation preassembled cable assemblies are available to fulfill your cabling requirements and eliminate the need for you to fabricate a cable assembly. Many preassembled cable assemblies are described in this handbook. Additional preassembled cable assemblies are described in the CABLE PRICE LIST AND CROSS-REFERENCE GUIDE published by Digital Equipment Corporation.

Digital Equipment Corporation also fabricates unique, special-purpose cables according to the customer's specifications to suit almost any requirement. These specially built cable assemblies are completely assembled and tested. Details on special-purpose cables are available from your local DIGITAL sales office or from Digital Equipment Corporation, Components Group, One Iron Way, Marlborough, Ma. 01752.

A cable clamp and two eyelets are supplied with each cable connector. The cable clamp desired should be specified in each order for cable connectors; if cable clamps are not specified, the cable clamp that is usually used with the cable connector will be supplied. Cable clamps are described elsewhere in this publication.

The following tables summarize the cable connectors; individual detailed descriptions and schematic diagrams of these cable connectors are contained in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

Flat Ribbon Cable Connectors

Module	No. of Pins*	No. of Cables	Size	Description
M908	36	2	Single-height, standard length	No contact fingers dedicated to ground; 10-ohm resistors in series with four contact fingers. Split-lug terminals. Similar to M901.
M933	20	1	Single-height, standard length	Twenty signal contact fingers, two ground contact fingers, three power contact fingers. Resistors, capacitors, and jumpers may be installed by user at all signal contact fingers to provide pull-up capabilities to any one of three jumper-selectable voltage fingers, or resistors may be installed by user to provide shunt-to-ground (termination) capabilities at all signal contact fingers. Split-lug terminals for cable conductors and voltage jumpers.
M957	36	2	Single-height, extended length	No contact fingers are dedicated to ground; 32 signal contact fingers; 10-ohm resistors in series with four contact fingers. Split-lug terminals.
M960	14	1	Single-height, standard length	Provides line drivers and pull-up resistors necessary to connect command signals from a TD8-E to a TU56. Requires user installation of jumpers. Sixteen signal contact fingers, one ground contact finger, one +5 V power contact finger. Split-lug terminals. Alternate signal/ground cable conductors. Usually used on cable with an M961 and a 12-10090.
M961	20	1	Double-height, standard length	Provides line drivers and pull-up resistors necessary to connect the data, and "daisy-chained" signals from a TD8-E to a TU56. Fourteen data signal contact fingers, 20 daisy-chained signal contact fingers, eight ground contact fingers, two +5 V power contact fingers. Split-lug terminals. Alternate signal/ground cable conductors. Usually used with an M960 and a 12-10090.

*Cable conductor connections.

Flat Ribbon Cable Connectors (Cont)

Module	No. of Pins*	No. of Cables	Size	Description
M976	120	2	Double-height, short length	Unibus cable connector. Fifty-six signal contact fingers, 14 ground contact fingers. Alternate signal/ground cable conductors. PC solder. Usually used to connect the Unibus to a system unit in an external drawer or cabinet or to a peripheral device. Similar to M919.
M983	36	2†	Double-height, extended length	Thirty-six contact fingers on one side; all can be assigned to signals. Usually used with an RK05. Split-lug terminals.
W011	18	1	Single-height, short length	Nine contact pins dedicated to ground; nine contact pins for signal use. Can be wired for alternate signal/ground configuration. Nineteen split-lug terminals.
W018	18	1	Single-height, short length	All 18 contact pins can be assigned to signals; none are dedicated to ground. A D664 diode is in series with each contact. Eighteen split-lug terminals.
W020	18	1	Single-height, single length	All 18 contact pins can be assigned to signals; none are dedicated to ground. A 1500-ohm resistor is in series with each contact. Eighteen split-lug terminals.
W021	18	1	Single-height, single length	Nine contact pins dedicated to ground; nine contact pins for signal use. Can be wired for alternate signal/ground configuration. Nineteen split-lug terminals.
W022	18	1	Single-height, single length	Nine contact pins dedicated to ground; nine contact pins for signal use. Can be wired for alternate signal/ground configuration. Nine 100-ohm resistors are included to provide a current-limiting capability. Nineteen split-lug terminals.

*Cable conductor connections.
†Cables enter at right angles to the board.

Flat Ribbon Cable Connectors (Cont)

Module	No. of Pins*	No. of Cables	Size	Description
W023	18	1	Single-height, single length	All 18 contact pins can be assigned to signals; none are dedicated to ground. Eighteen split-lug terminals. Two jumpers or resistors must be user-installed in series with contact pins A and B.
W027	18	1	Single-height, single length	All 18 contact pins can be assigned to signals; none are dedicated to ground. A 3000-ohm resistor is in series with each pin. Eighteen split-lug terminals.

Flat Mylar Cable Connectors

Module	No. of Pins*	No. of Cables	Size	Description
M901	36	2	Single-height, standard length	No contact fingers dedicated to ground; 32 signal contact fingers; 10-ohm resistors in series with four contact fingers. PC solder. Similar to M908 and M922.
M903	36	2	Single-height, standard length	Eighteen signal contact fingers, 14 ground contact fingers. Alternate signal/ground cable conductors. PC solder. Similar to M904 and M943.
M915	36	2	Single-height, standard length	Thirty-three signal contact fingers (24 equipped with 390-ohm resistors), two ground contact fingers, one +5 V power contact finger. PC solder.
M918	36	2†	Single-height, standard length	No contact fingers dedicated to ground. Jumpers in series with contact fingers U1 and V1; installation of jumpers or resistors required at contact fingers A2 and B2. PC solder.
M919	120	2	Double-height, standard length	Unibus cable connector. Fifty-six signal contact fingers, 14 ground contact fingers. Alternate signal/ground cable conductors. PC solder. Usually used on a cable with an M929 on the other end. Similar to M976.
M922	36	2	Single-height, standard length	No contact fingers dedicated to ground. Jumpers in series with four contact fingers. PC solder. Similar to M901.
M925	38	2†	Single-height, standard length	Eighteen signal contact fingers, 14 ground contact fingers. Alternate signal/ground cable conductors. PC solder. Similar to M927.
M926	36	2	Single-height, standard length	No contact fingers dedicated to ground. 100-ohm resistors in series with eight contact fingers, 10-ohm resistors in series with four contact fingers. PC solder.

*Cable conductor connections.
†Cables enter at right angles to the board.

Flat Mylar Cable Connectors (Cont)

Module	No. of Pins*	No. of Cables	Size	Description
M929	120	2	Double-height, standard length	Mirror image of M919 and usually used on other end of cable. PC solder.
M936	120	2	Double-height, short length	Omnibus cable connector. Forty-eight signal contact fingers, 16 ground contact fingers. Alternate signal/ground cable conductors. PC solder. Two M936s required for Omnibus extension.
M937	120	2	Double-height, short length	Mirror image of M936 and usually used on other end of cable. PC solder.
M943	32	2†	Single-height, standard length	Eighteen signal contact fingers, 14 ground contact fingers. Alternate signal/ground cable conductors. PC solder. Similar to M903.
M945	120	2	Double-height, short length	UDC system unit to expansion system unit bus cable connector. Fifty-four signal contact fingers, four ground contact fingers. Alternate signal/ground cable conductors. PC solder.
M946	120	2	Double-height, short length	Mirror image of M945 and usually used on other end of cable. PC solder.
M972	36	2	Single-height, extended length	No contact fingers dedicated to ground; 34 signal contact fingers, 10-ohm resistors in series with two contact fingers. PC solder.
W031	16	1	Single-height, short length	Nine contact fingers can be assigned to signals; seven contact fingers are dedicated to ground. Can be wired for alternate signal/ground configuration.
W033	18	1	Single-height, single length	All 18 contact fingers can be assigned to signals; none are dedicated to ground.

*Cable conductor connections.
†Cables enter at right angles to the board.

Flat Coaxial Cable Connectors

Module	No. of Pins*	No. of Cables	Size	Description
M904	26	2	Single-height, standard length	Eighteen signal contact fingers, 14 ground contact fingers. Twenty-six split-lug terminals, eight dedicated to ground. Similar to an M903; similar to ½ of an M912.
M917	30	2†	Single-height, standard length	Eighteen signal contact fingers, 14 ground contact fingers. Thirty split-lug terminals, 12 dedicated to ground.

Round Coaxial (TWP) Cable Connectors

Module	No. of Pins*	No. of Cables	Size	Description
M912	72	2	Double-height, standard length	Thirty-six signal contact fingers, 28 ground contact fingers. Split-lug terminals. Alternate signal/ground cable conductors. Each slot similar to M904.
M927	27	1†	Single-height, standard length	Sixteen signal contact fingers, 16 ground contact fingers. Split-lug terminals. Similar to M925.
W024	18	1	Single-height, short length	Sixteen signal contact fingers, two ground contact fingers. Thirty-three split-lug terminals. Can be wired for alternate signal/ground configuration.
W028	18	1	Single-height, single length	Same as W021 except with split-lug terminals for series or shunt resistors/capacitors in signal leads.

*Cable conductor connections (includes shields).
†Cables enter at right angles to the board.

Flat Shielded Cable Connectors

Module	No. of Pins*	No. of Cables	Size	Description
M953	40	1	Single-height, standard length	Eighteen signal contact fingers, 14 ground contact fingers. Alternate signal/ground cable conductors. Equipped with a connector for solderless connection of the cable.
M954	80	2	Single-height, standard length	None of the contact fingers are dedicated to ground; 32 signal contact fingers; 10-ohm resistors in series with four contact fingers: U1, V1, A2, and B2. Alternate signal/ground cable conductors possible. Equipped with two connectors for solderless connection of the cables.
M955	40	1	Single-height, standard length	None of the contact fingers are dedicated to ground; 16 signal contact fingers; 10-ohm resistors in series with two contact fingers. Alternate signal/ground cable conductors possible. Equipped with a connector for solderless connection of the cable.

Round Cable Connectors

Module	No. of Pins*	No. of Cables	Size	Description
M959	24	1†	Single-height, short length	No contact fingers are dedicated to ground; 24 signal contact fingers. Split-lug terminals.

*Cable conductor connections.
†Cables enter at right angles to the board.

Bus Interconnection and Termination Connectors

Module	No. of Pins*	No. of Cables	Size	Description
M920	N/A	N/A	Double-height, short length dual circuit board	Unibus jumper module.
M935	N/A	N/A	Double-height, short length dual circuit board	Omnibus jumper module.
M981	N/A	N/A	Double-height, standard length, dual circuit board	Unibus terminator module. Terminates all Unibus signals except AC LO L, DC LO L, BG7 H, BG6 H, BG5 H, BG4 H, and NPG H.

*Cable conductor connections.
†Cables enter at right angles to the board.

Miscellaneous Connectors

Module	No. of Pins*	No. of Cables	Size	Description
12-09340-00	8	See Description column	2.3 × 0.85 × 0.3 in. (5.8 × 2.2 × 0.8 cm) nominal	Female connector with up to eight female pins to provide termination for up to eight 20-14 AWG conductors. Equipped with two mounting holes and is usually mounted on a connector board or on the equipment. Requires 12-09379-01 pins. Mates with 12-09340-01 connector. Usually used with TTY and other serial devices.
12-09340-01	8	See Description column	2.2 × 1.5 × 0.3 in. (5.5 × 3.7 × 0.8 cm) nominal	Male connector that mates with 12-09340-00 connector and is usually used to terminate a cable with up to eight 20-14 AWG conductors. Requires 12-09378-01 pins. Usually used with TTY and other serial devices.
12-09350-03, -04,-06,-09, -12, -15	3, 4, 6, 9, 12, or 15	Refer to 12-09350 description in this section	Refer to 12-09350 description in this section	Female connectors that accommodate 3, 4, 6, 9, 12, or 15 female pins to provide termination for 26-14 AWG conductors. Usually bulkhead mounted. Requires 12-09879-01 pins. Mates with 12-09351-03, -04, -06, -09, -12, or -15 connectors. Usually used with TTY and other serial devices.
12-09351-03 -04, -06, -09, -12, -15	3, 4, 6, 9, 12, or 15	Refer to 12-09351 description in this section	Refer to 12-09351 description in this section	Male connectors that mate with 12-09350-03, -04,-06,-09, -12, or -15 connectors and are usually used to terminate a cable with 26-14 AWG conductors. Usually used with TTY and other serial devices.

*Cable conductor connections.

Miscellaneous Connectors (Cont)

Module	No. of Pins*	No. of Cables	Size	Description
H851	N/A	1	Two adjacent slots accommodate 36 single-height contact fingers	Edge connector providing busing of 36 signals of two adjacent modules equipped with top (handle end) contact fingers.
H854	40	1	2.5 × 0.75 × 0.3 in. (4.6 × 1.89 × 0.8 cm) nominal	A 40-pin connector designed to be mounted on a printed circuit board. The pins form right angles to intersect the printed circuit tracks. Mates with H856 connector.
H856	40	1	2.205 × 0.545 × 0.200 in. (5.600 × 1.384 × 0.508 cm) nominal	Designed to terminate a cable and mate with H854 connector.
M9100	80 at H854s	2	Single-height, extended length	Printed circuit cable connector with two 40-pin H854 connectors that mate with cables equipped with H856 connectors. The two H854 connectors and the board contact fingers form a "T" type connector. Thirty-two independent lines available at contact fingers with the remaining contact fingers, usually associated with ground, connected in common.

*Cable conductor connections.

Miscellaneous Connectors (Cont)

Module	No. of Pins*	No. of Cables	Size	Description
M971	40 at one H854	1	Single-height, standard length	Printed circuit cable connector with a 40-pin H854 connector that mates with a cable equipped with an H856 connector. Forty pins of the H854 in series with 36 board contact fingers; i.e., 32 pins of the H854 in series with 32 contact fingers (four with 10-ohm resistors in series) and eight pins of the H854 in series with four contact fingers. No contact fingers dedicated to ground.
M973	4	1	Single-height, standard length	Printed circuit cable connector with a 12-09340-00 connector equipped with four pins. The connector mates with a cable equipped with a 12-09340-01 connector. Normally used as a TTY cable connector.
M975	80 at two H854s	2	Double-height, short length	Printed circuit cable connector with two 40-pin H854 connectors that mate with cables equipped with H856 connectors. Eighteen pins of each H854 in series with 18 board contact fingers; the two H854 connectors are not electrically connected. Six contact fingers and 44 H854 pins dedicated to ground. Alternate signal/ground cable conductors.

*Cable conductor connections.

CABLE CLAMPS

Cable clamps provide strain relief where a cable enters a cable connector. Cable clamps are available for both flat and round cables.

Cable Clamp—12-09764

The 12-09764 cable clamp can be used with flat cable up to 4.562 in. (11.587 cm) wide. Two 0.128-in. (0.325-cm) diameter mounting holes are spaced 4.750 in. (12.065 cm) center-to-center to align with holes on the cable connector; nylon mounting hardware (No. 4 screw and nut) is recommended.

Cable Clamp—12-09925

The 12-09925 cable clamp can be used with module connector block H807 and a round cable. An H807 connector block and a round cable provide a convenient method of terminating a single-height module at a remote location. The 12-09925 cable clamp protects the solder connections of the cable and the connector pins; it also prevents excessive strain on the cable when the module is inserted into or removed from the module connector. The 12-09925 will accommodate cables from 0.290 in. (0.737 cm) to 0.390 in. (0.813 cm) in diameter.

The body of the 12-09925 is equipped with two 6-32 threaded inserts so that the cover of the 12-09925 can be secured to the body.

Cable Clamp—940

The 940 cable clamp can be used with flat cable up to 1.75 in. (4.45 cm) wide. The cable slot is 0.080 in. (0.203 cm) deep. Two 0.128-in. (0.325-cm) diameter mounting holes are spaced 2.000 in. (5.080 cm) center-to-center to align with holes on the cable connector; nylon mounting hardware (No. 4 screw and nut) is recommended.

Cable Clamp—941

The 941 cable clamp can be used with round cable that is 0.281 to 0.438 in. (0.714 to 1.113 cm) in diameter. The 941 cable clamp can also be used where cables require strain relief at the entry point to panels and cabinets. Two 0.136-in. (0.345-cm) diameter mounting holes are spaced 2.000 in. (5.080 cm) center-to-center to align with holes on the cable connector, panel, or cabinet; nylon mounting hardware (No. 4 screw and nut) is recommended.

Cable Clamp—943

The 943 cable clamp can be used with a ribbon cable up to 1.00 in. (2.54 cm) wide. The cable slot is 0.109 in. (0.277 cm) deep. Two 0.128-in. (0.325-cm) diameter mounting holes are spaced 2.000 in. (5.080 cm) center-to-center to align with holes on the cable connector; nylon mounting hardware (No. 4 screw and nut) is recommended.

Cable Clamp—944

The 944 cable clamp can be used with ribbon cables up to 1.00 in. (2.54 cm) wide when two cables require connection to the same side of the connector. The cable slot is 0.219 in. (0.556 cm) deep and can accommodate two ribbon cables. Two 0.128-in. (0.325-cm) diameter mounting holes are spaced 2.000 in. (5.080 cm) center-to-center to align with holes on the cable connector; nylon mounting hardware (No. 4 screw and nut) is recommended.

BLANK MODULE BOARDS

Blank module boards provide a convenient method of breadboarding (mounting) experimental or prototype circuits, and they provide a low-cost method of producing limited runs of production modules with special circuitry. They are completely compatible with the standard module mounting blocks summarized elsewhere in this publication and described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation. These glass epoxy, blank module boards have etched and gold-plated contact fingers and all have handles attached. The attached handles are stamped with their Digital Equipment Corporation identification number (part number). The handles on copper-clad boards are attached with reusable nylon hardware. Blank handle 937, described elsewhere in this publication, is available; this blank handle can be user-titled and is, therefore, particularly useful for identifying user-etched, copper-clad module boards for limited production runs.

Blank module boards are available in three basic forms: plain, perforated, and copper-clad. The following table lists and describes the blank module boards that are available.

Plain blank module boards provide complete flexibility in the placement of components since they are not perforated (predrilled), and they permit easy changes to the circuitry since etching is not required. Component connections are made via hook-up wire. Plain blank boards are, therefore, ideal for experimental or prototype modules because they permit easy changes to the circuitry and nearly unlimited component placement, and yet they provide stability and security for the circuits and components. All sizes are available, and all have etched and gold-plated contact fingers.

Perforated blank module boards provide nearly the same advantage as plain blank module boards except they are predrilled with 0.052-in. (0.132-cm) diameter holes spaced 0.1 in. (0.254 cm) center-to-center horizontally and vertically. This eliminates the need for user drilling and only slightly reduces the choices of component placement. All sizes are available, and all have etched and gold-plated contact fingers.

Copper-clad blank module boards provide a method of producing limited runs of modules with special circuitry and components. A complete selection of copper-clad blank module boards is available: some may be user-etched on both sides and others may be user-etched on one side. All sizes are available, and all have etched and gold-plated contact fingers.

These blank module boards are described in the following table; each of these blank module boards is described in detail in the HARDWARE/ACCESSORIES CATALOG.

Blank Module Boards

Part No.	Type	Contact Fingers	Size	Description
W930	Plain	36	Single-height, extended length	Bare board with 36 feed-through eyelets. Printed circuit etching from the eyelets to the contact fingers.
W970	Plain	36	Single-height, standard length	Bare board with 36 plated-through holes in the printed circuit etching to the contact fingers.
W971	Plain	72	Double-height, standard length	Same as W970 except double-height and has 72 plated-through holes and two handles.
W972	Copper-clad	36	Single-height, standard length	Copper-clad on both sides.
W9720	Copper-clad	36	Single-height, extended length	Same as W972 except extended length.
W9721	Copper-clad	72	Double-height, extended length	Same as W9720 except double-height and has two attached handles.
W9722	Copper-clad	144	Quad-height, extended length	Same as W9720 except quad-height and has four attached handles.
W973	Copper-clad	72	Double-height, standard length	Same as W972 except double-height.
W974	Perforated	36	Single-height, standard length	Perforated board with 36 plated-through holes in the printed circuit etching to the contact fingers.
W975	Perforated	72	Double-height, standard length	Same as W974 except double-height and has 72 plated-through holes and two handles.

Blank Module Boards (Cont)

Part No.	Type	Contact Fingers	Size	Description
W990	Plain	18	Single-height, standard length	Bare board with 18 split-lug terminals. Printed circuit etching from the split-lugs to the contact fingers. This board has contact fingers on one side only.
W991	Plain	36	Double-height, standard length	Same as W990 except double-height and has 36 split-lug terminals and two handles.
W992	Copper-clad	18	Single-height, standard length	Same as W972 except copper-clad on one side only and has contact fingers on one side only.
W993	Copper-clad	36	Double-height, standard length	Same as W973 except copper-clad on one side only and has contact fingers on one side only.
W998	Perforated	18	Single-height, standard length	Same as W974 except has 18 plated-through holes and has contact fingers on one side only.
W999	Perforated	36	Double-height, standard length	Same as W975 except has 36 plated-through holes and has contact fingers on one side only.

WIRE WRAPPABLE MODULE BOARDS

Wire wrappable modules provide a convenient, low-cost method of producing prototype or limited runs of production modules with special circuitry that utilizes, mainly, dual-in-line package (DIP) integrated circuits (ICs). They are completely compatible with the standard module mounting blocks summarized elsewhere in this publication and described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation. These glass epoxy, wire wrappable modules have +5 Vdc power and ground bused (printed circuit etch tracks) to wire wrap pins at each IC location to facilitate connection of V_{cc} and ground to the appropriate IC wire wrap pin. The wire wrap pins each accommodate two 30 AWG wire wraps.

Some of these wire wrappable modules are equipped with low-profile IC sockets that accept either 14- or 16-pin DIP ICs; others accept 14- or 16-pin DIP ICs either with or without sockets; and others, in addition to accepting 14- or 16-pin DIP ICs, are equipped to accept 24-pin DIP ICs. Discrete components, such as transistors and potentiometers, can also be mounted on these wire wrappable boards. These different configurations are described in the following table; each of these wire wrappable modules is described in detail in the HARDWARE/ACCESSORIES CATALOG. All of these modules have etched and gold-plated contact fingers and all have handles attached.

Wire Wrappable Modules

Part No.	Contact Fingers	Size	Description
W940	144	Quad-height, extended length	Accommodates up to fifty 14- or 16-pin DIP ICs with or without sockets. (Sockets not included.)
W941	72	Double-height, extended length	Same as W940 except accommodates up to twenty-five 14- or 16-pin DIP ICs with or without sockets. (Sockets not included.)
W942	144	Quad-height, extended length	Same as W940 except equipped with 50 low-profile, 16-pin DIP IC sockets.
W943	72	Double-height, extended length	Same as W941 except equipped with 25 low-profile, 16-pin DIP IC sockets.
W950	144	Quad-height, extended length	Accommodates up to thirty 14- or 16-pin DIP ICs and up to eight 24-pin DIP ICs with or without sockets. (Sockets not included.)
W951	72	Double-height, extended length	Same as W950 except accommodates up to fifteen 14- or 16-pin DIP ICs and up to four 24-pin DIP ICs with or without sockets. (Sockets not included.) The four 24-pin locations can also accommodate four 14- or 16-pin ICs instead of the 24-pin ICs.
W952	144	Quad-height, extended length	Same as W950 except equipped with 30 low-profile, 16-pin DIP IC sockets and eight 24-pin DIP IC sockets.
W953	72	Double-height, extended length	Same as W951 except equipped with 15 low-profile, 16-pin DIP IC sockets and four 24-pin DIP IC sockets.

PDP-8/E WIRE WRAPPABLE MODULE BOARDS—W966 AND W967

The W966 and W967 are wire wrappable modules designed specifically for the PDP-8/E. Both are quad-height, extended length modules that can accommodate forty-two 14- and/or 16-pin, dual-in-line package (DIP) integrated circuits (ICs). The wire wrappable modules are completely compatible with standard module mounting blocks summarized elsewhere in this publication and described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation. These glass epoxy, wire wrappable modules have +5 Vdc power and ground bused (printed circuit etch tracks) to wire wrap pins at each IC location to facilitate connection of V_{cc} and ground to the appropriate IC wire wrap pins. The wire wrap pins each accommodate two 30 AWG wire wraps.

All power and ground lines are common to the PDP-8/E OMNIBUS. These PDP-8/E wire wrappable modules are described in detail in the HARDWARE/ACCESSORIES CATALOG.

COLLAGE MODULE BOARDS

Collage module boards provide a convenient, low-cost method of producing prototype or limited runs of production modules with special circuitry that uses 14- or 16-pin dual-in-line package (DIP) integrated circuits (ICs), with or without wire wrap sockets and/or solder sockets. Collage module boards are completely compatible with the standard module mounting blocks summarized elsewhere in this publication and described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation. These glass epoxy modules have +5 Vdc power and ground bused (printed circuit etch tracks) to plated-through holes at each IC location to facilitate connection of V_{cc} and ground to the appropriate IC pin.

These collage module boards are described in the following table; each of these collage module boards is described in detail in the HARDWARE/ACCESSORIES CATALOG.

Collage Module Boards

Part No.	Contact Fingers	Size	Description
W968	144	Quad-height, extended length	Accommodates up to seventy-two 14- or 16-pin DIP ICs with or without wire wrap sockets and/or solder sockets.
W969	72	Double-height, extended length	Same as W968 except accommodates 36 ICs.
W979	72	Double-height, standard length	Same as W968 except accommodates 18 ICs.

SPECIAL-PURPOSE BLANK MODULE BOARDS

Special-purpose blank module boards provide pre-etched mounting facilities for user-defined, supplied, and installed components. These special-purpose module boards are low-cost and ideal for prototype and limited-production runs of circuitry unique to each user. They are completely compatible with the standard module mounting blocks summarized elsewhere in this publication and described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation. These glass epoxy module boards have etched and gold-plated contact fingers and all have handles attached. The attached handles are stamped with their Digital Equipment Corporation identification number (part number).

MSI Module Board—W960

The W960 MSI Module Board is a single-height, standard length module board that can accommodate either two 14- or 16-pin dual-in-line package (DIP) integrated circuits (ICs) or one 24-pin DIP IC, either with or without sockets. All IC pin plated-through hole locations are identified with their associated board contact finger and are all brought out to the board contact fingers via printed circuit etching. The W960 is described in detail in the HARDWARE/ACCESSORIES CATALOG.

Universal Terminator Board—W964

The W964 Universal Terminator Board is a single-height, standard length module. It is an etched and drilled module that can be used for mounting user-selected and user-supplied discrete components to provide a variety of termination or voltage source circuits for up to 28 signal pins. Each signal pin can have two components connected to ground and one component connected to a common tie point. Any discrete component can be mounted on the W964 if the physical size is approximately the size of a 1/4-W resistor or disk capacitor. The W964 is described in detail in the HARDWARE/ACCESSORIES CATALOG.

MODULE EXTENDER BOARDS

Module extender boards are usually used to extend system modules for test and/or maintenance. Module extender boards permit access to the system module circuits and components without breaking the electrical connections between the system module and the backplane or mounting panel wiring. Extended length module extender boards should be used when the system comprises extended length system modules. Double-height and quad-height module extender boards should be used when the system module to be extended is double or quad high; however, two single-height module extender boards could be used to extend a double-height system module, or two double-height (or four single-height) module extender boards could be used to extend a quad-height system module. The following table describes the module extender boards. The board contact fingers connect directly to the connector socket pins on a 1:1 basis except as noted in the "Description" column of the table.

Module Extender Boards

Part No.	Contact Fingers	Size	Description
W900	72	Double-height, extended length	Used in systems comprising extended length modules to extend a double-height, 72-pin module with +5 Vdc power at contact fingers AA2 and BA2 and with ground at contact fingers AC2, BC2, AT1, and BT1, i.e., most double-height M-series modules. This is a multilayer module: layer 2 is the ground plane and layer 3 is the +5 Vdc power plane.
W980	18	Single-height, standard length	Used in systems comprising standard length modules to extend a single-height, 18-pin (one side only) module, i.e., most A-, K-, and W-series modules. None of the contact fingers are interconnected.
W982	36	Single-height, standard length	Used in systems comprising standard length modules to extend a single-height, 36-pin module, i.e., single-height M-series modules. None of the contact fingers are interconnected.
W983	72	Double-height, standard length	Used in systems comprising standard length modules to extend a double-height, 72-pin module, i.e., double-height M-series modules. None of the contact fingers are interconnected.
W984	72	Double-height, extended length	The same as W983 except the W984 is an extended length module extender board and should be used to extend a system module located beside one, or between two, extended length modules.
W987	144	Quad-height, extended length	The same as W984 except the W987 is a quad-height module extender board and should be used to extend quad-height (144-pin) modules.

INTEGRATED CIRCUIT (IC) SOCKETS

IC Sockets—953, 954

The 953 and 954 integrated circuit (IC) sockets provide low-cost, reliable production packaging of 14- or 16-pin, dual-in-line package (DIP) integrated circuits (ICs). These low-profile IC sockets are especially useful for limited-production runs of special, user-designed circuitry using the blank or wire wrappable module boards (described in this section), which are available without factory-installed IC sockets. IC sockets 953 and 954 are available in packages of ten IC sockets per package.

The 953 IC socket is fabricated from nylon and has 16 beryllium copper contacts, gold over nickel plating, with wire wrap pins.

The 954 IC socket is fabricated from nylon and has 16 beryllium copper contacts, gold over nickel plating, with solder tail pins.

The 953 and 954 IC sockets are described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

INTEGRATED CIRCUITS (ICs)

Two, 956 and 957, special ICs are available from Digital Equipment Corporation.

DEC8640 Unibus Receiver IC (Quad 2-Input NOR Gates)—956

The 956 is a package of ten 14-pin, dual-in-line package (DIP) DEC8640* integrated circuits (ICs). Each IC comprises four 2-input NOR gates. Each gate performs the Boolean function $\overline{X} = A + B$. The DEC8640 gates are especially suitable as Unibus receivers because of their high impedance characteristics and, hence, minimal loading on the bus.

These NOR gates are described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

DEC8881-1 Unibus Driver IC (Quad 2-Input NAND Gates)—957

The 957 is a package of ten 14-pin, dual-in-line package (DIP) DEC8881-1 integrated circuits (ICs). Each IC comprises four 2-input NAND gates. Each gate performs the Boolean function $\overline{X} = AB$. The DEC8881-1 ICs are especially suitable as Unibus drivers because of their capability to sink 70 mA with a collector voltage of less than 0.8 V.

These NAND gates are described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

*DEC8640 IC replaces DEC380 IC.

MODULE HANDLES, MODULE HANDLE EXTENDERS, AND MODULE HOLDERS

Module Handle—937

The 937 (90-08337-08) is a package containing 25 blank, gray module handles and the eyelets to attach them to modules. These blank handles are generally user-attached to prototype or limited-production run modules that utilize blank copper-clad or wire wrappable modules. The blank handles provide a convenient method of identifying the prototype or limited-production run modules because the user can put his own identification on the handle. The handles are compatible with the handles of all Digital Equipment Corporation standard A-, K-, M-, and W-series modules. They have two 0.128-in. (0.325-cm) diameter mounting holes spaced 2.00 in. (5.08 cm) center-to-center.

Module Handle Extender—H850

The H850 Module Handle Extender mounts over the handle of a single-height, single-length module and physically extends the length to make a single-length module congruous with extended length modules. The H850, in addition to making removal and insertion of single-length modules easier when the system predominantly utilizes extended length modules, adds to the appearance of the system by making the modules the same length.

The H850 is manufactured from durable, U.L. Standard No. 94 recognized material and is sized to fit over Digital Equipment Corporation's standard module handle. It is sold in lots of ten.

Module Holders—H852, H853

The H852 and H853 Module Holders are used to maintain rigidity of the modules in a system. Each module holder fits over the top (handle end) of modules of the same length in adjacent slots of a system unit. The H852, a ribbed type holder, fits between handles of modules in the same connector block; the H853, a nonribbed type holder, fits between the handles of modules in adjacent (end-to-end) connector blocks. For example, on quad-high modules, an H852 fits between handles 1 and 2, an H853 fits between handles 2 and 3, and an H852 fits between handles 3 and 4.

The H852 and H853 are manufactured from durable, plastic-like material that is nonconductive. They are sold in lots of 25 each.

WIRE WRAPPING TOOLS AND ACCESSORIES

Wire wrapping provides positive, uniform electrical connections faster and more economically than solder connections. Digital Equipment Corporation has a complete line of tools and accessories for wire wrapping all of the wire wrappable module connector blocks and all of the wire wrappable module boards summarized elsewhere in this publication and described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

Pistol-Grip Wire Wrapping Tool Kit—H810(24), H810-A, H810-B

The H810(24) Pistol-Grip Wire Wrapping Tool Kit provides a pistol-grip mechanical wire wrapping tool and a sleeve and bit of the proper size to wrap 24 AWG wire wrap wire.

The H810-A is the same as the H810(24) except the sleeve and bit are the proper size for wrapping 30 AWG wire wrap wire.

The H810-B is a combination of H810(24) and H810-A. H810-B provides a pistol-grip mechanical wire wrapping tool and the bits and sleeves of the proper sizes for wrapping 24 AWG or 30 AWG wire wrap wire.

Battery-Powered Wire Wrap Gun—H810-C, H810-D, H810-E

The H810-C, H810-D, and H810-E battery-powered wire wrap guns are equipped with rechargeable, nickel-cadmium batteries. They do not require ac connection while in use. Their ease of operation reduces user-fatigue and provides uniform wire wrap connections.

The H810-C battery-powered wire wrap gun is supplied with a bit and sleeve for wrapping 24 AWG wire wrap wire.

The H810-D is supplied with a bit and sleeve for wrapping 30 AWG wire wrap wire.

The H810-E is supplied without bits or sleeves.

H813 bits and H814 sleeves can be used with any of these battery-powered wire wrap guns.

Hand Wire Wrapping Tool—H811(24), H811-A

The H811(24) and H811-A hand wire wrapping tools are especially useful for service and repair applications. They can also be used for producing limited numbers of prototype modules.

H811(24) is designed for 24 AWG wire wrap wire, and the H811-A is designed for 30 AWG wire wrap wire.

Hand Wire Unwrapping Tool—H812(24), H812-A

The H812(24) and H812-A hand unwrapping tools are ideal for unwrapping wire strapped terminals.

The H812(24) is designed for unwrapping 24 AWG wire, and the H812-A is designed for unwrapping 30 AWG wire.

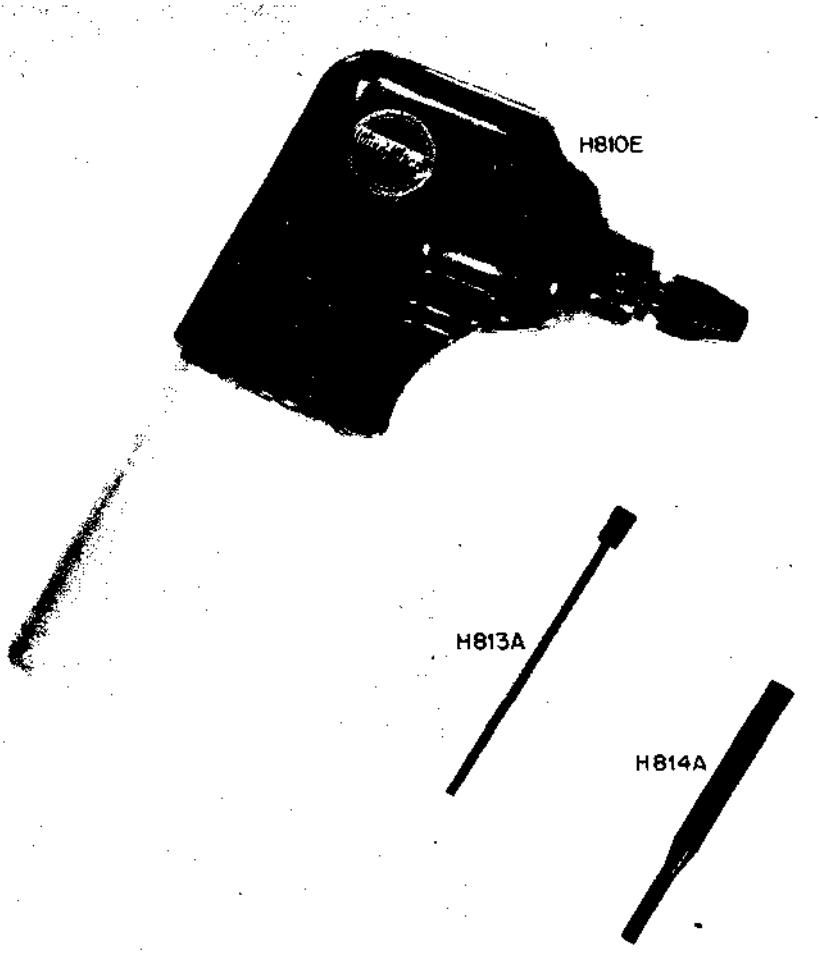
Bit for Battery-Powered Wire Wrap Gun—H813(24), H813-A

The H813(24) and H813-A bits are replacement bits for battery-powered wire wrap guns H810-C, H810-D, or H810-E.

The H813(24) is designed for 24 AWG wire, and the H813-A is designed for 30 AWG wire.

Sleeve for Battery-Powered Wire Wrap Gun—H814(24), H814-A
The H814(24) and H814-A sleeves are replacement sleeves for battery-powered wire wrap guns H810-C, H810-D, or H810-E.

The H814(24) is designed for 24 AWG wire ,and the H814-A is designed for 30 AWG wire.



BUS STRIPS

Bus Strips—932, 933, 939

Bus strips 932, 933, and 939 provide a convenient method of interconnecting all wire wrap pins in a system that are assigned identical control signals, power, or ground. These bus strips are flat, narrow conductors with holes that correspond to the connector block pin size and spacing. When a bus strip is placed over the pins and soldered to each, it will interconnect all of the pins with the same pin number for as many module slots as desired. After the modules have been selected and the slots of the mounting panel have been assigned to the modules, identical control signal, power, and ground pins can be bused with the bus strips.

Bus strip 932 can be used to bus systems using H800 Module Connector Blocks. Bus strip 933 can be used to bus systems using H803, H8030, and H863 Module Connector Blocks. Bus strip 939 can be used to bus systems using H808 Module Connector Blocks. Module connector blocks are summarized elsewhere in this publication and are described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

Length: 932 — 13.5 in. (39.4 cm)
933 — 21.5 in. (54.6 cm)
939 — 21.5 in. (54.6 cm)

PATCH CORDS AND ACCESSORIES

Grip-Clip Connectors for Slip-on Patch Cords—H820, H821

The H820 and H821 grip-clip connectors are identical to the connectors used on each end of 913 and 915 patch cords, respectively. These grip clips permit the fabrication of patch cords of any length.

H820 grip-clip connectors accept 24 to 20 AWG wire; they slip on wire wrap terminals that are sized for 24 AWG wire wrap wire, 0.031 by 0.062 in. (0.079 by 0.158 cm). H821 grip-clip connectors accept 30 to 24 AWG wire; they slip on wire wrap terminals that are sized for 30 AWG wire wrap wire, 0.025 in. (0.064 cm) square.

H820 and H821 grip-clip connectors are shipped in quantities of 1000 of one size.

Hand Crimping Tool—H825, H826

The H825 and H826 hand crimping tools can be used to secure H820 and H821 grip-clip connectors to the wire. These tools ensure good electrical connections quickly and easily.

The H825 hand crimping tool should be used to crimp H820 connectors to 24 to 20 AWG wire. The H826 hand crimping tool should be used to crimp H821 connectors to 30 to 24 AWG wire.

Patch Cords—913, 915

The 913 and 915 patch cords provide slip-on connections at the wire wrap pins of FLIP-CHIP modules and module connector blocks. They are ideal for breadboarding prototype modules and making temporary or semipermanent jumpers at a system backplane. They are available in 11 color-coded lengths from 2 to 64 inches (5.04 to 162.56 cm).

Patch cord 913 is 24 AWG stranded wire with IPVC insulation, and is equipped on each end with an H820 grip-clip connector; H820 connectors fit on wire wrap pins that are sized for 24 AWG wire wrap wire, 0.031 by 0.062 in. (0.079 by 0.158 cm).

Patch cord 915 is 26 AWG stranded (7/34) with IPVC insulation, and is equipped on each end with an H821 grip-clip connector; H821 connectors fit on wire wrap pins that are sized for 30 AWG wire wrap wire, 0.025 in. (0.064 cm) square.

Patch cords 913 and 915 are available in quantities of 100 of the same length and same gauge, and in quantities of 100 of assorted lengths and the same gauge. The following chart lists the part number, length, and color code for 913 and 915 patch cords.

Part Number		Length in Inches (Centimeters)	Color
24 AWG	26 AWG		
913-2	915-2	2 (5.08)	BRN
913-3	915-3	3 (7.62)	BRN/WHT
913-4	915.4	4 (10.16)	RED
913-6	915-6	6 (15.24)	RED/WHT
913-8	915-8	8 (20.32)	ORN
913-12	915-12	12 (30.48)	ORN/WHT
913-16	915-16	16 (40.64)	YEL
913-24	915-24	24 (60.96)	YEL/WHT
913-32	915-32	32 (81.28)	GRN
913-48	915-48	48 (121.92)	GRN/WHT
913-64	915-64	64 (162.56)	BLU
913-AF	915-AF	Assorted*	Assorted

* 913-AF and 915-AF comprise the following assorted patch cords: 30 BRN/WHT (-3); 25 RED/WHT (-6); 25 ORN (-8); 10 YEL/WHT (-24); 5 GRN (-32); and 5 BLU (-64).

When ordering, please specify part number 913 or 915 and the appropriate *dash* number.

Power Patch Cord—914-7, 914-19

The 914 power patch cords provide interconnections between power supplies and mounting panels that are equipped with Faston (TM) terminals, series 250. The 914 power patch cord is stranded wire with IPVC insulation and is equipped on each end with Faston receptacles, series 250. Power patch cord 914 is available in two lengths—7 inches and 19 inches (18 cm and 48 cm)—and is available in packages of ten of the same length. The 914-7 is a package of ten 7-inch (18-cm) patch cords. The 914-19 is a package of ten 19-inch (48-cm) patch cords.

Daisy Chain—917-2.5, 917-5

The 917 daisy chain is a continuous length of stranded insulated wire on a reel with 250 gold-plated and insulated terminals crimped at 2.5-in. (6.4-cm) or 5.0-in. (12.7-cm) intervals. A prototype system is easily and quickly hand patched when the 917 daisy chain is used.

(TM) Faston is a trademark of AMP, Inc.

The terminals are designed to fit on module connector blocks that have wire wrap pins sized for wrapping with 30 AWG wire [0.025/0.026 in. (0.064/0.066 cm) square] e.g., module connector blocks H803, H8030, H807, and H863, summarized elsewhere in this publication and described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

The dependable 917 daisy chain push-on terminals are easily removed from the connector block wire wrap terminals; this provides an ideal wiring technique in systems where unwiring and rewiring for changing system requirements are essential. If an additional lead is ever required on a wire wrap terminal, a 915 patch cord can be used; a 915 patch cord can be placed on the terminal after the wire wrap connection and before the 917 termination.

The 917-2.5 daisy chain has 250 terminals at 2.5-in. (6.4-cm) intervals.

The 917-5 daisy chain has 250 terminals at 5-in. (12.7-cm) intervals.

WIRE

30 AWG Wire Wrapping Wire—91-05740

Thirty AWG solid conductor wire is available on 1000-ft (304.8-m) spools for wire wrapping logic system backplane pins. This wire is excellent for wire wrapping H803, H8030, H807, and H863 Module Connector Blocks summarized in this publication and described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

Complete specifications for 91-05740 wire wrapping wire are contained in the HARDWARE/ACCESSORIES CATALOG.

NOTE

This wire should not be used for solder applications. 91-07470-44 wire, also described in this publication, should be used for solder applications.

24 AWG Hookup (Solder) Wire—91-07470-44

Twenty-four AWG solid conductor wire is available on 1000-ft (304.8-m) spools for soldering logic system backplane pins. This wire is excellent for soldering H800-F Module Connector Blocks summarized in this publication and described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

Complete specifications for 91-07470-44 wire wrapping wire are contained in the HARDWARE/ACCESSORIES CATALOG.

24 AWG Wire Wrapping Wire—91-07688

Twenty-four AWG solid conductor wire is available on 1000-ft (304.8-m) spools for wire wrapping logic system backplane pins. This wire is excellent for wire wrapping H800, H802, and H808 Module Connector Blocks summarized in this publication and described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation.

Complete specifications for 91-07688 wire wrapping wire are contained in the HARDWARE/ACCESSORIES CATALOG.

NOTE

This wire should not be used for solder applications. 91-07470-44 wire, also described in this publication, should be used for solder applications.

CABLE ASSEMBLIES

DIGITAL provides a complete line of preassembled cable assemblies which are compatible with Digital Equipment Corporation and customer-supplied equipments. Most of these cable assemblies are available in customer-specified lengths.

The connectors referenced with each cable are summarized elsewhere in this section and are described in detail in the Hardware/Accessories Catalog published by Digital Equipment Corporation.

The number following the dash in each cable listing denotes the cable length in feet. The xx suffix indicates the cable is available in most any length specified by the customer.

Single-Sided Connectors—20-Conductor Ribbon Cable

Type	Connectors
BC02A-xx	W011-W011
BC02B-xx	W011-W021
BC02E-xx	W011-W028
BC02K-xx	W020-W023
BC02L-xx	W021-W021
BC02M-xx	W021-W022
BC02N-xx	W021-W028
BC02P-xx	W022-W022
BC02T-xx	W023-W027
BC02U-xx	W024-W024
BC02W-xx	W028-W028
BC02Y-xx	W011-W021
BC04A-xx	W011-Open End
BC04B-xx	W018-Open End
BC04C-xx	W020-Open End
BC04D-xx	W021-Open End
BC04E-xx	W022-Open End
BC04F-xx	W023-Open End
BC04H-xx	W024-Open End
BC04J-xx	W027-Open End
BC04K-xx	W028-Open End

Single-Sided Connectors—9-Conductor Flat Coax Cable

Type	Connectors
BC03A-xx	W011-W011
BC03B-xx	W011-W021
BC03C-xx	W021-W021
BC03D-xx	W021-W022
BC03J-xx	W021-W028
BC04L-xx	W021-Open End
BC04M-xx	W021-Open End
BC04N-xx	W022-Open End

Single-Sided Connectors—19-Conductor Flat Mylar Cable

Type	Connectors
BC03E-xx	W031-W031
BC03F-xx	W033-W033

Double-Sided Connectors—Two 19-Conductor Cables (except as noted)

Type	Connectors
BC03H-xx	M901-M901
BC04T-xx	M901-Open End
BC04U-xx	M903-Open End
BC08A-01	M903-M903
BC08A-03	M903-M903
BC08A-05	M903-M903
BC08A-07	M903-M903
BC08A-10	M903-M903
BC08A-15	M903-M903
BC08A-25	M903-M903
BC08C-01	M903-2/W031
BC08C-03	M903-2/W031
BC08C-05	M903-2/W031
BC08C-07	M903-2/W031
BC08C-10	M903-2/W031
BC08C-15	M903-2/W031
BC08C-25	M903-2/W031
BC08E-xx (one cable)	W031-W031
BC08F-06	M903-M925

Double-Sided Connectors—Two 20-Conductor Ribbon Cables

Type	Connectors
BC02X-xx	M908-M908
BC04W-xx	M908-Open End
BC07D-10	H856-Open End
BC07D-15	H856-Open End
BC07D-25	H856-Open End

Double-Sided Connectors—Two 9-Conductor Flat Coax Cables

Type	Connectors
BC04P-xx	M904-Open End
BC08B-01	M904-M904
BC08B-03	M904-M904
BC08B-05	M904-M904
BC08B-07	M904-M904
BC08B-10	M904-M904
BC08B-15	M904-M904
BC08B-25	M904-M904
BC08D-01	M904-2/W011
BC08D-03	M904-2/W011
BC08D-05	M904-2/W011
BC08D-07	M904-2/W011
BC08D-10	M904-2/W011
BC08D-15	M904-2/W011
BC08D-25	M904-2/W011

Single-Sided Connectors—40-Conductor Flat Mylar Cable (18 signals with alternate grounds)

Type	Connectors
BC08J-06	M953-H856
BC08J-10	M953-H856
BC08J-15	M953-H856
BC08J-25	M953-H856
BC08J-50	M953-H856
BC08K-06	M955-H856
BC08K-10	M955-H856
BC08K-15	M955-H856
BC08K-25	M955-H856
BC08K-50	M955-H856

Double-Sided and 40-Pin Connectors—Two 40-Conductor Flat Mylar Cables (36 signals)

Type	Connectors
BC08L-06	M954-2/H856
BC08L-10	M954-2/H856
BC08L-15	M954-2/H856
BC08L-25	M954-2/H856
BC08L-50	M954-2/H856

H856 40-Pin Connectors—40-Conductor Flat Mylar Cable

Type	Connectors
BC04Z-xx	H856-Open End
BC08R-xx	H856-H856

BC08H OMNIBUS Cable

The BC08H Cable consists of two 60-conductor, flat mylar Flexprint cables used to connect system units in different mounting drawers or to connect peripheral devices not located within the drawer.

This cable accommodates one-half of the OMNIBUS signals and one-half of the ground lines; two BC08H cables are required to extend the complete OMNIBUS.

Flat Mylar Cables
(60-Conductor—Double)

Type	Connectors
BC08H-03F	M936-M937
BC08H-04 F	M936-M937

BC11A UNIBUS Cable

The BC11A Cable consists of two 60-conductor, flat mylar Flexprint cables used to connect system units in different mounting drawers or to connect peripheral devices not located within the drawer.

This cable accommodates all 56 UNIBUS signals and 64 ground lines.

Flat Mylar Cables
(60-Conductor—Double)

Type	Connectors
BC11A-02	M919-M929
BC11A-05	M919-M929
BC11A-08F	M919-M929
BC11A-10	M919-M929
BC11A-15	M919-M929
BC11A-20	M919-M929
BC11A-25	M919-M929
BC11A-35	M919-M929
BC11A-50	M919-M929

TTY, DECKit, and Other Serial Device Cables

Type	Connectors	Cable
BC05C-25	H856-Cinch #DB-25P*	25-Conductor, Round
BC05C-35	H856-Cinch #DB-25P*	25-Conductor, Round
BC05C-45	H856-Cinch #DB-25P*	25-Conductor, Round
BC05C-50	H856-Cinch #DB-25P*	25-Conductor, Round
BC05C-60	H856-Cinch #DB-25P*	25-Conductor, Round
BC05C-70	H856-Cinch #DB-25P*	25-Conductor, Round
BC05D-10	Cinch #DBM-25S-Cinch #DB-25P*	25-Conductor, Round
BC05D-25	Cinch #DBM-25S-Cinch #DB-25P*	25-Conductor, Round
BC05F-xx	12-09340-01—12-09340-01	4-Conductor, Round
BC05X-xx	12-09340-00—12-09340-01	4-Conductor, Round
BC07A-10	H856-Open End	20-TWP, Round
BC07A-15	H856-Open End	20-TWP, Round
BC07A-25	H856-Open End	20-TWP, Round
BC07B-10	H856-Open End	11-TWP, Round
BC07B-15	H856-Open End	11-TWP, Round
BC07B-25	H856-Open End	11-TWP, Round
BC07C-10	H856-Open End	10-TWP, Round
BC07C-15	H856-Open End	10-TWP, Round
BC07C-25	H856-Open End	10-TWP, Round
BC11K-25	H856-Open End	20-TWP, Round
BC14F-05	12-11354**—12-11390*	25-Conductor, Round
BC14F-10	12-11354**—12-11390*	25-Conductor, Round
BC14F-15	12-11354**—12-11390*	25-Conductor, Round
BC14F-25	12-11354**—12-11390*	25-Conductor, Round
BC70A-15	44-Pin***—Cinch #DB-25P*	10-Conductor, Round
BC70B-15	44-Pin****—Open End	Two 11-TWP, Round

*Mates with female connector with sockets conforming to EIA Specification RS-232-C or CCITT Recommendation V.25, or to 12-11354 or Cinch #DBM-25S connector.

**Mates with male connector with pins conforming to EIA Specification RS-232-C or CCITT Recommendation V.25, or to 12-11390 or Cinch #DB-25P connector.

***Mates with edge connector on PDM70-J or -JR options.

****Mates with edge connector on all PDM70 options.

POWER SUPPLIES, POWER CONTROLLERS, AND STEP-DOWN TRANSFORMERS

The electrical and mechanical features of a complete line of power supplies, power controllers, a step-down transformer, and power supply accessories are summarized in the following tables and paragraphs. These items are described in detail in the HARDWARE/ACCESSORIES CATALOG published by Digital Equipment Corporation. The following three paragraphs and tables summarize the power supplies according to their usual use. The fourth paragraph and table summarizes the power controllers and a step-down transformer. Power supply accessories are summarized in the fifth paragraph and table.

+5 Vdc POSITIVE LOGIC POWER SUPPLIES

These +5 Vdc positive logic power supplies are designed to provide V_{cc} (+5 Vdc) to the integrated circuits mounted on modules used in logic systems and interfaces. Many small systems and most interfaces comprise M-series gating, multiplexing, bus receivers, and bus transmitter modules that require only a V_{cc} power supply. The power supplies summarized in this table are ideal for these applications because of such features as overvoltage and short circuit protection, remote sensing, and input voltage ranges.

+5 Vdc Positive Logic Power Supplies

Part No.	Input Specs	Output Specs	Dimensions	Features
H710	105-125 Vac 210-250 Vac (47-63 Hz)	+5 Vdc @ 5 A, 1% regulation	8 in. long × 6 in. high × 5.25 in. deep (20.32 × 15.24 × 13.34 cm)	Short circuit proof Floating output Remote sensing Overvoltage protection
H716	120 Vac 240 Vac (47-63 Hz)	+5 Vdc @ 4.0 A, 3% regulation −15 Vdc @ 1.5 A, 5% regulation	5.25 in. long × 4.125 in. high × 12.00 in. deep (13.34 × 10.48 × 30.48 cm)	Floating output Short circuit proof Overvoltage protection for +5 Vdc output
H726-B	120/240 Vac (47-500 Hz)	+5 Vdc @ 7.0 A, 1% regulation	16.50 in. long × 2.23 in. high × 6.25 in. deep (41.91 × 5.66 × 15.88 cm)	Floating output Short circuit proof Parallel operation Overvoltage protection

ANALOG POWER SUPPLIES

Analog power supplies are designed to provide ±15Vdc for operational amplifiers and D/A and A/D converters used in analog systems. The power supplies summarized in this table are ideal for these applications because of their accuracy and regulation.

Analog Power Supplies

Part No.	Input Specs	Output Specs	Dimensions	Features
H704-A	105-125 Vdc (47-420 Hz)	±15 Vdc outputs @ 400 mA, 0.1% regulation	7.75 × 4.0 × 3.81 in. (19.68 × 10.16 × 9.67 cm)	Two 15 V floating outputs Overload protection Remote sensing
H707	Same as H704-A	±15 Vdc outputs @ 1.5 A, 0.1% regulation	5.5 in. × 5.0 in. × 4.0 in. (13.97 × 12.70 × 10.16 cm)	Same as H704 plus fuse holder

SYSTEM POWER SUPPLIES

System power supplies are designed to provide V_{cc} (+5 Vdc) and reference voltages to an entire system or to a large interface when spare power is not available from the system supply. The power supplies summarized in this table are ideal for these applications because of their high current output capabilities and voltage output ranges.

System Power Supplies

Part No.	Input Specs	Output Specs	Features
H720-C 19-in. (48.26-cm) panel-mounted	120 Vac, 47-63 Hz	+5 V @ 22 A −15 V @ 10 A +8 V (avg) @ 1.5 A −25 V @ 1.5 A	Ac frequency monitor Ac or dc low voltage detection Overvoltage and overcurrent protection
H720-D (Same as H720-C)	240 Vac, 47-63 Hz	Same as H720-C	Same as H720-C
H720-E (BA11-C or BA11-E Mounting Box)	120 Vac, 47-63 Hz	+5 V @ 22 A −15 V @ 10 A +8 V (avg) @ 1.5 A −22 V @ 1.5 A	Input frequency monitor Ac and dc low power detection Overvoltage and overcurrent protection
H720-F (Same as H720-E)	240 Vac, 47-63 Hz	Same as H720-E	Same as H720-E
H721 19-in. (48.26-cm) panel-mounted	88-132 Vac/176-264 Vac, 47-63 Hz	+5 V @ 20 A −15.5 V @ 3.5 A +10.5 V @ 2.5 A	20 ms hold-up on dc outputs
H740-D 19-in. (48.26 cm) panel-mounted	115 Vac/230 Vac, 47-63 Hz	+5 V @ 17 A −15 V @ 5 A +15 V @ 1.0 A	Ac frequency monitor Ac and dc low voltage detection

POWER CONTROLLER AND STEP-DOWN TRANSFORMER

A power controller and a power transformer are summarized in this table. The power controller is ideal for distributing ac power within a system; the power transformer is ideal for stepping down commercial power to 115 Vac for use within a system.

Power Controllers and Step-Down Transformer

Part No.	Input Specs	Output Specs	Features
861-A	90-130 Vac, 2 phase, 16 A/pole	90-130 Vac at 12 A (each ac outlet)	Local or remote control Four switched, dual receptacles
861-B	180-270 Vac, single phase, 16 A/pole	180-270 Vac at 12 A (each ac outlet)	Two unswitched, dual receptacles
861-C	90-130 Vac, single phase, 24 A/pole	90-130 Vac at 12 A (each ac outlet)	19-in. (48.26-cm) mounting-rail mounted
H722	115, 189, 200 217, 230, 245 Vac	115 Vac at 4.0 A	19-in. (48.26-cm) panel-mounted

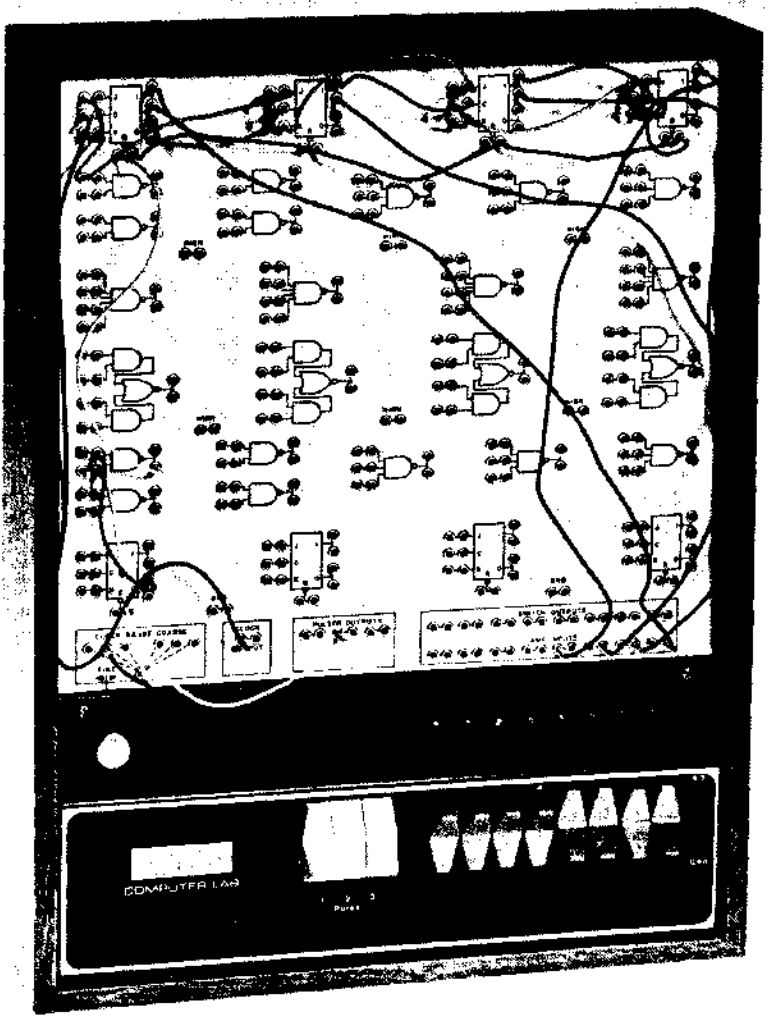
POWER SUPPLY ACCESSORIES

Line sets and ac receptacles are summarized in this table. The ac receptacles are wall-mounted and are designed to mate with the plug on the ac input cords of some power supplies. These receptacles are offered in this handbook because they may not be available in local supply stores. The line sets are ac input power cords terminated with an ac input box on one end; the line sets are specifically designed for use with H740-D Power Supplies. Also available is the H322 Distribution Panel, which can be mounted in a cabinet to distribute signals, power, and ground to one or more devices.

Power Supply Accessories

Part No.	Use	Specifications
12-11046	Receptacle that mates with ac input plug on Power Controller 861-A	125/250 V, 20 A 4-prong
12-11191	Receptacle that mates with ac input plug on Power Controller 861-B	250 V, 20 A 3-prong
12-11194	Receptacle that mates with ac input plug on Power Controller 861-C	125 V, 20 A 3-prong
BC05H-6	Line set designed to connect 115 Vac input to Power Supply H740-D	115 Vac 6-ft. (1.8-m) power cord
BC05J-6	Line set designed to connect 230 Vac input to Power Supply H740-D	230 6-ft. (1.8-m) power cord
H322	Distribution panel designed to provide general-purpose signal, power, and ground distribution from one or more devices to one or more devices.	Fits 19-in. (48.26-cm) rack. Two 40-pin H854 and two 9-pin 12-09350-09 connectors and nine 10-screw terminal strips.

lab series


COMPUTER LAB

COMPUTER LAB

LAB SERIES

The COMPUTER LAB is a high performance low-cost digital logic trainer. It uses the same monolithic integrated transistor-transistor logic circuitry used in DIGITAL's latest computers.

The digital logic fundamentals presented by the COMPUTER LAB can foster a basic understanding of computer technology for the computer career oriented user, or for a user applying computers for the first time. The COMPUTER LAB will also help the math-oriented user understand "new math" concepts, as computer logic operates with binary numbers according to Boolean algebraic laws.

Wiring is easy because of the standard logic symbology used on the front panel and the color coded Patchcords which are easily inserted and removed. An improper circuit will not damage the COMPUTER LAB. The faulty circuit merely "waits" for correction.

Once a logic configuration has been wired, it can be tested by using one of three pulser switches to supply momentary signals to the logic elements or by using one of eight rocker switches to supply sustained signals. A variable frequency clock is also available for supplying test signals and for synchronizing some of the more complex experiments. The eight indicator lamps may be wired into the circuit to provide a visual indication of the state of the logic at any point.

Features

- Transistor—Transistor logic circuitry as used in DIGITAL's PDP computers
- Teaches modern computer logic
- Easy to use: MIL-STD 806 logic symbology on front panel
- Portable: Dimensions of 12.5 in. (36.7 cm) w x 17 in. (43 cm) h x 3.25 (8.25 cm) d, weighing only 11 lbs. (5 kg)
- Comprehensive Workbook provides:
  - —Ten detailed chapters
  - —More than 30 experiments
  - —Over 200 hours of laboratory study
  - —Dozens of tables and diagrams
  - —An extensive appendix of supplementary information
- Instructor's Guide with answers, additional text, extra problems, course plans. Order no. B-400 (additional charge).

Model No.	Vac Operation
H500	115 Vac, 60Hz
H500-A	230 Vac, 50Hz

The DEClab-RT

DEClab-RT

LAB SERIES

The DEClab-RT is a highly versatile training unit that offers the user a functional approach to understanding digital system design utilizing the register transfer concept. (Refer to Register Transfer Modules section in this handbook.) A DEClab-RT consists of a series of functional sequential logic building blocks designated Register Transfer Modules (RTM) which obviate the need for conventional combinatorial and sequential logic design. The companion textbook/workbook for the DEClab-RT is *Designing Computers and Digital Systems Using PDP-16 Register Transfer Modules.*

Five functional building block sections comprise the DEClab-RT:

General Purpose Arithmetic Unit—Provides for manipulation of two or more 16-bit registers and performs both Boolean and arithmetic operations (Modules M7300 and M7301).

Bus Sense—Performs such functions as detect positive, negative, and zero by monitoring all bus transfers. Also contains bus terminations and initializing circuits plus other essential system functions.

Memory—Includes a variety of bipolar RAM devices such as M7318, a 16 x 16 scratch pad; M7319, a 16 x 256 scratch pad; and M7324, a 16 x 1K scratch pad.

Interfaces—A set of functional devices for parallel or serial interfacing. Includes Modules M7311, a general-purpose interface, and M7313, a serial I/O register.

Controls—These are the system control functions which define the solution to a particular computational problem. The control devices include evoke (M7310), two-way branch (M7312), eight-way branch (M7314), subroutine return (M7315), two-input OR gate (M1103), and four-input OR gate (M1307).

To fully implement the many RTM designs and applications as outlined in *Designing Computers and Digital Systems Using PDP-16 Register Transfer Modules*, DIGITAL has assembled a number of RTM modules in two kits.

RTKIT-1 (Basic Kit)

Qty.		
1	M7334	Light Interface and Switch Control Module including two 70-2222-3 foot Cables
2	M1307	Four-Input OR Gate
1	M1103	Two-Input OR Gate
1	M7315	Subroutine Return
1	M7306	Flags Module
3	M7312	Two-way Branch

6	M7310	Evoke Units
1	M7332	Bus Control and Terminator
1	M7300	General Purpose Arithmetic Unit Control
1	M7301	General Purpose Arithmetic Registers
1	H8513	Edge Connector Used to Connect M7300 and M7301.
1	M7318	16 x 16 Scratch Pad Memory
1	H914 RTM	19-inch Mounting Panel (Bused for Power, Data, and Control Lines)

2 Pkgs. 913-AF Patchcords, Assorted Sizes (100 per Package) for Use with 24-Gauge Pins.

NOTES:

1) A +5V 7A, DC power supply is required for the RTM modules. This type of power supply is readily available in most engineering labs. If a power supply is needed, consult Product Index.
2) H914-RTM mounting panel houses eight low-density connector blocks having 24-gauge connector pins. The H914-RTM is readily mounted in standard 19-inch racks. (Mounting racks, part no. 4913, are ideal 19-inch benchtop racks.)

RTKIT-2 (Expander Kit)

Qty.		
1	M7313	Serial I/O Register (TTY)
1	M7319	16 x 256 Scratch Pad Memory
1	M7311	General Purpose Interface
1	M7305	Transfer Register
1	M7314	Eight-way Branch
1	M7333	Serial Interface Adapter
1	M7307	Constants Generator 4 x 16

NOTE: The M7313 and M7319, in addition to the +5 Vdc power source, require a −15 or −12 DC volt power source.

about digital equipment corporation

In approximately 17 years, DIGITAL EQUIPMENT CORPORATION has grown from three employees and one floor of production space in a converted woolen mill, to a major international corporation. DIGITAL now employs more than 18,000. Our products are manufactured in several plants, and are sold and serviced from customer support centers in the United States, Canada, Japan, Australia and seven European countries.

We produce a wide variety of computer and control products ranging from logic modules to large time sharing computer systems. In addition to those logic modules and associated equipment detailed in this handbook, DIGITAL also manufactures 12-, 16-, 18- and 36-bit computers, peripheral devices, special systems, accessories, programmable controllers and a wide variety of software.

DIGITAL first began manufacturing computer-related equipment in 1957 when we introduced a line of solid state logic modules. These were initially used to test and build other manufacturers' electronic equipment. The logic module product lines have been continually broadened, and DIGITAL now ranks as the world's largest manufacturing supplier of digital logic modules, producing more than three million per year.

Our first computer, the PDP-1 was introduced over a decade ago, selling for $120,000 while competitive machines were priced over $1 million. Ever since the PDP-1, DIGITAL has specialized in on-line, real-time computers.

The PDP-5, introduced in 1963, was the first truly small computer. The PDP-8 series, the PDP-5 successor announced in 1965, is one of the most popular and successful families of computers ever produced.

The PDP-11 sixteen-bit computer also ranks as the industry leader of medium-sized systems.

DIGITAL is a leading force in small computers, but it also has been a pacesetter in other parts of the industry. For example, one of the first time sharing systems ever built incorporated a PDP-1. DITIGAL introduced the first large-scale, commercially available time sharing system in 1965—the PDP-6. Its successor, the DECsystem-10, can do more at a price well under $1 million than competitive systems costing several times as much.

With more than 30,000 computers now installed, DIGITAL is the second largest manufacturer in terms of installations.

In industry, DIGITAL computers provide engineers with a powerful control and testing tool. They control blast furnaces and open hearths, monitor slab mills and finishing mills, and control and monitor a variety of machine tools, transfer and material handling equipment. DIGITAL computers guided the SS MANHATTAN as she sailed the Northwest Passage, and are being used in testing the Boeing 747 jumbo jet, and the Anglo-French Concorde supersonic airplane.

In science, our computers have cut the researchers experiment time with direct, on-line data reduction. DIGITAL computers control and monitor powerful nuclear reactors, control X-ray diffractometers, analyze nuclear spectroscopy data, and assisted in the analysis of lunar rock samples. They are used extensively in environmental research and pollution control.

In virtually all DIGITAL computer installations, DIGITAL solid state logic is used for interfacing or control application.

GENERAL INFORMATION

FINANCIAL RESULTS

Total Sales (in millions)		Net Income (in millions)	
1974	$421.8	1974	$44.4
1973	265.5	1973	23.5
1972	187.6	1972	15.3
1971	146.8	1971	10.6
1970	135.4	1970	14.4
1969	91.2	1969	9.4
1968	57.3	1968	6.8
1967	38.8	1967	4.5
1966	22.7	1966	1.9

DIGITAL EQUIPMENT CORPORATION
CORPORATE HEADQUARTERS

Maynard, Massachusetts 01754

MANUFACTURING PLANTS

Mountain View, California
Maynard, Massachusetts
Marlboro, Massachusetts
Natick, Massachusetts
Springfield, Massachusetts
Westfield, Massachusetts
Westminster, Massachusetts
San German, Puerto Rico
Kanata, Ontario, Canada
Galway, Ireland
Taichi, Taiwan
Hong Kong, BCC

SPECIAL SYSTEMS

Anaheim, California
Maynard, Massachusetts
Wallensteinplatz 2, West Germany
Tokyo, Japan
Reading, Berkshire, England
Paris, France
Kanata, Canada
Stockholm, Sweden

TOTAL EMPLOYES 18,000

GENERAL DESCRIPTION OF DIGITAL PRODUCTS
(Excluding those discussed in this Handbook)

COMPUTERS

PDP-8E, PDP-8F, PDP-8M, PDP-8/A, the lower cost successors to the PDP-8/I and PDP-8/L. They are the outgrowth of the largest concentration of minicomputer engineering, programming and user expertise in the world. Among the PDP-8/E features are: a unique internal bus system called OMNIBUS™, which allows the user to plug memory and processor options into any available slot location; the availability of 256 words of read only or read/write memory; a 1.2 microsecond memory cycle time; the use of TTL integrated circuitry with medium scale integration; expansion to 32,768 12-bit words; low cost mass storage expansion with DECdisk, DECtape, or the new DECcassette.

PDP-11 A family of expandable general purpose computers with 4,096 basic words of standard cose memory, each word 16 bits in length. Memory cycle time is 1.2 microseconds. Machine uses integrated circuitry and has some medium-scale integration in central processor. Models are PDP-11/05, -10, -15, -20, -35, -40, -45, and -70.

PDP-12 Laboratory computer system capable of executing PDP-8 and LINC-8 programs. It has basic 4,096-word core memory. Each word is 12 bits in length. Basic laboratory system includes interactive graphics capability, magnetic tape storage, A/D converter, and prewired, real-time clock.

PDP-15 A medium-scale series with an 18-bit word length, available in 5 complete software operating systems and 8 applications packages.

DECSYSTEM-10 General purpose large computer with basic memory of 8,192 (36-bit) words, expandable to 262,144. Will handle up to 63 time-sharing users simultaneously with batch and real-time jobs at the same time.

COMPUTER-BASED SYSTEMS

Industrial Products. Digital's industrial computer systems are based on PDP-8 and PDP-11 processors and encompass a range of power and capability. Products designed specifically for the industrial user include programmable controllers, environmental computer enclosures industrial control subsystems and power demand control equipment.

Business Systems. Digital's business-oriented computer systems, called DEC DATASYSTEMS, are based on the PDP-8 and PDP-11 minicomputer families and configured with appropriate terminals and storage devices. They function as complete stand-alone data-handling systems or as intelligent terminals in a large network.

Education Products. These systems include a variety of applications software and vary from small stand-alone single-user systems to large, multi-user timesharing configurations capable of handling computer-aided instruction as well as administrative data processing.

Data Communications. The data communications capability of the computer is enhanced by the special products—data handlers, front-end preprocessors, data loggers, modems—as well as the software and services of Digital's DECcomm group.

Laboratory Data Products include the DECgraphic-11 series of interactive, stand-alone computer-based graphics systems, DEClab-11 laboratory data handling systems, the Gamma-11, designed for use in nuclear medicine, MUMPS-11 data base management system for the hospital environment, PHA-11 pulse height analysis systems designed specifically for nuclear and x-ray spectroscopy in low-energy physics and radiochemistry applications, and the PDL programmable data logger, an easy-to-use laboratory data acquisition system.

Computerized Typesetting. Computer-based systems for setting type, including justification and hyphenation, text storage and editing, classified ad handling and related business applications, are available in a range of size and capability—Typeset-8, Typeset-11, Typeset-10—depending on the Digital computer system.

Original Equipment Manufacturing. Digital serves the OEM with a complete range of products and services designed to enhance the capability and profitability of both the manufacturer and the end user.

Components. The same quality components found in Digital products are available to the high-volume user, in quantity, without the normal Digital supporting services.

Peripherals. Digital offers a wide range of peripheral equipment and accessory devices for the computer user. Among them: analog/digital converters, display and plotting equipment, drums and disks, magnetic tape equipment, card, equipment, lineprinters.

Graphic Systems. Digital's GT40 series interactive graphic terminal systems function as compete stand-alone graphics systems or as part of a larger system configuration.

Special Systems. Digital maintains a special systems group with the capability to custom-build hardware and software systems to fulfill specific applications.

Software. A comprehensive selection of software complements Digital hardware. Assemblers, debugging routines, editors, monitors, floating point packages, mathematical routines, and diagnostic programs are available, as are conversational, interpretive languages developed for use in specific application areas.

Supplies and Accessories. Digital also provides power supplies, cabinetry, mounting hardware, tape, tape reels, storage racks, teleprinter ribbon and paper.

DIGITAL EQUIPMENT CORPORATION ENGINEERING SERVICES

In addition to supplying a complete line of standard and special hardware and accessories, Digital Equipment Corporation also provides an engineering, design and manufacturing service in support of customer applications. These services are available upon request and consist of the following.

Special Logic Modules: Many of the same advanced manufacturing and testing techniques which DIGITAL employs to produce its standard modules are applied to building special modules. DIGITAL engineers can provide full module design and development services or they can work with user-supplied drawings and parts lists, depending upon user needs.

Wire Wrapping: Using the latest in automatic wire wrapping equipment, DIGITAL can efficiently wire and check connector panels according to customer-supplied wire list and specifications.

Special Cables: When standard cables and cable lengths are not applicable to customer requirements, DIGITAL offers a complete cable fabrication service to build special cables according to customer specifications.

Interface Design: DIGITAL maintains a staff of experienced applications engineers who are capable of designing or providing design information for interfacing DIGITAL computers to custom control systems and equipment.

Logic Arrays: Special-purpose logic systems can be efficiently designed and built from customer-supplied data. DIGITAL's capability extends from limited production system to high-volume production and insures both optimum design and high reliability at a reasonable cost to the customer.

TERMS AND CONDITIONS

PRICES

All prices listed herein apply only within the continental U.S.A. and Canada are based on delivery FOB DIGITAL's plant, and are subject to DIGITAL's Standard Terms & Conditions, including the return-to-factory warranty set forth below (or as may be set forth in modified form in an effective discount agreement).

VOLUME DISCOUNT SCHEDULE—is based upon total dollar value of the order at list prices (for all items except cabinets).

Aggregrate List Price	Applicable Discount
$ 5,000 - 9,999	3%
10,000 - 19,999	5%
20,000 - 49,999	10%
50,000 - 99,999	15%
100,000 - 249,999	18%
250,000 - 499,999	20%
500,000 - 999,999	22%
1,000,000 - AND OVER	25%

CABINET DISCOUNT SCHEDULE
The following discount schedule is for cabinet purchases only. The discount is computed from the total list price of cabinet parts purchased. On blanket purchase orders, minimum releases of ten units (cabinets) or balance is required.

Sale in Dollars	Discount
$ 500 - $ 999	8%
1,000 - 1,499	12%
1,500 - 2,499	20%
2,500 - 4,999	25%
5,000 - 7,499	26%
7,500 - 9,999	28%
$10,000 - And up	30%

WARRANTY

Warranty for Logic Products equipment listed in the then current Logic Handbook, Logic Products Price List, and Hardware/Accessories Catalog.

A) B, R, W, M, K, and A Series Modules are warranted as stated below for a period of one (1) year from date of shipment. H and Non-catalog FLIP CHIP modules, DECkits, Data Entry Terminals, Remote Data Acquisition Systems, Power Supplies, Cables, Cabinets, Labs, Hardware, and Accessories are warranted as stated below for a period of ninety (90) days from date of shipment.

B) All Logic Products equipment is warranted against defects in material and workmanship under normal and proper use and in their original unmodified condition. DIGITAL's sole obligation for equipment, defective under the terms of this warranty, is limited to repair or replacement (at its option), at its factory, at no charge to customer. All replaced equipment becomes the property of DIGITAL. As a condition of this warranty, customer must obtain a DIGITAL Return Authorization Number from the local DIGITAL Sales Office and must return all equipment, prepaid, to:

Digital Equipment Corporation
Logic Products Services
Repair Section
One Iron Way
Marlborough, Massachusetts 01752

Transportation charges for the return to the customer shall be paid by DIGITAL within the continental U.S.A. and Canada and will be made on a UPS or Parcel Post insured basis. The warranty outside of the continental U.S.A. and Canada is limited to repair or replacement only and excludes all costs of shipping, Customs clearance, and other related charges.

C) Premium methods of shipment are available at customer expense and will be used only when specifically requested. DIGITAL maintains a factory repair service for customer convenience and will repair equipment beyond the warranty at then current prices as long as repair components are available.

D) All the above warranties include the DISCLAIMER OF WARRANTIES clause as contained in DIGITAL's Standard Terms & Conditions.

HOW-TO-ORDER

All products described in this handbook can be ordered by telephone, TELEX, TWX, or mailed to your local DIGITAL sales office. When placing an order, please provide specific information regarding part number, full description, quantity, ship-to and bill-to addresses. Prices quoted are U.S.A. list and do not include applicable taxes or shipping charges.

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(Subject to change without notice)

TYPE	TITLE	Price in U.S. dollars
12-09154	Drawer Mounting Slides (pair)	25.00
12-09224	Latch	1.00
12-09340-00	8-Pin Cable Connector (Female) Housing (2/pkg)	1.00
12-09340-01	8-Pin Cable Connector (Male) Housing (2/pkg)	1.00
12-09350-(all dash items)	Cable Connector (Female) Housing pkg.	1.00
12-09351-(all dash items)	Cable Connector (Male) Housing pkg.	1.00
12-09703	Drawer Mounting Slides, Tilt (pair)	52.00
12-09764	Cable Clamp (5/pkg)	1.00
12-09925	Cable Clamp (4/pkg)	1.00
12-10152-1	Connector Block	5.00
12-10945	Chassis Slides (pair)	19.00
12-11046	Receptacle for use with 861-A Power Controller	8.00
12-11191	Receptacle for use with 861-B Power Controller	12.00
12-11194	Receptacle for use with 861-C Power Controller	24.00
12-11386	Thick Latch	1.00
29-15201	Touchup Paint, Black can	3.00
29-15202	Touchup Paint, Grey (Bezel/68) can	3.00
29-15205	Touchup Paint, Grey (End Panel/101) can	3.00
74-06706	Fan, Cover Plate	4.00
74-06782	Kickplate (use with H952-BA)	6.00
74-06793	Kickplate	10.00
74-07789	Spacer	1.00
74-09449	Bracket for Chassis Slides (right)	2.00
74-09459	Bracket for Chassis Slides (left)	5.00
74-09819	Key-Lock Strike Plate	1.00
861-A	Power Controller (90-130 Vac, Two-Phase)	300.00
861-B	Power Controller (180-270 Vac, Single-Phase)	300.00
861-C	Power Controller (90-135 Vac, Single-Phase)	350.00
90-06990	Cabinet Door Ground Strap	5.00
90-07786	Tinnerman Clip Nut and Phillips Pan Head Screw Collection bag	5.00
90-08887	Cabinet Frame Ground Strap	5.00
91-05740	Wire Wrapping Wire, 30 AWG (1000 ft/spool)	60.00
91-07470-44	Hookup (Solder) Wire, 24 AWG ft.	0.30
91-07688	Wire Wrapping Wire, 24 AWG (1000 ft/spool)	50.00
913-(all dash items)	Patch Cords, 24 AWG (100/pkg)	25.00
914-7	7-Inch Power Patch Cord (10/pkg)	4.00
914-19	19-Inch Power Patch Cord (10/pkg)	4.00
915-(all dash items)	Patch Cords, 26 AWG (100/pkg)	33.00
917-2.5	Daisy Chain, Clip every 2.5"	50.00
917-5	Daisy Chain, Clip every 5.0"	50.00

TYPE		Price in U.S. dollars
932	Bus Strip (5/pkg)	3.00
933	Bus Strip	1.00
937	Blank Module Handle (25/pkg)	7.00
939	Bus Strip (6/pkg)	9.00
940	Cable Clamp (25/pkg)	7.00
941	Cable Clamp (25/pkg)	7.00
943	Cable Clamp (25/pkg)	7.00
944	Cable Clamp (25/pkg)	7.00
953	Wire Wrap IC Sockets (10/pkg)	12.00
954	Solder IC Sockets (10/pkg)	7.00
956	DEC8640 UNIBUS Receiver IC (Quad 2-Input NOR Gate)	26.00
957	DEC8881-1 UNIBUS Driver IC (Quad 2-Input NAND Gate)	19.00
A123	4-Input Multiplexer	58.00
A126	8-Channel High Impedance Multiplexer	75.00
A207	Operational Amplifier	45.00
A260	Dual Amplifier	250.00
A460	Sample and Hold	250.00
A619	10-Bit D/A Converter, Single Buffered	210.00
A704	Reference Supply	184.00
A811	10-Bit A/D Converter	350.00
A866	High-Speed 12-Bit Bipolar A/D Converter	350.00
AR11	Analog Real-Time Module	1,500.00
B104	Inverter	18.00
B105	Inverter	22.00
B113	NAND/NOR Gate	24.00
B115	NAND/NOR Gate	22.00
B117	NAND/NOR Gate	17.00
B123	Inverter	37.00
B124	Inverter	33.00
B130	3-Bit Parity Circuit	54.00
B155	Half Binary-to-Octal Decoder	27.00
B171	NAND/NOR Gate	19.00
B201	Flip-Flop	60.00
B204	Quadruple Flip-Flop	37.00
B301	Delay	78.00
B360	Delay with Pulse Amplifier	90.00
B401	Variable Clock	61.00
B405	Clock	108.00
B602	Pulse Amplifier	47.00
B681	Power Inverter	30.00
B684	Bus Driver	56.00
BA11-ES	Expander Mounting Box	550.00
BB11	4-Slot System Interfacing Unit	170.00
BB11-A	4-Slot System Interfacing Unit	160.00
BB11-B	9-Slot System Interfacing Unit	239.00

For total cost of the following cable assemblies where the length is to be specified by the customer (-xx suffix), refer also to Note 1 at the end of this price list.

TYPE	TITLE	Price in U.S. dollars
BC02A-xx	20-Conductor Ribbon Cable	34.00
BC02B-xx	20-Conductor Ribbon Cable	32.00
BC02E-xx	20-Conductor Ribbon Cable	33.00
BC02K-xx	20-Conductor Ribbon Cable	34.00
BC02L-xx	20-Conductor Ribbon Cable	32.00
BC02M-xx	20-Conductor Ribbon Cable	32.00
BC02N-xx	20-Conductor Ribbon Cable	32.00
BC02P-xx	20-Conductor Ribbon Cable	32.00
BC02T-xx	20-Conductor Ribbon Cable	33.00
BC02U-xx	20-Conductor Ribbon Cable	30.00
BC02W-xx	20-Conductor Ribbon Cable	32.00
BC02X-xx	Two 20-Conductor Ribbon Cables	54.00
BC02Y-xx	20-Conductor Ribbon Cable	33.00
BC03A-xx	9-Conductor Flat Coax Cable	41.00
BC03B-xx	9-Conductor Flat Coax Cable	40.00
BC03C-xx	9-Conductor Flat Coax Cable	38.00
BC03D-xx	9-Conductor Flat Coax Cable	38.00
BC03E-xx	19-Conductor Flat Mylar Cable	31.00
BC03F-xx	19-Conductor Flat Mylar Cable	30.00
BC03H-xx	Two 19-Conductor Flat Mylar Cables	58.00
BC03J-xx	9-Conductor Flat Coax Cable	38.00
BC04A-xx	20-Conductor Ribbon Cable	16.00
BC04B-xx	20-Conductor Ribbon Cable	19.00
BC04C-xx	20-Conductor Ribbon Cable	18.00
BC04D-xx	20-Conductor Ribbon Cable	16.00
BC04E-xx	20-Conductor Ribbon Cable	16.00
BC04F-xx	20-Conductor Ribbon Cable	16.00
BC04H-xx	20-Conductor Ribbon Cable	16.00
BC04J-xx	20-Conductor Ribbon Cable	17.00
BC04K-xx	20-Conductor Ribbon Cable	16.00
BC04L-xx	9-Conductor Flat Coax Cable	19.00
BC04M-xx	9-Conductor Flat Coax Cable	19.00
BC04N-xx	9-Conductor Flat Coax Cable	19.00
BC04P-xx	Two 9-Conductor Flat Coax Cables	36.00
BC04T-xx	Two 19-Conductor Flat Mylar Cables	29.00
BC04U-xx	Two 19-Conductor Flat Mylar Cables	23.00
BC04W-xx	Two 20-Conductor Ribbon Cables	30.00
BC04Z-xx	40-Conductor Flat Mylar Cable	15.00
BC05C-25	25-Conductor Round Cable	102.00
BC05C-35	25-Conductor Round Cable	110.00
BC05C-45	25-Conductor Round Cable	120.00
BC05C-50	25-Conductor Round Cable	130.00
BC05C-60	25-Conductor Round Cable	150.00
BC05C-70	25-Conductor Round Cable	170.00
BC05D-10	25-Conductor Round Cable	85.00
BC05D-25	25-Conductor Round Cable	120.00
BC05F-xx	4-Conductor Round Cable	9.00
BC05H-6	Line Set	48.00
BC05J-6	Line Set	60.00
BC05X-xx	4-Conductor Round Cable	12.00
BC07A-10	20-TWP Round Cable	60.00
BC07A-15	20-TWP Round Cable	69.00

TYPE	TITLE	Price in U.S. dollars
BC07A-25	20-TWP Round Cable	80.00
BC07B-10	11-TWP Round Cable	30.00
BC07B-15	11-TWP Round Cable	32.00
BC07B-25	11-TWP Round Cable	34.00
BC07C-10	10-TWP Round Cable	30.00
BC07C-15	10-TWP Round Cable	32.00
BC07C-25	10-TWP Round Cable	34.00
BC07D-10	Two 20-Conductor Ribbon Cables	40.00
BC07D-15	Two 20-Conductor Ribbon Cables	42.00
BC07D-25	Two 20-Conductor Ribbon Cables	46.00
BC08A-01	Two 19-Conductor Flat Mylar Cables	48.00
BC08A-03	Two 19-Conductor Flat Mylar Cables	51.00
BC08A-05	Two 19-Conductor Flat Mylar Cables	55.00
BC08A-07	Two 19-Conductor Flat Mylar Cables	58.00
BC08A-10	Two 19-Conductor Flat Mylar Cables	63.00
BC08A-15	Two 19-Conductor Flat Mylar Cables	72.00
BC08A-25	Two 19-Conductor Flat Mylar Cables	85.00
BC08B-01	Two 9-Conductor Flat Coax Cables	75.00
BC08B-03	Two 9-Conductor Flat Coax Cables	79.00
BC08B-05	Two 9-Conductor Flat Coax Cables	84.00
BC08B-07	Two 9-Conductor Flat Coax Cables	88.00
BC08B-10	Two 9-Conductor Flat Coax Cables	95.00
BC08B-15	Two 9-Conductor Flat Coax Cables	105.00
BC08B-25	Two 9-Conductor Flat Coax Cables	125.00
BC08C-01	Two 19-Conductor Flat Mylar Cables	49.00
BC08C-03	Two 19-Conductor Flat Mylar Cables	52.00
BC08C-05	Two 19-Conductor Flat Mylar Cables	57.00
BC08C-07	Two 19-Conductor Flat Mylar Cables	60.00
BC08C-10	Two 19-Conductor Flat Mylar Cables	65.00
BC08C-15	Two 19-Conductor Flat Mylar Cables	72.00
BC08C-25	Two 19-Conductor Flat Mylar Cables	88.00
BC08D-01	Two 9-Conductor Flat Coax Cables	79.00
BC08D-03	Two 9-Conductor Flat Coax Cables	84.00
BC08D-05	Two 9-Conductor Flat Coax Cables	88.00
BC08D-07	Two 9-Conductor Flat Coax Cables	92.00
BC08D-10	Two 9-Conductor Flat Coax Cables	99.00
BC08D-15	Two 9-Conductor Flat Coax Cables	110.00
BC08D-25	Two 9-Conductor Flat Coax Cables	131.00
BC08E-xx	19-Conductor Flat Mylar Cable	24.00
BC08F-06	Two 19-Conductor Flat Mylar Cables	54.00
BC08H-03F	Two 60-Conductor Flat Mylar Cables	90.00
BC08H-04F	Two 60-Conductor Flat Mylar Cables	95.00
BC08J-06	40-Conductor Flat Mylar Cable	75.00
BC08J-10	40-Conductor Flat Mylar Cable	85.00
BC08J-15	40-Conductor Flat Mylar Cable	97.00
BC08J-25	40-Conductor Flat Mylar Cable	115.00
BC08J-50	40-Conductor Flat Mylar Cable	170.00
BC08K-06	40-Conductor Flat Mylar Cable	70.00
BC08K-10	40-Conductor Flat Mylar Cable	80.00
BC08K-15	40-Conductor Flat Mylar Cable	90.00
BC08K-25	40-Conductor Flat Mylar Cable	110.00
BC08K-50	40-Conductor Flat Mylar Cable	165.00
BC08L-06	Two 40-Conductor Flat Mylar Cables	115.00

TYPE	TITLE	Price in U.S. dollars
BC08L-10	Two 40-Conductor Flat Mylar Cables	140.00
BC08L-15	Two 40-Conductor Flat Mylar Cables	160.00
BC08L-25	Two 40-Conductor Flat Mylar Cables	205.00
BC08L-50	Two 40-Conductor Flat Mylar Cables	310.00
BC08R-xx	40-Conductor Flat Mylar Cable	45.00
BC11A-02	Two 60-Conductor Flat Mylar Cables	115.00
BC11A-05	Two 60-Conductor Flat Mylar Cables	130.00
BC11A-08F	Two 60-Conductor Flat Mylar Cables	145.00
BC11A-10	Two 60-Conductor Flat Mylar Cables	160.00
BC11A-15	Two 60-Conductor Flat Mylar Cables	175.00
BC11A-20	Two 60-Conductor Flat Mylar Cables	190.00
BC11A-25	Two 60-Conductor Flat Mylar Cables	200.00
BC11A-35	Two 60-Conductor Flat Mylar Cables	220.00
BC11A-50	Two 60-Conductor Flat Mylar Cables	250.00
BC11K-25	20-TWP Round Cable	135.00
BC14F-05	25-Conductor Round Cable	50.00
BC14F-10	25-Conductor Round Cable	50.00
BC14F-15	25-Conductor Round Cable	50.00
BC14F-25	25-Conductor Round Cable	50.00
BC70A-15	10-Conductor Round Cable	70.00
BC70B-15	Two 11-TWP Round Cable	70.00
CAB-I	Cabinet Assembly (Short Size)	535.00
CAB-J	Cabinet Assembly (Short Size)	462.00
CAB-K	Cabinet Assembly (Short Size)	386.00
DD11-A	4-Slot System Interfacing Unit	275.00
DD11-B	4-Slot System Interfacing Unit	275.00
DECkit01-A	Remote Analog Data Concentrator ..... Note 2	
DECkit11-D	PDP-11 Direct Memory Access Interface	850.00
DECkit11-F	PDP-11 I/O Interface (3 Words In/1 Word Out)	750.00
DECkit11-H	PDP-11 I/O Interface (4 Words In/4 Words Out)	1,165.00
DECkit11-K	PDP-11 I/O Interface (8 Words In)	695.00
DECkit11-M	PDP-11 I/O Interface (34 Bits In/24 Bits Out)	720.00
H019	Expander Frame	35.00
H020	Connector Block Mounting Frame	15.00
H033	4-Slot System Unit Mounting Frame	8.00
H034	9-Slot System Unit Mounting Frame	15.00
H035	Vertical System Unit Mounting Frame	20.00
H322	Distribution Panel	150.00
H500	Computer Lab (115 Vac)	375.00
H500A	Computer Lab (230 Vac)	375.00
H704-A	Power Supply (±15 Vdc)	325.00
H707	Power Supply (±15 Vdc)	430.00
H710	Power Supply (+5 Vdc)	190.00
H716	Power Supply (+5 Vdc, −15 Vdc)	160.00
H720-C	Power Supply (+5 Vdc, −15 Vdc, +8 Vdc, −25 Vdc)	750.00
H720-D	Power Supply (+5 Vdc, −15 Vdc, +8 Vdc, −25 Vdc)	750.00
H720-E	Power Supply (+5 Vdc, −15 Vdc, +8 Vdc, −22 Vdc	750.00
H720-F	Power Supply (+5 Vdc, −15 Vdc, +8 Vdc, −22 Vdc)	750.00

TYPE	TITLE	Price in U.S. dollars
H721	Power Supply (+5 Vdc, −15 Vdc, +10 Vdc)	800.00
H722	Step-Down Transformer	100.00
H726-B	Power Supply (+5 Vdc)	215.00
H740-D	Power Supply (+5 Vdc, −15 Vdc, +15 Vdc)	540.00
H800	Connector Block (144-Pin)	9.00
H802	Connector Block (18-Pin)	4.00
H803	Connector Block (288-Pin)	14.00
H8030	Connector Block (72-Pin)	6.00
H807	Connector Block (36-Pin)	5.00
H808	Connector Block (144-Pin)	12.00
H810(24)	Pistol-Grip Wire Wrapping Tool Kit for 24 AWG Wire	99.00
H810-A	Pistol-Grip Wire Wrapping Tool Kit for 30 AWG Wire	130.00
H810-B	Pistol-Grip Wire Wrapping Tool Kit for 24 or 30 AWG Wire	160.00
H810-C	Battery-Powered Wire Wrap Gun with Bit and Sleeve for 24 AWG Wire	150.00
H810-D	Battery-Powered Wire Wrap Gun with Bit and Sleeve for 30 AWG Wire	150.00
H810-E	Battery-Powered Wire Wrap Gun	130.00
H811(24)	Hand Wire Wrapping Tool for 24 AWG Wire	35.00
H811-A	Hand Wire Wrapping Tool for 30 AWG Wire	35.00
H812(24)	Hand Wire Unwrapping Tool for 24 AWG Wire	10.00
H812-A	Hand Wire Unwrapping Tool for 30 AWG Wire	12.00
H813(24)	Wire Wrap Gun Bit for 24 AWG Wire	30.00
H813-A	Wire Wrap Gun Bit for 30 AWG Wire	30.00
H814(24)	Wire Wrap Gun Sleeve for 24 AWG Wire	21.00
H814-A	Wire Wrap Gun Sleeve for 30 AWG Wire	21.00
H820	Grip Clip Connectors for 24 AWG (1000/pkg)	48.00
H821	Grip Clip Connectors for 30 AWG (1000/pkg)	98.00
H825	Hand Crimping Tool	146.00
H826	Hand Crimping Tool	210.00
H850	Module Handle Extender	10.00
H851	Edge Connector	15.00
H852	Module Holder (25/pkg)	7.00
H853	Module Holder (25/pkg)	7.00
H854	I/O Connector (40-Pin Male) Board Mount	12.00
H856	I/O Connector (40-Pin Female) Cable Mount	8.00
H863	Connector Block (288-Pin)	14.00
H904-A	Horizontal System Unit Mounting Enclosure	Note 2
H905-A	Horizontal System Unit Mounting Enclosure	Note 2
H906	Vertical System Unit Mounting Enclosure	Note 2
H907-A	Horizontal System Unit Mounting Enclosure	Note 2
H909-A	General Purpose Logic Box	150.00
H909-BA	General Purpose Logic Box with power supply	625.00
H911-J	Mounting Panel	180.00
H911-K	Mounting Panel	170.00
H911-R	Mounting Panel	180.00

TYPE	TITLE	Price in U.S. dollars
H911-S	Mounting Panel	175.00
H913	Mounting Panel	270.00
H914	Mounting Panel	125.00
H916	Mounting Panel	270.00
H917	Mounting Panel	260.00
H9190	Expander Panel	250.00
H920	Module Drawer Frame	170.00
H921	Front Panel for H920 Module Drawer Frame	15.00
H923	Chassis Slides for H920 Module Drawer Frame (pair)	75.00
H925	Module Drawer	250.00
H930	System Unit Drawer	300.00
H933-A	4-Slot System Unit	39.00
H933-B	4-Slot System Unit	39.00
H933-C	4-Slot System Unit	75.00
H933-CA	4-Slot System Unit	75.00
H933-CB	4-Slot System Unit	75.00
H933-D	4-Slot System Unit	42.00
H934-CB	9-Slot System Unit	145.00
H941-AA	Mounting Panel Frame	125.00
H941-BA	8-Inch Deep Cover for H941-AA	70.00
H941-BB	11.4-Inch Deep Cover for H941-AA	80.00
H950-AA	Cabinet Frame (Standard Size)	163.00
H950-BA	Full Door (RH) (Front or Rear Mounting)	47.00
H950-CA	Full Door (LH) (Front or Rear Mounting)	47.00
H950-DA	Mounting Panel Door Frame (RH) (Rear Mounting)	47.00
H950-EA	Mounting Panel Door Frame (LH) (Rear Mounting)	47.00
H950-FA	Mounting Panel Door Skin	25.00
H950-G	Cabinet Table	85.00
H950-HA	Short Door (Covers 21 in. Mounting Space)	48.00
H950-HB	Short Door (Covers 22¾ in. Mounting Space)	48.00
H950-HC	Short Door (Covers 26¼ in. Mounting Space)	48.00
H950-HD	Short Door (Covers 31½ in. Mounting Space)	60.00
H950-HE	Short Door (Covers 36¾ in. Mounting Space)	60.00
H950-HF	Short Door (Covers 42 in. Mounting Space)	65.00
H950-HG	Short Door (Covers 47¼ in. Mounting Space)	65.00
H950-HH	Short Door (Covers 52½ in. Mounting Space)	60.00
H950-HJ	Short Door (Covers 57¾ in. Mounting Space)	60.00
H950-HK	Short Door (Covers 63 in. Mounting Space)	65.00
H950-JA	Short Door (Covers 21 in. Mounting Space) (used with H952-BA installed)	60.00
H950-JE	Short Door (Covers 63 in. Mounting Space) (used with H952-BA installed)	60.00
H950-LA	Logo Frame Panel (Aluminum)	12.00
H950-LB	Logo Frame Panel (Plastic)	10.00
H950-PA	Bezel Cover Panel (5¼ in.)	11.00
H950-QA	Bezel Cover Panel (10½ in.)	14.00
H950-SA	Air Filter (for H952-BA or H952-CA)	4.00
H952-AA	End Panel (require 2 per cabinet)	65.00
H952-BA	Stabilizer Feet (Pair)	32.00

TYPE	TITLE	Price in U.S. dollars
H952-CA	Fan Assembly (Top Mounted) (115 Vac)	48.00
H952-CB	Fan Assembly (Top Mounted) (230 Vac)	48.00
H952-EA	Caster Set (4 per set; included with H950-AA Frame)	10.00
H952-FA	Leveler Set (4 per set included with H950-AA Frame)	2.00
H952-GA	Filler Strip Set (Front and Rear) (Joining Two Cabinets)	55.00
H952-HA	Free-Standing Table	275.00
H957-AA	Cabinet Frame (Short Size)	160.00
H957-BA	Full Door (RH) (Rear Mounting)	60.00
H957-CA	Full Door (LH) (Rear Mounting)	60.00
H957-DA	Mounting Panel Door Frame (RH)	45.00
H957-EA	Mounting Panel Door Frame (LH)	45.00
H957-FA	End Panel (R end)	63.00
H957-FB	End Panel (L end)	63.00
H957-GA	Filler Strip Set (Top, Front, and Rear) (Joining Two Cabinets)	50.00
H957-HA	Fan Assembly (Front or Rear Mounting)	70.00
H957-JA	Bottom Cover Plate	15.00
H957-LA	Logo Frame Panel	20.00
H957-SA	Filter (for H957-HA)	4.00
H960-BC	Cabinet Assembly (Standard Size)	850.00
H960-BD	Cabinet Assembly (Standard Size)	850.00
H960-CA	Cabinet Assembly (Standard Size)	850.00
H960-CB	Cabinet Assembly (Standard Size)	850.00
H961-A	Cabinet Assembly (Standard Size)	600.00
H961-AA	Cabinet Assembly (Standard Size)	600.00
H961-AB	Cabinet Assembly (Standard Size)	600.00
H967-BA	Cabinet Assembly (Short Size)	850.00
H967-BB	Cabinet Assembly (Short Size)	850.00
H970-BA	Free-Standing Table	150.00
H970-CA	Free-Standing Table	150.00
K003	Gate Expander	10.00
K012	Gate Expander	10.00
K026	Gate Expander	8.00
K028	Gate Expander	12.00
K113	Inverting Gate	13.00
K123	Non-Inverting Gate	15.00
K124	AND/OR Gate	16.00
K134	Inverters	16.00
K135	Inverters	17.00
K138	Inverters	24.00
K161	Binary-to-Octal Decoder	28.00
K174	Digital Comparator	24.00
K201	Flip-Flop	39.00
K202	Flip-Flop	30.00
K206	Flip-Flop Register	26.00
K207	Flip-Flop	30.00
K210	Counter	33.00
K211	Programmable Divider	26.00
K220	Up/Down Counter	64.00
K230	Shift Register	49.00

TYPE	TITLE	Price in U.S. dollars
K265	Reed Relay Driver	25.00
K281	Fixed Memory	30.00
K282	Diode Memory	73.00
K302	Dual Timers	49.00
K303	Timer	29.00
K323	One-Shots	35.00
K501	Schmitt Triggers	29.00
K564	DC Input Converters	80.00
K579	Isolated AC Input Converters	113.00
K580	Dry Contact Filters	28.00
K581	Dry Contact Filters	21.00
K616	Isolated AC Switches	126.00
K657	DC Driver	90.00
K658	DC Driver	128.00
K675	5-Digit Display	145.00
K681	Lamp Driver	17.00
K683	Lamp Driver	30.00
K716	Interface Block	267.00
K724	Interface Shell	65.00
K943-R	Mounting Panel	105.00
K943-S	Mounting Panel	105.00
K990	Timer Component Board	7.00
KC341-B	Monitor/Control Panel	555.00
KITS	See DECkits	
KMP01-A	Prewired System Backplane	160.00
LA36	DECwriter II Data Terminal	1,850.00
M002	Logic HIGH Source	13.00
M040	Solenoid Driver	39.00
M050	50 mA Indicator Driver	33.00
M051	Positive to Negative Logic Level Converter	31.00
M060	Solenoid Driver	55.00
M100	Bus Data Interace	50.00
M101	Bus Data Interface	24.00
M102	Device Selector	60.00
M103	Device Selector	45.00
M105	Address Selector	80.00
M107	Device Selector	70.00
M108	Flag Module	45.00
M1103	2-Input AND Gates	20.00
M1103	Ten 2-Input OR Gates	20.00
M111	Inverter	22.00
M112	NOR Gates	18.00
M1125	Exclusive-OR Gates	20.00
M113	NAND Gates	18.00
M1131	2-Input Open Collector NAND Gate	21.00
M115	NAND Gates	18.00
M116	Six 4-Input NOR Gates	20.00
M117	NAND Gates	19.00
M119	NAND Gates	18.00
M121	AND/OR Gates	23.00
M1307	4-Input AND Gates	20.00
M1307	Six 4-Input OR Gates	12.00
M133	2-Input NAND Gate	22.00

TYPE	TITLE	Price in U.S. dollars
M135	Eight 3-Input NAND Gates	22.00
M137	Six 4-Input NAND Gates	22.00
M139	Three 8-Input NAND Gates	24.00
M141	NAND/OR Gates	29.00
M1500	Bidirectional Bus Interacing Gates	35.00
M1501	Bus Input Interface	50.00
M1502	Bus Output Interface	100.00
M152	Dual 1-of-8 Decoder	36.00
M155	4-Line to 16-Line Decoder	30.00
M159	Arithmetic/Logic Unit	35.00
M160	AND/NOR Gate	33.00
M161	Binary-to-Octal/Decimal Decoder	35.00
M162	Parity Circuit	35.00
M1621	DVM Data Input Interface	125.00
M1623	Instrument Remote Control Interface	150.00
M163	Dual Binary-to-Decimal Decoder	27.00
M165	8 Buffers	30.00
M168	12-Bit Magnitude Comparator	45.00
M169	Gating Module	33.00
M1701	Data Selector	24.00
M1703	OMNIBUS Input Interface	82.00
M1705	OMNIBUS Output Interface	183.00
M1709	OMNIBUS Interface Foundation Module	150.00
M1710	UNIBUS Interface Foundation Module	250.00
M1713	16-Line to 1-Line Data Selector	17.00
M1801	16-Bit Relay Output Interface	350.00
M191	ALU Look-Ahead Logic	22.00
M2001	Dual 4-Bit Tri-State Registers	40.00
M202	Triple J-K Flip-Flop	20.00
M203	8 R/S Flip-Flops	26.00
M204	General-Purpose Buffer and Counter	24.00
M205	General-Purpose Flip-Flops	33.00
M206	General-Purpose Flip-Flops	30.00
M207	General-Purpose Flip-Flops	33.00
M208	8-Bit Buffer/Shift Register	30.00
M230	Binary-to-BCD and BCD-to-Binary Converter	70.00
M236	12-Bit Binary Up/Down Counter	50.00
M237	3-Digit BCD Up/Down Counter	50.00
M238	Dual 4-Bit Binary Synchronous Up/Down Counter	35.00
M239	Three 4-Bit Counter/Register	35.00
M245	Dual 4-Bit Shift Register	28.00
M246	5 D-Type Flip-Flops	21.00
M248	Dual 4-bit Multipurpose Shift Register	25.00
M2500	Dual 64-Word X 4-Bit First-In First-Out Serial Memory	160.00
M253	16-Word X 12-Bit RAM	73.00
M260	4-Word X 12-Bit Associative Memory	221.00
M261	4-State Motor Translator	40.00
M262	10-State Motor Translator	65.00
M302	Dual Delay Multivibrator	59.00
M3020	Dual Delay Multivibrators	40.00
M306	Integrating One-Shot	35.00
M310	Delay Line	58.00

TYPE	TITLE	Price in U.S. dollars
M401	Variable Clock	55.00
M403	RC Multivibrator Clock	40.00
M404	Crystal Clock	79.00
M405	Crystal Clock	120.00
M410	Reed Clock	70.00
M452	Variable Clock	44.00
M500	Negative Input/Positive Output Receiver	55.00
M501	Schmitt Trigger	26.00
M502	High-Speed Negative Input Converter	26.00
M506	Medium-Speed Negative Input Converter	52.00
M507	Medium-Speed Negative Bus Converter	45.00
M510	I/O Bus Receiver	51.00
M521	K-to-M Converter	20.00
M594	EIA/CCITT Level Converter	75.00
M598	1-Channel Transmit/Receive Optic-Coupled Current Isolator	70.00
M602	Pulse Amplifier	28.00
M606	Pulse Generator	43.00
M610	Open Collector 2-Input NAND Gate	66.00
M611	High-Speed Power Inverter	32.00
M617	4-Input Power NAND Gate	26.00
M622	8-Bit Positive Input/Output Bus Driver	45.00
M623	Bus Driver	40.00
M624	Bus Driver	45.00
M627	NAND Power Amplifier	29.00
M632	Positive Input/Negative Output Bus Driver	55.00
M633	Negative Bus Driver	50.00
M650	Negative Output Converter	29.00
M652	Negative Output Converter	42.00
M660	Positive Level Cable Driver	25.00
M661	Positive Level Driver	20.00
M671	M-to-K Converter	43.00
M706	Teletype Receiver	150.00
M707	Teletype Transmitter	150.00
M730	Bus Interface	95.00
M7300	Arithmetic and Logic Function Selection Module	90.00
M7301	Arithmetic and Logic Function Module	135.00
M7304	Bus Sense Register	115.00
M7305	Transfer Register Module	96.00
M7306	Flag Module	44.00
M7307	Four-Word Constants Generator	102.00
M731	Bus Interface	101.00
M7310	Evoke Units Module	31.00
M7311	General Purpose Parallel I/O Module	100.00
M7312	Hex Two-Way Branches	39.00
M7313	Bidirectional Serial Interface	175.00
M7314	Dual Eight-Way Branches	35.00
M7315	Hex Subroutine Returns	50.00
M7316	General Purpose Parallel Output Module	82.00
M7317	General Purpose Parallel Input Module	61.00
M7318	16-Word Scratch Pad RAM	140.00
M7319	256-Word Scratch Pad RAM	283.00
M732	Bus Interface	95.00

TYPE	TITLE	Price in U.S. dollars
M7320	Byte Register	84.00
M7322	Bus Indicator Module	125.00
M7323	64-to-1 Multiplexer	69.00
M7324	1K RAM	600.00
M7325	24-Word Constants Generator	107.00
M7327	256-Byte Reprogrammable Read-Only Memory	115.00
M7328	Evoke Decoder	50.00
M7329	30-to-1 Multiplexer	50.00
M733	Bus Interface	120.00
M7332	Bus Monitor and Terminator	140.00
M7333	Dual Serial Interface Connector	25.00
M7334	Switch and Light Module	200.00
M7335	Service Module	200.00
M7336	512 Program Control Sequencer	150.00
M734	I/O Bus Input Multiplexer	56.00
M7341	Processor Module	410.00
M7344-YA	Read/Write Memory, 1K	335.00
M7344-YB	Read/Write Memory, 2K	530.00
M7344-YC	Read/Write Memory, 4K	960.00
M7345	Programmable Read-Only Memory	140.00
M7346	External Event Detection	80.00
M735	I/O Bus Transfer Register	60.00
M736	Priority Interrupt Module	65.00
M737	12-Bit Bus Receiver Interface	52.00
M738	Counter-Buffer Interface	60.00
M7389	Asynchronous Transceiver	175.00
M7390	Asynchronous Transceiver	195.00
M7821	Interrupt Control Module	110.00
M783	UNIBUS Drivers	40.00
M784	UNIBUS Receivers	40.00
M785	UNIBUS Transceiver	50.00
M786	Device Register Interface	250.00
M795	Word Count and Bus Address Module	216.00
M796	UNIBUS Master Control	108.00
M798	UNIBUS Drivers	40.00
M901	Flat Mylar Cable Connector	15.00
M903	Flat Mylar Cable Connector	10.00
M904	Flat Coaxial Cable Connector	10.00
M906	Cable Terminator	20.00
M907	Diode Clamp Connector	21.00
M908	Flat Ribbon Cable Connector	10.00
M909	Terminator	21.00
M910	Terminator	23.00
M9100	Adapter (H854-to-H854) Connector	30.00
M912	Round Coaxial (TWP) Cable Connector	25.00
M915	Flat Mylar Cable Connector	30.00
M917	Flat Coaxial Cable Connector	10.00
M918	Flat Mylar Cable Connector	10.00
M919	Flat Mylar Cable Connector	10.00
M920	UNIBUS Jumper Module	64.00
M922	Flat Mylar Cable Connector	6.00
M925	Flat Mylar Cable Connector	9.00
M926	Flat Mylar Cable Connector	27.00

TYPE	TITLE	Price in U.S. dollars
M927	Round Coaxial (TWP) Cable Connector	6.00
M929	Flat Mylar Cable Connector	30.00
M933	Flat Ribbon Cable Connector	20.00
M935	OMNIBUS Jumper Module	49.00
M936	Flat Mylar Cable Connector	15.00
M937	Flat Mylar Cable Connector	15.00
M943	Flat Mylar Cable Connector	6.00
M945	Flat Mylar Cable Connector	20.00
M946	Flat Mylar Cable Connector	20.00
M953	Flat Shielded Cable Connector	25.00
M954	Flat Shielded Cable Connector	27.00
M955	Flat Shielded Cable Connector	27.00
M957	Flat Ribbon Cable Connector	21.00
M959	Round Cable Connector	11.00
M960	TU56-TD8-E Command Cable Connector	45.00
M961	TU56-TD8-E Data Cable Connector	45.00
M962	Bus Terminator	32.00
M971	Cable Connector	30.00
M972	Flat Mylar Cable Connector	30.00
M975	Flip Chip to H854 Adapter	35.00
M976	UNIBUS Cable Connector	18.00
M981	Internal UNIBUS Terminator Module	90.00
M983	RK05 Disk Drive Cable Connector	14.00
M9970	H854-to-Backplane Adapter	35.00
MR873-A	Read-Only Memory Programmer	1,100.00
PDM70-AA,-AB	Programmable Data Mover with Keyboard	1,550.00
PDM70-BA,-BB	Programmable Data Mover with Keyboard and Display	2,050.00
PDM70-CA,-CB	Programmable Data Mover, Basic Box	950.00
PDM70-D	32-Bit Input	300.00
PDM70-E	32-Bit Output	300.00
PDM70-F	4-Channel Analog Input	650.00
PDM70-H	2-Channel Analog Output	450.00
PDM70-J	Bit Serial I/O, EIA or 20 mA	500.00
PDM70-JR	Serial I/O Interface (M7377)	500.00
PDM70-M	8-Bit Parallel Input/Output	430.00
PDM70-N	64-Character PROM Read-In	110.00
PDM70-P	Programmable Bus Control	300.00
PDM70-R	Processor Interface	80.00
PDM70-SD	Foundation Module	185.00
QF500-AB	Software Package	150.00
R001	Diode Network	9.00
R002	Diode Network	9.00
R107	Inverter	25.00
R111	Expandable NAND/NOR Gate	16.00
R113	NAND/NOR Gate	23.00
R121	NAND/NOR Gate	18.00
R122	NOR/NAND Gate	32.00
R123	Input Bus Gate	22.00
R131	Exclusive-OR Gate	37.00
R141	AND/NOR Gate	16.00
R151	Binary-to-Octal Decoder	35.00
R181	DC Carry Chain	37.00

TYPE	TITLE	Price in U.S. dollars
R200	Flip-Flop	16.00
R201	Flip-Flop	23.00
R202	Dual Flip-Flop	27.00
R203	Triple Flip-Flop	30.00
R204	Quadruple Flip-Flop	30.00
R205	Dual Flip-Flop	35.00
R302	Delay	47.00
R303	Integrating One-Shot	53.00
R401	Variable Clock	48.00
R405	Crystal Clock	108.00
R601	Pulse Amplifier	27.00
R602	Pulse Amplifier	33.00
R603	Pulse Amplifier	37.00
R650	Bus Driver	30.00
RT01-AA,-AB	Numeric Data Entry Terminal, 110 Baud	600.00
RT01-BA,-BB	Numeric Data Entry Terminal, 300 Baud	600.00
RT01-NA	Four-Digit Display	100.00
RT01-NB	Eight-Digit Display	200.00
RT01-NC	Twelve-Digit Display	300.00
RT02-AA,-AB	Alphanumeric Data Entry Terminal	1,300.00
RT02-BA,-BB	Full-Keyboard Alphanumeric Terminal	1,500.00
RT02-CA,-CB	Badge Reader Terminal	2,800.00
RTKIT-1	RTM Basic Kit	1,185.00
RTKIT-2	RTM Expander Kit	639.00
VT50	DECscope Video Display Terminal	1,250.00
W002	Clamp Loads	18.00
W005	Clamp Loads	21.00
W011	Flat Ribbon Cable Connector	6.00
W018	Flat Ribbon Cable Connector	9.00
W020	Flat Ribbon Cable Connector	8.00
W021	Flat Ribbon Cable Connector	6.00
W022	Flat Ribbon Cable Connector	6.00
W023	Flat Ribbon Cable Connector	6.00
W024	Round Coaxial (TWP) Cable Connector	10.00
W027	Flat Ribbon Cable Connector	7.00
W028	Round Coaxial (TWP) Cable Connector	6.00
W031	Flat Mylar Cable Connector	5.00
W033	Flat Mylar Cable Connector	5.00
W040	Solenoid Driver	38.00
W042	10 Amp Driver	134.00
W043	Solenoid Driver	62.00
W050	30 mA Indicator Driver	19.00
W051	100 mA Indicator and Relay Driver	23.00
W061	Relay Driver	37.00
W500	High Impedance Follower	42.00
W501	Negative Input Converter and Schmitt Trigger	21.00
W510	Positive Input Converter	23.00
W511	Negative Input Converter	22.00
W512	Positive Level Converter	27.00
W520	Comparator	46.00
W532	Dual AC-Coupled Difference Amplifiers	32.00
W533	Dual Rectifying Slicer	32.00
W600	Negative Output Converter	19.00

TYPE	TITLE	Price in U.S. dollars
W601	Positive Output Converter	16.00
W602	Bipolar Output Converter	43.00
W603	Positive Level Amplifier	24.00
W607	Pulse Output Converter	55.00
W640	Pulse Output Converter	45.00
W690	DEC to IBM N Line Converter	38.00
W700	Switch Filter	27.00
W705	+3.6 V Power Supply	25.00
W706	Teletype Receiver	162.00
W707	Teletype Transmitter	190.00
W708	Teletype Interface	74.00
W800	Relay	65.00
W802	Relay Multiplexer	172.00
W900	Module Extender Board	100.00
W930	Blank Module	11.00
W940	Wire Wrappable Module	70.00
W941	Wire Wrappable Module	40.00
W942	Wire Wrappable Module with Sockets	140.00
W943	Wire Wrappable Module with Sockets	75.00
W950	Wire Wrappable Module	65.00
W951	Wire Wrappable Module	40.00
W952	Wire Wrappable Module with Sockets	151.00
W953	Wire Wrappable Module with Sockets	81.00
W960	MSI Module Board	8.00
W964	Universal Terminator Board	10.00
W966	OMNIBUS Wire Wrap Module	100.00
W967	OMNIBUS Wire Wrap Module with Sockets	172.00
W968	Collage Module Board	67.00
W969	Collage Module Board	34.00
W970	Blank Module	9.00
W971	Blank Module	14.00
W972	Blank Module, Copper-Clad on Both Sides	9.00
W9720	Blank Module, Copper-Clad on Both Sides	7.00
W9721	Blank Module, Copper-Clad on Both Sides	13.00
W9722	Blank Module, Copper-Clad on Both Sides	27.00
W973	Blank Module, Copper-Clad on Both Sides	15.00
W974	Blank Module, Perforated	9.00
W975	Blank Module, Perforated	19.00
W979	Collage Module Board	26.00
W980	Module Extender Board	15.00
W982	Module Extender Board	19.00
W983	Module Extender Board	29.00
W984	Module Extender Board	32.00
W987	Quad Module Extender Board	43.00
W990	Blank Module	7.00
W991	Blank Module	12.00
W992	Blank Module, Copper-Clad on One Side	4.00
W993	Blank Module, Copper-Clad on One Side	8.00
W998	Blank Module, Perforated	4.00
W999	Blank Module, Perforated	9.00

NOTE 1

Cable Ordering Information

Cables listed with an xx designation are available in lengths specified by the customer; however, the length must be ordered in increments of feet only.

To determine the cost of customer specified length cables, the price per foot of the type of cable required must be added to the basic price of the cable assembly (i.e., soldering the conductors to the connectors and testing the cable assembly). The cable assembly price is listed beside each "BC" cable in the price list. The price of the cable material is listed below.

CABLE TYPES AVAILABLE

Cable Type	Part No.	Price/ Foot
9-Conductor Flat Coax	17-00001-00	$ 1
19-Conductor Flat Mylar	17-00002-00	1
60-Conductor Flat Mylar	17-00002-01	2
40-Conductor Flat Mylar	17-00004-00	2
6-Conductor Round	17-00012	0.50
40-Conductor Round (20-TWP)	17-00018	2
20-Conductor Flat Ribbon	91-07575	0.60
4-Conductor Round	91-07706	0.50
9-Conductor Round Coax	91-07570	0.60
10-Conductor Round	91-07623	0.60
22-Conductor Round (11-TWP)	91-07707	1.50

Example for single cable BC02L-xx Cable Assembly:

BC02L-07

└ denotes cable length in ft.

1 — BC02L-xx	$32.00	
1 — 7 ft. 20-conductor ribbon at $0.60/ft.	4.20	
	$36.20	Total Cost

Example for double cable BC03H-xx Cable Assembly:

BC03H-07

└ denotes cable length in ft.

1 — BC03H-xx	$58	
2 — 7 ft. 19-conductor flat mylar at $1/ft.	14	
	$72	Total Cost

NOTE 2

Contact Sales Support Manager, Logic Products, for pricing information.

DIGITAL EQUIPMENT CORPORATION, Corporate Headquarters: Maynard, Massachusetts 01754, Telephone: (617) 897-5111
SALES AND SERVICE OFFICES
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