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M SERIES

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FOREWORD

This seventh edition of the LOGIC HANDBOOK is your guide to the most extensive line of products offered by Digital Equipment Corporation for implementing electronic logic designs for instrumentation, computer interfacing, data gathering or control. This handbook is a basic reference for anyone involved in specifying, manufacturing or using solid state logic.

Our M Series TTL integrated circuit modules are featured in this edition. The M Series line consists of more than 95 modules ranging from basic and functional logic modules to self contained computer interfacing modules. In addition to the new M Series modules, we are now offering a new M Series Logic Lab for use in breadboarding M Series logic designs. This new lab is discussed in the "Lab Series" section.

This handbook also discusses an expanded line of special purpose logic boards, W Series, which can be used for a variety of purposes including prototype construction, limited production runs and for configuring a collection of logic functions from a series of modules. Our expanded line of A Series analog modules is also fully discussed. More than two dozen modules are now in this line.

The K Series line of control logic modules is presented here in summary form but is fully described, along with other control products, in our CONTROL HANDBOOK. As with our other logic lines, K Series has been expanded again and now features some 90 units.

The R, B, and W Series negative logic modules are covered in previous editions of the LOGIC HANDBOOK.

As the cost of the basic logic itself decreases, it becomes increasingly important that efficient, reliable, and inexpensive hardware be available to keep total system costs down. Digital provides this hardware. Now, from a few to thousands of modules can be connected, wired, mounted, powered, and enclosed efficiently at the lowest cost per function in the industry.

Digital's complete line of power and hardware accessories provides everything needed to put your designs into action, from connector blocks to mounting cabinets. Power supplies, connector block variations, mounting panels, blank module configurations, connector cards and a complete line of computer-grade cabinetry are among the well over 100 different hardware, power, and accessory items described in this edition of the LOGIC HANDBOOK.

ACKNOWLEDGEMENTS

The production of a publication of this size and complexity can be achieved only through the efforts and cooperation of dozens of people. These include engineers, writers, artists, and production personnel. While it is impossible to cite all, a few individuals deserve special mention. Among these are: Dwight Baker of the Control Products Group module engineering staff who prepared and assembled most of the technical material for this Handbook; Elliott Hendrickson and his staff for their art direction and production assistance; and Joseph Codispoti for his editorial assistance. The cover of this Handbook was conceived and executed for Digital by Elliott Hendrickson.

March, 1971

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M Series Logic Modules

The development of monolithic integrated circuits has had an impact on the design of digital module systems. Advantages of small size and high operating speeds made these circuits initially attractive. However, a lower price/performance ratio compared to hybrid or discrete component modules offset the advantages. Recently, significant price reductions in both TTL (transistor-transistor logic) and DTL (diode-transistor logic) integrated circuits indicated a re-evaluation was needed.

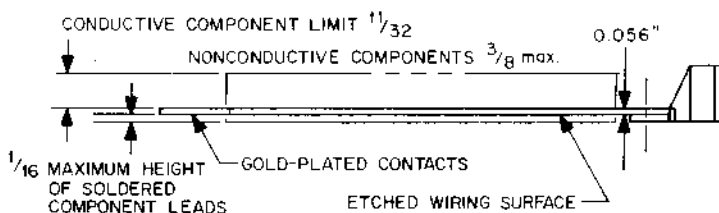
DIGITAL EQUIPMENT CORPORATION undertook a study of both types of logic, their performance in large and small systems, and their ease of use in system design. The result of this study is the M Series Integrated Circuit FLIP CHIP™ Module.

M Series modules contain high speed TTL logic in both general purpose and functional logic arrays. TTL was chosen for its high speed, capacitance drive capability, high noise immunity and choice of logical elements. High performance integrated circuit modules are now available at approximately one half the price of their discrete or hybrid counterparts.

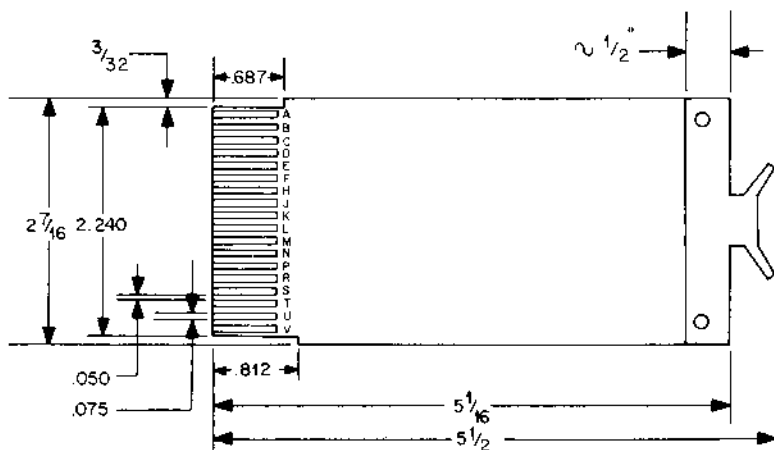
In addition to the reduced cost of integrated circuits, Digital's advanced manufacturing methods and computer controlled module testing have resulted in considerable production cost savings, reflected in the low price of all M Series Modules.

STANDARD MODULE DIMENSIONS

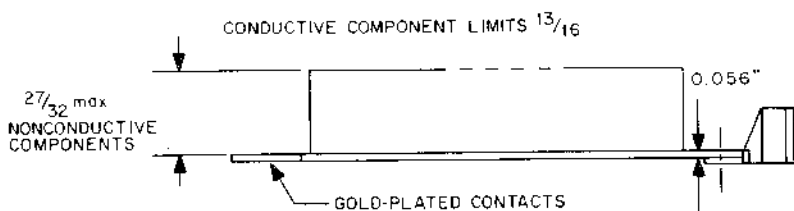
SINGLE WIDTH FLIP CHIP MODULE



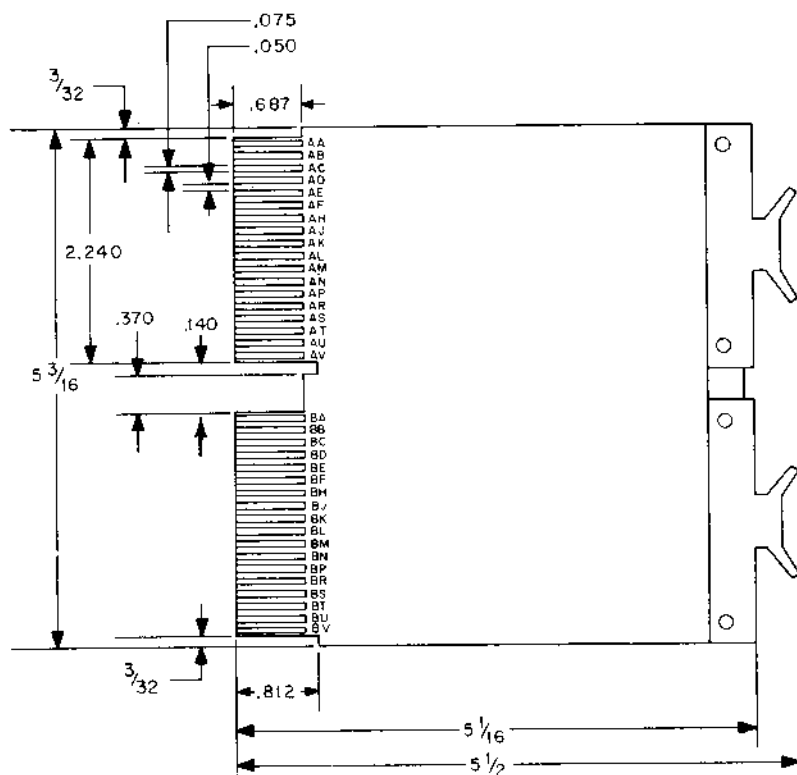
SINGLE HEIGHT FLIP CHIP MODULE



DOUBLE WIDTH FLIP CHIP MODULE

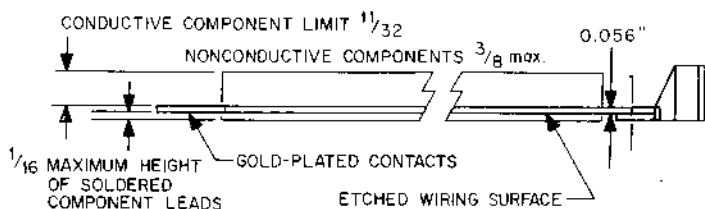


DOUBLE HEIGHT FLIP CHIP MODULE

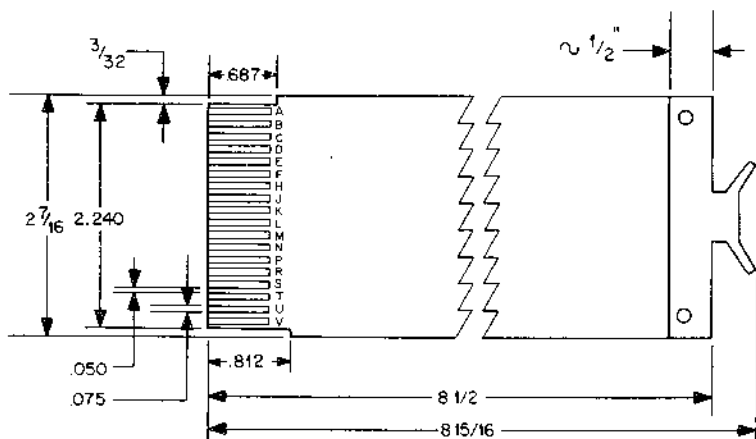


EXTENDED MODULE DIMENSIONS

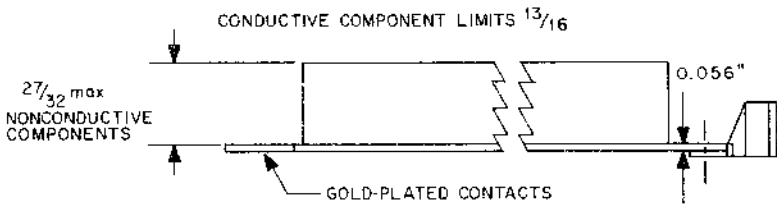
SINGLE WIDTH FLIP CHIP MODULE



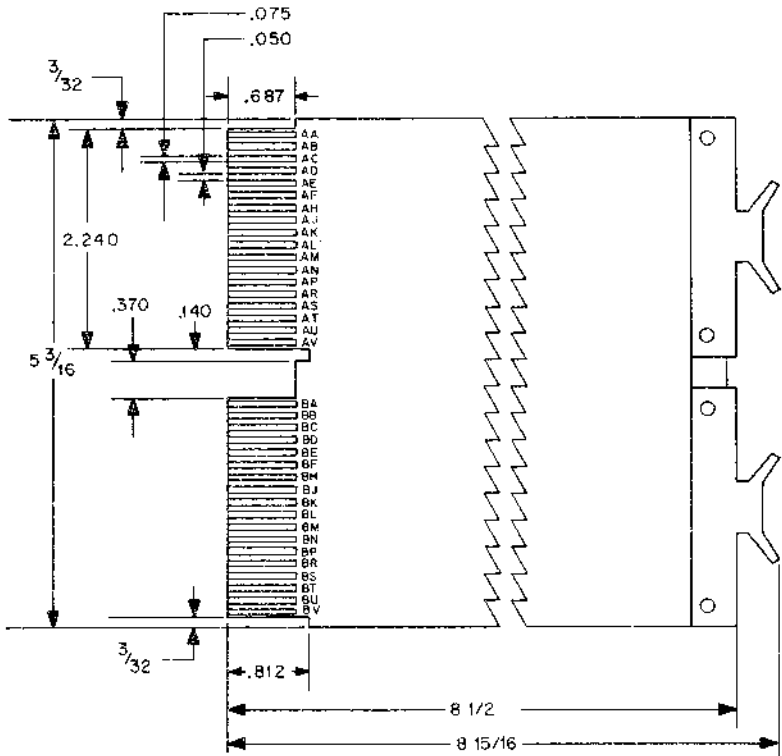
SINGLE HEIGHT FLIP CHIP MODULE



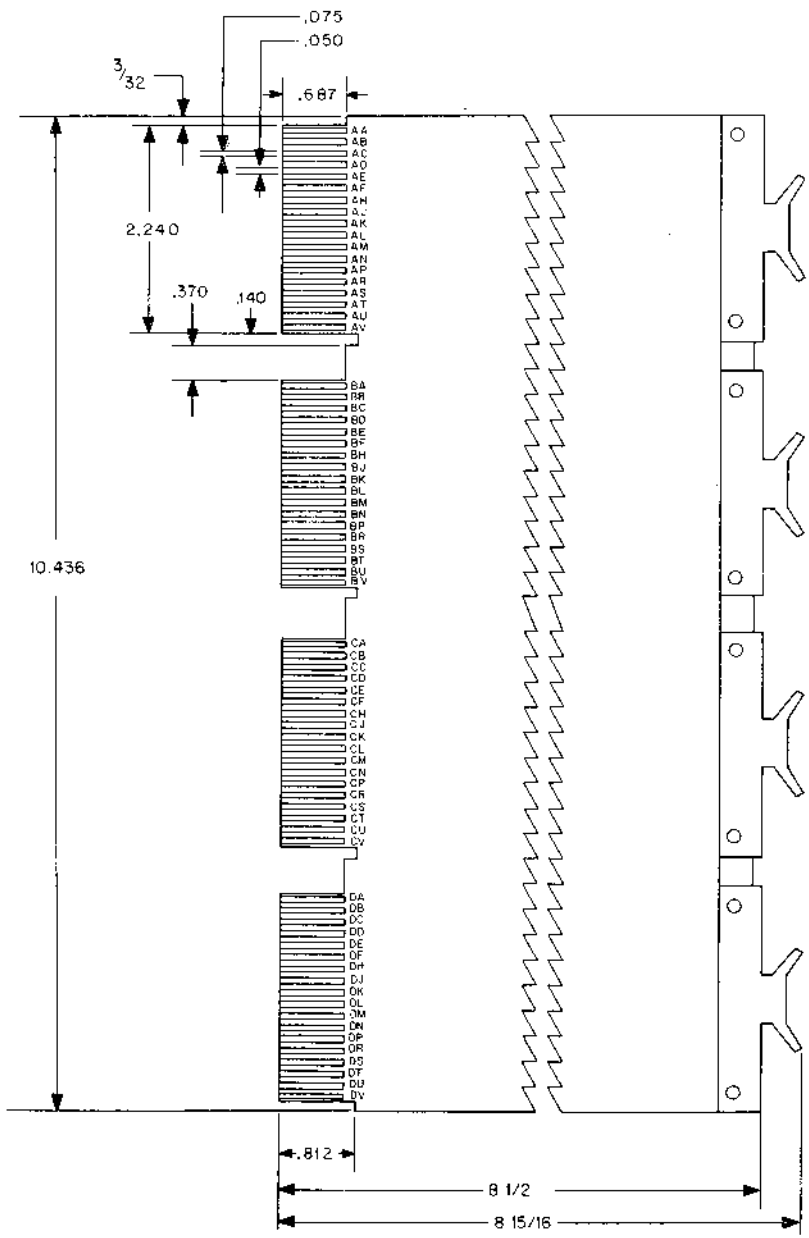
DOUBLE WIDTH FLIP CHIP MODULE

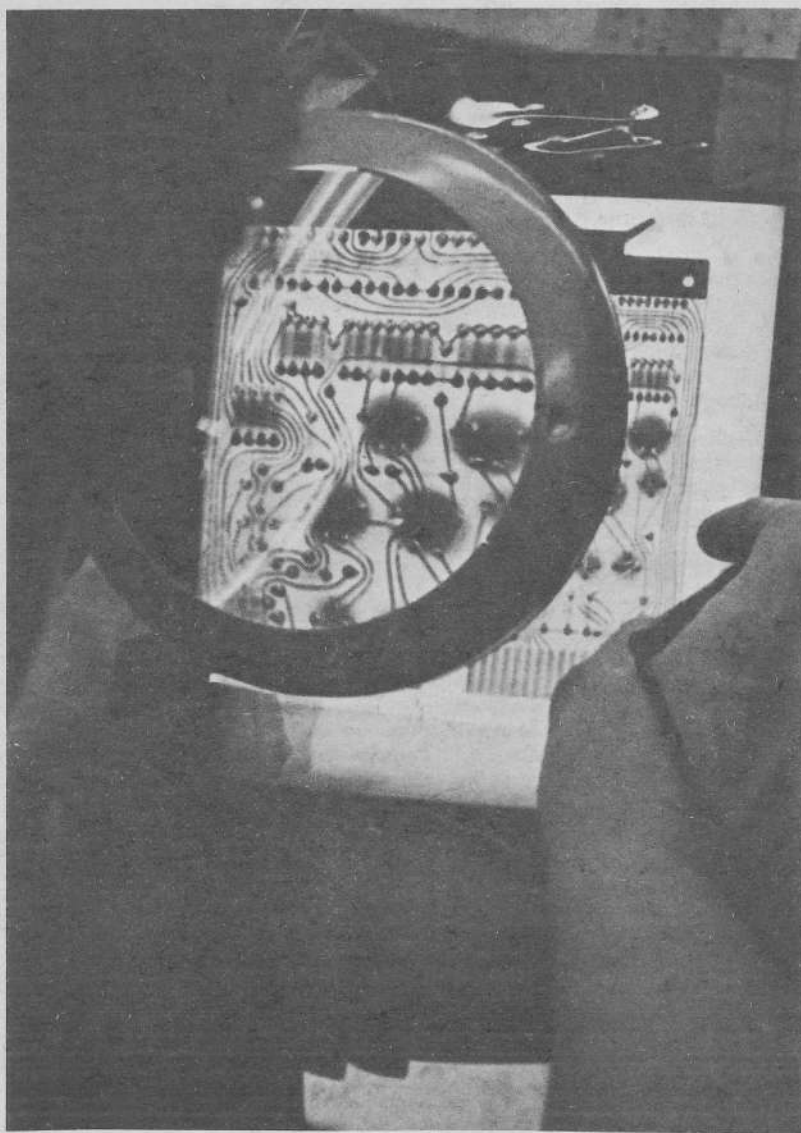


DOUBLE HEIGHT FLIP CHIP MODULE



EXTENDED MODULE DIMENSIONS QUAD HEIGHT





DEC Module assembly lines combine automated manufacturing steps with visual inspection and computer controlled testing.

GENERAL CHARACTERISTICS

M Series high-speed, monolithic integrated circuit logic modules employ TTL (transistor-transistor logic) integrated circuits which provide high speed, high fan out, large capacitance drive capability and excellent noise margins. The M Series includes a full digital system complement of basic modules which are designed with sufficient margin for reliable system operation at frequencies up to 6 MHz. Specific modules may be operated at frequencies up to 10 MHz. The integrated circuits are dual in-line packages.

The M Series printed circuit boards are identical in size to the standard FLIP CHIP™ modules. The printed circuit board material is double-sided providing 36-pins in a single height module. Mounting panels (H910 and H911) and 36-pin sockets (H803 and H808) are available for use with M Series modules. Additional information concerning applicable hardware may be found in the Power Supply & Hardware and Accessories section of this handbook.

M Series modules are compatible with Digital's K Series and, through the use of level converters, are compatible with all of Digital's other standard negative voltage logic FLIP CHIP® modules.

TTL NAND GATE

The basic gate of the M Series is a TTL NAND GATE. Figure 1 is the basic two input NAND gate schematic diagram. The circuit is divided into 3 major sections, the multiple emitter input, the phase splitter and the totem pole output circuit. The two diode model of a transistor shown in Figure 2 will be used in the analysis of the circuit. A forward biased silicon junction (i.e. diode) gives a voltage drop of about 0.75 volts and a saturated silicon transistor has a collector emitter voltage of 0.4 volts average. These two figures will be used throughout the following discussion.

With either input at the LO logic level (0.0V-0.8V) the multiple emitter input transistor will be ON with its base residing at about $0.75 + 0.4 = 1.15$ volts. The three diode string consisting of Q_1 's base collector diode, Q_2 's base emitter diode, and Q_4 's base emitter diode will have only 1.15 volts across it and will therefore be conducting only leakage currents ($0.75 + 0.75 + 0.75 = 2.25$ volts required for forward bias). With no current flowing into the base emitter junction of Q_2 , the transistor will be OFF and its collector emitter voltage is allowed to rise. Similarly with no current flowing in the base emitter diode of Q_3 , the transistor is OFF and its collector emitter voltage is allowed to rise. When both Q_2 and Q_3 are OFF, Q_1 is freed to pull the output voltage to a HI level. The voltage levels present in the circuit with one or more LO inputs is shown in Figure 4.

If both inputs are HI (2.4-3.6 volts) the head of the three diode string will reside at about 2.25 volts and there will be a current path from the 4K base resistor on the input transistor through the diode string to ground as shown in Figure 5. With current flowing in the base emitter junctions of both Q_2 and Q_3 , both transistors will be turned ON. Q_1 is held OFF whenever Q_2 is ON. The output is driven LO (0.0V-0.4V) by transistor Q_4 . The voltage levels present in the circuit with both inputs HI and are shown in Figure 6.

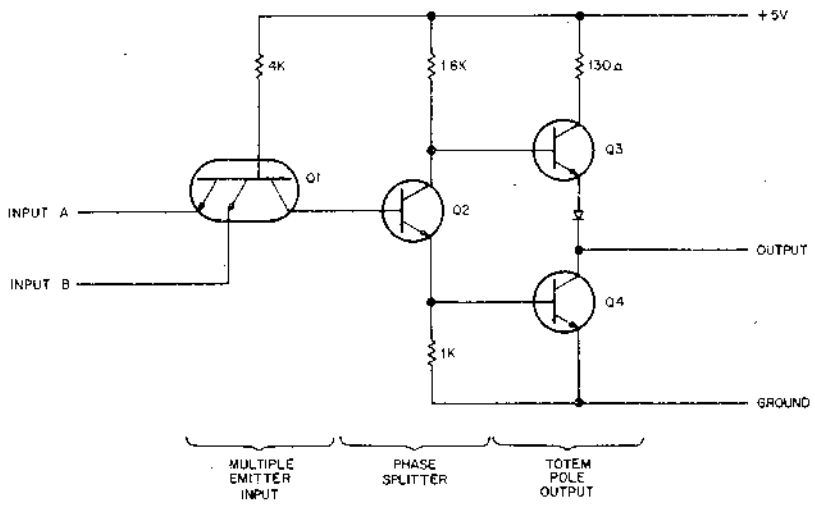


Figure 1 TTL NAND Gate Schematic Diagram

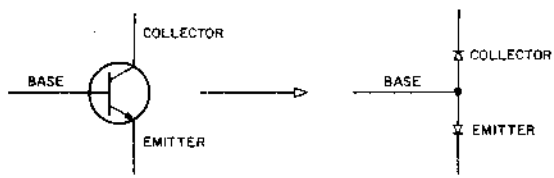


Figure 2 Two Diode Model For Transistor

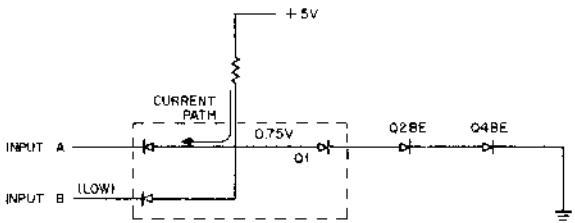


Figure 3 Diode Equivalent NAND Gate Circuit. One Input LO

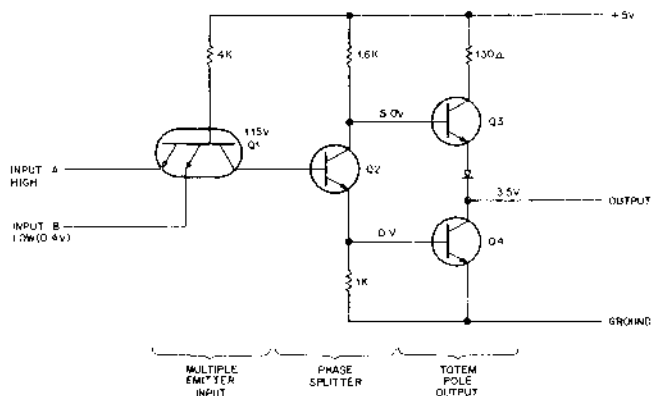


Figure 4 TTL NAND Gate Schematic Diagram, One Input LO

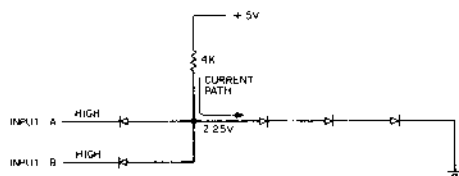


Figure 5 Diode Equivalent NAND Gate Circuit, Both Inputs HI

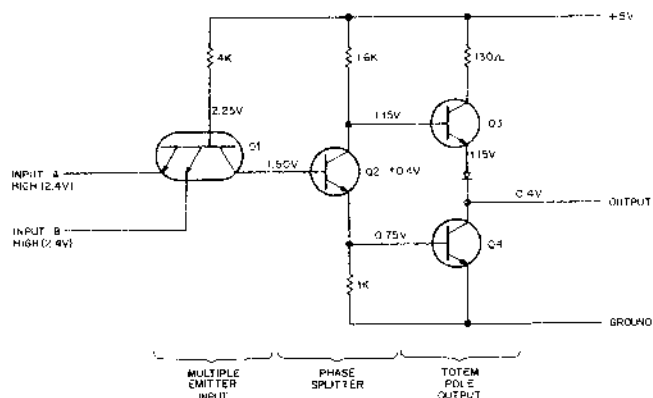


Figure 6 TTL NAND Gate Schematic Diagram, Both inputs HI

OPERATING CHARACTERISTICS

Power Supply Voltage: 5 Volts \pm 5%

Operating Temperature Range: 0° to 70°C

Speed: M Series integrated circuit modules are rated for operation in a system environment at frequencies up to 6 MHz. Specific modules may be operated at higher frequencies as indicated by the individual module specifications.

LOGIC LEVELS AND NOISE MARGIN

A gate input will recognize 0.0 volts to 0.8 volts as logical LO and 2.0 volts to 3.6 volts will be recognized as a logical HI. An output is between 0.0 volts and 0.4 volts in the logical LO condition. The logical HI output condition is between 2.4 volts and 3.6 volts. Figure 7 shows diagrammatically the acceptable transistor-transistor logic levels. The worst case noise margin is 400 millivolts that is, an output would have to make at least a 400 millivolt excursion to cause an input which is connected to it to go into the indetermined voltage region. For instance if an output were at 0.4 volts (worst case logical LO) there would have to be a + 400 mv swing in voltage to cause inputs connected to it to go into their indetermined region.

Input and Output Loading: The input loading and output drive capability of M Series modules are specified in terms of a specific number of unit loads. Typically the input loading is one unit, however certain modules may contain inputs which will present greater than one unit load. The typical M Series module output will supply 10 unit loads of input loading. However, certain module outputs will deviate from a 10 unit load capability and provide more or less drive. Always refer to the individual module specifications to ascertain actual loading figures.

Unit Load: In the logic 0 state, one unit load requires that the driver be able to sink 1.6 milliamps (maximum) from the load's input circuit while maintaining an output voltage of equal to or less than +0.4 volts. In the logic 1 state, one unit load requires that the driver supply a leakage current 40 microamps (maximum) while maintaining an output voltage of equal to or greater than +2.4 volts.

Timing: M Series pulse sources provide sufficient pulse duration to trigger any M Series flip-flop operating within maximum propagation delay specifications. Detailed timing information appears later in this section and in the module specifications.

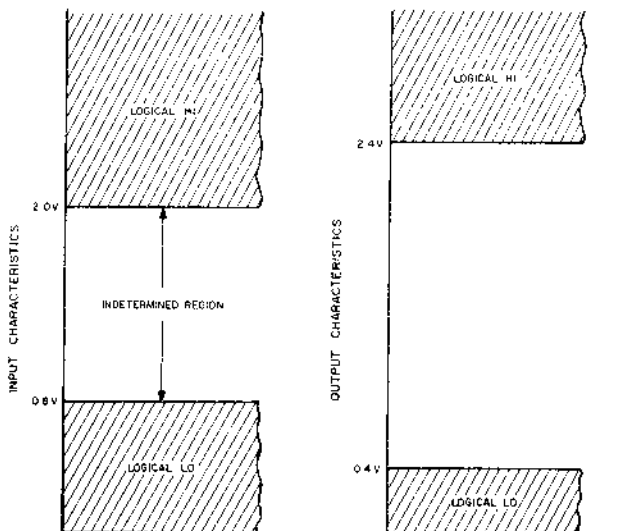


Figure 7 Logic Levels

NAND Logic Symbol: Logic symbology used to describe M Series modules is based on widely accepted standards. Logic symbols and a truth table for the NAND gate are shown in Figure 8.

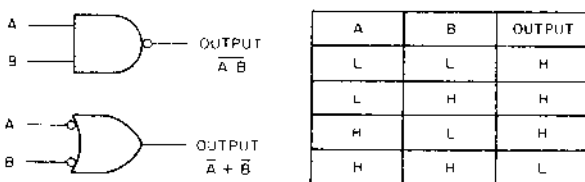


Figure 8 NAND Gate Logic Symbol and Truth Table

The first symbol is visually more effective in applications where two high inputs are ANDed to produce a low output. The second symbol better represents an application where low inputs are ORED to produce a high output.

TTL AND/NOR GATE

With a few modifications, the basic TTL NAND gate can perform an AND/NOR function useful in exclusive OR, coincidence, line selection and NOR gating operations. The modified circuit is shown in simplified form in Figure 9.

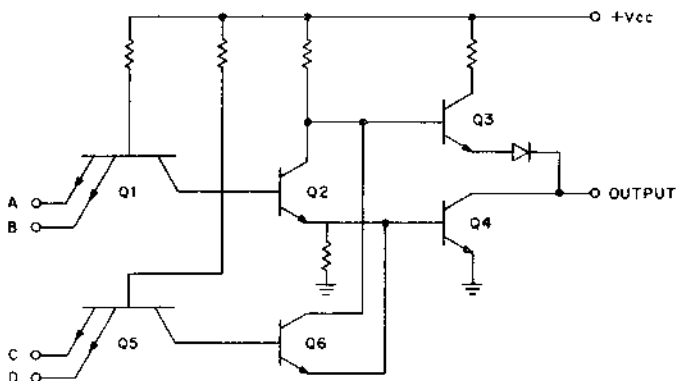


Figure 9 TTL AND/NOR Gate Simplified Schematic

Circuit Operation: The basic elements of the TTL NAND gate are used without modification. The phase-splitter (Q2) is paralleled with an identical transistor (Q6), also controlled by multiple-emitter input transistor which receives two additional inputs, C and D. When either of the input pairs are high, the phase inverter operates to switch the output voltage low. Circuit performance is essentially identical to the TTL NAND circuit.

AND/NOR Logic Symbol: The logic symbols for the AND/NOR gate are shown and defined in Figure 10.

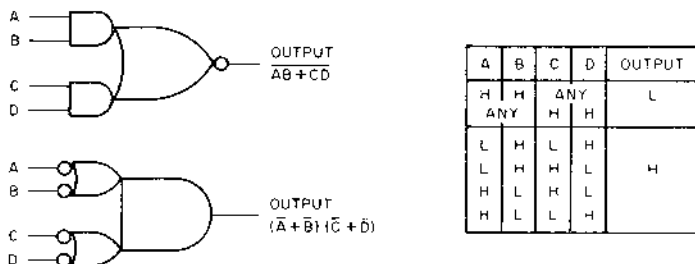


Figure 10 AND/NOR Gate Logic Symbols and Truth Table

NOR Configuration: The AND/NOR gate can perform a straight NOR function if the AND gate inputs are tied together as shown in Figure 11.

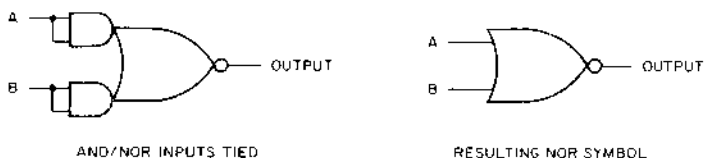
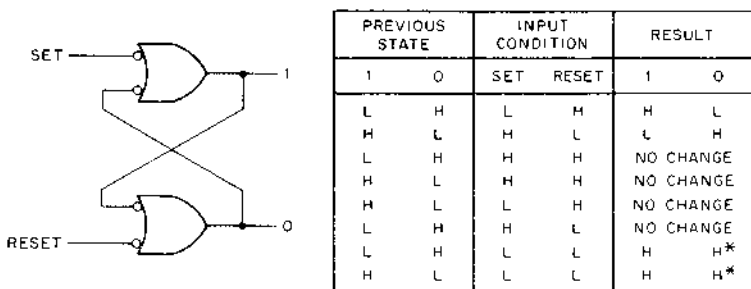


Figure 11 NOR Connection of AND/NOR Gate

NAND GATE FLIP-FLOPS

RS Flip-Flop: A basic Reset/Set flip-flop can be constructed by connecting two NAND gates as shown in Figure 12.



Ambiguous state: In practice the input that stays low longest will assume control.

Figure 12 RESET/SET NAND Gate Flip-Flop

CLOCKED NAND GATE FLIP-FLOPS

The Reset-Set flip-flop can be clock-synchronized by the addition of a two-input NAND gate to both the set and the reset inputs. (See Figure 13.) One of the inputs of each NAND is tied to a common clock or trigger line.

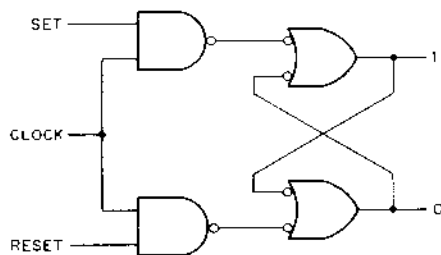


Figure 13 Clocked NAND Gate Flip-Flop

A change of state is inhibited until a positive clock pulse is applied. The ambiguous case will result if both the set and reset inputs are high when the clock pulse occurs.

M SERIES GENERAL-PURPOSE FLIP-FLOPS

Two types of general-purpose flip-flops are available in the M Series, both of which have built-in protection against the ambiguous state characteristic of NAND gate flip-flops.

FLIP-FLOP CLOCK INPUT SYMBOLS

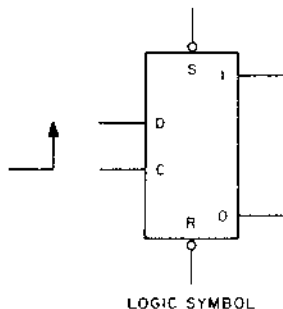
The D type flip-flop is a true leading (positive going voltage) edge triggered flip-flop and the D input is locked out until the clock input returns to low. The symbol to indicate this function will be as follows;

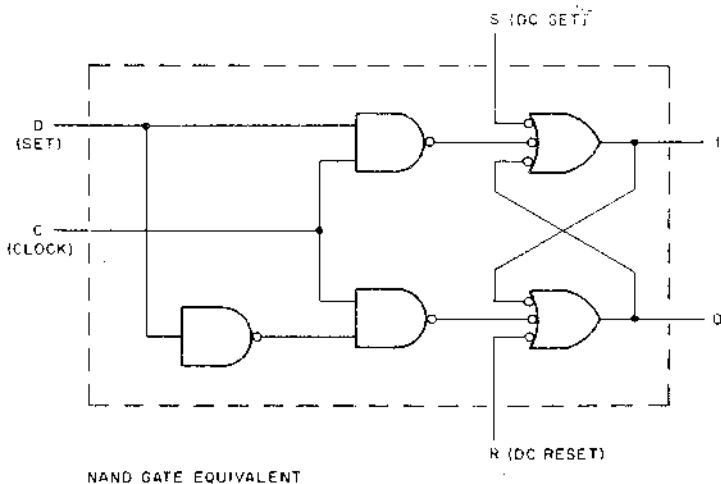


The operation of the J-K type flip-flop is to transfer the information present at the J and K inputs just prior to and during the clock pulse to the master flip-flop when the threshold is passed on the leading (positive going voltage) edge of the clock pulse. The information stored in the master flip-flop is transferred to the slave flip-flop, and consequentially to the outputs, when the threshold is passed on the trailing (negative going voltage) edge of the clock pulse. The symbol to indicate this function will be as follows;



D Type Flip-Flop: The first of these is the D type flip-flop shown in Figure 14. In this element, a single-ended data input (D) is connected directly to the set gate input. An inverter is provided between the input line (D) and the reset input. This ensures that the set and reset levels cannot be high at the same time.





SIMPLIFIED NAND GATE EQUIVALENT

Figure 14. D Type General Purpose Flip-Flop

The flip-flop proper employs three-input NAND gates to provide for dc set and reset inputs.

D type flip-flops are especially suited to buffer register, shift register and binary ripple counter applications. Note that D type devices trigger on the leading (or positive going) edge of the clock pulse. Once the clock has passed threshold, changes on the D input will not affect the state of the flip-flop due to a lockout circuit (not shown).

A characteristic of the D type flip-flop which is not illustrated in the NAND gate equivalent circuit is the fact that the D input is locked out after the clock input threshold voltage on the leading (positive going voltage) edge of the clock has been passed. The D input is not unlocked until the clock input threshold voltage of the trailing (negative going voltage) edge has been passed.

"MASTER-SLAVE J-K FLIP-FLOP"

The two unique features of a J-K flip-flop are: A) a clock pulse will not cause any transition in the flip-flop if neither the J nor the K inputs are enabled during the clock pulse, and B) if both the J and the K inputs are enabled during the clock pulse, the flip-flop will complement (change states). There is no indeterminate condition in the operation of a J-K flip-flop.

A word of caution is in order concerning the clock input. The J and K inputs must not be allowed to change states when the clock line is high, the output will complement on the negative going voltage transition of the clock. It is for this reason that the clock line must be kept low until it is desired to transfer information into the flip-flop and no change in the states of the J and K inputs should be allowed when the clock line is high.

The J-K flip-flops used are master-slave devices which transfer information to the outputs on the trailing (negative going voltage) edge of the clock pulse. The J-K flip-flop consists of two flip-flop circuits, a master flip-flop and a slave flip-flop. The information which is present at the J and K inputs when the leading edge threshold is passed and during the clock high will be passed to the master flip-flop (The J and K inputs must not change after the leading edge threshold has been passed). At the end of the clock pulse when the threshold of the clock is passed during the trailing (negative going voltage) edge, the information present in the master flip-flop is passed to the slave flip-flop. If the J input is enabled and the K input is disabled prior to and during the clock pulse, the flip-flop will go to the "1" condition when the trailing edge of the clock occurs. If the K input is enabled and the J input is disabled prior to and during the clock pulse, the flip-flop will go to the "0" condition when the trailing edge of the clock pulse occurs. If both the J and K inputs are enabled prior to and during the clock pulse, the flip-flop will complement when the trailing edge of the clock pulse occurs. If both the J and K inputs are disabled prior to and during the clock pulse, the flip-flop will remain in whatever condition existed prior to the clock pulse when the trailing edge of the clock pulse occurs.

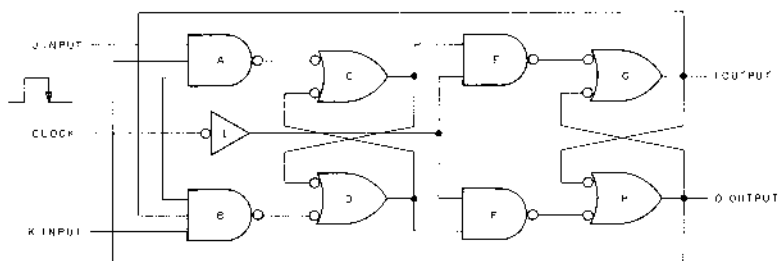


Figure 15. Master-Slave J-K Flip-Flop

Figure 16 shows a functional block diagram of a master slave J-K flip-flop using NAND gates. Gates C and D are the master flip-flop. Gates G and H are the slave flip-flop. Gates A and B are the steering network of the master flip-flop and the steering network for the slave flip-flop is comprised of gates E, F, and I. The 1 output of the master flip-flop is point X. The operation of the flip-flop will be studied by examining the "1" to "0" transition of the flip-flops, with both the J and the K inputs enabled with a HI level before the clock pulse. When the leading edge of a HI clock pulse occurs, gate B will be enabled with three HI inputs. This will provide a RESET signal for the master flip-flop which will then go to the "0" condition. The slave flip-flop remains in the "1" condition while the clock pulse is HI because gate I is providing a LO signal to both gates E and F, thereby blocking inputs to the slave flip-flop. When the trailing edge of the clock pulse occurs, gate F will be enabled with a HI level at both its inputs and a RESET signal will be provided to the slave flip-flop, which will then go to the "0" condition. The next clock pulse, with both the J and K enabled, would cause the master flip-flop to go to the "1" condition on the leading edge of the clock pulse and cause the slave flip-flop to go to the "1" condition on the trailing edge of the pulse. Figure 16 is a truth table for the J-K flip-flop showing all eight possible initial conditions.

INITIAL CONDITIONS				FINAL CONDITIONS	
OUTPUTS		INPUTS		OUTPUTS	
1	0	J	K	1	0
LO	HI	LO	LO	LO	HI
LO	HI	LO	HI	LO	HI
LO	HI	HI	LO	HI	LO
LO	HI	HI	HI	HI	LO
HI	LO	LO	LO	HI	LO
HI	LO	LO	HI	LO	HI
HI	LO	HI	LO	HI	LO
HI	LO	HI	HI	LO	HI

Figure 16. Master-Slave J-K Flip-Flop Truth Table

UNUSED INPUTS (GATES AND FLIP-FLOPS)

Since the input of a TTL device is an emitter of a multiple-emitter transistor, care must be exercised when an input is not to be used for logic signals. These emitters provide excellent coupling into the driving portions of the circuit when left unconnected. To insure maximum noise immunity, it is necessary to connect these inputs to a source of Logic 1 (High). Two methods are recommended to accomplish this:

1. Connect these inputs to a well filtered and regulated source of +3 volts. Pins U1 and V1 are provided on the M113, M117, M119, M121, M617, and M627 for this purpose.
2. Connect these inputs to one of the active inputs on the same gate. This results in a higher leakage current due to the parallel emitters and should be considered as an additional unit load when calculating the loading of the driving gate.

Connection of unused inputs to the supply voltage, V_{cc} , is not advisable, since power supplies are subject to transients and voltage excursions which could damage the input transistor.

TIMING CONSIDERATIONS

Standard Timing Pulse: In digital system design, a reference for system timing is usually required. The M Series modules M401 or M405 produces a standard pulse which provides such a reference. The standard pulse derived from each of these two modules is shown in Figure 17.

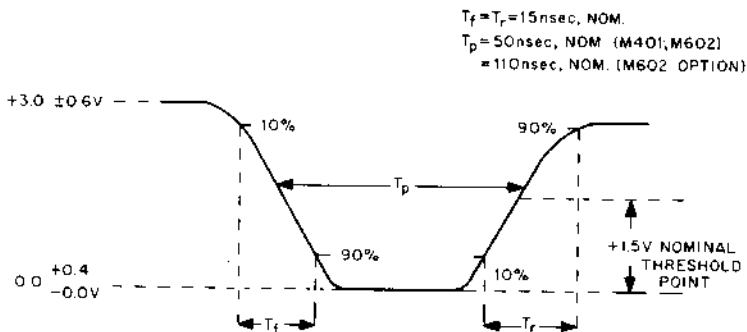


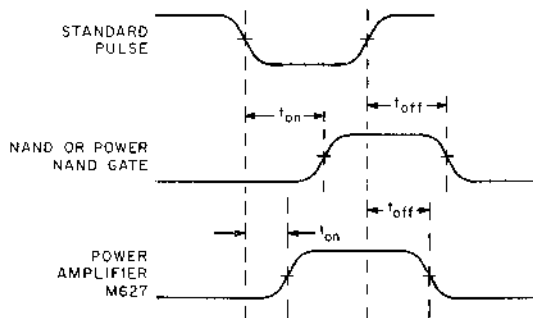
Figure 17. Standard Pulse

NAND Gate and Power Amplifier Propagation Delays: The standard pulse (Figure 17) is distributed throughout a system in negative form to maintain the leading edge integrity. (Since the TTL gate drives current in the logic 0 state, the falling edge is more predictable for timing purposes.) However, the standard pulse is of the wrong polarity for use as a clocking input to the type D and J-K flip-flops, requiring the use of a local inverter. Ordinarily, a NAND inverter is adequate. Where high fan-out is necessary, a M617 Power NAND is preferred.

For applications requiring both high fan-out and critical timing the M627 Power Amplifier is available. This module contains extremely high-speed gates which exhibit turn-on times differing by only a few nanoseconds.

Simultaneity is desirable in clock or shift pulses distributed to extended shift registers or synchronous counters.

Delays introduced by inverting gates and power amplifiers are illustrated in Figure 18. (Delays are measured between threshold points.)



DELAY (NANOSECONDS)			
t_{on}		t_{off}	
TYP.	MAX.	TYP.	MAX.
18	29	8	15
7	—	5	—

Figure 18. NAND Gate and Power Amplifier Delays

Flip-Flop Propagation Delays: D type flip-flops trigger on the leading or rising edge of a positive clock pulse; the propagation delay is measured from the threshold point of this edge. The set-up time of the D flop is also measured from this threshold point. Data on the D input must be settled at least 20 nanoseconds prior to the clock transition. The advantage of the D-flip-flop, however, is that the leading edge triggering allows the flip-flop AND gates to propagate while the clock pulse is still high. Figure 19 illustrates this situation.

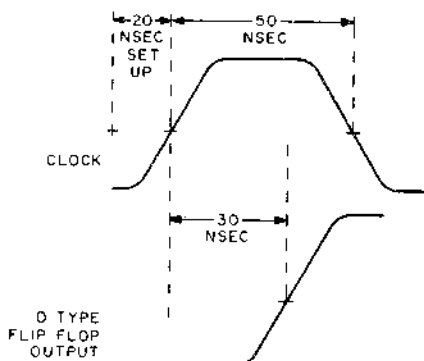


Figure 19. D Type Flip-Flop Timing

JK type flip-flops are, in effect, trailing edge triggering devices as explained previously. The only restriction on the J and K inputs is that they must be settled by the time that the rising edge occurs. Timing is shown in Figure 20.

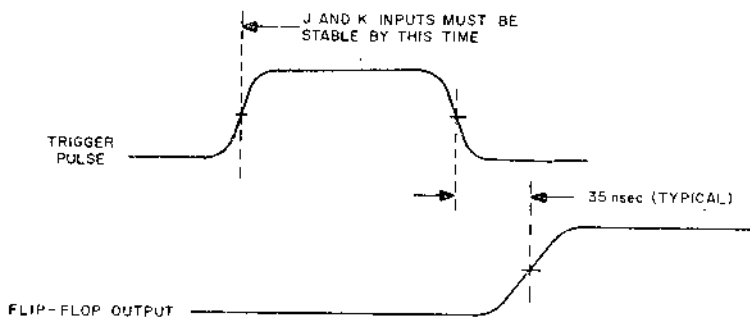


Figure 20. J-K Flip-Flop Timing

When using the dc Set or Reset inputs of either flip-flop type, propagation delays are referenced to the falling edge of the pulse. This is due to the inverted sense of these inputs. When resetting ripple type counters (where the output of one flip-flop is used as the trigger input to the next stage) the reset pulse must be longer than the maximum propagation delay of a single stage. This will ensure that a slow flip-flop does not introduce a false transition, which could ripple through and result in an erroneous count.

One-Shot Delay: Calibrated time delays of adjustable duration are generated by the M302 Delay Multivibrator. When triggered by a level change from a logical one to a logical zero, this module produces a positive output pulse that is adjustable in duration from 50 to 750 nsec with no added capacitance. Delays up to 7.5 milliseconds are possible without external capacitance. (See M302 specification.) Basic timing and the logic symbol are shown in Figure 21. The 100 picofarad internal capacitance produces a recovery time of 30 nsec. Recovery time with additional capacitance can be calculated using the formula;

$$t_r \text{ Nanoseconds} = \frac{30 C \text{ Total (Picofarads)}}{100}$$

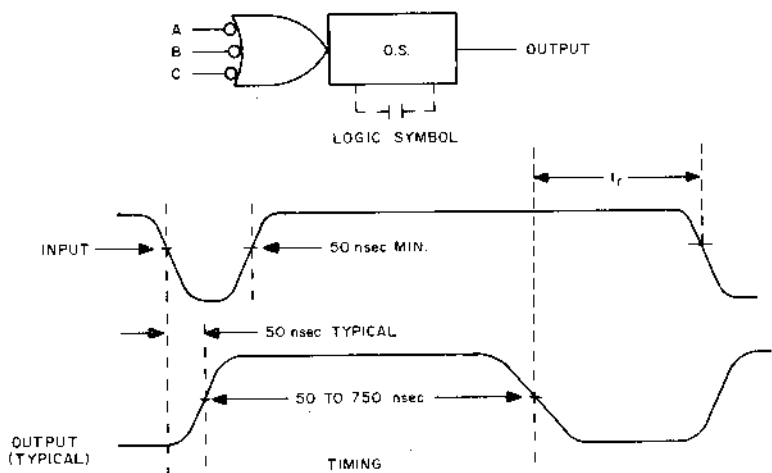


Figure 21. One-Shot Delay Timing and Logic Symbol

SYSTEM OPERATING FREQUENCY

Although individual propagation delays are significant in the design of digital logic, even more important is the maximum operating frequency of a system which is composed of these individual modules. Specifically designed systems may be operated at 10 MHz, but a more conservative design may result in a somewhat lower operating speed. M Series modules can be designed into a system with a 6 MHz clock rate with relative ease. This system frequency is derived by summing the delays in a simple logic chain:

1. A standard clock pulse width of 50 nsec is assumed. This period is measured from the threshold point of the leading edge to the threshold point of the trailing edge.
2. One flip-flop propagation delay of 35 nsec from the trailing edge of the clock pulse to the threshold point of the final state of the flip-flop is allowed.
3. Two gate-pair delays of 30 nsec each are assumed. (A gate-pair consists of two inverting gates in series.) Two gate-pair delays are usually required to perform a significant logic function with a minimum of parallel operations. The two gate-pair delays total 60 nsec.

The time necessary to perform these operations before the next occurrence of the clock pulse is the sum of the delays; $50 + 35 + 60$, or 145 nsec. Allowing 20 nsec for variations within the system, the resulting period is 165 nsec, corresponding to a 6 MHz clock rate. This timing is demonstrated in Figure 22.

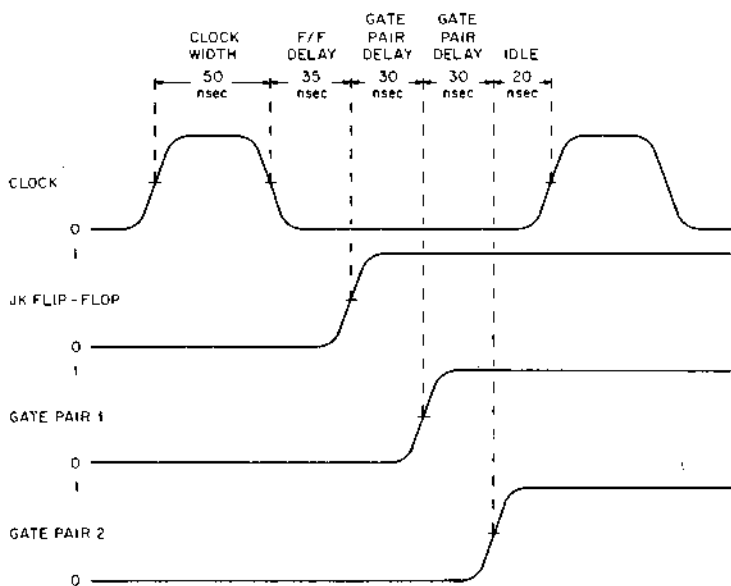


Figure 22. Delays Determining System Operating Frequency

Substitution of a D type flip-flop results in a similar timing situation. In a system using both D and J-K flip-flops, note that the D flip-flop triggers on the leading edge of the clock pulse and the J-K flip-flop triggers on the trailing edge. When calculating system timing using D flip-flops, remember that the flip-flop inputs must be settled at least 20 nsec prior to the occurrence of the clock pulse.

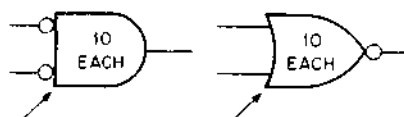
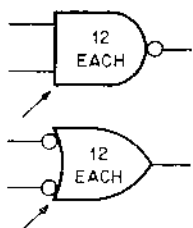
Preparation of a timing diagram that considers delays introduced by all logic elements will aid the designer in achieving predictable system performance.

LOGIC APPLIQUES**M
SERIES**

For convenient drawing of neat block diagrams, to supplement the DEC drawing template, self sticking matte-surface appliques lift from backing with a sharp knife.

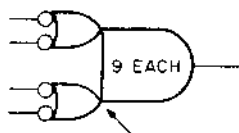
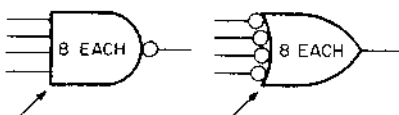
	DIAGRAMS	MODULES	APPLIQUE TYPE
12	2-input NOR,	M101, M113	DRT-1-47
12	2-input NAND	K113, M141	
10	2-input NAND,	M112	DRT-1-03
10	2-input NOR		
8	4-input NOR,	M117, M617,	DRT-1-35
8	4-input NAND	M627	
10	8-input NOR,	M119	DRT-1-51
10	8-input NAND		
9	4-input AND/NOR	M121, M160	DRT-1-25
9	4-input NOR/AND		
3	Binary to Octal/Decimal Decoder	M161	DRT-1-20
24	JK Flip-flops	M203, M206, M207	DRT-1-23
16	JK Flip-flops with gates	M204	DRT-1-22
3	8-bit Buffer/Shift Register	M208	DRT-1-41
18	Level Converters	M502, M652	DRT-1-39
10	NOR Level Converters	M506	DRT-1-52
10	NAND Level Converters		
7	NOR Pulse Amplifiers	M602, M650	DRT-1-34
7	AND Pulse Amplifiers		
2	12-input AND/NOR	M160, M302	DRT-1-21
2	12-input NOR/AND	M401	
2	Timers, 2 clocks		

PRICE: \$1.50/sheet

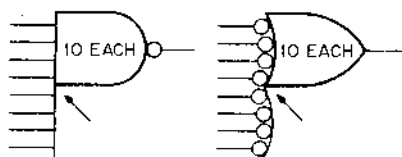
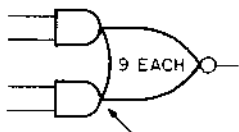


M117, M617, M627

M121, M160

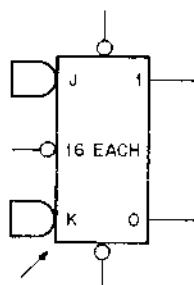
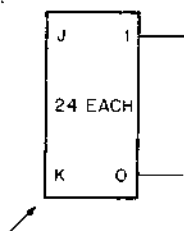


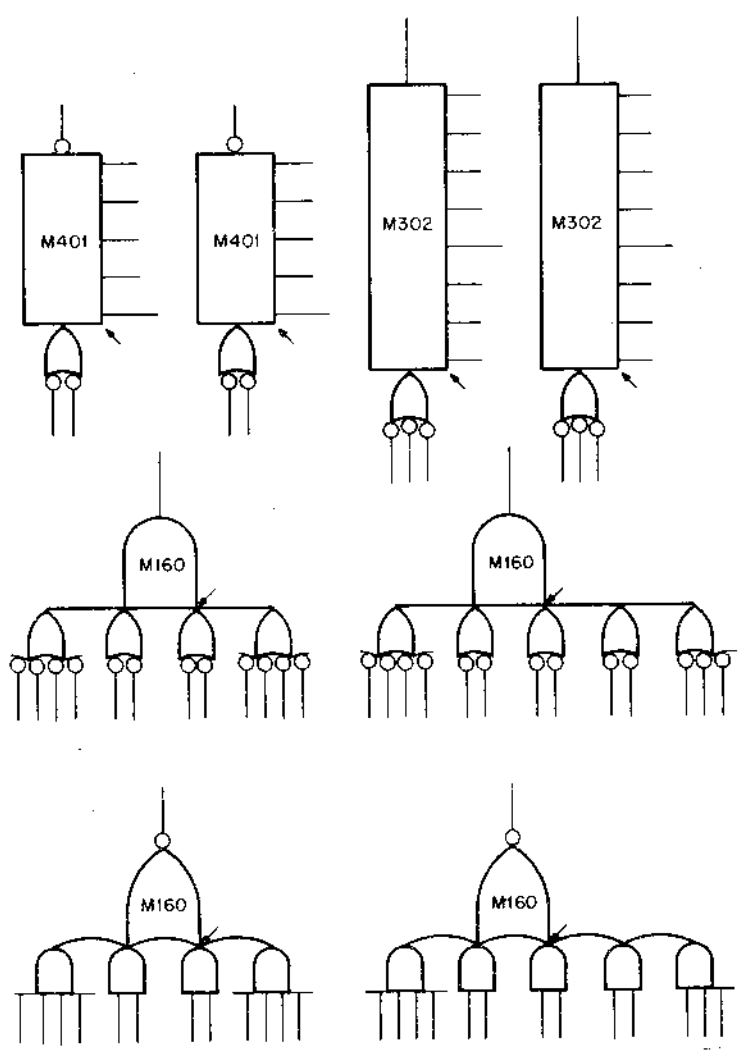
M119



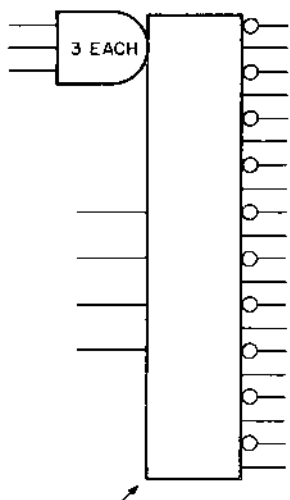
M203, M206, M207

M204

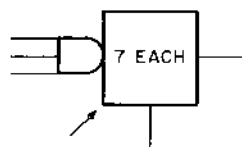
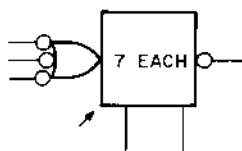




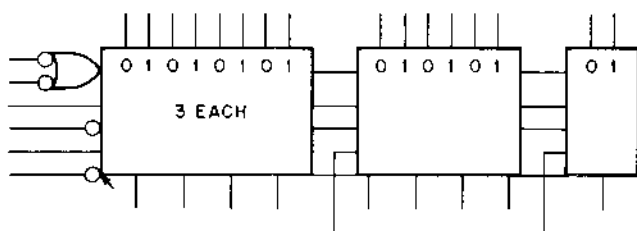
M161



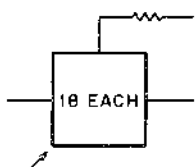
M602, M650



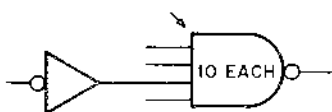
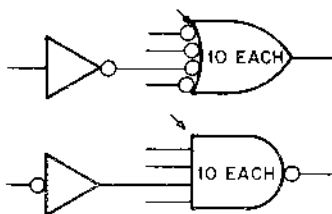
M208

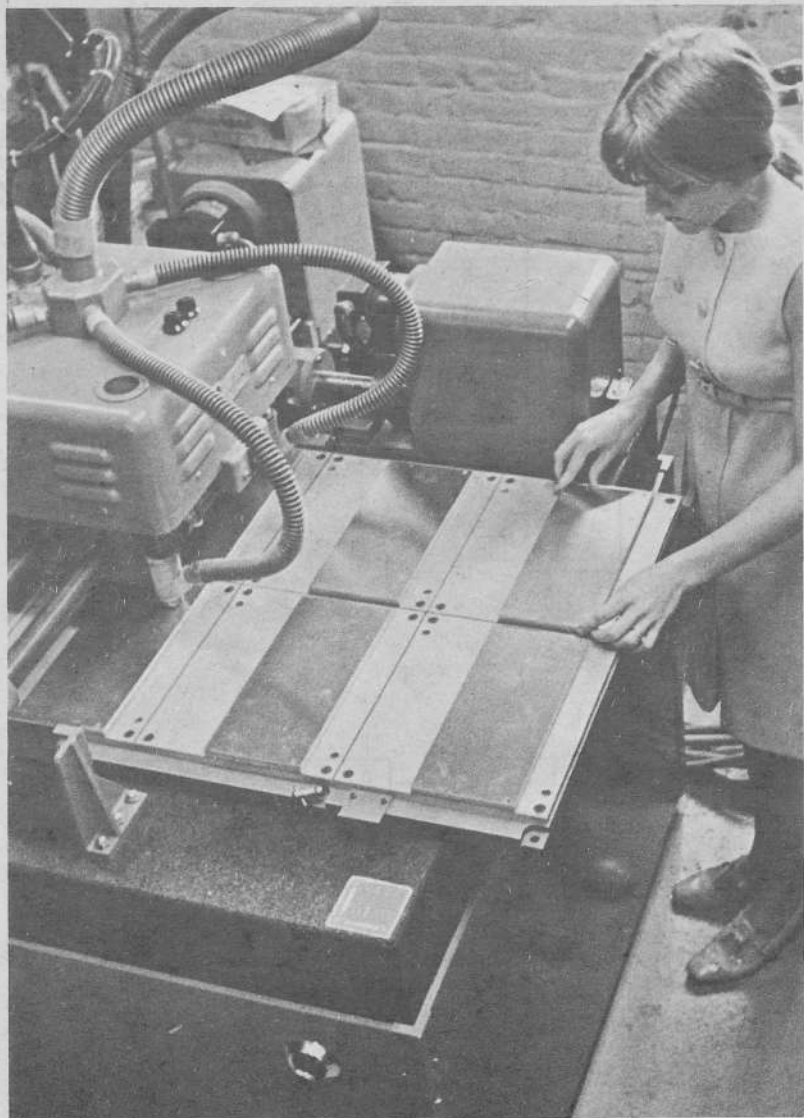


M502, M652



M506

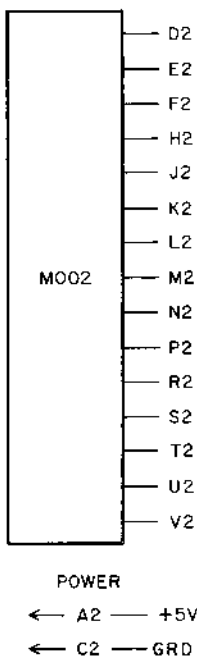




Twenty module boards are drilled simultaneously from a computer-generated coordinate tape. Other pantograph-controlled machines drill up to 200 boards simultaneously from a computer-generated template.

**LOGIC 1 SOURCE
M002**

**M
SERIES**



To hold unused M-Series TTL gate inputs high, the M002 provides 15 outputs at +3 Volts (Logic 1), on pins D2 through V2. Up to 10 unused M-Series gate inputs may be connected to any one output. If a M002 circuit is driven by a gate, it appears as two TTL unit loads or 3.2 mA. at ground.

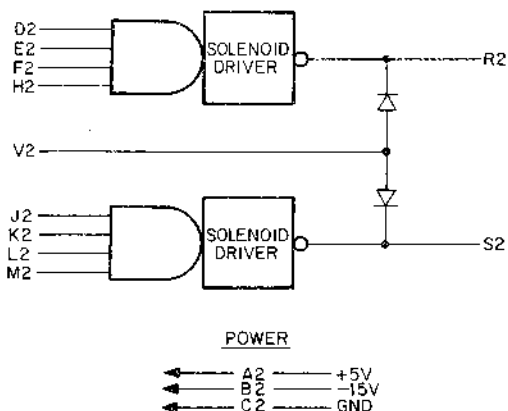
Power: +5 V at 16 mA. (max)

Size: Standard, single height, single width FLIP CHIP module.

M002 — \$10

SOLENOID DRIVER M040

M SERIES



M040 Solenoid Driver

These high current drivers can drive relays, solenoids, stepping motor windings, or other similar loads. The output levels are -2 Volts and a more negative voltage determined by an external power supply. One terminal of the load device should be connected to the external power source, the other to the driver output. There are two drivers per module.

Pin V2 of the driver module must be connected to the external supply so that the drivers will be protected from the back voltage generated by inductive loads. If the wire to the power supply is more than 3 feet long it may have to be by-passed at the module with an electrolytic capacitor to reduce the short over-shoot caused by the inductance of the wire. If pin V2 is connected to the supply through a resistor, the recovery time of inductive loads can be decreased at a sacrifice in maximum drive voltage capability. Maximum rated supply voltage less actual supply voltage should be divided by load current to find the maximum safe resistance. When both circuits on a module are used, the load current for the above calculation is the sum of the currents.

Inputs: Each input presents one unit load.

Outputs: The M040 has maximum ratings of -70 Volts and 0.6 amp. Typical delay for the circuit is 5 μ sec. No more than two circuits should be paralleled to drive loads beyond the current capabilities of single circuits.

Grounding: High current loads should be grounded at pin C2 of the M040. -15 Volts at 9 mA. (max)

Power: +5 Volts at 47 mA. (max)

The external voltage supply must provide the output current of the two drivers. (1.2 amps. max.)

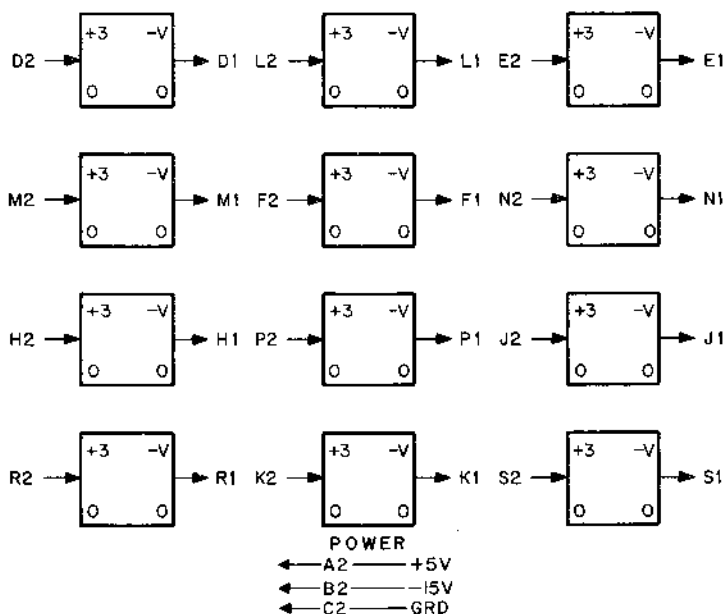
Size: Standard, single height, single width FLIP CHIP module.

Note:

Refer to K Series driver modules for increased current drive, increased voltage breakdown or AC current drive capability.

50 MA. INDICATOR DRIVER M050

M SERIES



M050 INDICATOR DRIVER

The M050 contains twelve transistor inverters that can drive miniature incandescent bulbs such as those on an indicator panel. It is used to provide drive current for a remote indicator, such as Drake 11-504, Diaico 39-28-375, or Digital Indicator type 4908, or level conversion to drive 4917 and 4918 indicator boards (See the Hardware Section.) A low level on the input of the driver causes current to flow in the output.

Inputs: Each input presents two unit loads.

Outputs: Each output is capable of driving 50 ma. into an external load connected to any voltage between ground and -30 Volts.

Power: +5 Volts at 47 mA. (max)
 -15 Volts at 16 mA. (max.)

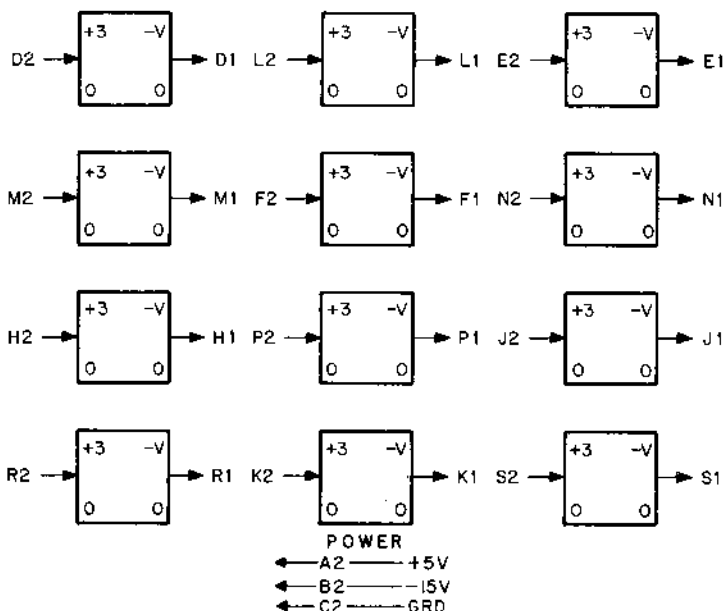
Size: Standard, single height, single width FLIP CHIP module.

Note: For those applications requiring the sinking of current, refer to K Series.

M050—\$31

**POSITIVE TO NEGATIVE LOGIC
LEVEL CONVERTER
M051**

**M
SERIES**



The M051 contains twelve level converters that can be used to shift M and K Series logic levels to negative logic levels of ground and -3 Volts. A grounded input on the driver causes the output to be grounded.

Inputs: Each input presents two TTL unit loads.

Outputs: The output consists of an open collector PNP transistor and can drive 20 mA. to ground —6V maximum may be applied to the output.

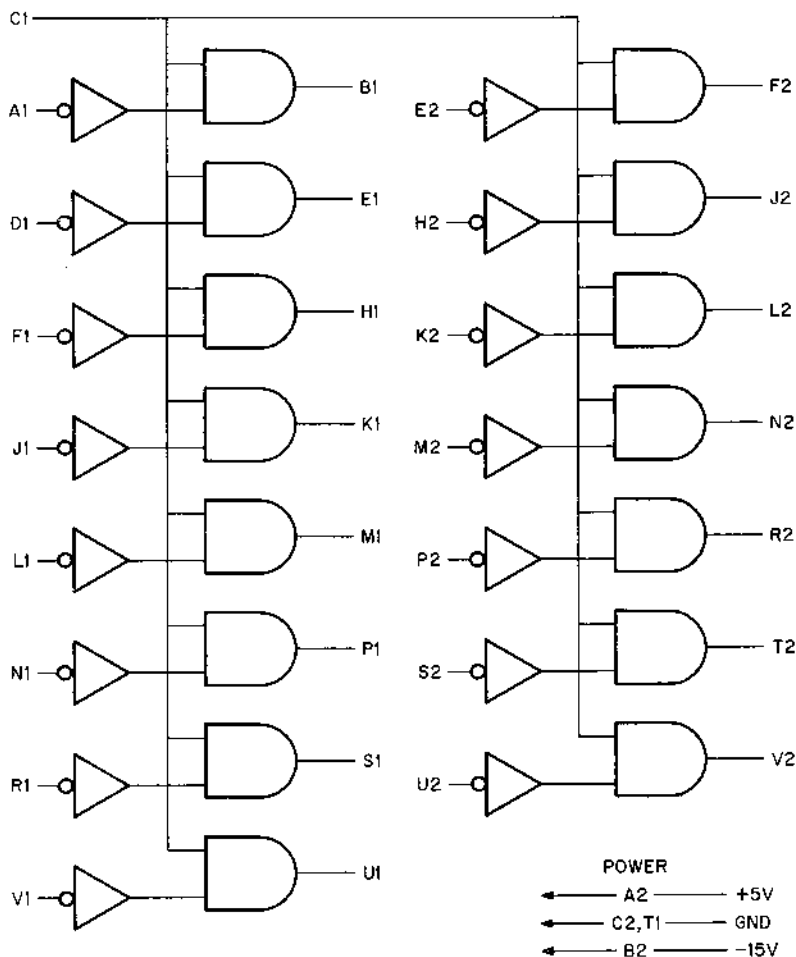
Power: +5V at 47 mA. (max.); -15V at 16 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

M051—\$31

BUS DATA INTERFACE M100

M SERIES



The M100 Bus Data Interface contains fifteen circuits for convenient reception of data from the PDP-8, PDP-8/I negative voltage bus. It is pin compatible with the M101 Positive Bus Data Interface.

The loading presented to the negative voltage bus differs from that loading using the standard negative bus modules (i.e., R107, R111) in that the data lines are loaded only if the appropriate device is selected. The option select output of the M102 must be connected to the strobe input pin, C1, of the M100.

The enabling line of the M100 cannot be used as a strobe line. The output signals are indeterminant for a period of 200 nsec after the enabling line has become true.

Inputs: All outputs will drive 10 TTL unit loads.

Conversion: Logic Diagram: An active voltage is a True State, i.e., -3 V or $+3\text{ V} = "1"$.

A ground is a True State.

A data input of -3 V will yield an output of $+3\text{ V}$ when C1 is gated by a positive voltage logic "1" of $+2.4\text{ Volts}$.

Threshold switching level: -1.5 V . typ.

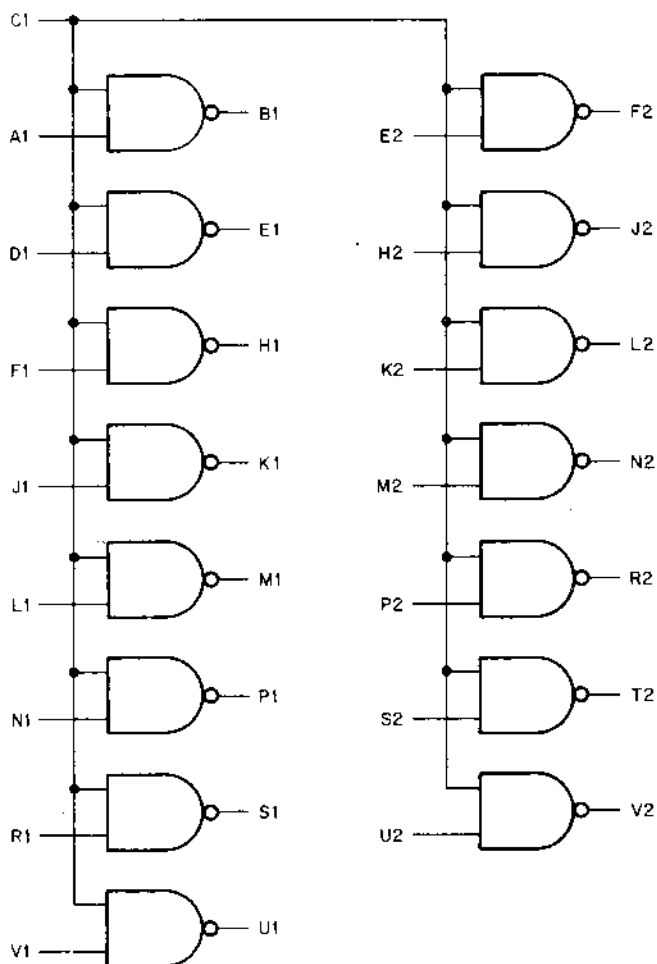
Propagation delay: 40 nsec typ.

Power: $\pm 5\text{ Volts}$ at 60 ma. (max.); -15 Volts at 10 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

BUS DATA INTERFACE M101

M SERIES



POWER

← A2 — +5V

← C2, T1 — GRD

The M101 contains fifteen, two-input NAND gates arranged for convenient data strobing off of the PDP8/I or PDP8/L positive bus. One input of each gate is tied to a common line so that all data signals on the second input of each gate can be enabled simultaneously. The M101 can also be used as inverters or a data multiplexer. All data inputs are protected from a negative of more than -0.8 Volts.

Inputs: Each data signal input presents one TTL unit load. The common line input presents fifteen unit loads.

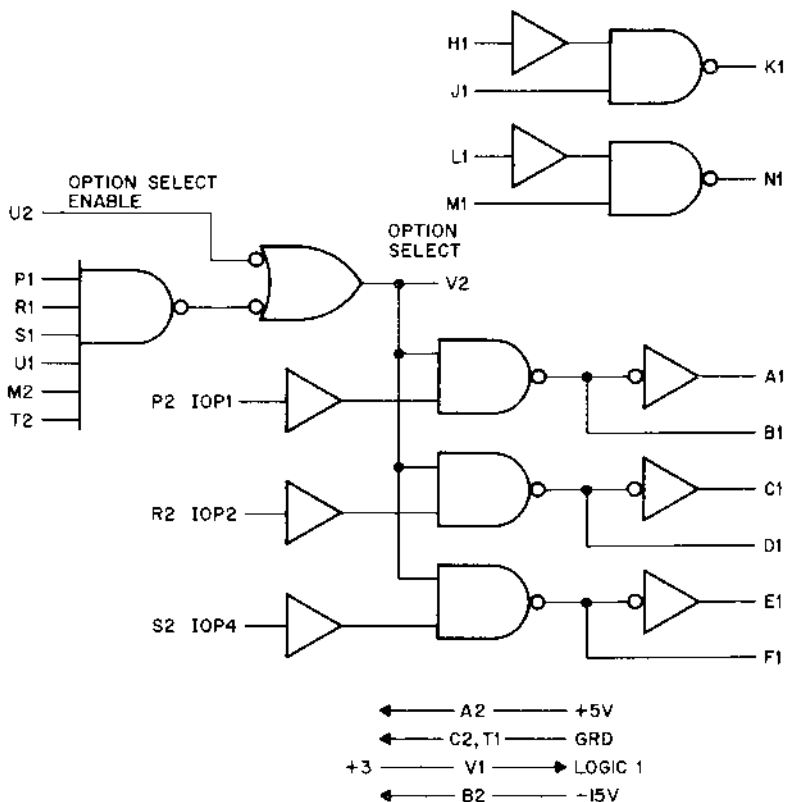
Outputs: Each output can drive ten unit loads.

Power: $+5V$ at 82 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

DEVICE SELECTOR M102

M SERIES



The M102 is used to decode the six device address bits transmitted in complementary pairs on the negative bus of the PDP-8, PDP-8/I. The outputs of the M102 are compatible with M Series TTL logic. The M102 is pin compatible with the M103 Positive bus device selector with the exception of the address inputs. The true state of the BMB outputs of the PDP-8 and PDP-8/I are defined as ground where the true states of the PDP-8/I positive bus and PDP-8/L are defined as an active voltage state. This fact requires that the complement of the address bits used for an M103 must be connected to the M102.

As the address complement is tied to the pins D2, E2, F2, H2, J2, K2, an M103 may be directly substituted for an M102 when changing from a negative to a positive bus.

Inputs: U2 represents 1.25 TTL unit loads, J1, M1 represents 1 TTL, P1, R1, S1, U1, M2 and T2 standard levels of -3Volts and ground. Input load is 1 mA. shared among the inputs that are at ground.

P2, R2, S2, H1 and L1

0.2 mA. when $V_{in} = 0V$

0.0 mA. when $V_{in} = -3V$

Propagation Delay 40 nsec typ.

Outputs: K1 and N1 can drive 10 TTL unit loads. A1, B1, C1, D1, E1, F1 can each drive 37 TTL unit loads. V2 can drive 16 TTL unit loads.

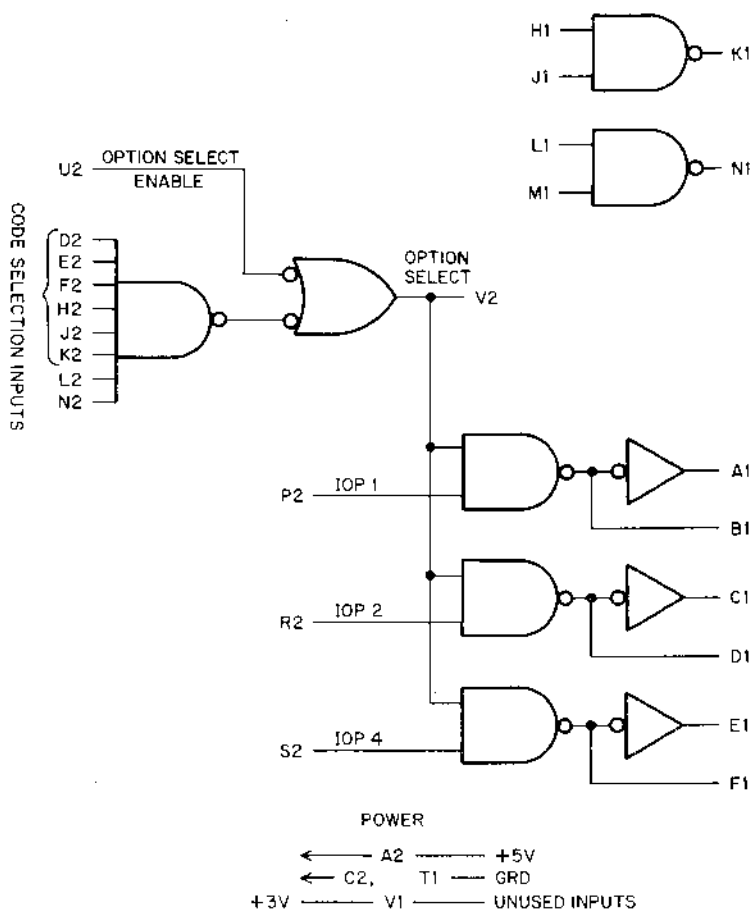
Conversion: Logic Diagram. An active voltage is a True State, i.e., -3V or +3V = "1". A ground is a False State.

Power: +5 Volts at 130 mA. (max.); -15 Volts at 40 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

DEVICE SELECTOR M103

M SERIES



The M103 is used to decode the six device bits transmitted in complement pairs on the positive bus of the PDP8/I and PDP8/L. Selection codes are obtained by selective wiring of the bus signals to the code select inputs D2, E2, F2, H2, J2, and K2. This module also includes pulse buffering gates for the IOP signals found on the positive bus of the above computers. Two two-input NAND gates are also provided for any additional buffering that is required.

Inputs: All inputs which receive positive bus signals are protected from negative voltage undershoot of more than $-0.8V$.

The following inputs each present one TTL unit load D2, E2, F2, H2, J2, K2 H1, J1, L1, and M1. Inputs P2, R2, and S2 present 2.5 TTL unit loads. Inputs U2, L2 and N2 each present 1.25 unit loads. These inputs need not be tied to a source of logic 1 when not used.

Outputs: Gate outputs K1 and N1 can each drive ten TTL unit loads.

Pulse buffering outputs A1, B1, C1, D1, E1 and F1 can each drive 37 TTL unit loads.

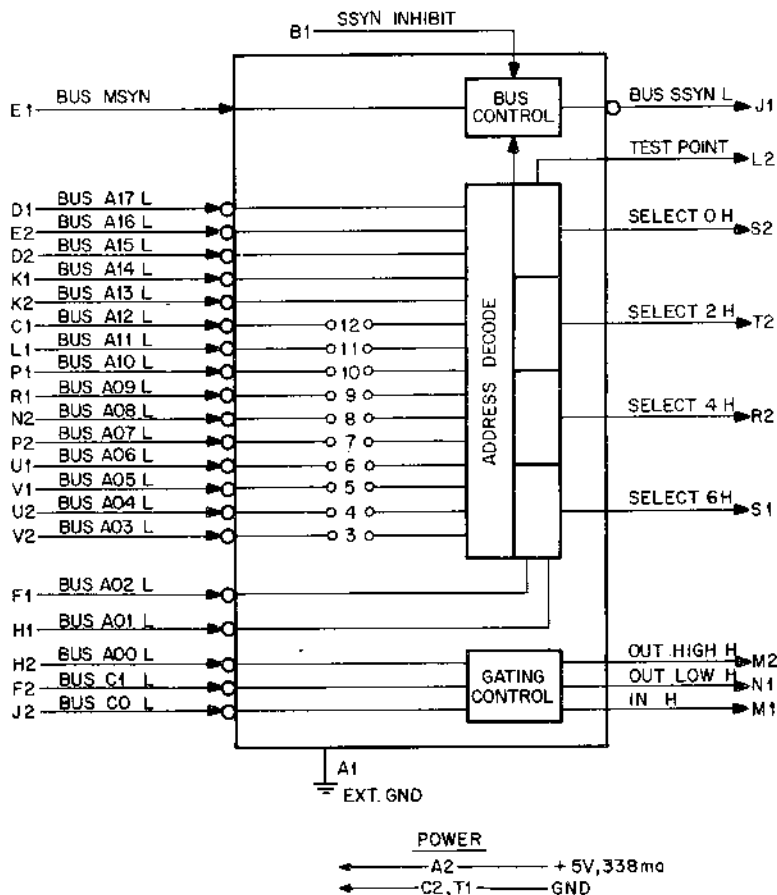
The Option Select output can drive 16 TTL unit loads.

Power: +5Volts at 110 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

ADDRESS SELECTOR M105

M SERIES



The M105 is used in PDP-11 device interfaces to control the flow of data between the device registers and the UNIBUS. It provides gating signals for up to four device registers that indicate a register is being referenced and three control signals that indicate the path for data flow.

The selector decodes the 18-bit address $A \langle 17:00 \rangle$ as follows: $A \langle 17:13 \rangle$ defines the memory "page" assigned to peripheral devices (external bank) and must all be asserted. $A \langle 12:03 \rangle$ is determined by jumpers on the card.

When the jumper is "in" the selector will look for a zero on that address line. A02 and A01 provide a coding array for the four SELECTED addresses. A00 is for byte control.

Signals for gating control are determined by decoding A00, C1, and C0. The signals obtained are: IN, OUT LOW, and OUT HIGH.

$$\begin{aligned} \text{IN} &= \text{DATI} + \text{DATIP} \\ \text{OUT LOW} &= \text{DATO} + (\text{DATOB} \cdot \overline{\text{A00}}) \\ \text{OUT HIGH} &= \text{DATO} + (\text{DATOB} \cdot \text{A00}) \end{aligned}$$

IN is used to gate data from a device register onto the bus. OUT LOW is used to gate D <07:00> into the low byte of a device register. OUT HIGH is used to gate D <15:08> into the high byte of a device register.

In relation to bus control, the M105 is actually the "slave" in the relationship when data transfer occurs on the Unibus.

SSYN is asserted whenever it sees its address being referenced and MSYN is asserted. SSYN is negated when MSYN is negated. There is an approximate 100 nsec. delay between receiving MSYN and the assertion of SSYN to allow for decoding.

Input Loading:	One UNIBUS receiver load* (each)	BUS A <17:00> BUS C <1:0 > BUS MSYN
	−8.2 mA (max.)	SSYN INHIBIT
	−66 mA (max.)	EXT GND
	*A UNIBUS receiver is characterized at:	
	<1.4V at 25µA (max.)	LOW LEVEL
	>2.5V at 160µA (max.)	HIGH LEVEL
Output Drive:	Ten TTL units loads (each)	SELECT 0,2,4,6 OUT HIGH, LOW
	Eight TTL unit loads	IN
	One Unibus driver load*	BUS SSYN
	*A UNIBUS driver load is characterized at:	
	<0.8V at 50mA (max.)	LOW LEVEL
	25µA (max.)	Open collector leakage

Power: +5 Volts at 338 mA (max.)
EXT GND is used for testing purposes and should be tied to ground in normal operation.

SSYN INHIBIT can be left open when not used.

Size: Extended length, single height, single width FLIP CHIP module.

DEVICE SELECTOR M107

M SERIES

The M107 is a device selector which, by the use of extended decoding of the BMB lines 9 through 11, will provide seven discrete IOT pulses. Five additional IOT pulse outputs are provided to allow the user to reduce software requirements by the combining of IOT codes. The IOT instruction and the IOP times at which the various IOT pulses occur at the module pins are outlined in the following chart:

Module Pin	IOT	AT IOP TIME		
		1	2	4
BH2	1 - 1	X		
BM2	2 - 2		X	
BJ2	3 - 1	X		
BN2	3 - 2		X	
BS2	4 - 4			X
BK2	5 - 1	X		
BT2	5 - 4			X
BP2	6 - 2		X	
BU2	6 - 4			X
BL2	7 - 1	X		
BR2	7 - 2		X	
BV2	7 - 4			X

Example: If an IOP-7 is issued, IOT pulses will exist only at output pins BL2 (7-1), BR2 (7-2) and BV2 (7-4). IOT pulses will not exist at any other output pin.

The M107 also contains two flag flip-flops which may be directly cleared or set. The outputs of the flag flip-flops are connected to the skip and program interrupt lines. Interrogation of the flags is accomplished by IOT 1 - 1 for flag 1 and IOT 2 - 2 for flag 2.

The M107 also provides two inputs to accomplish the "clear the accumulator" function.

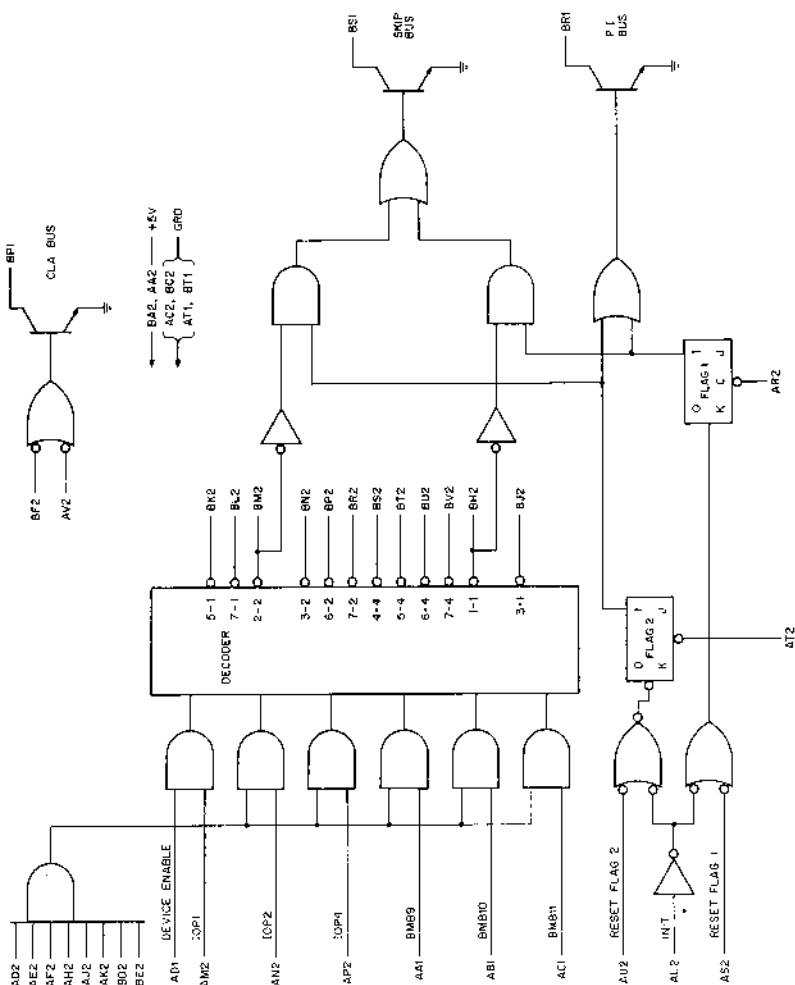
INPUTS: Pins — AD2, AE2, AF2, AH2,
AJ2, AK2, AA1, AB1,
AC1, AL2, AV2, BF2,
Present one TTL load
Pins — BD2, BE2, AM2, AN2,
AP2, AU2, AS2
Present 1.25 TTL load.
Pins — AR2, AT2 resent 2 TTL loads.

Outputs: Option Select Pin AD1 can drive 13 TTL loads. Bus driver outputs pins BP1, BS1, and BR1 are open collector NPN transistors and can sink 30 ma. at ground. The maximum voltage applied to these outputs must not exceed +20 Volts and each output is diode protected against negative under-shoot in excess of -0.9Volts.

All other outputs will drive up to 35 TTL loads.

Power: +5Vat 245 mA. (maximum).

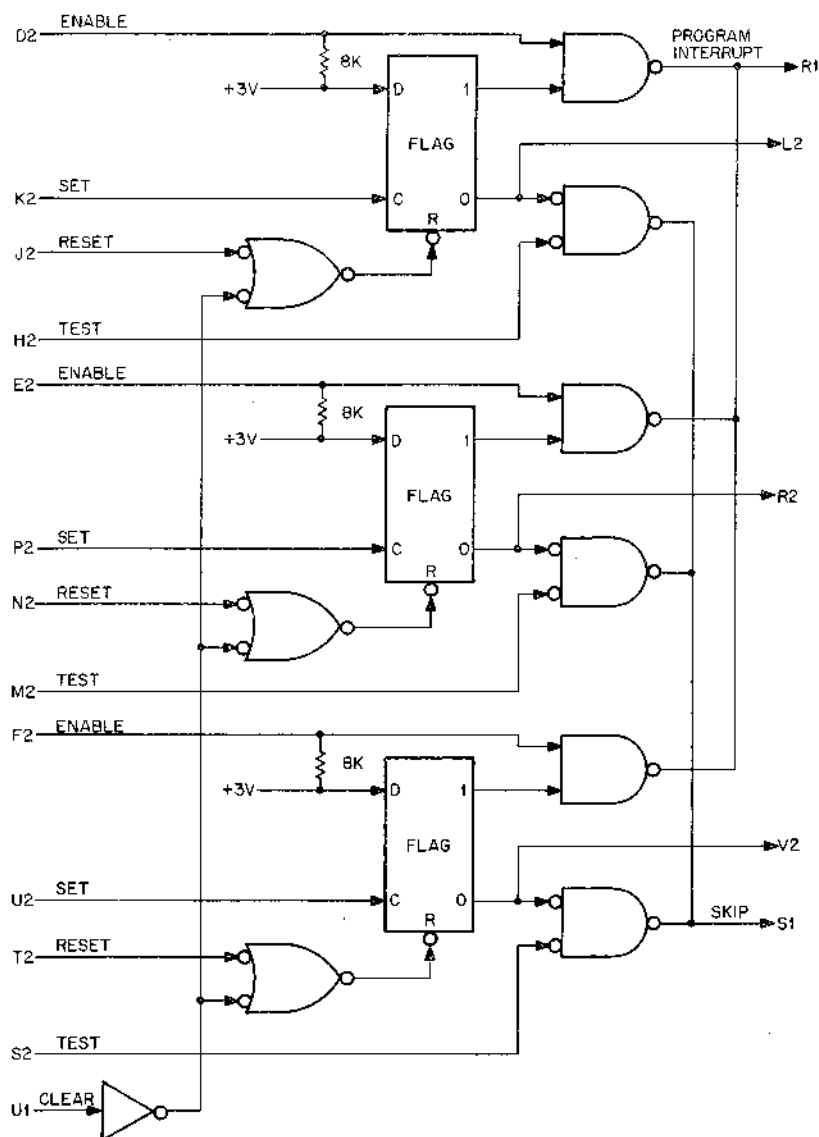
Size: Standard, double height, single width FLIP CHIP module.



M107 — \$105

FLAG MODULE M108

M SERIES



The M108 is a single height module and contains three flag flip-flops. Each flag flip-flop may be independently cleared or all flip-flops may be cleared simultaneously.

The output of each flag flip-flop is gateable and are open collector "OR"ed to the Program Interrupt bus.

The output of each flag flip-flop is passed through a gate and open collector to the skip bus. This facility allows the user to test for a flag.

The "0" side of each flip-flop has been extended to module pins for peripheral control.

Each flip-flop may be independently set by the application of the leading (positive going voltage) edge of a pulse or level to the clock inputs.

If use of the Program Interrupt feature is not desired, the ENABLE inputs (D2, E2, F2) must be connected to ground. If Program Interrupt is desired, no connections to the ENABLE inputs are required.

Inputs: K2, P2, U2, present 2 TTL loads. D2, E2, F2 present 1.25 TTL loads. All other inputs present 1 TTL load.

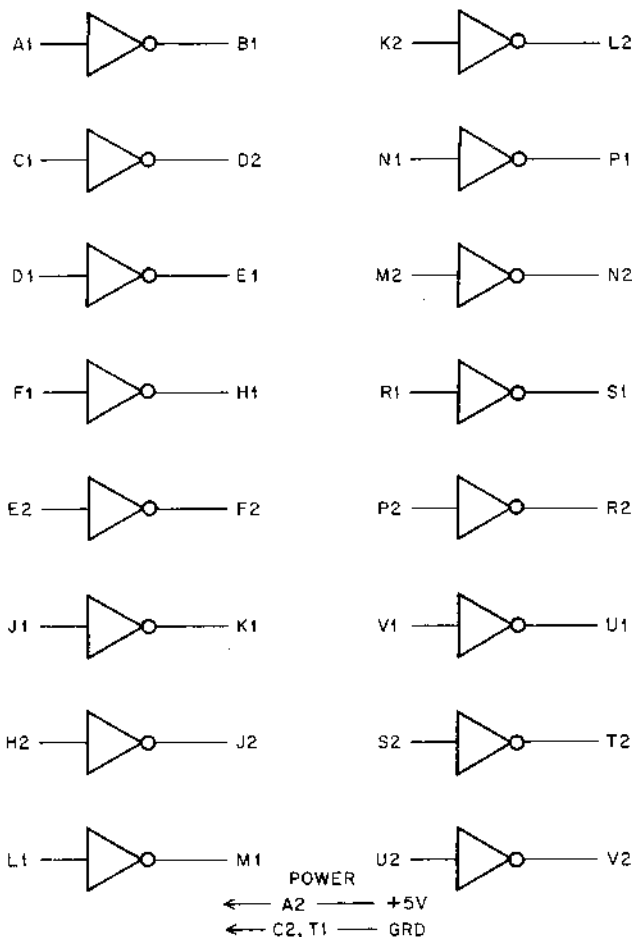
Outputs: L2, R2, V2 supply 9 TTL loads. R1 (P. I. Function) and S1 (Skip Function) are open collector NPN Transistors and will sink 100mA to ground. The voltage applied to these outputs must not exceed +20 Volts.

Power: +5 Volts at 137 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

INVERTER M111

M SERIES



Sixteen Inverters with input/output connections as shown.

Input: Each input presents one unit load.

Output: Each output can drive up to ten unit loads.

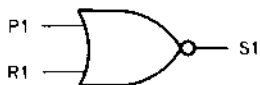
Power: +5Volts, 87 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

M111 — \$22

NOR GATE M112

M SERIES



POWER

← A2 → +5V

← C2, T1 → GRD

+3V ← U1, V1 → UNUSED INPUTS

The M112 contains ten positive NOR gates, each performing the function $A + B$. Pins U1 and V1 provide +3 Volts, each capable of holding High (Logic 1) up to 40 unused M-Series inputs.

Input: Each input presents one unit load.

Output: Each output can drive up to ten unit loads.

Power: +5V at 50 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

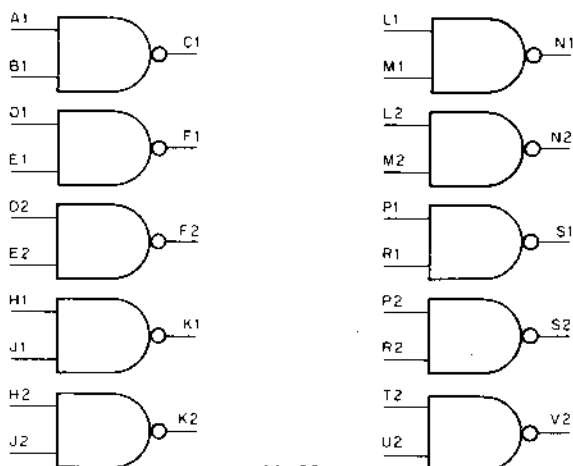
M112 — \$35

NAND GATES

M113, M115, M117, M119

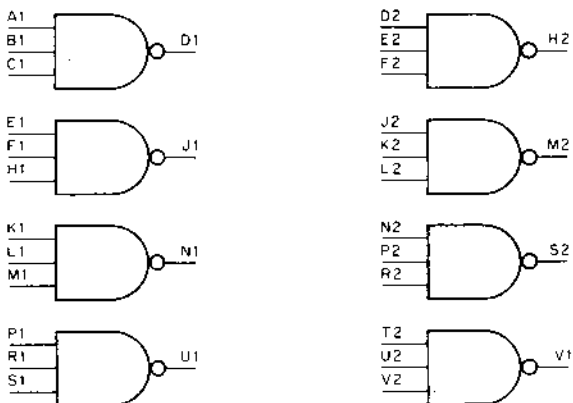
M

SERIES



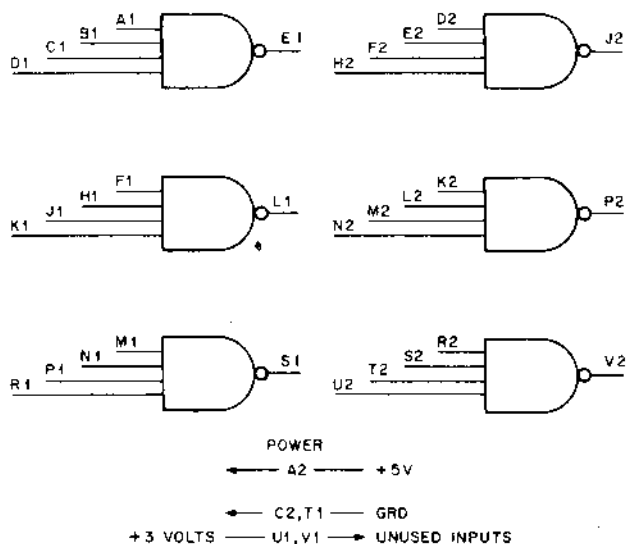
POWER:
 ← A2 ——— +5V
 ● C2, T1 — GRD
 +3V → U1, V1 → UNUSED INPUTS

M113 2-INPUT NAND GATES

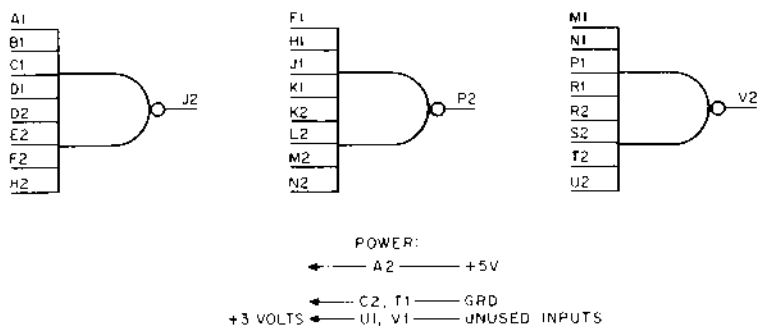


POWER
 ← A2 ——— +5V
 ● C2, T1 — GRD

M115 3-INPUT NAND GATES



M117 4-INPUT NAND GATES



M119 8-INPUT NAND GATES

These modules provide general-purpose gating for the M Series, and are most commonly used for decoding, comparison, and control. Each module performs the NAND function $A \cdot B \cdot \dots \cdot N$, depending upon the number of inputs.

M113—Ten, two-input NAND gates that also may be used as inverters.

M115—Eight, three-input NAND gates.

M117—Six, four-input NAND gates.

M119—Three, eight-input NAND gates.

Unused inputs on any gate must be returned to a source of logic 1, for maximum noise immunity. In the M113, M117, M119, M121, M617 and M627 modules, two pins are provided (U1 and V1) as source of +3 volts for this purpose. Each pin can supply up to 40 unit loads.

M103, M111 and M002 provide additional sources of logic 1 level.

Typical propagation delay of M Series gates is 15 nsec.

Inputs: Each input presents one unit load.

Outputs: Each output is capable of supplying 10 unit loads.

Power:

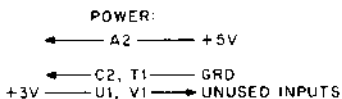
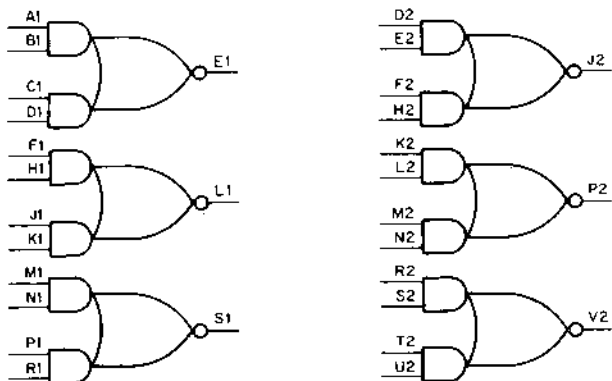
M113:	71 mA.	} +Max. current at 5 Volts.
M115:	41 mA.	
M117:	41 mA.	
M119:	19 mA.	

Size: Standard, single height, single width FLIP CHIP module.

M113	— \$18
M115	— \$18
M117	— \$19
M119	— \$18

AND/NOR GATE M121

M SERIES



M121 AND/NOR GATES

The M121 module contains six AND/NOR gates which perform the function $AB + CD$. By proper connection of signals to the AND inputs, the exclusive OR, coincidence, and NOR functions can be performed.

Typical propagation delay of an M121 gate is 15 nsec.

Inputs: Each input presents one unit load to the driving module.

Outputs: Each output is capable of driving up to 10 unit loads.

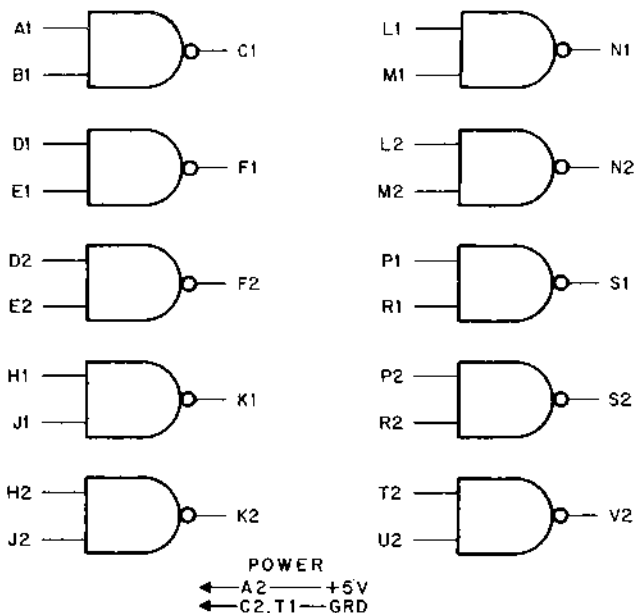
Power: +5Volts at 50 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

M121 — \$23

INPUT NAND GATES M133

M SERIES



This module provides general purpose high speed gating for the M-Series. Maximum output propagation delay to a logic 1 or 0 is 10 nsec. The high speed characteristic of these gates frequently will solve tight timing problems in complex systems. Unused inputs on any gate must be returned to a source of logic 1 for maximum speed and noise immunity.

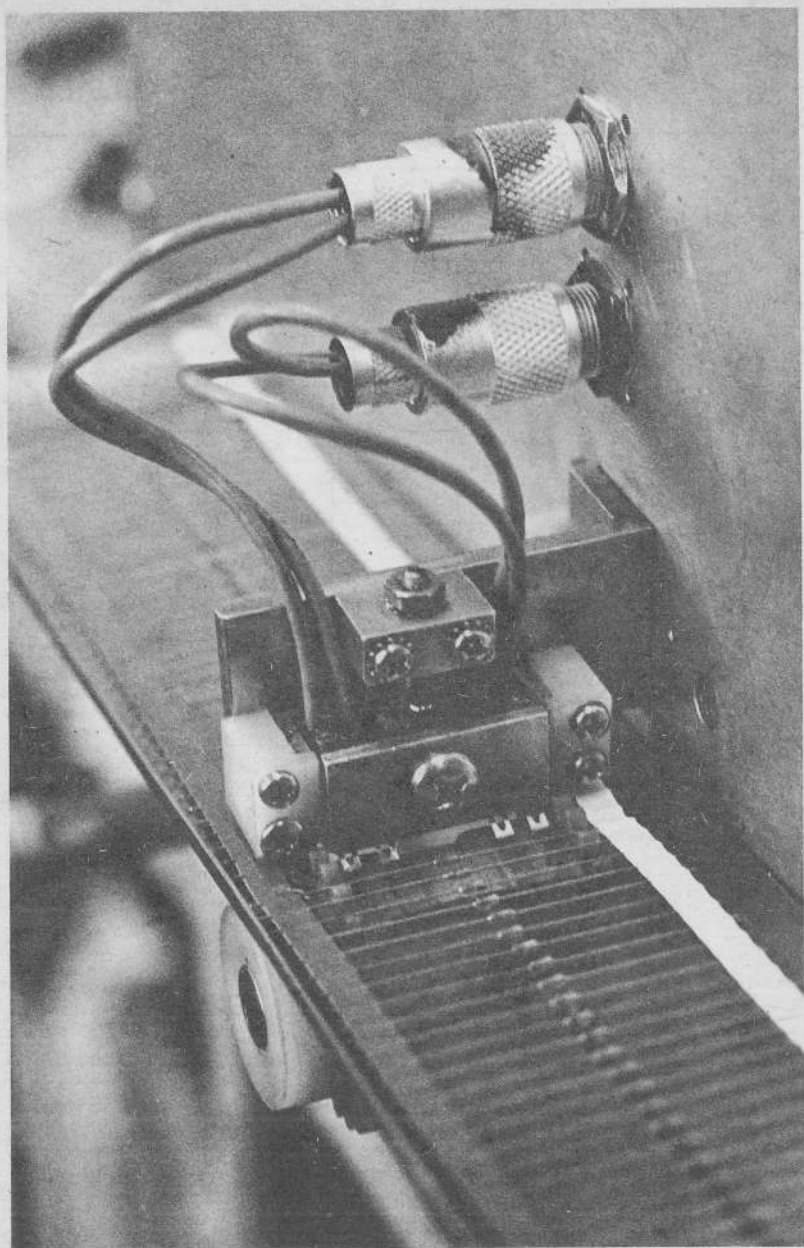
Inputs: Each input presents 1.25 unit loads.

Outputs: Each output is capable of driving 12.5 unit loads.

Power: +5V at 160 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

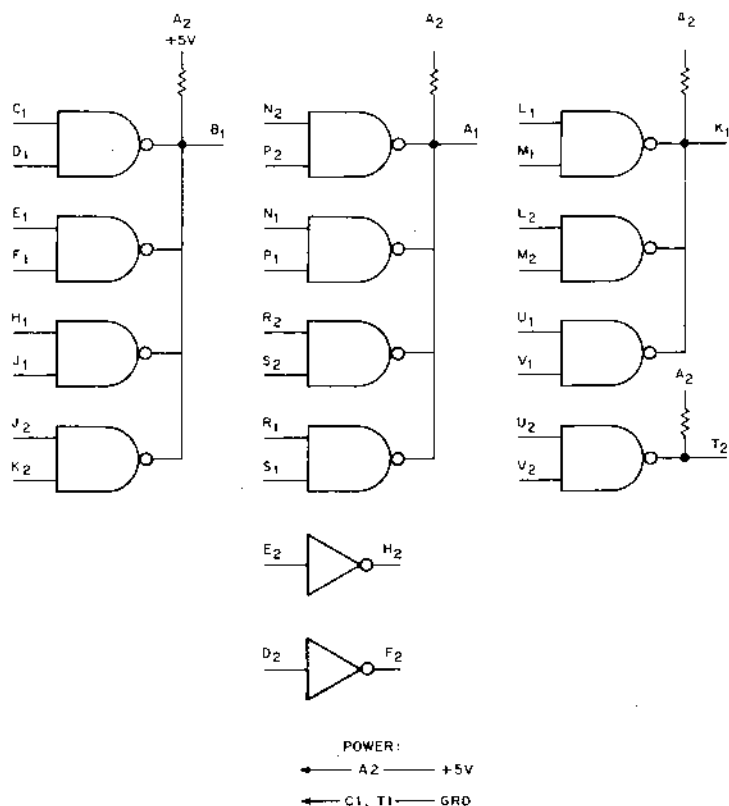
M133 — \$27



All incoming components are 100% tested. Here, diodes are being tested automatically.

NAND/OR GATES M141

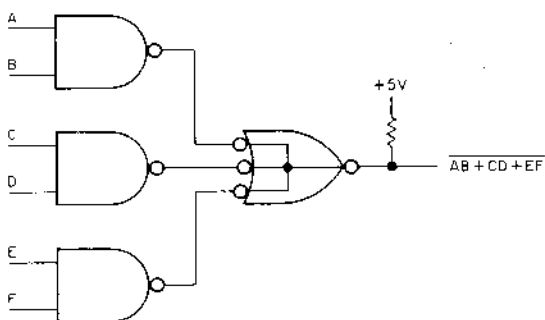
M SERIES



M141 NAND/OR GATE

The M141 NAND/OR gate performs two levels of logic. The first is the NAND function which is identical to the M113 NAND gate. The second level is that of a wired OR for low logic levels. The two input NAND gate which is used in the M141 does not have the standard TTL output circuit, but only the lower half of the totem pole output. This allows the outputs of these gates to be connected together and to share a common pull-up resistor. Propagation delay through these gates is a maximum of 70 nsec.

The NAND/OR gates are arranged in four groups consisting of 4, 4, 3, and 1 two input NAND gates respectively. The outputs in each group are connected together which provide a wired OR for low levels. The function of these gates can be shown as:



By using one of the two inverters provided, a true AND/OR function can be realized. A maximum of four groups of gates can be connected together. Connection is made by merely connecting output pins together.

Inputs: Each input presents one unit load.

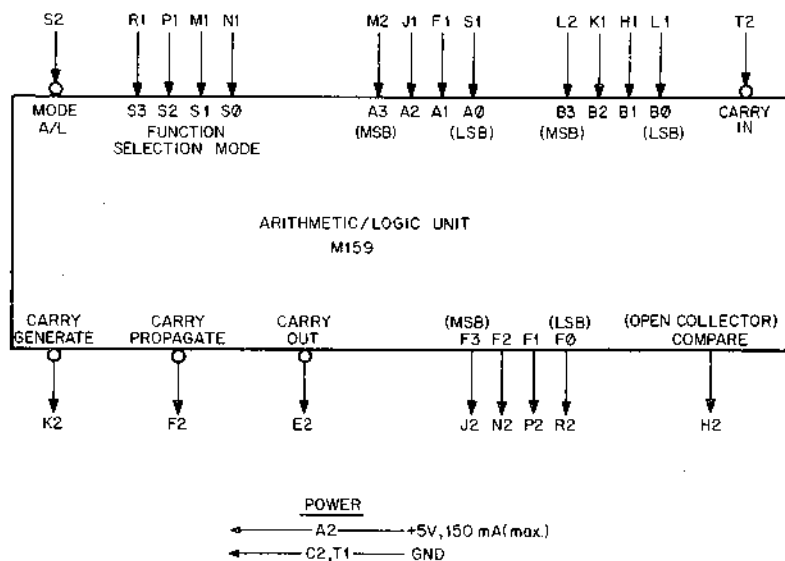
Outputs: Four gate outputs, each capable of driving 7 unit loads. The load resistor of each output presents 2 unit loads when connected to another output. For example, four groups are connected together, therefore 3 groups present two unit loads each to the fourth group, totalling 6 unit loads. This leaves 1 unit load capability. Each inverter output is capable of driving up to 10 unit loads.

Power: +5 Volts at 117 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

ARITHMETIC/LOGIC UNIT M159

M SERIES



The M159 can perform 16 word-oriented arithmetic operations and 16 bit oriented logic functions. Arithmetic operations are performed on two 4-bit input words and an input carry to produce one 4-bit output word and a carry out. In the logic mode the M159 looks like four 2-input functional gates. Where N indicates one out of four, the output F_N depends only on the inputs A_n, B_n , and the logic function code selected.

The M159 is fully cascadable. The CARRY OUT of the less significant M159 should be connected directly to the CARRY IN of the next more significant M159. The CARRY PROPAGATE and CARRY GENERATE output should be used with a carry look-ahead module or left unconnected.

The COMPARE output goes High whenever all the "F" outputs go High. This output is open-collector so that it can be wire-AND connected when M159 modules are cascaded. An example of how this output can be used is shown in the table below.

When the arithmetic operation A minus B minus 1 is selected, the M159 can be used as a comparator.

A and B Data Inputs	COMPARE Output	CARRY OUT
A > B	0	0
A = B	1	1
A < B	0	1

The maximum propagation delay from the "A_N" or "B_N" bit input to the output bit "F_N" in the logic mode is 48 nsec. which does not change as M159's are cascaded. In the arithmetic mode, the maximum delay from the "A" or "B" word input to the "F" word output, CARRY OUT, or COMPARE is 50 nsec. which increases by 19 nsec. per additional cascaded M159 when carry look-ahead is not used. When carry look-ahead is used, the maximum additional delay is limited to 20 nsec. for up to three additional M159's.

Table of Logic Mode Operations

(MODE Input = 1)

(CARRY IN has no effect on Logic Mode Operations)

Function				NOTE that F _N is complemented when the Function Selection Code is complemented		Complemented Function			
SELECTION CODE				Bit F _N Equals	Bit F _N Equals	SELECTION CODE			
S3	S2	S1	S0	Bit F _N Equals	Bit F _N Equals	S3	S2	S1	S0
0	0	0	0	\bar{A}_N	A _N	1	1	1	1
0	0	0	1	\bar{A}_N AND \bar{B}_N	A _N OR B _N	1	1	1	0
0	0	1	0	\bar{A}_N AND B _N	A _N OR \bar{B}_N	1	1	0	1
0	0	1	1	0	1	1	1	0	0
0	1	0	0	\bar{A}_N OR \bar{B}_N	A _N AND B _N	1	0	1	1
0	1	0	1	\bar{B}_N	B _N	1	0	1	0
0	1	1	0	(A _N AND \bar{B}_N) OR (\bar{A}_N AND B _N)	(A _N AND B _N) OR (\bar{A}_N AND \bar{B}_N)	1	0	0	1
0	1	1	1	A _N AND \bar{B}_N	\bar{A}_N OR B _N	1	0	0	0

Inputs: MODE A/L input presents 1 TTL unit load.
 Each A or B bit input presents 3 TTL unit loads.
 Each FUNCTION SELECT input presents 4 TTL unit loads.
 CARRY IN input presents 5 TTL unit loads.

Outputs: Each output is capable of driving 10 TTL unit loads.

Power: +5V at 150 mA (max.)

Size: Standard, double height, single width FLIP CHIP module.

Table of Less Useful Arithmetic Mode Operations

(MODE Input = 0)

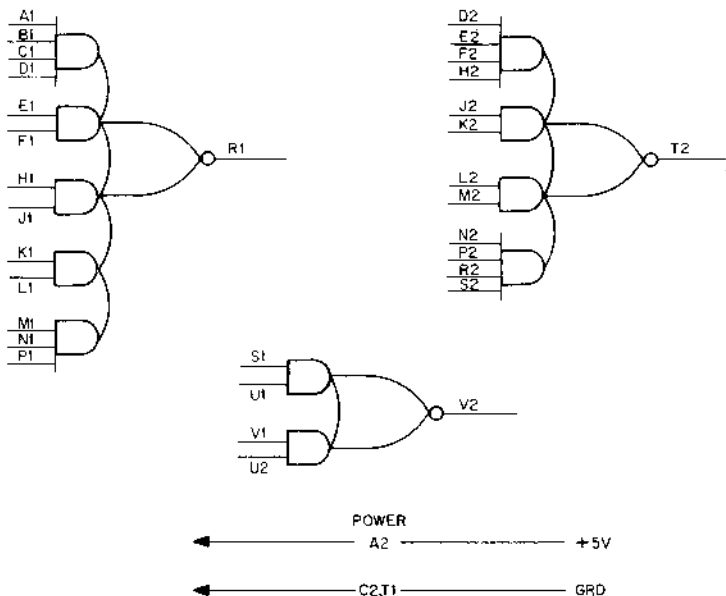
Function				Word F Equals	
SELECTION CODE				CARRY IN = 1	CARRY IN = 0
S3	S2	S1	S0		
0	0	0	0		
0	0	0	1	A OR B	A OR B plus 1
0	0	1	0	A OR \bar{B}	A OR \bar{B} plus 1
0	0	1	1		
0	1	0	0	A plus (A AND \bar{B})	A plus (A AND B) plus 1
0	1	0	1	(A OR B) plus (A AND \bar{B})	(A OR B) plus (A AND B) plus 1
0	1	1	0		
0	1	1	1	(A AND \bar{B}) minus 1	A AND B
1	0	0	0	A plus (A AND B)	A plus (A AND B) plus 1
1	0	0	1		
1	0	1	0	(A OR \bar{B}) plus (A AND B)	(A OR B) plus (A AND B) plus 1
1	0	1	1	(A AND B) minus 1	A AND B
1	1	0	0		
1	1	0	1	(A OR B) plus A	(A OR B) plus A plus 1
1	1	1	0	(A OR \bar{B}) plus A	(A OR B) plus A plus 1
1	1	1	1		

**Table of Most Useful Arithmetic Mode Operations
(MODE Input =0)**

Function				Word F Equals	
SELECTION CODE				CARRY IN = 1	CARRY IN = 0
S3	S2	S1	S0		
0	0	0	0	WORD A	WORD A plus 1
0	0	0	1		
0	0	1	0		
0	0	1	1	Minus 1 (2's Comp.)	ZERO
0	1	0	0		
0	1	0	1		
0	1	1	0	A Minus B Minus 1	A Minus B
0	1	1	1		
1	0	0	0		
1	0	0	1	A plus B	A plus B plus 1
1	0	1	0		
1	0	1	1		
1	1	0	0	A Times 2	A Times 2 plus 1
1	1	0	1		
1	1	1	0		
1	1	1	1	A Minus 1	A

AND/NOR GATE M160

M SERIES



M160 AND/NOR GATES

The M160 module contains three general purpose AND/NOR gates which perform functions similar to the M121. By connecting signals to the AND inputs, these gates can be used to select and place on a single output any of several input signals.

Typical propagation delay of an M160 gate is 20 nsec.

Inputs: Each input presents one unit load

Outputs: Each output is capable of driving 10 unit loads

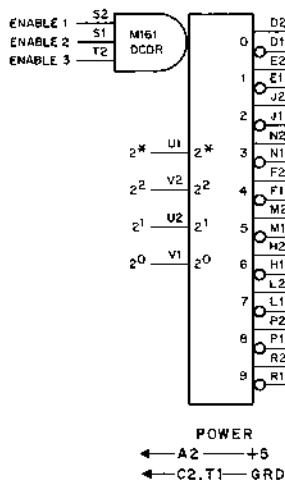
Power: 5 Volts at 30 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

M160 — \$33

BINARY TO OCTAL/DECIMAL DECODER M161

M SERIES



M161 BINARY TO OCTAL/DECIMAL DECODER

The M161 is a functional decoding module which can be used as a binary-to-octal or binary-coded decimal (8421 or 2421 codes) to decimal decoder. In the binary-to-octal configuration, up to eight M161's can be linked together to provide decoding of up to six bits. Three ENABLE inputs are provided for selective enabling of modules in decoders of more than one digit. In the octal mode, the bit 2^* input is connected to ground, which automatically inhibits the 8 and 9 outputs. Connections for a 5-bit binary/octal decoder (4 modules) are shown below. The figure assumes that the inputs to the decoder are the outputs of flip-flops such as FF2^o (1), 1 output side; and FF2^o (0), 0 output side.

The 2^* input may be of decimal value 2, 4, 6, 8 as long as illegal combinations are inhibited before connections to the inputs, and the 4-2-1 part of the code is in binary.

The propagation delay through the decoder is typically 55 nsec in the binary-to-octal mode, and 75 nsec in the BCD-to-decimal mode. The maximum delay in the BCD-to-decimal mode is 120 nsec, frequency-limiting this module to 8MHz when used in this fashion. The enable inputs can be used to strobe output data providing inputs 2^* — 2^0 have settled at least 50 nsec prior to the input pulse.

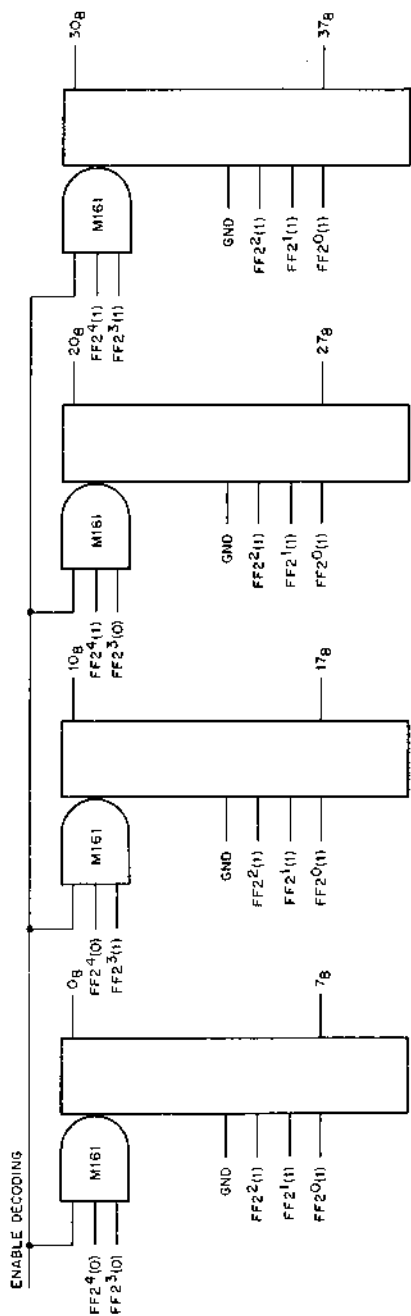
Inputs: 2^0 through 2^* , 1 unit load each; ENABLE 1 through ENABLE 3, 2 unit loads each.

Outputs: Each positive output is capable of driving 10 unit loads, and each negative output, 9 unit loads.

Power: 5 Volts at 120 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

M161 — \$55

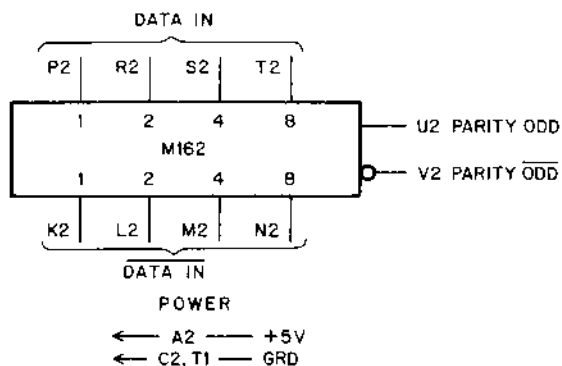
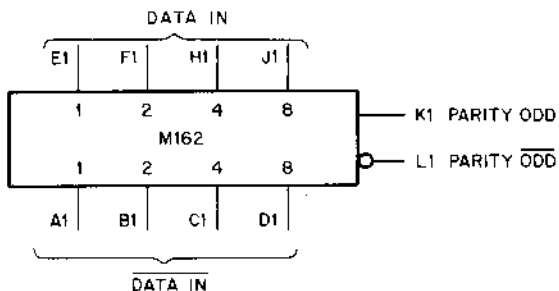


5-BIT BINARY/OCTAL DECODER
 (OUTPUTS ARE REPRESENTED IN
 OCTAL 37₈ = 31₁₀)

5-BIT BINARY/OCTAL DECODER

PARITY CIRCUIT M162

M SERIES



The M162 is a parity detector and contains two Parity Circuits. Each circuit indicates whether the Binary Data presented to it contains an ODD or EVEN number of ONES. The DATA and its complement are required as shown.

Indication of ODD PARITY is given by a High level of pins K1 and U2 respectively. Pins L1 and V2, when High, indicate EVEN PARITY or no input.

Input: Each input presents four unit loads.

Output: Pins L1 and V2 can each supply up to ten unit loads. Pin K1 and U2 can each supply up to six unit loads.

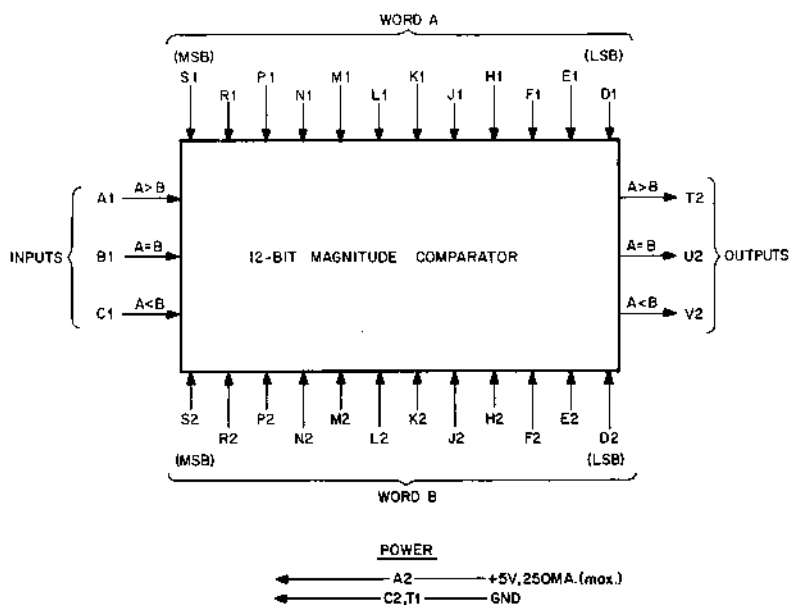
Power: +5 Volts at 102 mA. (max.)

Size: Standard, double height, single width FLIP CHIP module.

M162 — \$63

12-BIT MAGNITUDE COMPARATOR M168

M SERIES



INPUTS				OUTPUTS		
A > B	A = B	A < B	Data	A > B	A = B	A < B
1	0	0	A > B	1	0	0
1	0	0	A = B	1	0	0
1	0	0	A < B	1	0	0
1 or 0	1	1 or 0	A > B	1	0	0
1 or 0	1	1 or 0	A = B	0	1	0
1 or 0	1	1 or 0	A < B	0	0	1
0	0	1	A > B	0	0	1
0	0	1	A = B	0	0	1
0	0	1	A < B	0	0	1

The M168 12-Bit Magnitude Comparator performs magnitude comparison of two 12-bit words. When the comparison inputs are not connected to the comparison outputs of another M168, the "A=B" input must be connected to a logical "1". The A>B and A<B inputs may individually be made a logic "1" or logic "0". However, connecting both these inputs to GND, a logic "0" is recommended.

The M168 Comparator may be cascaded to compare longer words. The outputs T2, U2, and V2 should be connected to the corresponding inputs of the next comparator which are A1, B1, and C1 respectively. The inputs of the first comparator must all be made a logical "1".

The propagation delay time from Data (A and B) to outputs is 48 nsec typical and 72 nsec maximum for one unit.

When cascading the total typical time is 48 nsec plus 36 nsec per additional unit. The total maximum time is 72 nsec plus 54 nsec per additional unit.

Inputs: A > B and A < B (A1 and C1) each present 1 unit load.
A = B, Word A, and Word B inputs each present 3 unit loads.

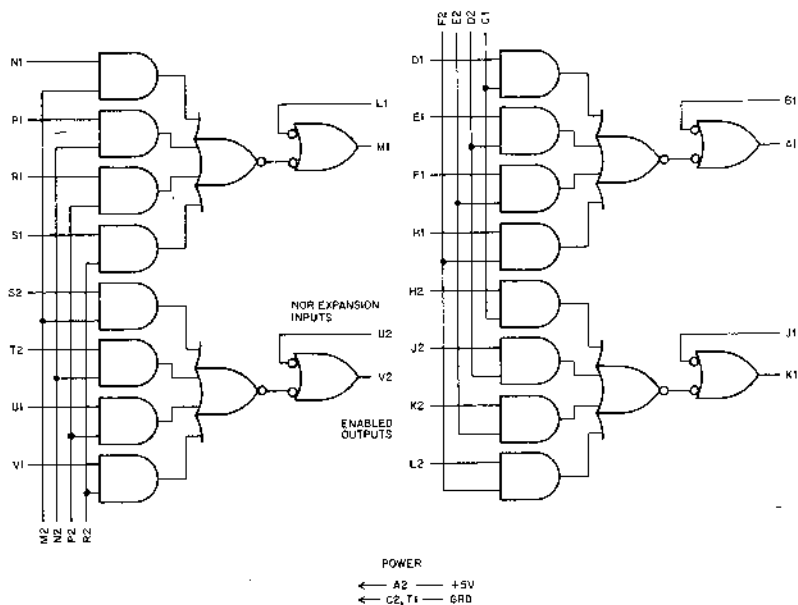
Outputs: Each output can drive 10 unit loads.

Power: +5 Volts, 250 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

GATING MODULE M169

M SERIES



M169 GATING MODULE

The M169 provides a general gating function, and may be used as a four-output multiplexer. Raising High a DATA INPUT and selecting a corresponding INPUT ENABLE line, generates a High at the appropriate ENABLED OUTPUT, A1, K1, M1 or V2. Any of the ENABLED OUTPUTS may be enabled directly through an M121 or M160 AND/NOR gate, used as an NOR Expander. Maximum input to output propagation delay for any circuit is 45 nsec.

Inputs: Each DATA INPUT pin and EXPANSION INPUT pin presents one unit load. Each INPUT ENABLE pin presents two unit loads.

Outputs: Each output can drive up to ten unit loads.

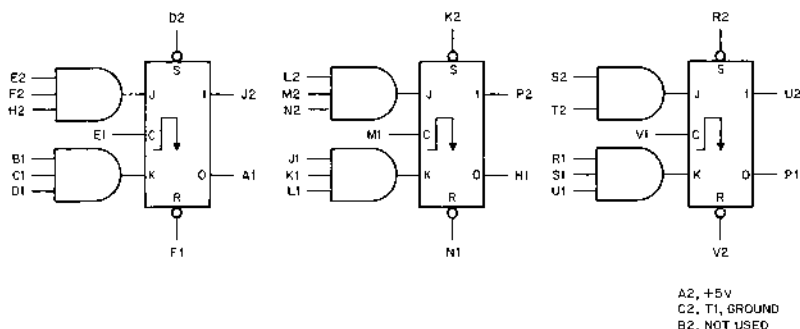
Power: +5 Volts at 50 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

M169 — \$33

TRIPLE J-K FLIP-FLOP M202

M SERIES



The M202 contains three J-K flip-flops augmented by multiple-input and gates. For general use as gated control flip flops or buffers.

Logical operation of the J-K flip flops used in this module is identical to those flip-flops used in the M207 (described in detail) except clock, J-K inputs, inputs, direct clear, direct set and both output lines for each flip-flop are independent.

Inputs: All gate inputs represent 1 unit load. The dc set and clear input each represent two unit loads. Clock inputs represent two unit loads.

Outputs: Each output will drive 10 unit loads.

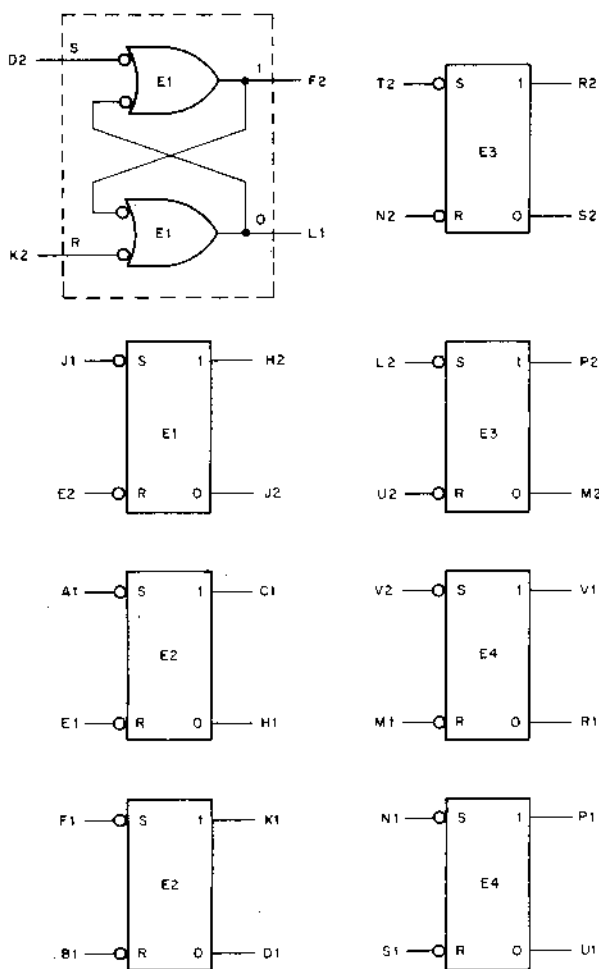
Power: +5V at 57 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

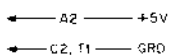
M202 — \$29

8-R/S FLIP-FLOPS M203

M SERIES



POWER:



M203 8-R/S FLIP-FLOPS

The M203 is made up of 8 R/S type flip-flops. Each flip-flop is made up of two 2-input NAND gates whose outputs are cross coupled. R/S flip-flops provide an inexpensive method of storage but care must be taken to inhibit placing the Set and Reset inputs low at the same time. In this case, the last of the inputs to be removed will control the final state of the flip-flop.

The propagation delay of the M203 is approximately 30 nsec.

Inputs: All inputs present 1 unit load.

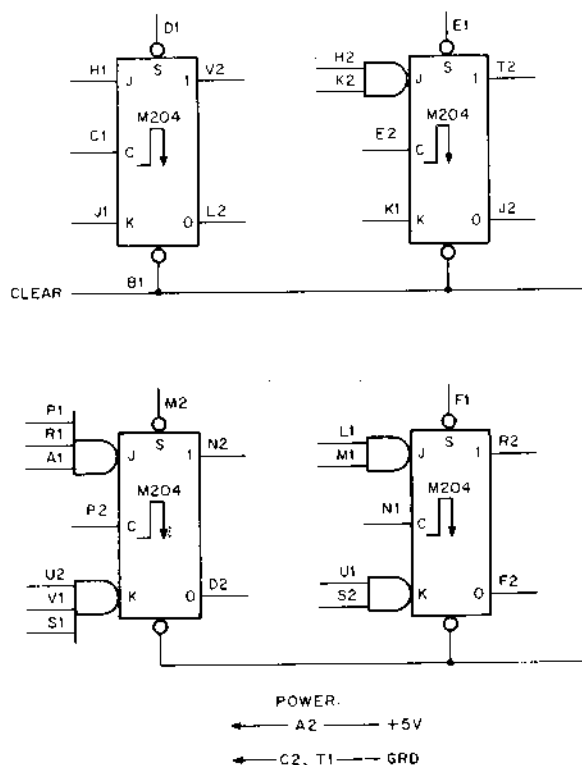
Outputs: All outputs are capable of driving 9 unit loads.

Power: +5 Volts, 55 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

GENERAL-PURPOSE BUFFER AND COUNTER M204

M SERIES



M204 GENERAL-PURPOSE BUFFER AND COUNTER

The M204 contains four J-K type flip-flops, augmented by multiple-input AND gates, for general use as gated control flip-flops or buffers. The gating scheme permits the formation of counters of most moduli up to 16, by simple connector wiring. Clock, trigger and input lines for each flip-flop are independent. A common CLEAR input is provided.

Input information is transferred to the outputs when the threshold point is reached on the trailing (negative going voltage) edge of the clock pulse.

Logical operation of the J-K flip-flops used in this module is identical to the M207 (described in detail) except for the addition of dc set inputs.

Inputs: The "C" inputs present two unit loads each to the source. The dc set ("S") inputs present two unit loads each. The common CLEAR line presents 8 unit loads. All other inputs present one unit load to the source.

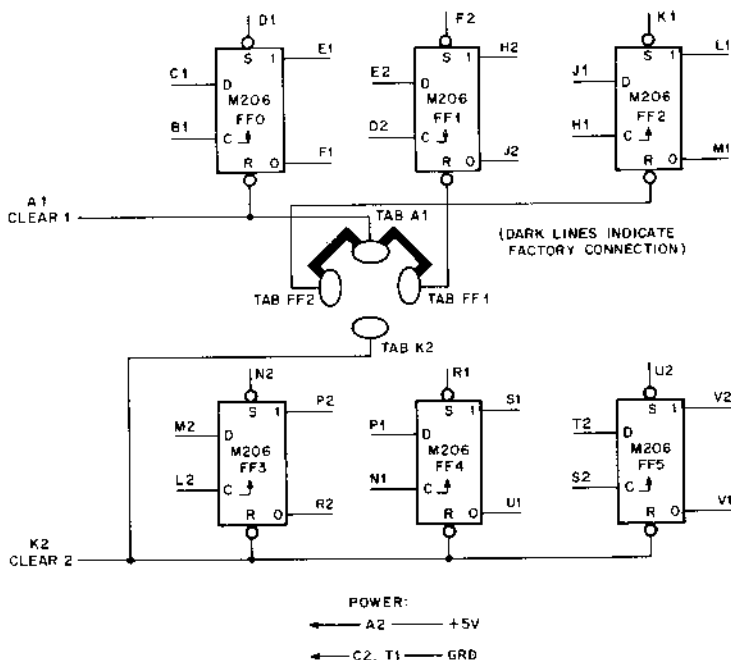
Outputs: Each output, before interconnection as a counter, is capable of driving 10 unit loads.

Power: +5 Volts, 74 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

GENERAL-PURPOSE FLIP-FLOPS M206

M SERIES



M206 D TYPE FLIP-FLOPS

The M206 contains six separate D-Type flip-flops. Each flip-flop has independent gated data, clock, and dc set inputs.

Provision is made on the printed circuit board for changing the configuration of the two CLEAR lines to the flip-flops. All M206 modules are supplied with the 3-3 configuration, but the grouping can be changed as follows:

CONFIGURATION	CLEAR 1 (A1)	CLEAR 2 (K2)	DELETE JUMPER	ADD JUMPER
3-3	FF0, 1, & 2	FF3, 4, & 5		
4-2	FF0 & 1	FF2, 3, 4, & 5	A1 to FF2	K2 to FF2
5-1	FF0	FF1, 2, 3, 4, & 5	A1 to FF2 A1 to FF1	K2 to FF2 K2 to FF1

Information must be present on the D input 20 nsec (max) prior to a standard clock pulse and should remain at the input at least 5 nsec (max) after the clock pulse leading edge has passed the threshold voltage. Data transferred into the flip-flop will be stable at the output within 50 nsec, maximum. Typical width requirement for the clock, dc reset and dc set pulses is 30 nsec each.

Information present on the D input is transferred to the output when the threshold is reached on the leading (positive going voltage) edge of the clock pulse.

Inputs: D inputs present 1 unit load each. C inputs present 2 unit loads each. CLEAR lines present 3 unit loads per connected flip-flop. S inputs present 2 unit loads each.

Outputs: Each output is capable of driving 10 unit loads.

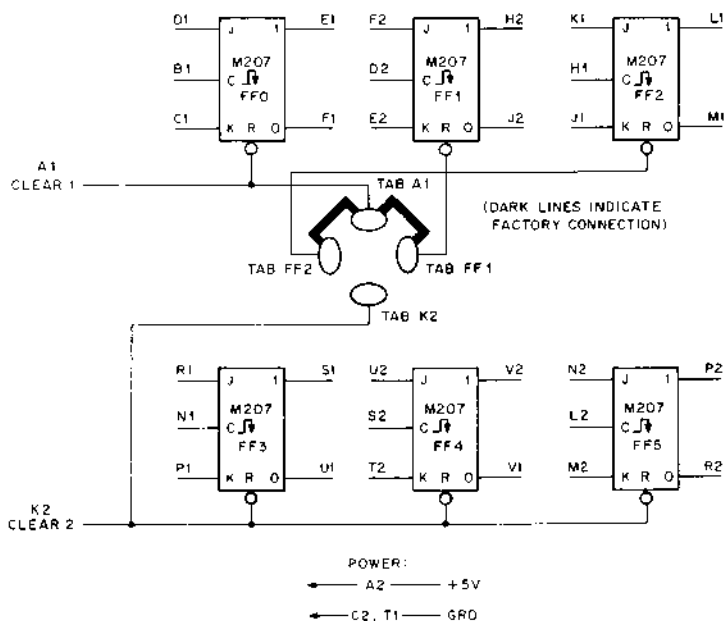
Power: +5 Volts, 87 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

A common clear for all six flip-flops can be obtained by wiring pins A1 and K2 together externally. **CAUTION:** The loading of each clear line is calculated on the basis of 3 unit loads per flip-flop. For example, the 4-2 configuration results in 12 unit loads at input K2 and 6 unit loads at input A1.

GENERAL-PURPOSE FLIP-FLOP M207

M SERIES



M207 J-K FLIP FLOPS

The M207 contains six J-K type flip-flops which can be used as buffers, control flip-flops, shift registers, and counters. A truth table for clocked set and reset conditions appears below. Note that when the J and K inputs are both high, the flip-flop complements on each clock pulse.

STARTING CONDITION (OUTPUT)		INPUT CONDITION		RESULT AT END OF STANDARD CLOCK PULSE (OUTPUT)	
1	0	J	K	1	0
L	H	L	L	No change	
		L	H	No change	
		H	L	H	L
		H	H	H	L
H	L	L	L	No change	
		L	H	L	H
		H	L	No change	
		H	H	L	H

Application of a low level to an R input for at least 25 nsec resets the flip-flop unconditionally. Two CLEAR inputs are provided, with jumper terminals for optional clearing in groups of 3 and 3 (standard), 4 and 2, 5 and 1, or 6 and 0.

J and K inputs must be stable during the leading-edge threshold of a standard clock input and must remain stable during the positive state of the clock. Data transferred into the flip-flop will be stable at the output within 30 nsec (typical) of the clock pulse trailing edge threshold (negative going voltage).

Provision is made on the printed circuit board for changing the configuration of the two CLEAR lines to the flip-flop. All M207 modules are supplied with the 3-3 configuration, but the grouping can be changed as follows:

CONFIGURATION	CLEAR 1 (A1)	CLEAR 2 (K2)	DELETE JUMPER	ADD JUMPER
3-3	FF0, 1, & 2	FF3, 4, & 5		
4-2	FF0 & 1	FF2, 3, 4, & 5	A1 to FF2	K2 to FF2
5-1	FF0	FF1, 2, 3, 4, & 5	A1 to FF2 A1 to FF1	K2 to FF2 K2 to FF1

Inputs: J or K inputs present 1 unit load each. C inputs present 2 unit loads each. CLEAR lines present 2 unit loads per connected flip-flop.

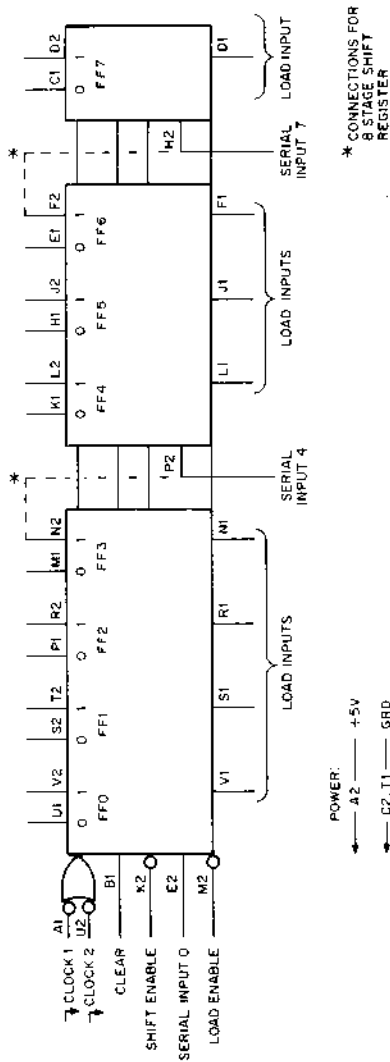
Outputs: Each output is capable of driving 10 unit loads.

Power: +5 Volts, 96 mA. (max.)

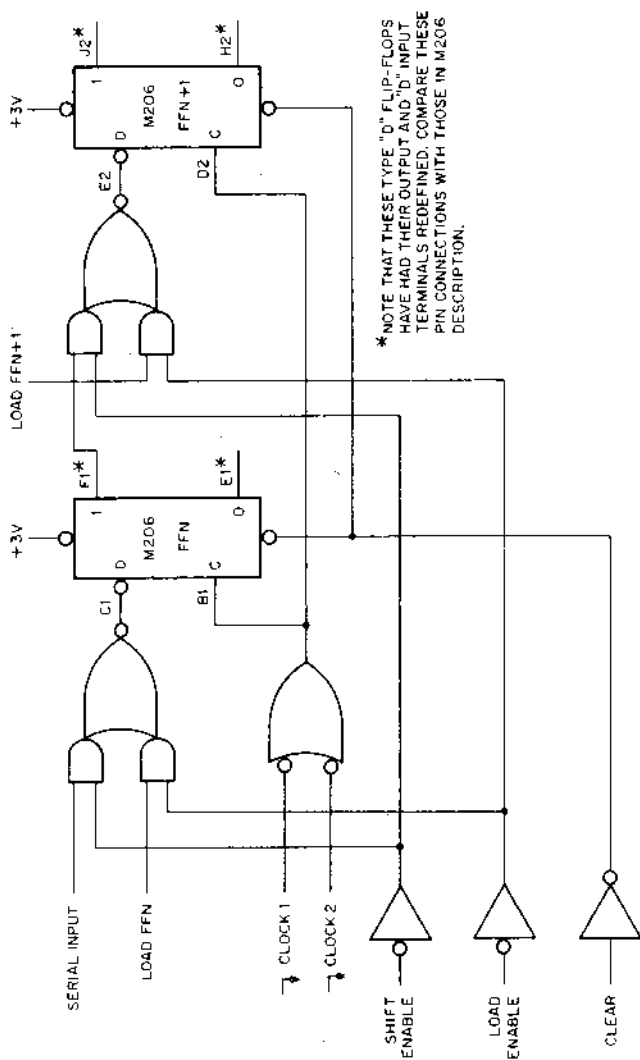
Size: Standard, single height, single width FLIP CHIP module.

8-BIT BUFFER/SHIFT REGISTER M208

M SERIES



M208 8-BIT BUFFER/SHIFT REGISTER



TWO REPRESENTATIVE STAGES

The M208 is an internally connected 8-bit buffer/shift register. Provisions are made for gated single-ended parallel load, bipolar parallel output, and serial input. The shift register is divided into three segments:

Bits 0 through 3: Serial input to bit 0, bipolar outputs from bits 0 through 3.

Bits 4 through 6: Serial input to bit 4, bipolar outputs from bits 4 through 6.

Bit 7: Serial input to 7, bipolar outputs from bit 7.

Each of these groups shares a common shift line (the ORed CLOCK 1 and CLOCK 2 inputs) and a common parallel load line (LOAD ENABLE). To form a 6-bit shift register, for example, the true output of bit 3 is connected to the serial input of stage 4. A shift register of 8 bits may be constructed from a single module. Modules may be cascaded to form shift registers of any desired length. A few additional stages may be formed more economically from NAND and AND/NOR gates plus a D-type flip-flop. A representative stage of this type is illustrated.

Two clock inputs are provided so that individual Load and Shift clock sources may be used. Care must be taken that the clock inputs remain in the high state in the off condition because either input going to the low state will produce a positive edge at the output of the NAND gate and trigger the D type flip-flop. Data shifted or parallel loaded into the M208 will appear on the outputs within 55 nsec (max) of the clock pulse leading edge threshold. Load of Shift Enable levels and parallel data must be present at least 50 nsec prior to a clock pulse. Propagation delay from the leading edge of a CLEAR pulse to the outputs is 40 nsec max.

Inputs: Serial data, dc set, and enable inputs present one unit load each to the source module. Each clock input presents $2\frac{1}{2}$ unit loads. The CLEAR input presents two unit loads.

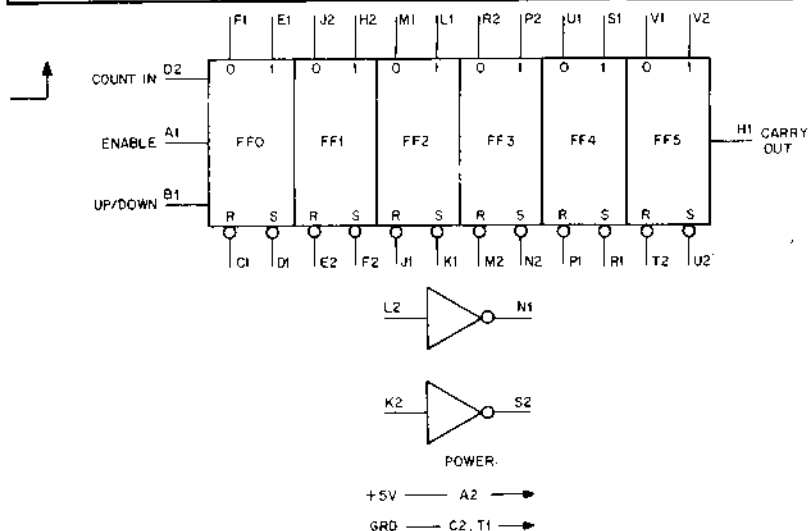
Outputs: Parallel outputs are capable of driving 10 unit loads each.

Power: +5 Volts, 184 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

BINARY UP/DOWN COUNTER M211

M SERIES



M211 BINARY UP/DOWN COUNTER

The M211 is a 6 bit binary UP/DOWN counter. It can switch counting mode (UP or DOWN) without disturbing the contents of the counter. Maximum count rate is 10 MHz. SET/RESET inputs are available for each bit. Maximum carry propagation time is 80 ns per bit.

Enable Line: The Enable input must be negated 100 nsec. prior to an UP/DOWN level command.

The Enable input must **not** be negated earlier than 500 nsec. after the leading edge (positive going voltage) of the clock pulse.

The Enable input must be asserted at least 60 nsec. prior to the first count.

UP/DOWN Control Line: A logical 1 on this line will yield an up count.

A logical 0 on this line will yield a down count.

Carry Out: The Carry Out will yield a positive level change whenever a carry or borrow occurs.

Inputs: Count In—positive transition or pulse with less than 400 nsec rise-time. Count In presents 2 unit loads. Reset—Each reset input presents 3 unit loads. Set—Each set input presents 2 units loads. All other inputs present 1 unit load.

Outputs: Each flip flop output (1 or 0) can drive 8 unit loads. Carry Out can drive 10 unit loads. Each inverter output can drive 30 unit loads.

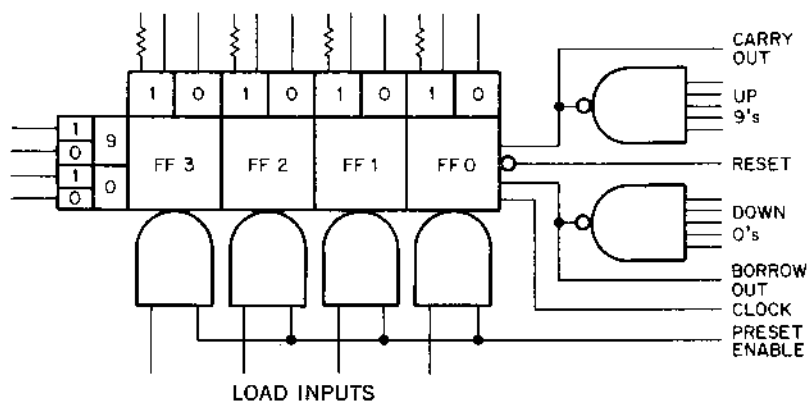
Power: +5.0 Volts, 217 mA.(max.)

Size: Standard, single height, single width FLIP CHIP module.

M211 — \$69

BCD UP/DOWN COUNTER M213

M SERIES



PIN	A CONNECTOR		B CONNECTOR	
	SIDE (1)	SIDE (2)	SIDE (1)	SIDE (2)
A	—	+5	—	+5
B	—	—	—	—
C	—	Ground	—	Ground
D	9 (0) Out	9 (1) Out	0 (0) Out	0 (1) Out
E	9 In	Up	0 In	Down
F	9 In	9 In	0 In	0 In
H	Carry Out	9 In	Borrow Out	0 In
J	Test Point	9 In	—	0 In
K	—	9 In	—	0 In
L	—	9 In	—	0 In
M	Test Point	Preset Enable	—	—
N	—	Clock	Test Point	Reset
P	Test Point	Load FF 0	Test Point	Load FF 2
R	Test Point	Load FF 1	Test Point	Load FF 3
S	FF 0 (0)	FF 0 (1)	FF 2 (0)	FF 2 (1)
T	Ground	FF 0 (1)	Ground	FF 2 (1)
U	FF 1 (0)	FF 1 (1)	FF 3 (0)	FF 3 (1)
V	—	FF 1 (1)	—	FF 3 (1)

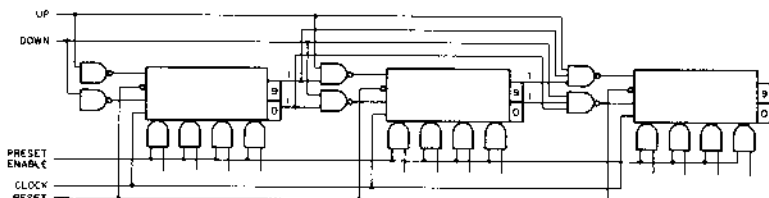
The M213 can be used to construct multi-digit synchronous counters for up/down counting in binary coded decimal. The maximum counting rate is 5 MHz. The counting direction is controlled by enabling the up or down control gate inputs. For maximum noise immunity, the up and down control lines should be kept low until counting is desired. Clock pulses that occur while the up and down lines are both low will not change the contents of the counter. Unpredictable operation will result if both the up and down lines are high at the same time. Positive clock pulses should not occur sooner than 50 ns after any change in the up or down control lines.

The "1" side of each flip-flop output is available directly for controlling nearby logic or through an isolation resistor when decoding displays are being driven at the end of long lines.

The counter may be preset by first resetting the counters and enabling the preset line. The clock input should then be pulsed once with a positive pulse to transfer data from the load inputs into the flip-flops. The up and down control lines must both be low for correct preset operation.

Counter Construction: The up and down input gate wiring for cascading M213 modules makes it possible to construct the hardware for fixed decimal point counters so that additional digits to the left or right of the decimal point can be added later as options. If the sockets are wired initially for a larger counter than is thought to be required, the unused high order digits may be left blank. Unused low order digit sockets should have pins AD2 and BD2 connected to +3 Volts. When it is found that additional counter capacity or accuracy is needed, M213 modules can be plugged into the blank sockets on either side of the decimal point as required.

The diagram below shows how to connect three M213 counters for up/down counting. Notice that all the counters are clocked at the same time, but that a counter will not count unless the counters of lower significant digits all contain 9's for up counting or 0's for down counting. All unused module inputs should be connected to +3 Volts.



Inputs: The input loads presented are:

CLOCK	— Eight unit loads
RESET	— Eight unit loads
PRESET ENABLE	— Four unit loads
All other inputs	— One unit load

Pulse widths required:

CLOCK	POSITIVE	> 20 nsec
RESET	NEGATIVE	> 25 nsec

Outputs: Output drive ability:

FLIP-FLOP 1 or 0	— Seven unit loads
FLIP-FLOP 1 (Resistor)	— Five unit loads
(Total load on a 1 output is 7 unit loads.)	
CARRY OUT	— Eight unit loads
BORROW OUT	— Eight unit loads

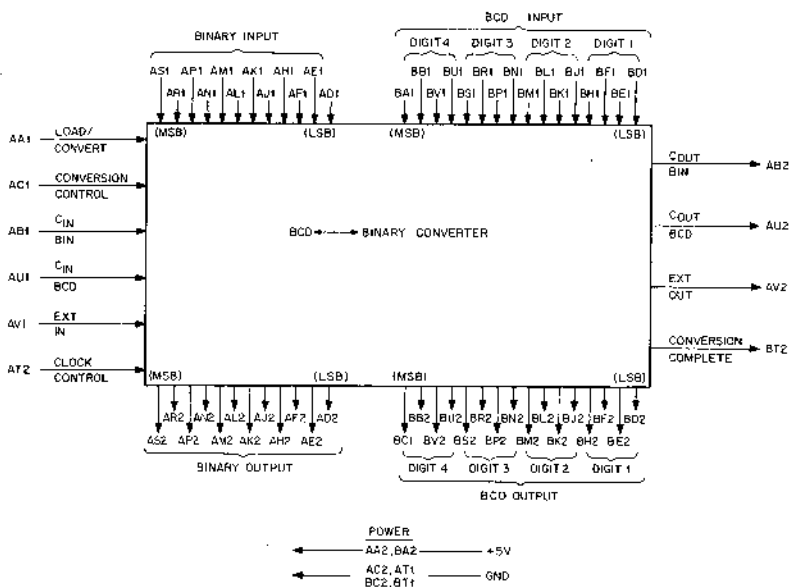
Cascade Outputs:

9 (1), 9 (0)	
0 (1), 0 (0)	Ten unit loads

Power: +5 Volts at 160 mA. (max.)**Size:** Standard, double height, single width FLIP CHIP module.M213 — \$86

BINARY TO BCD AND BCD TO BINARY CONVERTER M230

M SERIES



The M230 converts a binary number to its binary coded decimal equivalent or a binary coded decimal number to its binary equivalent.

The maximum number that can be converted from either binary to BCD or BCD to binary is 4095 which is 7777₈. This converter utilizes a counting technique where the count frequency is typically 5 MHz. Therefore, the conversion time for the maximum number 7777₈ is typically 0.82 millise.

The M230 is fully cascable. When using more than one M230 the C_{OUT} BIN, must be connected to the C_{IN} BIN, and the C_{OUT} BCD must be connected to the C_{IN} BCD of the next higher significant unit. C_{IN} BIN, and C_{IN} BCD of the least significant unit must be made a logic "1". C_{OUT} BIN, and C_{OUT} BCD of the most significant unit may be left open.

CONVERSION CONTROL on pin AC1 will cause a Binary to BCD conversion when connected to ground and a BCD to Binary conversion when connected to a logic "1" source. When cascading M230's, connect all CONVERSION CONTROL inputs in parallel.

LOAD/CONVERT on pin AA1 reads the input data when connected to a logic "1" level and starts the conversion when this input is returned to a logic "0" level. When cascading M230's, connect all LOAD/CONVERT inputs in parallel.

CONVERSION COMPLETE on pin BT2 goes High when the conversion process is finished.

EXT. IN on pin AV1 and EXT. OUT on pin AV2 convey conversion finished information between cascaded M230's. This information travels from the most significant M230 to the least significant M230. Therefore, the EXT. IN of the most significant M230 **must** be connected to a logic "1" source. Each EXT. OUT is connected to the EXT. IN of the next less significant M230. The EXT. OUT of the least significant M230 is left unconnected.

CLOCK CONTROL on pin AT2 of the least significant M230 should be enabled by connecting it to a logic "1" source. All others should be connected to ground.

The following is an ordered summary for operating a single M230:

1. Make the conversion control (pin AC1) a logic "0" for converting Binary to BCD or a logic "1" for converting BCD to Binary.
2. When converting Binary to BCD, connect the Binary number to the BINARY INPUTS and ground the BCD INPUTS. Conversely, when converting BCD to Binary, connect the BCD number to the BCD INPUTS and ground the BINARY INPUTS.
3. C_{IN} BIN., C_{IN} BCD, EXT. IN, and CLOCK CONTROL inputs should be tied to a source of logic "1". The outputs C_{OUT} BIN., C_{OUT} BCD, and EXT. OUT should be left unconnected.
4. Pulse the LOAD/CONVERT input with a positive pulse of 150 nsec. minimum pulse width. There is no limit on the maximum width of this pulse. Conversion begins on the negative going edge of this pulse.
5. When converting Binary to BCD read the BCD OUTPUT for the BCD equivalent. For converting BCD to Binary read the BINARY OUTPUT for the Binary equivalent. The CONVERSION COMPLETE OUTPUT becomes a logic "1" when the conversion is through.

Inputs: Each Binary Input bit, each BCD Input bit, LOAD/CONVERT, CONVERSION CONTROL, CLOCK CONTROL, and EXT. IN each present 1 TTL load. C_{IN} BIN. and C_{IN} BCD each present 1.25 TTL loads.

Outputs: Each BINARY OUTPUT bit, each BCD OUTPUT bit, C_{OUT} BIN., C_{OUT} BCD, and CONVERSION COMPLETE can supply 10 TTL loads. Ext. Out can supply 9 TTL loads.

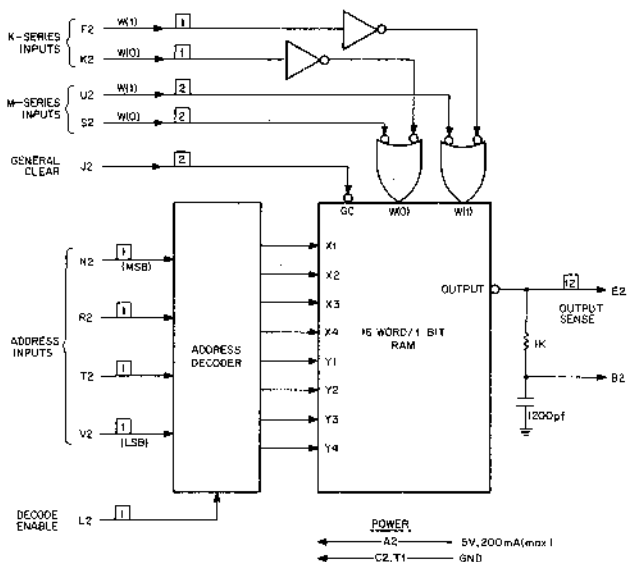
Power: +5 Volts, 860 mA (max.)

Size: Standard length, double height, single width FLIP CHIP module.

16 WORD RAM M232

1 BIT/WORD

M SERIES



On a standard $2\frac{1}{2}'' \times 5''$ FLIP CHIP module, the M232 provides individually addressable storage for 16 bits. Each bit is addressed by a 4-bit code on input lines N2, R2, T2, and V2. Access to an addressed location occurs 25 nanoseconds after the decode enable pin L2 goes High. If a "0" is stored at an accessed address, the output sense pin E2 remains High. If a "1" is stored, the output sense signal goes Low. Writing with M Series signals, 25 nanosecond minimum pulse width, is achieved by causing pin U2 to go Low for a "1" or pin S2 to go Low for a "0" after a location has been accessed. Writing with K Series signals, 5 microseconds minimum pulse width, is achieved by causing pin F2 to go High for a "1" or pin K2 to go High for a "0" after a location has been accessed. All locations can be accessed simultaneously and all bits cleared to "0" by a 5 microsecond Low signal on the general clear pin J2. Pin B2 is a special purpose output sense connection which is used when module outputs are ORed or connected in parallel as is done in some PDP-14 systems.

Input Loading: 1 unit on pins F2, K2, L2, N2, R2, T2, V2
2 units on pins J2, S2, U2

Output Drive: Pin E2 will supply 12 unit loads

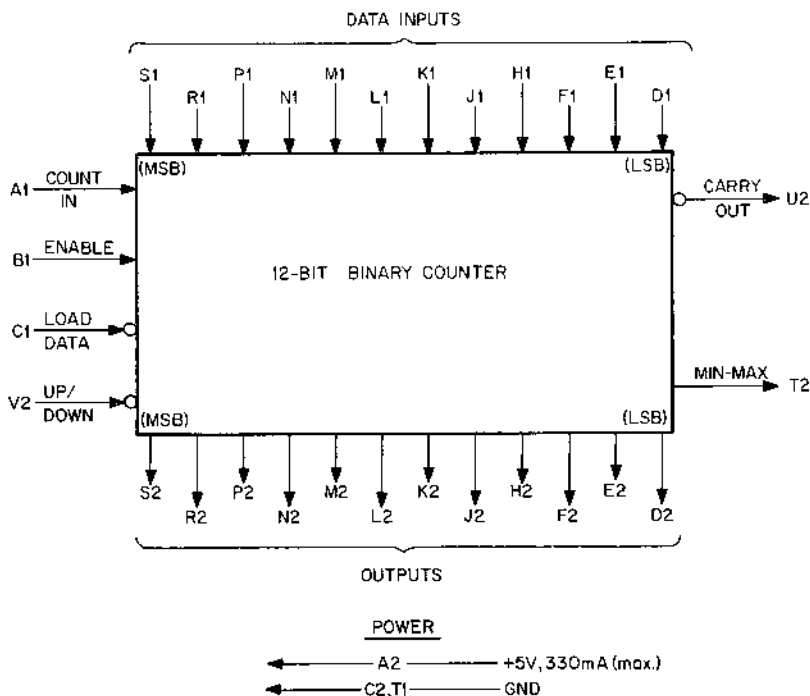
Power: +5 Volts at 200 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

M232—\$125

12-BIT BINARY UP/DOWN COUNTER M236

M SERIES



The M236 is a 12-Bit **synchronous** Binary UP/DOWN COUNTER. It has a single control input that can switch the counting mode from up to down without disturbing the contents of the counter. The maximum count frequency is 10 MHz.

The M236 has been designed to be cascadable and fully programmable. Cascading simply involves paralleling the respective COUNT IN, LOAD DATA, and UP/DOWN signals while each MAX-MIN signal drives the ENABLE input of the next M236.

Caution: Cascading more than two units involves paralleling the respective LOAD DATA, UP/DOWN, and ENABLE signals and connecting each CARRY OUT to the CARRY IN of the next M236.

The programmability of the M236 makes it ideal for use as a modulo-N divider. Modification of the count length is easily done by "Setting" the DATA input lines to N and "Loading" each time the count down reaches zero. When counting down the MAX-MIN output goes high when all twelve bits equal zero.

COUNT IN on pin A1: The high going edge of this input signal causes counting when the ENABLE input is in the logic "1" state. The minimum pulse width for either the "1" or "0" state is 50 nsec. There are no maximum pulse width limitations.

ENABLE on pin B1: A logic "1" on this line enables the counter. This input must go High no later than 70 nsec. before the first Low to High transition of the signal to be counted. This input will disable the counter when held Low. The ENABLE signal should not be changed from High to Low while the COUNT IN is Low or during the 40 nsec. period before the COUNT IN signal goes Low.

LOAD DATA on pin C1: The outputs assume the same state as their associated data inputs independent of the count when the LOAD DATA is taken to a logic "0" for at least 50 nsec. Loading data overrides all other input signals and may be done at any time. The maximum propagation delay from LOAD DATA input to any output is 50 nsec. The DATA inputs will have no affect upon the outputs immediately after the LOAD DATA line goes High.

UP/DOWN CONTROL on pin V2: A logic "0" on this line will yield an up count. A logic "1" on this line will yield a down count. This control signal may be changed when the COUNT IN signal is High. It must not be changed while the COUNT IN is Low or during the 40 nsec. period before the COUNT IN signal goes Low.

CARRY OUT on pin U2: When the counter has reached either the maximum up-count state (7777₈) or the minimum down-count state (0000₈) the CARRY OUT signal follows the COUNT IN signal. The maximum delay time from the COUNT IN pulse to the CARRY OUT pulse is 60 nsec.

When cascading M236's the MAX-MIN should be connected to the ENABLE of the next M236 if the COUNT IN's are paralleled; or the CARRY OUT should

be connected to the COUNT IN of the next M236 if the ENABLE's are paralleled.

MAX-MIN on pin T2: This provides a logic "1" output when the counter has reached either the maximum up-count state (7777₈) or the minimum down-count state (0000₈). The maximum delay time for this output measured from the positive going edge of the COUNT IN signal is 120 nsec. This signal is also used to accomplish look-ahead for very high speed operations.

Inputs: The DATA INPUTS, COUNT IN and ENABLE present 1 unit load.

The UP/DOWN and LOAD DATA inputs present 3 unit loads.

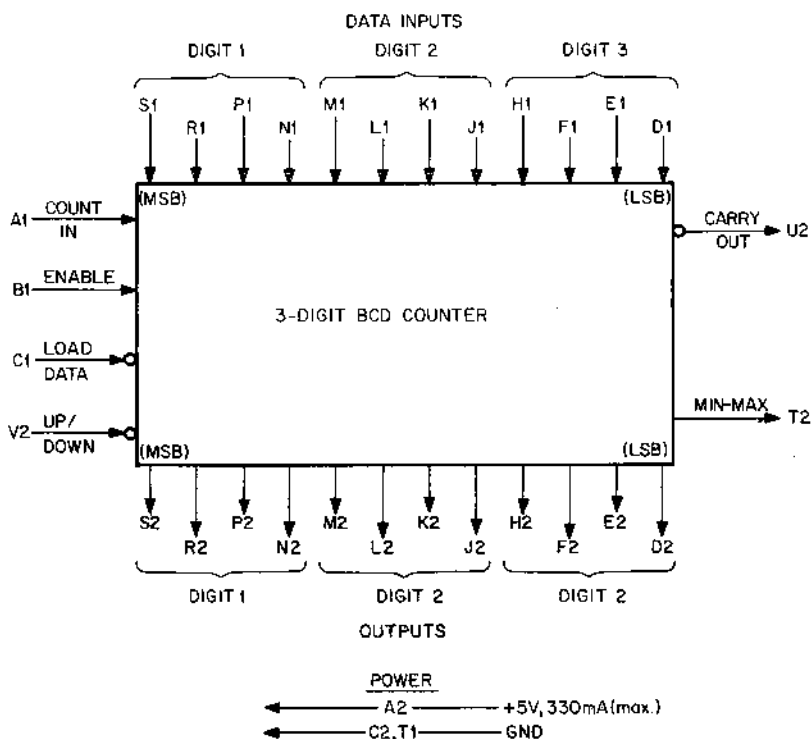
Outputs: All outputs including MAX-MIN and CARRY OUT are capable of driving 10 unit loads.

Power: +5 Volts, 330 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

3-DIGIT BCD UP/DOWN COUNTER M237

M SERIES



The M237 is a 3-digit **synchronous** BCD UP/DOWN COUNTER. It has a single control input that can switch the counting mode from up to down without disturbing the contents of the counter. The maximum count frequency is 10 MHz:

The M237 has been designed to be cascadable and fully programmable. Cascading simply involves paralleling and respective COUNT IN, LOAD DATA, and UP/DOWN signals while each MAX-MIN signal drives the ENABLE input of the next M237 in line.

Caution: Cascading more than two units involves paralleling the respective LOAD DATA, UP/DOWN, and ENABLE signals and connecting each CARRY OUT to the CARRY IN of the next M237.

The programmability of the M237 makes it ideal for use as a modulo-N divider. Modification of the count length is easily done by "Setting" the DATA

input lines to N and "Loading" each time the count down reaches zero. When counting down the MAX-MIN output goes high when all three digits equal zero.

COUNT IN on pin A1: The high going edge of this input signal causes counting when the ENABLE input is in the logic "1" state. The minimum pulse width for either the "1" or "0" state is 50 nsec. There are no maximum pulse width limitations.

ENABLE on pin B1: A logic "1" on this line enables the counter. This input must go High no later than 70 nsec. before the first Low to High transition of the signal to be counted. This input will disable the counter when held Low. The ENABLE signal should not be changed from High to Low while the COUNT IN is Low or during the 40 nsec. period before the COUNT IN signal goes Low.

LOAD DATA on pin C1: The outputs assume the same state as their associated data inputs independent of the count when the LOAD DATA is taken to a logic "0" for at least 50 nsec. Loading data overrides all other input signals and may be done at any time. The maximum propagation delay from LOAD DATA input to any output is 50 nsec. The DATA inputs will have no affect upon the outputs immediately after the LOAD DATA line goes High.

UP/DOWN CONTROL on pin V2: A logic "0" on this line will yield an up count. A logic "1" on this line will yield a down count. This control signal may be changed when the COUNT IN signal is High. It must not be changed while the COUNT IN is Low or during the 40 nsec. period before the COUNT IN signal goes Low.

CARRY OUT on pin U2: When the counter has reached either the maximum up-count state (999) or the minimum down-count state (000) the CARRY OUT signal follows the COUNT IN signal. The maximum delay time from the COUNT IN pulse to the CARRY OUT pulse is 60 nsec.

When cascading M237's the MAX-MIN should be connected to the ENABLE of the next M237 if the COUNT IN's are paralleled; or the CARRY OUT should be connected to the COUNT IN of the next M237 if the ENABLE's are paralleled.

MAX-MIN on pin T2: This provides a logical "1" output when the counter has reached either the maximum up-count state (999) or the minimum down-count state (000). The maximum delay time for this output measured from the positive going edge of the COUNT IN signal is 120 nsec. This signal is also used to accomplish look-ahead for very high speed operations.

Inputs: The DATA INPUTS, COUNT IN and ENABLE present 1 unit load.

The UP/DOWN and LOAD DATA inputs present 3 unit loads.

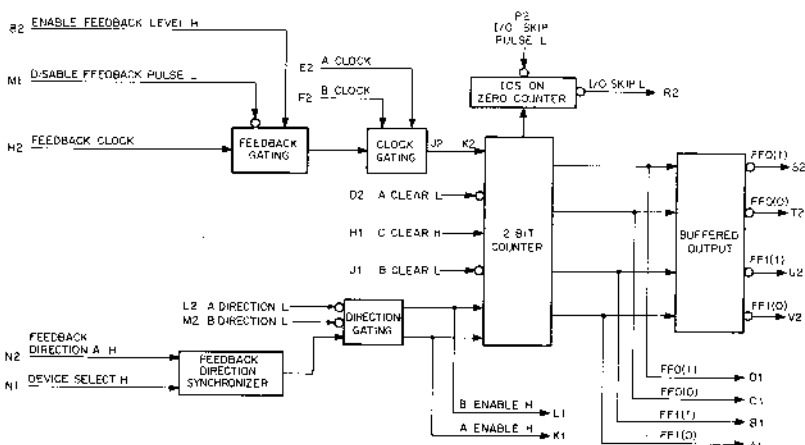
Outputs: All outputs including MAX-MIN and CARRY OUT are capable of driving 10 unit loads.

Power: ± 5 Volts, 330 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

4-STATE MOTOR TRANSLATOR M261

M SERIES



M261

BLOCK DIAGRAM

The M261 motor translator will develop the sequence of patterns necessary to step a Sigma or Superior Electric type stepping motor (4 winding). It is a 2-bit switch-tail ring counter which, if initially cleared, would be in state 1. (Fig. 1)

State	Flip Flop	0	1
1		0	0
2		0	1
3		1	1
4		1	0

State	Winding	A	B	C	D
1		1	1	0	0
2		0	1	1	0
3		0	0	1	1
4		1	0	0	1

1 = current supplied to winding

FIGURE 1

FIGURE 2

The state sequence (1, 2, 3, 4, 1, . . . or 1, 4, 3, 2, 1, . . .) is determined by the direction gating. The pattern for motor stepping (Fig. 2) is achieved by assigning flip flop outputs to windings; A-FF1(1), B-FF0(1), C-FF1(0), D-FF0(0). These buffered flip flop outputs can enable K-series DC drivers to energize the selected winding.

The translator is clocked by a High to Low transition on A CLOCK or B CLOCK. The ORed clock signal must be jumpered externally to the counter (J2-K2). DIRECTION is stored in an RS flip flop and can be loaded by asserting one

of the direction inputs Low. This arrangement facilitates the use of M103 or M107 device selectors; the first pulse of an IOT (input/output transfer instruction) sets the direction, the second clocks the counter.

For closed loop operation, the direction flip flop may be synchronized with the motor shaft rotation. If there is a direction level available from the transducer, this level should be asserted high when the direction of rotation is the same as that represented by the A DIRECTION L input to the flip flop. This gating may be disabled by DEVICE SELECT H. The clock input for feedback operation is a Low to High transition and is ORed with the other clocks after gating. The two gating signals are an enable, asserted High, and a pulse or level asserted Low which truncates the clock pulse after it has made its transition. This is necessary because the clock signal is from an asynchronous device and is often a square wave which remains High a long time (20-100 μ s) after the clocking transition. This High level at the clock input of the counter will mask subsequent transitions on the other clock inputs.

This module may be used in conjunction with the I/O skip facility on a computer. An IOT at I/O SKIP PULSE L and both flip flops in the zero state will cause I/O SKIP L to be generated.

The unbuffered flip flop outputs are available for additional gating. These lines are electrically distinct from the buffered outputs.

Inputs:	H2 FEEDBACK CLOCK	2 unit loads
	K2 CLOCKS IN	4 " "
	N2 FEEDBACK DIRECTION A H	2 " "

All other inputs represent one unit load

Outputs:	K1 A ENABLE	7 units loads
	L1 B ENABLE	7 " "
	A1 FF1(0)	7 " "
	B1 FF1(1)	8 " "
	C1 FF0(0)	7 " "
	D1 FF0(1)	8 " "

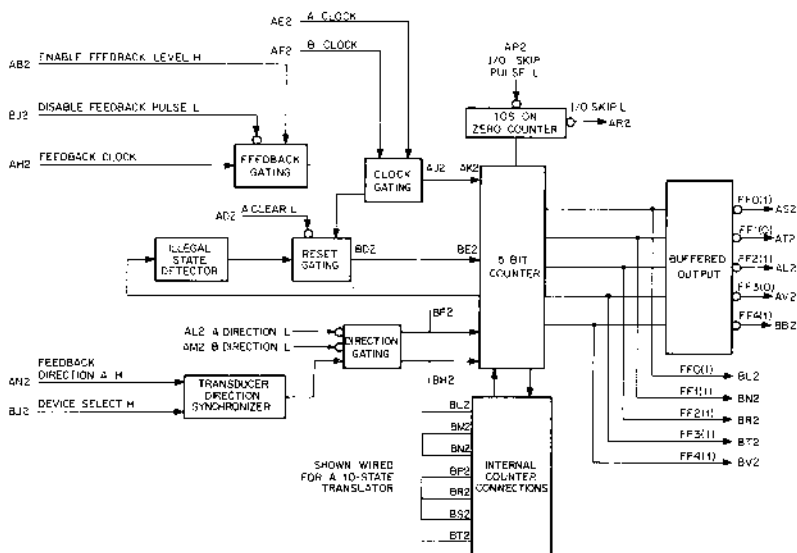
All other outputs will drive ten unit loads

Power: \pm 5V, 175 mA (max)

Size: Standard, single height, single width FLIP CHIP module

10-STATE MOTOR TRANSLATOR M262

M SERIES



M262 BLOCK DIAGRAM

The M262 motor translator will generate the sequence of patterns necessary to step a Fujitsu type stepping motor (5 winding). It is a double height module with a five bit switch-tail ring counter which may be truncated to four or three bits by external jumpers. (Fig. 1)

BM-BN
BP-BR
BR-BS

BM-BN
BP-BN
BT-BS

BL-BP
BT-BM

10-state jumpers

8-state jumpers

6-state jumpers

Figure 1

State	FLIP	FLOP	0	1	2	3	4
1			0	0	0	0	0
2			1	0	0	0	0
3			1	1	0	0	0
4			1	1	1	0	0
5			1	1	1	1	0
6			1	1	1	1	1
7			0	1	1	1	1
8			0	0	1	1	1
9			0	0	0	1	1
10			0	0	0	0	1

FIGURE 2

State	Winding	A	B	C	D	E
1		1	1	1	0	0
2		0	1	1	0	0
3		0	1	1	1	0
4		0	0	1	1	0
5		0	0	1	1	1
6		0	0	0	1	1
7		1	0	0	1	1
8		1	0	0	0	1
9		1	1	0	0	1
10		1	1	0	0	0

FIGURE 3

1 = current supplied to winding

FF2 is removed for the 8-state counter and both FF1 and FF2 are bypassed for the 6-state counter.

After the counter is cleared it will be in state 1. (Fig. 2) The state sequence (1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 1 . . . or 1, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1 . . .) is determined by the direction gating. The pattern for motor stepping (Fig. 3) is achieved by assigning flip flop outputs to windings; FF0(1)-A FF2(1)-B, FF4(1)-C, FF1(0)-D, FF3(0)-E. These buffered flip flop outputs can enable K-series DC drivers to energize the selected windings.

The translator is clocked by a High to Low transition on A CLOCK or B CLOCK. The ORed clock signal must be jumpered externally to the counter (AJ-AK). Direction is stored in an RS flip flop and can be loaded by asserting one of the direction inputs Low. This arrangement facilitates the use of M103 or M107 device selectors; the first pulse of an IOT (input output transfer instruction) set the direction, the second clocks the counter.

With a 5-bit counter there are 32 (2^5) possible states, but the counter is clocked through a ring of only 10 states (Fig. 2). Gating is available to detect illegal states and clear the counter to state 1. This gating must be connected by an external jumper (BD-BE).

For closed loop operation, the direction flip flop may be synchronized with the motor shaft rotation. If there is a direction level available from the transducer, this level should be asserted High when the direction of rotation is the same as that represented by the A DIRECTION L input to the flip flop. This gating may be disabled by DEVICE SELECT H. The clock input for feedback operation is a Low to High transition and is ORed with the other clocks after gating. The two gating signals are an enable, asserted High, and a pulse or level asserted Low which truncates the clock pulse after it has made its transition. This is necessary because the clock signal is from an asynchronous device and is often a square wave which remains high a long time (20-100 μ s) after the clocking transition. This High level at the clock input of the counter will mask subsequent transitions on the other clock inputs.

This module may be used in conjunction with I/O skip facility on a computer. An IOT at I/O SKIP PULSE L and both flip flops in the zero state will cause I/O SKIP L to be generated.

The unbuffered flip flop outputs are available for additional gating. These lines are electrically distinct from the buffered outputs.

Inputs:	AD A CLEAR L	3	unit	loads
	AH FEEDBACK CLOCK	2	"	"
	AK CLOCKS IN	10	"	"
	AN FEEDBACK DIRECTION A H	3	"	"
	AP I/O SKIP PULSE L	2	"	"
	BE RESET IN	15	"	"

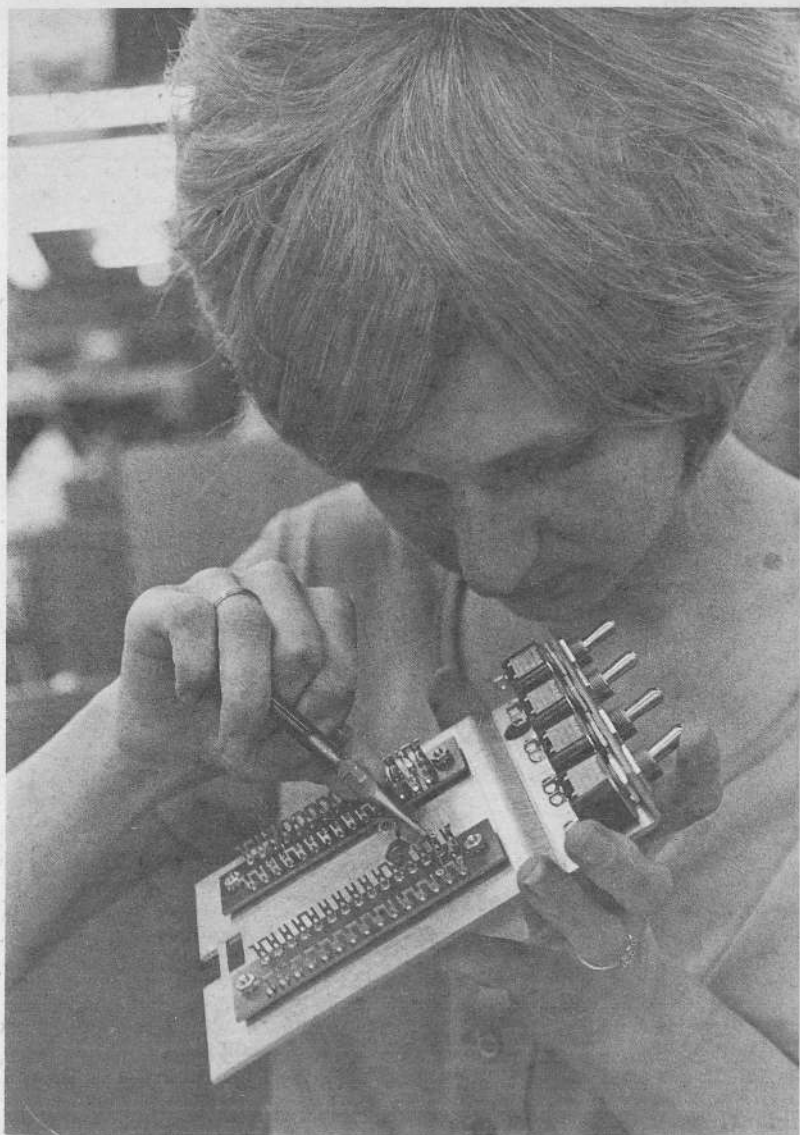
All other inputs represent one unit load

Outputs:	BF A ENABLE	4	unit	loads
	BH B ENABLE	4	"	"
	BL FF0(1)	8	"	"
	BN FF1(1)	7	"	"
	BR FF2(1)	7	"	"
	BT FF3(1)	7	"	"
	BV FF4(1)	8	"	"

All other outputs will drive ten unit loads

Power: +5V, 350 mA (max)

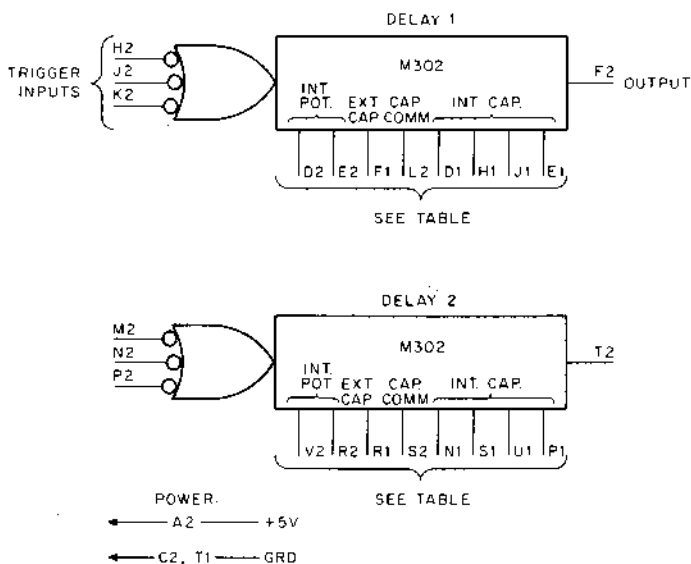
Size: Standard, double height, single width FLIP CHIP module.



This subassembly process shows the placing of components and jumpers on a specially prepared terminal strip.

DUAL DELAY MULTIVIBRATOR M302

M SERIES



The M302 contains two delays (one-shot multivibrators) which are triggered by a level change from high to low or a pulse to low whose duration is equal to or greater than 50 nanoseconds. When the input is triggered, the output changes from low to high for a predetermined length of time and then returns to low. The basic DELAY RANGE is determined by an internal capacitor. The delay range may be increased by selection of additional capacitance which is available by connecting various module pins or by the addition of external capacitance. An internal potentiometer can be connected for fine delay adjustments within each range or an external resistance may be used. If an external resistance is used, the combined resistance of the internal potentiometer and the external resistance should be limited of 10,000 ohms.

The fall time of the input trigger should be less than 400 nanoseconds.

The delay time is adjustable from 50 nanoseconds to 7.5 milliseconds using the internal capacitors and can be extended by adding an external capacitor.

Care should be exercised in the selection of external capacitors to assure low leakage as leakage will affect the time delay.

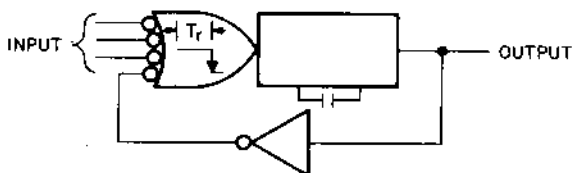
Recovery time is determined by the size of the capacitance used. The minimum recovery time of this module is 30 nanoseconds when not using any additional capacitance. Recovery time with additional capacitance can be calculated using the formula:

$$T_r = 300 C$$

Where T_r is in seconds

C is in farads

Recovery time is defined for this module as follows: Recovery time, T_r , is the minimum time interval which must exist before each trigger with all inputs high and the output low. The figure shown below illustrates these conditions:



Delay Range	Capacitor Value	Interconnections Required	
		Delay 1	Delay 2
50 nsec — 750 nsec	100 pf (internal)	None	None
500 nsec — 7.5 usec	1000 pf (internal)	D1 — L2	N1 — S2
5 usec — 75 usec	0.01 uf (internal)	H1 — L2	S1 — S2
50 usec — 750 usec	0.10 uf (internal)	J1 — L2	U1 — S2
500 usec — 7.5 msec	1.0 uf (internal)	E1 — L2	P1 — S2
Above 7.5 msec	Add external capacitors between specified pins	F1 — L2	R1 — S2

Adjustable Delays: connect pins to add internal adjustment potentiometer. Without a potentiometer, the delay will not recover. An external potentiometer of less than 10K Ω can be used by connecting it between E2 or R2 and ground pin C2. Use of an external adjustment resistor will cause some increase in jitter. It is recommended that leads to an external potentiometer be twisted pairs and as short as possible.

Inputs: Each input presents 2½ unit loads.

Outputs: Each output is capable of driving 25 unit loads.

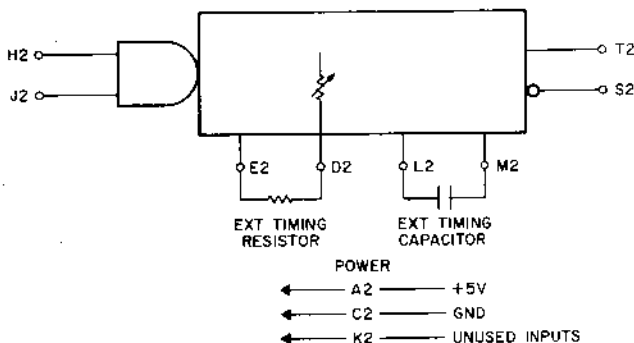
Power: +5 Volts, 166 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

M302 — \$46

INTEGRATING ONE SHOT M306

M SERIES



The M306 is a zero recovery time integrating monostable multivibrator with complementary outputs. The M306 has the ability to respond to an input even while in the active state, so that successive inputs above a preset frequency can postpone the return to the inactive state indefinitely.

TIMING CAPACITORS

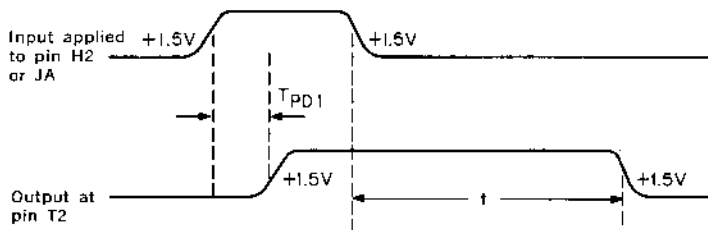
Course adjustment of the integration period is accomplished by customer supplied capacitors which may be attached to module pins L2 and M2. When using polarized capacitors, the positive terminal should be connected to pin M2. Two split lugs are also provided on the module for those customers who would like to permanently install the capacitor on the module itself. The minimum equivalent parallel resistance of capacitor leakage should always exceed 250K ohms.

TIMING RESISTANCE

Fine adjustment of the timing period may be accomplished by a multiturn potentiometer provided on the module. Provision is also made to allow the customer to connect an external timing resistor or potentiometer between pins D2 and E2. When an external potentiometer is used, care should be taken to prevent the coupling of externally generated electrical noise into the module. The maximum resistance of the timing resistance, including the internally provided potentiometer, should not exceed 25,000 ohms. If an external timing resistor is not used, pins D2 and E2 must be connected together.

TIMING PERIOD

The operation of the M306 is illustrated in the timing diagram shown below:



The integration period is measured from the trailing edge of the input pulse to the trailing edge of the output pulse. The approximate integration time may be calculated by the following:

$$t \approx .87 (R + 700 \Omega) (C + 175 \times 10^{-12} \text{ F})$$

where R is in ohms and C is in farads. The width of the input pulse is independent of the integration time. An input pulse of 30NS will trigger the M306.

STABILITY

The inherent temperature stability of the M306 is normally $-.06\% \text{ } ^\circ\text{C}$, exclusive of the temperature coefficient of the timing capacitor.

Inputs: Each Input represents 1.25 unit loads

Outputs: Pin S2 will supply 12.5 unit loads. Pin T2 will supply 11 unit loads.

Pin K2 is a source of Logic "1" used to return unused inputs. It will supply 10 unit loads. The minimum pulse width is 225NS and maximum pulse width is limited only by capacitor leakage (40sec is a typical maximum)

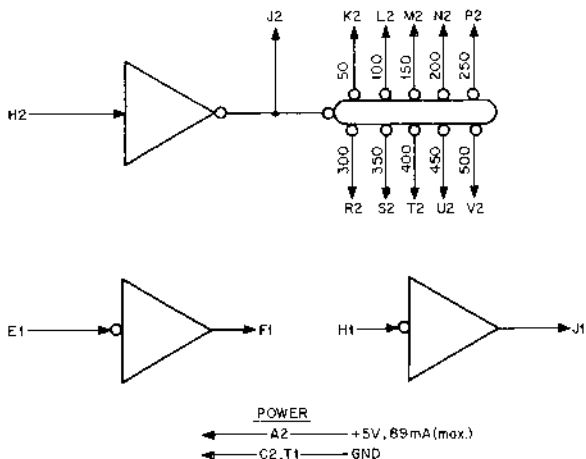
TPD1 = 40NS Max.

POWER: +5Volts at 120mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

DELAY LINE M310

M SERIES



The M310 consists of a tapped delay line with associated circuitry and two pulse amplifiers. The total delay is 500 nanoseconds with taps available at 50 nanosecond intervals.

The time delay is increased when the amplifier is connected to the delay line taps in ascending order as follows: J2, K2, L2, M2, N2, P2, R2, S2, T2, U2, and V2. The tap J2 yielding the minimum delay and the tap V2 yielding the maximum delay.

The pulse amplifiers are intended to be used to standardize the outputs of the delay line. The output of the pulse amplifier is a positive pulse whose duration is typically 50 to 200 nanoseconds. These amplifiers are not intended to be driven by TTL IC logic.

Inputs: Pin H2 represents 2.5 TTL unit load.

Outputs: Pin F1 and J1 outputs can drive 30 unit loads.

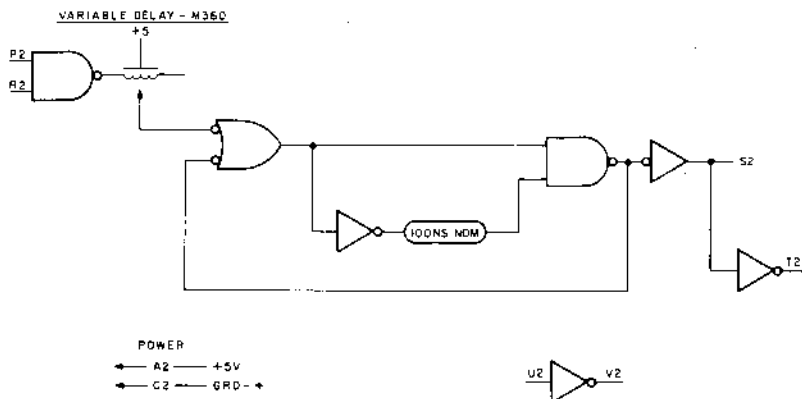
Power: +5 Volts at 89 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

M310 — \$58

VARIABLE DELAY M360

M SERIES



The M360 contains an adjustable delay line with a standardizing amplifier. The delay is adjustable between the limits of 50 nanoseconds to 300 nanoseconds by means of a slotted screw which is accessible from the handle end of the module. The resolution of the delay adjustment is approximately 1 nanosecond. The output consists of a positive pulse whose width is nominally 100 nanoseconds and the leading (positive going voltage) edge of which, is delayed with respect to the leading (positive going voltage) edge of the input by a length of time as determined by the setting of the delay line adjustment.

Inputs: Pins P and R represent one TTL unit load. Pin U represents two TTL unit loads.

Outputs: Pin S can drive 27 TTL unit loads. Pins T and V are outputs consisting of open collector NPN transistors and can sink 30 milliamperes to ground. Voltage applied to Pins T and V must not exceed +20 volts.

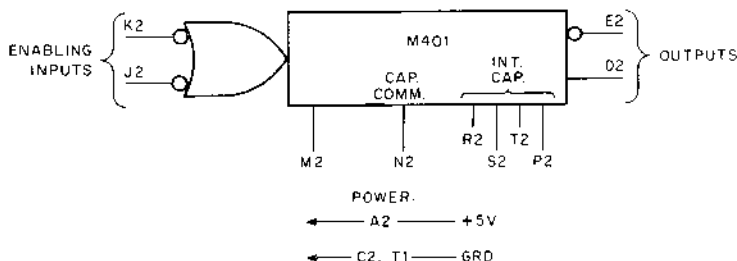
Power: +5 Volts, 50 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

M360 — \$68

VARIABLE CLOCK M401

M SERIES



M401 VARIABLE CLOCK

The M401 Variable Clock is a stable RC-coupled multivibrator which produces standard timing pulses at adjustable repetition rates.

The module is intended for use as the primary source of timing signals in a digital system. Repetition rate is adjustable from 175 HZ to 10 MHz in five ranges. Internal capacitors, selected by jumper pin connections, provide coarse frequency control. An internal potentiometer provides continuously variable adjustment within each range.

A two-input OR gating input is provided for start-stop control of the pulse train. A level change from high to low with fall time less than 400 nsec is required to enable the clock.

Enabling inputs to output E2 is 50 nanoseconds.

Frequency Range	Interconnections Required	
1.5 MHz to 10 MHz	(100 pf)	NONE
175 KHz to 1.75 MHz	(1000 pf)	N2 — R2
17.5 KHz to 175 KHz	(.01 μ fd)	N2 — S2
1.75 KHz to 17.5 KHz	(0.1 μ fd)	N2 — T2
175 Hz to 1.75 KHz	(1.0 μ fd)	N2 — P2

Fine Frequency Adjustment:
Controlled by an internal potentiometer. No provision is made for any external connections.

External capacitor may be added by connection between pin N2 and ground.

The M401 may also be voltage controlled by applying a control voltage to pin M. This feature is available only in M401 modules using printed circuit board revision "E" or later. The voltage applied to Pin M should be limited to the range of 0 Volts to +10.0 Volts. This voltage swing will allow the frequency to be shifted by approximately 30 percent in the frequency range using the internal capacitors of 1.0, 0.1, 0.01 and 0.001 ufd. If the voltage applied to Pin M is D.C. or low frequency (below 1 KHz), Pin M will appear approximately as a -1.0 volt source with a Thevenin resistance of 800 ohms. Modulating the M401 with a 10V P-P signal about a center frequency, as derived by the application of a mean voltage of +5 Volts to Pin M, will yield a typical frequency excursion in excess of $\pm 15\%$ about the center frequency. Typical frequency excursions which may be obtained are shown below:

Voltage applied to Pin M	CAPACITOR			
	1.0 ufd.	0.1 ufd.	0.01 ufd.	.001 ufd.
0	1.000	10.00	100.0	1000
+1	1.054	10.49	104.6	1036
+2	1.101	10.94	109.2	1071
+3	1.147	11.39	113.6	1108
+4	1.193	11.83	118.0	1142
+5	1.238	12.26	122.2	1181
+6	1.282	12.69	126.4	1271
+7	1.325	13.10	130.4	1295
+8	1.368	13.50	134.2	1312
+9	1.408	13.87	137.7	1322
+10	1.443	14.20	140.9	1323

Output frequency
in KHz

Inputs: Each enable input represents 1 unit load. Pin M, refer to text above.

Outputs: The output pulse width is 50 nsec. The positive output can drive 10 unit loads; the negative output, 9 unit loads.

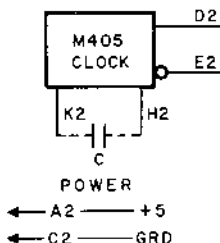
Power: +5 Volts, 80 mA. (max.) using printed circuit board revision "E" or later.

Size: Standard, single height, single width FLIP CHIP module.

M401 — \$55

CRYSTAL CLOCK M405

**M
SERIES**



The M405 clock employs a series resonant crystal oscillator to obtain a frequency stability of .01% of specified value between 0°C and +55°C. The clock frequency may be specified anywhere in the range of 5 KHz to 10 MHz by the customer.

Outputs: Outputs at pins D2 and E2 are respectively positive and negative going 0-+3Volts 50 nsec pulses. Pin D2 can drive 10 unit loads while E2 can drive only 9 unit loads. Pulses at pins D2 and E2 are time shifted by one gate delay with negative pulse at pin E2 leading the positive pulse at D2 by a maximum of 20 nsec. The output pulse width can be modified by the addition of an external capacitor between pins K2 and H2. This capacitor will increase the output pulse width by approximately 1 nsec per 2.5 mmfd of additional capacitance.

Power: +5Volts, 50 mA. (maximum)

Size: Standard, single height, single width FLIP CHIP module.

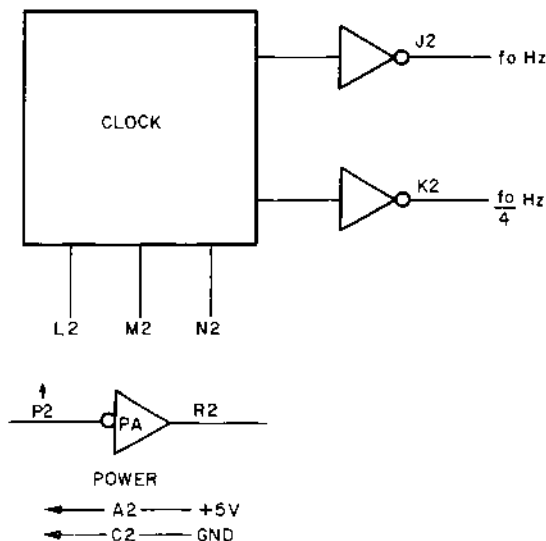
Ordering Information: When ordering the M405 always specify frequency. Allow six weeks for delivery.

Standard Stock Frequencies: 1.333 MHz, 2.000 MHz, 5.000 MHz.

M405 — \$100

REED CLOCK M410

M SERIES



The M410 is a free-running contactless-resonant-reed-tuned clock which provides stable timing signals for a system using the M706 and M707 teletype converter modules. Overall frequency stability of the outputs is better than .1% in the temperature range 0°C-70°C. Available clock frequencies are listed below. A pulse amplifier is provided for the generation of nominal 150 nsec pulses.

Available Frequencies: (f_0 in HZ) = 400 (50 baud), 550, 600 (75 baud), 750, 880 (110 baud), 1200 (150 baud), 1800, 2000, 2200, 2400 (300 baud).

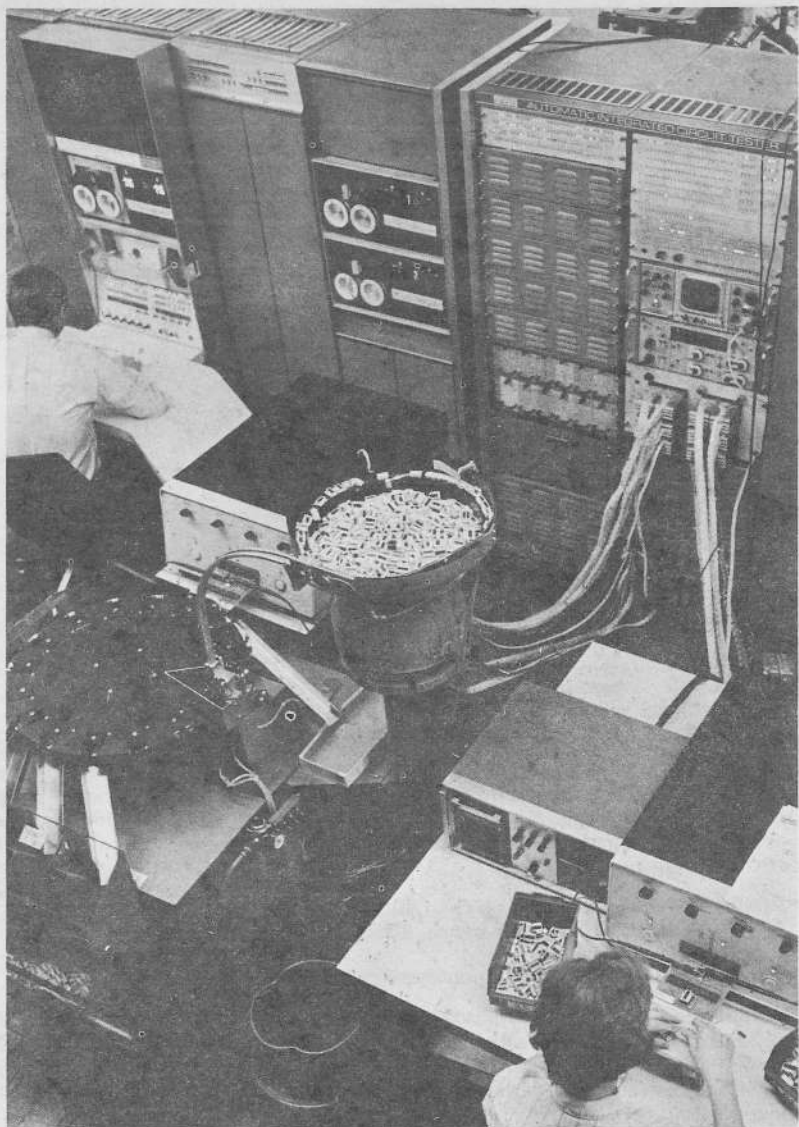
Inputs: The pulse amplifier input presents one unit load.

Outputs: Pin J2 drives 30 unit loads at f_0 . Pins N2 and M2 drive 9 unit loads at $f_0/2$. Pin L2 drives 9 unit loads at $f_0/4$. Pin K2 drives 30 unit loads at $f_0/4$. Pin R2 drives 10 unit loads with a nominal 150 nsec positive output pulse. Under normal operating conditions, pins L2, M2, N2, are used as test points.

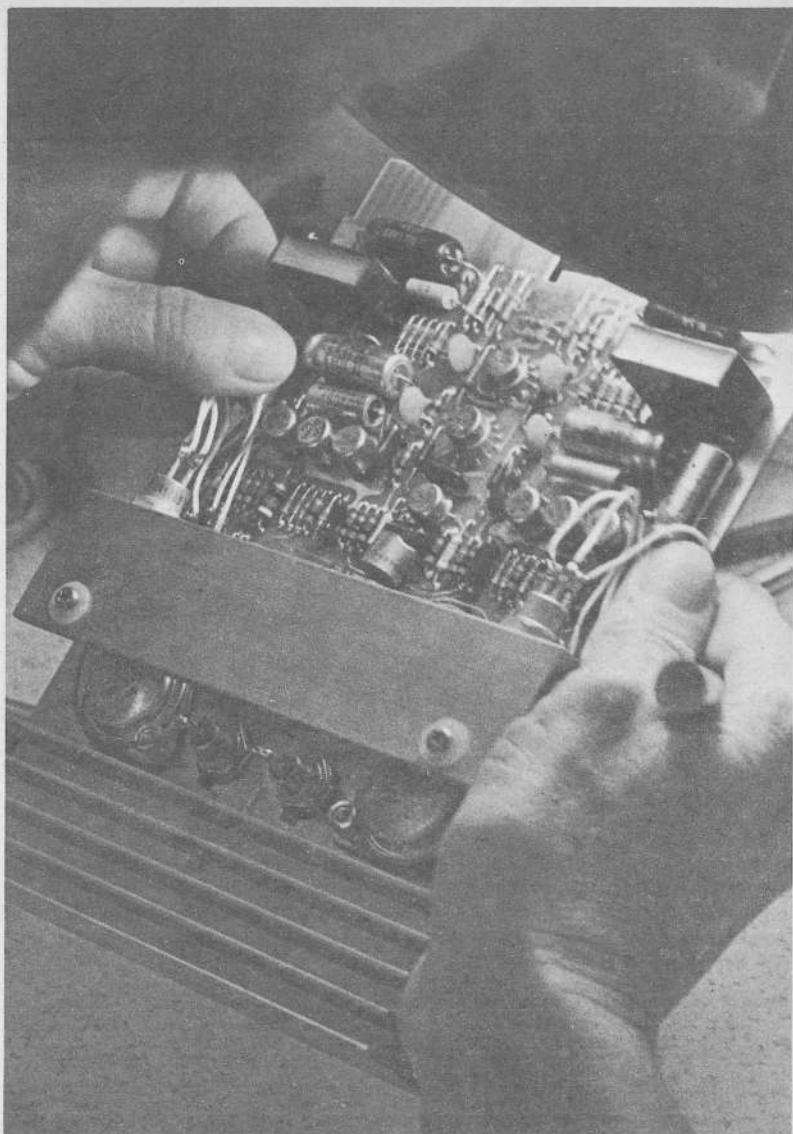
Power: +5 Volts at 95 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

M410 — \$70



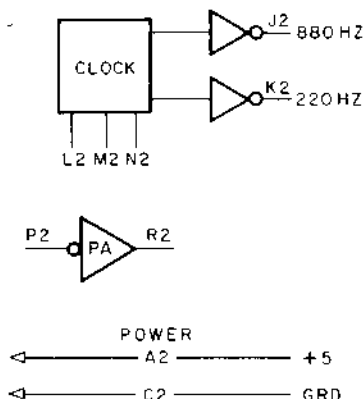
All incoming integrated circuits undergo computer controlled testing, with 40 dc and 16 ac tests performed in 1.1 seconds. This 100% inspection speeds production by minimizing the diagnosis of component failures in module test.



All DEC modules are exhaustively inspected and tested, both visually and electronically. A typical module undergoes a printed circuit board inspection procedure that consists of over 70 individual steps.

VARIABLE CLOCK M452

M
SERIES



The M452 is a free running clock which generates the necessary timing signals for the PDP 8/1 teletype control. Frequency adjustment of this module is limited to less than 5% and the overall clock stability with respect to supply voltage and temperature variations is about 1%. The available output frequencies are 880Hz, and 220Hz. A pulse amplifier is provided for the generation of nominal 150 nsec pulses.

Inputs: The pulse amplifier input presents one unit load.

Outputs: Pin J2 drives 30 unit loads at 880Hz. Pins N2 and M2 drive 9 unit loads at 440Hz. Pin L2 drives 9 unit loads at 220Hz. Pin K2 drives 30 unit loads at 220Hz. Pin R2 drives 10 unit loads with a nominal 150 nsec positive output pulse. Under normal operating conditions, pins L2, M2, N2, are used as test points.

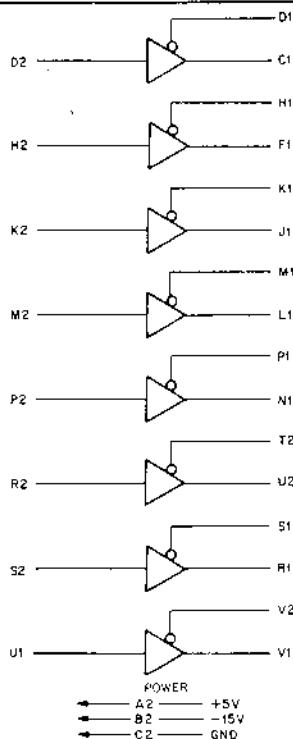
Power: +5 Volts, 77 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

M452 — \$40

**NEGATIVE INPUT POSITIVE
OUTPUT RECEIVER
M500**

**M
SERIES**



The M500 module is used to convert negative input signals to positive output signals. Each card contains 8 converters and is pin compatible with the M510 positive receiver card.

A ground input at D2 will yield a +3 at D1 and ground at C1. The propagation delay is 40 nsec. Do not connect to pin E2 (used for manuf. test only).

Inputs: 1 mA. at ground; 0 mA. at -3 Volts

Input switching level is normally -1.5 Volts. The maximum input voltage is -3 Volts.

Output: Each output is capable of driving 10 unit loads.

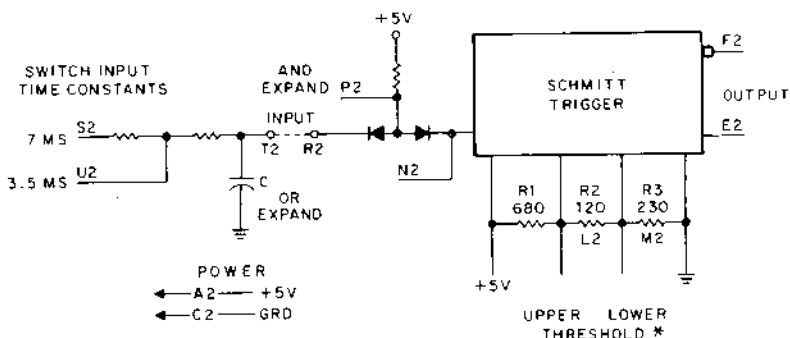
Power: +5 Volts at 160 mA. (max.); -15 Volts at 64 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

M500 — \$55

SCHMITT TRIGGER M501

M SERIES

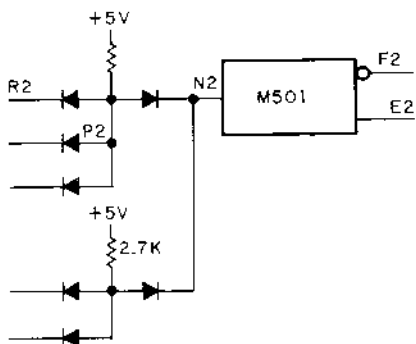


Basically a Schmitt Trigger with variable thresholds, the M501 is used as a Switch Filter, Pulse Shaper and Threshold Detector. Complementary positive logic levels are provided as outputs.

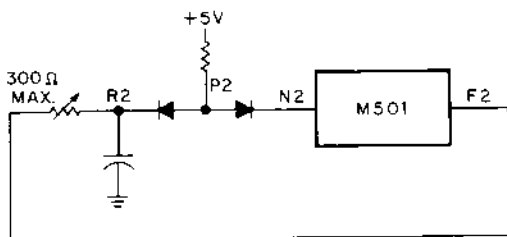
The INPUT on PIN R2 is compared with the thresholds set on PINS L2 and M2, Upper and Lower respectively. AND and OR EXPANSION may be performed on PINS P2 and N2. Module R001 and R002 provide the diodes required. An integrator is provided on the input, allowing SWITCHES to be connected to the Schmitt Trigger with contact bounce effects eliminated. Two switch TIME CONSTANTS are provided. Inputs to PIN S2 result in a 7 m sec TIME CONSTANT, to PIN U2, 3.5 m sec.

The Upper and Lower threshold are preset at 1.7 Volts and 1.1 Volts. They may be modified by the addition of resistor combination in parallel with the internal network. However, the upper threshold must not exceed 2.0 Volts or the lower threshold fall below 0.8 V.

R _x	PARALLEL	R2	—	THRESHOLD CLOSER
R _x	PARALLEL	R1	—	UPPER RISES
R _x	PARALLEL	R3	—	LOWER FALLS



Connecting a resistor from OUTPUT PIN F TO INPUT PIN R with PIN T tied to PIN R forms an oscillator.



Inputs: Input signal swing on PIN R2 is limited to ± 20 Volts.

Input Pin R2: 2.7 K Ω to +5 Volts or 1.8 mA. at ground.

Pin P2—AND EXPAND input

Pin N2—OR EXPAND input

Pin S2—RC SWITCH INPUT Filter 7 msec

Pin U2—RC SWITCH INPUT Filter 3.5 msec

Pin L2, M2—Available for threshold modification.

Outputs: PIN F2 goes to GROUND when the input on PIN R2 rises above the UPPER threshold, having been below the lower threshold.

PIN F2 rises to +3 volts when the input on PIN R2 falls below the LOWER threshold, having been above the upper threshold.

PIN E2 is the complement of the PIN F2.

PIN E2 can drive ten unit loads.

PIN F2 can drive eight unit loads.

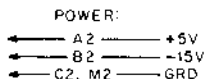
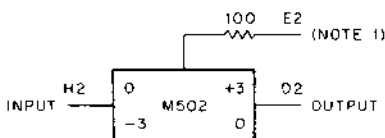
Power: +5 Volts at 31 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

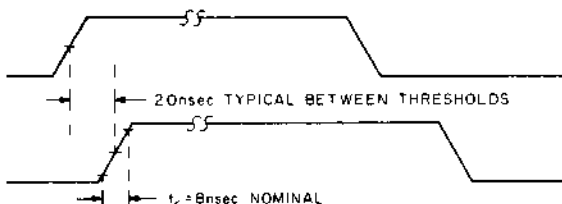
M501 — \$25

HIGH SPEED NEGATIVE INPUT CONVERTER M502

M SERIES



NOTE
1. CONNECT TO OUTPUT WHEN NOT DRIVING 92ohm COAX.



M502 NEGATIVE INPUT CONVERTER

INPUT	OUTPUT
0V	+3V
-3V	0V

The M502 contains two non-inverting high-speed signal converters which interface standard negative (-3V and ground) DIGITAL logic levels or pulses with M and K Series positive logic modules. These converters provide sufficient current drive at a low output impedance for system interconnections by means of terminated 92-ohm coaxial cable. The converters operate at frequencies up to 10 MHz, with typical output rise and fall times of 8 nsec. Propagation times for output rise and fall are typically 20 nsec.

Inputs: Input loading is equivalent to a 3 mA. clamped load.

Outputs: Each output can drive terminated 92-ohm coaxial cable, and supply an additional 30 mA. at +3 Volts or sink an additional 30 mA. at ground. Output rise and fall times depend on the length of coaxial cable driven. When coaxial cable is not driven, switching speeds are increased by connecting the 100 ohm resistor to the output.

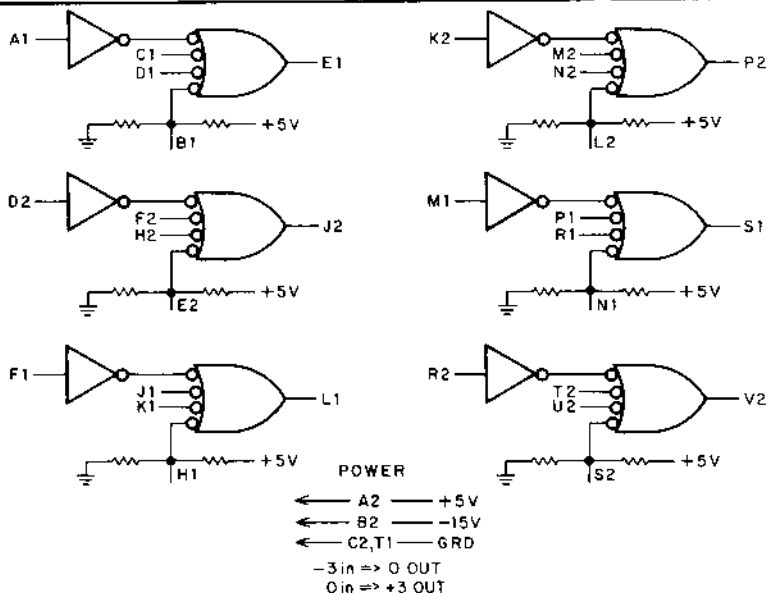
Power: +5 Volts, 49 mA. (max.); -15 Volts, 92 mA. (max.). Add 44 mA. for each 100 ohm resistor connected to outputs.

Size: Standard, single height, single width FLIP CHIP module.

M502 — \$26

MEDIUM SPEED NEGATIVE INPUT CONVERTER M506

M SERIES



The M506 contains six non-inverting signal converters which can be used to interface the negative logic levels or pulses of duration greater than 100 nsec to M and K Series positive logic levels of +3 Volts and ground. These converters operate at frequencies up to 2 MHz with typical rise and fall propagation time of respectively 70 nsec and 40 nsec.

In addition, to the negative level inputs, each converter circuit has three additional NOR inputs for positive logic levels of +3 Volts and ground. One of these inputs is tied to +3 Volts so that unused inputs can be tied to a source of logic 1.

Inputs: All negative level inputs (A1, D2, . . . R2) present a 10 ma. at ground load.

Inputs B1, E2, . . . S2 present five TTL unit loads and can drive seven TTL unit loads at logic 1 if not used as an input.

All other inputs present 1 unit load.

Outputs: Each output can drive 10 TTL unit loads.

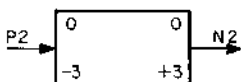
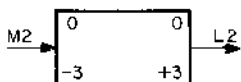
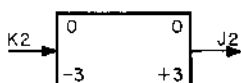
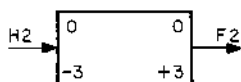
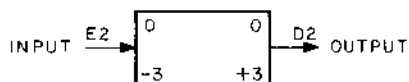
Power: +5V at 81 mA. (max.); -15V at 115 mA. (max.).

Size: Standard, single height, single width FLIP CHIP module.

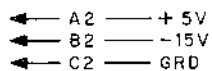
M506 — \$52

BUS CONVERTER M507

M SERIES



POWER



INPUT
GRD
-3V

OUTPUT
GRD
+3V

The M507 contains six inverting level shifters which will accept -3 Volts and GRD as inputs. The input to each level shifter consists of a 10 ma. clamped load and is diode protected against positive voltage excursions.

The output consists of an open collector NPN transistor. The output of each level shifter will sink 100 ma. to GRD. The maximum voltage which may be applied to the output is $+20$ Volts. The output transistor is protected against negative voltage excursions by a diode connected between the collector and GRD. The output rise is delayed by 100 nsec. for pulse spreading.

The principle use of this module is to convert negative voltage logic levels or pulses of duration greater than 100 nsec.

Inputs: Input loading is equivalent to a 3 mA. clamped load.

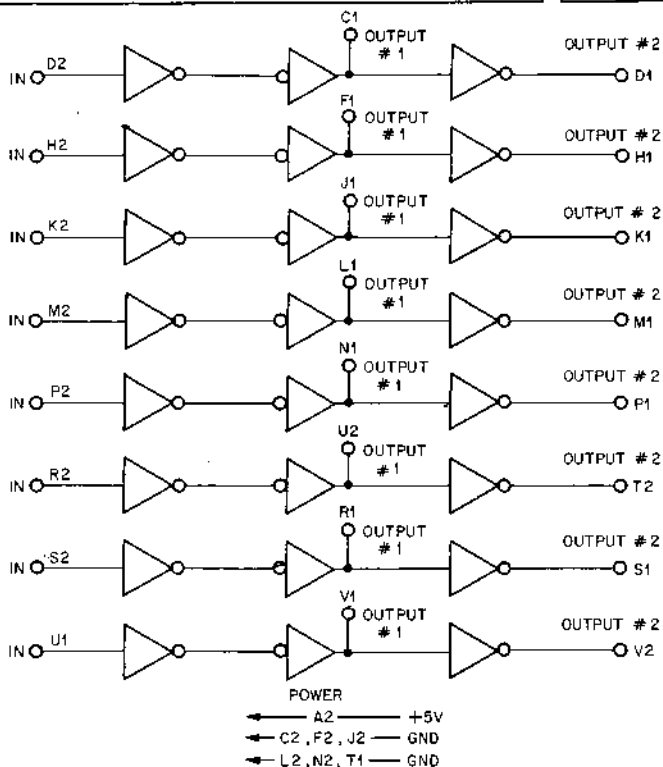
Outputs: Each output can sink 100 ma. to GRD. Maximum voltage applied to any output is $+20$ Volts.

Power: $+5$ Volts, 42 mA. (max.); -15 Volts, 115 mA. (max.).

Size: Standard, single height, single width FLIP CHIP module.

I/O BUS RECEIVER M510

M SERIES



The M510 is a positive input/output receiver card for use with the PDP15. It contains 8 high input impedance circuits of at least 27 K Ω and input switching thresholds of about +1.5 Volts. Each receiver has two outputs, one of the same polarity as the input, the other, the inverse of the input. The receiver card can be used anywhere on the I/O Bus, but power (B+) must be applied at all times, since the input impedance drops to 1 K Ω when power is off. Do not connect to pin E2 (used for manuf. test only).

Inputs: The input impedance is 27 Ω (min.). Each input load current is 80 mA. (max.) and the threshold switching level is 1.4 to 1.6 volts.

Outputs: Output #1 fan out = 9 unit loads. Output #2 fan out = 10 unit loads. Output #2 delay = 50 nsec (from input)

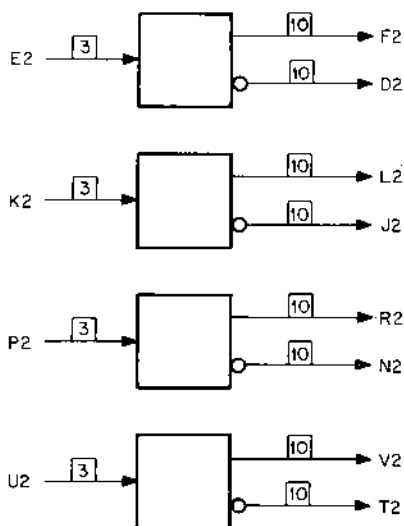
Power: +5 Volts at 170 mA. (max.)

Size: Standard, double height, single width FLIP CHIP module.

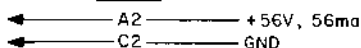
M510 — \$51

K TO M CONVERTER M521

M SERIES



POWER



The M521 K Series to M Series Converter contains four circuits which can convert any K Series input to complementing M Series outputs. Typically a K Series input would have a 7μ sec rise time and a 1.5μ sec fall time, the M521 speeds both those rise and fall times to approximately 15 nsec. Input circuit has built-in hysteresis and is slowed to a maximum frequency of 100 KHz.

Inputs: Each input represents a 3 mA. load.

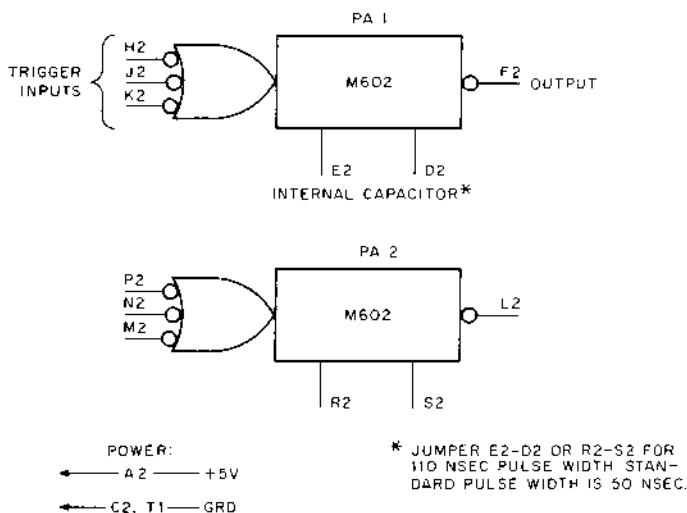
Outputs: Each output is capable of driving 10 unit loads.

Power: 56 mA. maximum current at +5 Volts.

M521—\$16

PULSE AMPLIFIER M602

M SERIES



The M602 contains two pulse amplifiers which provide power amplification, standardize pulses in amplitude and width, and transform level changes into a standard pulse. A negative pulse output is produced when the input is triggered by a transition from high to low. Propagation time between input and output thresholds is 30 nsec maximum. An internal capacitor is brought out to pin connections to permit the standard 50 nsec output pulse to be increased to 110 nsec (nominal). Recovery time is equal to that of the output pulse width. The input must have a fall time (10% to 90% points) of less than 400 nsec and must remain below 0.8 volts for at least 30 nanoseconds. Maximum PRF is 10 MHz.

Inputs: Each input presents $2\frac{1}{2}$ unit loads.

Outputs: Each output is capable of driving 30 unit loads.

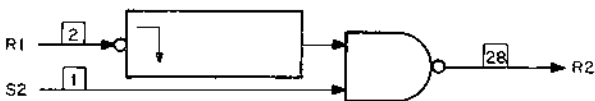
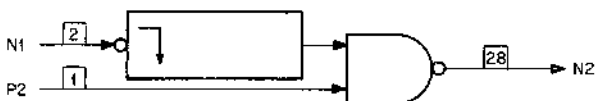
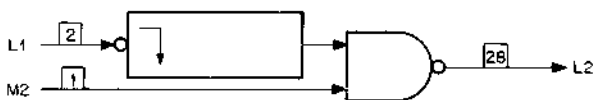
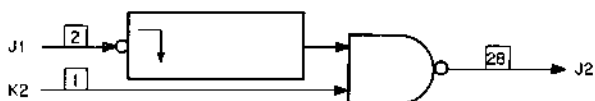
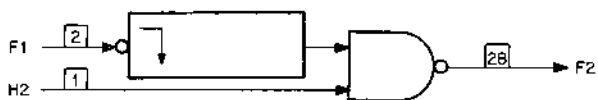
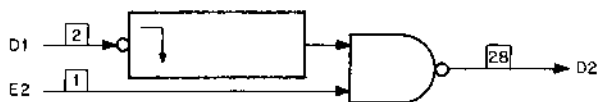
Power: +5 volts, 213 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

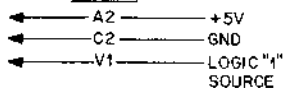
M602 — \$28

PULSE GENERATOR M606

M SERIES



POWER



The M606 contains six pulse generators. Each circuit will produce a pulse to ground upon the application of a level shift from high to low to the input. The time duration of the output pulse will be at least 30 nsec. but no longer than 100 nsec. Each circuit contains an inhibit input. The output will be inhibited when the inhibit input is grounded. If this input is not used, it should be tied to a logic 1 level.

The M606 may be used for setting or clearing of flip-flops by applying the output of the M606 to the direct clear or set inputs of up to 14 flip-flops.

Inputs: Pins D1, F1, J1, N1, and R1 represent two unit loads. Pins E2, H2, K2, M2, P2, and S2 represent one unit load.

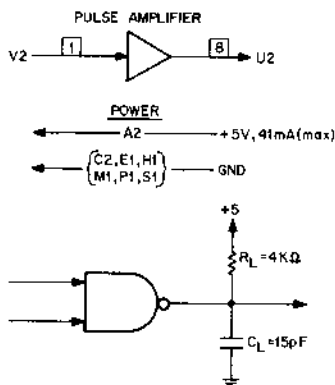
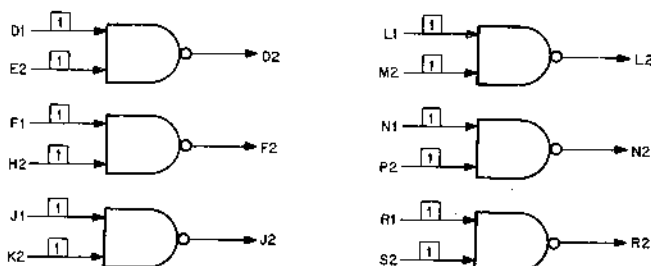
Outputs: All outputs may drive 28 unit loads and consists of a ground level with a time duration of at least 30 nsec. but not greater than 100 nsec. Pin V1 is a source of logic 1 and may supply ten unit loads.

Power: +5 Volts at 188 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

OPEN COLLECTOR TWO-INPUT NAND GATE M610

M SERIES



The M610 contains 8 two-input NAND gates with open collector outputs. It also contains a pulse amplifier which does not have an open collector output.

The NAND gate maximum propagation delay when the output goes from High to Low is 15 nsec. However, when the output goes Low to High the propagation delay depends upon the load impedance. As an example, with the load shown in Figure 2, the maximum propagation delay time from a logic "0" to a logic "1" is 45 nsec.

The pulse amplifier maximum propagation delay is 60 nsec. for both High going and Low going output pulse transitions.

Inputs: Each input presents 1 TTL unit load.

Outputs: D2, F2, J2, L2, N2, R2 are capable of sinking 16mA to ground. U2 can drive 8 TTL unit loads.

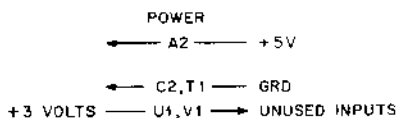
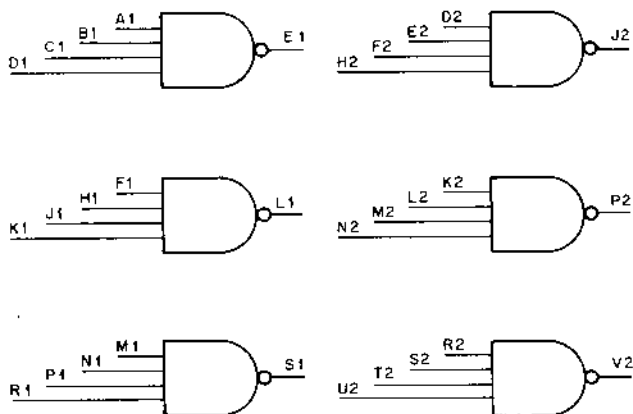
Power: +5V, 41mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

M610—\$20

FOUR-INPUT POWER NAND GATE M617

M SERIES



M617 POWER NAND GATE

The M617 contains 6 four-input NAND gates each capable of driving up to 30 unit loads. Typical gate propagation delay is 15 nsec. Physical configuration and logical operation are identical to the M117.

Inputs: Each input presents 1 unit load.

Outputs: Each output is capable of driving 30 unit loads.

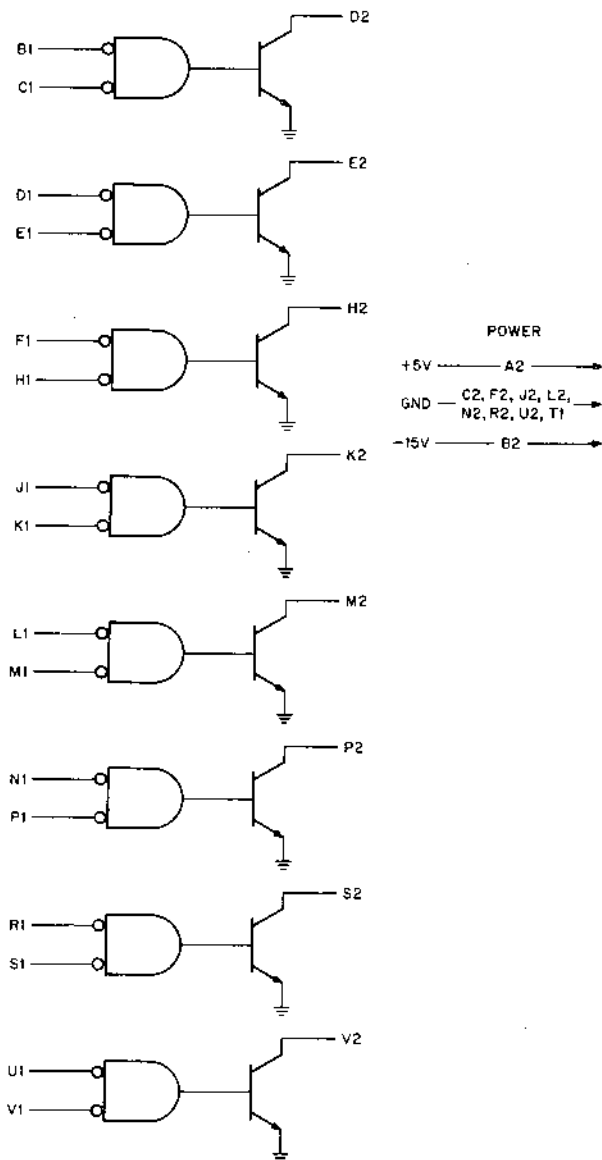
Power: +5 Volts, 97 mA. (max.).

Size: Standard, single height, single width FLIP CHIP module.

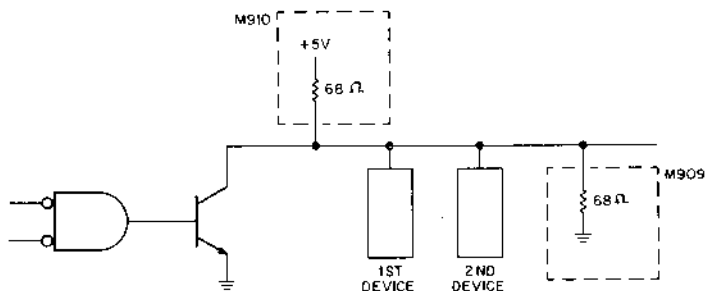
M617 — \$26

**EIGHT BIT POSITIVE INPUT/OUTPUT
BUS DRIVER
M622**

**M
SERIES**



The M622 contains eight two input AND gate bus drivers for convenient driving of the positive input bus of the PDP-15. The output consists of an open collector NPN transistor.



Pull up resistors of 68Ω to +5.0 Volts (supplied on M910) must be tied to the output and the last device should terminate all lines to ground with a 68Ω resistor (supplied on M909).

Inputs: Each input presents 1.25 TTL unit loads.

Outputs: The maximum voltage applied to the output transistor must not exceed +20 Volts and the collector current must not exceed 100 mA. The propagation time is 25 nsec.

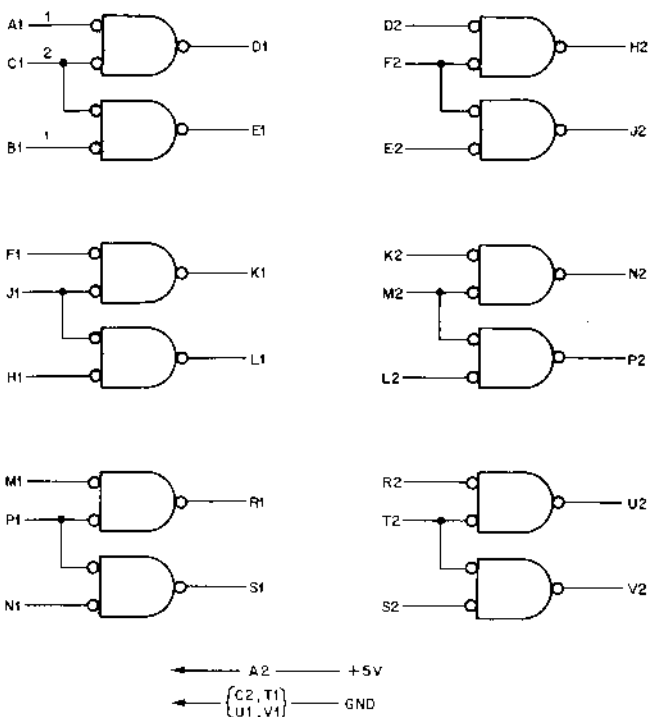
Power: +5 Volts, 210 mA. (max.) excluding output current.

Size: Standard, single height, single width FLIP CHIP module.

M622 -- \$45

BUS DRIVER M623

M SERIES



The M623 contains twelve two input AND gate bus drivers for convenient driving of the positive input bus of either the PDP-8/I or PDP-8/L. Each driver can sink 100 mA. at ground and allows a maximum output voltage of +20 Volts. The output consists of an open collector NPN transistor.

Inputs: Input levels are standard TTL levels of 0 Volts and +2.4 Volts. Data inputs A1, B1, F1, H1, M1, N1, D2, E2, K2, L2, R2, and S2 each present one TTL unit load. All other inputs present two unit loads.

Outputs: A driver output will be at ground when both inputs are at ground. Output rise and fall (TTT) are typically 30 nsec when a 100 mA. resistive load is connected to a driver output. Output voltage must not exceed +20 Volts.

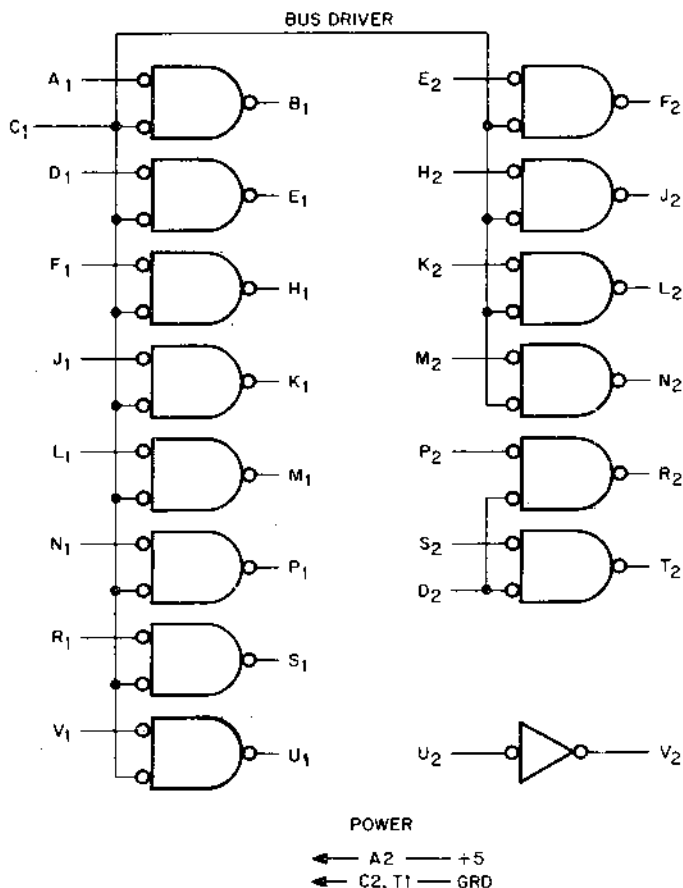
Power: +5 Volts, 71 mA. (max.) plus external load.

Size: Standard, single height, single width FLIP CHIP module.

M623 — \$40

BUS DRIVER M624

M SERIES



The M624 contains fifteen bus drivers intended for convenient driving of the positive input bus of either the PDP-8I or PDP-8L. Twelve of the drivers have a common gate line and would be used for DATA. There are three additional drivers, two of which share a common gate line and the third without a gate line. These three additional drivers were intended to accommodate the functions of "Program Interrupt", "IO Skip" and "Clear AC".

Inputs: Pin C1 presents 12 TTL unit loads.
Pin D2 and U2 present two unit loads.
All other input pins present one unit load.

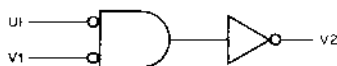
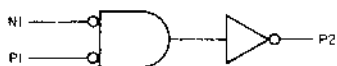
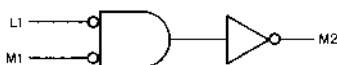
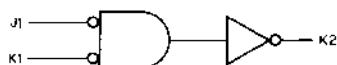
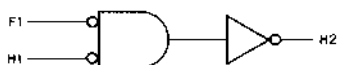
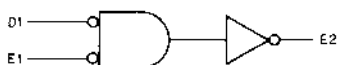
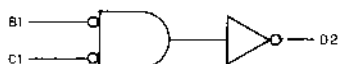
Outputs: All outputs can sink 100 ma. to ground. Voltage applied to the output should be equal to or less than +20 Volts. The output consists of an open collector NPN transistor. Output rise and fall TTT are typically 30 nanoseconds when a 100 mA. resistive load to +5.0 Volts is connected to a driver output.

Power: +5 Volts, 89 mA. (max.). (Driver outputs not connected).

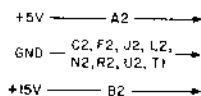
Size: Standard, single height, single width FLIP CHIP module.

**POSITIVE INPUT NEGATIVE OUTPUT
BUS DRIVER
M632**

**M
SERIES**



POWER



The M632 contains eight, two input AND gate bus drivers for convenient driving of the negative bus.

Inputs: Each input presents 1.25 TTL unit loads.

Outputs: The output is internally clamped to keep it between - 3 Volts and ground. The output current must not exceed 100 mA.

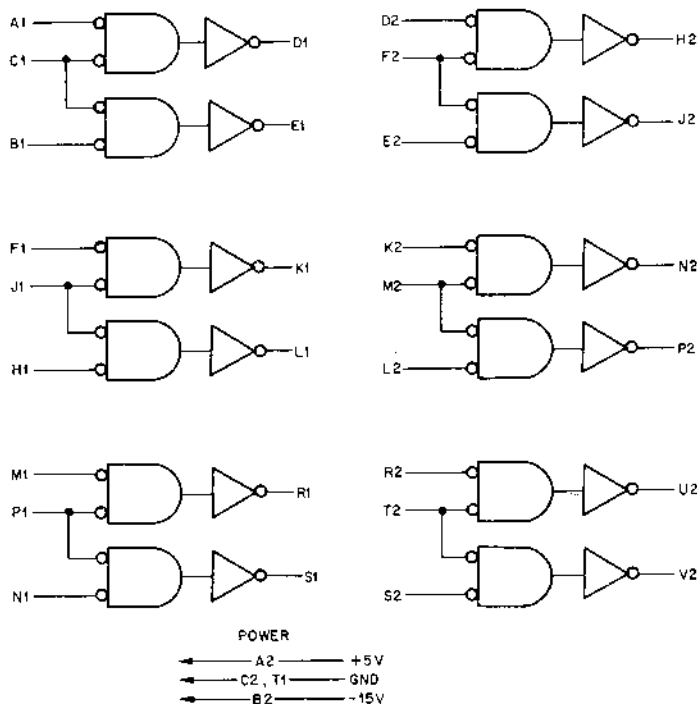
The propagation delay is 50 nsec. (Max.)

Power: +5 Volts, 175 mA. (max.); -15 Volts, 40 mA. (max.), excluding output current

Size: Standard, single height, single width FLIP CHIP module.

NEGATIVE BUS DRIVER M633

M SERIES



The M633 contains twelve bus drivers intended for convenient driving of the negative bus of the PDP-8, PDP-8/i. Each driver consists of an open collector PNP transistor. It is pin compatible with the M623 positive voltage bus driver.

Inputs: Input levels are standard TTL levels. Data inputs A1, B1, F1, H1, M1, N1, D2, E2, K2, L2, R2 and S2. Each present one TTL unit load. All other inputs represent two unit loads.

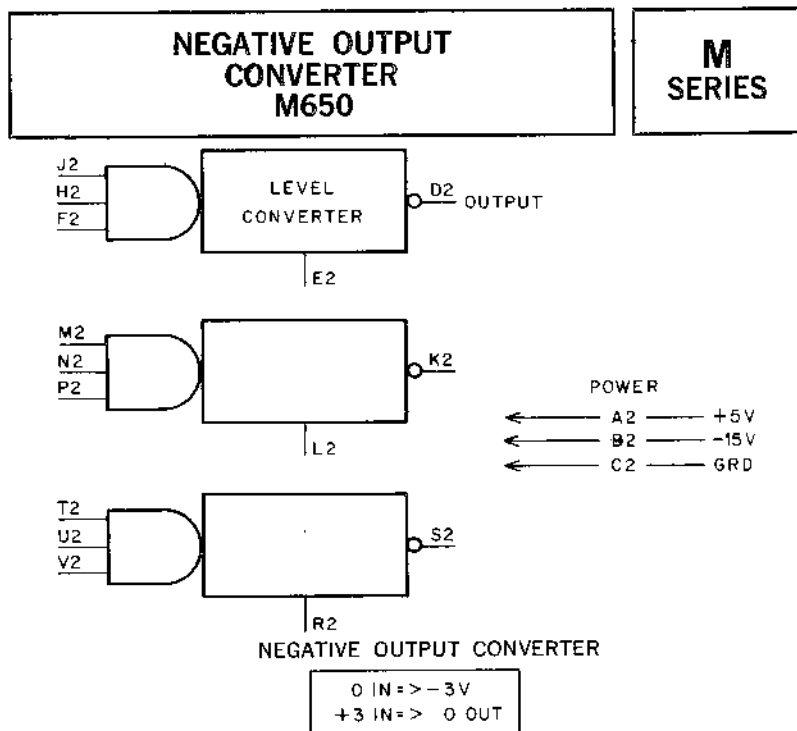
Outputs: Open collector PNP transistor capable of supplying 20 mA. from ground. Voltage applied to the output should not exceed -6 Volts.

Conversion: Logic Diagram: An active voltage is a True State, i.e., -3 V. or +3 V. = "1.". A ground is a True State. Grounded inputs will yield grounded outputs.

Propagation Delay: 40 nsec. typ.

Power: +5 Volts at 100 mA. (max.); -15 Volts at 40 ma. (max.)

Size: Standard, single height, single width FLIP CHIP module.



The M650 contains three non-inverting signal converters which can be used to interface the positive logic levels or pulses (of duration greater than 100 nsec) of K and M series to DIGITAL negative logic levels of -3 Volts and ground. These converters provide current drive at a low output impedance so that unterminated cables or wires can be driven with a minimum of ringing and reflections.

The converters operate at frequencies up to 2 Mc with maximum rise and fall total transition of respectively 75 nsec and 115 nsec. By grounding pin E2 (L2 or R2) the rise and fall total transition times can be increased to avoid ringing on exceptionally long lines. The converter then operates at frequencies up to 500 KHz with typical rise and fall total transition times of 500 nsec.

A positive AND condition at the input gate produces a ground output. If any input is at ground the converter output is at -3 Volts.

Inputs: Each input presents 1 unit load.

Outputs: Each output is capable of driving 20 mA. at ground and at -3 Volts.

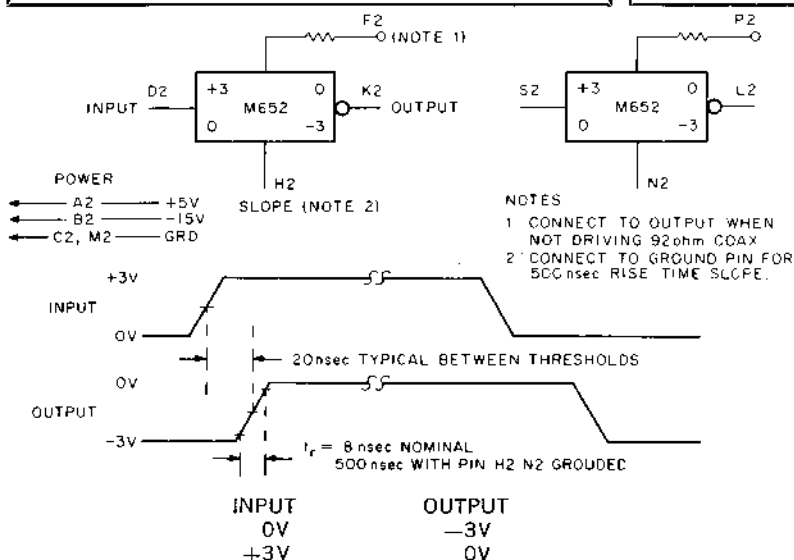
Power: +5 Volts, 37 mA. (max.); -15 Volts, 29mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

M650 — \$25

NEGATIVE OUTPUT CONVERTER M652

M SERIES



The M652 contains two non-inverting high-speed signal converters which can be used to interface the positive logic levels or pulses of the K and M Series to DIGITAL negative logic levels of -3 Volts and ground. These converters provide current drive at a low output impedance so that system interconnections can be made using terminated 92-ohm coaxial cable. The converters operate at frequencies up to 10 MHz with typical output rise and fall times of 8 nsec. Propagation times for output rise and fall are typically 20 nsec. The slope of the output transition can be decreased by grounding an internal RC network, to avoid ringing on exceptionally long lines. The converter then operates at frequencies up to 1 MHz.

Inputs: Positive logic levels of 0 and +3 Volts (nominal). Input loading is 2 unit loads. Input signals more positive than +6 Volts will damage the circuit.

Outputs: Each output can drive terminated 92 ohm coaxial cable and supply an additional 20 mA. at ground or sink an additional 20 mA. at -3 Volts. Output rise and fall times are dependent on the length of coaxial cable driven. When coaxial cable is not driven, switching speeds will be increased by connecting the 100-ohm resistor to the output.

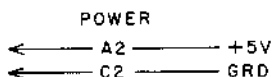
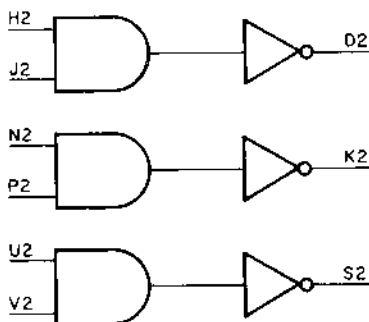
Power: +5 Volts, 122 mA. (max.); -15 Volts, 202 Volts(max.)

Size: Standard, single height, single width FLIP CHIP module.

M652 — \$26

POSITIVE LEVEL DRIVER M660

M SERIES



<p>+ 3 IN => 0 OUT 0 IN => +3 OUT</p>

The M660 Cable Driver consists of three circuits each of which will drive 100 ohm terminated cable with M Series levels or pulses whose duration is greater than 100 nsec.

Inputs: Each input represents 1 unit load.

Outputs: M Series logic levels with 50 mA. drive current at logic "1" or "0".

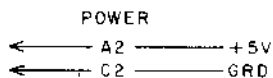
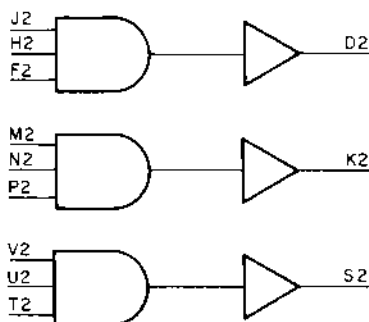
Power: +5V, 71 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

M660 — \$25

**POSITIVE LEVEL DRIVER
M661**

**M
SERIES**



+3 IN => +3 OUT
0 IN => 0 OUT

The M661 contains three circuits which may be used to drive low impedance unterminated cable with M Series logic levels or pulses whose duration is 100 nsec or greater.

Inputs: Each input represents 1 unit load.

Outputs: M Series logic "1" at 5 mA.
M Series logic "0" at 20 mA.

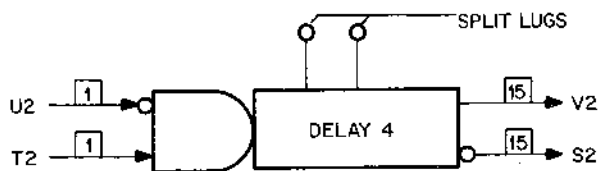
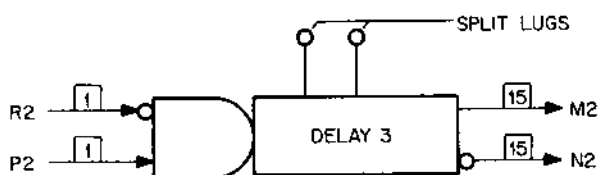
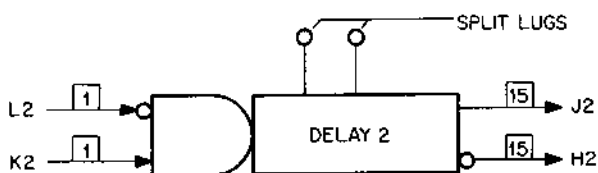
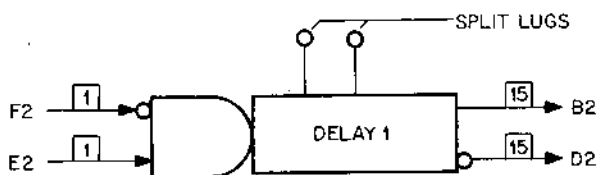
Power: +5V, 111 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

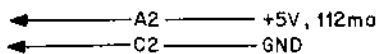
M661 — \$15.

M TO K CONVERTER M671

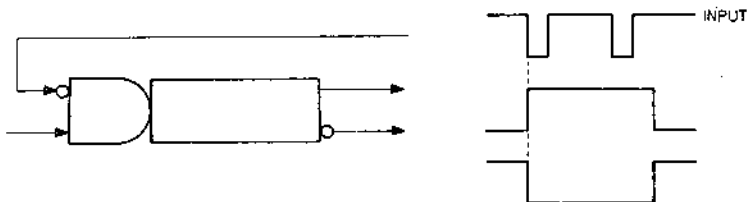
M SERIES



POWER



The M671 M Series to K Series Converter contains four pulse stretching circuits which can convert any M Series input, longer than 50 nanoseconds, to complimentary K Series output pulses of 10 to 15 microseconds in length. Non-Electrolytic capacitors can be connected to the split lugs provided in each circuit, if longer K Series output pulse widths are desired. Pulses of up to 40 seconds in length are possible using this technique. When capacitance is added, the output pulse width is increased by $6400 C$ seconds where C is the capacitance added.



This circuit is insensitive to input transitions during its timeout period as shown in the example above.

Inputs: Each input represents one unit load

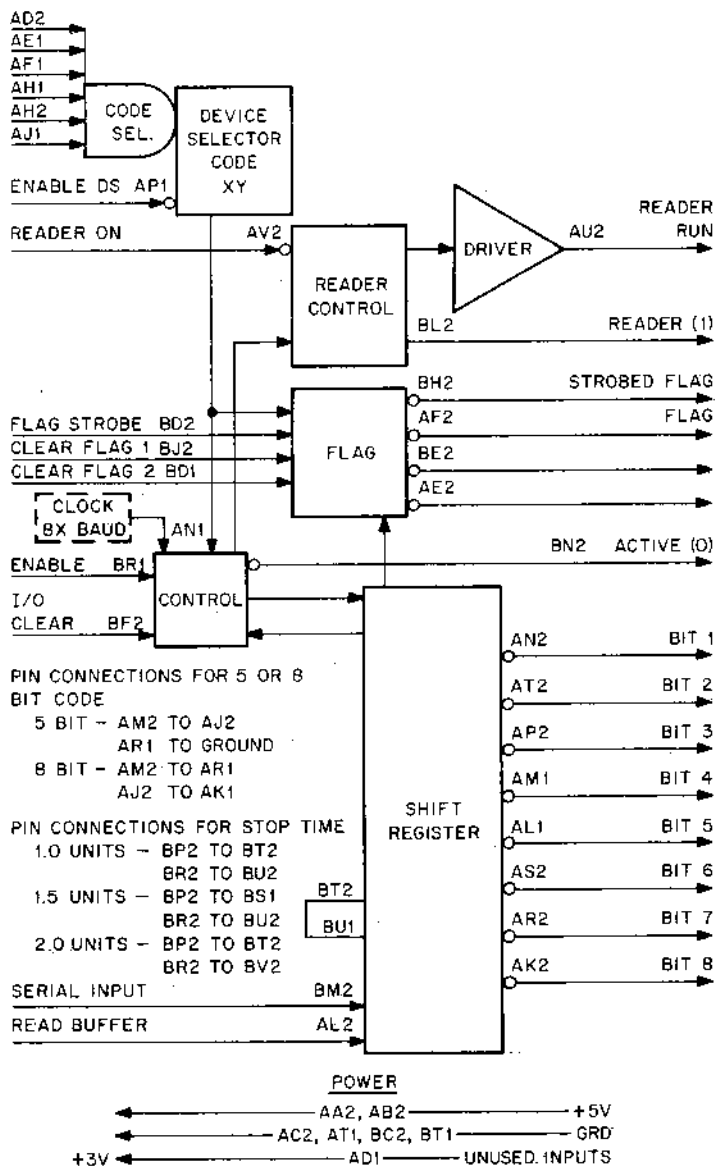
Outputs: Each output is capable of driving 15 mA. of load

Power: +5V at 112 mA.

Size: Standard, single height, single width FLIP CHIP module.

TELETYPE RECEIVER M706

M SERIES



The M706 Teletype Receiver is a serial-to-parallel teletype code converter self contained on a double height module. This module includes all of the serial-to-parallel conversion, buffering, gating, and timing (excluding only an external clock necessary to transfer information in an asynchronous manner between a serial data line or teletype device and a parallel binary device). Either a 5-bit serial character consisting of 7.0, 7.5, or 8.0 units or an 8-bit serial character of 10.0, 10.5, or 11.0 units can be assembled into parallel form by the M706 through the use of different pin connections on the module. When conversion is complete, the start and stop bits accompanying the serial character are removed. The serial character is expected to be received with the start bit first, followed by bits 1 through 8 in that order, and completed by the stop bits. Coincident with reception of the center of bit eight, the Flag output goes low indicating that a new character is ready for transmission into the parallel device. The parallel data is available at the Bit 1 through Bit 8 outputs until the beginning of the start bit of a new serial character as received on the serial input. See the timing diagram of Figure 1 for additional information.

In addition to the above listed features, the M706 includes the necessary logic to provide rejection of spurious start bits less than one-half unit long, and half-duplex system operation in conjunction with the M707. Device selector gating is also provided so that this module can be used on the positive I/O bus of either the PDP8/I or the PDP8/L. To obtain additional applications information on the M706, write for Applications Note AP-M-013.

Inputs: All inputs present one TTL unit load except where noted. When input pulses are required, they must have a width of 50 nsec or greater.

Clock: The clock frequency must be eight times the serial input bit rate (baud rate). This input can be either pulses or a square wave. Input loading on the clock line is three unit loads.

Enable: This input when brought to ground will inhibit reception of new characters. It can be grounded any time during character reception, but returned high only between the time the Flag output goes to ground and a new character start bit is received at the serial input. When not used this input should be tied to a source of +3 Volts.

I/O Clear: A high level or positive pulse at this input clears the Flag and initializes the state of the control. When not used, or during reception, this input should be at ground.

Code Select Inputs: When a positive AND condition occurs at these inputs the following signals can assume their normal control functions—Flag Strobe, Read Buffer, and Clear Flag 1. Frequently these inputs might be used to multiplex receiver modules when a signal like Read Buffer is common to many modules. The inputs can also be used for device Selector inputs when the M706 is used on the positive I/O bus of the PDP8/I or PDP8/L. The code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If it is desired to bypass the code select inputs, they can be left open and the Enable D.S. line tied to ground.

Clear Flag 1: A high level or positive pulse at this input while the code select inputs are all high, will clear the Flag. When not used, this line should be grounded. Propagation delay from input rise until the Flag is cleared is a maximum of 100 nsec. The Flag cannot be set if this input is held high.

Clear Flag 2: A high level or positive pulse at this input, independent of the state of the code select inputs, will clear the Flag. All other characteristics are identical to those of Clear Flag 1.

Flag Strobe: If the Flag is set, and the code select inputs are all high, a positive pulse at this input will generate a negative going pulse at the Strobed Flag output. Propagation delay from the strobe to output is a maximum of 30 nsec.

Read Buffer: A high level or positive pulse at this input while the code select inputs are all high will transfer the state of the shift register to outputs Bit 1 through Bit 8. Final parallel character data can be read by this input as soon as the Flag output goes to ground. Output data will be available a maximum of 100 nsec after the rising edge of this input. See the timing diagram of Figure 1 for additional information.

Reader On: A low level or ground at this input will turn the internal reader flip-flop on. This element is turned off at the beginning of a received character start bit. This input can also be pulsed by tying it to one of the signals derived at output pins AE2 or BE2. A low output will exist at pin BE2 if the M706 is addressed and the clear Flag 1 (pin BJ2) is high. A low output will exist at pin AE2 if the M706 is addressed and the Clear Flag 1 (pin BJ2) is high or if Clear Flag 2 (pin BD1) is high.

Serial Input: Serial data received on this input is expected to have a logical zero (space) equal to +3 Volts and a logical 1 (mark) of ground. The input receiver on the M706 is a schmitt trigger with hysteresis thresholds of nominally 1.0 and 1.7 Volts so that serial input data can be filtered up to 10% of bit width on each transition to remove noise. This input is diode protected from voltage overshoot above +5.9 Volts and undershoot below -0.9 Volts. Input loading is four unit loads.

Outputs: All outputs can drive ten unit loads unless otherwise specified.

Bits 1 through 8: A read Buffer input signal will transfer the present shift register contents to these outputs with a received logical 1 appearing as a ground output. If the Read Buffer input is not present, all outputs are at logical 1. When the M706 is used for reception of 5-bit character codes, the output data will appear on output lines Bit 1 through 5 and bits 6, 7, 8 will have received logical zeros.

Active (0): This output goes low at the beginning of the start bit of each received character and returns high at the completion of reception of bit 8 for an 8-bit character or of bit 5 for a 5-bit character. Since this signal uses from ground to +3 Volts one-half bit time after the Flag output goes to ground, it can be used to clear the flag through Clear Flag 2 input while the Flag Output after being inverted can strobe parallel data out when connected to Read Buffer.

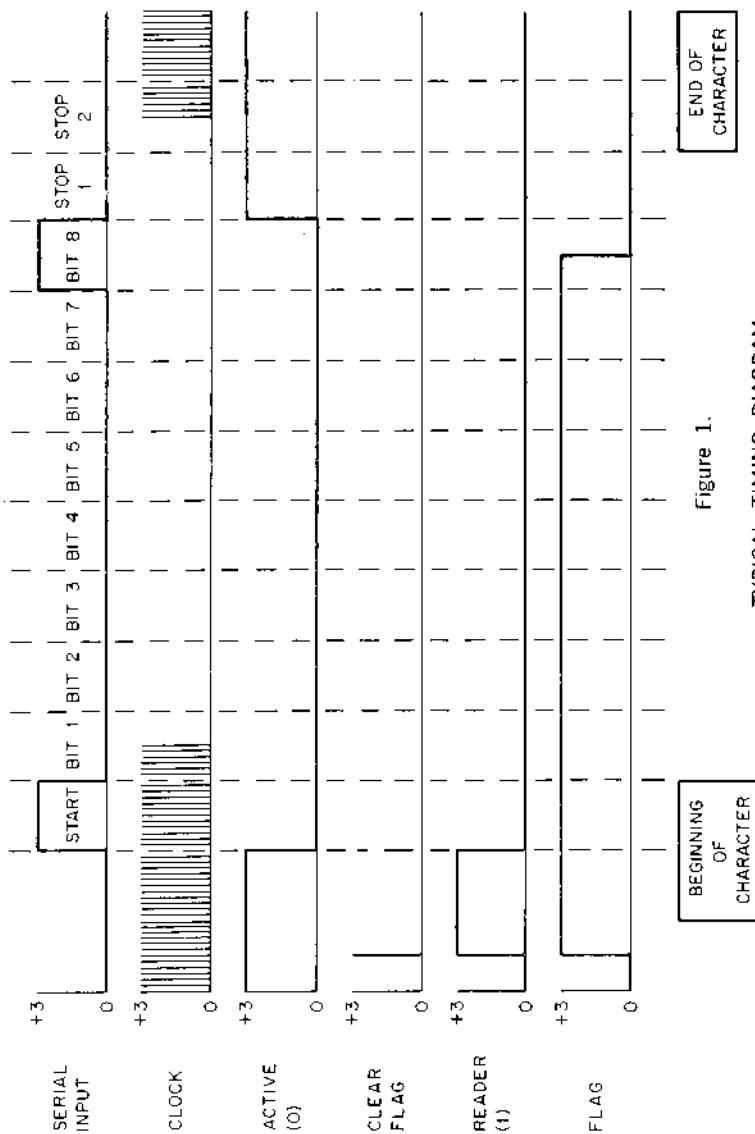


Figure 1.

TYPICAL TIMING DIAGRAM

Serial Input-Parallel Output 8-Bit (01, 111, 111)-2 Unit Stop Time

If an M706 and M707 are to be used in half duplex mode, this output should be tied to the Wait input of the M707 to inhibit M707 transmission during M706 reception. Output drive is eight unit loads.

Flag: This output falls from +3 Volts to ground when the serial character data has been fully converted to parallel form. Relative to serial bit positions, this time occurs during the center of either bit 8 or bit 5 depending respectively on the character length. If the M706 is receiving at a maximum character rate, i.e. one character immediately follows another; the parallel output data is available for transfer from the time the Flag output falls to ground until the beginning of a new start bit. This is Stop bit time plus one-half bit time.

Strobed Flag: This output is the NAND realization of the inverted Flag output and Flag Strobe.

Reader (1): Whenever the internal reader flip-flop is set by the Reader ON input, this output rises to +3 Volts. It is cleared whenever a start bit of a new character received on the serial input.

Reader Run: For use with Digital modified ASR33 and ASR35 teletypes which have relay controlled paper tape readers. This output can drive a 20 ma at +0.7 Volts load. The common end of the load can be returned to any negative voltage not exceeding -20 Volts.

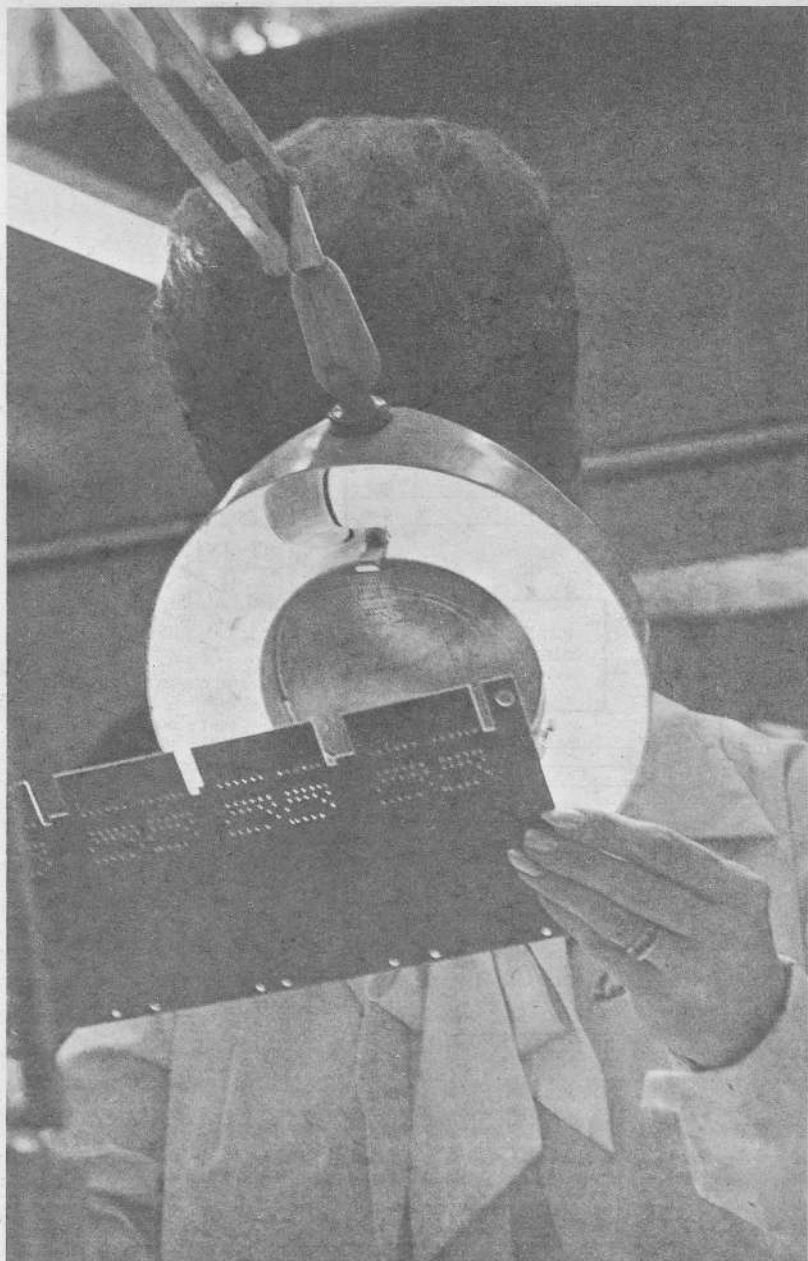
Pin AE2: This output is the logical realization of NOT (Clear Flag 1 or Clear Flag 2 or I/O Clear) and is a +3 Volts to ground output level or pulse depending on the input. This signal can be used to pulse Reader On for control of Reader Run as used in DEC PDP8/I or PDP8/L computers.

Pin BE2: This output is brought from +3 Volts to ground by an enabled Clear Flag 1 input. It can be connected to Reader On for a different form of control of Reader Run.

+3 Volts: Pin AD1 can drive ten unit loads at a +3 Volt level.

Power: +5 Volts at 400 mA. (max.).

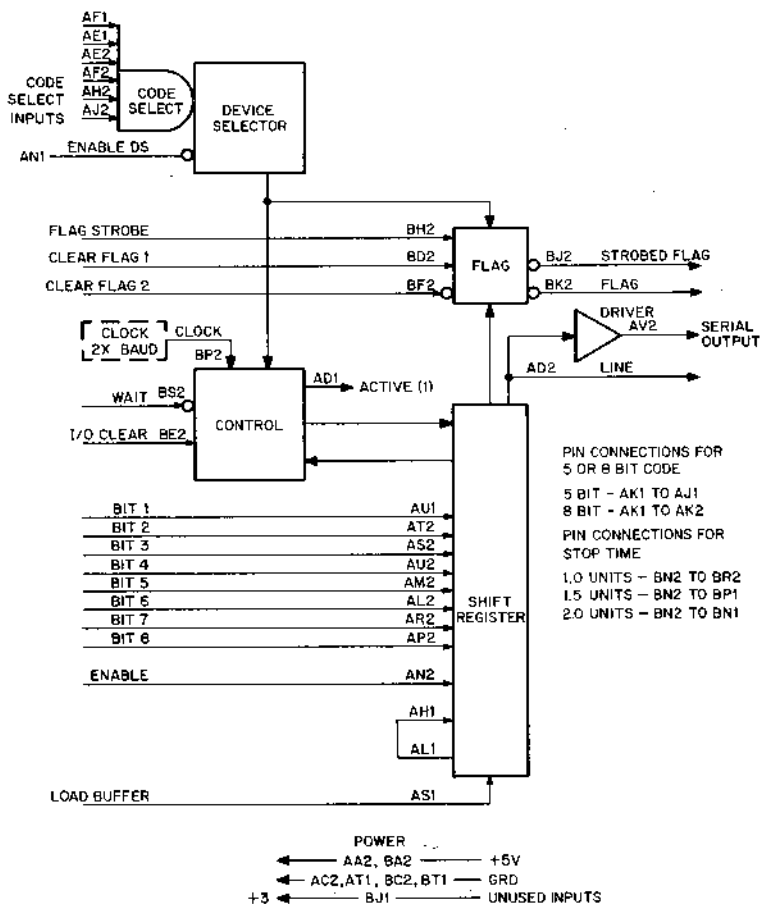
Size: Standard, double height, single width FLIP CHIP module.



Quality of plated-thru holes is checked in our new electrochemical facility before boards go to the module assembly area.

TELETYPE TRANSMITTER M707

M SERIES



The M707 Teletype Transmitter is a parallel-to-serial teletype code converter self contained on a double height module. This module includes all of the parallel-to-serial conversion, buffering, gating, and timing (excluding only an external clock) necessary to transfer information in an asynchronous manner between a parallel binary device and a serial data line or teletype device. Either a 5-bit or an 8-bit parallel character can be assembled into a 7.0, 7.5, or 8.0 unit serial character or a 10.0, 10.5, or 11.0 unit serial character by the M707 through the use of different pin connections on the module. When conversion is complete, the necessary start bit and selected stop bits (1.0, 1.5, or 2.0 units) have been added to the original parallel character and transmitted over the serial line. The serial character is transmitted with the start bit first, followed by bits 1 through 8 in that order, and completed by the stop bits. Coincident with the stop bit being put on the serial line, the Flag output goes low indicating that the previous character has been transmitted and a new parallel character can be loaded into the M707. Transmission of this new character will not occur until the stop bits from the previous character are completed. See the timing diagram of Figure 1 for additional information.

In addition to the above listed features, the M707 includes the necessary gating so that it can be used in a half-duplex system with the M706. Device selector gating is also provided so that this module can be used on the positive bus of either the PDP8/I or the PDP8/L. To obtain additional applications information on the M707 write for Applications Note AP-M-013.

Inputs: All inputs present one TTL unit load with the exception of the Clock input which presents ten unit loads. Where the use of input pulses is required, they must have width of 50 nsec or greater.

Clock: The clock frequency must be twice the serial output bit rate. This input can be either pulses or a square wave.

Bits 1 through 8: A high level at these inputs is reflected as a logic 1 or mark in the serial output. When a 5-bit code is used, bit inputs 1 through 5 should contain the parallel data, bit 6 should be considered as an Enable, and bits 7, 8 and Enable should be grounded.

Enable: This input provides the control flexibility necessary for transmitter multiplexing. When grounded during a Load Buffer pulse, this input prevents transmission of a character. It can be driven from the output of an M161 for scanning purposes or in the case of a single transmitter, simply tied to +3 Volts.

Wait: If this input is grounded prior to the stop bits of a transmitted character, it will hold transmission of a succeeding character until it is brought to a high level. A ground on this line will not prevent a new character from being loaded into the shift register. This line is normally connected to Active (0) on a M706 in half duplex two wire systems. When not used, this line should be tied to +3 Volts.

Code Select Inputs: When a positive AND condition occurs at these inputs the following signals can assume their normal control functions—Flag Strobe, Load Buffer, and Clear Flag 1. Frequently these inputs might be used to multiplex transmitter modules when signals like Load Buffer are common to many modules. These inputs can also be used for device selector inputs when the M707 is used on the positive bus of the PDP8/I or PDP8/L. The

code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If it is desired to by-pass the code select inputs, they can be left open and the Enable DS line tied to ground.

Clear Flag 1: A high level or positive pulse at this input while the code select inputs are all high, will clear the Flag. When not used, this line should be grounded. Propagation delay from input rise until the Flag is cleared at the Flag output is a maximum of 100 nsec. The Flag cannot be set if this input is held at logic 1.

Clear Flag 2: A low level or negative pulse at this input will clear the Flag. When not used this input should be tied to +3 Volts. The Flag will remain cleared if this input is grounded. Propagation from input fall to Flag output rise is a maximum of 80 nsec. If it is desired to clear the flag on a load buffer pulse, Clear Flag 2 can be tied to pin AR1 of the module.

Flag Strobe: If the Flag is set, and the code select inputs are all high, a positive pulse at this input will generate a negative going pulse at the Strobed Flag output. Propagation delay from the strobe to output is a maximum of 30 nsec.

I/O Clear: A high level or positive pulse at this input clears the Flag, clears the shift register and initializes the state of the control. This signal is not necessary if the first serial character transmitted after power turn-on need not be correct. When not used, or during transmission, this input should be at ground.

Load Buffer: A high level or positive pulse at this input while the code select inputs are all high will load the shift register buffer with the character to be transmitted. If the Enable input is high when this input occurs, transmission will begin as soon as the stop bits from the previous character are counted out. If a level is used, it must be returned to ground within one bit time (twice the period of the clock).

Outputs: All outputs present TTL logic levels except the serial output driver which is an open collector PNP transistor with emitter returned to +5 Volts.

Serial Output: This open collector PNP transistor output can drive 20 mA into any load returned to a voltage between +4 Volts and -15 Volts. A logical output or mark is +5 Volts and a logical 0 or space is an open circuit. If inductive loads are driven by this output, diode protection must be provided by connecting the cathode of a high speed silicon diode to the output and the diode anode to the coil supply voltage.

Line: This output can drive ten TTL unit loads and presents the serial output signal with a logical 1 as +3 Volts and logical 0 as ground.

Active: During the time period from the occurrence of the serial start bit and the beginning of the stop bits, this output is high. This signal is often used in half duplex systems to obtain special control signals. Output drive is eight TTL unit loads.

Flag: This output falls from +3 Volts to ground at the beginning of the stop bits driving a character transmission. The M707 can now be reloaded and the Flag cleared (set to +3 Volts). This output can drive ten TTL unit loads.

Strobed Flag: This output is the NAND realization of the inverted Flag output and Flag Strobe. Output drive is ten TTL unit loads.

+3 Volts: Pin BJ1 can drive ten TTL unit loads at a +3Volts level.

Power: +5 Volts at 375 mA. (max.)

Size: Standard, double height, single width FLIP CHIP module.

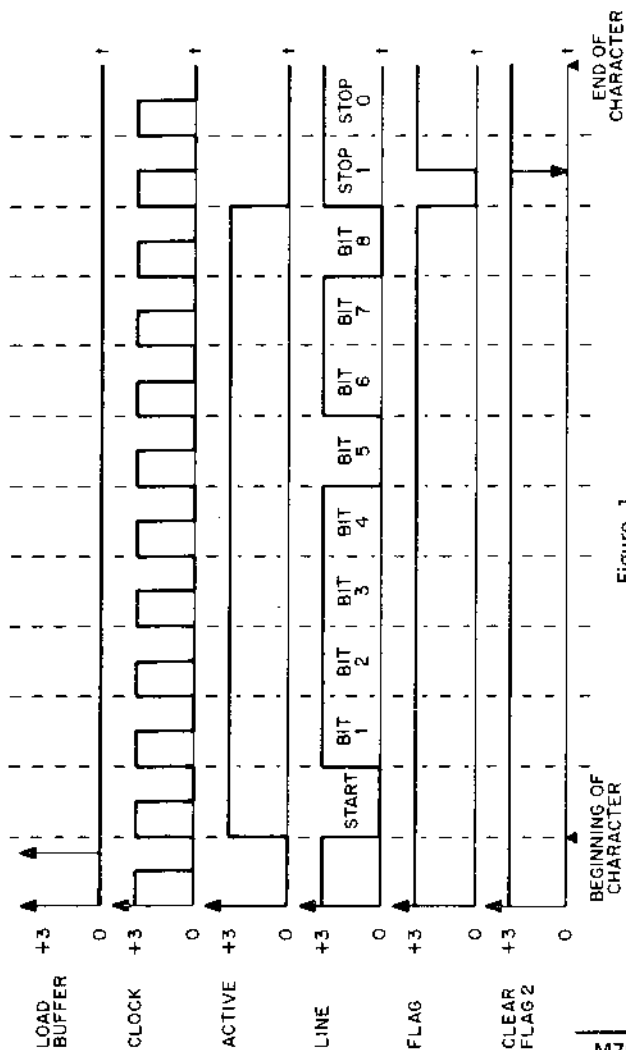
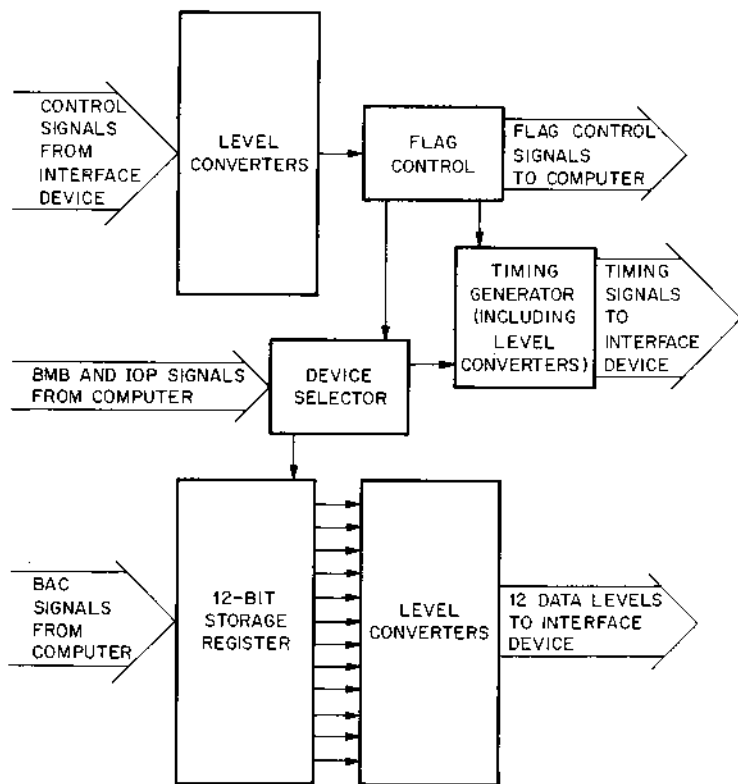


Figure 1.

Typical Timing Diagram, Parallel input, 8-Bit Character (11, 110, 110) With two bit Stop time.

BUS INTERFACE M730 & M731

M SERIES



The M730 and M731 interface modules provide extremely flexible interface control logic to connect devices, systems, and instruments to the output half of the programmed I/O transfer bus of either a PDP8/I or a PDP8/L positive bus computer. Peripheral equipment which operates either asynchronously or synchronously to a computer and expects to receive data from that computer, can to a large degree be interfaced by either the M730 or M731. Basic restrictions on the device or system to be interfaced are simply that it receive data in parallel, provide one or more control lines, and operate at a data transfer rate of less than 20 KHz. Complete interfaces to such peripheral gear as card punches and other repetitive devices is possible using the M730 and M731; however part of the controlling functions, such as counting etc. must be performed by computer software.

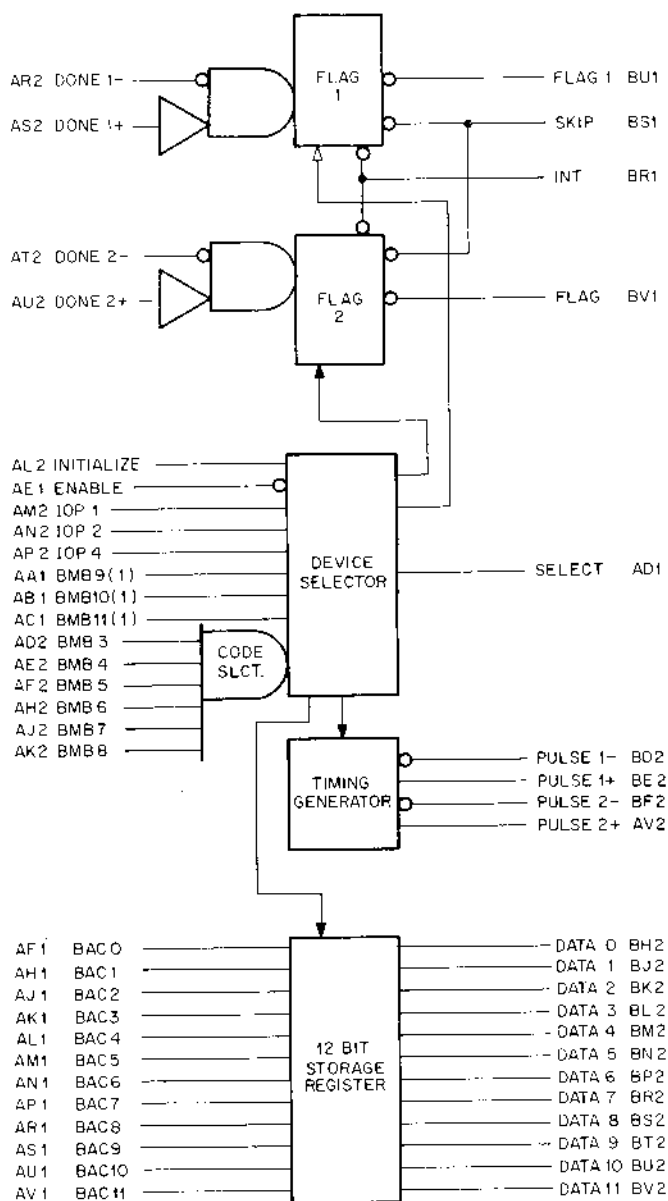


Figure 1

BUS INTERFACE — M730 (POSITIVE OUTPUT)

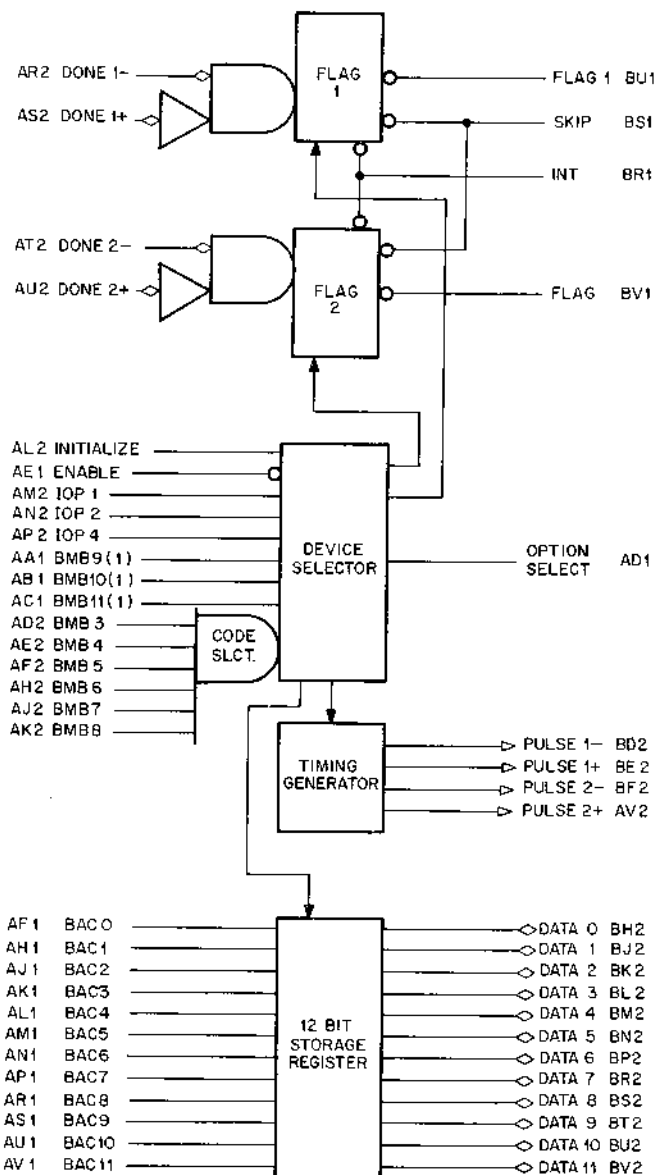


Figure 2

BUS INTERFACE — M731 (NEGATIVE OUTPUT)

Functionally, these modules contain five distinct sections which are as follows:

1. **Device Selector**—This logic network converts the buffered memory buffer (BMB) signals and IOP timing pulses from the computer into internal module control pulses.
2. **Timing Generator**—Through the use of device selector signals, control signals from the interfaced device, and module jumpers, this unit can supply variable width pulses or synchronous control levels at amplitudes specified in section 5 below.
3. **Storage Register**—This 12-bit flip-flop buffer register provides output data storage for information to be transmitted to the interfaced device.
4. **Flag Control**—Provisions for generation of I/O Skip and Program Interrupt signals for the computer are made in this area.
5. **Level Converters**—All level converters from the storage register or timing generator are open-collector transistor types which can drive 30 ma at ground. The M730 has npn drivers and can interface loads returned to a maximum positive supply of +20 Volts and the M731 has pnp drivers which can interface loads returned to a maximum negative supply of -20 Volts. Level converters which input control signals to the Flag control can receive signals of the same polarity and magnitude as the output drivers can sustain.

Thresholds on the input converters are +1.5 Volts and -1.5 Volts for the M730 and M731 respectively. All positive voltage levels are compatible with K and M series and all negative voltage signals are compatible with R, B and W Series.

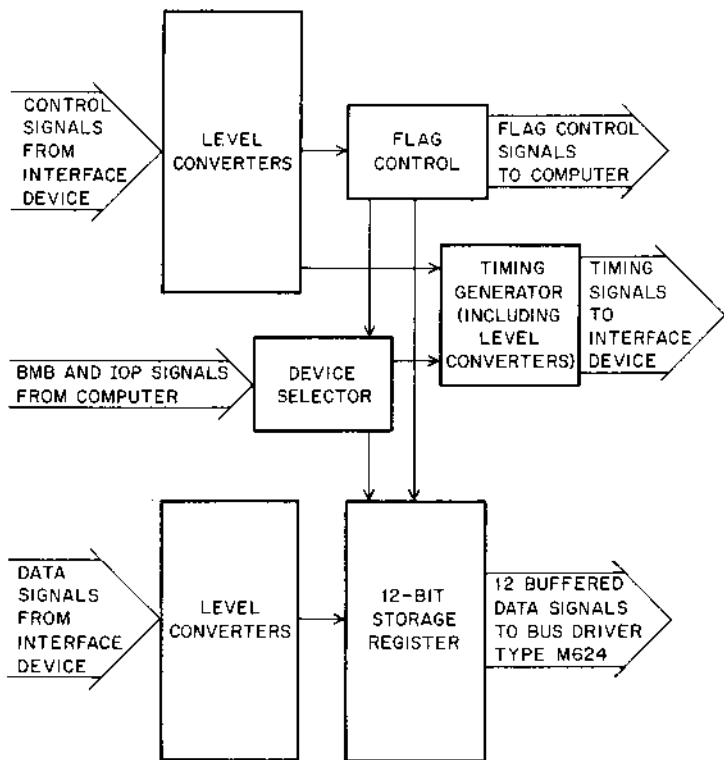
For additional information, technical specifications and applications assistance, a Digital module specialist can be contacted at any Digital Sales office. Application Note AP-M-017 contains useful information concerning the use of the M730 and M731.

Size: Standard, double height, single width FLIP CHIP module.

M730	—	\$160
M731	—	\$160

BUS INTERFACE M732 & M733

M SERIES



The M732 and M733 interface modules provide extremely flexible interface control logic to connect devices, systems, and instruments to the input half of the programmed I/O transfer bus of either a positive bus PDP8/I or PDP8/L computer. Peripheral equipment which operates either asynchronously or synchronously to a computer and expects to transmit data to that computer, can to a large degree be interfaced by either the M732 or M733. Basic restrictions on the device or system to be interfaced are simply that it transmit data in parallel, provide one or more control lines, and operate at a data transfer rate of less than 20KHZ. Complete interfaces to such peripheral gear as card readers and other repetitive devices is possible using the M732 and M733; however, part of the controlling functions such as counting, etc., must be performed by computer software.

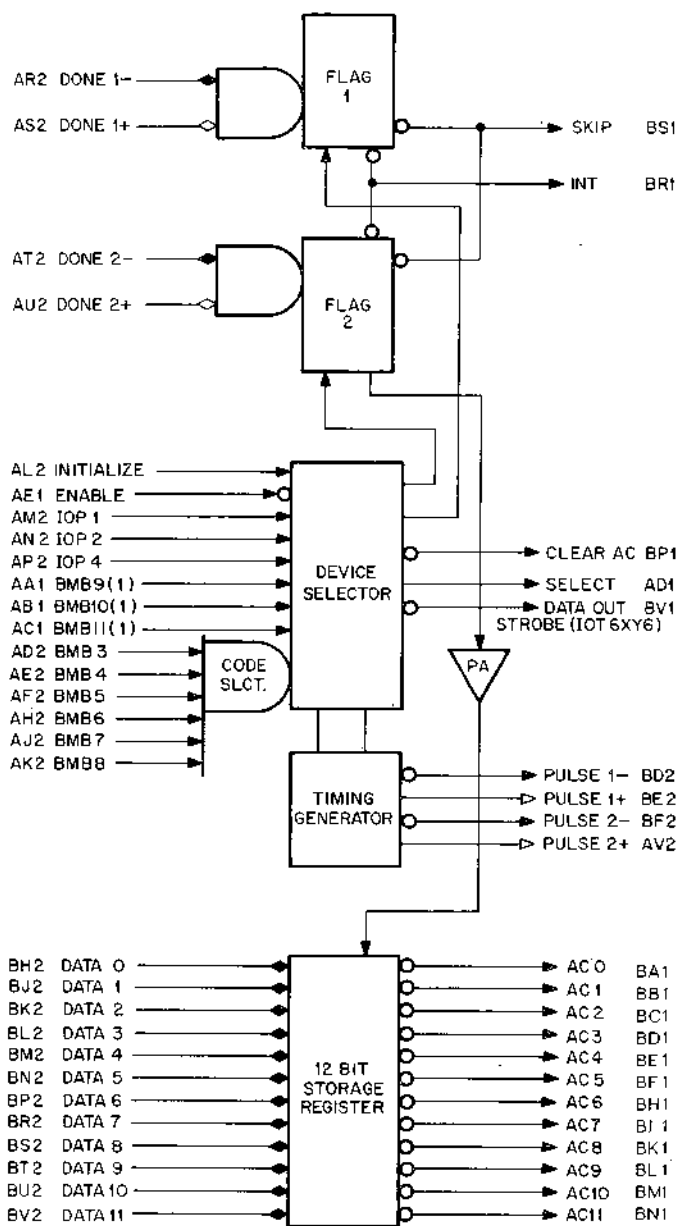


Figure 1

BUS INTERFACE — M732 (POSITIVE INPUT)

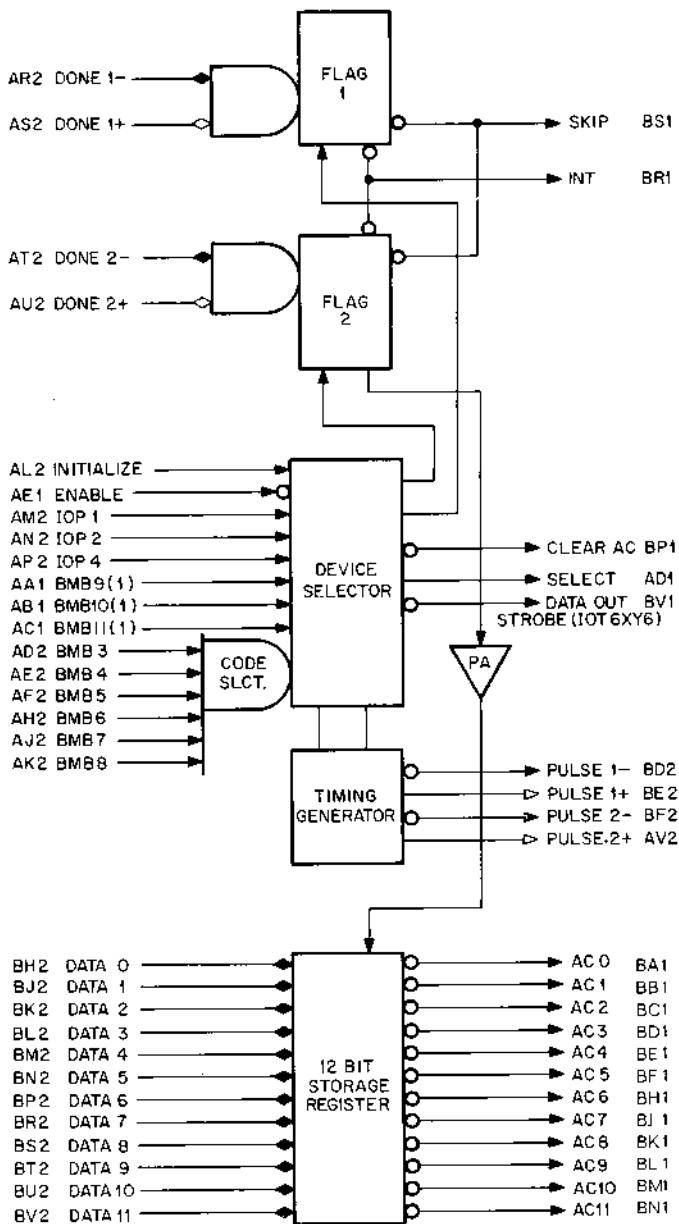


Figure 2

BUS INTERFACE — M733 (NEGATIVE INPUT)

Functionally, these modules contain five distinct sections which are as follows:

1. Device Selector—This logic network converts the buffered memory buffer (BMB) signals and IOP timing pulses from the computer into internal module control pulses.
2. Timing Generator—Through the use of device selector signals, control signals from the interfaced device, and module jumpers, this unit can supply variable width pulses or synchronous control levels at amplitudes specified in section 5 below.
3. Storage Register—This 12-bit flip-flop buffer register provides input data storage of information received from the interfaced device. Information is loaded into this register by a control line from the peripheral.
4. Flag Control—Provisions for generation of I/O Skip and Program Interrupt signals for the computer are made in this area.
5. Level Converters—All level converters from the timing generator are open collector transistor types which can drive 30 mA at ground. The M732 has npn drivers and can interface loads returned to a maximum positive supply of +20 Volts and the M733 has pnp drivers which can interface to a maximum negative supply of -20 Volts. Level converters which input control and data signals to these modules can receive signals of the same polarity and magnitude as the output drivers can sustain. Thresholds on the input converters are +1.5 Volts and -1.5 Volts for the M732 and M733 respectively.

All positive voltage levels are compatible with K and M Series and all voltage signals are compatible with R, B, and W Series.

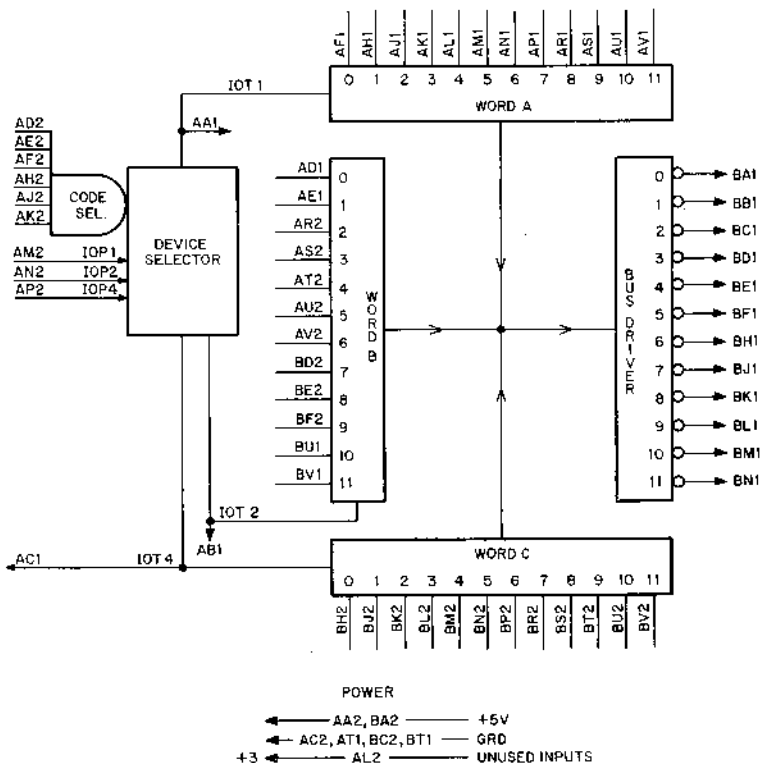
For additional information, technical specifications and applications assistance, a Digital module specialist can be contacted at any Digital Sales Office. Application Note AP-M-018 contains useful information concerning the use of the M732 and M733.

Size: Standard, double height, single width FLIP CHIP module.

M732	—	\$160
M733	—	\$165

I/O BUS INPUT MULTIPLEXER M734

M SERIES



The M734 is a double height, single width module and is a three word multiplexer used for strobing twelve-bit words on the positive voltage input bus; usually the input of the PDP8/I or the PDP8/L. Device selector gating is provided. The data outputs of the M734 Multiplexer consist of open collector npn transistors which allow these outputs to be directly connected to the bus. All inputs present one TTL unit load and function as follows:

Code select Inputs: When a positive AND condition occurs at these inputs, the pulse inputs IOP1, IOP2, and IOP4 are enabled for use in strobing input data. The code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If all select inputs are not required, unused inputs must be tied to a source of +3 Volts (Pin AL2). These inputs are all clamped so that no input can go more negative than -0.9 Volts.

IOP1, 2, 4: These three 50 nsec or longer positive pulse inputs strobe respectively 12-bit words A, B, and C into the bus driver. All three lines are clamped so that no input can go more negative than -0.9 Volts.

Data inputs: Bit 0-11 on words A, B, and C are strobed in 12-bit words as above. Bus driver output lines correspond numerically (0-11) to the selected word input lines (0-11). A high data input will force a bus driver output to ground during a data strobe. Inputs must be present at least 30 nsec prior to issuance of IOP 1, 2, or 4.

Bus driver: These open collector npn transistor bus driver outputs can sink 100 mA at ground. The maximum output voltage must not exceed $+20$ Volts. Each driver output is protected from negative undershoot by a diode clamp. When this module is used with the PDP8/I or PDP8/L, these outputs would be connected to the accumulator input lines of the I/O bus. Typical rise and fall TTT at these outputs with a 100 mA resistive load are 100 nsec.

Data Strobes: Pins AA1, AB1, and AC1 can each drive 18 TTL unit loads. These outputs appear coincident with IOP1, IOP2, and IOP4 respectively only if the code select inputs are all high.

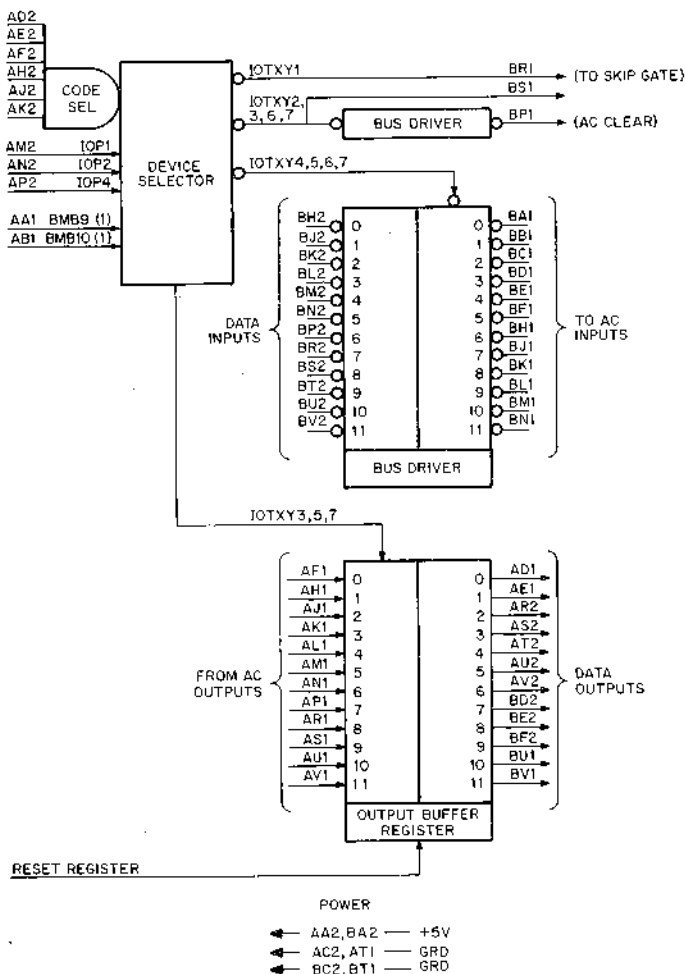
$+3V$ — Pin AL2 can drive 19 inputs at a high logic level.

Power: $+5$ Volts at 325 mA. (max.)

Size: Standard, double height, single width FLIP CHIP module.

I/O BUS TRANSFER REGISTER M735

M SERIES



The M735 provides one 12-bit input bus driver and one 12-bit output buffer register for input and output data transfers on the positive I/O bus of either a PDP8/I or a PDP8/L. Device selector gating plus additional signal lines provide the flexibility necessary for a complete interface with the exception of flag sense signals. Use of the M735 is not restricted to a computer, as it can be used in many systems to provide reception and transmission of data over cables.

Inputs:

All inputs present one TTL unit load with few exceptions as noted in the functional descriptions below:

Code Select Inputs: When a positive AND condition occurs at these inputs, the pulse input gates for IOP1, IOP2, and IOP4 are enabled for use as detailed below. The code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If all select inputs are not required, unused inputs must be tied to a source of +3 Volts. These inputs are all clamped so that no input can go more negative than -0.9 Volts. When this module is used with the PDP8/I or PDP8/L these inputs would be connected to BMB outputs 3-8 to generate a device code. Where required in discussions below, this 6-bit device code will be referred to as code XY.

IOP1, 2, 4, BMB9(1) and BMB10(1): These three IOP's 50 nsec or longer positive pulse inputs, in conjunction with control level inputs BMB9(1) (Pin AA) and BMB10(1) (Pin AB1) provide all of the necessary signals for operation of this module. Table 1 below indicates the recommended use of these pulses and levels. A "1" or "0" in this table indicates the presence or absence respectively of a pulse (an IOP) or the logic level at pins AA1 or AB1.

The M735 module operation as associated with the various mnemonic IOT codes is quite explicit with the exception of IOTXY5. This code (IOTXY5) would be used to load zeros into the M735 with IOTXY1 and then to load into the AC the data present at the data inputs of the bus driver when IOTXY4 occurs. In this particular operation the AC has been effectively cleared as the content of the AC was zero during IOTXY1 thereby allowing the transfer of data into the AC without the use of the AC clear command usually generated by IOT2.

IOP 4	IOP 2	IOP 1	BMB 9(1)	BMB 10(1)	PDP/8 Mnemonic	Module Operation
0	0	1	0	0	IOTXY1	+3V → OV output pulse on pin BR1 used for skip function.
0	1	0	0	1	IOTXY2	+3V → OV output pulse on pin BS1, bus driver output on BP1 pulsed to ground and is used for the AC clear function.
0	1	1	0	1	IOTXY3	Load output register from accumulator outputs on IOP1 execute IOTXY2.
1	0	0	1	0	IOTXY4	Data inputs strobed onto accumulator inputs.
1	0	1	1	0	IOTXY5	Load output register on IOP1, Execute IOTXY4.
1	1	0	1	1	IOTXY6	Execute IOTXY2, and IOTXY4.
1	1	1	1	1	IOTXY7	Execute IOTXY3, and IOTXY4.

Although it is not implicit from Table 1, BMB9(1) and BMB10(1) inputs are gated in a positive OR circuit, so that when the M735 is not used on a PDP8/I or PDP8/L I/O bus one of these inputs can be grounded and the other used for control. They must appear at least 50 nsec prior to an IOP pulse. If the M735 is used with one of the above computers, these inputs must be tied to the corresponding I/O bus lines. The input load on IOP1 is two TTL unit loads. All five inputs are clamped so that no input can go more negative than -0.9 Volts.

Data Inputs: Each data input when at ground, enables the corresponding bus driver output to be pulsed to ground during IOTXY4. A high input will inhibit the bus driver from being strobed. Since each input is ANDed with IOTXY4, any change of data after this strobe begins will change the bus driver output.

Accumulator Inputs: The input level presented to these inputs will be the same as that assumed by the buffer outputs after executing inputs strobes IOTXY, 5, or 7. Input data must be present at least 50 nsec prior to an IOP. Each input is protected from negative undershoot by a diode clamp.

Reset Register Pin AL2: A positive pulse of 50 nsec or longer at this input sets all buffer outputs to ground. When high, this input overrides any data loading from the accumulator inputs. The output register will be cleared within 70 nsec from the rising edge of this input. Diode input clamping is provided to limit negative undershoot to -0.9 Volts.

Outputs:

Pin BR1: This output can drive ten TTL unit loads and has a propagation delay of less than 20 nsec. See Table 1.

Bus Driver: These open collector npn transistor bus driver outputs, including pin BP1, can sink 100 ma. at ground. The maximum output voltage cannot exceed +20 Volts and each driver output is protected from negative undershoot by a diode clamp. When this module is used with the PDP8/I or PDP8/L, output pins BA1—BN1 would be connected to the accumulator input lines and pin BP1 to the clear accumulator line of the I/O bus. Typical rise and fall TTT of these outputs with a 100 mA. resistive load are 100 nsec.

Buffer Outputs: Each output can drive ten TTL unit loads.

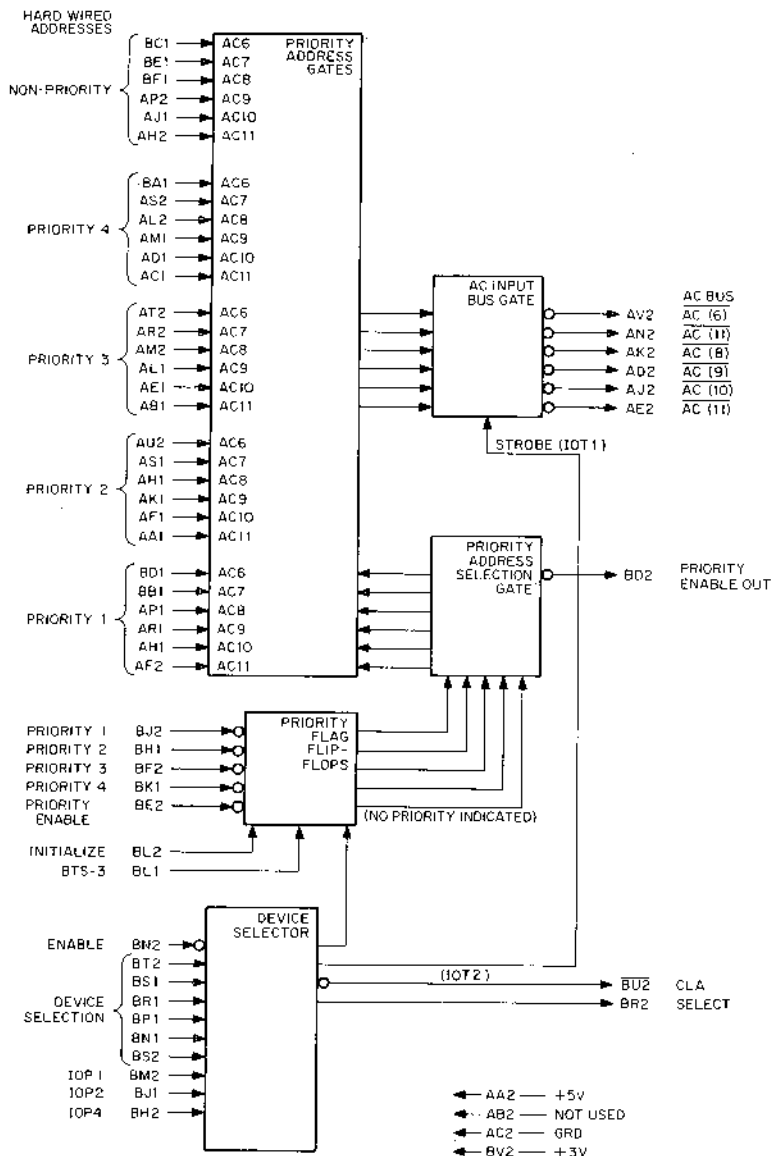
Power: +5 Volts at 425 mA. (max.)

Size: Standard, double height, single width FLIP CHIP module.

M735 — \$135

PRIORITY INTERRUPT MODULE M736

M SERIES



The M736 is used in conjunction with the PDP8/I or 8/L to provide the capability of assigning priorities to various I/O devices connected to the I/O bus of the computer. The M736 can be used to assign priorities for one thru four external devices. Priority assignment may be provided for more than four devices by using additional M736 modules for each additional group of four devices. All M736's in a particular priority system would utilize the same device code.

THEORY OF OPERATION

Basically the M736 module consists of the following:

1. The M103 device selector function.
2. A Bit Time State-3 (BTS-3) input.
3. Four priority input lines.
4. Priority enable line, input and output.
5. Five groups of six gates, each of which is capable of being hard wired to provide address information to locate subroutines to service the various devices associated with the priority interrupt system. The output of each of these gates is strobed onto the accumulator input bus on lines AC(6) thru AC(11).

SEQUENCE OF OPERATION

The external device activates its skip and/or interrupt FLAG flip-flop. The activation of the FLAG causes two things to happen; (a) The computer's interrupt request line is pulled to ground. This tells the computer that an external device requires service and requests the computer to jump to an I/O priority interrupt service subroutine as soon as the computer completes its present cycle. (b) The external device FLAG pulls to ground the appropriate hard wired priority line connected to a "D" flip-flop in the M736.

A Bit Time State-3 (BTS-3) pulse from the computer is applied to the clock input of the "D" flip-flop to which the activating device flag is connected, as mentioned in section 1b above, and causes this flip-flop in the M736 to set. If more than one priority device called to be serviced at the same time, all of the associated priority "D" flip-flops in the M736 would be set at this time. The outputs of the priority flip-flops in the M736 are connected to a priority gate structure which is arranged in such a manner that only one output line will be activated and that line will be associated with the external device with the highest priority.

This activated output of the priority gate structure is applied to one group of six two-input gates which make up the address gate. The other input of each of the six two-input gates of the address gate is hard wired to provide a discrete address which will correspond to the starting location of the particular subroutine associated with that priority request. Each of the six output lines of the activated address gates is applied to one input of a two-input gate of the AC input strobe gate.

The computer now has had time to jump to the priority interrupt service routine and now issues a device selection code corresponding to the hard wired device selection code assigned to the M736 priority interrupt modules. This device selection code will pre-enable the IOP gates of the M736 of M736's.

The computer now issues an IOP-2 pulse to the IOP-2 gate of the M736 module. The output of the IOP-2 gate now produces an IOT-2 pulse which causes the "Clear the AC" line of the I/O bus to be pulled to ground, and thereby clears the AC.

The computer issues an IOP-1 pulse to the IOP-1 gate of the M736 module. The output of the IOP-1 gate produces an IOT-1 pulse which is applied to the strobe inputs of the AC input bus gate. As the other inputs of the AC input bus gate are connected to the outputs of the address gate, appropriate lines of the AC input bus (AC 6 thru AC 11) will be pulled to ground thereby loading into the AC the starting address of the subroutine associated with the particular priority I/O device to be serviced.

The computer now refuses to accept any further interrupt requests and jumps to the subroutine with the particular starting address which was loaded into the AC. The service routine of the particular priority device contains an instruction to clear the interrupt flag flip-flop of the particular I/O device and at the end of the subroutine issues the M736 device selector code with an IOP-4 which clears the priority flag flip-flops of the M736. The computer now turns on the priority interrupt system capability which allows the computer to service any future interrupt requests.

USING THE M736 PRIORITY INTERRUPT MODULES

1. Assign a device selection code to the M736 priority system and connect the device selection inputs of the M736 to the proper device selection lines to assure decoding for that code. If more than one M736 is used connect the device selection lines for each M736 in exactly the same manner. Each M736 will use the same device selection code. These inputs are: BT2, BS1, BR1, BP1, BN1 and BS2.
2. Connect the enable input, BN2, of each M736 to +3V.
3. Connect the IOP-1 input, BJ1, to the IOP-1 bus line.
4. Connect the IOP-2 input, BM2, to the IOP-2 bus line.
5. Connect the IOP-4 input, BH2, to the IOP-4 bus line.
6. Connect the BTS-3 input, BL1, to the BTS-3 bus line.
7. Connect the outputs of the external I/O device flag flip-flops to the priority

NOTE: In normal operation, IOP-4, is not required as the flag flip-flop in the external priority I/O device is cleared by the subroutine servicing that device. When the flag in the I/O device is cleared, the next BTS03 pulse will load the disabled flag output into its respective priority flag flip-flop in the M736 effectively clearing the priority flag flip-flop.

inputs in such a manner as to pull the corresponding priority input line of the M736 to GRD when the device flag is activated. These inputs are as follows:

1st priority	BJ2	1st	M736 Module
2nd priority	BH1	"	" "
3rd priority	BF2	"	" "
4th priority	BK1	"	" "
5th priority	BJ2	2nd	" "
6th priority	BH1	"	" "

Carry on for additional priority interrupt devices.

8. Assign starting address to the subroutines which will service each priority interrupt device attached to the priority interrupt system. Also assign a starting address for the subroutine to service non-priority devices. Hard-wire the various starting address of the service routines as follows:

	AC(6)	AC(7)	AC(8)	AC(9)	AC(10)	AC(11)
Priority 1	BD1	BB1	AP1	AR1	AH1	AF2
Priority 2	AU2	AS1	AN1	AK1	AF1	AA1
Priority 3	AT2	AR2	AM2	AL2	AE1	AB1
Priority 4	BA1	AS2	AL2	AM1	AD1	AC1
NON-Priority	BC1	BE1	BF1	AP2	AJ1	AH2

NOTE: If more than four external I/O devices require priority assignments, the NON-priority address inputs BC1, BE1, BF1, AP2, AJ1 and AH2 of the M736 module used for the first four highest priorities, must be connected to GRD. If more than two M736 modules are required all of the NON-priority address lines of each module except the last M736 containing the lowest priorities, must be connected to GRD. The NON-Priority address is hardwired to the NON-Priority address inputs of only the lowest priority M736 module. All un-used priority address inputs must be grounded. Logic 1 level for address may be obtained from module pin BV2 of each M736 module. Lower priority addresses would be hardwired on succeeding M736 modules in the same order hard wired to the second M736 module as follows:

	AC(6)	AC(7)	AC(8)	AC(9)	AC(10)	AC(11)
Priority 5	BD1	BB1	AP1	AR1	AH1	AF2
Priority 6	AU2	AH2	AK2	AD2	AJ2	AE2

9. Connect the AC input bus gate outputs to the AC bus as follows:

	AC(6)	AC(7)	AC(8)	AC(9)	AC(10)	AC(11)
Module Pins	AV2	AH2	AK2	AD2	AJ2	AE2

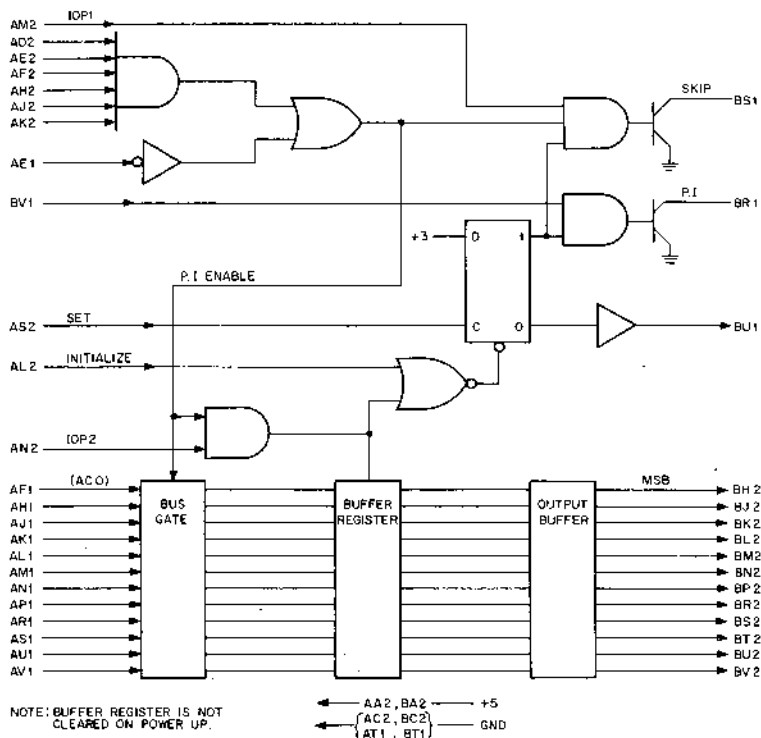
10. Connect the Priority Enable input line BE2, of the M736 with the highest priorities, or the only priorities, to ground.
11. If lower priorities of 5 or more are assigned, connect the Priority output of the module with the higher priorities, Pin BD2, to the next M736 module (with the next following four lesser priorities) Priority enable input pin BE2.
12. Last, but not least, connect the INITIALIZE input, BL2 to the Initialize line of the computer I/O bus.

Size: Standard, double height, single width FLIP CHIP module.

M736 — \$125

12-BIT BUS RECEIVER INTERFACE M737

M SERIES



The M737 12-Bit Bus Receiver Interface is completely contained on a double height, single width module.

The M737 was designed primarily to receive and store in a buffer register twelve parallel data bits from the positive bus of the PDP-8/I or PDP-8/L. The M737 is pin compatible with the M738 Counter-Buffer Interface, the M107 Device Selector, the M108 Flag Module, and the 12-Bit Bus Paneloid E100. The 12-Bit Bus Receiver Interface, M737, consists of three basic sections: device selector, flag, and buffer register section.

Device Selector Section

The device selector section contains six address inputs which are to be connected to the proper BMB bits for address selection. IOP 1 input is used to generate an IOT 1 which is used internally to test the flag. The output of flag test gate is connected directly to the skip bus with an NPN transistor. The output of the address selection gate is connected to the bus gate of the buffer

register section and functions as an option select level. IOP 2 is used for two purposes. It is internally connected in such a manner as to clear the flag and to load the buffer register with the contents of the BAC lines.

The Flag Section

The flag section is used to generate a programmed interrupt. The flag flip-flop may be set by a level shift from low to high (a positive going voltage) applied to the set input at pin AS2. The output of the flag is connected to the P. I. line by way of a P. I. enable gate and an open collector NPN transistor. The output of the flag is also connected to pin BU1. The flag is reset by IOP2 applied to pin AN2 or by initialize pulses applied to Pin AL2.

Buffer Register Section

Data from the bus is applied to the inputs of the bus gate. The bus gate prevents the buffer register from loading the bus when M737 is not addressed. The bus gate is enabled by the option select level derived internally from the output of the device selector section. The buffer register is loaded by jam transfer upon the command of an IOT2 instruction. The output of the buffer register is buffered by the use of TTL circuitry.

Inputs: All inputs which receive positive bus signals are protected against negative voltage undershoot. AE1, BV1 represent 1.25 TTL unit loads. These two inputs need not be tied to a logic 1 source when not used.

AM2, AN2 represent 2.5 TTL unit loads.

AS2 represents 2 TTL unit loads.

All other inputs represent 1 TTL unit load.

Outputs: BS1, BR1 will sink 25 MA to ground. Voltage applied to these outputs must not be allowed to exceed ± 20 Volts. These outputs are protected against negative voltage undershoot and consist of open collector NPN transistors.

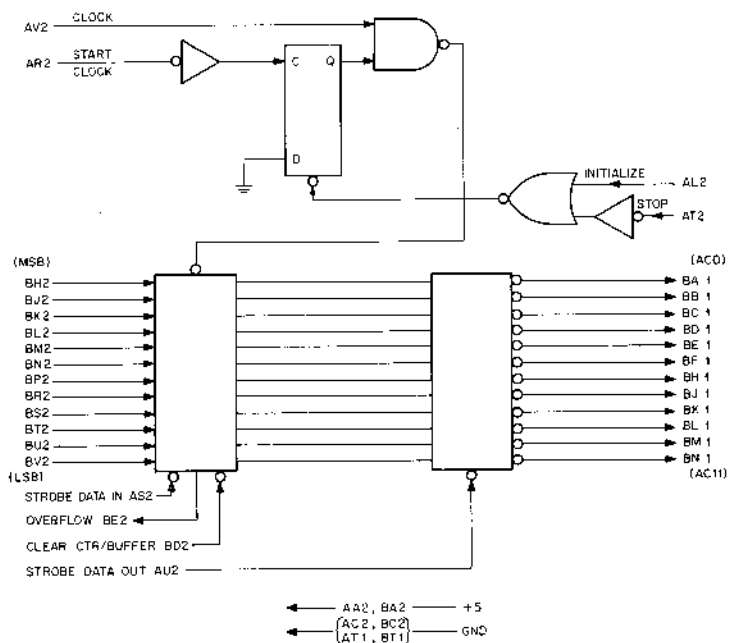
All other outputs will drive 10 TTL unit loads.

Power: ± 5 Volts, 300 mA (maximum).

Size: Standard, double height, single width FLIP CHIP module.

COUNTER-BUFFER INTERFACE M738

M SERIES



The M738 Counter-Buffer Interface is contained on a double height, single width module.

The M738 was designed primarily to strobe twelve parallel bits onto the positive bus of the PDP-8/1 or PDP-8/L. This module consists of three basic sections: 1) A twelve bit bus driver, 2) A twelve bit Up Counter which is presettable by jam transfer, and 3) A clock input gate circuit twelve bit bus driver.

The twelve bit bus driver is used to strobe the contents of the buffer counter onto the bus when a logic 0 (gnd) is applied to the "Strobe Data Out" pin AU2. The output of the bus driver consists of an open collector NPN transistor which allows the data outputs of other M738 modules to be parallel in a collector OR to ground fashion.

These outputs can sink 25 mA to ground and are protected against negative voltage undershoot in excess of $-0.9V$.

The input to the "Strobe Data Out" pin AU2 would normally be an IOT pulse derived from a M103 or M107.

Twelve bit up counter-buffer:

The twelve bit counter-buffer consists of three MSI, 4-bit presetable counters connected in tandem. Twelve parallel bits of data may be applied to the data inputs and then jam transferred into the counter by the application of a logical zero of time duration equal to or greater than 250 n seconds to the "Strobe Data In" pin AS2. This input could be an IOT pulse from a M102 or M107.

The contents of the counter may be cleared by the application of a logical zero of time duration equal to or greater than three micro-seconds applied to the "clear counter/buffer" input pin BD2. The requirement of a three micro-second pulse precludes the direct use of an IOT pulse for clearing the counter. If it is required to clear the counter by the command of an IOT pulse, a M302 dual delay multivibrator could be used to stretch the IOT pulse length. At times, it may be desirable to connect two or more M738 module counters in tandem. This may be accomplished by connecting the "overflow" output pin BE2 of the first M738 to the "clock" input pin AV2 of the next M738. The clear pulse time duration should be an additional 3 micro-seconds for each M738 added in tandem; i.e. 24 bits would require a 6 micro-second clear pulse.

Clock Input Gate

The clock input gate circuit contains a storage flip-flop which serves to gate a clock pulse applied to the "Clock" input, pin AV2, into the counter buffer. This flip-flop may be initialized by the application of a logic one pulse (+ voltage pulse) to pin AL2 or by a logic zero (ground pulse) applied to the "Stop" input AT2. When the flip-flop is initialized, clock pulses applied to the clock input, pin AV2, will not be counted. Clock pulses may be counted by setting the flip-flop with the application of a logic zero pulse to the "Start Clock" input AR2. The four inputs, clock, start clock, stop and initialize require a minimum pulse width of 50 nanoseconds and therefore could use IOT pulses derived from the device selectors M103 or M107.

Inputs: AS2 3TTL Loads
AU2 12TTL Loads
All other inputs 1 TTL Load
(See text for timing considerations)

Outputs: BE2 10TTL Loads

All other outputs consist of open collector NPN transistors which are capable of sinking 25 MA to ground. Voltage applied to these outputs must not exceed +20 Volts. The outputs are diode protected against negative voltage undershoot in excess of -0.9 Volts.

Power: +5V at 250 MA (maximum) — no strobe onto bus.
370 MA (maximum) — during bus strobe.

Size: Standard, double height, single width FLIP CHIP module.

M738 — \$105

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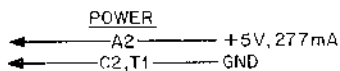
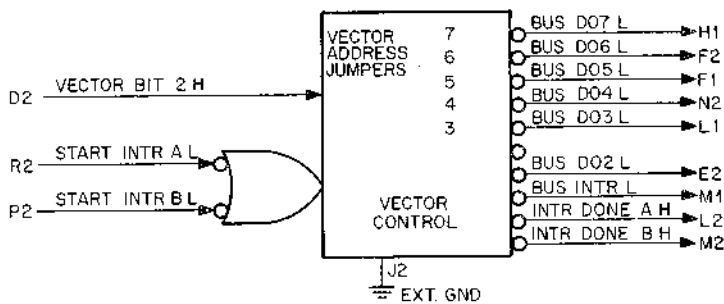
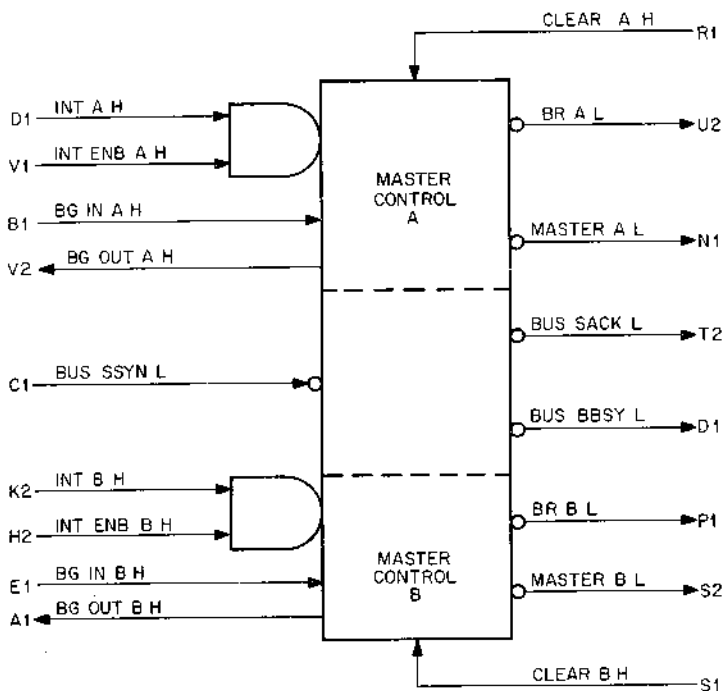
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INTERRUPT CONTROL M782

M SERIES



The M782 is used in PDP-11 device interfaces. It consists of logic circuits that can be divided into three functional sections: Master Control A, Master Control B, and INTR Control.

The Master Control circuits are used to gain control of the UNIBUS for satisfying the need to either Gain direct memory access (DMA), or to perform the INTR bus operation which alters program flow.

To become master of the bus involves a question of priority. Briefly, this priority question is split into three phases: 1) bus request lines, 2) processor's priority level, and 3) physical placement of a device on the UNIBUS.

- 1) NPR (highest)
BR7
BR6 (except for trap instructions)
BR5
BR4 (lowest)
- 2) The processor acknowledges BR's of level $> N$: where N is an Octal number in processor's status register. (NPR's are not affected.)
- 3) Highest priority goes to the device closest to the processor on the unique bus grant chain.

Theory Of Operation

If a device wants control of the bus, it asserts both INT A and INT ENB A. Then a request is made on a BR. This then leads to priority determination and a BG results. Now the Master Control A responds with BUS SACK. The processor sees this acknowledgement and removes BG. When BUS BBSY and BUS SSYN are negated, the Master Control A removes its BR and asserts BUS BBSY itself. It also asserts Master A when it is in control of the bus. Now the device can use the bus. To release control of bus, the device can assert CLEAR A or negate: INT A or INT ENB A. Master Control B is identical to A.

The INTR operation transfers a "vector address" to the processor. At this address is stored two consecutive words: 1) The starting address of the interrupt service routine, and 2) A status word. When the processor detects this, a trap sequence is initiated (current value of PC and current status of PS are stored and new ones are fetched.) Now the interrupt service routine is executed.

To start the process: START INTR A or START INTR B is asserted. Then BUS INTR is asserted along with a 6-bit address. This is transferred onto the data lines: BUS D (07:02) providing a range of 000 to 374 (OCTAL) in increments of 4. D(07:03) are controlled by jumpers, which when "in," forces the bit to zero. The processor seeing BUS INTR asserts BUS SSYN: When this is detected, an INTR DONE A is asserted which negates the START INTR signal. This in turn negates BUS INTR, which negates BUS SSYN. As a result, a trap sequence is initiated. Vector bit-2 controls D02. When it is asserted D02 is asserted. It does not control any other bits.

LOGIC LEVEL	1	(high) $> +3V$ at	40 μ A
LOGIC LEVEL	0	(low) $< .4V$ at	-1.6mA

Input Loading: One TTL load (each)

INT¹ A,B
INT ENB A,B
MASTER CLEAR A,B
VECTOR BIT 2

Two TTL load (each)

START INTR A,B

One Unibus receiver load* (each)

BG IN A,B
BUS BBSY
BUS SSYN

-25 mA (max.)

EXT. GND

*A UNIBUS receiver load is characterized at:

< 1.4V at 25 μ A (max.) Low level
> 2.5V at 160 μ A (max.) High level

Output Drive: Ten TTL loads (each)

MASTER A,B
INTR DONE A,B

One UNIBUS driver load* (each)

BR A,B
BUS INTR
BUS D (07:02)

Two UNIBUS driver loads* (each)

BUS SACK
BUS BBSY
BG OUT A,B

*A UNIBUS driver load is characterized at:

< 0.8V at 50 mA (max.)
25 μ A (max.)

LOW LEVEL
Open collector leakage

Power: +5 Volts at 277 mA (max.)

The grant chain to tie in the Master Control as follows:

BG IN has 390 Ω to GND and BG has 180 Ω
+5 Volts.

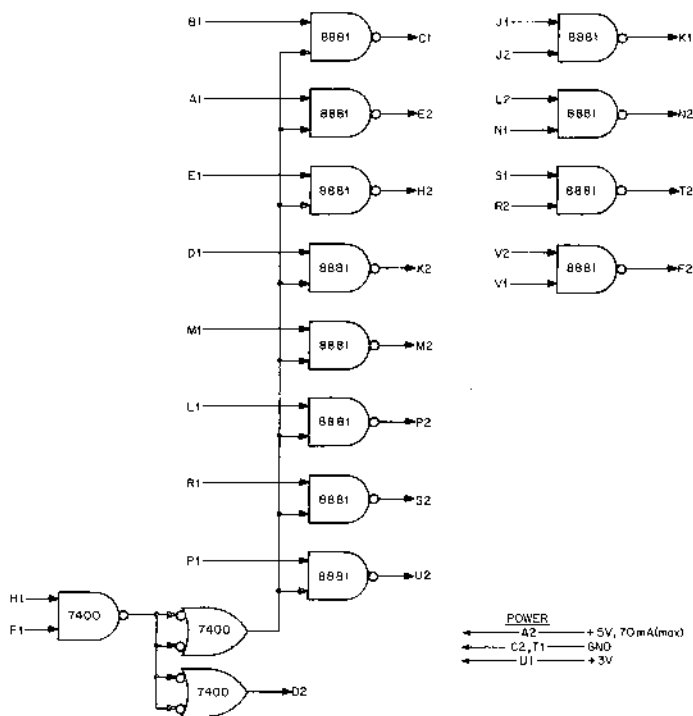
EXT GND is used for testing purposes and should be tied to ground in normal operations.

Size: Extended length, single height, single width FLIP CHIP module.

M782--\$100

UNIBUS DRIVERS M783

M SERIES



The M783 consists of twelve drivers to be used as an interface with the UNIBUS of the PDP-11. Pin U1 provides +3 Volts and has an output capability of ten TTL loads.

Input Loading: Each input represents 1.5 TTL loads.

Output Drive: Fanout of 10 from pin D2; all others are capable of sinking 50 mA. with a collector voltage of less than or equal to 0.8 Volts.
Leakage current is less than 25 microamps.

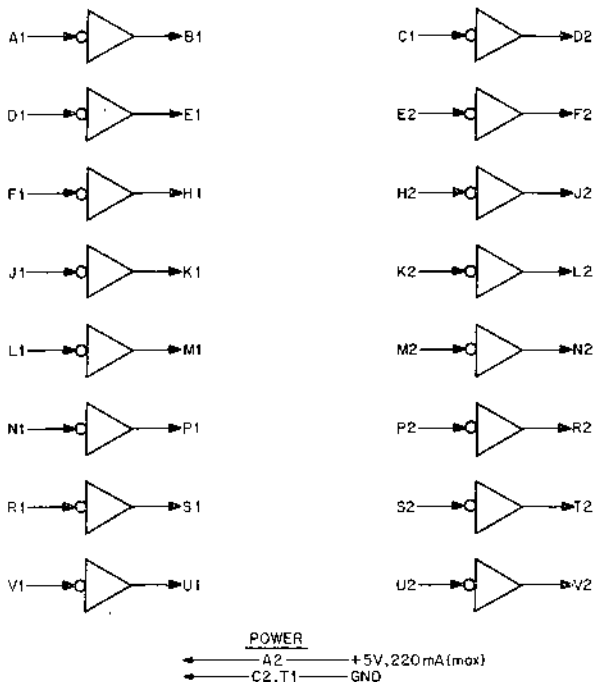
Power: +5 Volts at 69.9 mA. (max.)

Size: Extended length, single height, single width FLIP CHIP module.

M783—\$30

UNIBUS RECEIVERS M784

M SERIES



The M784 consists of sixteen inverting receivers that are used as interface with the UNIBUS of the PDP-11.

Input Loading: All inputs have one Unibus receiver load.*

*A Unibus receiver load is characterized as:

$< 1.4V$ at $25\mu A$ (max.)	LOW LEVEL
$> 2.5V$ at $160\mu A$ (max.)	HIGH LEVEL

Output Drive: Each output has a fanout capability of 7 TTL loads.

Output LOW Level 0.6V	@ 12.5 mA
Output HIGH Level 3.5V	@ -2.5 mA

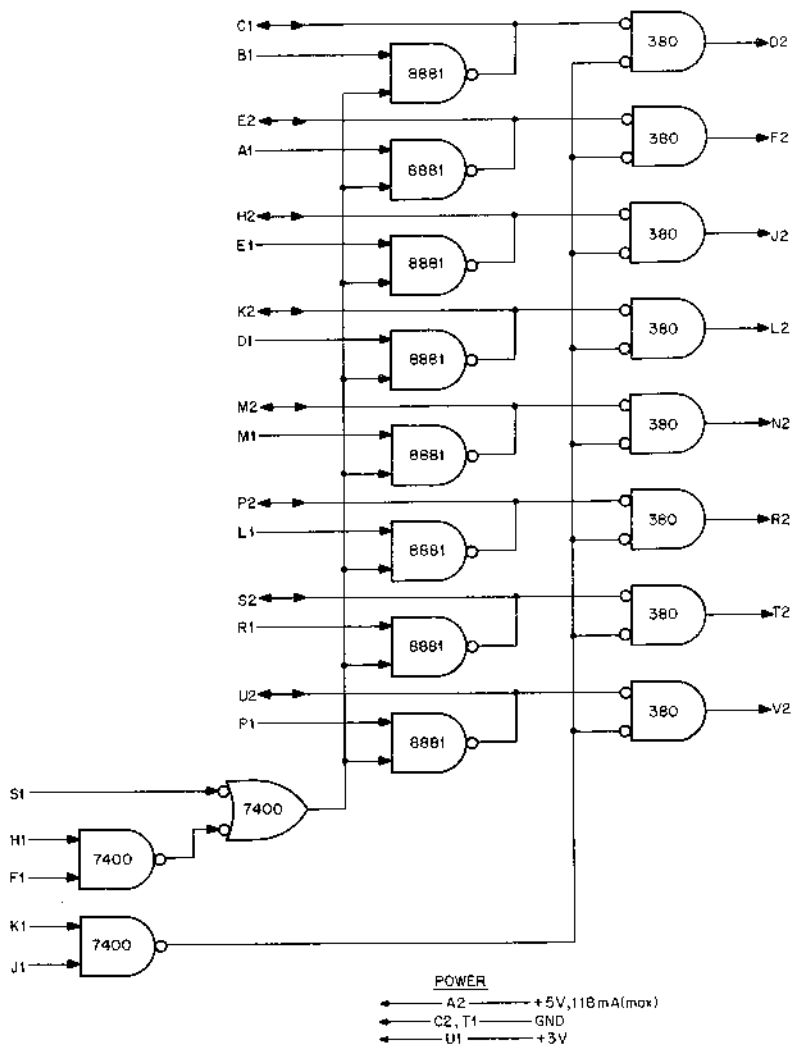
Power: +5 Volts at 200 mA (max.)

Size: Extended length, single height, single width FLIP CHIP module.

M784—\$30

UNIBUS TRANSCEIVER M785

M SERIES



The M785 consists of 8 drivers and 8 receivers, and is used as a device interface with the PDP-11 UNIBUS. Pin U1 provides +3 Volts and has an output capability of ten TTL loads. Driver gates are open collectors and capable of sinking 50 mA with a collector voltage of less than 0.8V.

Input Loading: All driver inputs represent 1.5 TTL loads.

All other inputs have one Unibus receiver load*

*A Unibus Receiver load is characterized at:

< 1.4V at 25 μ A (max.) LOW LEVEL
> 2.5V at 160 μ A (max.) HIGH LEVEL

Output Drive: Each output has a fanout capability of 7 TTL loads.

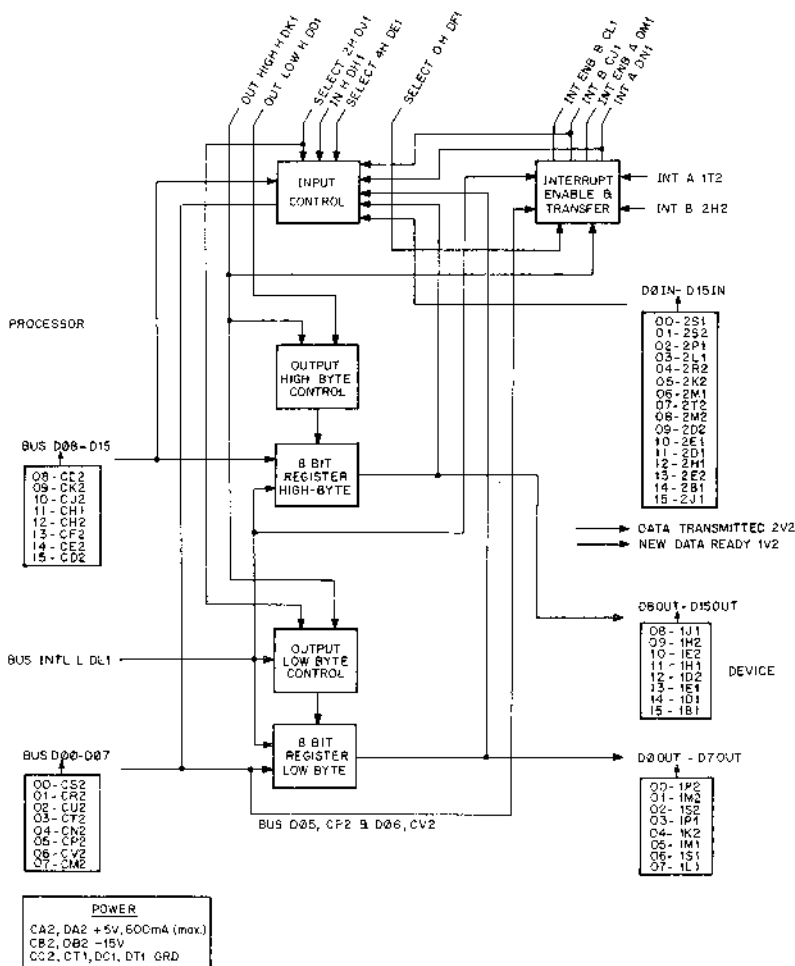
Output LOW Level 0.6V @ 12.5 mA
Output HIGH Level 2.5V @ -2.5 mA

Power: +5 Volts at 118 mA (max.)

Size: Extended length, single height, single width FLIP CHIP module.

DEVICE INTERFACE M786

M SERIES



The M786 Device Interface is a double height module used in conjunction with the M105 Address Selector and the M782 Interrupt Control to enable an external device containing up to 16 bits to communicate with the KA11 Processor.

The Device Interface contains controls for reading a 16 bit word from an external device into the processor, a 16 bit register that may both be loaded and read by the processor (whose outputs are available to an external device), two interrupt enable flip-flops which may also both be read and loaded by the processor, and two REQUEST bits controlled by an external device.

The device may signal the processor by generating an interrupt signal on one of the two REQUEST lines. If the appropriate interrupt enable flip-flop in the device interface is set, an interrupt signal is sent to the processor.

Input Loading: All standard TTL loads.

All one unit loads except REQUEST lines which are two unit loads.

Output Drive: All 8 unit loads.

Power: +5 Volts at 600mA (max.)

Size: Extended length, double height, single width FLIP CHIP module.

M786—\$220

The BB11 is a prewired system unit used for general interfacing. It consists of three 288-pin blocks assembled end-to-end in a casting which can be mounted in the basic PDP-11 box or extension box. Six of the module slots are used for bus and power connectors. These slots are:

POWER-A3

UNIBUS-A1-B1 and A4-B4

+5 Volts to all A2 pins

-15 Volts to all B2 pins (except in slots A1, B1, A4 and B4)

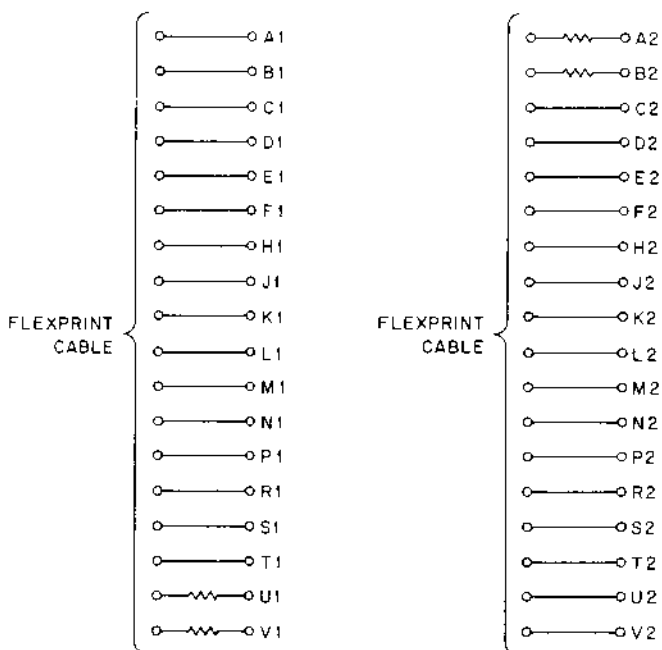
Ground to all C2 and T1 pins.

	1	2	3	4
A	UNIBUS CONN.	RESERV.	POWER	UNIBUS CONN.
B	UNIBUS CONN.			UNIBUS CONN.
C				
D				
E				
F				

BB11—\$90

FLEXPRINT CABLE CONNECTOR M901

M SERIES



This module allows 36 lines to be used as signals and/or grounds. The 100-ohm resistors connected in series with the modules pins A2, B2, U1 and V1 are provided to afford some measure of protection in the event that these pins are inadvertently connected to a source of supply voltage.

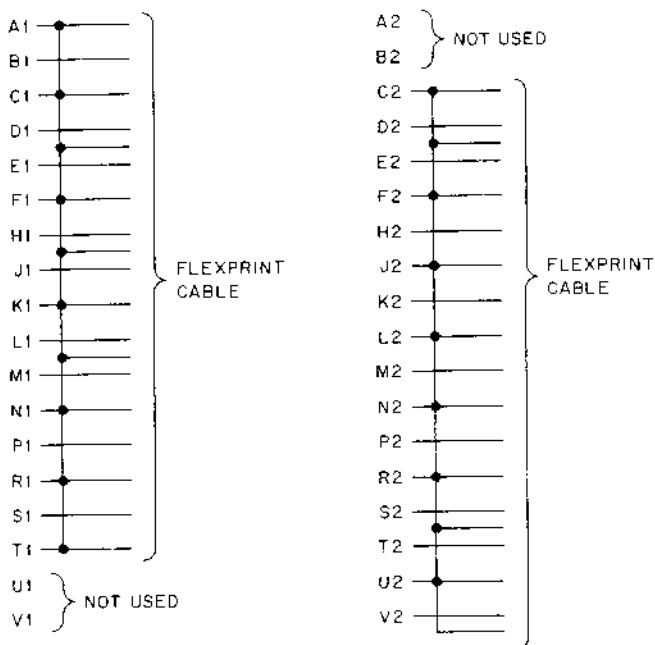
Input: Recommended current per line is 100 mA. maximum.

Size: Standard; single height, single width FLIP CHIP module.

M901 — \$ 15

FLEXPRINT CONNECTOR M903

M SERIES



The M903 connector is a single sized, double sided board.

This connector provides high density cable connections using two single flex-print cables. Eighteen signal leads and grounds are used as listed below.

Signal: B1, D1, E1, H1, J1, L1, M1, P1, S1
 D2, E2, H2, K2, M2, P2, S2, T2, V2

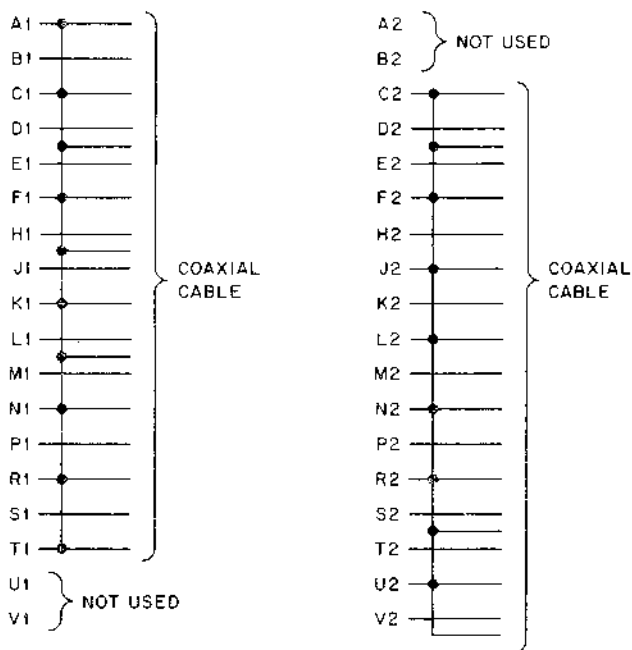
Common Ground: A1, C1, F1, K1, N1, R1, T1
 C2, F2, J2, L2, N2, R2, U2

Size: Standard, single height, single width FLIP CHIP module.

M903 — \$12

COAXIAL CABLE CONNECTOR M904

M SERIES



The M904 connector is a single sized, double sided board.

This connector provides high density cable connections using coaxial cable. Provisions are made for connection of two nine-conductor coaxial cables to this connector. Eighteen signal leads and grounds are used.

Signal: B1, D1, E1, H1, J1, L1, M1, P1, S1
D2, E2, H2, K2, M2, P2, S2, T2, V2

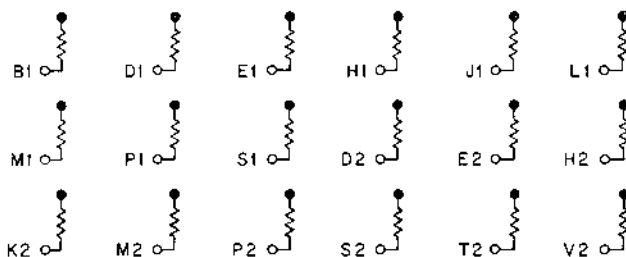
Common (ground): A1, C1, F1, K1, N1, R1, T1
C2, F2, J2, L2, N2, R2, U2

Size: Standard, single height, single width FLIP CHIP module.

M904 — \$14

CABLE TERMINATOR M906

M SERIES



The M906 cable terminator module contains 18 load resistors which are clamped to prevent excursions beyond +3V and ground. It may be used in conjunction with M623 to provide cable driving ability similar to M661 using fewer module slots.

The M906 may be used to terminate inputs. In this configuration, M906 and M111 are a good combination.

Inputs:

This module is normally used standard M-Series levels of 0 and +3V to partially terminate 100 ohm cable. It presents a load of 22.5 ma or 14 TTL unit loads at ground, and therefore, must be driven from at least an M617 type circuit, or preferably a cable driver.

The following pins MUST be grounded: A1, C1, F1, K1, N1, R1, T1
C2, F2, J2, L2, N2, R2, U2

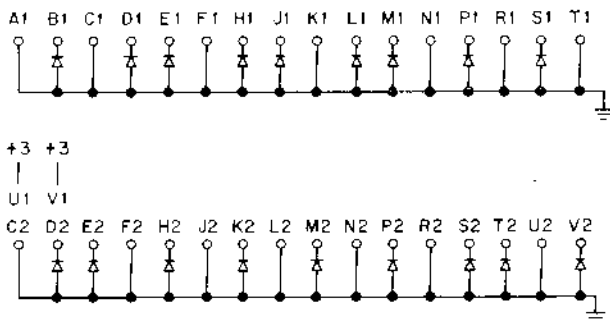
Power: +5V @ 440 ma. (max.) (all lines grounded).

Size: Standard, single height, single width FLIP CHIP module.

M906 — \$20

DIODE CLAMP CONNECTOR M907

M SERIES



The M907 is used to provide proper undershoot ground clamps for PDP8/I positive bus signals not using M103 or M101 inputs.

The M907 also provides +3V for clamping 25 unused inputs. Diode clamps appear on signal leads used in double-sided alternate ground I/O cables.

Diode clamp: B1, D1, E1, H1, J1, L1, M1, P1, S1,
D2, E2, H2, K2, M2, P2, S2, T2, V2

Ground: A1, C1, F1, K1, N1, R1, T1,
C2, F2, J2, L2, N2, R2, U2

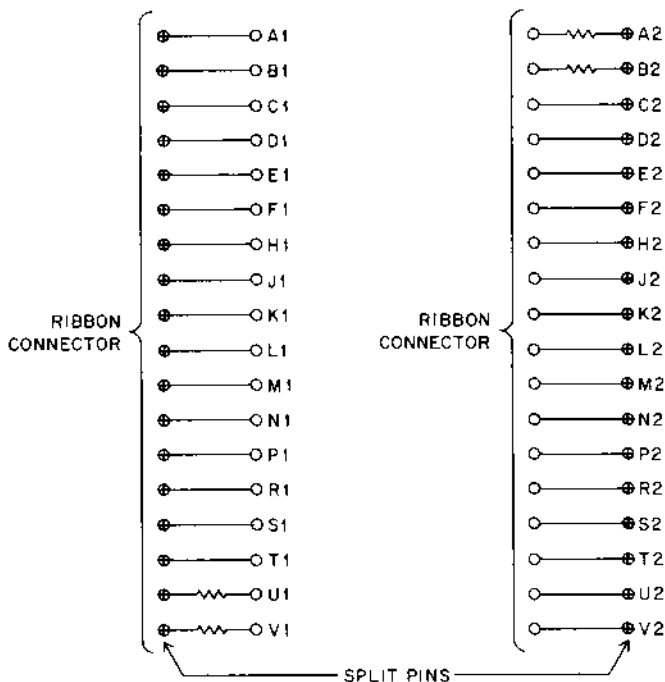
Power: +5V at 10.2 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

M907 — \$16

RIBBON CONNECTOR M908

M SERIES



The M908 cable connector consists of a single sized, double sided board which contains thirty-six split pins which allows the connection of thirty-six separate wires. All connections are made on the component side of the module. The 10 ohm, $\frac{1}{4}$ watt resistors connected in series with module pins A2, B2, U1 and V1 are provided to afford some measure of protection in the event that these pins are inadvertently connected to a source of supply voltage.

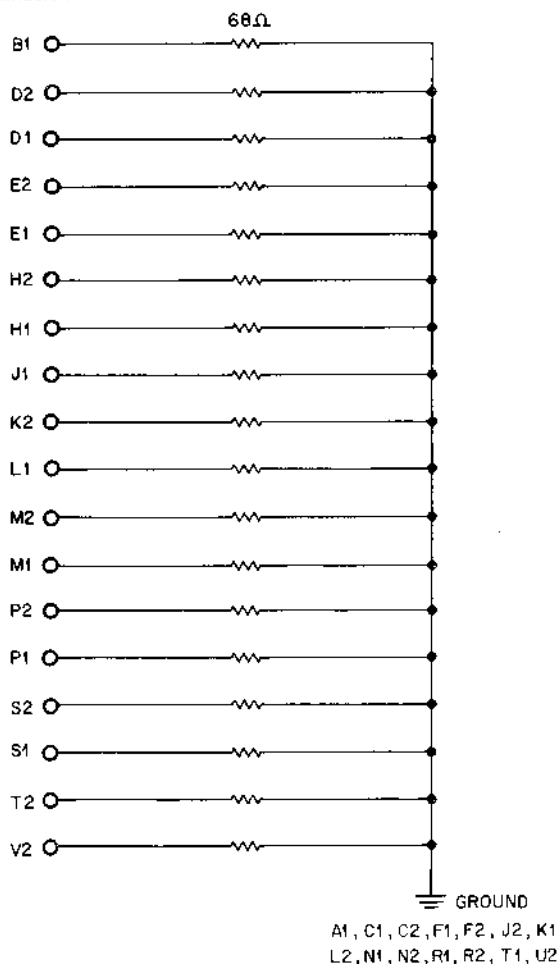
The M908 is primarily intended for use with ribbon cable and is normally supplied with a ribbon cable clamp unless otherwise specified.

Size: Standard, single height, single width FLIP CHIP module.

M908 — \$18

TERMINATOR M909

M SERIES



The M909 module contains 18 68Ω resistors. All 18 resistors are tied to ground through a common bus.

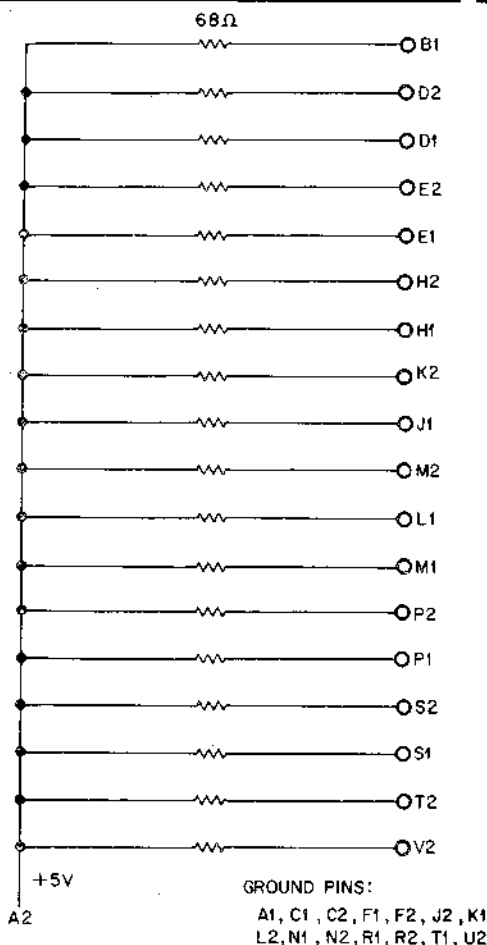
This module is used in conjunction with the M910 to form 1/2 of the biasing circuitry used in the driving network of the M622.

Size: Standard, single height, single width FLIP CHIP module.

M909 — \$14

TERMINATOR M910

M SERIES



The M910 module contains 18-68Ω resistors. All resistors are tied to a common +5 Volts bus.

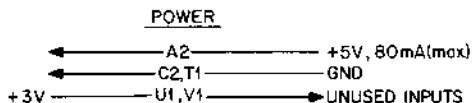
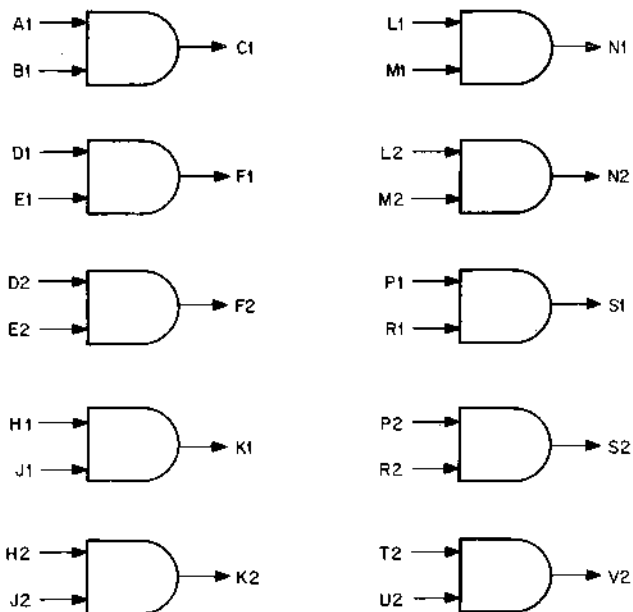
This module is used in conjunction with the M909 to form 1/2 of the biasing circuitry used in the driving network of the M622.

Size: Standard, single height, single width FLIP CHIP module.

M910—\$20

2-INPUT AND GATES M1103

M SERIES



The M1103 contains 10 2-input AND gates. Unused inputs on any gate must be returned to a source of logic "1" for maximum noise immunity. Two pins are provided (U1 and V1) as a source of +3 Volts for this purpose.

Inputs: Each input represents 1 TTL unit load.

Outputs: Each output can drive 10 TTL unit loads.

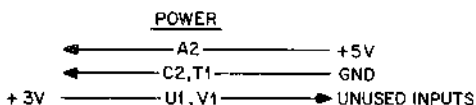
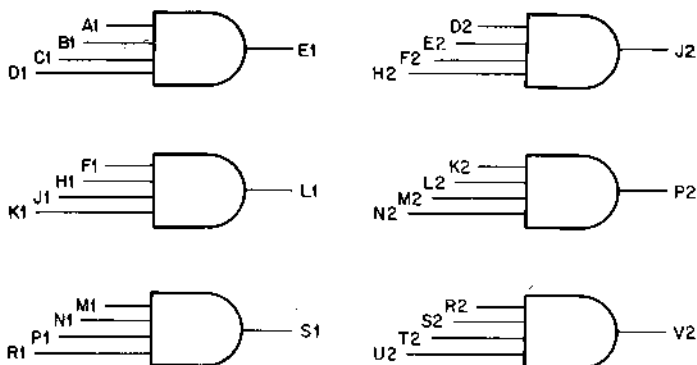
Power: +5 Volts @ 80 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

M1103—\$14

4-INPUT AND GATES M1307

M SERIES



The M1307 contains 6 4-input AND gates. Unused inputs on any gate must be returned to a source of logic "1" for maximum noise immunity. Two pins are provided (U1 and V1) as a source of +3 Volts for this purpose.

Inputs: Each input presents 1.25 TTL unit loads.

Outputs: Each output is capable of driving 12.5 TTL unit loads.

Power: +5 Volts @ 100 mA. (max.)

Size: Standard, single height, single width FLIP CHIP module.

M1307—\$12



The Module Assembly area has shifted emphasis from volume production to complex experimental work. The above process is a special sub-assembly of an indicator light board designed for a control unit.



W Series Special Purpose Logic Boards

**WIRE WRAPPABLE MODULES
W940-W943, W950-W951**

**W
SERIES**



W940

W941

These six wire wrappable boards with wire wrappable pins will accommodate dual-in line IC's. Two separate leads of 30-gauge may be wire wrapped to each pin. All boards have accommodations for 14 and/or 16 pin dual-in-line IC's.

However, the W950 and W951 boards also have accommodations for 24 pin dual-in-line IC's. Some boards are supplied with low profile IC sockets. The boards are designed to offer customer flexibility by providing additional pin locations for mounting discrete components, such as transistor sockets and potentiometers. These boards offer the user such advantages as easy construction of prototypes and low cost limited production runs. The following table describes each individual module:

**MODULES W940, W942
W950**

← AA2, BA2, CA2, DA2, — +5
 ← } AC2, AT1, BC2, BT1 { — GND
 ← } CC2, CT1, DC2, DT1 { — GND

**MODULES W941, W943
W951**

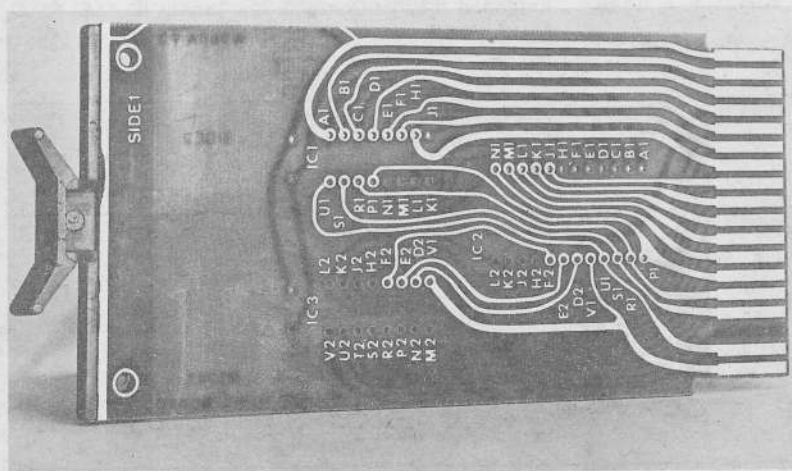
← AA2, BA2 — +5
 ← } AC2, AT1 { — GND
 ← } BC2, BT1 { — GND

MODULE	CONNECTOR PINS	SIZE	DESCRIPTION	PRICE
W940	144	Entended length Quad height	Accommodates up to 50 14 and/or 16 pin IC's with or without sockets. (sockets not included)	\$70.00
W941	72	Entended length Double height	Accommodates up to 25 14 and/or 16 pin IC's with or without sockets. (sockets not included)	\$40.00
W942	144	Entended length Quad height	Contains low profile IC sockets. Accommodates up to 50 14 and/or 16 pin IC's	\$140.00
W943	72	Entended length Double height	Contains low profile IC sockets. Accommodates up to 25 14 and/or 16 pin IC's	\$75.00
W950	144	Entended length Quad height	Has 30 14 and/or 16 pin type accommodations. Also contains 8 24 pin type accommodations that can also accommo- date 14 and/or 16 pin IC's. IC's may be mounted with or without sockets (sockets not included).	\$65.00
W951	72	Entended length Double height	Has 15 14 and/or 16 pin type accommodations. Also contains 4 24 pin type accommodations that can also accommo- date 14 and/or 16 pin IC's. IC's may be mounted with or without sockets (sockets not included).	\$40.00

MSI MOUNTING BOARD W960

W SERIES

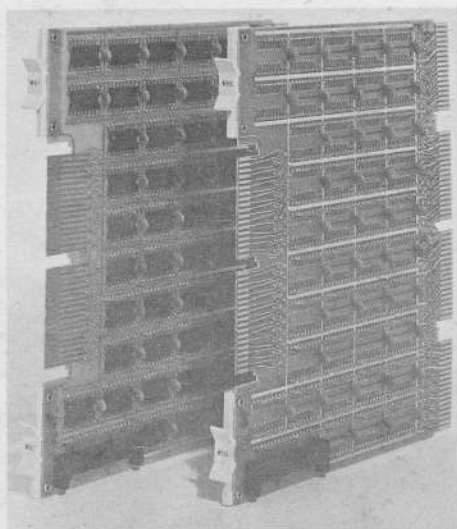
The W960 is a single-height, standard-length, double-sided PC board that can accommodate either two 14 or 16 pin dual-in-line IC's, or one 24 pin dual-in-line IC with or without socket(s). All IC pins are brought out to connector pins.



W960 — \$8

WIRE WRAPPABLE MODULES W966, W967

W SERIES

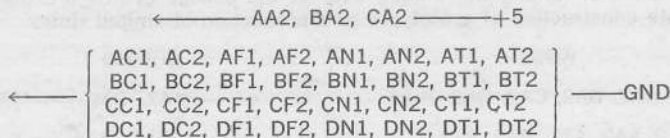


W967

W966

The W966 is the 8/e collage mounting board. It is double sided, extended length, and quad height with wire wrappable pins. It will accommodate 14 and/or 16 pin dual-in-line IC's with or without 16 pin sockets. Two separate leads may be wire wrapped to each pin. Up to 42 IC's can be mounted on the W966. Discrete components may be directly soldered onto the board. The top center of the W966 board has 72 terminal fingers with terminating wire wrap pins. An I/O connector (male) terminating in wire wrap pins is mounted on the left side of the W966 board to provide access to the "outside world" when using BC08J-XX cable with a double sided connector board or a BC08K-XX single sided connector board. Both connector boards have 18 conductor lines.

All power and ground lines are common to the 8/E "OMNIBUS".



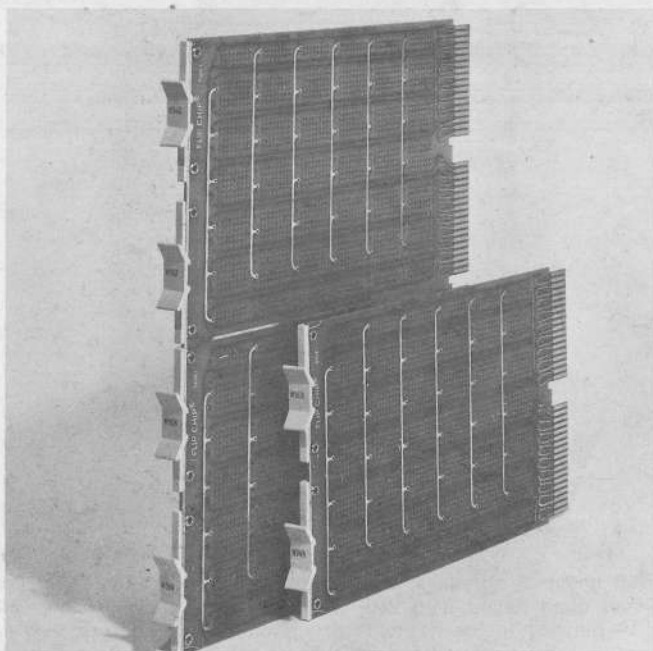
The W967 is similar in all details to the W966 except that the W967 is supplied with 42 low profile IC sockets.

W966 — \$85

W967 — \$165

COLLAGE MOUNTING BOARDS W968, W969

W SERIES



W968

W969

The W968 and W969 collage mounting boards will accommodate 14 and/or 16 pin dual-in line IC's with or without 16 pin wire wrap sockets and/or solder sockets. The W968 is a double-sided, quad-height, extended length board and can accommodate up to 72 IC's.

The W969 is the double-height version of the W968 and can accommodate up to 36 IC's. Among the unique uses of the collage boards are that they facilitate construction of prototypes and production of limited runs.

W968

W969

← AA2, BA2, CA2, DA2 —+5

← AA2, BA2 —+5

← { AA2, AT1, BA2, BT1 }
{ CA2, CT1, DA2, DT1 } —GND

← { AA2, AT1 }
{ BA2, BT1 } —GND

W968—\$45

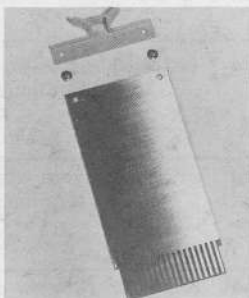
W969—\$30

BLANK MODULES
W970-W975, W990-W999

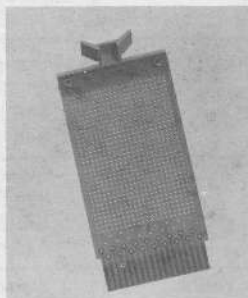
W
SERIES



W990



W992



W998

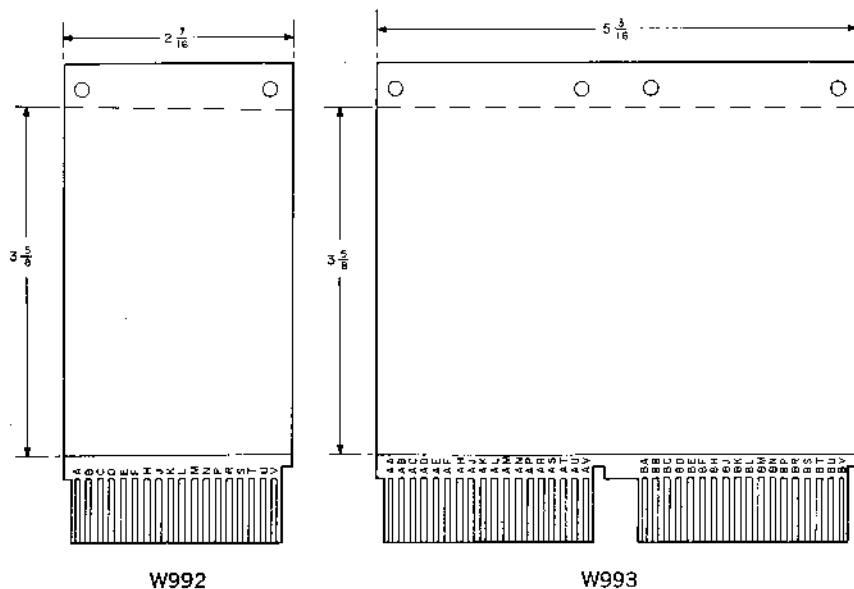
These 10 blank modules offer convenient means of integrating special circuits and even small mechanical components into a FLIP CHIP system, without loss of modularity. Both single- and double-size boards are supplied with contact area etched and gold plated. The W990 Series modules provide connector pins on only one module side for use with H800 connector blocks. W970 series modules have etched contacts on both sides of the module for use with double density connectors Type H803, and low density Type H808.

Module	Con- nector Pins	Size	Handle	Description	Price
W970	36	Standard length Single height	Attached	Bare board, no split lugs, similar to W990.	\$ 4.00
W971	72	Standard length Double height	Attached	Bare board, no split lugs, similar to W991.	\$ 8.00
W972	36	Standard length Single height	Separate	Copper clad, similar to W992.	\$ 4.00
W973	72	Standard length Double height	Separate	Copper clad, similar to W993.	\$ 6.00
W974	36	Standard length Single height	Attached	Same as W998, contact both sides.	\$ 9.00

Module	Con- nector Pins	Size	Handle	Description	Price
W975	72	Standard length Double height	Attached	Same as W999, contact both sides.	\$18.00
W990	18	Standard length Single height	Attached	Bare board, split lug terminals.	\$ 2.50
W991	36	Standard length Double height	Attached	Bare board, split lug terminals.	\$ 5.00
W992	18	Standard length Single height	Separate	Copper clad, to be etched by user.	\$ 2.00
W993	36	Standard length Double height	Separate	Copper clad, to be etched by user.	\$ 4.00
W998	18	Standard length Single height	Attached	Perforated, 0.052" holes, 18 with etched lands. The holes are on 0.1" centers, both horizontally and vertically.	\$ 4.50
W999	36	Standard length Double height	Attached	Perforated, 0.052" holes, 36 with etched lands. The holes are on 0.1" centers, both horizontally and vertically.	\$ 9.00

**BLANK COPPER CLAD MODULES
W972, W973, W992, W993**

**W
SERIES**



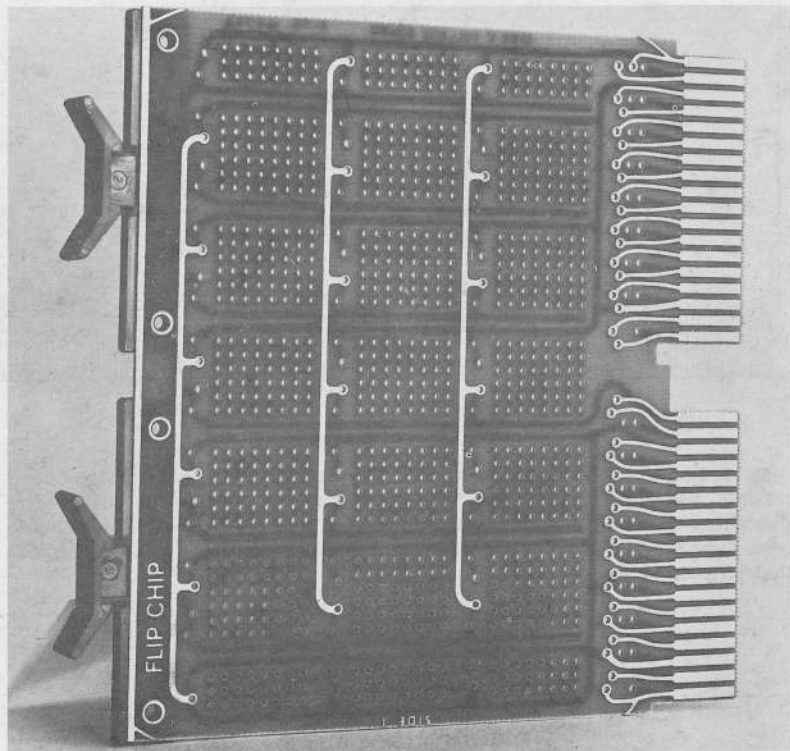
Type W992 and W993 are single side copper clad boards. The diagrams above indicate the copper clad area that is usable for etching purposes. The identifying numbers are etched from the clad using a minimum of etchable area. Type W972 and W973 are equivalent to the above types but have copper clad on both sides.

W972	— \$4
W973	— \$6
W992	— \$2
W993	— \$4

**COLLAGE MOUNTING BOARD
W979**

**W
SERIES**

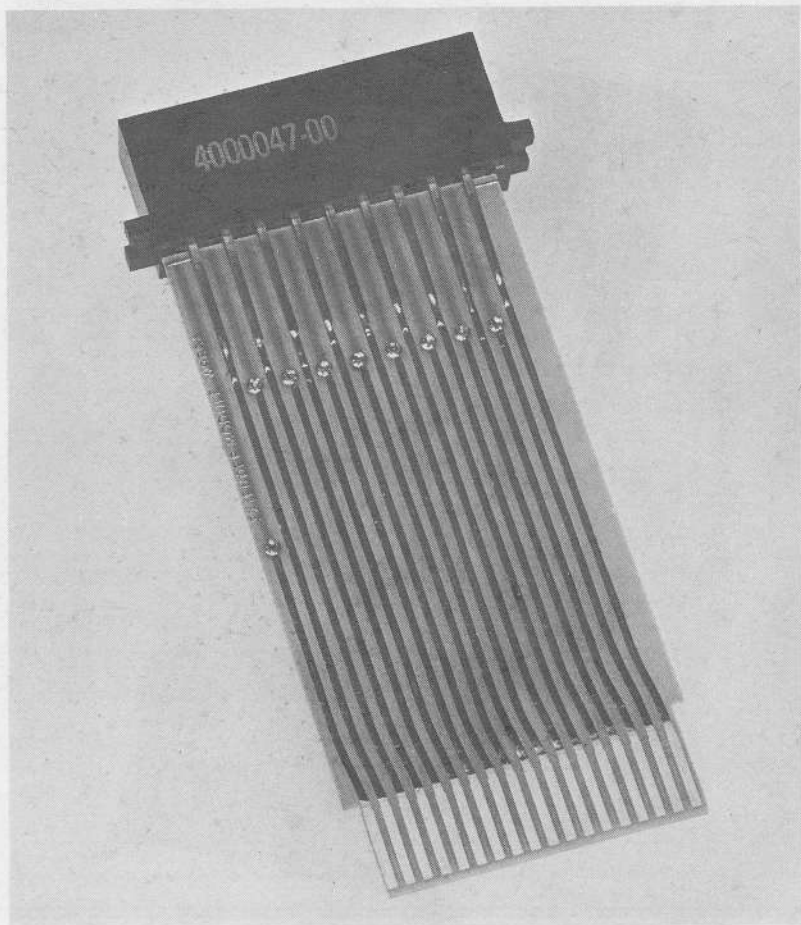
The W979 Collage Mounting Board will accommodate 14 and/or 16 pin dual-in-line IC's with or without 16 pin wire wrap sockets and/or solder sockets. It is the double-height, standard-length version of the W969.



W979 — \$20

**MODULE EXTENDER
W980**

**W
SERIES**



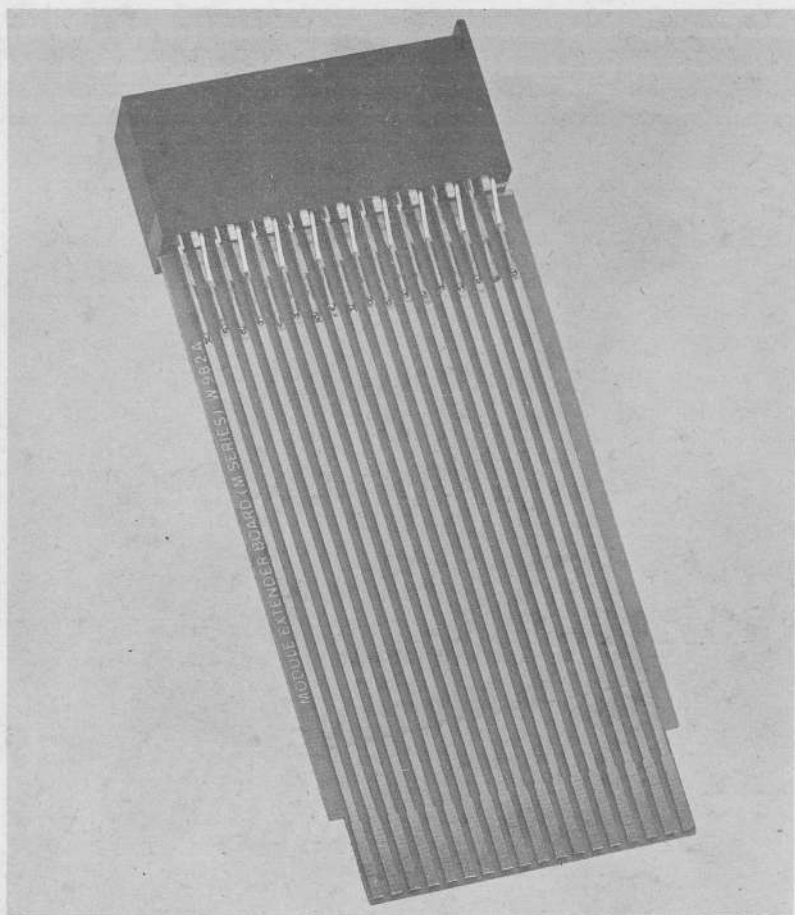
The W980 Module Extender allows access to the module circuits without breaking connections between the module and mounting panel wiring.

For double size flip-chip modules use two W980 extenders side by side. The W980 is for use with A, K and W Series 18 pin modules.

W980 — \$14

**MODULE EXTENDER
W982**

**W
SERIES**



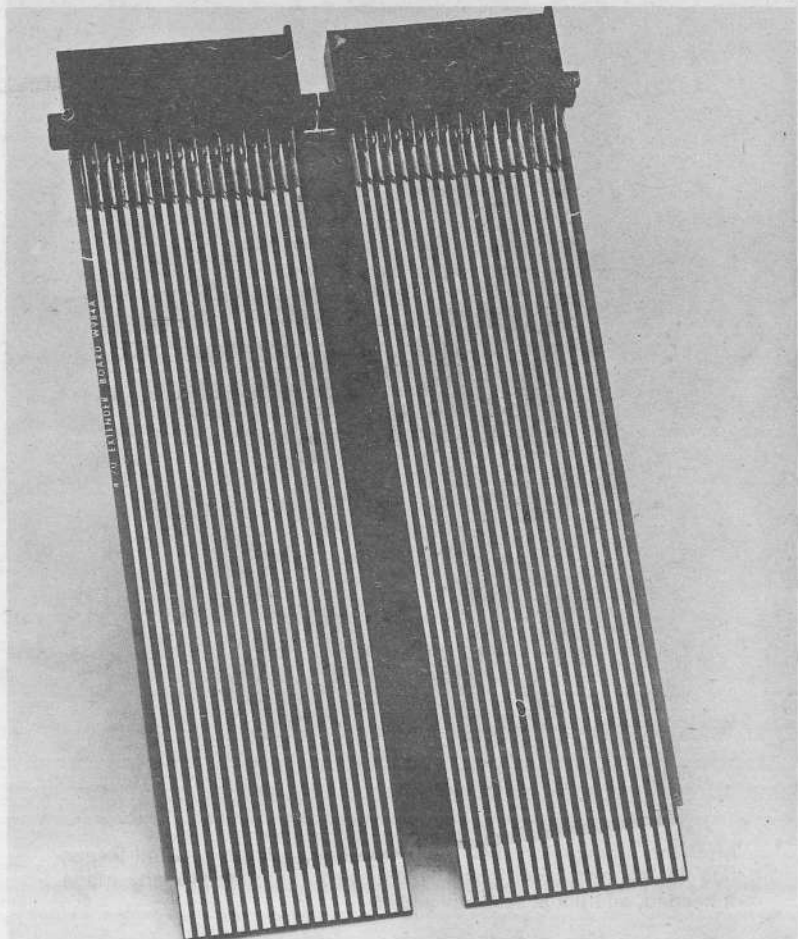
The W982 serves a function similar to the W980 except it contains 36 pins for use with M series modules. The W982 can be used with all modules in this catalog. A, K, and W series modules will make contact with only 2 side pins. A2, B2, etc.

W982 — \$18

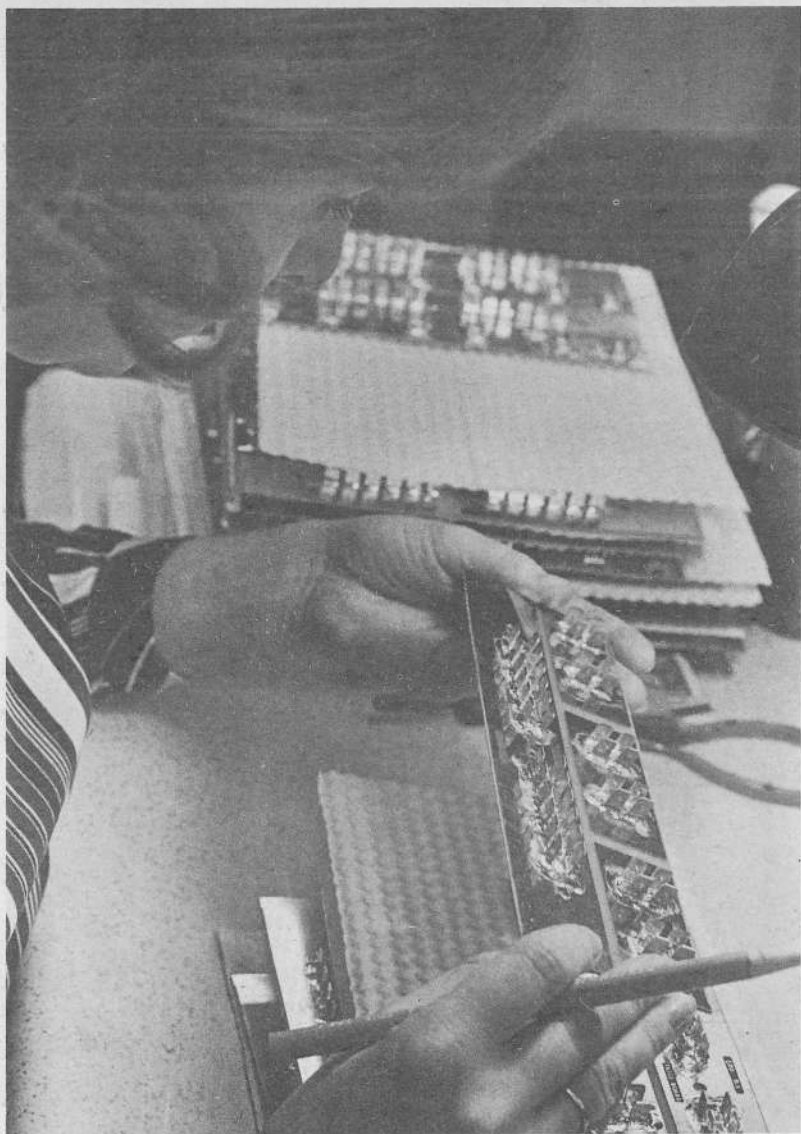
**MODULE EXTENDER
W984**

**W
SERIES**

The W984 Module Extender allows access to the module circuits without breaking connections between the module and module panel wiring. It is double height and extended length with 72 connector pins for double height M Series modules. For single height M Series modules use the W982 Module Extender.



W984—\$30



After the modules are flow-soldered, they undergo a visual inspection to insure that all solder points and runs are properly made. If needed, additional solder is added.

Hardware, Accessories and Power Supplies

Digital manufactures a complete line of hardware accessories in support of its module series. Module connectors are available for as few as one module and as many as 64 in a single rack (H020). A complete line of cabinets is available to house the modules and their connector blocks, as well as providing a convenient means for system expansion. Power supplies for both large and small systems and reference supplies are also available.

Coupled with the recent additions to the hardware line, Digital has made every effort to maintain or improve the high standards of reliability and performance of its present line. Through the availability of a wide range of basic accessories, DEC feels that it is offering the logic designer the necessary building blocks which he requires for complete system design.

50-CYCLE POWER

Because of the demand for Digital's products in areas where 115-V, 60-cps power is not available, each of the power supplies with a frequency-sensitive regulating transformer is also available in a multi-voltage 50-cps version. All 50-cps supplies have the same input connections. The line input is on pins 3 and 4. Jumpers should be connected depending on the input voltage. These connections are shown below along with a schematic.

WIRING HINTS

These suggestions may help reduce mounting panel wiring time. They are not intended to replace any special wiring instructions given on individual module data sheets or in application notes. For fastest and neatest wiring, the following order is recommended.

- (1) All power & ground wiring and any horizontally bussed signal wiring. Use Horizontal Bussing Strips Type 932 for type H800, 933 for type H803, or 939 for type H808.
- (2) Vertical grounding wires interconnecting each chassis ground with pin C grounds. Start these wires at the uppermost mounting panel and continue to the bottom panel. Space the wires 2 inches apart, so each of the chassis-ground pins is in line with one of them. Each vertical ground wire makes three connections at each mounting panel.
- (3) All other ground wires. Always use the nearest pin C above the pin to be grounded, unless a special grounding pin has been provided in the module.
- (4) All signal wires in any convenient order. Point-to-point wiring produces the shortest wire lengths, goes in the fastest, is easiest to trace and change, and generally results in better appearance and performance than cabled wiring. Point-to-point wiring is strongly urged.

The wire size for use with the H800 connector blocks and 1943 mounting panel is 24 for wire wrap, and 22 for soldering. The size for use with H803 block and H911 mounting panel is #30 wire. Larger or smaller wire may be used depending on the number of connections to be made to each lug. Solid wire and a heat resistant spaghetti (Teflon) are easiest to use when soldering.

Adequate grounding is essential. In addition to the connection between mounting panels mentioned above, there must be continuity of grounds between cabinets and between the logic assembly and any equipment with which the logic communicates.

When soldering is done on a mounting panel containing modules, a 6-V (transformer) soldering iron should be used. A 110-V soldering iron may damage the modules.

When wire wrapping is done on a mounting panel containing modules, steps must be taken to avoid voltage transients that can burn out transistors. A battery- or air-operated tool is preferred, but the filter built into some line-operated tools affords some protection.

Even with completely isolated tools, such as those operated by batteries or compressed air, a static charge can often build up and burn out semiconductors. In order to prevent damage, the wire wrap tool should be grounded except when all modules are removed from the mounting panel during wire wrapping.

AUTOMATIC WIRING

Significant cost savings can be realized in quantity production if the newest automatic wiring techniques are utilized. Every user of FLIP CHIP modules benefits from the extensive investment in high-production machinery at Digital, but some can go a step further by taking advantage of programmed wiring for their FLIP CHIP digital systems.

While the break-even point for hand wiring versus programmed wiring depends upon many factors that are difficult to predict precisely, there are a few indications:

1. One-of-a-kind systems will probably not be economical with automatic wiring, unless a customer has high overhead costs and performs a time-consuming (costly) hand assembly.
2. At the other end of the spectrum, production of 50 or 100 identical systems of almost any size would be worth automating, not only to lower the cost of the wiring itself but also to reduce human error. At this level of volume, machine-wired costs can be expected to be considerably less than the cost of hand wiring.
3. For two to five systems of several thousand wires each, a decision on the basis of secondary factors will probably be necessary: ease of making changes, wiring lead time, reliability predictions, and availability of relevant skills are factors to consider.

Digital can supply further information to those interested in programmed wiring techniques. Contact the Module Marketing Manager, Module Products Group.

COOLING OF FLIP CHIP MODULES

The low power consumption of K and M series modules results in a total of only about 25 watts dissipation in a typical 1943 Mounting Panel with 64 modules. This allows up to six panels of modules to be mounted together and cooled by convection alone, if air is allowed to circulate freely. In higher-dissipation systems using modules in significant quantities from the A series, the number of mounting panels stacked together must be reduced without forced-air cooling. In general, total dissipation from all modules in a convection-cooled system should be 150 watts or less.

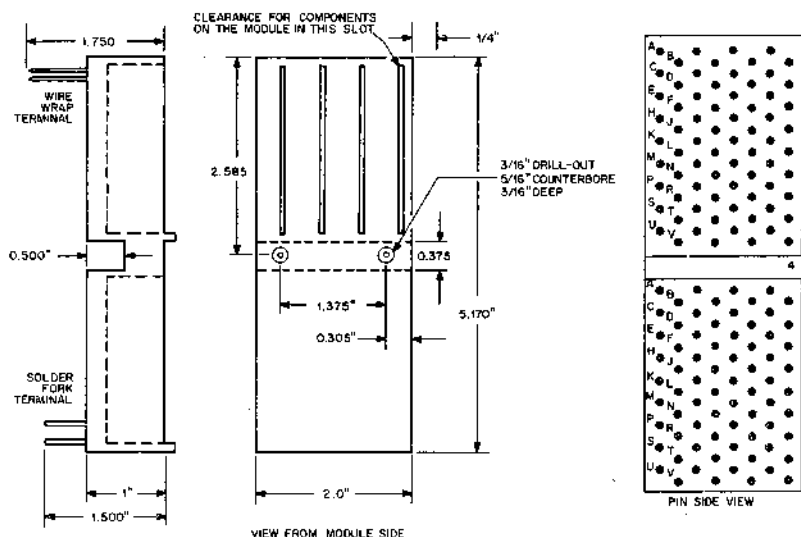
The regulating transformers used in most DEC power supplies have nearly constant heat dissipation for any loading within the ratings of the supply. Power dissipated within each supply will be roughly equal to half its maximum rated output power. If power supplies are mounted below any of the modules in a convection-cooled system, this dissipation must be included when checking against the 150 watt limit.

CONNECTOR BLOCKS H800-W, H800-F

HARDWARE

This is the 8-module socket assembly used in Flip-Chip® mounting panels. Because of its 18 pin connectors, it can be used for all modules except those with pins on both sides of the board. Pin dimensions are .031 inches by .062 inches and may be of either a wire trap or solder fork type. Number 24 awg. gauge wire should be used with these connectors.

The drawings below show the pertinent dimensions.



REPLACEMENT CONTACTS TYPES H801-W, H801-F

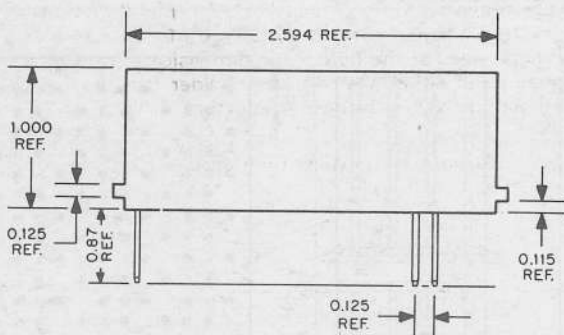
These contacts are offered in packages of 18 for replacement purposes. In each package, nine straight and nine offset contacts are included, enough to replace all contacts in one socket.

H801-W is for wire-wrap connectors; H801-F is for solder-fork connectors.

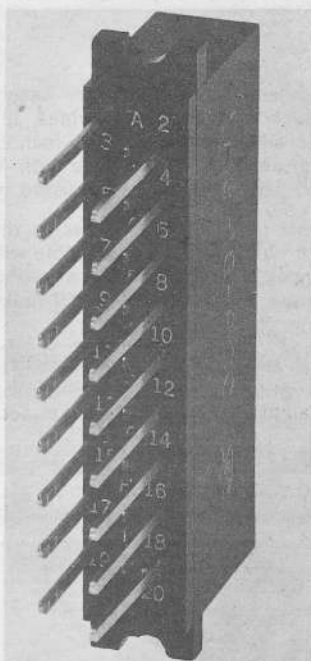
H800F	—\$8
H800W	—\$8
H801F	—\$2
H801W	—\$2

CONNECTOR BLOCK H802

HARDWARE



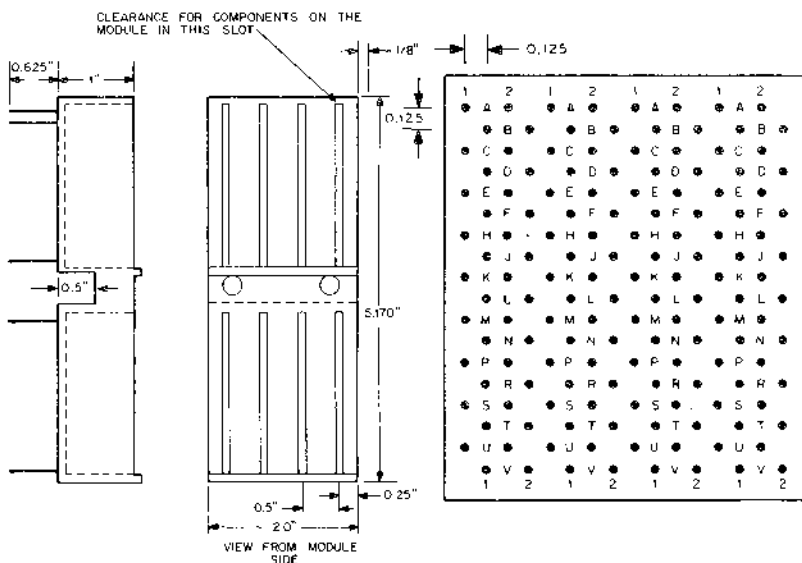
This is an 18 pin connector block for a single FLIP CHIP® module. It can be used to mount all modules except those with pins on both sides of the board. Pin dimensions are .031 inches by .062 inches and may be of the wire wrap type only. Number 24 wire should be used with this connector.



H802—\$4

CONNECTOR BLOCK H803, AND H805 PINS

HARDWARE



The H803 is the 8-module molded Connector Assembly used in the H911 mounting panels. For each of the eight modules, it provides a 36-pin connector with the wirewrap pins forming a 0.125-inch staggered grid as shown above. This connector is designed to be used with M Series modules; however, it can also be used with all other series listed in this handbook.

The blocks have the same physical dimensions as the H800 with the exception of pin length. These blocks are only available with wire wrap pins which are designed to be wrapped with number 30 wire. Pin dimensions are 0.025 inches square. W&K Series 18 pin modules will make contact with only the 2-side pins (A2, B2, etc.).

H805 is a package of 36 pins (18 left and 18 right) to be used as replacements in H803 blocks.

H803 — \$13
H805 — \$4

**CONNECTOR BLOCK
H807, H808 AND H809 PINS**

HARDWARE

H807

This is a 36 pin single shot connector. It is provided for M Series modules but can be used with modules or connector boards in the K and W Series. Uses include mounting in confined or irregular spaces. Often the H807 is used to terminate a connector board at a remote location. The H807 is available only with wire wrap pins. Number 30 wire should be used with this connector.

H808

The H808 is a relatively low density connector block for use with all modules in the catalog. This includes A, K, M, and W Series modules. The connector provides 4 module slots each having 36 pins. On A, K and W Series modules only the 2 side pins, (A2, B2, etc.) will make contact. This connector adds a measure of convenience and versatility to the many uses to which these catalog modules can be applied. The dimensions of the connector pins are the same as those for the H800 (.031 inches by .062 inches). Number 24 wire should be used with these blocks, H800 and H808 connector blocks can be mixed for M and A, K, W module mixing purposes. Wire wrapping patterns can be maintained even though module letter series are mixed because H800 and H808 pin layout is identical. H809 is a package of 36 replacement pins, 18 left and 18 right.

H807 — \$5
H808 — \$10
H809 — \$ 4

MOUNTING PANEL HARDWARE H001, H002, H020, H021, H022 AND 1907 COVER

HARDWARE

Pairs of brackets. H001 provides $\frac{3}{4}$ " standoff to mount 1907 over mounting panel wiring. H002 provides a 2" setback so a control panel with switches, lamps, etc. can be mounted flush with mounting rack or cabinet in front of logic wiring.

The H020 consists of a 19" mounting frame casting. Components which can be mounted on this frame include, H800, H803, H808 connector blocks, power supplies or customer components that are adapted to the frame mounting requirements.

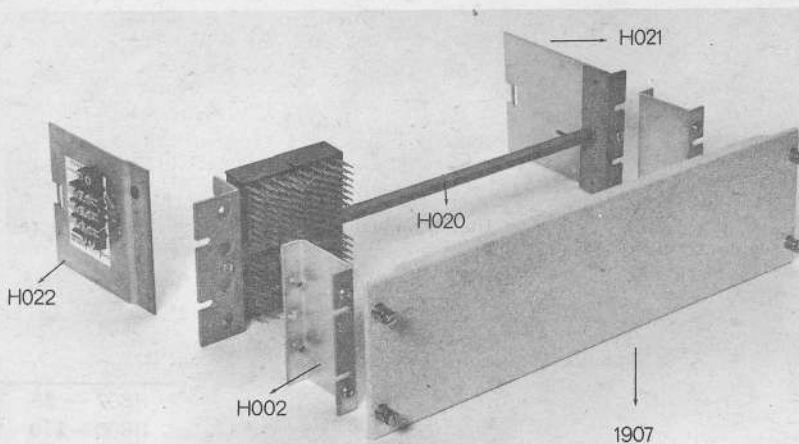
H021—Single offset end plate which mounts to the H020. This end plate provides a mount for the 1945-19 hold down bar, if required.

H022—Single end plate similar to the H021 on which is mounted a terminal block assembly for ease of parallel power wiring to adjacent panels.

1945-19 HOLD DOWN BAR: Reduces vibration and keeps modules securely mounted when panel or system is moved. Adds $\frac{1}{2}$ in. to depth of mounting panel.

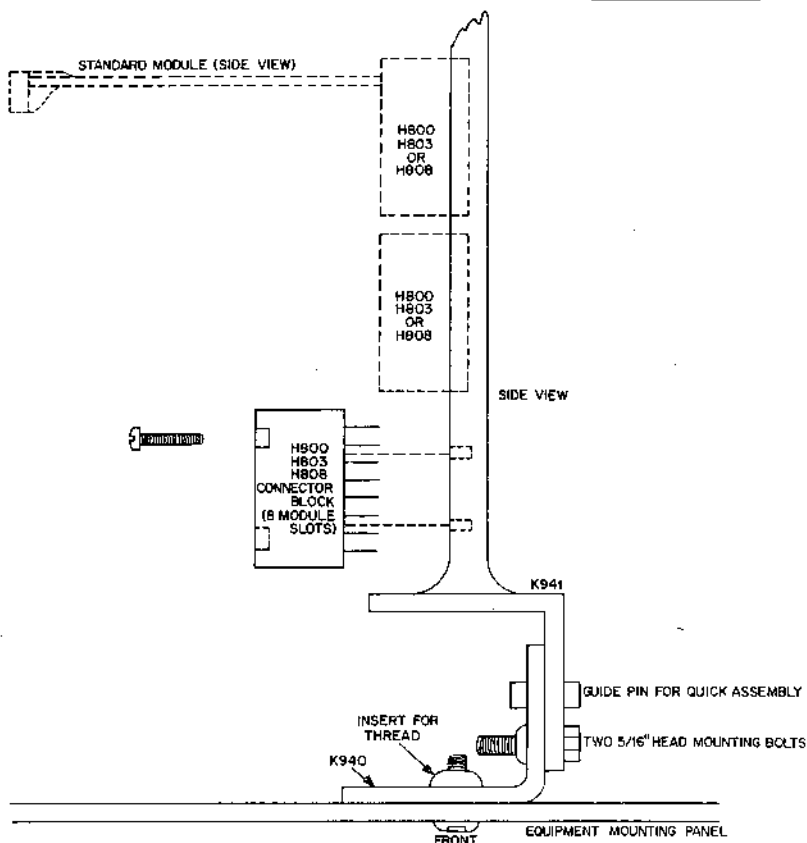
1907 Panel Cover—Blue or brown tweed painted aluminum cover with captive screws to mate threaded bushings in K980 and H001. Adds to appearance while protecting system against vibration and tampering. When choice of color is not specified, blue will be supplied.

H001-PR — \$8	H022 — \$20
H002-PR — \$8	1945-19 — \$15
H020 — \$15	1907 — \$9
H021 — \$7	



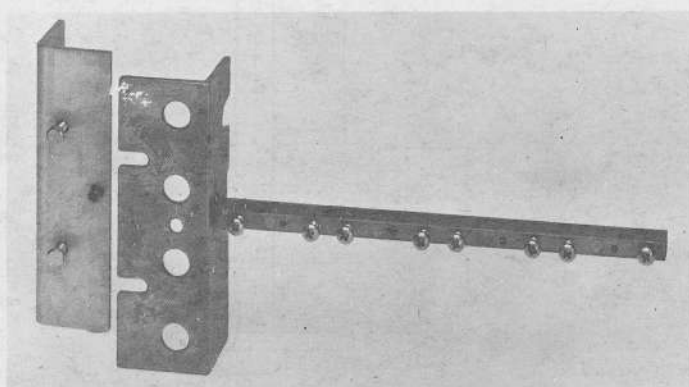
MOUNTING HARDWARE K940, K941

HARDWARE



This convenient mounting hardware permits logic connector pin wiring to be done before logic is installed in the enclosure.

K940 is a mounting support that attaches to the enclosure. K941 is a removable bracket that mounts up to four H800, H803, or H808 connector blocks. Any connections to external equipment are made through the ribbon connectors of interface signal modules (K508, K524, K604, K644) to the K716 Interface Block.



↑
K 940

↑
K 941

TOP VIEW

K940—\$4
K941—\$6

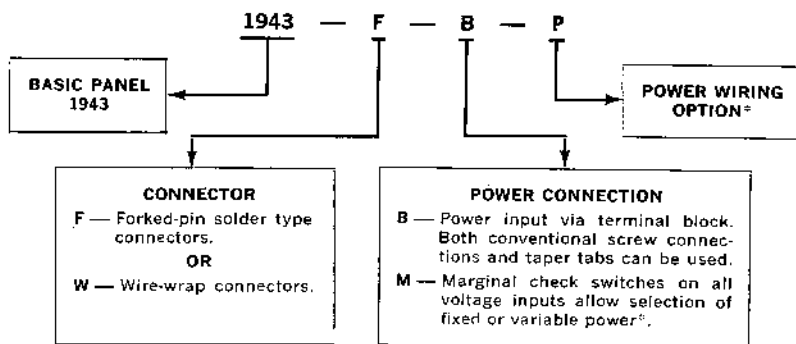
MOUNTING PANEL 1943

HARDWARE

TYPE 1943 MOUNTING PANEL

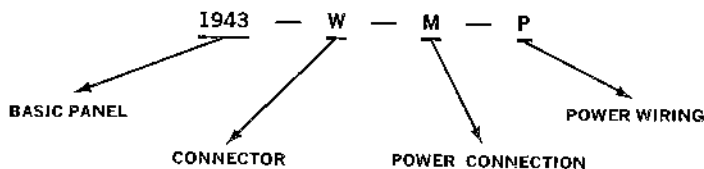
The 1943 Mounting Panel consists of an H020 that houses up to 64 modules. It is designed for mounting in a standard 19-in. rack. The mounting panel is finished with an aluminum conversion coating (Chromicoat). Filter capacitors are included on all power supply lines.

Available options are solder or wire-wrap connectors, power input via terminal strip or marginal check switches, and power wiring. The chart below shows how the options are indicated when ordering.



^aAdditional charge.

EXAMPLE: If you require a Type 1943 Mounting Panel with wire-wrap connectors, marginal check switches on the power connection, and prewired power, you would order:

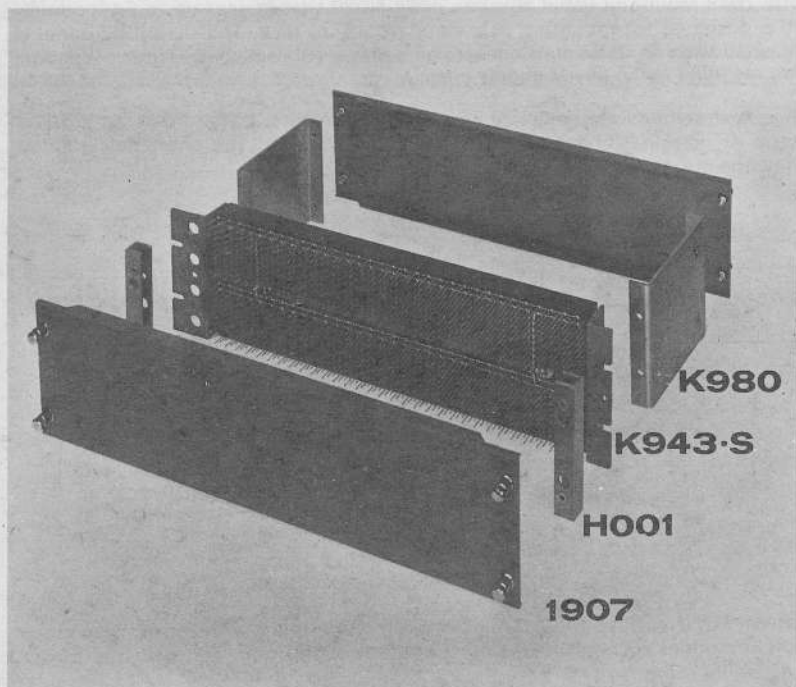


MECHANICAL DIMENSIONS: 19 in. wide; 5-3/16 in. high; 6-3/4 in. deep. Tabs for power connections fit AMP "Faston" receptacles, series 250, part 41774 or Type 914 power jumpers.

1943-F-B	— \$111.00	1943-F-M	— \$132.00
1943-W-B	— \$111.00	1943-W-M	— \$132.00
1943-F-B-P	— \$121.00	1943-F-M-P	— \$142.00
1943-W-B-P	— \$121.00	1943-W-M-P	— \$142.00

**19" MOUNTING PANEL
K943-R, K943-S**

HARDWARE



These low cost, 19" panels have sixty-four 18 pin connector sockets with either wire-wrap (S) or solder fork (R) contact pins. Shipped with connector blocks installed and pins A and C bussed.

No terminal strips are included in the K943, since power regulators K731 and K732 will normally be plugged in to make power connections. If hold-down is required to prevent modules from backing out under vibration, order a pair of end plates K980. These assemble by means of added nuts on the rear of the rack mount screws. They accept the painted 1907 cover plate, making a hold-down system that contacts the module handles and can allow flexprint cables to be threaded neatly out the end. Rack space: $5\frac{1}{4}$ ". See photos showing K943-S, K980, 1907, and H001.

K943R — \$96
K943S — \$96

**MOUNTING PANEL
H911-J, H911-K**

HARDWARE

The H911 mounting panel uses eight H803 connector blocks and houses sixty four, 36 pin connectors. Mechanical dimensions are identical to those of the H910.

The H911 is available with wire wrap pins only, and is generally used for M Series modules.

The unit is a combination of the following parts:

H020 — Mounting frame

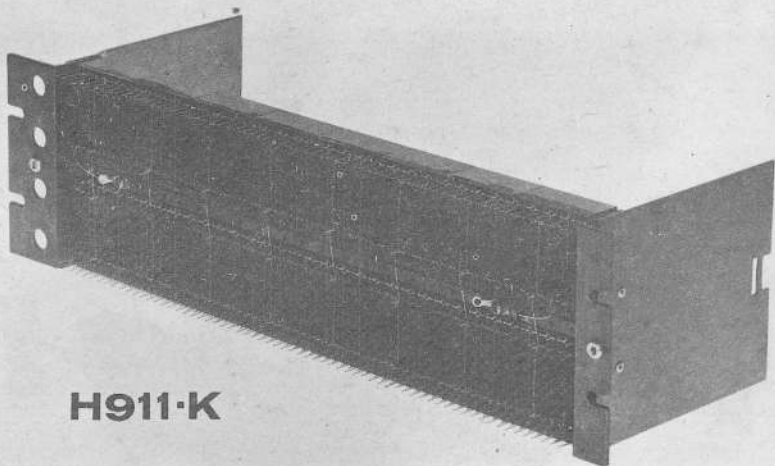
H021 — Standoffs

H803 — Connector blocks

933 — Bussing strips (optional with H022 standoff)

The H911J is not prewired or bussed for power.

The H911K does have prewired power.



933 BUS STRIP — For H911 mounting panel, makes wiring power and register pulse busses easy.

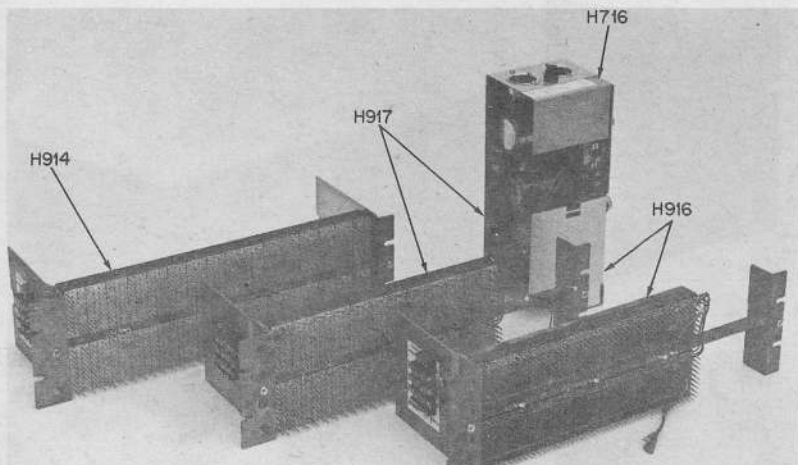
Consult following table for mounting panel options and ordering information.

H911J — \$151
H911K — \$161

MOUNTING PANEL H914, H916 & H917

HARDWARE

- H914 — This panel houses 8 low density H808 connector blocks. The panel will hold 32 of either A, K, M or W Series modules. It can be used for expanding slot capacity in conjunction with H913 or alone using other voltage supply options, e. g. K731 and K732 combinations. Mechanical characteristics are like those of the H911.
- H916 — This panel contains an H716 power supply and 6 H803 (green) connector blocks. The unit provides for forty-eight, 36 pin module slots. Although generally used for mixes of M and A series modules, K and W series modules can also be accommodated.
- H917 — This panel is similar to the H916 panel except 6 low density H808 connector blocks are supplied instead of H803 blocks. With these connector blocks, 24 module slots are available, allowing the use of any module series. Electrical and mechanical characteristics are similar to those of type H916 with the exception of the connector blocks.



H913	—	\$270
H914	—	\$125
H916	—	\$270
H917	—	\$260

**TABLE OF MOUNTING PANELS
WITH & WITHOUT POWER SUPPLY**

ORDER NO.		AVAILABLE VARIATIONS						PRICE
PANEL	ORDER LETTER	X	V	F	W	B	P	
H911	J	*			*	*		\$151
H911	K	*			*	*	*	\$161
H914	L	*			*	*		\$125
H916	M		*		*	*	*	\$270
H917	N		*		*	*	*	\$260
K943	R	*		*			*	\$ 96
K943	S	*			*		*	\$ 96
1943	(see page 215 for details)							

X = NO POWER
V = POWER OPTION
 105-125 VAC OR
 210-250 VAC
 47-63 Hz

P — PREWIRED FOR POWER

F — SOLDER FORKED
 CONNECTIONS
W — WIRE WRAP
 CONNECTIONS

B — POWER INPUT VIA TERMINAL
 BLOCK. BOTH CONVENTIONAL
 SCREW CONNECTIONS AND
 TAPER TABS CAN BE USED

Example Order: H911KX

This describes a Type H020 casting with 8 Type H803 wire wrap connectors and ground wired to a terminal block incorporated into the end plate assembly.

**SYSTEMS UNIT
MOUNTING PANEL
H933**

HARDWARE

The H933 is a special 16½" x 2¼" systems unit casting which contains three connector blocks of any one type. The table below shows the various types of H933 panels and the number of connector slots in each.

PANEL	TYPE CONNECTORS	CONNECTOR SLOTS
H933-A	H800W	24-18 pin
H933-B	H800F	24-18 pin
H933-C	H803	24-36 pin
H933-D	H808	12-36 pin

H933-A — \$37
H933-B — \$37
H933-C — \$54
H933-D — \$42

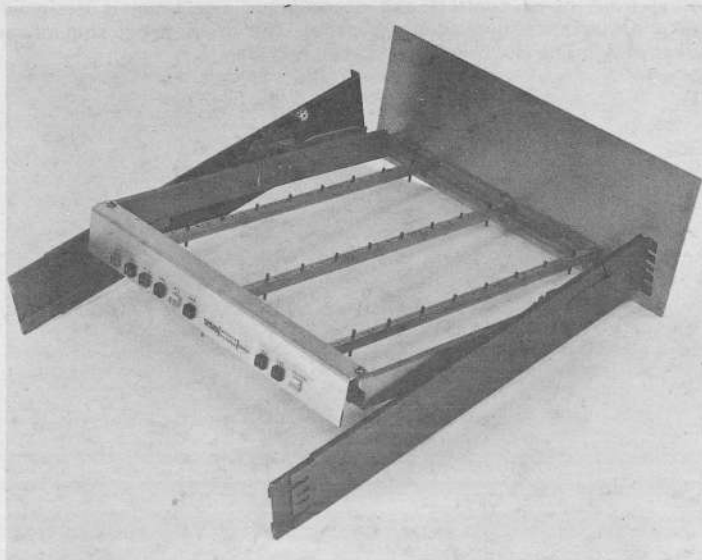
MODULE DRAWER H920

HARDWARE

The H920 Module Drawer provides a convenient mounting arrangement for a complete digital logic system. The H920 has space for 20 mounting blocks in addition to an H710, or H716 power supply, or 24 mounting blocks without a supply. It accepts H800, H803, and H808 mounting blocks and fits standard 19" racks. Width of the H920 is 16 $\frac{3}{4}$ ", depth is 19" and height is 6 $\frac{3}{4}$ " including an H921 front panel. The H920 is equipped with a bracket for distributing power within the drawer, or to other drawers or mounting panels. Mounting arrangements are provided for the H921 front panel and H923 slide tracks.

The H921 front panel is designed for use primarily with the H920 Module Drawer. It provides mounting space for switches, indicators, etc. The H921 is pre-drilled and ready to mount on the H920. Height of the H921 is 6 $\frac{3}{4}$ ", width is 19".

H923 chassis slides are intended for use with the H920 Module Drawer. The H923 allows the user to slide the drawer out of the rack and tilt the drawer for easy access to either the pin or module side.



H920	—\$170
H921	—\$ 10
H923	—\$ 75

MODULE DRAWER H925

HARDWARE

The H925 Module Drawer provides mounting space for H800, H803, and H808 connector blocks to accommodate up to 144 modules. The connector blocks mount pins upward on the H925 for easy access during system checkout.

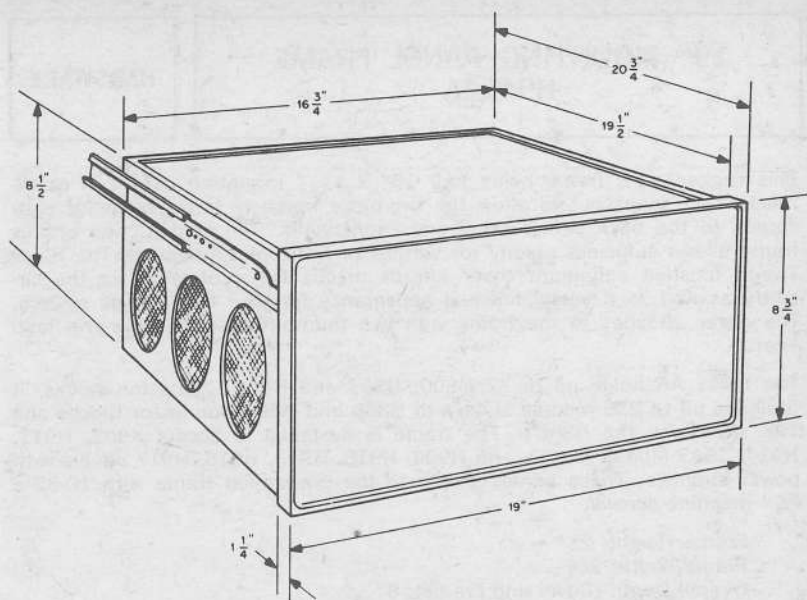
The right side of the H925 is provided with three axial flow fans (300 cfm) which are mounted internally. They provide cooling air flow across the mounted modules.

For power supply mounting in the H925 cabinet, omit 4 connector blocks thereby deleting 32 module slots, when using the H800 or H803 connector blocks. If the H808 blocks are used, 16 module slots are deleted. Mount the power supply externally if all logic mounting space is required.

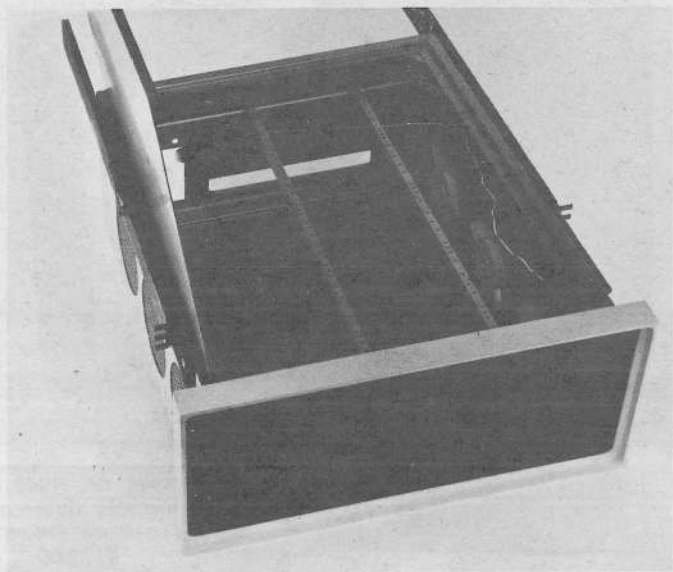
For ease of mounting, the H925 is provided with two non-tilting slides, similar to Grant type SS-168-NT. Considering possible servicing, the H925 should be mounted with enough height for using bottom access.

The H925 includes top and bottom cover plates along with an attractive bezel and front subpanel. The subpanel is made of sturdy 16-gauge metal for mounting front panel controls and accessories. The bezel is designed for installing a customer-supplied dress panel. The dress panel should have a thickness of $\frac{1}{8}$ ". The H925 fits all DEC 19" racks.

H925—\$250



H925



19" MOUNTING PANEL FRAME H941AA

HARDWARE

This rugged steel frame holds four 19" x 5 $\frac{1}{4}$ " mounting panels. A quick-release pin snaps out to allow the two-piece frame to swing open for easy access to the back panel wiring and connections. The construction of this frame allows sufficient rigidity for vertical or horizontal mounting. The Black Tweed finished aluminum cover affords mechanical protection for the circuitry as well as a neatly finished appearance for your digital logic system. The cover attaches to the frame with two thumb-release, positive-grip fasteners.

The H941 AA holds up to 32 H800, H803 and H808 Connector Blocks. It provides up to 256 module slots with H800 and H803 Connector Blocks and 128 slots with the H808's. The frame is designed to accept K943, H911, H914, 1943 Module Panels and H900, H910, H913, H916, H917 panels with power supplies. These panels attach to the pre-tapped frame with 10-32 x $\frac{1}{2}$ " machine screws.

Frame Height: 23"

Frame Width: 24"

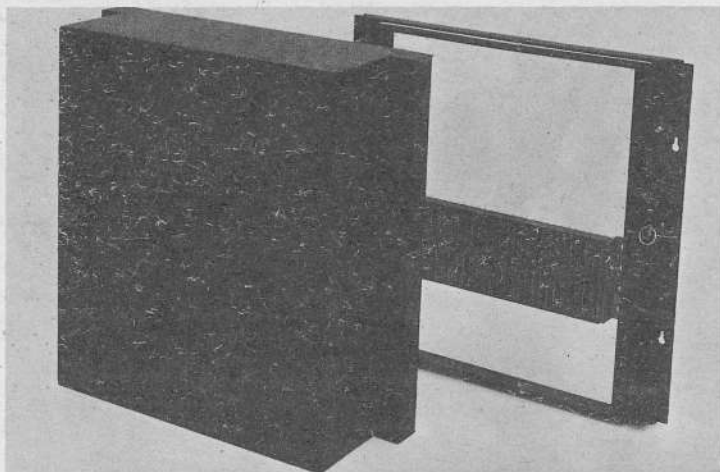
Overall Depth (Cover and Frame): 8"

Frame Mounting Hole Centers: 12 x 22 $\frac{1}{2}$ "

Frame Mounting Bolt: $\frac{1}{4}$ " dia.

Weight (Cover and Frame): Approx. 25 lbs.

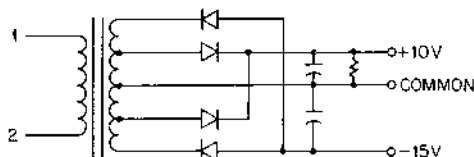
Cover Material: .093" Sheet Aluminum



H941 BA, H941 AA
Includes Cover and
Two Piece Frame
\$175.00

POWER SUPPLIES
H701, H701A, 782, 782A
+ 10, - 15 VOLTS

POWER SUPPLY



The 782 and 782A power supplies are ruggedly built, low cost units that fit into a standard 19-inch rack. The H701 and H701A are identical to these units, except they can be mounted on a chassis or panel in applications where space is added to an existing device. The basic supply can be mounted in various configurations and is identical to the power supplies used in models 700D and H900. The Types 782A and H701A are Power Supplies with 50 Hertz transformers. The Types 782 and 701 are 60 Hertz.

ELECTRICAL CHARACTERISTICS

Input Voltage: H701: 115 V 60 cps. H701A: 112.5, 123.5, 195, 220, 235 V, 50 cps. See "50 cps power"

Output Voltage: +10V, -15 vdc, floating

Output Current: -15V: 1/2 to 3 amp; +10V: 0 to 0.4 amp.

Line and Load Regulation: The output voltage remains between -14.5 and -16.5 V for the -15 output, and within +9.2 and +11.5 V for the +10 output, when load varies from minimum to maximum and line voltage varies $\pm 10\%$.

P-P Ripple: Less than 0.6 V for +10 output. Less than 0.6 V for -15 output; 20% more ripple on the 50-cps type.

Line Frequency Tolerance: $\pm 2\%$ of line frequency.

MECHANICAL CHARACTERISTICS

Height: 5-3/4"

Width: 4-15/16"

Length: 8"

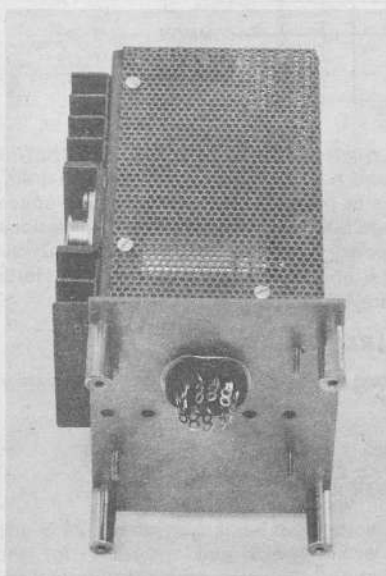
Finish: Chromicoat

Power Connections: Screw terminals are provided on transformer for input power connections. Output power connections are made via tab terminals which fit the AMP "Faston" receptacle series 250, part #41774 or Type 914 power jumpers. All required mounting hardware is supplied with this unit.

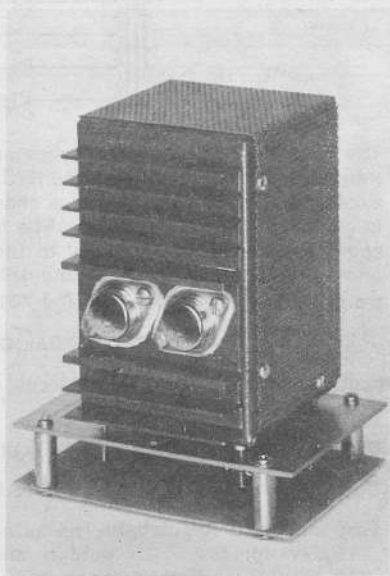
H701	— \$116.00	782	— \$128.00
H701A	— \$136.00	782A	— \$148.00

DUAL POWER SUPPLY
H704, H707
15 Volts

POWER
SUPPLY



H704



H707

These supplies differ only in dimensions and output current capabilities: 400 mA and 1.5 Amperes respectively for the H704 and H707. May be mounted on the bars in an H920 drawer, taking the space of two connector blocks.

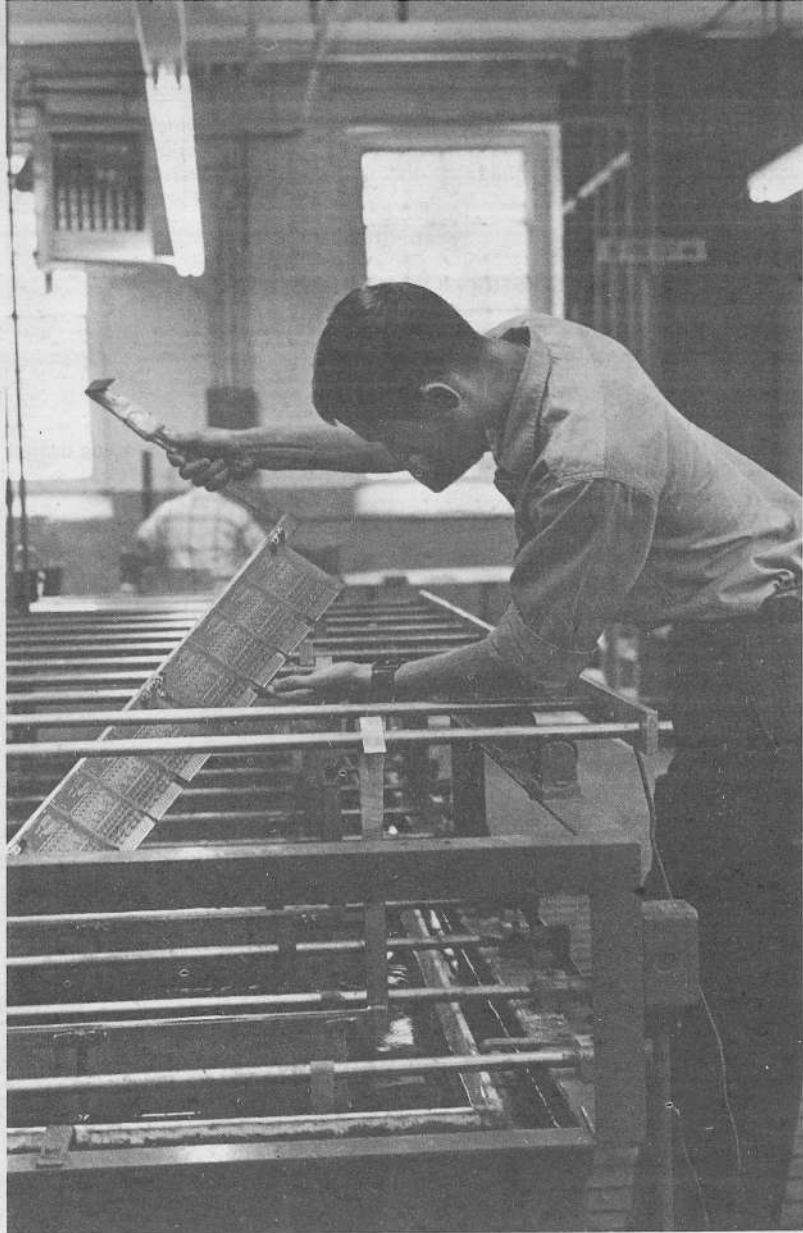
MECHANICAL CHARACTERISTICS

DIMENSIONS: $3\frac{1}{4} \times 3\frac{3}{8} \times 5$ in. height (H704)

DIMENSIONS: $4 \times 5 \times 5\frac{1}{2}$ in. height (H707)

CONNECTIONS: All input-output wires must be soldered to octal socket at the base of the power supply.

OPERATING TEMPERATURE: -20 to $+71^{\circ}\text{C}$ ambient



Checking the appearance of board contacts being gold-plated. Our 100 micro-inch plating is verified by periodic checking on a radiation gauge.

**POWER SUPPLY
H716**

**POWER
SUPPLY**

Type H716 provides +5 Volts at 4 amperes and -15 Volts at 1.5 amperes with over voltage protection for +5 Volts. This dual voltage power supply is designed to be mounted at the right end of any mounting panel. The supply is mounted by using the four holes in the Type H020. The supply takes 2 connector blocks of Type H800, H803, or H808. This provides 48 module slots with Types H800 and H803, 24 slots with Types H800 and H803 and 24 slots when Type 808 is used.

MECHANICAL CHARACTERISTICS

Maximum Dimensions $5\frac{1}{4} \times 4\frac{1}{8} \times 12$ deep

Power input via Amphenol 160-5 or equivalent connector with an Amphenol 160-5 or equivalent, in parallel.

Low voltage connections are by slip on terminals.

ELECTRICAL SPECIFICATIONS

Input: 120/240 vac $\pm 10\%$, 47-63 Hz. Normally supplied wired for 120V. For 240 Volts change transformer tap connections.

Output 1: +5V, adjustable from 4.5 to 5.5 Volts at 4 amperes maximum. Line-Load-Ripple total regulation $\pm 3\%$.

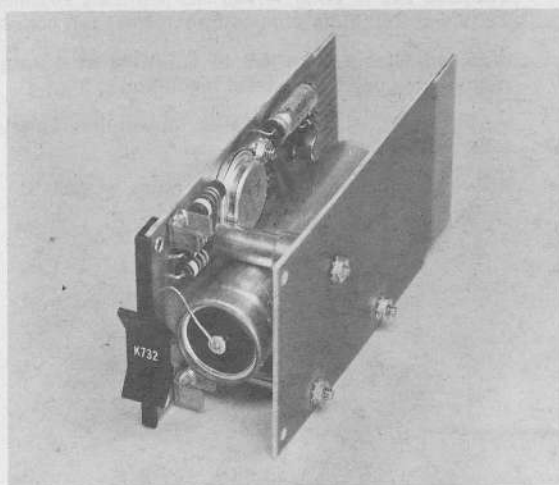
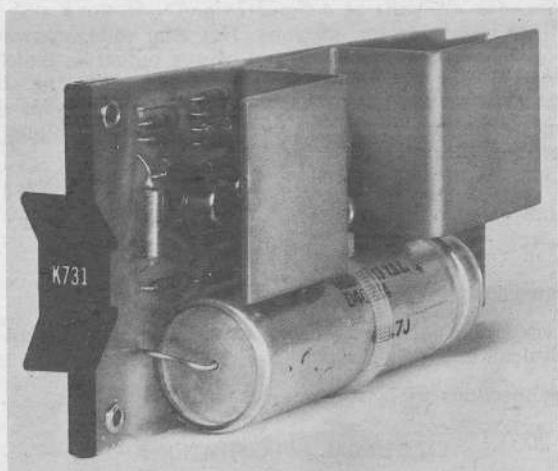
Output 2: -15V $\pm 5\%$ at 1.5 amperes, maximum. Line-Load-Ripple total regulation $\pm 5\%$.

Temp. Range: Above specifications are over a range of 0-50°C.

H716 — \$150

**POWER SOURCE MODULE K731
SLAVE REGULATOR K732**

**POWER
SUPPLY**

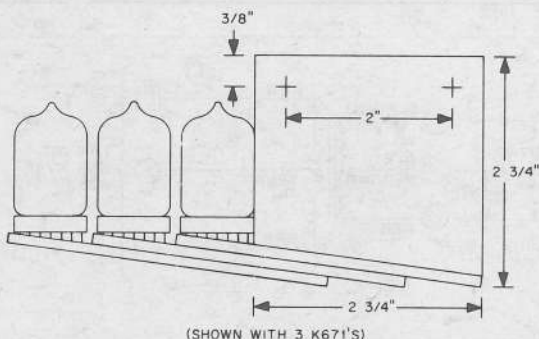


One K731 plus up to 3 K732 can provide from 1 to 7 amperes at +5V.
Consult K Series text for additional characteristics and hook up information.

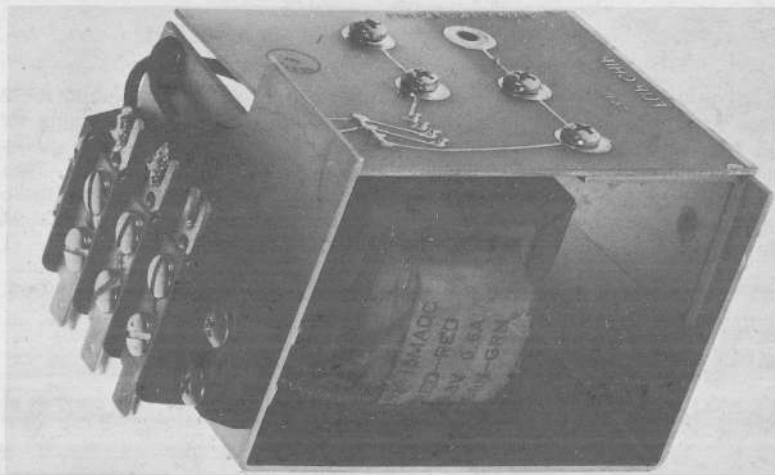
K731 — \$30
K732 — \$27

DISPLAY SUPPLY K771

POWER SUPPLY



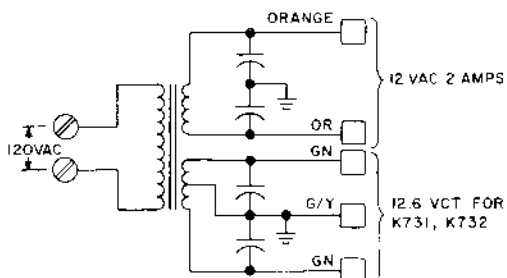
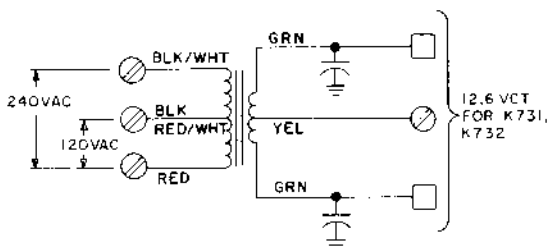
Shown above from the viewing side, the K771 supplies power and a convenient two-screw mounting for up to 6 K671 display tubes. Display tubes are stacked to the left, the first tube board being attached to the K771. The second tube board attaches to the first, and so on. Board mounting screws provide both mechanical mounting and electrical power connections. The two panel mounting screw locations dimensioned above have No. 6 steel threaded inserts. Several 1" holes using a standard chassis punch may be cut on 0.8" centers for viewing display tubes. To seal opening against dust, a 3" by 3-6" piece of Lucite® or Plexiglas® may be assembled between display and mounting surface. Power 120 VAC enters the supply from a terminal strip at the rear. Total depth behind mounting surface: 4".



K771 — \$35

POWER TRANSFORMERS K741, K743

POWER SUPPLY

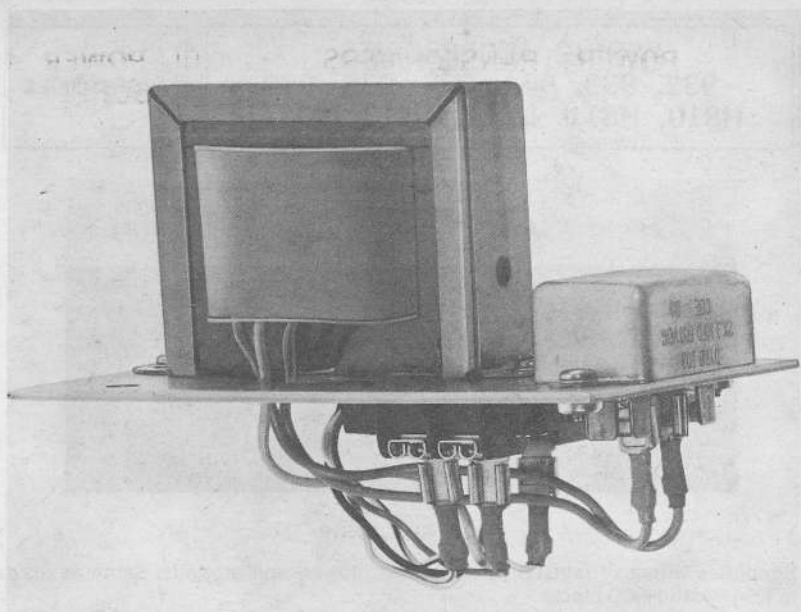


These hash-filtered, 50/60 Hz transformers supply K731 Source and K732 Slave Regulator modules. The K743 also provides an auxiliary winding for use with K580 Dry Contact Filters, K681 or K683 Lamp Drivers (requires additional bridge rectifier, and the K730 Supply and Control Module. Type 914 Power Jumpers are convenient for connecting to tab terminals on these transformers and on the K732 and K943. Both transformers have holes at the corners of the chassis plate for mounting on K980 endplates:

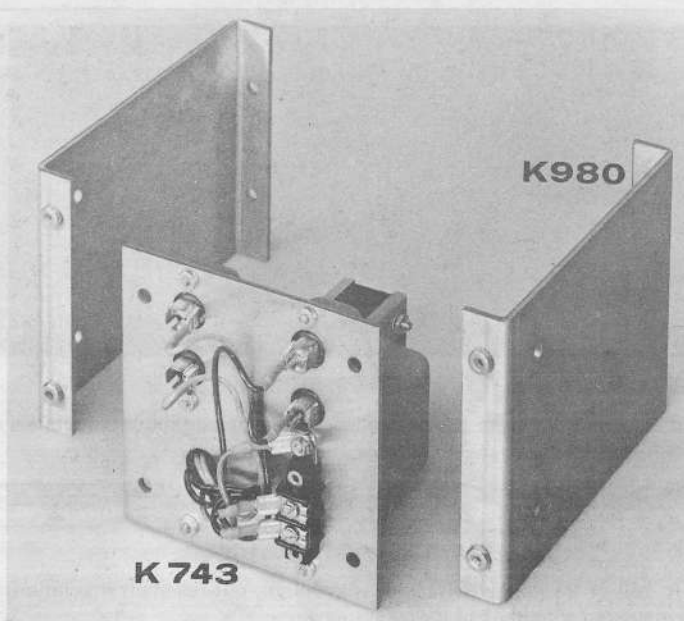
	PLATE DIMENSIONS	HOLE CENTERS	MATCHING K980 Ctrs.
K741	3½" x 5"	2½" x 3¾"	2½"
K743	5" x 5"	4" x 3¾"	4"

The K741 is sufficiently light in weight to be mounted on one side only, as at the end of a K943 mounting panel.

K741 — \$30
K743 — \$45



K741



K743

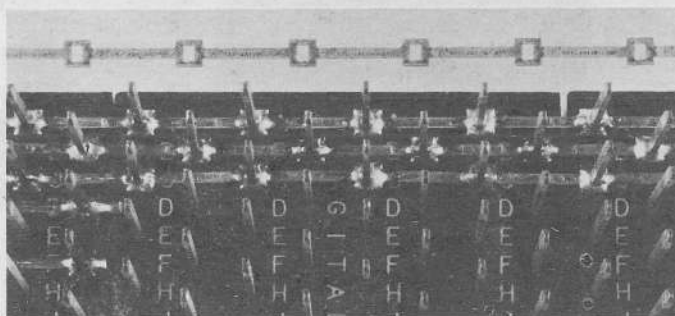
K980

K743

WIRING ACCESSORIES

932, 933, 934, 935, 936, 939
H810, H811, H812, H813, H814

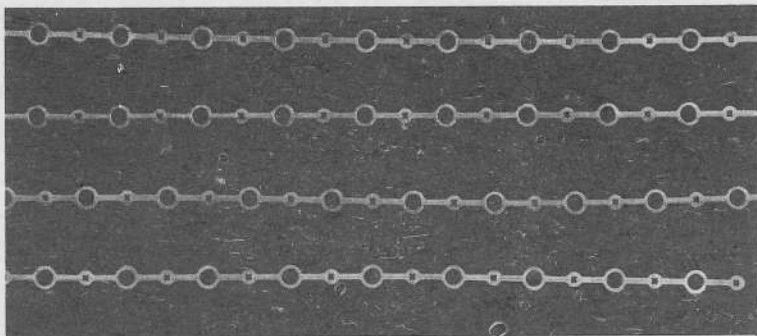
ACCESSORIES



932 BUS STRIP

Simplifies wiring of register pulse busses, power, and grounds. Same as used in K943 with H800 blocks.

932 — \$0.60



933 BUS STRIP

Simplifies wiring of power, ground and signal busses on mounting panels using H803 connectors.

933 — \$1

934 WIRE-WRAPPING WIRE

1000 ft. roll of 24 gauge solid wire with tough, cut-resistant insulation. (Use Teflon insulated wire instead for soldering.)
For use with H800 connectors.

934 — \$50

935 WIRE-WRAPPING WIRE

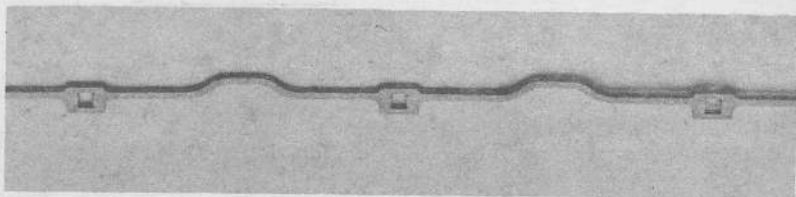
1000 foot roll or 30 gauge insulated solid wire for use with H803 connectors.

935 — \$60

936 19 CONDUCTOR RIBBON CABLE

Use on W Series connector modules or split into 9-conductor cables for use with K580, K681, K683, etc.

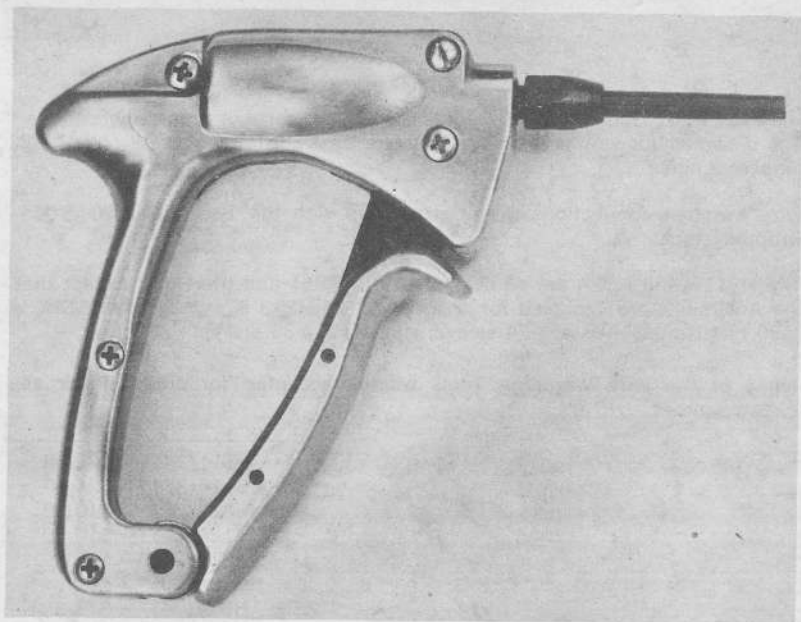
936 — \$0.60



939 BUS STRIP

For use with H808 connectors.

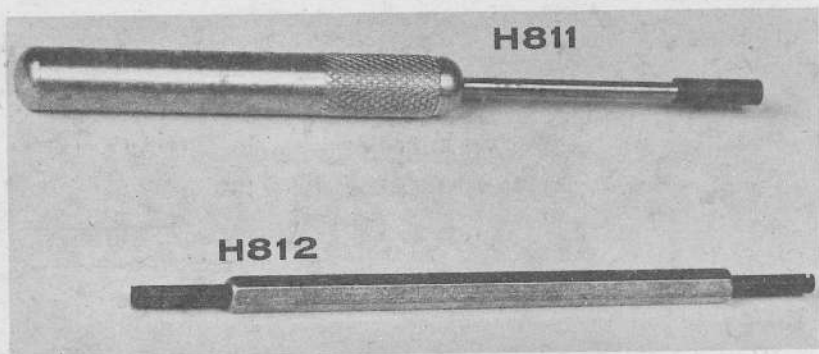
939 — \$1



H810 PISTOL GRIP HAND WIRE WRAPPING TOOL

The type H810 Wire Wrapping Tool is designed for wrapping #24 or #30 solid wire on Digital-type connector pins. The H810 Kit includes the proper sleeves and bits. It is recommended that five turns of bare wire be wrapped on these pins. This tool may also be purchased from Gardner-Denver Co. (Gardner-Denver part No. 14H-1C) with No. 26263 bit and No. 18840 sleeve for wrapping #24 wire. Specify bit #504221 and sleeve #500350 for wrapping #30 wire. When ordering from Digital specify the sleeve and bit size desired for #24 and #30 wire.

H810(24) —	\$ 99
30 ga. H810A —	\$ 99
30 and 24 ga. H810B —	\$150



The Type H811 Hand Wrapping tool is useful for service or repair applications. It is designed for wrapping #24 solid wire on DEC Type H800-W and H808 connector pins.

Wire wrapped connections may be removed with the Type H812 Hand Unwrapping tool.

The H811A and H12A are equivalent to the H811 and the H812 except that the A versions are designed for #30 wire. The H813 is a #24 bit; H813A, a #30 bit. The H814 is a #24 sleeve; H814A, a #30 sleeve.

None of the Wire Wrapping Tools will be accepted for credit under any circumstances.

H811(24) —	\$21.50
H811A(30) —	\$24.50
H812(24) —	\$10.50
H812A(30) —	\$10.50
H813(24) —	\$30
H813A(30) —	\$30
H814(24) —	\$21
H814A(30) —	\$21

WIRING ACCESSORIES
913, 914, 915, 917
H820, H821, H825, H826

ACCESSORIES

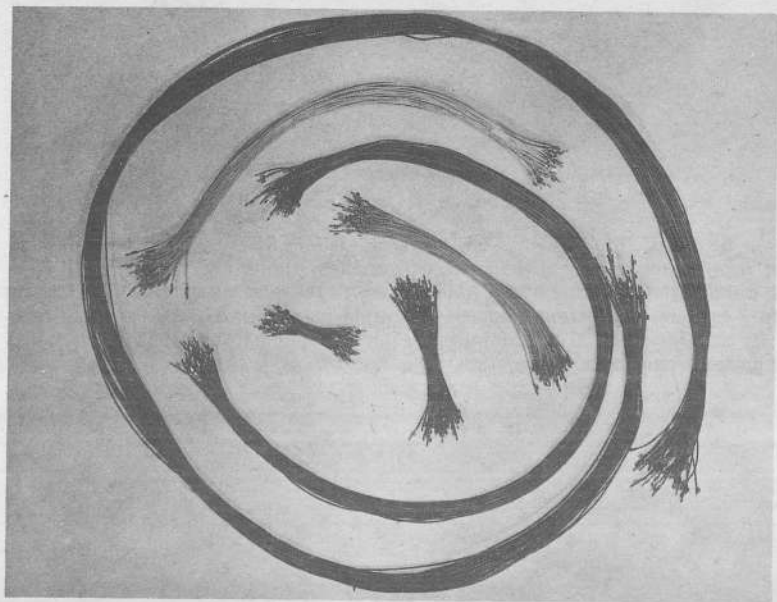
913 AND 915 PATCHCORDS

These patchcords provide slip-on connections for FLIP CHIP mounting panels and are available in color-coded lengths of 2, 3, 4, 6, 8, 12, 16, 24, 32, 48, and 64 inches. All cords are shipped in quantities of 100 in handy polystyrene boxes. Type 913 patchcords are for 24 gauge wirewrap and use AMP Terminal Type #60530-1. Type 915 patchcords are for 30 gauge wirewrap and use AMP Terminal Type #85952-3.

PATCHCORD COLOR-CODE			
Size	Color	Size	Color
2"	brown	16"	yellow
3"	black/white	24"	yellow/white
4"	red	32"	green
6"	red/white	48"	green/white
8"	orange	64"	blue
12"	orange/white		

H820 AND H821 GRIP CLIPS FOR SLIP-ON PATCHCORDS

The type H820 and H821 GRIP CLIPS are identical to slip-on connectors used in respectively the 913 and 915 patchcords. These connectors are shipped in packages of 1000 and permit fabrication of patchcords to any desired length. H820 GRIP CLIPS will take size 24-20 awg. wire. H821 GRIP CLIPS will take size 30-24 awg. wire.

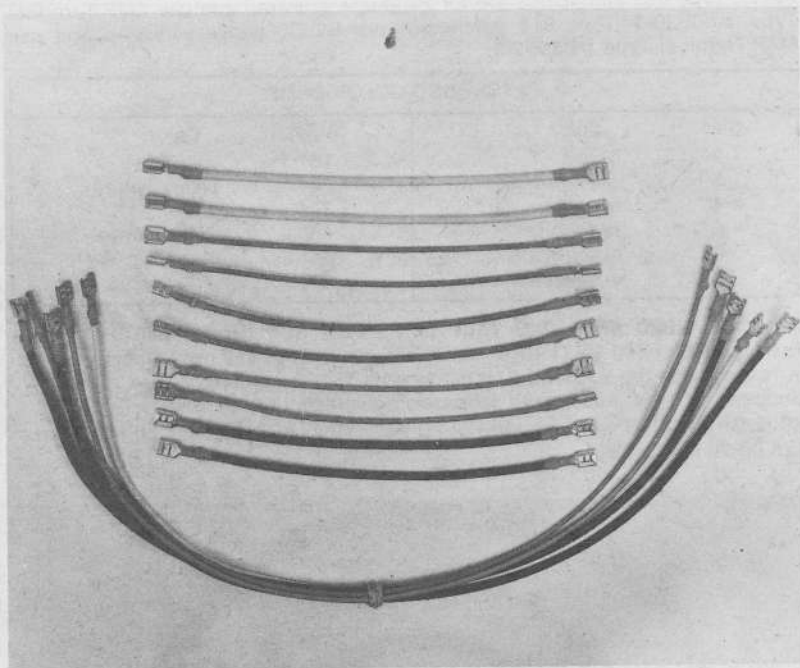


H825 HAND CRIMPING TOOL

Type H825 hand crimping tool may be used to crimp the type H820 GRIP CLIP connectors. Use of this tool insures a good electrical connection. This tool may also be obtained from AMP, Inc. as AMP part #90084.

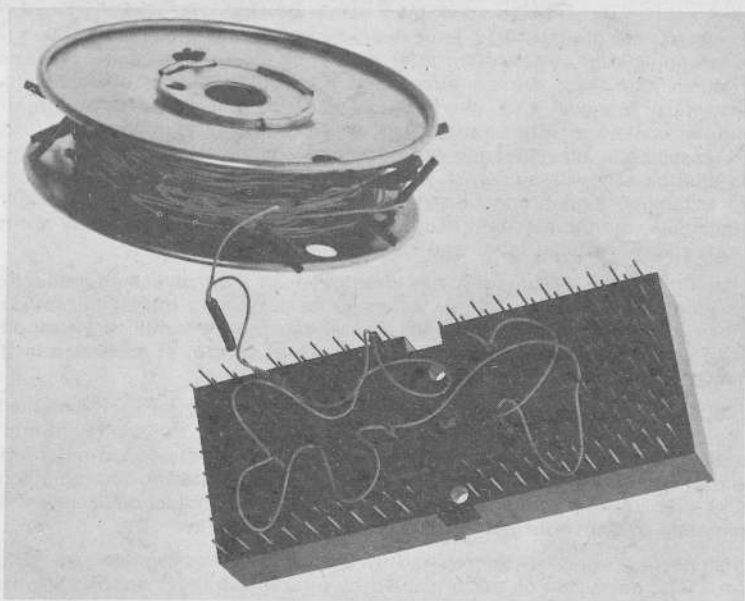
H826 HAND CRIMPING TOOL

Type H826 hand crimping tool may be used to crimp the type H821 GRIP CLIP connectors.



914 POWER JUMPERS

For interconnections between power supplies, mounting panels, and logic lab panels, these jumpers use AMP "Faston" receptacles series 250. Specify 914-7 for interconnecting adjacent mounting panels, or 914-19 for other runs of up to 19 inches. 914-7 contains 10 jumpers per package; 914-19 contains 10 jumpers per package.



917 DAISY CHAIN

Type 917 is a continuous length of unbroken #25 AWG stranded wire. 250 gold plated and insulated terminals are crimped at predetermined intervals on each reel. In conjunction with type H803 or type H807 connector blocks and M Series modules, hand patch wiring of prototype systems is easily and quickly accomplished. All that is required is a reel of type 917 Daisy Chain and wire cutters. These dependable push on connections are also easily removeable making this wiring technique ideal in cases where wiring and unwiring for changing systems needs is required. If ever a third lead is necessary a type 915 patchcord can be used if placed on the pin before the Type 917 termination. Two contact spacings available at 2½" or 5".

917 — 2.5 — blue
917 — 5 — white

Also available from:
Berg Electronics
New Cumberland, Pa. 17070
Tel. (717) 938-6711

913	— \$ 18	pkg. of 100
914-7	— \$ 4	pkg. of 10
914-19	— \$ 4	pkg. of 10
915	— \$ 33	pkg. of 100
H820	— \$ 48	pkg. of 1000
H821	— \$ 75	pkg. of 1000
H825	— \$146	
H826	— \$210	

WIRE WRAPPING SERVICE

The electronics industry has long been aware of the many advantages of wire wrapping over soldering for interconnecting electronic circuits. Soldering introduces numerous human errors and presents problems of cold solder joints, flux removal and overheating sensitive components. Automatic, computer-controlled wire wrapping, however, not only eliminates the problems associated with soldering but adds many technical and economic benefits unattainable with soldering. Automatic wire wrapping provides extremely high reliability, high production rates, elimination of human error, long-life connections, simple mechanical inspection techniques, high density wiring, rework ability, reduced labor and reduced inspecting time.

Digital Equipment Corporation has developed an extensive high-production wire wrapping capability and now offers to its customers the significant cost savings of automatic wire wrapping. Digital can provide a full wire wrapping service and our "Smooth-Flo" processing insures control at each step in the process.

Digital automatically verifies the correctness of the wiring on each panel with its computer-controlled Automatic Wire Test equipment. This verification is a standard part of Digital's wire wrapping service and is provided at no charge. The only restriction is that the size of the panel be limited to four connector blocks high by ten connector blocks wide. No price reduction is given for elimination of the verification service.

Digital needs a wire listing prepared by the customer on Digital Form DR22. Form DR22 must also be accompanied by a purchase order specifying which mounting panels are being purchased. In addition, if any special bussing is needed, a copy of the updated bussing diagram must also accompany the purchase order. It is extremely important that a complete wire listing, either punched cards or Form DR22, and complete bussing information be received with each order. Pricing of a wire wrapping order cannot be completed until the source deck has been processed and buss print received. These are needed to determine wire count and number of points to be bussed.

Special Services

The customer will receive one copy each of the Name Sort and Pin Sort lists at no charge.

Digital will perform special bussing where required. The rate for this \$0.20 (including the cost of the buss strip) per point.

Delivery

The normal delivery time for wire wrapped panels is two to five weeks after receipt of the purchase order, accurate source inputs (card or wire list), and updated bussing diagram if special bussing is required.

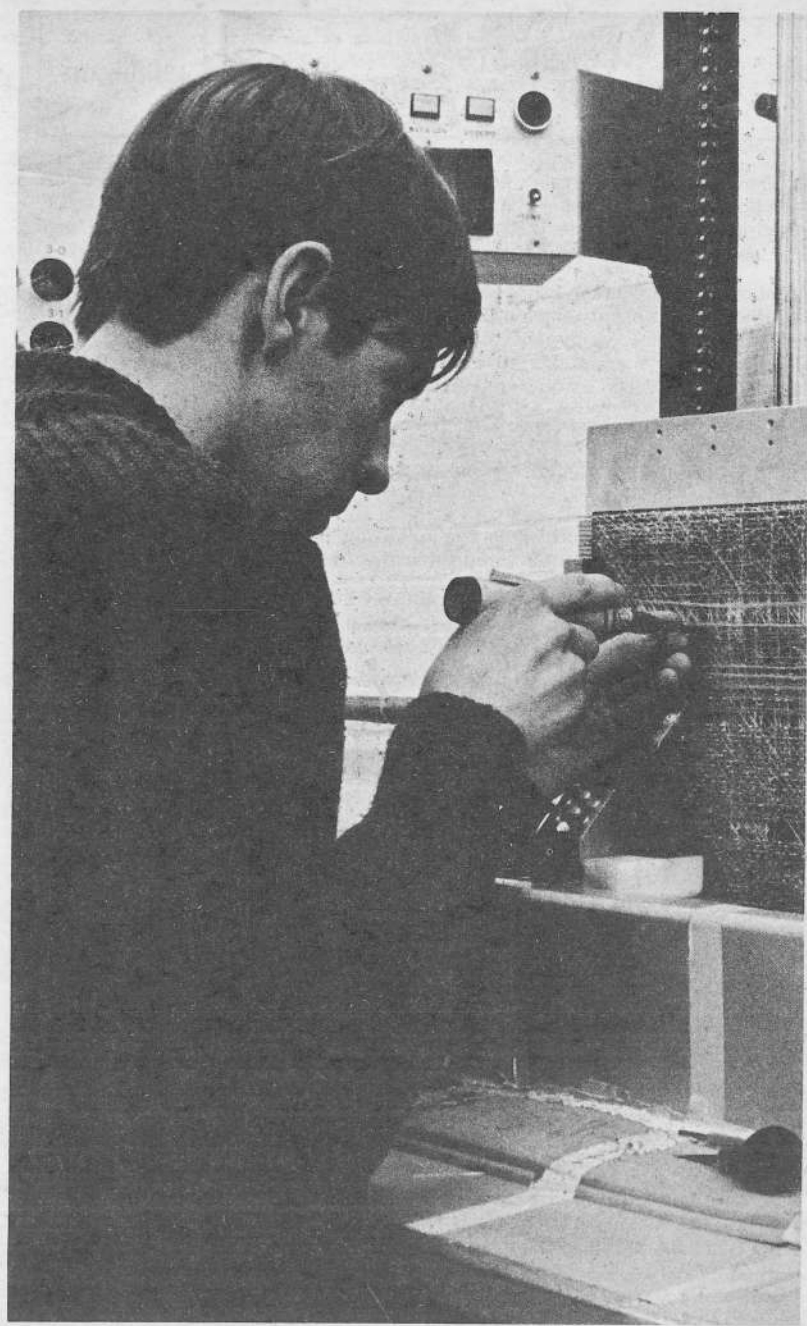
On repeat orders for the same panels and wiring configuration, normal delivery time is often reduced to almost half that of initial processing time.

Pricing

*30 ga. Set-up Charge	\$125.00
*24 ga. Set-up Charge	\$175.00
30 ga. Wire/Cost per Wire30
24 ga. Wire/Cost per Wire25

.20 per point for special bussing, including buss strip.

*One time charges are not discountable.



CABINETS H950 AND H954 SERIES

HARDWARE

The Control Products Group offers standard 19" mounting cabinet frame assemblies in two series—H950-AA (68 25/32" high x 25" deep x 63" mounting space), and the H954-AC cabinet frame assembly (49 8/16" high x 25" deep x 42 1/16" mounting space).

The above-listed cabinet frame assemblies offer complete flexibility and expandability to present and future DEC customers, single users, multiple users and original equipment manufacturers. The enclosure area in these cabinet frames is adaptable to customer-designed hardware, logic module racks, power supplies, computer systems, and peripherals.

The cabinet frame assemblies are constructed of rugged 12- and 13-gauge steel. The frame uprights have 9/32" holes drilled at standard EIA spacing (5/8-5/8-1/2) the full length of the 42" and 63" front and rear mounting panel heights.

Note: The cabinets described in the following pages, Cabinet A through H, do not include in their listed price the front cabinet mounting options.

Cabinet customers have the option of selecting the type of front cabinet hardware mounting of their choice. Consult the H950 and H954 parts list for prices and add to basic cabinet price listed.

Cabinet A (H960-A)

- 1—H950-AA 19" Mounting Frame (71 7/16" w/casters x 25" x 63"), includes mounting hardware
- 1—7406782 Kickplate (Lower Cab Trim)
- *1 pr. H952-BA Stabilizer Feet
- 1—H952-FA Leveler Set (4)
- *1—H950-LA Logo Frame Panel
- 2—H952-AA End Panels
- 1—H950-BA Full Door Rear (Right Hanging)
- 1—H952-EA Caster Set (4)
- 1—H952-CA Fan Assembly

Cabinet A—List Price—\$378.50

OPTION: Front Cabinet Mounting/Cover Panels—
H950-P (5 1/4") and/or H950-Q (10 1/2")

- * H950-SA Filter (for fan) Assembly
- * See Special Considerations Sections 5, 8 and 13.

Cabinet B (H960-B)

- 1—H950-AA 19" Mounting Frame (71 7/16" w/casters x 25" x 63") includes mounting hardware
- 1—7406782 Kickplate (Lower Cab Trim)
- *1 pr. H952-BA Stabilizer Feet
- 1—H952-CA Fan Assembly
- 1—H952-EA Caster Set (4)
- 1—H952-FA Leveler Set (4)

- *1—H950-LA Logo Frame Panel
- 2—H952-AA End Panels
- 1—H950-DA Mounting Panel Rear Door (Right Hanging)
- 1—H950-FA Mounting Panel Door Skin

Cabinet B—List Price—\$392.50

OPTION: Cabinet Front Mounting/Cover Panels—
H950-Q (10 1/2") and/or H950-P (5 1/4")

- * H950-SA Filter (for fan assembly)
- * See Special Considerations, Sections 5, 8, and 13.

Cabinet C

- 1—H950-AA 19" Mounting Frame (71 7/16" w/casters x 25" x 63") includes mounting hardware
- 1—7406793 Kickplate (Lower Cab Trim)
- *1—H950-LA Logo Frame Panel
- 1—H952-CA Fan Assembly
- 1—H952-EA Caster Set (4)
- 1—H952-FA Leveler Set (4)
- 2—H952-AA End Panels
- 1—H950-DA Mounting Panel Door (Right Hanging)
- 1—H950-BA Full Door Rear (Right Hanging)

Cabinet C—List Price—\$397.00

OPTION: Front Cabinet Mounting/Cover Panels—
H950-P (5 1/4") and/or H950-Q (10 1/2")
Short Doors—See H950 Cabinet Parts List—
H950-HA—HK—short door selection.

- * H950-SA Filter (for fan assembly)
- * See Special Considerations, Sections 5, 8, and 13.

Cabinet D

- 1—H950-AA 19" Mounting Frame (71 7/16" w/casters x 25" x 63") includes cover filter and mounting hardware
- 1—7406793 Kickplate (Lower Cab Trim)
- 1—H952-CA Fan Assembly
- *1—H950-LA Logo Frame Panel
- 1—H952-EA Caster Set (4)
- 1—H952-FA Leveler Set (4)
- 2—H952-AA End Panels
- 1—H950-BA Full Door Rear (Right Hanging)

Cabinet D—List Price—\$358.00

OPTION: Front Cabinet Mounting—Cover Panels—
H950-P (5 1/4") and/or H950-Q (10 1/2")
Short Doors—See H950 Parts List—
H950-HA—HK—Short Door Selection.

- * H950-SA Filter (for fan assembly)
- * See Special Considerations, Sections 5, 8, and 13.

Cabinet E,

Same as Cabinet D, except:

- 1—H950-DA Mounting Panel Door Rear (Right Hanging) and
- 1—H950-FA Mounting Panel Door Skin,
are substituted for:
- 1—H950-BA Full Door Rear (Right Hanging)

Cabinet E—List Price—\$372.00

OPTIONS: Front Cabinet Mounting—
Same as listed for Cabinet D

Cabinet F (H961-A)

Add-on—Designed for combining two or more cabinets, in the H950 Series.
No end panels are required (H952-AA).

- 1—H950-AA 19" Mounting Frame (71 7/16" w/casters x 25" x 63"), includes mounting hardware
- 1—74-6793 Kickplate (Lower Cab Trim).
- 1—H950-FA Mounting Panel Door Skin
- 1—H950-EA Mounting Panel Door Plenum (Left Hanging)
- 1—H952-CA Fan Assembly
- 1—H952-EA Caster Set (4)
- 1—H952-FA Leveler Set (4)
- *1—H950-LA Logo Frame Panel
- 1—H952-GA Filler Strip (Front and Rear)

Cabinet F—List Price—\$316.00

OPTIONS: Front Cabinet Mounting
Same as used for Cabinet D.

* See Special Considerations Section 13, 2

Cabinet G—Short Cabinet Series

- 1—H954-AC 19" Mounting Frame (51 12/16" w/casters x 25" x 42 1/16") includes mounting hardware
- 1—H954-BA Full Door—Rear Mounting (Right Hanging)
- 1—H954-CA Fan Assembly
- 1—H950-LB Logo Frame Panel
- 1—H952-EA Caster Set (4)
- 1—H954-SA Filter (for fan assembly)
- 1—H952-FA Leveler Set (4)
- 1—H954-UA Cabinet Cover
- 2—H952-AM End Panels
- *1 pr. H952-BA Stabilizer Feet
- 1—74506782 Kickplate (for use with H952-BA)

Cabinet G—List Price—\$450.00

OPTION: Front Cabinet Mounting/Cover Panels
H950-P (5 1/4") and/or H950-Q (10 1/2")

* See Special Considerations, Section 5

Cabinet H

- 1—H954-AC 19" Mounting Frame (51 12/16" w/casters x 25" x 42 1/16") includes mounting hardware
- 1—7406793 Kickplate (Lower Cab Trim)
- 1—H954-BA Full Door Rear (Right Hanging)
- 1—H954-CA Fan Assembly
- 1—H950-LB Logo Frame Panel
- 1—H952-EA Caster Set (4)
- 1—H954-SA Filter (for fan assembly)
- 1—H952-FA Leveler Set (4)
- 1—H954-UA Cabinet Cover
- 2—H952-AM End Panels

Cabinet H—List Price—\$427.00

OPTION: Front Cabinet Mounting/Cover Panels

H950-P (5 1/4") and/or H950-Q (10 1/2")

Short Doors from H950-HA (21") through H950-HF (42") only.

Cabinet Specials

Non standard cabinet configurations are made to order by using the two basic cabinet frame assemblies—H950-AA (68 25/32" x 25" x 63") and H954-AC (49 8/16" x 25" x 42 1/16").

It is recommended that all cabinet specials have the following basic parts:

1. H950 Series Cabinet
 - A—H950-AA Frame (71 7/16" height w/casters x 25" x 63")
 - B—H952-EA Caster Set (4)
 - C—H952-FA Leveler Set (4)
2. H954 Series Cabinet
 - A—H954-AC Frame (51 12/16" height w/casters x 25" x 63")
 - B—H952-EA Caster Set (4)
 - C—H952-FA Leveler Set (4)
 - D—H954-UA Cabinet Cover

Consult H950 and H954 Cabinet Parts List to complete special cabinet configuration. **Cabinets are shipped assembled.**

Special Considerations

Before ordering a cabinet, the following should be considered:

1. If logo frame H950-LA or H950-LB is used, short doors and/or cover panels H950-P (5 1/4")—H950-Q (10 1/2") can be used for cabinet front mounting.
2. When ordering a cabinet to add to an existing system with a H950-AA frame assembly, or in joining two or more cabinets front and rear, filler strip H952-GA is used. (See Cabinet F.)
3. If power supplies with meters or switches are mounted to the rear mounting panel, (plenum) door H950-DA (RH) or H950-EA (LH), a full door H950-DA (RH) or H950-LA (LH) is needed. (See Cabinet C.)
4. The mounting panel door skin H950-FA bolts to the plenum door H950-DA (RH) or H950-EA (LH) and is used in place of a full door when hardware mounted to the plenum door (mounting panel door) does not require servicing. (See Cabinet B, E, and F.)

5. When using stabilizer feet H952-BA, the kickplate #7406782 (lower cabinet trim) is used. Special short doors can be used for cabinet front mounting. (See Cabinet A, B, and G.) For list of special short doors H950-JA through H950-JE for mounting with stabilizer feet, see H950 and H954 Parts List.
6. When using fan assembly, indicate direction of airflow (up or down).
7. When using short doors, make certain that the equipment for cabinet installation will not interfere with door height.
8. The filter H950-SA for use with H952-CA fan assembly should be ordered only for fans that are to be used for airflow intake.
9. Fan assembly specifications for H952-CA and H954-CA are 300 CFM.
10. H952-EA casters add 2 4/16" to cabinet frame assembly height.
H950-AA—Cabinet frame height w/casters—71 7/16".
H954-AC—Cabinet frame height w/casters—51 12/16".
11. Short doors H950-HA (21") through H950-HK (63") series—Dimensions of the doors listed in Parts List only cover mounting panel height; e.g., the H950-AA cabinet frame has 63" mounting panel height. Using a H950-HA (21") short door would leave 42" of mounting panel space.
12. Doors for rear mounting are listed as right hanging in Cabinets A, B, C, D, E. Left hanging doors may be substituted by changing suffix letters as listed in Parts List.
Key: (RH)—Right Hanging
(LH) Left Hanging
13. The H950-LA Logo Frame Panel is an aluminum extrusion that can be supplied with a blank adhesive inlay strip in assorted color combinations. "When the inlay strip is ordered as part of a cabinet, there is no charge for the inlay. Inlay strips ordered separately are priced at \$15.00 each." The adhesive inlay strip designed for PDP-8/E, PDP-11 require the H950-LB Logo Frame.
 1. Adhesive inlay color strip available for use with H950-LA frame panel
 - a. Brown/Yellow
 - b. Navy Blue/Bright Copen Blue
 - c. Bright Chartreuse/Lime Peel
 2. Adhesive inlay color strips available for use with H950-LB panel.
 - a. Terra Cotta/Amber
 - b. Magenta/Bright Rose

Ordering

Before ordering hardware for existing cabinets, make certain that they are compatible with the H950-AA cabinet frame assembly (overall height, 71 7/16" from floor, including casters); the H954-CA cabinet frame assembly (overall height, 51 12/16" including casters and cabinet cover). Module Marketing Services of Digital Equipment Corporation will assume responsibility only for parts ordered from the H950 and H954 Cabinet Parts List.

Assembly

Cabinet selections A through H, including cabinet specials, are shipped assembled.

Shipping

All shipments are FOB Maynard, Massachusetts. Specifications are subject to change without notice. Special packaging has been designed to ensure safe shipping.

Color

Basic color of cabinet hardware is black. Gray is used for end panels and the inlay of the cover panels.

Customized painting will be accepted with a minimum lot release of 10 cabinets at an extra charge of \$10 per cabinet painted. The customer must supply a color chip for color desired. DEC will not inventory custom painted cabinets without special consideration.

Order should be sent to Module Marketing Services. No cabinet hardware will be accepted for credit or exchange without the prior written approval of DEC, and without the proper return authorization number (RA#). **No cabinet returns are accepted on special paint orders.**

Prices do not include state or local taxes. Prices, discounts, and specifications are subject to change without notice.

Cabinet Discount Schedule

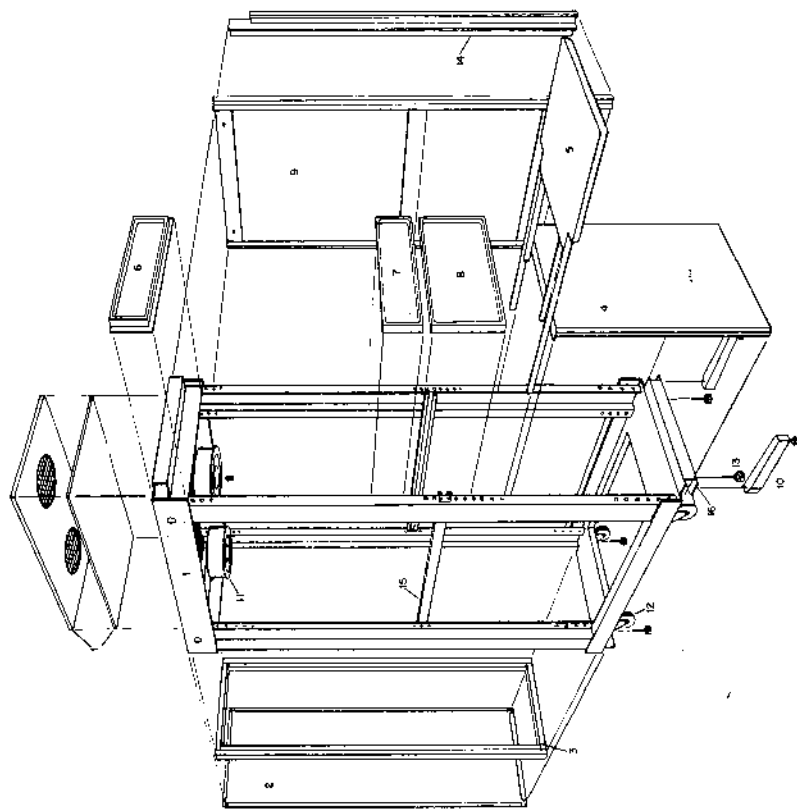
The following discount schedule is for cabinet purchases only. The discount is computed from the total list price of cabinet parts purchased. On blanket purchase orders, minimum releases of ten units (cabinets) or balance is required.

Sale in Dollars	Discount
\$ 500 - \$ 999	8%
1000 - 1499	12%
1500 - 2499	20%
2500 - 4999	25%
5000 - 7499	26%
7500 - 9999	28%
\$10,000 - And up	30%

PARTS AND PRICE LIST H950 — SERIES CABINET

Catalog No.	Description	List Price
H950-AA	Frame, 19" wide, 69" hi, 25" deep, 63" mounting panel, includes mounting hardware.	\$157.00
H950-BA	Full Door (RH), front and rear door mounting	42.00
H950-CA	Full Door (LH), front and rear door mounting	42.00
H950-DA	Mounting Panel (Plenum) Door, (RH) rear mounting ..	39.00
H950-EA	Mounting Panel (Plenum) Door, (LH) rear mounting ..	39.00
H950-FA	Mounting Panel Door Skin	17.00
H950-HA	Short Door (covers 21" mounting)	48.00
H950-HB	Short Door (covers 22 3/4" mounting)	48.00
H950-HC	Short Door (covers 26 1/4" mounting)	48.00
H950-HD	Short Door (covers 31 1/2" mounting)	48.00
H950-HE	Short Door (covers 36 3/4" mounting)	48.00
H950-HF	Short Door (covers 42" mounting)	48.00
H950-HG	Short Door (covers 47 1/4" mounting)	48.00
H950-HH	Short Door (covers 52 1/2" mounting)	48.00
H950-HJ	Short Door (covers 57 3/4" mounting)	48.00
H950-HK	Short Door (covers 63" mounting)	48.00
H950-JA	Special Short Door (17 1/2" mounting)	60.00
H950-JB	Special Short Door (22 3/4" mounting)	60.00
H950-JC	Special Short Door (28" mounting)	60.00
H950-JE	Special Short Door (62 3/4" mounting)	60.00
H950-G	Table Top Assembly (19" wide, 21 7/32" x 1 3/4")	50.00
H950-LA	Frame Panel Aluminum	6.00
H950-LB	Frame Panel Plastic	7.00
H950-P	5 1/4" Bezel Cover Panel	7.00
H950-Q	10 1/2" Bezel Cover Panel	11.00
H950-SA	Filter (for Fan Assembly)	4.00
*H952-AA	End Panel (require 2 per cabinet)	48.00
H952-BA	Stabilizer Feet (pair)	23.00
H952-CA	Fan Assembly (specify airflow), top mounted	40.00
H952-EA	Caster Set (4)	7.00
H952-FA	Leveler Set (4)	2.00
H952-GA	Filler Strip (front and rear), joining two cabinets	44.00
7406782	Kickplate (use with H952-BA)	5.00
7406793	Kickplate (Lower Cab Trim)	8.00

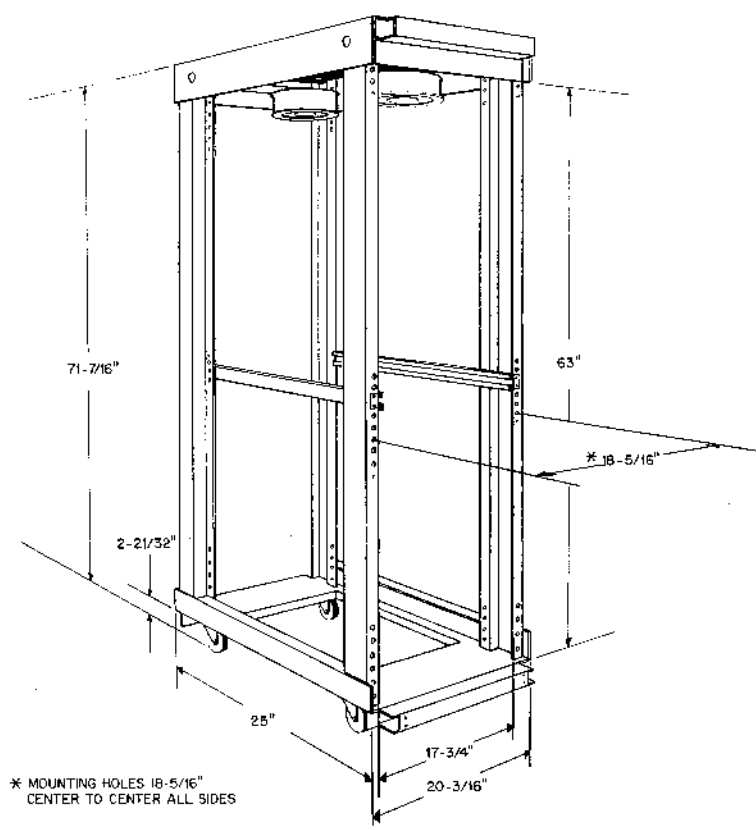
* Color of end panel is gray. Consult color section for customized painting.

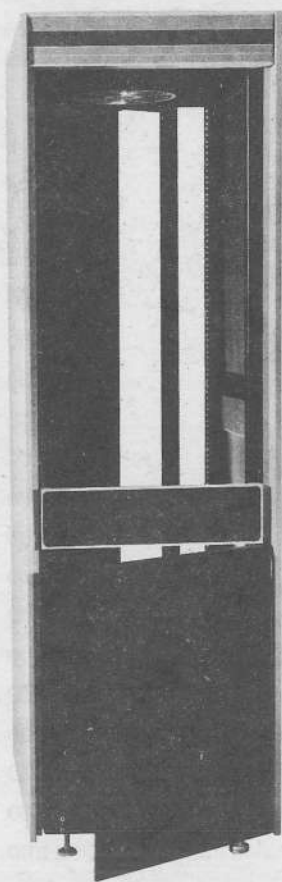


PART DESIGNATIONS

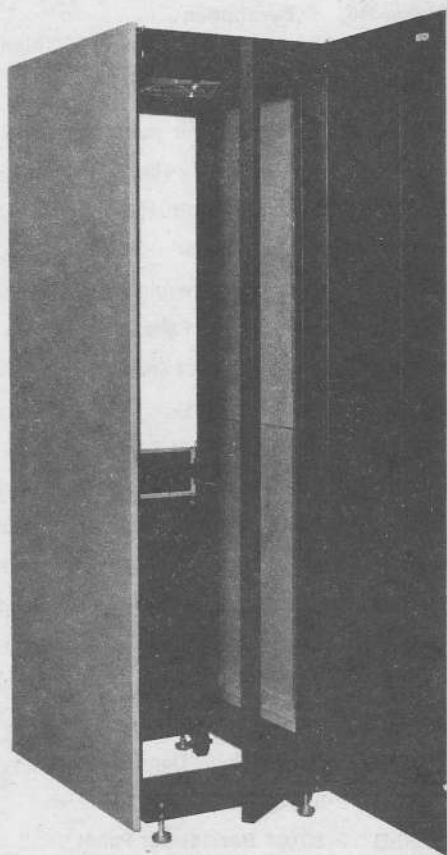
H950 SERIES CABINET

1. Frame
2. Full Door
3. Mounting Panel (Plenum) Door
4. Short Door
5. Table Top Assembly (19" wide,
21 $\frac{1}{2}$ " x 19 $\frac{1}{4}$ ")
6. Frame Panel
7. 5 $\frac{1}{4}$ " Bezel Cover Panel
8. 10 $\frac{1}{2}$ " Bezel Cover Panel
9. End Panel (require 2 per cabinet)
10. Stabilizer Feet (pair)
11. Fan Assembly (specific airflow),
top mounted
12. Caster Set
13. Leveler Set
14. Filler Strip (front & rear), joining
two cabinets
15. Slides
16. Kickplate





Front view of H950 frame.



Rear view of H950 frame.

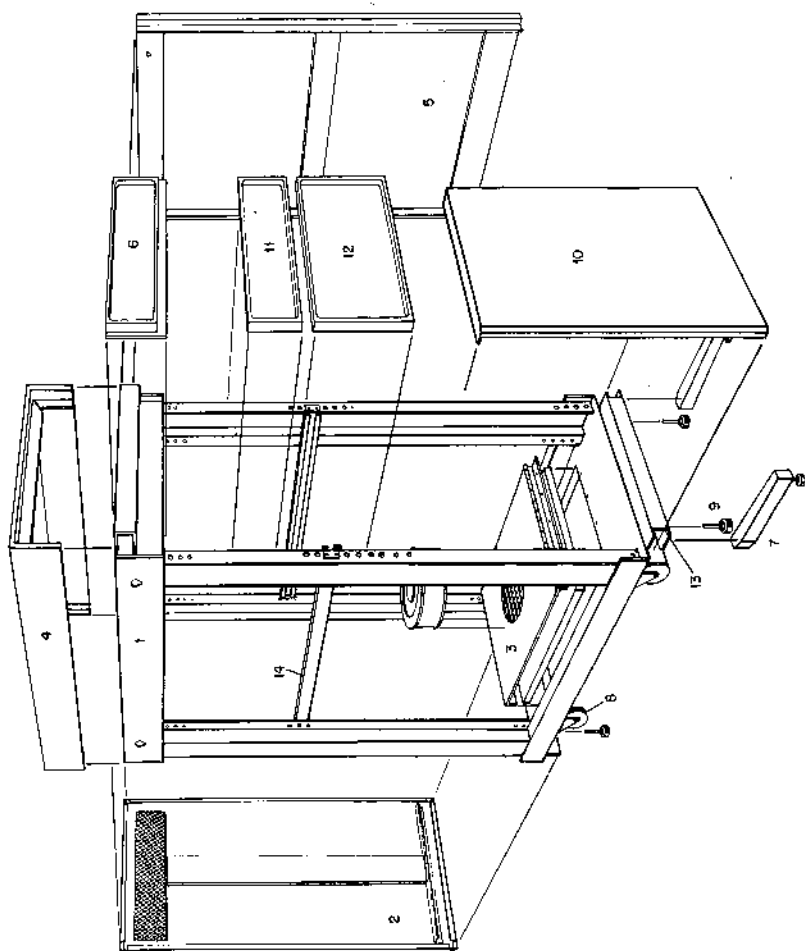
PARTS AND PRICE LIST

H954 — SERIES CABINET

Catalog No.	Description	List Price
H954-AC	Frame, 19" wide, 49 8/16" high, 25" deep, 42" mounting panel, includes mounting hardware	\$127.00
H954-BA	Full Door, rear mounting (RH)	65.00
H954-CA	Fan Assembly (bottom mounted)	73.00
H954-SA	Filter (use with H954-CA)	3.50
H954-UA	Cabinet Cover	47.00
*H952-AM	End Panel (require 2 per cabinet)	45.00
H950-LB	Logo Frame Panel	7.00
H952-BA	Stabilizer Feet (pair)	23.00
H952-EA	Caster Set (4)	7.00
H952-FA	Leveler Set (4)	2.00
H950-HA	Short Door (covers 21" mounting)	48.00
H950-HB	Short Door (covers 22 3/4" mounting)	48.00
H950-HC	Short Door (covers 26 1/4" mounting)	48.00
H950-HD	Short Door (covers 31 1/2" mounting)	48.00
H950-HE	Short Door (covers 36 3/4" mounting)	48.00
H950-HF	Short Door (covers 42" mounting)	48.00
H950-JA	Special Short Door (covers 17 1/2" mounting)	60.00
H950-JB	Special Short Door (covers 22 3/4" mounting)	60.00
H950-P	5 1/4" Bezel Cover Panel	7.00
H950-Q	10 1/2" Bezel Cover Panel	11.00
7406782	Kickplate (use with H952-BA)	5.00
7406793	Kickplate (Lower Cab Trim)	8.00

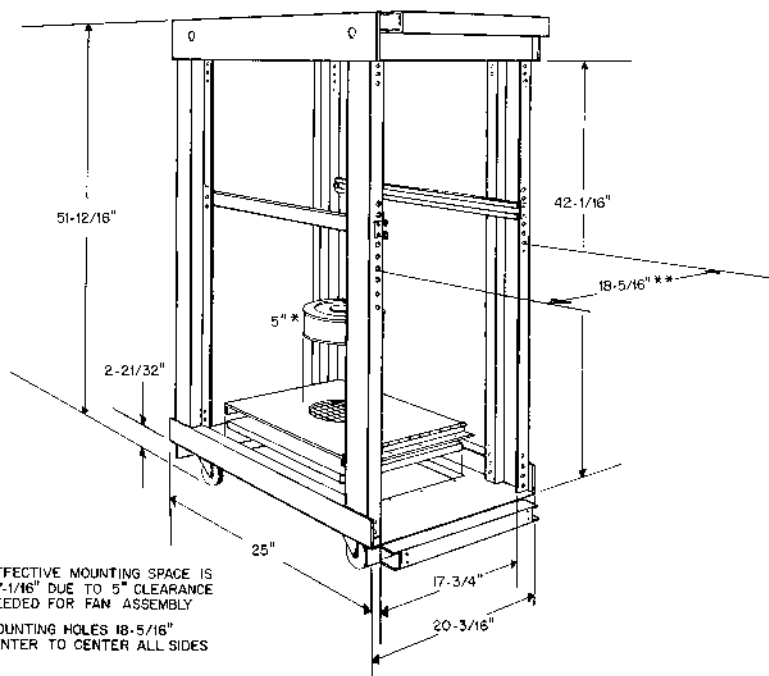
Prices and discounts shown are subject to change without notice.

* Color of end panel is gray. Consult color section for customized painting.



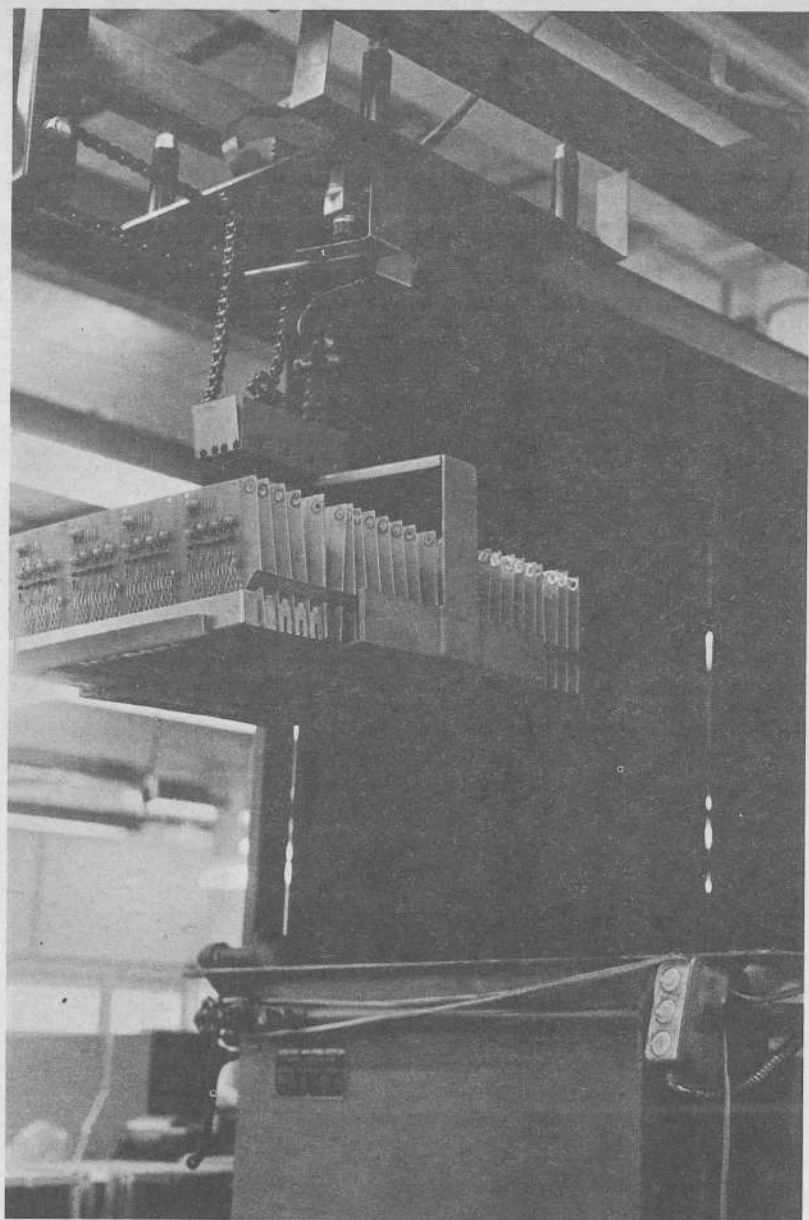
PART DESIGNATIONS
H954 SERIES CABINET

1. Frame
2. Full Door
3. Fan Assembly
4. Cabinet Cover
5. End Panel
6. Logo Frame Panel
7. Stabilizer Feet
8. Caster Set
9. Leveler Set
10. Short Door
11. 5/4" Bezel Cover Panel
12. 10 1/2" Bezel Cover Panel
13. Kickplate
14. Slides





Cabinets for DEC systems are manufactured in this portion of DEC's recently opened Westfield, Massachusetts production facility.



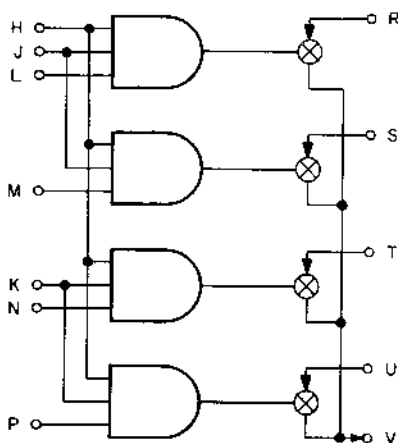
After all the components have been attached to the board, the module is degreased to remove contaminants in preparation for flow soldering.

A Series Analog Modules



POSITIVE LOGIC MULTIPLEXER A123

A SERIES



INPUT	OUTPUT TERMINALS
+3V	CONNECTED
0V	OPEN

The A123 Multiplexer provides 4 gated analog switches that are controlled by logic levels of 0V and +3V. The module is equivalent to a single-pole, 4-position switch, since one output terminal of each MOS FET switch is tied together. If all three digital inputs of a circuit are at +3V (or not connected) the two output terminals are connected together. If any digital input is at 0V, the switch terminals are disconnected. Two switches should not be on at the same time. The analog switch can handle signals between +10V and -10V, with currents up to 1 mA.

The positive power supply must be between +5V and +15V, and at least equal to or greater than the most positive excursion of the analog signal. The negative power supply must be between -5 and -20V, and at least 10 Volts more negative than the most negative excursion of the analog signal. The voltage difference between the two supplies must not be more than 30V.

SPECIFICATIONS

Digital Inputs

Logic ONE:	+2.4v to +5.0V
Logic ZERO:	0.0v to +0.8V
Input loading:	0.5mA. at 0Volts

Analog Signal

Voltage range:	+10v to -10v
Current (max.):	1 mA

Output Switch

On resistance, max.:	1000 ohms
On offset:	0 Volts
Off leakage, capacitance:	10 nA, 10 pF
Turn on delay, max.:	0.2 μ sec
Turn off delay, max.:	0.5 μ sec

Power

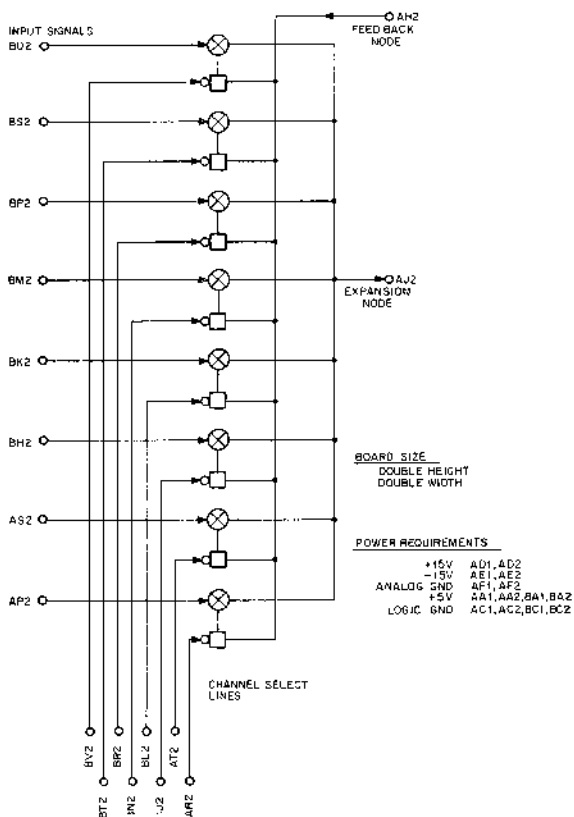
+5v (pin A):	45 mA
+10V (pin D):	18 mA
-20V (pin E):	50 mA

Size: Standard, single height, single width FLIP CHIP module.

A123—\$58

HIGH IMPEDANCE MULTIPLEXER EXPANDER A160

A SERIES



The A160 is a high impedance multiplexer expander consisting of 8 independent FET channels.

This unit may be used with any of the DEC high impedance multiplexers to perform single or double level multiplexing. It also may be used to expand the channel capabilities of the A152, A163, and A164, Multiplexer.

The A160 is DTL and TTL compatible and may be used with DEC's standard K and M Series logic modules. Each channel has its own channel selector driver and may be controlled from an external source such as a shift register, clock, or gating function.

A160—\$250

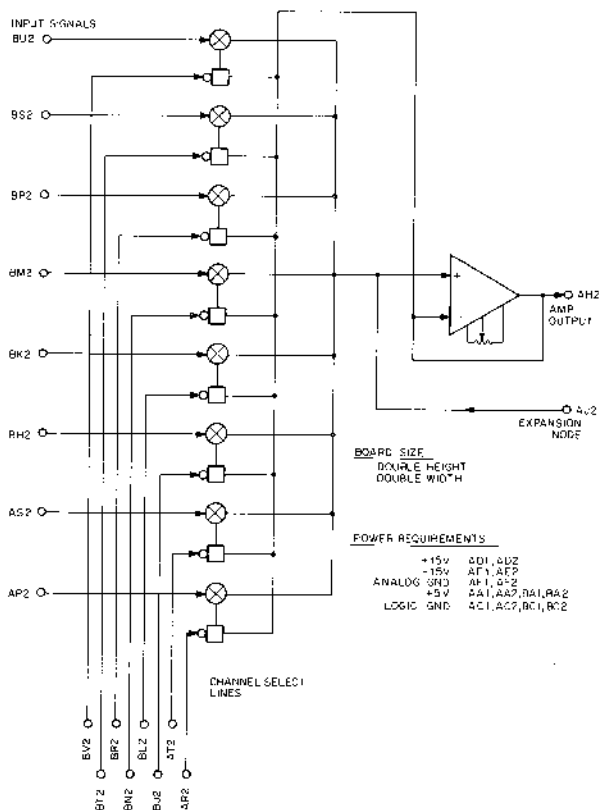
Advanced shielding techniques and optimized circuit layout have been employed in the A160, ensuring stable operation under normal ambient electrostatic and electromagnetic conditions, as well as allowing minimal cross-talk between channels.

SPECIFICATIONS

Analog Inputs:	8 single ended
Input Voltage Range:	$\pm 10V$. Maximum full scale
Expander Node:	Common point of 8 channels brought out to a common pin for input to external buffer amplifier
Feedback Input:	Feedback control point of multiplexer switches connected to output of buffer amplifier
Input Leakage:	0.5 nano Ampere max., per channel
Input Feedthrough Capacity:	4 pF per channel
OFF Channel Capacity:	7 pF per channel, shunt capacity at common node
ON Resistance of Channel (Without Buffer):	1000 ohms
Max. Input Voltage	$\pm 15V$.
Switching plus Settling Time:	5 μ sec., max., to settle to within .01% of full value for full scale excursion with zero source impedance
Output Range:	Same as input (± 10 VFS)
Transfer Accuracy:	$\pm 0.01\%$ of full scale at 25° C.
Selector Input (Direct into Multiplexer):	One TTL Load
ON Level	Logic Zero (0 Volts)
OFF Level	Logic One (+3 Volts)
Power:	+15 Volts at 25 mA. -15 Volts at 25 mA.
Size:	Standard, double height, double width FLIP CHIP module.

HIGH IMPEDANCE MULTIPLEXER WITH OUTPUT BUFFER A161

**A
SERIES**



The A161 is a high impedance multiplexer consisting of 8 independent FET switched channels and a noninverting unity gain follower amplifier, designed for application where accuracy, high speed, and high input impedance are prime requirements.

This unit is DTL and TTL compatible and may be used with DEC K and M Series logic modules. It will also provide excellent performance with systems employing sample and holds, high speed multiplexing, A/D converters, as well as single and double level multiplexing.

Provided on the A161 are eight channel select lines, which may be controlled from an external source such as a shift register, clock, or gating function.

A161—\$375

The A161 has been engineered and factory adjusted to provide rated performance. It also employs advanced shielding techniques and optimized circuit layout, ensuring stable operation under normal ambient electrostatic and electromagnetic conditions, as well as allowing minimal crosstalk between channels.

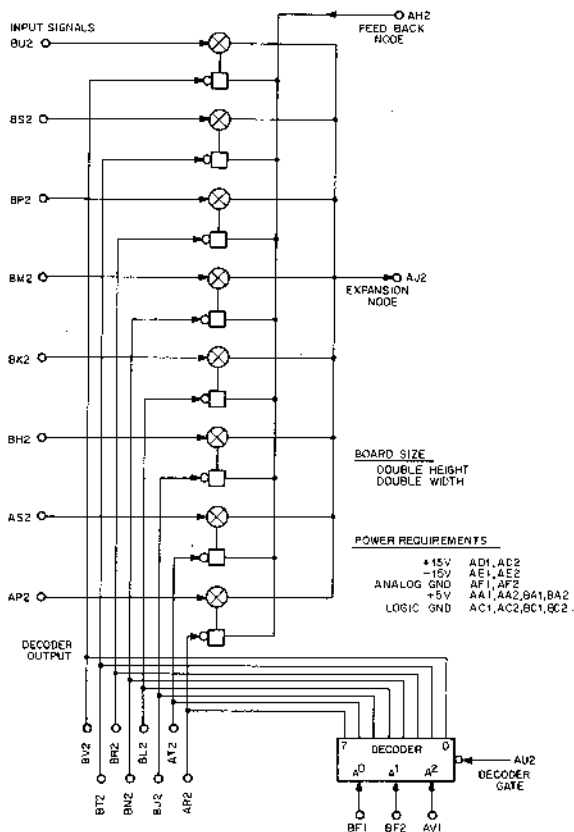
The A161 has the capability of output channel expansion simply by typing in the A160 or A162 Multiplexer Expanders.

SPECIFICATIONS

Analog inputs:	8 single ended
Input voltage range:	± 10 V. Maximum full scale
Expander node:	Common point of 8 channels brought out to pin as well as to input of buffer amplifier.
Input leakage:	0.5 nano Ampere, max., per channel
Input feedthrough capacity:	4 pF per channel
OFF channel capacity:	7 pF per channel, shunt capacity at common node
Series ON resistance of channel:	1000 ohms
Shunt ON Resistance to ground:	10^8 ohms min.
Switching plus settling time:	5 μ sec., max., to settle to within .01% of final value for full scale excursion with zero source impedance
Fault protection:	Current limiting to 10 mA. provided
Max. Input Voltage (Without Damage):	± 15 V.
Output Range:	Same as input (± 10 VFS)
Output Current:	± 20 mA., maximum
Output Protection:	Short circuit protection, indefinitely to ground
Amplifier Offset:	Adjustable to zero
Transfer Accuracy:	$\pm 0.01\%$ of full scale at 25° C.
Temp. Coefficient:	30 μ V/° C.
Selection Inputs (Direct into Multiplexer):	One TTL Load
ON Level:	Logic Zero
OFF Level:	Logic One
Power Requirements:	± 15 v. at 35 mA.
Size:	Standard, double height, double width FLIP CHIP module.

HIGH IMPEDANCE MULTIPLEXER WITH DECODER A162

A SERIES



The A162 is a high impedance multiplexer with decoder consisting of 8 independent FET switched channels. Included on this module is a gated binary to octal decoder for selecting any of the eight high speed channels.

The A162 may be used as a stand-alone multiplexer or with any of the high impedance multiplexers to perform single or double level multiplexing. It also may be used as an expander to increase the channel capabilities of the A163 or A164, Multiplexers.

This unit has been engineered and factory adjusted to provide rated performance, and is fully compatible with DTL and TTL systems.

A162—\$270

The A162 employs advanced shielding techniques and optimized circuit layout, ensuring stable operation under normal ambient electrostatic and electromagnetic conditions, as well as allowing minimal crosstalk between channels.

SPECIFICATIONS

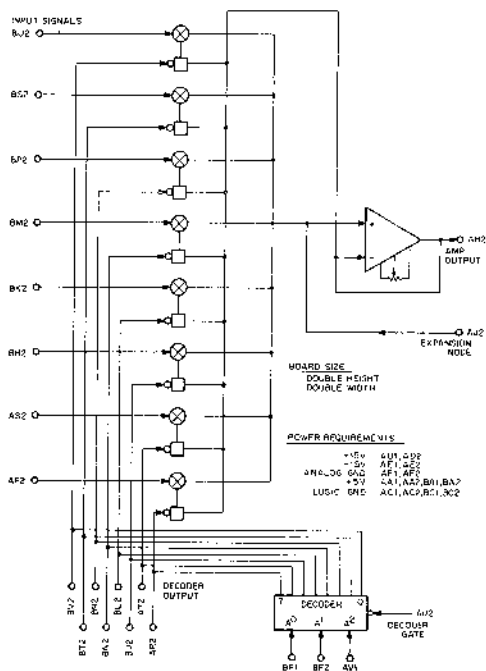
Analog Inputs:	8 Single Ended
Input Voltage Range:	± 10 V. Maximum full scale
Expander Node:	Common point of 8 channels brought out to a common pin for connection to the input of the external buffer amp.
Feedback Input:	Feedback control point of multiplexer switches connected to output of buffer amplifier.
Input Leakage:	0.5 nano Ampere, max., per channel
Input Feedthrough Capacity:	4 pF per channel
OFF Channel Capacity:	7 pF per channel, shunt capacity at common node
ON Resistance of Channel (Without Buffer):	1000 ohms
Switching Plus Settling Time:	5 μ sec., max., to settle to within .01% of final value for full scale excursion with zero source impedance

Decoder

Decoder:	One of 8 lines, decoded, binary
Decoder Outputs:	Select: Logic zero De-select: Logic one
Decoder Inputs—	
A0 IN to A2 IN:	Address Lines One TTL Load High = One
Decoder Gate Input:	Logic zero enables decoder out
Fault Protection:	Current limiting to 10 mA provided
Max. Input Voltage (Without Damage):	± 15 V.
Output Range:	Same as input (± 10 VFS)
Power Requirements:	± 15 v. at 35 mA. +5 v. at 30 mA. (with decoder option)

HIGH IMPEDANCE MULTIPLEXER WITH DECODER AND BUFFER A163

A SERIES



The A163 is a high impedance multiplexer consisting of 8 FET switched channels, a noninverting unity gain follower amplifier, and an 8 bit binary to octal decoder for channel selecting.

This unit was designed for application where accuracy, speed, and high input impedance are important factors. It also may be used in systems which employ sample and holds, D/A converters, and high speed multiplexing.

Provided on the A163 is an expansion node, which when used in conjunction with either of the high impedance multiplexer expanders (A160, A162) will provide additional input channels.

The A163 is fully compatible with DTL and TTL logic levels and may be used with DEC's standard K and M Series digital logic modules.

This module has been engineered and factory adjusted to provide proper operation over the specified range.

Optimized circuit layout has been employed in the packaging of the A163 ensuring minimal crosstalk between channels. Advanced shielding techniques

A163—\$395

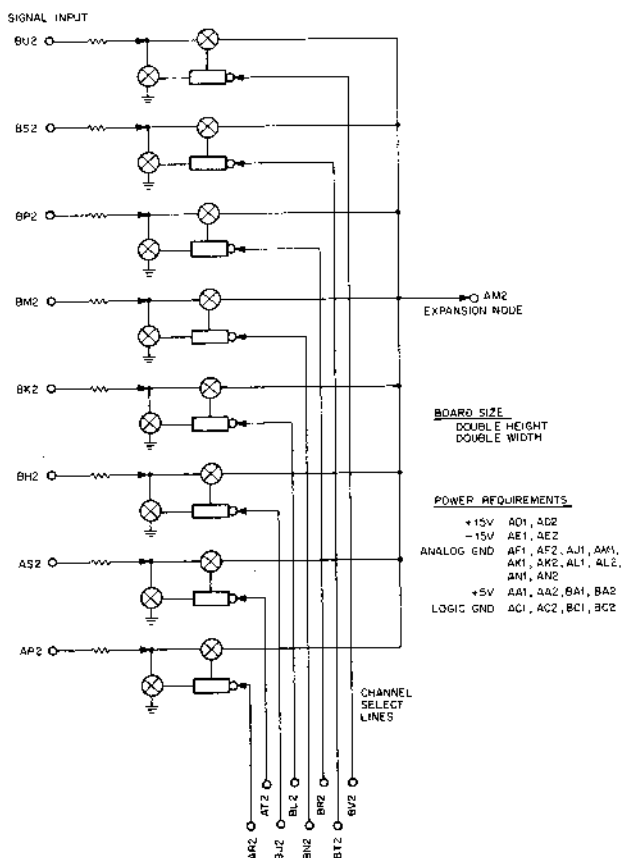
of the switching circuitry have been used to allow proper operation under normal ambient electrostatic and electromagnetic conditions.

SPECIFICATION

No. of Inputs:	8 Single Ended
Input Voltage Range:	± 10 V, maximum full scale
Expander Node:	Common point of 8 channels brought out to pin as well as to input of buffer amplifier
Input Leakage:	0.5 nano Ampere, max., per channel
Input Feedthrough Capacity:	4 pF per channel
OFF Channel Capacity:	7 pF per channel, shunt capacity at common node
ON Resistance of Channel (Without Buffer):	1000 ohms
Switching Plus Settling Time:	5 μ sec, max. to settle to within .01% of final value for full scale excursion with zero source impedance
Fault Protection:	Current limiting to 10 mA provided
Max. Input Voltage (Without Damage):	± 15 V.
Output Range:	Same as Input (± 10 VFS)
Output Current:	± 20 mA, max.
Output Protection:	Short circuit protection, indefinitely to ground
Amplifier Offset:	Adjustable to zero
Transfer Accuracy:	$\pm 0.01\%$ of full scale at 25° C.
Temp. Coefficient:	30 μ V/° C.
Decoder	
Decoder:	One of 8 lines, decoded, binary
Decoder Outputs:	Select: Logic zero De-select: Logic one
Decoder Inputs—	
A0 IN to A2 IN:	Address Lines One TTL Load
Decoder Gate Input:	Logic zero enables decoder out
Power Requirements:	± 15 V. at 35 mA. $+5$ V. at 30 mA (with decoder option)
Size:	Standard, double height, double width FLIP CHIP module.

EIGHT CHANNEL CONSTANT IMPEDANCE MULTIPLEXER EXPANDER A164

A SERIES



The A164 is an 8 channel constant impedance multiplexer expander utilizing eight FETS to switch the input signal through eight precision resistors either to ground (OFF) or to a virtual ground null point of an operational amplifier (ON).

This unit is used primarily with the A165, A166, and the A167 as a means of providing additional input channels. It may also be used to do high voltage multiplexing and input scaling.

A164—\$350

The A164 does not contain an output amplifier; therefore, to ensure proper operation, the output must be terminated into a buffer amplifier whose gain is equal to minus one. The A164 or the A165 may be used to accomplish this if the A164 is being used as an expander to either of these modules. If used as a stand alone module, the A260 dual amplifier card may be used as a buffer amplifier.

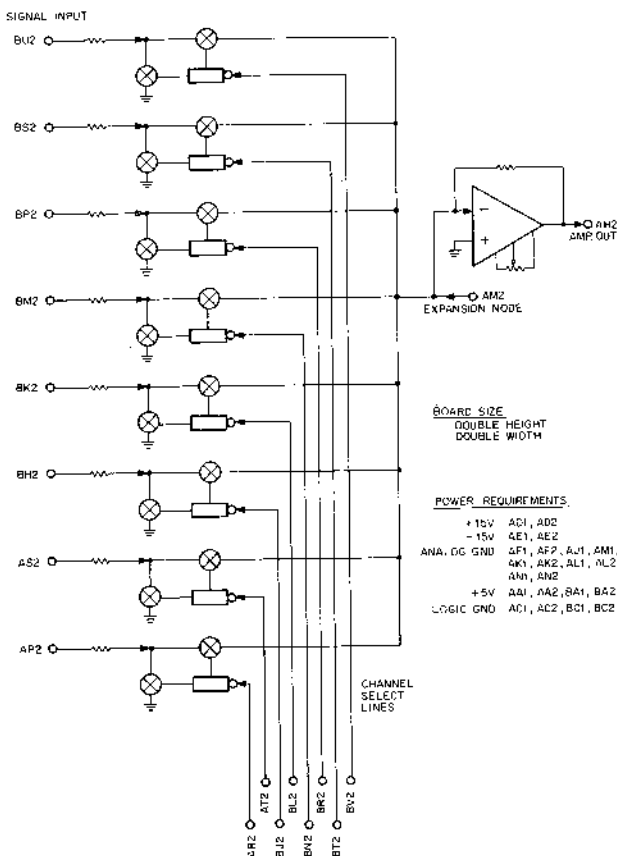
Provided on the A164 are eight channel select lines. These lines are brought to pin connections and may be controlled from an external source such as a shift register, clock, or gating functions.

SPECIFICATIONS

Number of Inputs:	8
Input Impedance:	10,000 ohms
Input Range:	± 10 Volts
Switching Plus Settling Time:	5 μ sec to .01%
Expander Node:	Summing point brought to pin to allow expansion of number of channels.
Switch Leakage:	0.5 nano Amp per "OFF" channel
Feedthrough (all channels OFF & 20 Vp-p at inputs):	-86dB at 1 kHz (Ratio = 20,000: 1)
Select Lines (1 TTL Load)—	
"ON":	Logic Zero
"OFF":	Logic One
Power Requirements:	± 15 v. at 40 mA.
Size:	Standard, double height, double width FLIP CHIP module.

CONSTANT IMPEDANCE MULTIPLEXER WITH OUTPUT AMPLIFIER A165

A SERIES



The A165 is a constant impedance multiplexer consisting of eight independent channels which utilize FETS to switch the input signal through precision resistors into either a ground (OFF) or a virtual ground of an operational amplifier (on).

Included on this module is the operational amplifier, which has been factory adjusted to yield a gain of minus one. Also included on the A165 are eight channel select lines which may be controlled from an external source, such as a shift register, clock, or gating functions.

A165—\$475

The A165 is DTL and TTL compatible and may be used with DEC's standard "K" and "M" Series modules to perform control functions.

The A165 may also be used in the multiplexing of high voltage or input scaling. It also may be used in conjunction with other constant impedance multiplexers.

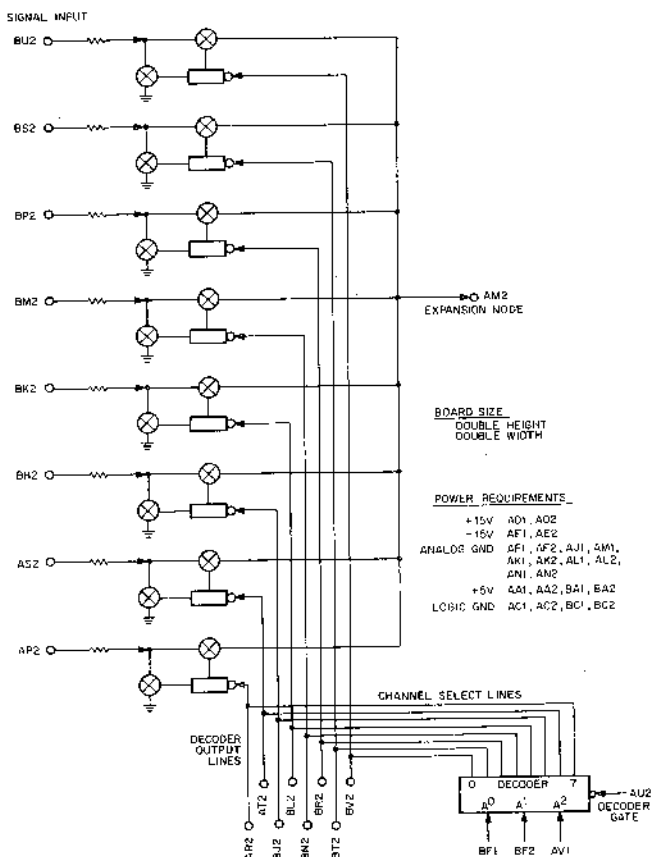
DEC's constant impedance multiplexers have been engineered and packaged using optimized circuit layouts to ensure minimal crosstalk between channels. Advanced shielding techniques allow stable operation under normal ambient electrostatic and electromagnetic conditions.

SPECIFICATIONS

Number of Inputs:	8
Input Impedance:	10,000 ohms
Input Range:	± 10 Volts
Output Range:	± 10 Volts, inverted with respect to input.
Output Drive:	20 mA.
Switching Plus Settling Time:	5 μ sec to .01%
Expander Node:	Summing point brought to pin to allow expansion of number of channels.
Switch Leakage:	0.5 nano Amp per "OFF" channel
Transfer Ratio:	Minus one for 10V range
Transfer Accuracy:	$\pm 0.015\%$ of full scale
Temp. Coefficient of Offset:	50 μ V/degrees C.
Temp. Coefficient of Gain:	7 PPM/degrees C.
Feedthrough (all channels OFF & 20 Vp-p at inputs):	-86dB at 1 kHz (Ratio 20,000 :: 1)
Select Lines (1 TTL Load)—	
"ON":	Logic Zero
"OFF":	Logic One
Power Requirements:	± 15 v. at 40 mA.
Size: Standard, double height, double width FLIP CHIP module.	

CONSTANT IMPEDANCE EXPANDER MULTIPLEXER WITH DECODER A166

A SERIES



The A166 is a constant impedance eight channel multiplexer with decoder.

This unit can be used for multiplexing high voltage signals, single level or double level multiplexing, input scaling, or as a means to expand the channel capabilities of either the A165 or A167 DEC multiplexer.

Contained on the A166 as a binary to octal decoder which can be used to select either randomly or in sequence any of the eight analog input channels.

If the A166 is to be used as a stand alone multiplexer, its output must terminate into the null point of a buffer amplifier whose feedback resistor is 10,000 ohms.

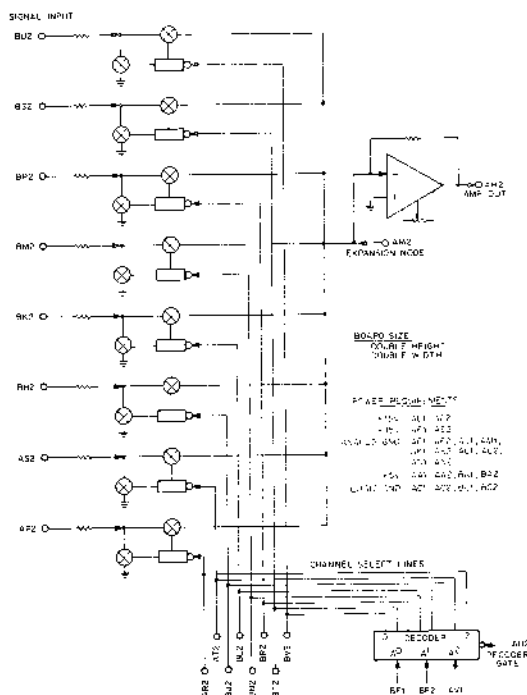
A166—\$365

SPECIFICATIONS

Number of Inputs:	8
Input Impedance:	10,000 ohms
Input Range:	± 10 Volts
Switching Plus Settling Time with output amp	5 μ sec to .01%
Expander Node:	Summing point brought to pin to allow expansion of number of channels.
Switch Leakage:	0.5 nano Amp per "OFF" channel
Transfer Accuracy:	$\pm 0.015\%$ of full scale
Feedthrough (all channels OFF & 20 Vp-p at inputs):	-86dB at 1 kHz (Ratio 20,000: 1)
Decoder	
Decoder:	One of 8 lines decoded, binary
Decoder Outputs:	9 TTL Loads Select = Logic Zero Deselect = Logic One
Select Lines (1 TTL Load)—	
"ON":	Logic Zero
"OFF":	Logic One
Decoder Inputs—	
A0 IN to A2 IN:	Address Lines—3 bit binary code One TTL Load Positive Voltage = Logic One
Decoder Gate:	One TTL Load Logic One yields disable Logic Zero yields enable
Power Requirements:	± 15 V. at 40 mA. ± 5 V. at 30 mA. (with decoder option)
Size:	Standard, double height, double width FLIP CHIP module.

CONSTANT IMPEDANCE MULTIPLEXER WITH DECODER AND OUTPUT AMP A167

A SERIES



The A167 is an eight channel constant impedance multiplexer with output amplifier and decoder. The operation of the A167 is performed in the same manner as any of the other DEC constant impedance multiplexers, where the input signal is switched via FETs to either ground (OFF) or into a virtual ground null point (ON) of the operational amplifier.

This unit may be used for multiplexing of high voltages, input scaling, and in situations that require single or double level multiplexing.

The A167 has the capability of being expanded by any of the constant impedance multiplexers (A166, A164). The limitation to the number of channel expansions will depend upon system specifications, speed, leakage current of OFF channels, and the output drive capabilities of the source.

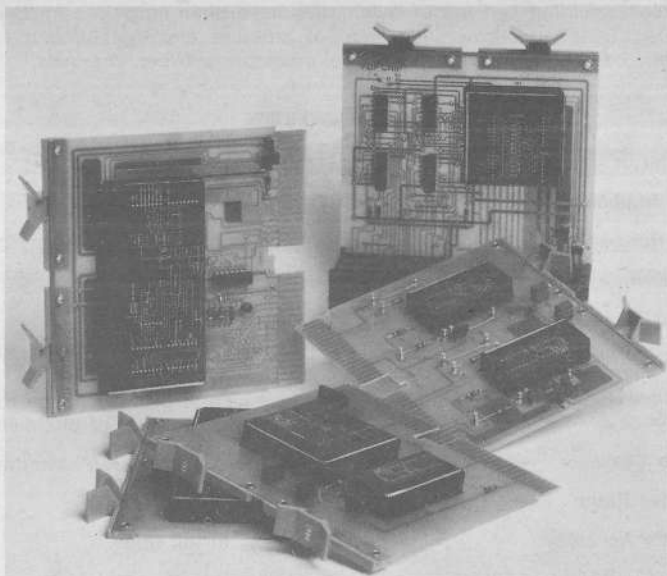
The output amplifier has been factory adjusted and preset to a gain of minus one. The decoder is an eight bit binary to octal decoder with gating facilities on the decoder to control its states.

A167—\$490

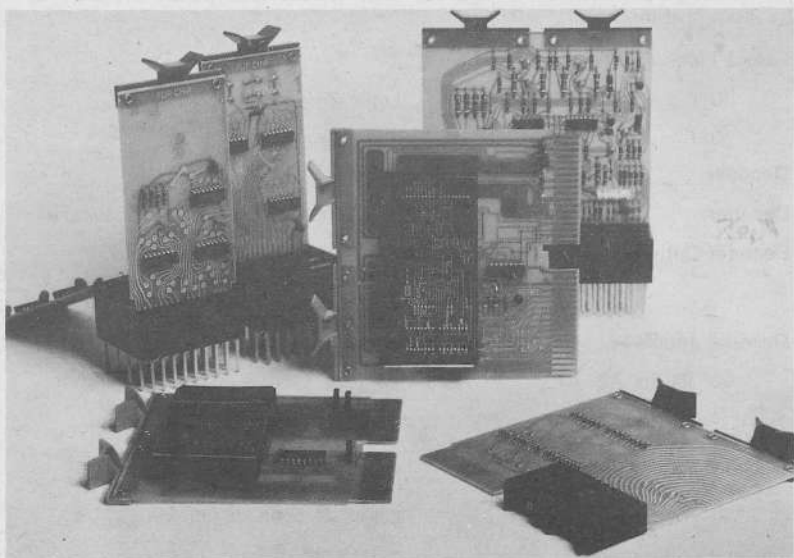
Advanced shielding and layout techniques have been employed on the A167 to allow stable operation under normal ambient electrostatic and electromagnetic conditions as well as minimal crosstalk between channels.

SPECIFICATIONS

Number of Inputs:	Eight
Input Impedance:	10,000 ohms
Input Range:	± 10 Volts
Output Range:	-10 Volts
Output Drive:	20 mA.
Switching Plus Settling Time:	5 μ sec to .01%
Expander Node:	Summing point brought to pin to allow expansion of number of channels.
Switch Leakage:	0.5 nano Amp per "OFF" channel
Transfer Ratio:	Minus one for 10V range
Transfer Accuracy:	+0.015% of full scale
Temp. Coefficient of Offset:	50 μ V/degrees C.
Temp. Coefficient of Gain:	7 PPM/degrees C.
Feedthrough (all channels OFF & 20Vp-p at inputs):	--86dB at 1 kHz (Ratio 20,000 : 1)
Select Lines (1 TTL Load)—	
"ON":	Logic Zero
"OFF":	Logic One
Decoder	
Decoder:	One of eight lines decoded, binary
Decoder Outputs:	9 TTL Loads Select = Logic Zero Deselect = Logic One
Decoder Inputs—	
A0 IN to A2 IN:	Address Lines—3 bit binary code One TTL Load Positive voltage = Logic One
Decoder Gate:	One TTL Load Logic One yields disable Logic Zero yields enable
Power Requirements:	± 15 V. at 40 mA. ± 5 V. at 30 mA. (with decoder option)
Size:	Standard, double height, double width FLIP CHIP module.



The A Series analog module line has been substantially expanded. Shown here are a few of the new units.



The A Series additions are DTL and TTL compatible and compatible with DEC K and M Series modules, computers, control systems and standard instrumentation.

NOTES ON OPERATIONAL AMPLIFIERS

I. INTRODUCTION

This article describes some of the basic characteristics and uses of operational amplifiers. It is written especially for people with a digital background, but with a limited exposure to analog technology. The equations presented are not exact, but are good engineering approximations, which are accurate enough for most applications. It is hoped that this simplified discussion will provide more insight into the uses and limitations of operational amplifiers than a more rigorous approach.

The operational amplifier is a basic building block in analog work, much the same way as a NAND gate can be a basic building block in a digital computer. An operational amplifier (op amp) together with other components such as resistors and capacitors, can be used to perform addition, subtraction, integration, and many other functions. Op amps can be used to make oscillators, active filters, and even digital circuits such as Schmitt triggers, gates, and flip-flops. When used with A/D and D/A converters in data processing work, op amps perform such functions as scale changing, offsetting, and isolation between source and load.

II. GENERAL CHARACTERISTICS

An operational amplifier can be considered a 3 terminal device, plus a common or ground return, see Fig. 1. Chopper-stabilized op amps, which will not be considered here, have the Plus input permanently tied to ground. The op amp is really a difference amplifier, in that it amplifies only the difference between the two inputs, and tries to reject any DC or AC signal that is common to both inputs.

Op amps are characterized by high DC gain, high input impedance, low output impedance, and a gain that decreases with increasing frequency. Op amps used without feedback would be operating open loop, a rare situation; but with feedback the operation would be closed loop. The use of properly applied negative feedback stabilizes the operation of the composite circuit against changes in the amplifier, and provides its versatility and usefulness.

When an op amp is working in the linear region, two approximations can be made to help in the analysis of the circuit configuration. First, the voltages of the two inputs are the same; and second, no current flows into or out of the input terminals. Fig. 2 shows a simple inverting amplifier. Assume the Minus Input is 0 volts, the same as the Plus Input, and that no current flows into the Minus Input, called the summing junction. Then $i_1 = i_f$, and some simple manipulations show that the gain is equal to $-R_f/R_1$. Similar reasoning applied to the non-inverting amplifier of Fig. 3 shows that the gain is equal to $1 + \frac{R_2 + R_3}{R_1}$. An easy way to remember this is to think of the two resistors as forming a tapped divider network.

III. SPECIFICATIONS

Specifications are usually given for open loop performance, so that the user has to interpret and calculate how this will affect his particular closed loop circuit. The following section will give some brief descriptions of what some of the specifications mean.

Settling time. This is the time it takes the output to get within and stay within a certain amount of its final value, after the input has received a step input, see Fig. 4. This parameter is important when an amplifier is used in front of an A/D converter, since the A/D should not begin its conversion until the amplifier has settled.

Overload recovery. It takes an overload recovery time for the output to first assume its proper value after an overdriving input signal has been removed. However, the output still has not settled, and this extra time must be waited before the output is valid.

Slew rate. This term is comparable to rise or fall time in a digital circuit. It is a measure of how fast the output can change. If an amplifier output could go from 0 volts to 10 volts in 2 μ sec, it would have a slew rate of 5 volts/ μ sec.

Frequency for full output. This is the maximum frequency at which a full scale sine wave (such as +10 to -10 volts) can be assured at the output, without noticeable distortion. In many ways this is real frequency limitation of an op amp, since up to this frequency there are no other restrictions on the amplitude of the input signal.

Frequency for unity gain. The open loop gain of an amplifier is equal to one at this frequency. But the input signal must be restricted in amplitude such that the maximum rate of change of output (slew rate) is not exceeded. Usually only millivolt signals may be processed at this frequency, therefore the full amplifier bandwidth is not usable for normal data processing systems.

Impedance. The input impedance is simply the resistance between the two inputs. The common mode impedance is the highest resistance attainable with feedback.

Common mode rejection. This is a measure of how well an amplifier will not respond to a signal common to both inputs. If used as a voltage follower, an op amp with a common mode rejection ratio (CMRR) of 10,000 could have error of 1 mv if the input were 10 v. (10/10,000 volts).

Voltage offset. The inability to achieve perfect balance in the input circuit causes the output to respond to an apparent signal when the inputs are tied to ground. For an inverting amplifier, the output error due to the input voltage offset is equal to the offset times the closed loop gain plus one. With an input offset of 3 mv, and a gain of 1, the output error would be 6 mv. Fortunately, initial voltage offset can be trimmed with a potentiometer at the right place in the circuit.

Current offset. Current offset (or bias current) multiplied by the feedback resistor (Fig. 2) produces an output error. This effect can be minimized by using the differential offset (the difference in offset currents for the two inputs) when the resistance seen from both inputs to ground are equal. For Fig. 2, the Plus Input should then be returned to ground through a resistor equal to the parallel combination of R_1 and R_f .

Output ratings. The output voltage and current ratings imply a minimum value for the load resistor. 10 volts and 5 ma would correspond to a load resistor of 2 K. In an inverting amplifier, the feedback resistor is a load for the output, and the current through this resistor must be subtracted from

the amount of current still available at the output. All really useful operational amplifiers can be shorted to ground without damage, but shorting to a voltage will usually destroy some of the circuitry.

IV. APPLICATIONS

Some common configurations for operational amplifiers are shown in Figs. 5 through 10. The pin letter assignments correspond to the op amps sold by Digital Equipment Corp. If these op amps are used, the jumper between Pin 5 and the Minus input should be removed.

The voltage follower, Fig. 5, features high input impedance, but will have an error depending on the CMRR. Large voltages cannot be handled, since common mode voltage ratings should not be exceeded. The inverter configuration, Fig. 7, is very versatile and does not have a common mode voltage problem, since both inputs are near ground. Large input voltages can be handled if the input resistor is made appropriately large. One disadvantage of the inverting configuration is that the input impedance is relatively low, essentially equal to the input resistor. When a gain trim potentiometer is used, the gain accuracy by itself becomes irrelevant. What is important is gain resolution (mostly determined by the potentiometer), and the gain stability (mostly determined by the temperature coefficients of the input and feedback resistors). The ratio of the closed loop gain to the open loop gain gives the suitability of an amplifier as far as static accuracy is concerned. With a closed loop gain of 5, and an open loop gain of 10,000, an amplifier could be used in a system with an allowable error of 1 part in 2,000.

The possibility of oscillation must always be considered when feedback amplifiers are used. Usually the more feedback used, the greater is the tendency to oscillate. Oscillations can always be attributed to phase shift. Therefore, stabilization of operational amplifiers involves phase shifting to oppose oscillation. In Fig. 7, the feedback capacitor allows high frequency signals to be fed back to the inverting input (degenerative feedback) with a phase lead. In the inverting configuration, the output will be 180° out of phase with the input at low frequencies, and the feedback signal will oppose the input signal. At high frequencies, there are additional phase lags in the amplifier and feedback circuitry. If the feedback signal has a total phase shift (lag) of 360° with a gain through the amplifier and feedback network of greater than 1, the amplifier will oscillate, since the input and output are in phase.

V. REFERENCES

1. "An Operational Amplifier Application Manual"
Analog Devices, Inc., Cambridge, Mass.
2. "Handbook of Operational Amplifier Applications"
Burr-Brown Research Corp., Tucson, Arizona
3. "Linear Integrated Circuits Applications Handbook"
Fairchild Semiconductor, Mountain View, California
4. "Applications Manual for Operational Amplifiers"
Philbrick/Nexus Research, Dedham, Mass.

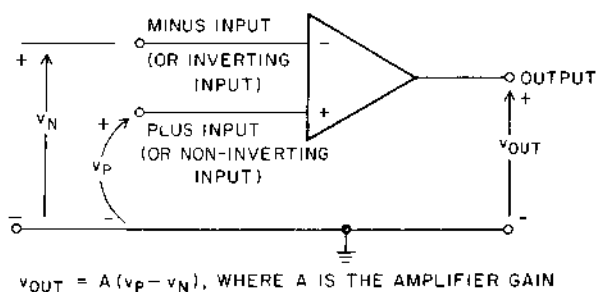


Fig. 1, Basic Operational Amplifier Symbol

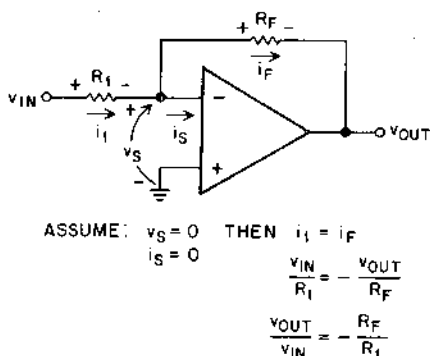


Fig. 2, Inverting Amplifier

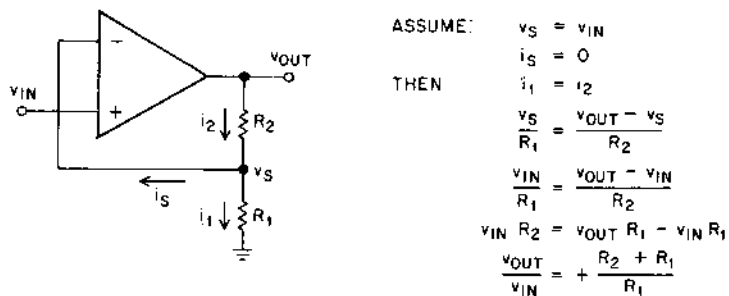


Fig. 3, Non-Inverting Amplifier

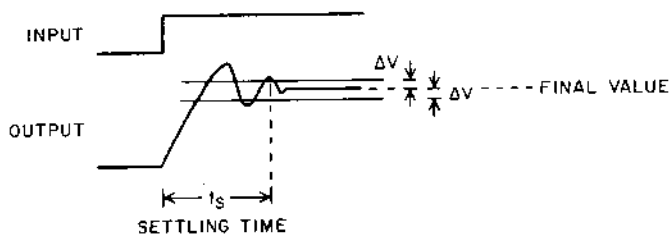


Fig. 4, Setting Time

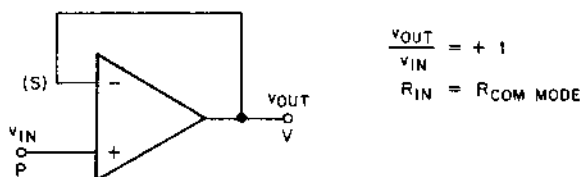


Fig. 5, Voltage Follower

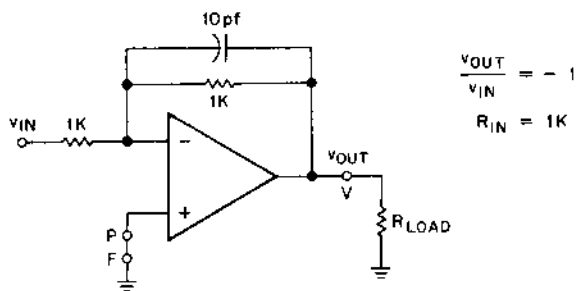
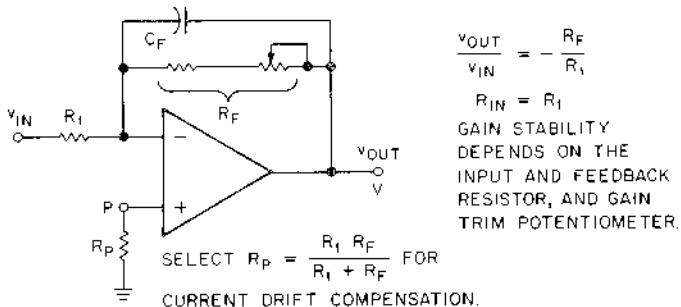


Fig. 6, Inverter



TYP VALUES

R_1 1K TO 10K

R_F 1K TO 100K

R_P 500Ω TO 5K

THE USE OF C_F REDUCES THE
 TENDENCY OF THE OP AMP
 TO OSCILLATE

Fig. 7, Adjustable Gain and Current Compensation

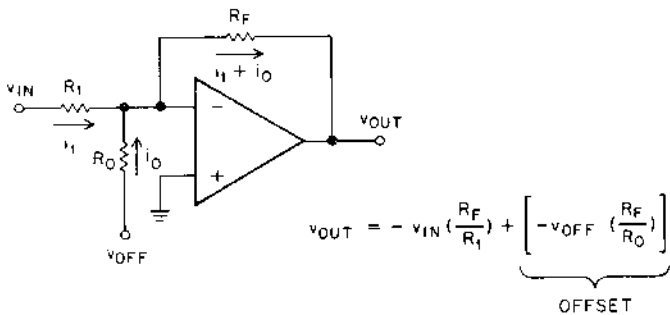


Fig. 8, Offsetting

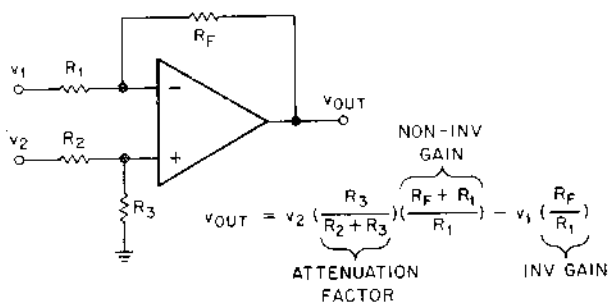
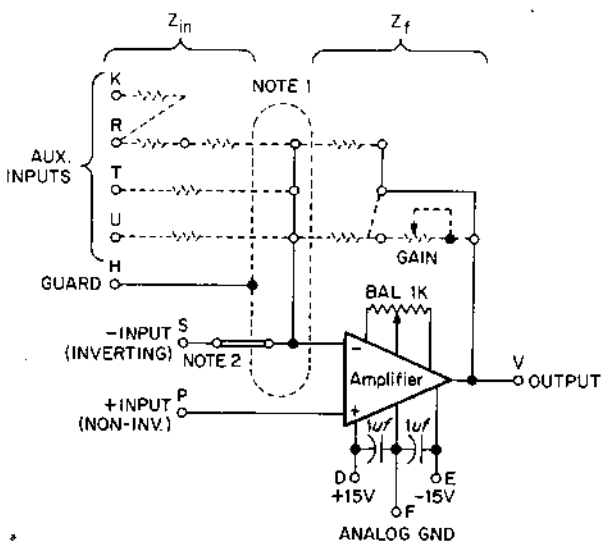


Fig. 9, Differential Gain

OPERATIONAL AMPLIFIER A207

A SERIES



NOTE 1. Mounting holes are provided on the module so that input and feedback components can be added. Components shown with dashed lines are not included with the module.

NOTE 2. This jumper comes with the module. It may be removed to suit circuit requirements.

NOTE 3. Pins L & M can be connected together to improve settling time, but parameters such as drift and open loop gain are degraded.

The A207 is an economical Operational Amplifier featuring fast settling time ($5 \mu\text{s}$ to within 10 mv), making it especially suited for use with Analog-to-Digital Converters. The A207 can be used for buffering, scale-changing, off-setting, and other data-conditioning functions required with A/D Converters. All other normal operational amplifier configurations can be achieved with the A207.

The A207 is supplied with a zero balance potentiometer. Provisions are made on the board for the mounting of input and feedback components, including a gain trim potentiometer. The A207 is pin-compatible with the A200 Operational Amplifier.

A207—\$45

SPECIFICATIONS—At 25°C, unless noted otherwise.Pins L & M Differences with Pins
Connected L & M Not Connected**Settling Time***

Within 10 mV, 10V step input, typ:	3 μ sec	6 μ sec
Within 10 mV, 10V step input, max:	5 μ sec	8 μ sec
Within 1 mV, 10V step input, max:	7 μ sec	10 μ sec

Frequency Response

Dc open loop gain, 670 ohm load, min:	15,000	100,000
Unity gain, small signal, min:	3 MHz	
Full output voltage, min:	50 kHz	
Slewing rate, min:	3.5v/ μ sec	
Overload recovery, max:	8 μ sec	

Output

Voltage, max:	-10V
Current, max:	\pm 15 mA

Input Voltage

Input voltage range, max:	\pm 10V
Differential voltage, max:	\pm 10V
Common mode rejection, min:	10,000

Input Impedance

Between inputs, min:	100 k ohms
Common mode, min:	5 M ohms

Input Offset

Avg. voltage drift vs. temp, max:	60 μ V/ $^{\circ}$ C	30 μ V/ $^{\circ}$ C
Initial current offset, max:	0.5 μ A	
Avg. current drift vs. temp, max:	5 nA/ $^{\circ}$ C	

Temperature Range

0°C to +60°C

Power

+15v (pin D), quiescent:	6 mA
-15v (pin E), quiescent:	10 mA

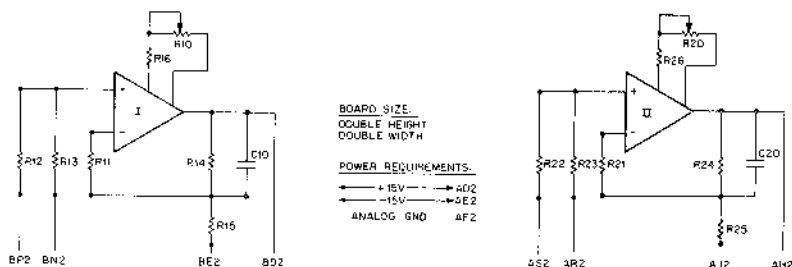
If the Output is accidentally shorted to ground, the amplifier will not be damaged.

Size: Standard, single height, single width FLIP CHIP module.

*Gain of 1, inverting or non-inverting configuration.

DUAL AMPLIFIER CARD A260

A SERIES



The A260 is a universal dual amplifier card which contains two independent operational amplifiers. Provisions have been made for mounting input and feedback components so that the A260 may be used in a variety of modes.

Some of the configurations in which the A260 may be used are:

1. Voltage follower with a gain of plus one.
2. Voltage follower with positive gain of greater than one.
3. Attenuated follower with positive gain of less than one.
4. Differential amplifier with differential input and single ended output.
5. Inverter with negative gain of one or greater.

The A260 may also be used as the output buffer for the A160 and A164 multiplexer series, as well as the input buffer for the A400 series sample and hold modules. Individual offset adjustments are provided for on each amplifier.

A260—\$300

SPECIFICATIONS

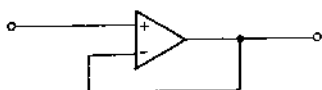
Description:	Two differential amplifiers mounted on one board with provision for mounting resistors in a variety of modes.
Offset:	Adjustments provided to adjust offset to zero.

Configurations

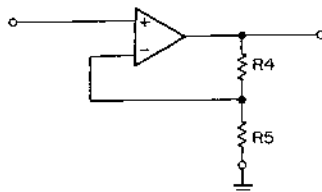
A. Follower	High input impedance, gain of plus one.
Transfer Accuracy:	$\pm 0.01\%$ of FS
Settling Time (0 to 10v):	1.5 μ s to .01%
Output drive:	20 mA., short circuit proof to ground.
Input/output range:	± 10 Volts
Input impedance:	1000 megohms
Temp. Coefficient:	30 μ V/ $^{\circ}$ C.
B. Follower with Gain—	High input impedance, positive gain greater than one.
Transfer accuracy:	Function of resistors provided.
Gain:	Determined by $\frac{R14 + R15}{R15}$
Settling Time:	(Gain) x (1.5 μ s) to .01%
Output Drive:	20 mA. short circuit proof to ground.
Input/Output range:	± 10 Volts
Input Impedance:	≥ 100 megohms
Temp. Coefficient:	30 μ V/ $^{\circ}$ C. (referred to input)
C. Attenuated follower—	Input attenuator, positive gain less than one.
Gain:	$\frac{R13}{R12 + R13}$ (see schematic)
Transfer Accuracy:	Function of resistors provided.
Settling Time:	1.5 μ s to .01% if not limited by attenuator.
Input Range:	0 to ± 100 Volts, max.
Output Range:	± 10 Volts

Output Drive:	20 mA., short circuit proof to ground.
Input Impedance:	$R12 + R13$
Temp. Coefficient:	$30 \mu V/^{\circ} C.$ plus input attenuation.
D. Differential Amplifier:	Differential input, single ended output.
Gain:	$\frac{R14}{R15}$
Transfer Accuracy:	Function of resistors provided.
Settling Time:	$(\text{Gain}) \times (1.5 \mu s)$
Input Voltage (Signal plus common mode):	$(1 + \frac{1}{\text{Gain}}) \times (10V) \text{ max.}$
Output Range:	$\pm 10 \text{ Volts}$
Output Drive:	20 mA., short circuit proof to ground.
Temp. Coefficient:	$(30 \mu V/^{\circ} C) \times (1 + \text{Gain})$
Common Mode Rejection:	Function of resistor matching in each input $> 86 \text{ dB}$ for .01% resistor watch in addition to transfer accuracy of .01%
E. Inverter	Negative gain of one or greater
Specs same as differential amplifier, except input referenced to ground.	
F. Power	
	+15v @ 20mA
	-15v @ 15mA
Size:	Standard, double height, double width FLIP CHIP module.

1. FOLLOWER

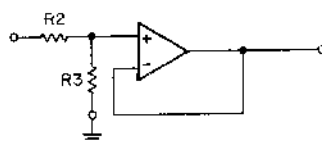


2. PLUS GAIN



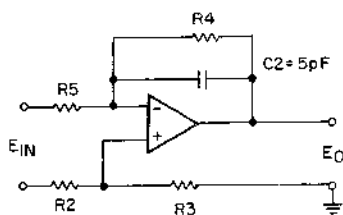
$$\frac{E_O}{E_{IN}} = \frac{R_4 + R_5}{R_5}$$

3. POSITIVE GAIN LESS THEN ONE



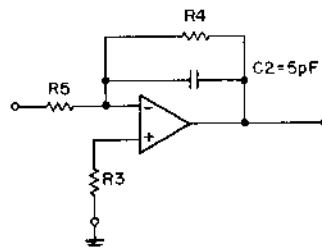
$$\frac{E_O}{E_{IN}} = \frac{R_3}{R_3 + R_2}$$

4. DIFF. INPUT



$$\frac{E_O}{E_{IN}} = \frac{R_4}{R_5}$$

5. INVERTER

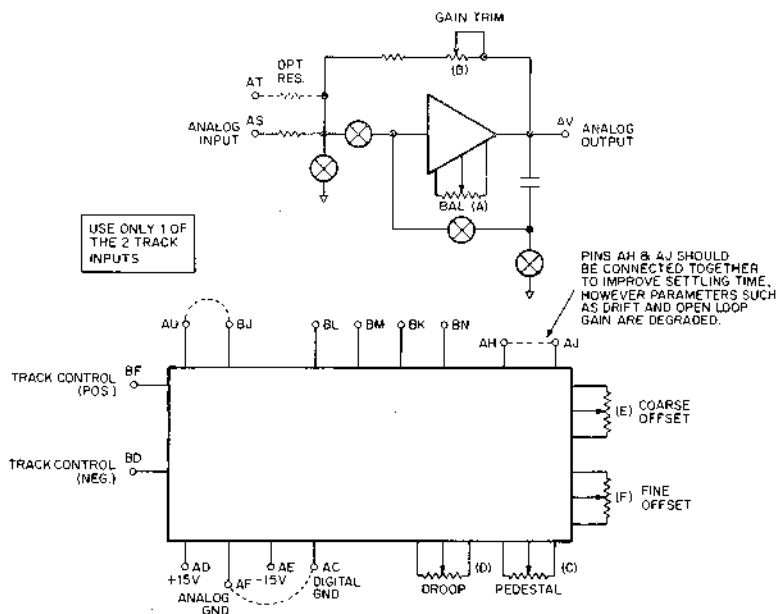


$$\frac{E_O}{E_{IN}} = \frac{R_3}{R_4}$$

R12 R22	R13 R23	R14 R24	R15 R25
0Ω	∞	0	∞
0Ω	∞	5K G =	5K +2
		9K G =	1K +10
50K G =	50K +1/2	0	∞
20K	20K G =	20K 1	20K
∞	10K G =	20K -1	20K

SAMPLE AND HOLD A404

A SERIES



JUMPER CONNECTIONS TO OFFSET OUTPUT

MODE			Positive	Negative
PIN	TRACK	(sample) HOLD	AU to BJ	AU to BJ
BF (pos)	+3v or open	0v		BL to AD
BD (neg)	-3v or open	0v	BM to AE	
			BK to AF	BN to AF

Analog gnd (pin AF) and digital gnd (pin AC) must be connected together at one point in the system.

The A404 Sample & Hold has an acquisition time of 6 μ sec for a 10 volt signal to within 10 mV (0.1%). The circuit inverts the input signal, and has an input impedance to 10 k. Features of the circuit include potentiometers to control the pedestal and the droop of the output signal.

A404—\$130

Two digital Track Control (sample) inputs are provided: one for negative logic (0v & -3v), and the other for positive logic (0v & +3v). Either input by itself will perform the necessary control, and the inadvertent application of both digital signals will cause no damage to the circuit.

Potentiometers are also provided for zero balancing, gain trim, and offset adjustment (up to $\pm 10v$). If offsetting is desired, connections should be made according to the table shown with the diagram. The A404 is pin-compatible with the A400 Sample & Hold.

SPECIFICATIONS—At 25°C, unless noted otherwise. Pins AH & AJ are connected together.

Acquisition Time

Within 10 mV, 10V step input, typ:	4 μ sec
Within 10 mV, 10V step input, max:	6 μ sec
Within 2.5 mV, 10V step input, max:	11 μ sec

Aperture Time, max: 0.2 μ sec

Gain -1.000 (adjustable $\pm 0.2\%$)

Input

Voltage range, max:	$\pm 10V$
Impedance:	10 k ohms

Output

Voltage range, max:	$\pm 10V$
Current, max:	10 mA

Pedestal*

Initial pedestal:	Adjustable to less than 1 mV
Pedestal variation vs. temp, max:	0.2 mV/°C

Droop

Initial droop:	Adjustable to less than 5 mV/ms
Droop variation vs. temp, max:	2 mV/ms/°C

Track Control

Pos. (pin BF)	+3V, Track 0V at 2 mA, Hold
Neg. (pin BD)	-3V, Track 0V at 1 mA, Hold

Board Size 1 double height board, single module width

Temperature Range 0°C to +50°C

Power

+15v (pin AD), quiescent:	22 mA
-15v (pin AE), quiescent:	35 mA.

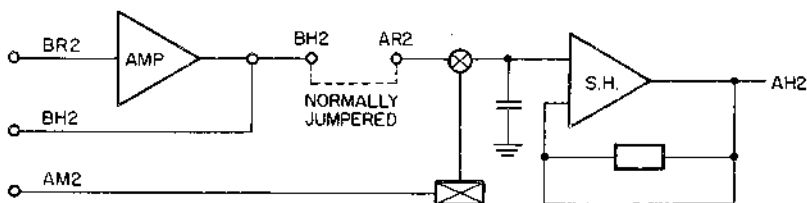
If the Output is accidentally shorted to Ground, the circuit will not be damaged.

Size: Standard, double height, single width FLIP CHIP module.

*Difference in output voltage when changing from Track to Hold mode.

SAMPLE AND HOLD A460/A461

A SERIES



POWER REQUIREMENTS:

-15V AE2
+15V AD2
ANALOG GND AF2

BOARD SIZE:

DOUBLE HEIGHT
DOUBLE WIDTH

The A460 and A461 are one channel sample and held modules used to sample the value of a changing analog signal at a particular point in time and store this information.

The difference between the A460 and the A461 is that the A460 is a S/H without input buffering and the A461 is S/H with input buffering. It should be noted that when using the A461 an external jumper is required between pins BH2 and AR2.

Provided on the A460 and A461 is a select line which can be used to control the sample or hold operation of the module.

Both the A460 and A461 are DTL and TTL compatible and may be used with standard "M" or "K" Series modules in control and system configurations.

The output circuitry consists of a buffer amplifier with output drive capability of 20 ma. Both the A460 and A461 are compatible with DEC "A" Series high impedance and constant impedance multiplexers and may be used in conjunction with each to perform various levels of multiplexing.

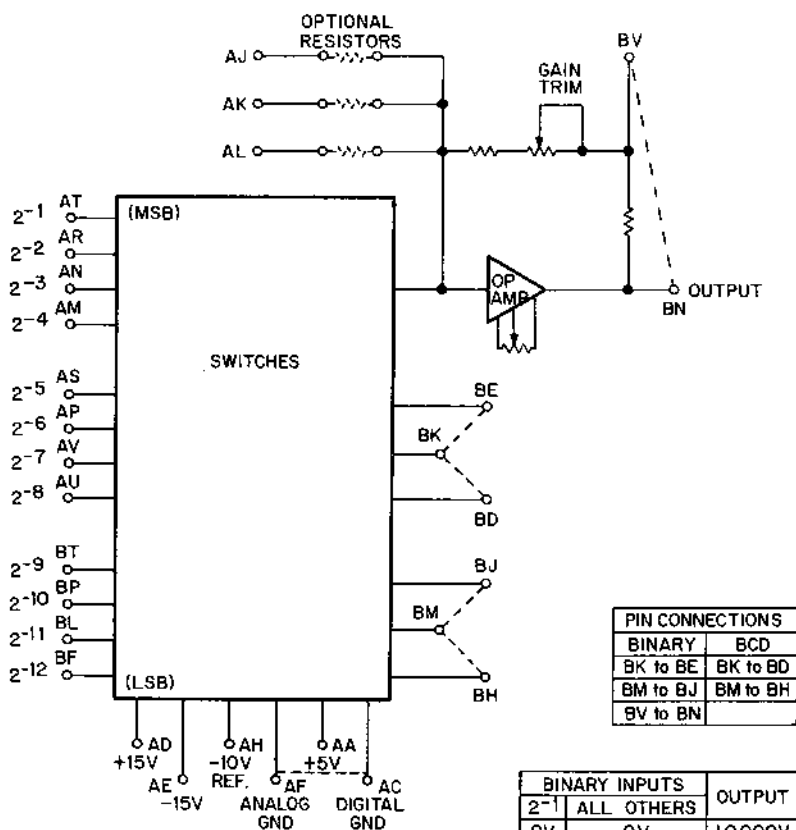
A460—\$400
A461—\$525

SPECIFICATIONS

Transfer Accuracy at 23° C.	±0.01% FS
Input/Output Voltage Range	±10V Full Scale
Transfer Characteristic	+1
Acquisition Time (to 0.01%)	5 microseconds for -10V to +10V excursion
Aperture Time	Less than 50 nanoseconds
Input Impedance (During Sample Time)— (With No Buffer):	100 ohms in series with 0.002 microfarad capacitor
	34
(With Buffer):	1000 meg ohms in parallel with 10 pF.
Output Drive:	20 mA.
Hold Decay:	15 microvolts per millisecond
Offset:	Adjustable to zero
Temp. Coefficient of Offset:	50 μ V/° C.
Control Input (1 TTL Load)— Sample:	Logic Zero
Hold:	Logic One
Power:	±15V at 12 mA w/o buffer ±15V at 20 mA with buffer
Size: Standard, double height, double width FLIP CHIP module.	

12-BIT DAC A613

A SERIES



PIN CONNECTIONS	
BINARY	BCD
BK to BE	BK to BD
BM to BJ	BM to BH
BV to BN	

BINARY INPUTS		OUTPUT
2 ⁻¹	ALL OTHERS	
0V	0V	+0.000V
+3	0	+5.000
+3	+3	+9.975

ANALOG GND (PIN AF) & DIGITAL GND (PIN AC)
MUST BE CONNECTED TOGETHER AT ONE
POINT IN THE SYSTEM.

The A613 is a 12-bit Digital-to-Analog Converter for moderate speed applications. The module is controlled by standard positive logic levels, has an output between 0v and +10v, and will settle within 50 μ sec for a full scale input change. The input coding can be either straight binary or 3 decades of 8421 BCD with only simple connector jumpers required to take care of the change.

A613—\$200

The A613 requires a -10.0V reference that can supply negative current, such as an A704. Provisions are made for adding up to 3 extra resistors to implement offsetting functions. Potentiometers are provided for zero balancing, and gain trim. The A613 is a double height board.

An input of all Logic 0's produces zero volts out; all Logic 1's produces close to $+10\text{V}$ out. The operational amplifier output can be shorted to Ground without damaging the circuit.

SPECIFICATIONS

Inputs

Logic ONE:	$+2.0\text{V}$ to $+5.0\text{V}$
Logic ZERO:	0.0V to $+0.8\text{V}$
Input loading:	1 mA (max.) at 0 Volts

Output

Standard:	0V to $+10\text{V}$
Optional, (requires Positive REF)	10v range between -10V and $+10\text{V}$
Settling time, (10V step):	50 μsec
Output current:	10 mA
Capacitive loading:	0.1 μF (without oscillation)

Binary Dig. In.	Analog Out	BCD (8421)	Analog Out
000 — 00	0.0000v	000	0.000v
000 — 01	$+0.0025$	001	$+0.010$
001 — 00	$+5.0000$	050	$+0.500$
111 — 11	$+9.9975$	500	$+5.000$
		999	$+9.990$

Accuracy

	Binary	BCD
At $+25^{\circ}\text{C}$:	$\pm 0.015\%$ of full scale	$\pm 0.05\%$ of full scale
Temp. coef:	$\pm 0.001\%/^{\circ}\text{C}$ (plus drift of REF)	$\pm 0.002\%/^{\circ}\text{C}$ (plus drift of REF)

Temperature Range

$+10^{\circ}\text{C}$ to $+50^{\circ}\text{C}$

Power

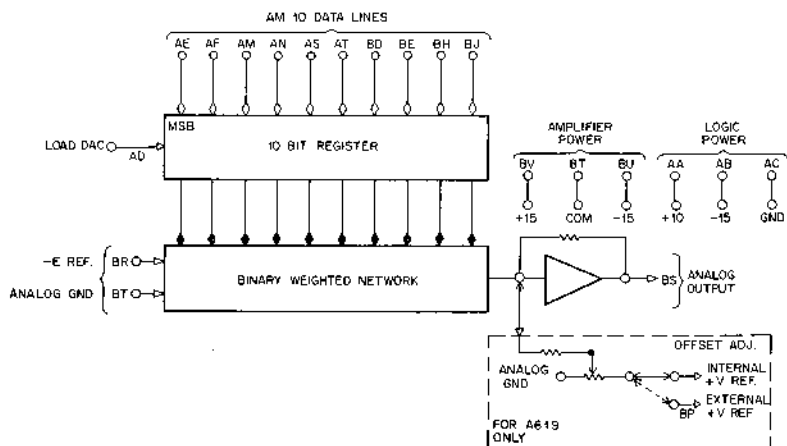
$+15\text{V}$ at 35 mA	} at max. load
-15V at 60 mA	
$+5\text{V}$ at 60 mA	
-10.0V REF at -7 ma (reverse current)	

If the Output is accidentally shorted to Ground, the output amplifier will not be damaged.

Size: Standard, single height, single width FLIP CHIP module.

10-BIT D/A CONVERTER SINGLE BUFFERED A618 and A619

A SERIES



The A618 and the A619 Digital to Analog Converters (DAC) are double width in the lower (B section) half. The converters are complete with a 10-bit buffer registers, level converters, a precision divider network, and a current summing amplifier capable of driving external loads up to 10 mA. The reference voltage is externally supplied for greatest efficiency and optimum scale factor matching in multi-channel applications.

The A619 DAC output voltage is bi-polar while the A618 DAC output voltage is uni-polar.

Binary numbers are represented as shown (right justified) in Table 1:

TABLE 1

Binary Input	Analog Output (Standard)	
	A618	A619
0000 ₈	0V	-5V
0400 ₈	+2.5V	-2.5V
1000 ₈	+5.0V	0 V
1400 ₈	+7.5V	+2.5V
1777 ₈	+10.0V	+5V

A618—\$300

A619—\$325

OUTPUT:

Voltage: A618	0 to +10 volts
Voltage: A619	±5 volts
Current:	10 mA. (max)
Impedance:	<0.1 ohm
Settling Time:	
(Full scale step, resistive load)	<5.0 µsec
(Full scale step, 1000 pf)	<10.0 µsec
Resolution:	1 part in 1024
Linearity:	±0.05% of full scale
Zero Offset:	±5 mV. (max)
Temperature Coefficient:	<0.2 mV/°C
Temperature Range:	0 to 50°C

INPUT

Level: 1 TTL Unit Load	
Pulse: (positive)	
Input loading: 20 TTL Unit load	
Rise and Fall Time:	20 to 100 nsec
Width:	>50 nsec
Rate:	10 ⁶ Hz max.
Timing:	

Data lines must be settled 40 nsec before the "LOAD DAC" pulse (transition) occurs.

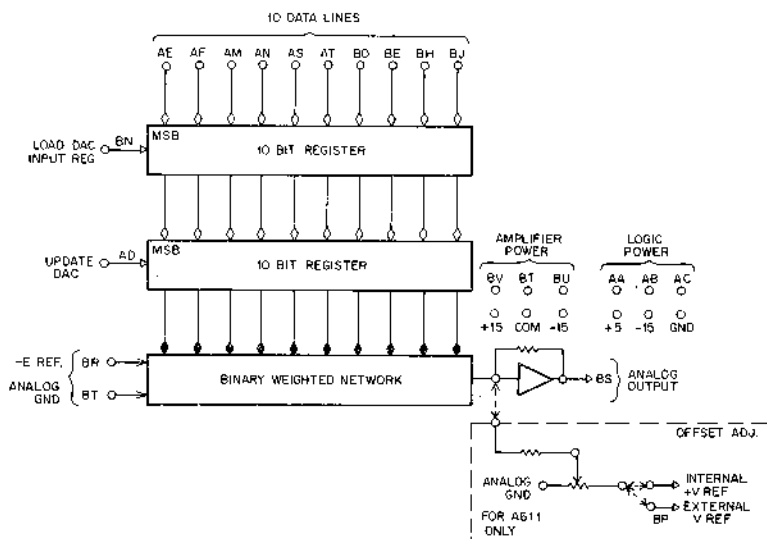
POWER REQUIREMENTS:

Reference Power:	—10.06 Volts, 60 mA
Amplifier Power:	±15 Volts, 25 mA (plus output loading)
Logic Power:	+5 Volts, 135 mA
	—15 Volts, 60 mA

Size: Standard, double height, single width FLIP CHIP module.

10-BIT D/A CONVERTER DOUBLE BUFFERED TYPES A620 and A621

A SERIES



The A620 and the A621 Digital-to-Analog Converters (DAC) are double-width in the lower (B section) half. The converters are complete with two 10-bit buffer registers, level converters, a precision divider network, and a current summing amplifier, capable of driving external loads up to 10 mA. The reference voltage is externally supplied for greatest efficiency and optimum scale-factor matching in multi-channel-application.

The A621 DAC output voltage is bi-polar while the A620 DAC output voltage is uni-polar.

The double-buffered DAC's are offered to satisfy those applications where it is imperative to update several analog output simultaneously. When DAC's deliver input to a multi-channel analog tape system or update the constants of an analog computer, the double-buffer feature may be necessary to prevent skew in the analog data.

A620—\$300
A621—\$375

Binary numbers are represented as shown (right justified) in Table 1:

TABLE 1

Binary Input	Analog Output (Standard)	
	A620	A621
0000 ₈	0V	-5V
0500 ₈	+2.5V	-2.5V
1000 ₈	+5.0V	0V
1500 ₈	+7.5V	+2.5V
1777 ₈	+10.0V	+5V

OUTPUT:

Voltage: A620	0 to 10 Volts
Voltage: A621	±5 Volts
Current:	10 mA. (max)
Impedance:	<0.1 ohms
Settling Time:	
(Full scale step, resistive Load)	<5.0 μsec
(Full scale step, 1000 pf)	<10 μsec
Resolution:	1 part in 1024
Linearity:	±0.05% of full scale
Zero Offset:	+5 mV. (max)
Temperature Coefficient:	<0.2 mV/°C
Temperature Range:	0 to 50°C

INPUT:

Level: 1 TTL Unit load	
Pulse: (positive)	
input loading:	20 TTL Unit load
Rise and Fall Time:	20 to 100 nsec
Width:	>50 nsec
Rate:	10 ⁶ Hz (max)

Timing:

1. Data lines must be settled 40 nsec before the "LOAD DAC" pulse (transition) occurs.
2. The "Update DAC" pulse must occur more than 100 nsec after the "LOAD DAC" pulse.

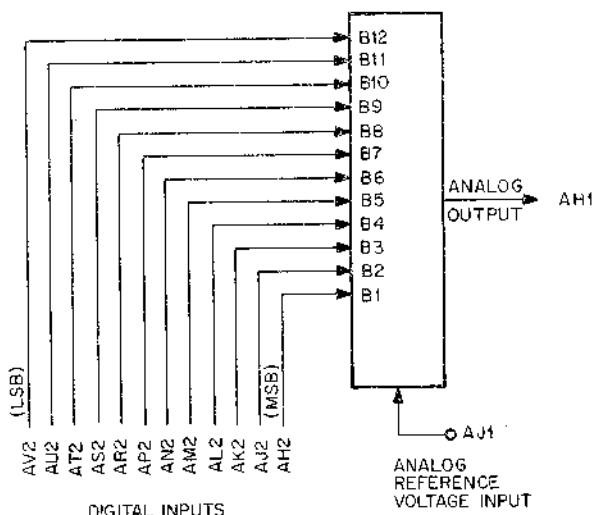
POWER REQUIREMENTS:

Reference Power:	--10.6 Volts, 60 mA
Amplifier Power:	±15 Volts, 25 mA (plus output loading)
Logic Power:	+ 5 Volts, 190 mA
	-15 Volts, 60 mA

Size: Standard, double height, double width FLIP CHIP module.

12 BIT MULTIPLYING DIGITAL TO ANALOG CONVERTER A660

A SERIES



	+15V	AD1, AD2
	-15V	AE1, AE2
ANALOG RETURN		AF1, AF2
	+5V	AA1, AA2, BA1, BA2
DIGITAL RETURN		AC2, BC2

The A660 is a precision 12 bit multiplying digital to analog converter whose output is the product of the external analog reference voltage supplied and digital code presented.

This D/A converter is DTL and TTL compatible, requires essentially zero warmup time, and has high output current drive capabilities. It also may be used in either unipolar or operations.

This unit may be used in applications where precision digital control must be exercised over an analog signal. It also may be used in systems requiring synchro to digital conversion, AC transducer digitization, or in hybrid computation.

A660—\$500

When operating in conjunction with an external DC reference source, the A660 may be used as a conventional D/A converter with the output polarity determined by the reference voltage polarity.

The A660 employs advance shielding techniques which allow proper operation under normal ambient electrostatic and electromagnetic conditions.

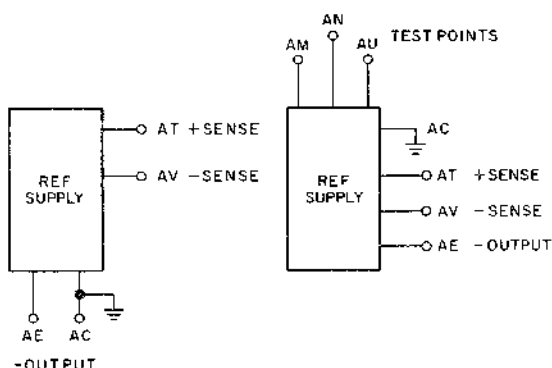
SPECIFICATIONS

Number of Bits:	12
Coding:	Binary—Absolute Value
Input Logic Levels:	High = Logic One ↑ TTL Load
Accuracy—(dc to 4 kHz)	$\pm 0.025\%$ FS, $\pm 0.01\%$ of output
Temp. Coefficient of Offset:	200 microvolts/ $^{\circ}$ C.
Temp. Coefficient of Range:	20 PPM/ $^{\circ}$ C.
Feedthrough (for 20 V. p-p sine wave; all bits off):	at 1 KHz: 1 mV RMS
Analog Reference Input Range:	± 10 v. Full Scale
Input Impedance:	10 k ohms
Frequency:	Down 0.02% at 20 kHz
Phase Shift:	$< 7^{\circ}$ at 20 kHz
Output Range:	± 10 V.
Output Current:	15 mA.
Short Circuit Protection:	Indefinitely to ground
Phase	Output in Phase with Ref.
Attenuation Range—Absolute Value	
	DIGITAL
	000 000 000 000
	111 111 111 111 Binary
	OUTPUT
	0.0000 Volts
	(0.9976) X (Input Ref.) Volts
Settling Time to Digital Change:	10ms.
Power Requirement:	+15V @ 14 mA. -15V @ 3 mA. +5V @ 20 mA.

Size: Standard, double height, double width FLIP CHIP module.

REFERENCE SUPPLIES
A702, A704
(DOUBLE HEIGHT)

A
SERIES



Module Type	Output	Current	Temperature Coefficient	Regulation	Peak Peak to Ripple
A702	-10V	±60 mA	1mV/°C	30 mV, no load to full load	10 mV
A704	-10 v	-90 to +40 mA	1 mV/8hrs 1 mV/15° to 35°C 4 mV/0° to 50°C	0.1 mV, no load to full load	0.1 mV

Module Type	Adjustment Resolution	Input Power	Use	Output Impedance
A702	5 mV	-15 v/100 mA +10 v (B)/10 mA.	Load with 500μF at load. May also be preloaded if desired	0.5 ohms
A704	0.01 mV	-15 ±2 V/250 mA	See below for sensing and preloading	0.0025 ohms

Remote Sensing: The input to the regulating circuits of the A704 is connected at sense terminals AT (+) and AV (-). Connection from these points to the load voltage at the most critical location provides maximum regulation at a selected point in a distributed or remote load. When the sense terminals are connected to the load at a relatively distant location, a capacitor of approximately 100 μF should be connected across the load at the sensing point.

A702—\$58
A704—\$175

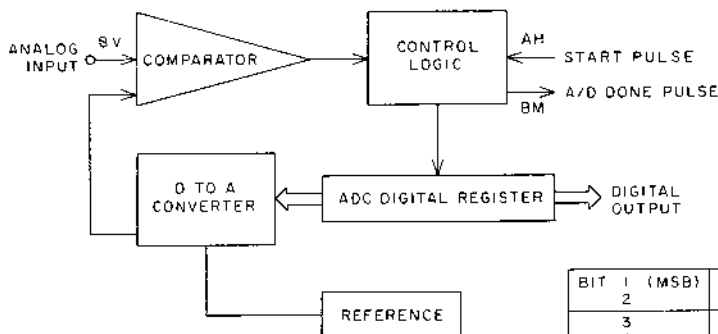
Preloading: The supplies may be preloaded to ground or $-15V$ to change the amount of current available in either direction. For driving DEC Digital-Analog Converter modules, -125 mA maximum can be obtained by connecting a $270\Omega \pm 5\%$ 1 watt resistor from the $-10v$ pin AE reference output to pin ac ground (A704 only).

Wiring: Digital-analog and analog-digital converters perform best when module locations and wiring are optimized. All Digital-Analog Converter modules should be side-by-side. In an analog-digital converter, the comparator should be mounted next to the converter module for the bits of most significance. The reference supply modules should be mounted nearby, and if the A704 is used, its sense terminals should be wired to the most-significant-bits converter module. The high quality ground must be connected to the common ground only at pin ac of the reference supply module, and this point should also be the common ground for analog inputs to analog-digital converters. Do not mount A-series modules closer than necessary to power supply transformers or other sources of fluctuating electric or magnetic fields.

Size: Standard, double height, single width FLIP CHIP module.

10 BIT A/D CONVERTER A811

A SERIES



A801 10-BIT ANALOG-TO-DIGITAL CONVERTER

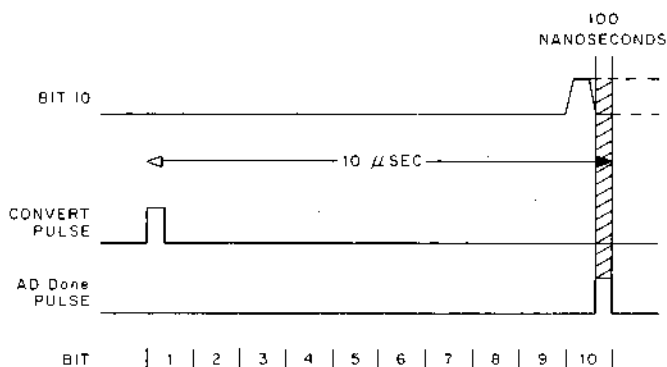
BIT 1 (MSB)	AE
2	AD
3	AN
4	AM
5	BL
6	BR
7	BK
8	BP
9	BS
10 (LSB)	BT

A811 10-BIT ANALOG-TO-DIGITAL CONVERTER

The A-811 is a complete, 10-bit successive approximation, analog to digital converter with a built in reference supply. Conversion is initiated by raising the Convert input to logic 1 (+4 volts). The digital result is available at the output within 10 microseconds. An A/D Done Pulse is generated when the result is valid. The A-811 uses monolithic integrated circuits for control logic, output register, and comparator.

The A811 requires 2 vertical connectors and the top section (connector A) requires 2 connector widths.

A811—\$350



SPECIFICATIONS:

	Max.	Min.
Convert Pulse Input:		
Input loading	10 TTL unit load	
Pulse Width	500 nsec	100 nsec
Pulse Rise Time	250 nsec	—
A/D Done Pulse Output:		
Pulse Width	300 nsec	100 nsec
Digital Output:		
Logical "0"	+0.4V	0V
Logical "1"	+3.6V	+2.4V
Output Current "0"	16 mA	
Output Current "1"	-0.4 mA	
Input:		
Input Voltage	0 to +10V	
Input Impedance	1000 ohms	
Resolution:	10 bits	
Accuracy:	0.1% of full scale	
Temperature:		
Coefficient:	0.5 mV/°C	
Operating Temperature:	0°C to 50°C	
Conversion Rate:	100 kHz (max)	
Output Format:	Parallel Binary Uni-polar	
+15 Volts ±1%	20 mA (pin BU)	
-15 Volts ±1%	160 mA (pin AV)	
+ 5 Volts ±1%	300 mA (pin AA)	

Size: Standard, double height, single double FLIP CHIP module.

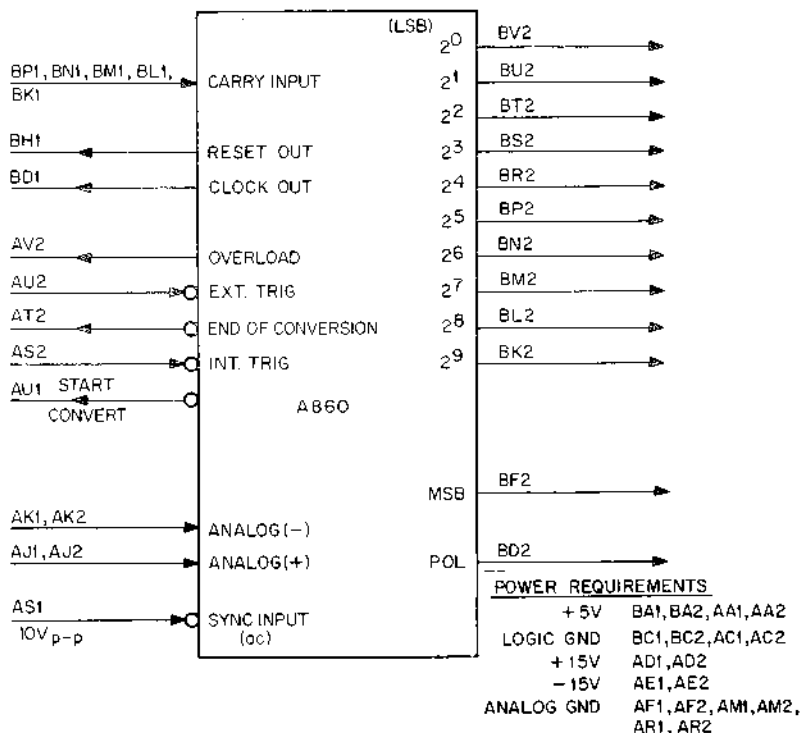
Analog Ground (pin BN)

Options:

The input impedance of the A/D converter can be raised to greater than 100 megohms by adding an input amplifier module. A sample and hold amplifier module may also be included. The impedance of the converter with sample and hold is 10,000 ohms. Both options may be included simultaneously if high impedance and narrow aperture are both required.

12 BIT INDUSTRIAL CONVERTER A860

A SERIES



The A860 is a 12 bit industrial converter employing dual slope integrating techniques whereby an analog signal is converted into 12 bits (11 bits + sign) of digital information in 9 milliseconds.

This unit may be used in industrial systems where sensing of an analog signal is essential in the control of a digital system.

The A860 may be used in application where the output of analytical instruments, strain gauges, and resistance bridges must be converted into digital form. Other uses of this module are industrial and machine tool control and conversion of instrumentation to digital displays. Because of its bit rate (1200—3600 BPS), the A860 may also be used to transmit data over telephone lines.

The A860 is both DTL and TTL compatible and may be used with standard K and M Series modules, as well as DEC's A Series multiplexers and sample and hold.

A860—\$395

The A860 has been engineered and designed using advance shielding techniques which allow proper operation under normal ambient electrostatic and electromagnetic conditions.

SPECIFICATIONS

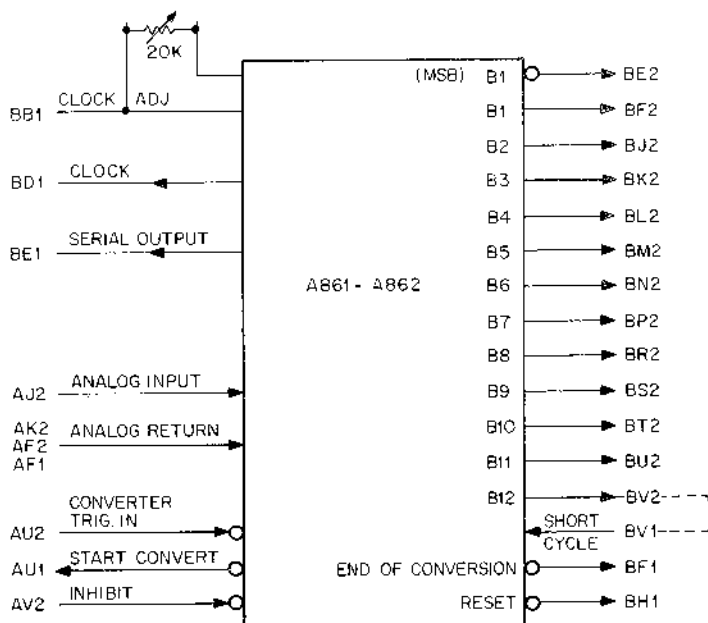
Technique:	Dual Slope Integration
Input Voltage Range:	+2 volt
Coding:	Sign bit + 11 magnitude bits
Accuracy at 23° C.:	±0.05% of input voltage +1 millivolt
Conversion Time:	9 milliseconds
Sample Aperture (part of conv. time):	3 milliseconds
Input Type:	Differential
Input Impedance:	> 1000 meg ohms
Common Mode Voltage: [⊘]	0.25 V max.
Common Mode Rejection:	> 70dB at 60 Hz
Control Inputs	
Internal Trigger:	Internal oscillator provided for autonomous operation of converter; can be enabled by grounding internal trigger line.
External Trigger:	Triggered by leading (negative-going voltage) edge 1 TTL load. Internal trigger must be disabled by hard wire to +5volts.
Digital Outputs—	
Data (11 lines):	Parallel data available after end of conversion. Logic one is high; 8 TTL loads.
End of Conversion (Busy Status):	Output logic one during conversion. High to low transition indicates end of conversion.
Carry Input:	Input to control flip flop that determines word length of converter. For 11 bits + sign, connect carry input (BK1) to 2 ⁹ out (BK2).
Overload:	Output logic one when analog exceeds full scale
Power Requirements:	-15V ± 0.3% at 20 mA +5V at 150 mA
Size:	Standard, double height, double width FLIP CHIP module.

[⊘] Note: Unit normally supplied with analog minus input connected to analog return through R6 (r). For differential inputs remove R6.

HIGH SPEED 12 BIT A/D CONVERTERS

A861 A862

A SERIES



POWER REQUIREMENTS

+5V	BA2, AA2, BA1, AA1
LOGIC GROUND	BC2, AC2, BC1, AC1
-15V	AE1, AE2
+15V	AD1, AD2
ANALOG RETURN	AK2, AF2, AF1

The A861 and A862 are high speed analog/digital converters that provide adjustment-free 12 bit accuracy at the specified temperature range.

The A861 is a unipolar converter with an input range of 0 to +10 volts and a straight binary output, whereas the A862 is a bipolar converter whose input is in the -10 volt range with an output that is coded offset binary or 2's complement.

A861—\$595
A862—\$595

SPECIFICATION

A861 (UNIPOLAR)

Technique:
Resolution:
Accuracy vs. speed @ 23°C:

Successive Approximation

12 Bits

- ± 0.01% of FS. @ 48 μ sec conv.
- ± 0.015% of FS. @ 24 μ sec conv.
- ± 0.05% of FS. @ 12 μ sec conv.

Reference:

Internal +5V and +10V supplies;
 adjustable

Code:

Straight binary

Temp. Coeff. of Offset:

± 0.001% of FS/°C

Temp. Coeff. of Gain:

(12 ppm/°C) X Input Voltage Applied

Signal Input Load:

2.5K ohms returned to +5 volts

Input Range:

0 to +10V

Data Output-Parallel:

True side of all bits

7 TTL unit loads.

Clock Adjustment (Multi-Turn Pot):

Variable from 1.2 to 48 microsecond
 conversion time

End of Conversion Output:

Goes High During Conversion;

Returns to low state @ at end of conversion

8 TTL LOADS

Serial Data (available during conversion):

NRZ code available

(Binary) 8 TTL loads

Converter Trigger:

Triggered on the leading

(negative-going voltage) edge,

1 TTL load

Inhibit Trigger:

Logic zero inhibits

Power Requirements:

+ 15V @ 55 mA.

- 15V @ 12 mA.

+ 5V @ 420 mA.

Size: Standard, double height, Double width FLIP CHIP module.

A862 (BIPOLAR)

Successive Approximation

12 Bits

- ± 0.01% of FS. @ 48 μ sec conv.
- ± 0.015% of FS. @ 24 μ sec conv.
- ± 0.05% of FS. @ 12 μ sec conv.

Internal +5V and +10V supplies;
 adjustable

OFFSET Binary or 2's complement

.001% of FS/°C

(12 ppm/°C) X Input Voltage Applied

5000 ohms returned to +5 volts

--10V to +10V.

True side or All Bits

plus false side of MSB

7 TTL unit loads.

Variable from 1.2 to 48 microsecond
 conversion time

Goes High During Conversion;

Returns to low state @ at end of conversion

8 TTL LOADS

NRZ code available

(offset binary)

8 TTL loads

Triggered on the leading

(negative-going voltage) edge,

1 TTL load

Logic zero inhibits

1 TTL load

+ 15V @ 55 mA.

- 15V @ 12 mA.

+ 5V @ 420 mA.

One double height

double width module.

Both of these modules employ the successive approximation techniques and include a self-contained clock and trigger circuitry that will allow adjustment of the conversion time to a level from 12 microseconds to 48 microseconds.

The A861 and A862 are DTL and TTL compatible and may be used with standard M and K Series modules, as well as standard DEC hardware for system configuration.

Both A/D converters contain internal reference supplies that are adjustable. In packaging the A861 and A862, advance shielding techniques have been employed to allow stable operation under ambient electrostatic and electromagnetic conditions. To minimize potential ground loop problems, separate ground returns are brought to:

- a. Digital power supply return pin,
- b. Analog power supply return pin,
- c. Analog signal return pin.

Both of these modules are useful in systems demanding high integral accuracy and long term reliability, such as computer linkage, biomedical data transmission, process control, and conversion of instrumentation data.

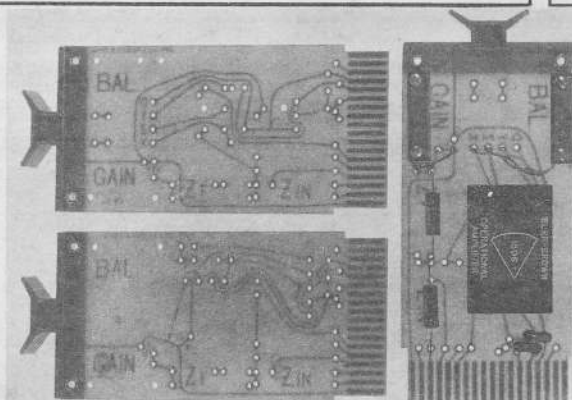
Range and offset adjustments are provided on the module.

2ⁿ and Resolution

2 ⁿ	# OF BITS	RESOLUTION	
	n	(%)	PPM
1	0	100.0	1,000,000
2	1	50.0	500,00
4	2	25.0	250,000
8	3	12.5	125,000
16	4	6.25	62,500
32	5	3.125	31,250
64	6	1.563	15,625
128	7	0.781	7,812
256	8	0.391	3,906
512	9	0.195	1,953
1 024	10	0.0977	977
2 048	11	0.0488	488
4 096	12	0.0244	244
8 192	13	0.0122	122
16 384	14	0.00610	61
32 768	15	0.00305	31
65 536	16	0.00153	15
131 072	17	0.000763	8

AMPLIFIER BOARDS A990, A992

A SERIES



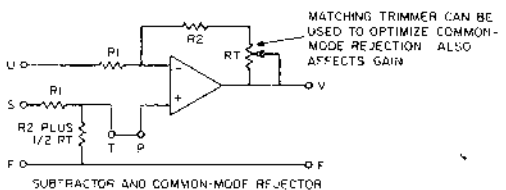
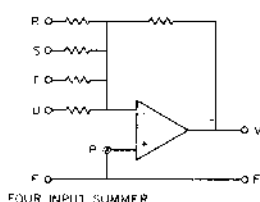
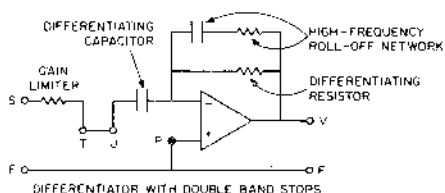
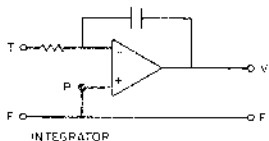
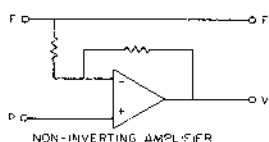
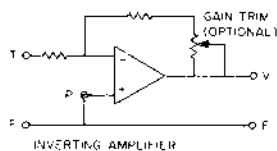
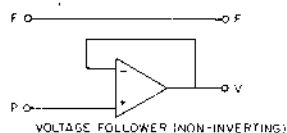
Many types of commercially available operational amplifiers can be mounted in the holes provided on these predrilled etched boards. Mounting holes and printed wires provide for balance trim, gain trim, and feedback networks required to build such common operational devices as voltage followers, inverting or non-inverting amplifiers, integrators, differentiators, summers and subtractors. Most amplifiers listed in the table below require $\pm 15V$ regulated supplies which are readily available from the amplifier manufacturers. Notable exceptions are Analog Devices' Models 101, 103, and 104 which may be used with standard DEC $+10V$, $-15V$ supplies at some sacrifice in voltage range ($+5$, $-10V$) and noise.

Power: Positive at pin D, negative at pin E, common at pin F for all types. Space is provided for mounting bypass capacitors used with some high frequency amplifiers.

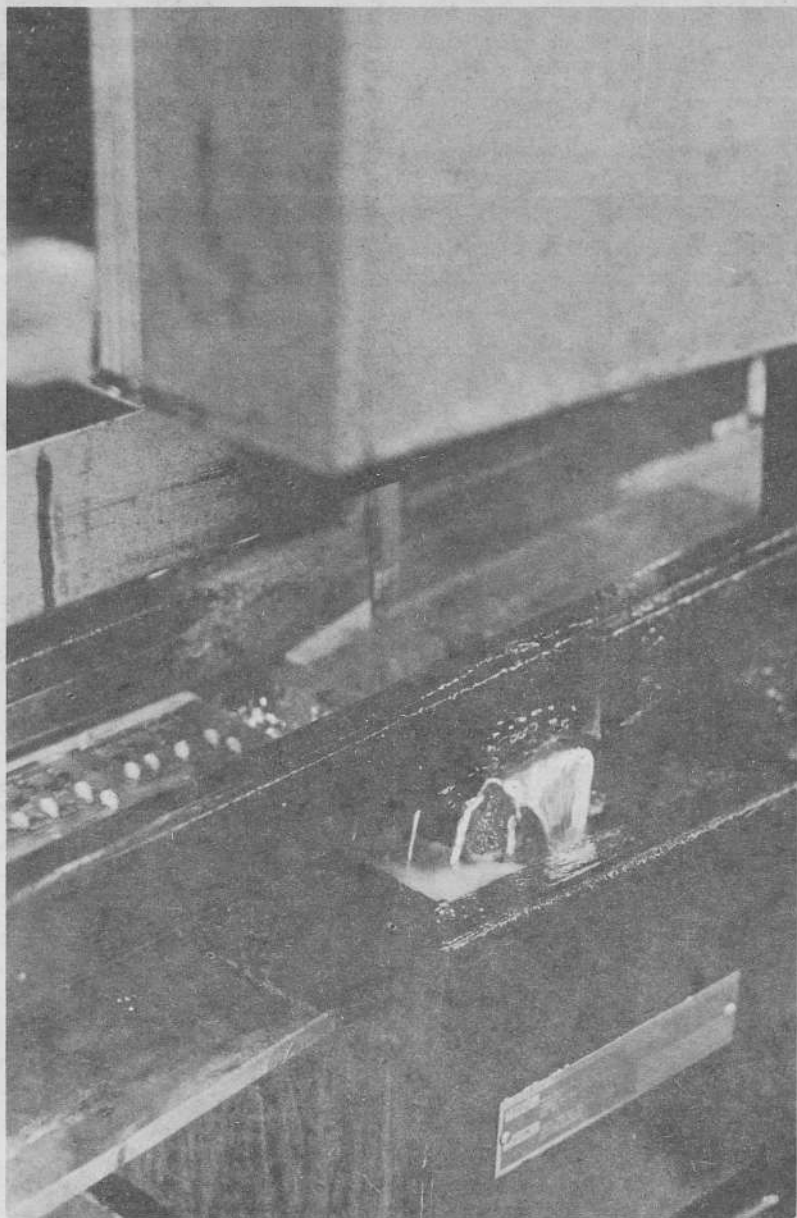
Trimming: Mounting holes on 1" centers at the handle end accept wirewound potentiometers for balance and feedback (gain) trimming. Gain rheostat may be connected in series with feedback components to allow precise adjustment of gain using inexpensive 1% feedback resistors. Board is etched to allow for use without gain trimming, and one pointed conductor must be cut at caret marks to put a rheostat in the circuit. Gain rheostat stray capacitance to ground is driven by amplifier output.

Amplifier Supplier	Types accepted by A990	Types accepted by A992 (boosters too)
Analog Devices	101, 102, 104, etc.	103, 106, 107, etc.
Burr-Brown*	1500-46, 1500-68	—
Data Device Corp.	—	most types, except boosters
Nexus	Case K or Case L	Case Q
Philbrick	—	Case PP
Union Carbide	—	most types
Zeltex	—	Case A

⊗ Except Burr-Brown differential output and chopper stabilized types: Perforated board W994 or other blank module may be used to mount non-standard configurations.



A990 — \$4
A992 — \$4



This flow-soldering machine solders all component leads to the board and makes all solder runs in one fast, exceedingly reliable, operation.

Lab Series



COMPUTER LAB

LAB
SERIES

The COMPUTER LAB is a high performance low-cost digital logic trainer. It uses the same monolithic integrated transistor-transistor logic circuitry used in DIGITAL's latest computers.

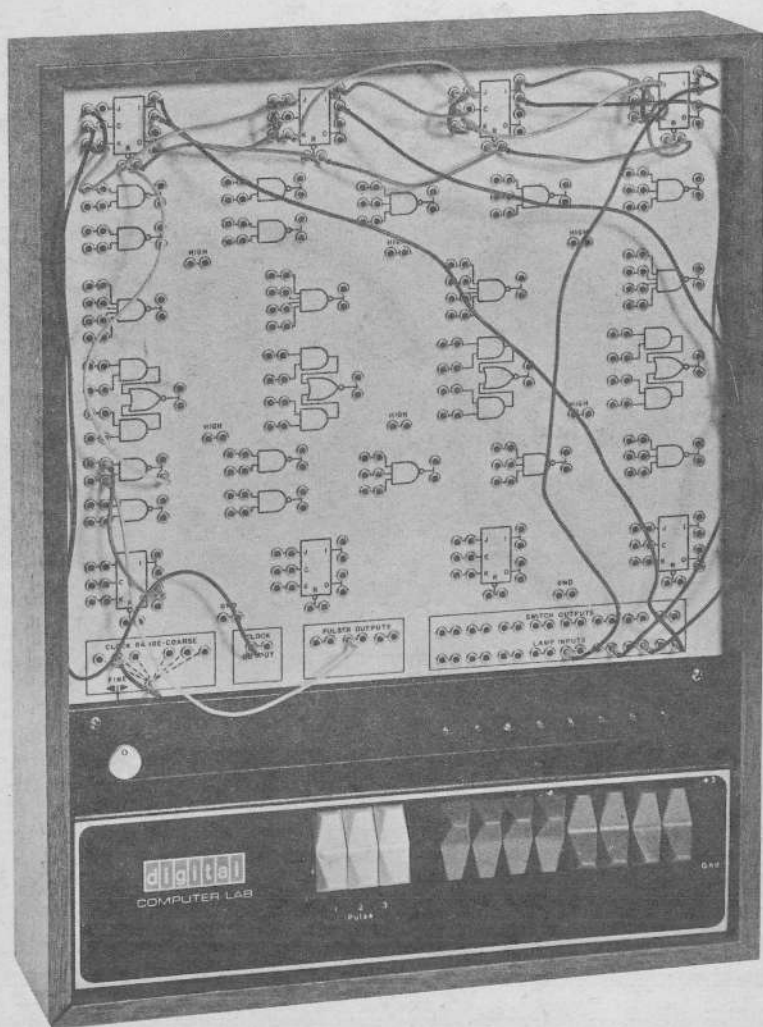
The digital logic fundamentals presented by the COMPUTER LAB can foster a basic understanding of computer technology for the computer career oriented user, or for a user applying computers for the first time. The COMPUTER LAB will also help the math-oriented user understand "new math" concepts, as computer logic operates with binary numbers according to Boolean algebraic laws.

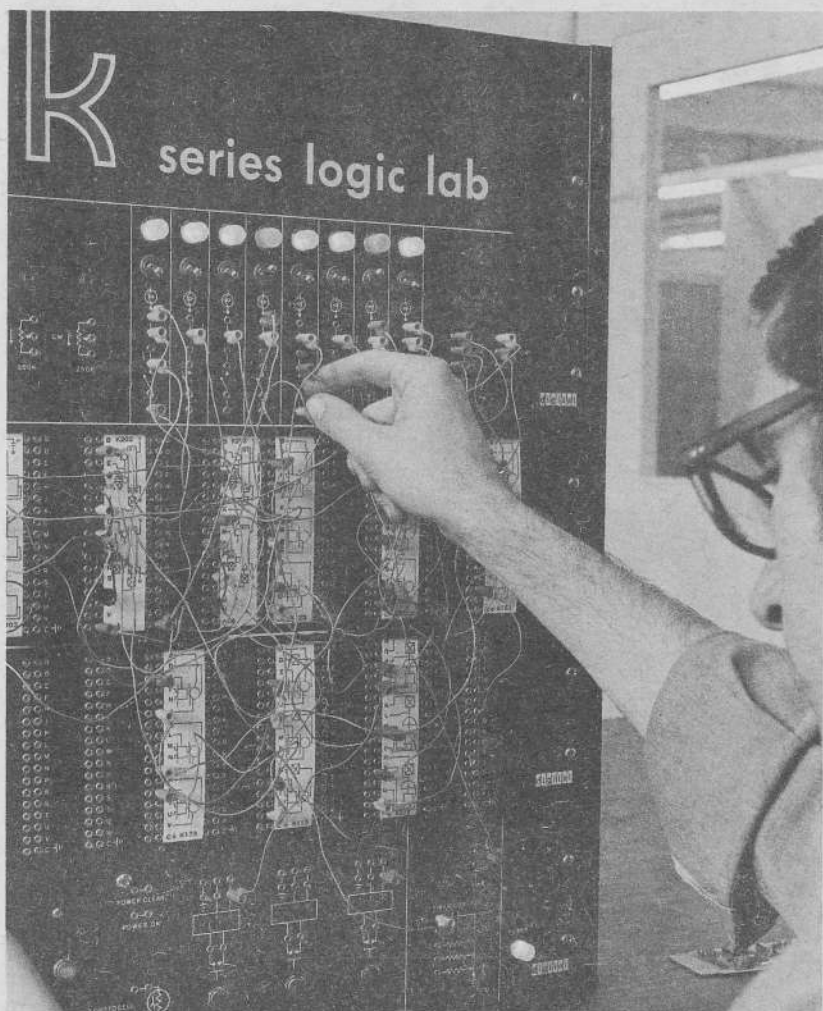
Wiring is easy because of the standard logic symbology used on the front panel and the color coded Patchcords which are easily inserted and removed. An improper circuit will not damage the COMPUTER LAB. The faulty circuit merely "waits" for correction.

Features:

- Transistor—Transistor logic circuitry as used in DIGITAL's PDP computers
- Teaches modern computer logic
- Easy to use: MIL-STD 806 logic symbology on front panel
- Portable: Dimensions of $12\frac{1}{2}$ " x 17" x $3\frac{1}{4}$ ", weighing only 11 lbs.
- Comprehensive Workbook provides:
 - Ten detailed chapters
 - More than 30 experiments
 - Over 200 hours of laboratory study
 - Dozens of tables and diagrams
 - An extensive appendix of supplementary information
- Instructor's Guide with answers, additional text, extra problems, course plans, at only \$5.00
- Low cost: COMPUTER LAB, Workbook and Patchcord set, ready to use \$445.00

H 500 — \$445





K-SERIES LOGIC LAB

LAB
SERIES

INTRODUCTION

The K Series Logic Laboratory is designed for use with K Series Modules. It is a device for building prototype systems for experimentation and proof of logic design as well as an effective tool for learning solid state control logic.

It is excellent for training users in digital logic techniques by enabling an individual to construct logical networks, with a "hands on approach" to learning control systems for Industrial Applications.

The K Series Logic Lab is a completely self contained system consisting of a power supply, photo cell, pulse generator, switch controls, indicators, mounting hardware and a recommended basic complement of logic modules necessary to construct a working system. The system is expandable and can accommodate additional K901 patchboard panels for mounting additional logic modules.

EDUCATION AND TRAINING

As a training device the K Series Logic Lab offers the engineer, technician, and user a step by step approach to building an understanding of various digital logic functions, such as, AND, OR and the operations of NAND and NOR etc. The user has the option of using NEMA or MIL spec symbology when making logic connections. Symbology cards on basic logic modules for use with the K901 patchboard panel are printed with NEMA on one side and MIL SPEC 806 on the reverse side.

BREADBOARDING AND TESTING

The logic laboratory power supply is capable of supplying 5V-DC for about 100 modules. There is no restriction on the size of a system which can be implemented, since additional patchboard panels can be ordered and "K" Logic Laboratories interconnected directly.

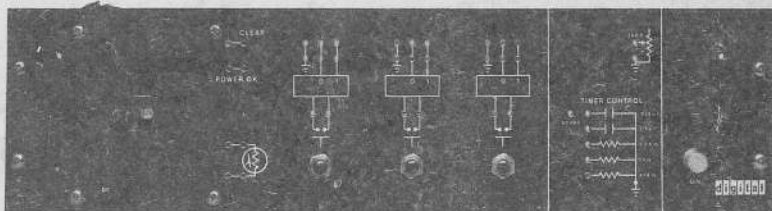
There is no substitute for actually building the system and verifying the logic.

Some common uses of the Logic Laboratory are listed below. Many of these are described in detail in the Control Handbook and part III in the 1969 Positive Edition Logic Handbook.

Timer Sequencers	Serial Adder
Shifter Sequencers	Stepping Motors Control
Parallel Counters	Pulse Generator
Pulse Rate Multiplier	Annunciator

CONTROL PANEL — POWER SUPPLY K900

LAB
SERIES



The K900 is a combination power supply and input control panel. The input devices include a photocell, three push button pulsers and timing components for a K303 clock mounted in a K901 panel. Clock timing components are provided for frequency steps in ranges of 2Hz to 60Hz and 200Hz to 6K Hz. Wiring diagrams for properly connecting the clock are shown in the logic and control handbooks (reference K303). The power supply can drive approximately ten type K901 panels of K series flip chip™ logic. Pulsers consist of a K501 schmitt trigger with a K581 switch filter. Power is supplied by K731, K743 and K732 power supply modules.

Electrical Characteristics

Input voltage: Power supply: 115V 50-60 cps

Output voltage: +5 VDC $\pm 10\%$

Output current: 3 amp

Mechanical Characteristics

Panel width: 19"

Panel height: 5 $\frac{1}{16}$ "

Depth: 12"

Finish: black

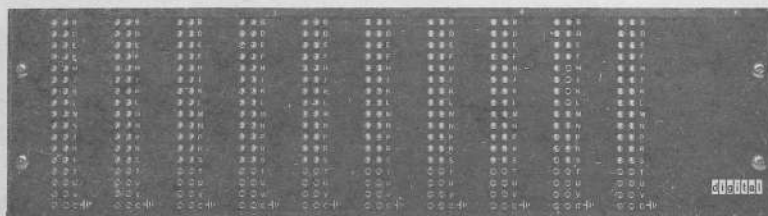
Power Unit connection: 18/3 AC power cord

Power Output connection: Hayman Tab terminals which fit AMP "Faston" receptacle series 250, part 41774 or Type 914 Power Jumpers.

K900 — \$185

**PATCH BOARD PANEL
K901, 911**

**LAB
SERIES**



K901 PATCHCORD MOUNTING PANEL

This panel provides up to ten FLIP CHIP modules with power and patch connections. Space between patching sockets allows insertion of logic diagrams. Logic diagrams are printed on all FLIP CHIP module data sheets. More permanent plastic diagrams are available for those modules listed.

PANEL WIDTH: 19 in.

PANEL HEIGHT: 5 $\frac{3}{8}$ in.

DEPTH: 6 $\frac{1}{2}$ in. with FLIP CHIP modules inserted

FINISH: Black

POWER INPUT CONNECTIONS: Tabs which fit AMP "Faston" receptacle series 250, part 41774.

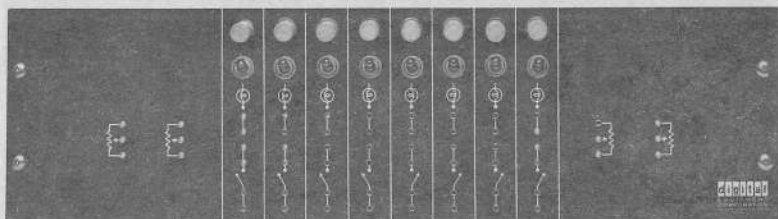
911 PATCHCORDS

DEC Type 911 Banana-Jack Patchcords are supplied in color-coded lengths of 2 in. (brown), 4 in. (red), 8 in. (orange), 16 in. (yellow), 32 in. (green), and 64 in. (blue). Patchcords may be stacked to permit multiple connections at any circuit point on the graphic panels of the DEC K901 Mounting Panel. The cords are supplied in snap-lid plastic boxes of ten for handy storage.

K901 — \$125
911 — \$9/pkg. of 10

INDICATOR SWITCH PANEL K902

LAB
SERIES



The H902 Panel provides facilities for control and observation of the Logic Laboratory. It contains eight indicator lights and a lamp driver module, eight toggle switches and four potentiometers. Connections to these devices are made with Type 911 Stacking Banana-Jack Patchcords.

INDICATORS: Indicators inputs accepts signals of +5V and ground. An open circuit input will light the indicator. If the input is returned to ground, the indicator will not light. The load is 1 mA.

TOGGLE SWITCHES: The toggle switches are single pole, single throw with a logic diagram to show the open and closed positions.

POTENTIOMETERS: The potentiometers are 250,000 ohms. They may be used to control the frequency of delay one-shots or clock circuits in the K901 Mounting Panel.

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19 in.

PANEL HEIGHT: $5\frac{3}{16}$ in.

DEPTH: $6\frac{1}{2}$ in.

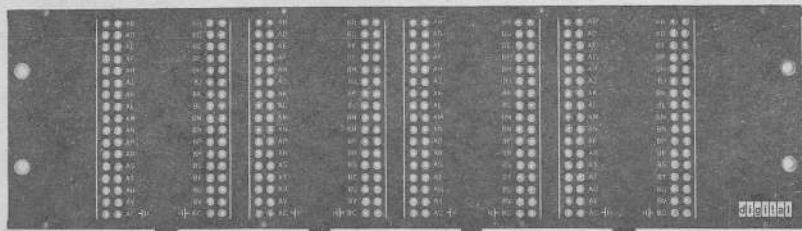
FINISH: Black

POWER INPUT CONNECTIONS: Tabs which fit AMP "Faston" receptacle series 250, part 41774.

K902 — \$145

**PATCH PANEL BOARD
K903**

**LAB
SERIES**



This patch panel provides logic power and patch connections for four double-height or eight single height FLIP-CHIP[®] modules. The panel was designed particularly for K Series double height modules including the interfacing modules (K5xx and K6xx). Two K903 panels cannot however be mounted together on a mounting rack due to socket overhang at the bottom of each K903 panel. Space between patching sockets allows insertion of logic diagrams. Logic diagrams are printed on all FLIP-CHIP[®] module data sheets. More permanent plastic diagrams are available for those modules listed.

PANEL WIDTH: 19 in.

PANEL HEIGHT: 5 $\frac{3}{16}$ in.

DEPTH: 6 $\frac{1}{2}$ in. with FLIP-CHIP[®] modules inserted.

FINISH: Black

POWER INPUT CONNECTIONS: Tabs which fit
AMP "Faston" receptacle series 250, part 41774

K903—\$155

MISCELLANEOUS ACCESSORIES
4913, 914

LAB
SERIES

4913 MOUNTING RACK

The 4913 Mounting Rack provides support for a and up to four K901 Patchcord Mounting Panels, for a total of up to 40 FLIP CHIP modules ready to be patched together for experiments. It may also be used to mount general purpose mounting panels such as the K943. The power supply must be mounted at the bottom for stability.

Height: 26 $\frac{1}{4}$ in.

Threads for mounting panels: 10-32

914 POWER JUMPERS

For interconnections between power supplies, mounting panels, and logic lab panels, these jumpers use AMP "Faston" receptacles series 250. Specify 914-7 for interconnecting adjacent mounting panels, or 914-19 for other runs of up to 19 inches. 914-7 contains 10 jumpers; 914-19 contains 5.

4913K — \$25
914-7 — \$ 4
914-19 — \$ 4

BASIC EQUIPMENT LISTS

BASIC LOGIC LABORATORY

1-K901	Patchboard panel	125.00
1-K902	Indicator Switch Panel (complete with K683 module)	145.00
1-K900	Power Supply and Control Panel (complete with Power modules)	185.00
1 pair—4913	Mounting Rack	25.00

RECOMMENDED LOGIC MODULES AND PATCHCORDS FOR USE WITH THE LOGIC LABORATORY

	UNIT PRICE	TOTAL PRICE
4-K003 Expander	5.00	20.00
2-K012 Expander	8.00	16.00
3-K113 Gate	11.00	33.00
3-K123 Gate	12.00	36.00
2-K134 Inverter	13.00	26.00
1-K161 Decoder	25.00	25.00
1-K174 Comparator	24.00	24.00
1-K184 Rate Multiplier	25.00	25.00
2-K202 Flip-flop	27.00	54.00
1-K206 Flip-flop	20.00	20.00
2-K210 Counter	27.00	54.00
1-K220 Up-down Counter	55.00	55.00
1-K230 Shift Register	40.00	40.00
1-K303 Timer	27.00	27.00
1-K323 One shot delay	35.00	35.00
1-K376* Timer Control (0.1-3.0 sec)	15.00	15.00
1-K378* Timer Control (1.0-30 sec)	15.00	15.00
1-K373* Timer Control (20 Hz-600 Hz clock)	11.00	11.00
1-K522 Sensor Converter	25.00	25.00
4 pks. of 10 patchcords (911-2")	9.00	36.00
5 pks. of 10 patchcords (911-4")	9.00	45.00
2 pks. of 10 patchcords (911-16")	9.00	18.00
1 pkg. of 10 patchcords (911-16")	9.00	9.00
26 symbology cards	.25 ea.	6.50

Complete K-Series logic lab with workbook
and modules listed — H510 \$995.00

Asterisk* denotes symbology cards unavailable. Symbology cards for use with K901 patchboard panel. .25 ea., minimum purchase of \$5.00 applies.

IF ADDITIONAL K901 PATCHBOARDS ARE ORDERED:

1-911-4"	pkg. of 10 patchcords	9.00
1-911-8"	pkg. of 10 patchcords	9.00
1-911-16"	pkg. of 10 patchcords	9.00
1-911-32"	pkg. of 10 patchcords	9.00

K-SERIES INTERFACE MODULES

Recommended logic modules for input/output functions.

AC Input/Output

1-K578	120 VAC Input converter	80.00
1-K614	120 VAC Isolated AC switch	88.00

DC Input/Output

1-K580	Dry Contact Filter	28.00
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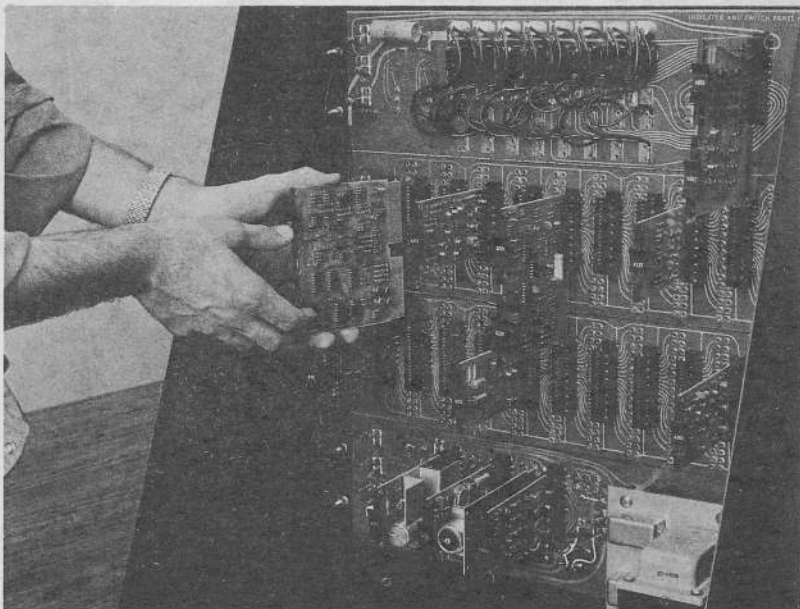
Listed below are a number of DC output drivers that may be used:

1-K644	DC output Driver	66.00
	or	
1-K656	DC output Driver	80.00
	or	
1-K658	DC output Driver	128.00

Each additional K series workbook 5.00

Note: only 3 out of 4 circuits are available when using above 3 modules with the K901 mounting panel.

Reference logic or control handbook for additional module information and selection.



A rear view of the K Series Logic Lab shows how modules are plugged into mounting panels.

M SERIES LOGIC LAB

LAB SERIES

Introduction

The M Series Logic Lab is a highly versatile unit that can be used successfully at all stages of digital logic design, from training, to experimentation, to systems design, to final system checkout. It can be used to build prototype logic systems or as a tool to test and design actual hardware. Educationally, it provides the designer with a flexible system for experimentation as well as a basic unit for learning the fundamentals of electronic circuitry and logic design.

The Logic Lab's exceptional training abilities stem mainly from the fact that the student can design and actually construct his logic networks directly on the unit. This provides valuable practical reinforcement of theoretical concepts.

The M Series Logic Lab is designed for use with any Series of DEC modules which uses +5 Volts for power.

The M Series Logic Lab is a completely self-contained system, consisting of a power supply, lights, switches, and two racks of connector blocks. The system is expandable and can accommodate an additional rack of connector blocks.

Education and Training

As a training device, the M Series Logic Lab offers the user an easy step-by-step way to gain an understanding of various logic functions, such as AND, OR, NAND, NOR, etc. Because this tool is not limited to any one technology, it can be used to study not only TFL but also DTL, ECTL, and other types of logic.

Breadboarding and Testing

The Logic Lab power supply can supply +5 V dc at 6.5 amps (max.). This supplies sufficient current for systems using all module slots.

The Logic Lab is an effective tool for bridging the gap between paper design and a fully tested, marketable product.

Console

The Console consists of a light and a switch panel. The light panel is made up of 80 lights arranged in four rows of 16 lamps and four rows of four lamps. The user can write designations on the panel adjacent to each lamp.

The switch panel has three groupings of switches—16 on/off-type switches, two on/off-type switches, and two pulser-type switches. This switch configuration provides highly versatile control.

Connector Racks

The M Series Logic Lab has two 19" racks of low-density H808 connector blocks. Each rack contains eight connector blocks and each connector block has four module slots; therefore, there are 32 module slots per rack for a total of 64 module slots in the standard M Series Logic Lab. One additional rack can be mounted increasing the available module slots to 96. Regardless of how many racks are used, four slots must be dedicated to receiving flex-print cables from the switch and light panels.

Power bussing of pins A2, C2, T1 is also available as a standard item on the rack of connector blocks.

MEMORY AUXILIARY DEVICE—H521 \$000
(THIS DEVICE CAN BE USED TO
INTERFACE MEMORY TO THE M-LAB)

CABLES

Switch Board (Switches are numbered from right to left)

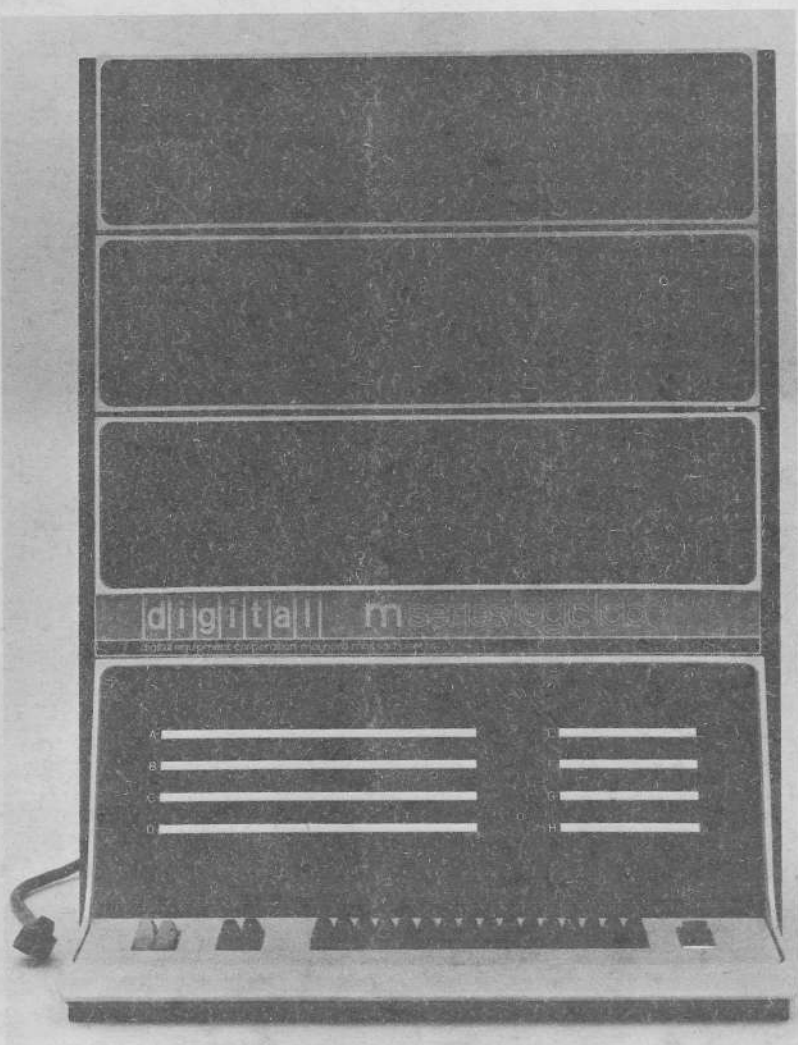
S0-Pin E1	S8-Pin R2	C1-Pin E2
S1-Pin D1	S9-Pin P2	C2-Pin F2
S2-Pin C1	S10-Pin N2	
S3-Pin B1	S11-Pin M2	P1-Pin A1
S4-Pin V2	S12-Pin L2	P2-Pin D2
S5-Pin U2	S13-Pin K2	
S6-Pin T2	S14-Pin J2	
S7-Pin S2	S15-Pin H2	

Light Board (Lights are numbered on the indicator panel)

A0-Pin CN1	B0-Pin CL1	C0-Pin CD1	D0-Pin CJ1
A1-Pin CP1	B1-Pin CM1	C1-Pin CH1	D1-Pin CF1
A2-Pin CR1	B2-Pin CS1	C2-Pin CK1	D2-Pin CE1
A3-Pin CP2	B3-Pin CD2	C3-Pin CU1	D3-Pin CC1
A4-Pin CV2	B4-Pin CJ2	C4-Pin CV1	D4-Pin CB1
A5-Pin CN2	B5-Pin CU2	C5-Pin CH2	D5-Pin CA1
A6-Pin CS2	B6-Pin CL2	C6-Pin BP2	D6-Pin CM2
A7-Pin CE2	B7-Pin CR2	C7-Pin BJ2	D7-Pin CT2
A8-Pin CK2	B8-Pin BV2	C8-Pin BU2	D8-Pin CF2
A9-Pin BF2	B9-Pin BM2	C9-Pin BK2	D9-Pin BN2
A10-Pin BS2	B10-Pin BL2	C10-Pin BD2	D10-Pin BH2
A11-Pin BE2	B11-Pin BR2	C11-Pin BA1	D11-Pin BT2
A12-Pin BP1	B12-Pin BK1	C12-Pin BE1	D12-Pin BD1
A13-Pin BL1	B13-Pin BF1	C13-Pin BN1	D13-Pin BC1
A14-Pin BJ1	B14-Pin BH1	C14-Pin BM1	D14-Pin BB1
A15-Pin BV1	B15-Pin BU1	C15-Pin BR1	D15-Pin BS1
E0-Pin AA1	F0-Pin AC1	G0-Pin AB1	H0-Pin AD1
E1-Pin AN1	F1-Pin AM1	G1-Pin AL1	H1-Pin AE1
E2-Pin AR1	F2-Pin AU1	G2-Pin AK1	H2-Pin AF1
E3-Pin AP1	F3-Pin AS1	G3-Pin AJ1	H3-Pin AH1

H520-A (240v./50Hz) ALSO AVAILABLE

M Series Logic Lab H520—\$995





Testing K Series modules

K Series Control Logic Modules

K Series modules were designed to be used in control applications. Their unique characteristics of slow speed (100 KHz maximum) and high noise immunity make them ideal for many industrial applications. Some K Series modules are compatible with the M Series line previously described. In the following pages a brief summary will be made of each K Series module.

Further information on all K Series modules may be obtained from Digital's CONTROL HANDBOOK

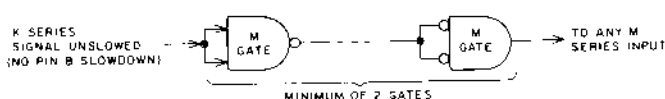
COMBINING K WITH M-SERIES MODULES

There are several types of applications in which a combination of M and K Series modules is better than either one alone, such as interfacing a K Series system to a computer or interfacing an M Series system to electro-mechanical devices. Here are the things to consider and recommended designs for both pulses and levels in each direction.

TIMING

Timing considerations are important, but unfortunately are not reducible to simple rules: as in any other logic design task, interfacing K with M Series modules requires adherence to all timing constraints of the output device, the input device, and the logic loops (if any) as a whole. As a minimum, M Series signal driving K Series circuits must last long enough (at least 4 microseconds even if no propagation within the K Series is required) so that the K Series will not reject it as if it were noise; and as a minimum, K Series signals driving M Series circuits must be received by M Series inputs that will not be confused by ultra-slow risetimes.

K TO M SERIES LEVELS



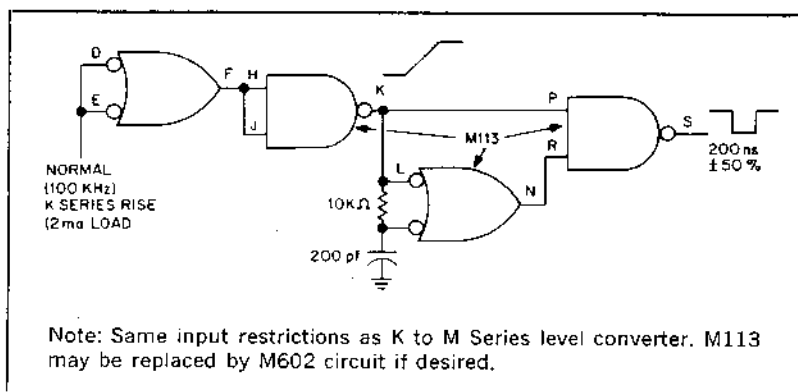
K TO M-SERIES LEVEL CONVERTER

Note: Total lead length connected to input of first M Series gate should be less than 6 inches, to minimize any tendency toward oscillation while active region is being traversed. Do not use slowed K Series levels. If noise still gets through, a .001 capacitor from M Series input pin to ground can be added.

M TO K SERIES LEVELS

1. Diode gate inputs (K113, K123, etc.) and drivers with flexprint cables (K604, K644, K671) may be paralleled freely with M Series inputs.
2. M Series outputs should not be paralleled (wired AND) with K Series outputs.
3. K303 inputs, K220, K230 readin gate inputs, and K135 and K161 inhibit inputs require the full 5 Volt K Series swing, and normally should not be paralleled with M Series inputs. Also in this category are clear inputs to K202, K210, K220, and K230. M Series gate outputs will rise all the way to +5V if no M Series inputs are paralleled with these points, except the K161 inhibit input.
4. Other K Series inputs generally may be driven directly, but in some cases heavy capacitive loading will slow the transitions.

K TO M SERIES PULSES



M TO K SERIES PULSES

Use a type M302 delay multivibrator set for at least 5 μ sec (capacitor pins H1-L2 or S1-S2). Observe same restrictions on K Series inputs to be driven as listed above under "M to K Series levels."

Loading

Driving M from K Series modules, each risetime-insensitive input should be regarded as a 2ma K Series load, and K Series inputs may be freely mixed with M Series inputs up to the total K Series fanout of 15 milliamperes. M Series inputs could be regarded as 1.6 mA each if more complicated rules and qualifications concerning use with K303 timers and reduction in low-output noise rejection were established, but the 2 mA equivalence is simpler and safer.

Driving K from M Series, each milliampere of K Series load should be regarded as one M Series unit load.

For computer interfacing and other M-Series applications where K Series is used as a buffer to keep noise in the external environment from reaching high-speed logic, beware of long wires between the M and K Series portions. For full noise protection, all signal leads penetrating the noisy environment normally must have K-series modules at both ends. EIA converters (K596, K696) or lamp drivers may offer a helpful increase in signal amplitude or decrease in allowable line impedance for long data links. In any case, use all the slowdown connections or slant capacitors that the required data rates permit.

GATE EXPANDERS
K003, K012, K026, K028

K
SERIES

K003 — AND Expander: three triple input expanders which may be connected to the AND expansion node of any K Series module.

AND/OR Expander's: three dual input AND gates which may be connected to the OR expansion node of any K Series module.

K012 — OR Expander: three four input OR expanders which may be connected to the OR expansion node of any K Series module.

K026 — AND/OR Expander: three sets of dual input AND gates which are OR'ed into an OR expander gate. The resulting OR'ed output may then be connected to the OR expansion node of any K Series module.

K028 — AND/OR Expander: eight dual input AND gates which are OR'ed into an OR expander gate. The resulting OR'ed output may then be connected to the OR expansion node of any K Series module.

K003 — \$5
K012 — \$8
K026 — \$8
K028 — \$8

K080 — Connector cable: Single height module on which can be mounted a 19 conductor cable. Cable clamp included.

K080—\$3

LOGIC GATES
K112, K113, K122, K123, K124

K
SERIES

K112 — Inverting Gate: three dual input gates which perform the NAND function. Both AND and OR expansion connections are available. Maximum speed 1 kHz with provisions on one circuit for slowdown to 50 Hz.

K113 — Inverting Gate: three dual input gates which perform the NAND function. Both AND and OR expansion connections are available. Maximum speed 100 kHz with provisions on one circuit for slowdown to 5 kHz.

K122 — Noninverting Gate: three dual input gates which perform the AND function. AND and OR expansion nodes provided. Maximum speed of 1 kHz with provisions on one circuit for slowdown to 50 Hz.

K123 — Noninverting Gate: three dual input gates which perform the AND function. AND and OR expansion nodes are provided. Maximum speed of 100 kHz with provisions on one circuit for slowdown to 5 kHz.

K124 — AND/OR Gate: two circuits where two dual input AND gates are ORed together. This module provides a convenient method of implementing exclusive OR's, control flip-flops, and two term boolean "OR" equations. It is not expandable.

K112—\$12

K113—\$11

K122—\$13

K123—\$12

K124—\$14

INVERTERS
K134, K135, K138

K
SERIES

K134 — Inverting Gate: four inverting gates with a common enable input. These gates may only be AND expanded.

K135 — Inverting Gate: four inverting gates with a common enable input. These gates may only be OR expanded.

K138 — Inverting Gate: eight inverter circuits each having a single input and output.

K134—\$13

K135—\$13

K138—\$24

K161 — Binary to Octal Decoder: Takes a three bit binary number and produces one out of eight lines high.

K161 — \$25

K171 — Equality Comparator: four bit equality comparator whose expansion output is high if the two numbers being compared are equal.

K171—\$13

K174 — Digital Comparator: This module makes a numerical comparison between two binary numbers and tells which of the two quantities is larger.

K174 — \$24

K184 — Rate Multiplier: Module emits a pulse train at an average rate equal to the product of counter and binary fraction inputs.

K184 — \$25

FLIP-FLOPS
K201, K202, K206

K
SERIES

K201 — Flip-Flop: dual set-reset flip-flops for low speed (1 KHz maximum) operation in highly noisy surroundings.

K202 — Flip-Flop: two D type flip-flops whose outputs go to the state of their data inputs when their clock inputs fall from high to low.

K206 — Flip-Flop Register: four set-reset flip-flops with a common read-in enable and direct clear input.

K201 — \$39

K202 — \$27

K206 — \$20

COUNTERS
K210, K211, K220, K230, K271, K273,
K281, K282

K
SERIES

K210 — Counter: a four bit binary or BCD up counter. With expansion gates, it can be connected to count anywhere from 2 to 16.

K211 — Programmable Divider: a binary counter which can be wired to produce a high to low output transition after any number of input cycles from 2 to 16.

K220 — UP/DOWN Counter: a binary or BCD UP/DOWN Counter which can be parallel loaded.

K230 — Shift Register: a four bit shift register which can be parallel loaded.

K265 — Reed Relay Driver: Special module which provides input buffers and mounting capabilities for 5 customer mounted reed relays.

K265 — \$25

K271 — Set-Reset Retentive Memory: a magnetically latched mercury wetted contact relay flip-flop which can follow important data in a system and retain that data should a power failure occur.

K273 — Retentive Memory: three magnetically latched mercury wetted contact relays which can follow 3 bits of information, and retain that data should a power failure occur.

K281 — Fixed Memory: diode matrix which can code eight four-bit words.

K282 — Diode Memory: diode matrix which can code eight, 16 bit words.

K210 — \$27

K211 — \$20

K220 — \$55

K230 — \$40

K271 — \$40

K273 — \$85

K281 — \$10

K282 — \$40

TIMERS

**K301, K303, K323, K333, K371,
K373, K374, K375, K376, K378**

**K
SERIES**

K301 — Basic Timer: timer circuit which can provide delays ranging from 10 microseconds to 30 seconds. It may be used as an OFF delay, or ONE shot.

K303 — Timer: three delay circuits which provide delays from 10 microseconds to 30 seconds. Delay circuits may be connected to form clocks, with frequency ranges between 2Hz and 6KHz.

K323 — One Shot: three one shot circuits which convert an input transition (high to low) to an output pulse from 10 microseconds to 30 seconds.

K333 — Pulsers: three pulse circuits which produce pulse widths above 10 microseconds. Pulse widths can be varied by adding capacitance to connections provided.

K371 — Timer Controls: Full complement of timing component boards which bolt directly on timing

K373

K374
K375
K376
K378

modules. These timing component boards contain calibrated controls for setting the time required.

K301	---	\$15
K303	---	\$27
K323	---	\$35
K333	---	\$23
K371	---	\$11
K373	---	\$11
K374	---	\$15
K375	---	\$11
K376	---	\$15
K378	---	\$15

<p>MANUAL CONTROLS K410, K420, K422, K424, K432</p>

<p>K SERIES</p>

K410 — Indicator Lights: five indicator lights which can be used to monitor logic level outputs.

K415 — Nixie Display: Side-viewing Nixie with right and left decimal points and numerals 0-9. Accepts BCD input and needs only a 12.6 Volt supply.

K415	---	\$46
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K420 — Switches: three manual switches with built in switch filters.

K422 — Thumbwheel Encoders: dual 10 position thumbwheels with circuitry to produce BCD outputs.

K424 — Thumbwheel Decoders: dual 10 position thumbwheels with circuitry to detect any BCD digit.

K432 — Timer Controls: various timing components to be used with K3XX Series modules.

K410	---	\$18
K420	---	\$33
K422	---	\$27
K424	---	\$27
K432	---	\$33

INPUT CONVERTERS
K501, K508, K522, K524, K531,
K578, K580, K581, K596

K
SERIES

K501 — Schmitt Triggers: four circuits which may be connected to noisy signal sources to prevent false triggering. Built in hysteresis and slowed outputs insure reliable operation.

K508 — AC Input Converter: operating through a K716 interface block, this module converts 120 VAC input voltages to logic levels.

K522 — Sensor Converters: two comparator circuits which convert resistance changes and small voltage variations to logic levels.

K524 — Sensor Converters: four comparator circuits which convert resistance changes and small voltage variations to logic levels.

K531 — Quadrature Decoder: quadrature decoder that provides the proper direction and count controls for a K220 UP/DOWN counter register.

K578 — 120 VAC Input Converter: eight circuits which convert 120 VAC inputs to logic levels. The inputs to the converter are through transformers which provide sufficient reactive load to keep contacts clean.

K580, K581 — Dry Contact Filters: these filters are used with wiping type switches and provide a voltage divider to convert high DC voltages to logic levels.

K596 — EIA Input Converter: transforms any bipolar input signal with amplitudes between ± 3 Volts and ± 25 Volts into standard K Series or M Series logic signals.

K501	—	\$25
K508	—	\$44
K522	—	\$25
K524	—	\$98
K531	—	\$70
K578	—	\$80
K580	—	\$28
K581	—	\$20
K596	—	\$20

OUTPUT CONVERTERS
K604, K614, K615, K644, K656,
K658, K671, K681, K683, K696

K
SERIES

K604 — Isolated AC Switch: four switching circuits, which allow logic levels to control AC devices, such as, solenoids, AC valves, small motors, and motor starters. Each switch can handle 250 Volt amperes.

K614 — Isolated AC Switch: four switching circuits which allow logic levels to control AC devices, such as, solenoids, AC valves, small motors, and motor starters. Each switch can handle 500 Volt amperes.

K615 — Isolated AC Switch: four switching circuits which allow logic levels to control AC devices, such as, solenoids, AC valves, small motors, and motor starters. Each switch is rated at 500 VA and provides a fail-safe against accidental removal of modules or cut wires that connect directly to the AC switch input.

K644 — DC Driver: four switching circuits used to switch stepping motors, DC solenoids and similar devices rated up to 2.5 amperes at 48 Volts.

K650 — DC Driver: four switching circuits used to switch DC loads rated up to 1 ampere at up to 55 Volts.

K652 — DC Driver: four switching circuits used to switch DC loads rated up to 2.5 amperes at up to 55 Volts.

K656 — DC Driver: four switching circuits used to switch stepping motors, DC solenoids and similar devices rated up to 1 ampere at 250 Volts.

K658 — DC Driver: four switching circuits used to switch stepping motors, DC solenoids, and similar devices rated up to 4 amperes at 125 Volts.

K671 — Decimal Decoder and NIXI Display: contains a side viewing Burroughs type nixi glow tube, and a decimal decoder. One K771 power supply is needed for each 6 nixi displays.

K681 and K683 — Lamp Drivers: eight circuit modules which can drive external resistive and inductive loads. They are used primarily to drive incandescent lamps.

K696 — EIA Output Converter: six bipolar non-inverting driver circuits which convert standard logic levels to either American EIA or European CCITT signals for data transmission.

K604 — \$110

K614 — \$ 88

K615 — \$ 92

K644 — \$ 66

K650 — \$ 40

K652 — \$ 50

K656 — \$ 80

K658 — \$128

K671 — \$ 55

K681 — \$ 15

K683 — \$ 30

K696 — \$ 44

INTERFACE HARDWARE
K716, K724

K
SERIES

K716 — Interface Block: interconnection interface for those K-Series modules that communicate with external equipment. External field wiring terminates at a 24-terminal screw connection block that accepts plain stripped wire up to 14 gauge.

K724 — Interface Shell: shell which provides the connectors and mechanical support for self-contained interface modules, K578, K604, K614, K615, K656 and K658.

K716 — \$75
K724 — \$55

POWER
K730, K731, K732, K741, K743

K
SERIES

K730 — General Purpose Module: the K730 can be used with any +5 VDC power supply to generate the turn on and power OK signals. It also rectifies 12.6 VDC to approximately 16 VDC and 10 VDC.

K731 — Source Module: supplies +5 VDC power to pin A of all K Series modules and provides several specialized once-per-system control functions.

K732 — Slave Regulator: this module is normally tied to pins of a K731 source. For each unit of current emitted by the K731 the K732 emits two. Up to three K732 slaves can be controlled by a single K731 for a total system current of 7 amperes.

K741 and K743 — Power Transformers: these hash-filtered, 50/60 Hz transformers supply K731 source and K732 Slave Regulator modules. The K743 also provides an auxiliary 12 VAC winding for use with K902, K508, K681, K683 and K730 modules.

K730 — \$19
K731 — \$30
K732 — \$27
K741 — \$30
K743 — \$45

K771 — Display Supply: the K771 supplies power and a convenient two screw mounting for up to six K671 display tubes.

K771 — \$35

K782 and K784 — Terminals: these modules offer an alternative to the K716 for obtaining field wiring connections in K Series systems. The K782 has straight-through connections for use with K508, K524, or K644 modules. The K784 includes 60 V clamp diodes for protection of K681 or K683 modules driving inductive loads.

K782 — \$12
K784 — \$17

K791 — Test Probe: pocket test probe contains two pulse-stretching lamp drivers for visual indication of both transient and steady-state conditions.

K791 — \$40

K900 — Control Panel — Power Supply: Combination power supply and input, control panel for K Series Logic Laboratory.

K900 — \$185

K901 — Patch Board Panel: K Series Logic Laboratory panel that provides up to ten single height FLIP CHIP modules with logic power and patch connections.

K901 — \$125

K902 — Indicator Switch Panel: This panel provides facilities for control and observation of the Logic Laboratory.

K902 — \$145

K903 — Patch Panel Board: K Series Logic Laboratory panel that provides logic power and patch connections for four double height or eight single height FLIP CHIP modules.

K903 — \$155

K940 and K941 — Mounting Hardware: K940 is a mounting support that attaches to the enclosure. K941 is a removable bracket that mounts up to four H800 connector blocks.

K940 — \$4
K941 — \$6

K943-R and K943-S-19" Mounting Panel: these 19" panels have sixty-four 18 pin connector sockets with either wire-wrap (R) or solder fork (S) contact pins.

K943-R — \$96
K943-S — \$96

K950 — Modular Panel Hardware: the K950 provides a convenient way to build control panels containing lights, toggle and push button switches, timer controls and thumbwheel switches. The lower connector half of the control modules, K410, K420, K422, and K432 are plugged into the upper connectors across a K943 mounting panel and the manual controls protrude through the K950 panel frame.

K950 — \$39

K980 — End Plates: pair of plates for supporting 1907 cover to hold modules in K943 panel under shock and vibration.

K980 — \$6

K982 — Mounting Panel: the K982 is a predrilled 19" mounting panel on which can be mounted up to three separate power transformers (K741 or K743).

K982 — \$10

K990 — Timer Component Board: the K990 is a predrilled etched module for mounting up to six RC networks for K301, K303 or K323 timer controls.

K990 — \$4



DEC has more than 1.5 million square feet of manufacturing space. This view shows a portion of a module assembly area.

About Digital Equipment Corporation

In a little over a decade, Digital Equipment Corporation has grown from three employees and one floor of production space in a converted woolen mill, to a major international corporation. DEC now employs more than 5500. Our products are manufactured in several plants, and are sold and serviced from customer support centers in the United States, Canada, Japan, Australia and seven European countries.

We produce a wide variety of computer and control products ranging from logic modules to large time sharing computer systems. In addition to those logic modules and associated equipment detailed in this handbook, DEC also manufactures 12-, 16-, 18- and 36-bit computers, peripheral devices, special systems, accessories, programmable controllers and a wide variety of software.

DEC first began manufacturing computer-related equipment in 1957 when we introduced a line of solid state logic modules. These were initially used to test and build other manufacturers' electronic equipment. The logic module product lines have been continually broadened, and DEC now ranks as the world's largest manufacturing supplier of digital logic modules, producing more than three million per year.

Our first computer, the PDP-1 was introduced a decade ago, selling for \$120,000 while competitive machines were priced over \$1 million. Ever since the PDP-1, DEC has specialized in on-line, real-time computers.

The PDP-5, introduced in 1963, was the first truly small computer. The PDP-8 series, the PDP-5 successor announced in 1965, is one of the most popular and successful families of computers ever produced.

DEC is a leading force in small computers, but it also has been a pacesetter in other parts of the industry. For example, one of the first time sharing systems ever built incorporated a PDP-1. DEC introduced the first large-scale, commercially available time sharing system in 1965—the PDP-6. Its successor, the PDP-10, can do more at a price well under \$1 million than competitive systems costing several times as much.

With more than 12,000 computers now installed, DEC is the second largest manufacturer in terms of installations.

In industry, DEC computers provide engineers with a powerful control and testing tool. They control blast furnaces and open hearths, monitor slab mills and finishing mills, and control and monitor a variety of machine tools, transfer and material handling equipment. DEC computers assisted in the analysis of lunar rock samples, guided the SS MANHATTAN as she sailed the Northwest Passage, and are being used in testing the Boeing 747 jumbo jet, and the Anglo-French Concorde supersonic airplane.

In science, our computers have cut the researchers experiment time with direct, on-line data reduction. DEC computers control and monitor powerful nuclear reactors, control X-ray diffractometers, and analyze nuclear spectroscopy data. They are used extensively in environmental research and pollution control.

In virtually all DEC computer installations, DEC solid state logic is used for interfacing or control application.

GENERAL INFORMATION

FINANCIAL RESULTS

Total Sales (in millions)		Net Income (in millions)	
1970	\$ 135.4	1970	\$ 14.4
1969	\$ 91.2	1969	\$ 9.4
1968	\$ 57.3	1968	\$ 6.8
1967	\$ 38.8	1967	\$ 4.5
1966	\$ 22.7	1966	\$ 1.9

MAIN PLANT & CORPORATE HEADQUARTERS:

146 Main Street, Maynard, Massachusetts
(617) 897-5111

1,000,000 square feet

OTHER MANUFACTURING FACILITIES

Carleton Place, Ont., Canada	40,000 square feet
Leominster, Mass.	60,000 square feet
Reading, England	25,000 square feet
San German, Puerto Rico	58,000 square feet
Westfield, Mass.	260,000 square feet
Westminster, Mass.	260,000 square feet
TOTAL EMPLOYEES	5,900
Sales, Service and Support	1,400
Manufacturing	2,700
Engineering, Marketing, Programming	600
General and Administrative	1,200



PDP-8/E

GENERAL DESCRIPTIONS OF DEC PRODUCTS

(Excluding those discussed in this Handbook)

COMPUTERS

PDP-8/E The all new, lower cost successor to the PDP-8/I and PDP-8/L. It is the outgrowth of the largest concentration of minicomputer engineering, programming and user expertise in the world. Among the PDP-8/E features are: a unique internal bus system called OMNIBUS™, which allows the user to plug memory and processor options into any available slot location; the availability of 256 words of read only or read/write memory; a 1.2 microsecond memory cycle time; the use of TTL integrated circuitry with medium scale integration; expansion to 32,768 12-bit words; low cost mass storage expansion with DECdisk or DECTape.

PDP-11 An expandable general purpose computer with 4,096 basic words of standard core memory, each word 16 bits in length. Memory cycle time is 1.2 microseconds. Machine uses integrated circuitry and has some medium-scale integration in central processor.

PDP-12 Laboratory computer system capable of executing PDP-8 and LINC-8 programs. It has basic 4,096-word core memory. Each word is 12 bits in length. Basic laboratory system includes interactive graphics capability, magnetic tape storage, A/D converter, and pre-wired, real-time clock.

PDP-15 A medium-scale series with an 18-bit word length. Four basic versions: PDP-15/10, PDP-15/20, PDP-15/30, and PDP-15/40.

PDP-10 General purpose large computer with basic memory of 8,192 (36-bit) words, expandable to 262,144. Will handle up to 63 time-sharing users simultaneously with batch and real-time jobs at the same time.

COMPUTER-BASED SYSTEMS

The following describes a sample of some of the hardware/software application systems available from DEC.

INDAC-8 Small computer-based system for industrial data acquisition, process control, data logging, process monitoring and quality testing, uses simplified language designed for engineers, not programmers.

680/I Small computer-based data communications system built around PDP-8 family computers. It concentrates up to 128 teleprinter grade lines into one or more medium speed channels, drastically reducing the charges for telephone lines.

LAB-8 Small computer-based data signal averaging system, used in bio-medical, chemistry, and physics laboratories. Includes software for other functions.

TSS-8 Small computer-based general purpose time-sharing system designed to accommodate up to 16 users with a variety of software for many tasks.

TYPESET-8 Small computer-based system for setting type, producing punched tape containing all hyphenation, justification and format commands needed to set 12,000 lines of copy per hour.

GLC-8 Small computer-based gas liquid chromatography system that will service 20 or more gas chromatographs simultaneously. It reduces and analyzes data accurately, repetitively and economically.

CLINICAL-LAB-12 Real-time, on-line multiterminal small computer system designed to provide the clinical laboratory with an economical means of data collection, data reduction, and analysis.

EDUCATIONAL SYSTEMS These systems include computer and a variety of applications software. In the group are single language time-sharing systems and hardware/software calculator replacements.

DISPLAYS A variety of displays are available for all applications where the speed and flexibility of graphic communications increase system efficiency.

SPECIAL SYSTEMS

DEC's special systems group custom builds hardware and software systems for special applications.

SOFTWARE

A comprehensive line of software is available with DEC's hardware. Assemblers, debugging routines, editors, monitors, floating point packages and mathematical routines, diagnostic programs, are made available.

DEC has also developed such conversational, interpretive languages as: FOCAL[®], an on-line language used as a tool by students, engineers and scientists in solving a wide variety of numerical problems; and DIBOL[®], a business-oriented computer language designed to bring the speed and power of PDP-8 family computers to small- and medium-size business establishments.

OPTIONS & PERIPHERALS

Analog/Digital converters, display and plotting equipment, drums and disks, magnetic tape equipment, card equipment, line printers, and many others.

SUPPLIES

Power supplies, cabinetry, mounting hardware, tape, tape reels, storage racks, teletype ribbon and paper.

CONTROL PRODUCTS

In 1969 Digital formed the Control Products Group to focus attention on meeting the needs for advanced control systems for industry and other applications. Its organization is such that it provides the most effective use of Digital's resources in developing new products and application techniques necessary to achieve this goal. We suggest you obtain a Digital CONTROL HANDBOOK for more detailed explanation of the Control Products line. The line includes:

PDP-14 and PDP-14/L Programmable Controllers; Quickpoint-8, a system for preparing numerical control tape; **MINI-DNC**, a computer-based system for direct numerical control of machines. In addition, all the products described in this handbook, and the services of a Control Systems group are available through the Control Products Group.

WARRANTY

WARRANTY 1—B, R, W, M, K, AND A MODULES — All B, R, W, M, K, and A modules as shown in the Logic Handbook and Control Handbook, as revised from time to time, are warranted against defects in workmanship and material under normal use and service for a period of ten years from date of shipment providing parts are available. DEC will repair or replace, at DEC's option, any B, R, W, M, K, or A module found to be defective in workmanship or material within ten years of shipment for a handling charge of \$5.00 or 10 per cent of list price per unit, whichever is higher. Handling charges will be applicable from one year after delivery.

WARRANTY 2—SYSTEM MODULES, LABORATORY MODULES, HIGH CURRENT PULSE EQUIPMENT, G, S, H, AND NON-CATALOG FLIP-CHIP MODULES — All items referenced are warranted against defects in workmanship and material under normal use and service for a period of one year from date of shipment. DEC will repair or replace, at DEC's option, any of the above items found to be defective in workmanship or material within one year of shipment. Repair charges will be applicable from one year after delivery with repair charges varying depending on the complexity of the circuit.

The Module Warranty outside the continental U.S.A. is limited to repair of the module and excludes shipping, customer's clearance or any other charges.

Modules must be returned prepaid to DEC. Transportation charges covering the return of the repaired modules shall be paid by DEC except as indicated in previous paragraph, and will be made on a UPS basis, where available, or Parcel Post insured. Premium methods of shipment are available at customer's expense and will be used only when requested. If DEC selects the carrier, DEC will not thereby assume any liability in connection with the shipment nor shall the carrier be in any way construed to be the agent of DEC. Please ship all units to:

**Digital Equipment Corporation
Module Marketing Services
Repair Division
146 Main Street
Maynard, Mass. 01754**

No module will be accepted for credit or exchange without the prior written approval of DEC, plus proper Return Authorization Number (RA#).

All shipments are F.O.B. Maynard, Massachusetts, and prices do not include state or local taxes. Prices and specifications are subject to change without notice.

DISCOUNT SCHEDULE

Aggregate List Price	Applicable Discount
\$ 5,000 - 9,999	3%
10,000 - 19,999	5%
20,000 - 49,999	10%
50,000 - 99,999	15%
100,000 - 249,999	18%
250,000 - 499,999	20%
500,000 - 999,999	22%
1,000,000 - AND OVER	25%

Discounts apply to any combination of FLIP CHIP Modules.

See separate cabinet discount schedule on page 247.

PRODUCT LIST

Model #	Title	+5V Current in mA (max.)	Board Size	No. Slots	Price	Page
782	Power Supply				\$128.00	225
782-A	Power Supply				148.00	225
911	Patchcords (pkg/10)				9.00	321
914-7	Power Jumpers (pkg/10)				4.00	235, 324
914-19	Power Jumpers (pkg/10)				4.00	235, 324
915	Patchcords (pkg/100)				33.00	235
917	Daisy Chain				50.00	327
932	Bus Strip				.60	324
933	Bus Strip				1.00	234
934	Wire Wrapping Wire (1000 ft. roll)				50.00	234
935	Wire Wrapping Wire (1000 ft. roll)				60.00	234
936	19 Conductor Ribbon Cable				.60	234
939	Bus Strip				1.00	234
1907	Panel Cover				9.00	234
1943	Mounting Panel			F-B	111.00	215
				W-B	111.00	215
				F-B-P	121.00	215
				W-B-P	121.00	215
				F-M	132.00	215
				W-M	132.00	215
				F-M-P	142.00	215
				W-M-P	142.00	215
1945-19	Hold Down Bar				15.00	212
4913-K	Mounting Racks				25.00	324
74-06782	Kickplate				5.50	253
74-06793	Kickplate				8.00	253
A123	Positive Logic Multiplexer	45	SSS	1	58.00	258
*A160	High Impedance Multiplexer Expander	§	SDD	4	250.00	260
*A161	High Impedance Multiplexer with Output Buffer	§	SDD	4	375.00	262
*A162	High Impedance Multiplexer with Decoder	30 §	SDD	4	270.00	264
*A163	High Impedance Multiplexer with Decoder & Buffer	30 §	SDD	4	395.00	266
*A164	8 Channel Constant Impedance					

*New Modules

§ Refer to individual module data for additional power requirements.

Model =	Title	+5V Current in mA (max.)	Board Size	No. Slots	Price	Page
*A165	Multiplexer Expander Constant Impedance Multiplexer with Output Amplifier	§	SDD	4	350.00	268
*A166	Constant Impedance Expander Multiplexer with Decoder	§	SDD	4	475.00	270
*A167	Constant Impedance Multiplexer with Decoder & Output Amplifier	30 §	SDD	4	365.00	272
A207	Operational Amplifier	30 §	SDD	4	490.00	274
*A260	Dual Amplifier Card	§	SSS	1	45.00	284
A404	Sample & Hold	§	SDD	4	300.00	286
*A460	Sample & Hold	§	SDS	2	130.00	290
*A461	Sample & Hold	§	SDD	4	400.00	292
A613	12 Bit DAC	§	SDD	4	525.00	292
A618	10 Bit D/A Converter, Single Buffered	60 §	SDS	2	200.00	294
A619	10 Bit D/A Converter, Single Buffered	135 §	SDD	4	300.00	296
A620	10 Bit D/A Converter, Double Buffered	135 §	SDD	4	325.00	296
A621	10 Bit D/A Converter, Double Buffered	190 §	SDD	4	300.00	298
*A660	12 Bit Multiplying D/A Converter	190 §	SDD	4	375.00	298
A702	Reference Supplies	20 §	SDD	4	500.00	300
A704	Reference Supplies	§	SDS	2	58.00	302
A811	10 Bit A/D Converter	§	SDS	2	175.00	302
*A860	12 Bit Industrial Converter	300 §	SDD	4	350.00	304
*A861	High Speed 12 Bit A/D Converters	150 §	SDD	4	395.00	306
*A862	High Speed 12 Bit A/D Converter	420 §	SDD	4	595.00	308
A990	Amplifier Boards	§	SDD	2	4.00	312
A992	Amplifier Boards	§	SDD	2	4.00	312
Cab A	Cabinets				378.50	242
Cab B	Cabinets				392.50	242
Cab C	Cabinets				397.00	243
Cab D	Cabinets				358.00	243

Model =	Title	+5V Current in mA (max.)	Board Size	No. Slots	Price	Page
Cab E	Cabinets				372.00	244
Cab F	Cabinets				316.00	244
Cab G	Cabinets				450.00	244
Cab H	Cabinets				427.00	245
H001	Mounting Brackets (pr)				8.00	212
H002	Mounting Brackets (pr)				8.00	212
H020	19" Mounting Frame Casting				15.00	212
H021	End Plate				7.00	212
H022	End Plate				20.00	212
H500	Computer Lab				445.00	317
°H510	M Series Logic Lab				995.00	327
H520	K Series Logic Lab				995.00	319, 325
H701	Power Supply				116.00	225
H701-A	Power Supply				136.00	225
H704	Power Supply				200.00	227
H707	Power Supply				400.00	227
H716	Power Supply				150.00	229
H800-F	Connector Block				8.00	208
H800-W	Connector Block				8.00	208, 213
H801-F	Replacement Pins				2.00	208
H801-W	Replacement Pins				2.00	208
H802	Connector Block				4.00	209
H803	Connector Block				13.00	210, 213
H805	Connector Block				4.00	210, 211
H807	Connector Block				5.00	211
H808	Connector Block				10.00	211
H809	Replacement Pins				4.00	211
H810	Hand Wire Wrapping Tool (24 ga.)				99.00	238
H810-A	Hand Wire Wrapping Tool (30 ga.)				99.00	238
H810-B	Hand Wire Wrapping Tool (24 & 30 ga.)				150.00	238
H811	Hand Wrapping Tool				21.50	239
H811-A	Hand Wrapping Tool				24.50	239
H812	Hand Wrapping Tool				10.50	239
H812-A	Hand Wrapping Tool				10.50	239
H813	Hand Wrapping Tool				30.00	239
H813-A	Hand Wrapping Tool				30.00	239
H814	Hand Wrapping Tool				21.00	239
H814-A	Hand Wrapping Tool				21.00	239

Model #	Title	+5V Current in mA (max.)	Board Size	No. Slots	Price	Page
H820	Grip Clips (pkg/1000)				48.00	235
H821	Grip Clips (pkg/1000)				71.00	235
H825	Hand Crimping Tool				146.00	235, 236
H826	Hand Crimping Tool				210.00	235, 326
H911-J	Mounting Panel				151.00	217, 219
H911-K	Mounting Panel				161.00	217, 219
H914	Mounting Panel				125.00	218
H916	Mounting Panel				270.00	218
H917	Mounting Panel				260.00	218
H920	Module Drawer				170.00	221
H921	Front Panel				10.00	221
H923	Chassis Slides				75.00	221
H925	Module Drawer				250.00	222
H933	System Unit Mounting Panel			A—	37.00	220
				B—	37.00	220
				C—	54.00	220
				D—	42.00	220
H941-AA	19" Mounting Panel Frame				175.00	224
H950-AA	Frame				157.00	208, 249, 253
H950-BA	Full Door				42.00	253
H950-CA	Full Door				42.00	253
H950-DA	Mounting Panel Door				39.00	253
H950-EA	Mounting Panel Door				39.00	253
H950-FA	Mounting Panel Door Skin				17.00	253
H950-G	Table Top Assembly				50.00	253
H950-HB	Short Door				48.00	253
H950-HC	Short Door				48.00	253
H950-HE	Short Door				48.00	253
H950-HF	Short Door				48.00	253
H950-HG	Short Door				48.00	253
H950-HH	Short Door				48.00	253
H950-HJ	Short Door				48.00	253
H950-HK	Short Door				48.00	253
H950-JA	Special Short Door				60.00	253
H-950-JB	Special Short Door				60.00	253
H950-JC	Special Short Door				60.00	253
H950-LA	Frame Panel				6.00	248, 249, 253
H950-LB	Frame Panel				7.00	253
H950-P	Cover Panel				7.00	253
H950-Q	Cover Panel				11.00	253
H950-SA	Filter				4.00	253
H952-AA	End Panel				48.00	253
H952-BA	Stabilizer Feet				23.00	253

Model #	Title	+5V Current in mA (max.)	Board Size	No. Slots	Price	Page
H952-CA	Fan Assembly				40.00	253
H952-EA	Caster Set				7.00	253
H952-FA	Leveler Set				2.00	253
H952-GA	Filler Strip				40.00	253
H952-AM	End Panel				45.00	252
H954-AC	Frame				127.00	252
H954-BA	Full Door				65.00	252
H954-CA	Fan Assembly				73.00	252
H954-SA	Filter				3.50	252
H954-UA	Cover				47.00	252
H960-JE	Special Short Door				60.00	248,
	See Control Handbook for K Series modules					249,
K900	Control Panel— Power Supply				185.00	342
K901	Patch Board Panel				125.00	342
K902	Indicator Switch Panel				145.00	342
K903	Patch Panel Board				155.00	342
K940	Mounting Support				4.00	342, 213
K941	Mounting Frame				6.00	342, 213
K943-R	Mounting Panel				96.00	342, 216
K943-S	Mounting Panel				96.00	342, 216
K950	Modular Panel Hardware				39.00	343
K980	End Plates				6.00	343
K982	Mounting Panel				10.00	343
K990	Timer Component Board		SSS	1	4.00	343
M002	Logic 1 Source	16	SSS	1	10.00	29
M040	Solenoid Driver	47	SSS	1	39.00	30
M050	50 mA. Indicator Driver	47	SSS	1	31.00	32
M051	Positive to Negative Logic Level Converter	47	SSS	1	31.00	33
M100	Bus Data Interface	60	SSS	1	50.00	34
M101	Bus Data Interface	82	SSS	1	24.00	36
M102	Device Selector	130	SSS	1	60.00	38
M103	Device Selector	110	SSS	1	45.00	40
M105	Address Selector	338	ESS	1	65.00	42
M107	Device Selector	425	SDS	2	105.00	44
M108	Flag Module	137	SSS	1	45.00	46
M111	Inverter	50	SSS	1	22.00	48
M112	NOR Gate	50	SSS	1	35.00	41
M113	NAND Gates	71	SSS	1	18.00	50
M115	NAND Gates	41	SSS	1	18.00	50
M117	NAND Gates	41	SSS	1	19.00	50
M119	NAND Gates	19	SSS	1	18.00	50
M121	AND NOR Gate	50	SSS	1	23.00	53
M133	Input NAND Gates	160	SSS	1	27.00	54
M141	NAND OR Gates	117	SSS	1	29.00	56
M159	Arithmetic/Logic Unit	150	SDS	2	35.00	58

Model =	Title	+5V Current in mA (max.)	Board Size	No. Slots	Price	Page
M160	AND NOR Gate	30	SSS	1	33.00	62
M161	Binary to Octal/ Decimal Decoder	120	SSS	1	55.00	63
M162	Parity Circuit	102	SSS	1	63.00	65
*M168	12 Bit Magnitude Comparator	250	SSS	1	45.00	66
M169	Gating Module	50	SSS	1	33.00	68
M202	Triple J-K Flip Flop	57	SSS	1	29.00	69
M203	8 R'S Flip Flops	55	SSS	1	26.00	70
M204	General Purpose Buffer & Counter	74	SSS	1	34.00	72
M206	General Purpose Flip Flops	87	SSS	1	30.00	74
M207	General Purpose Flip Flops	96	SSS	1	33.00	76
M208	8 Bit Buffer/Shift Register	184	SSS	1	84.00	78
M211	Binary Up/Down Counter	217	SSS	1	69.00	81
M213	BCD Up/Down Counter	160	SDS	2	86.00	82
M230	Binary to BCD & BCD to Binary Converter	860	SDS	2	105.00	85
*M232	16 Word RAM	200	SDS	2	125.00	87
*M236	12 Bit Binary Up/ Down Counter	330	SSS	1	50.00	88
*M237	3 Digit Binary Up/ Down Counter	330	SSS	1	50.00	90
*M261	4 State Motor Translator	175	SSS	1	40.00	92
*M262	10 State Motor Translator	350	SSS	1	65.00	94
M302	Dual Delay Multivibrator	166	SSS	1	46.00	98
M306	Integrating One Shot	120	SSS	1	27.00	100
M310	Delay Line	89	SSS	1	58.00	102
M360	Variable Delay	50	SSS	1	68.00	103
M401	Variable Clock	80	SSS	1	55.00	104
M405	Crystal Clock	50	SSS	1	100.00	106
M410	Reed Clock	95	SSS	1	70.00	107
M452	Variable Clock	77	SSS	1	40.00	110
M500	Negative Input Positive Output Receiver	64	SSS	1	55.00	111
M501	Schmitt Trigger	31	SSS	1	25.00	112
M502	Negative Output Converter, High Speed	49	SSS	1	26.00	114
M506	Negative Input Converter, Medium Speed	81	SSS	1	52.00	115
M507	Bus Converter	42	SSS	1	45.00	116
M510	I/O Bus Receiver	170	SSS	1	51.00	118
*M521	K to M Converter	56	SSS	1	16.00	119
M602	Pulse Amplifier	213	SSS	1	28.00	120
M606	Pulse Generator	188	SSS	1	43.00	121

WIDTH: Single, Double, or Triple
HEIGHT: Single, Double, or Quad
LENGTH: Standard, Extended

Model #	Title	+5V Current in mA (max.)	Board Size	No. Slots	Price	Page
*M610	Open Collector 2 Input NAND Gate	41	SSS	1	20.00	123
M617	4 Input Power NAND Gate	97	SSS	1	26.00	124
M622	8 Bit Positive Input/Output Bus Driver	210	SSS	1	45.00	125
M623	Bus Driver	71	SSS	1	40.00	127
M624	Bus Driver	89	SSS	1	45.00	128
M632	Positive Input Negative Output Bus Driver	175	SSS	1	55.00	130
M633	Negative Bus Driver	100	SSS	1	50.00	132
M650	Negative Output Converter	37	SSS	1	25.00	134
M652	Negative Output Converter	122	SSS	1	26.00	135
M660	Positive Level Driver	71	SSS	1	25.00	136
M661	Positive Level Driver	111	SSS	1	15.00	137
*M671	M to K Converter	112	SSS	1	52.00	138
M706	Teletype Receiver	400	SDS	2	150.00	140
M707	Teletype Transmitter	375	SDS	2	150.00	146
M730	Bus Interface	500	SDS	2	160.00	150
M731	Bus Interface	500	SDS	2	160.00	150
M732	Bus Interface	500	SDS	2	160.00	154
M733	Bus Interface	500	SDS	2	165.00	154
M734	I/O Bus Input Multiplexer	325	SDS	2	105.00	158
M735	I/O Bus Transfer Register	425	SDS	2	135.00	160
M736	Priority Interrupt Module		SDS	2	125.00	163
M737	12 Bit Bus Receiver Interface	300	SDS	2	120.00	167
M738	Counter Buffer Interface	250	SDS	2	105.00	169
*M782	Interrupt Control	277	ESS	1	100.00	171
*M783	Unibus Drivers	69.9	ESS	1	30.00	174
*M784	Unibus Receivers	200	ESS	1	30.00	175
*M785	Unibus Transceiver	118	ESS	1	35.00	176
*M786	Device Interface	600	EDS	2	220.00	178
*BB11	System Unit for General Interfacing				90.00	179
M901	Flexprint Cable Connector	100	SSS	1	15.00	180
M903	Flexprint Connector		SSS	1	12.00	181
M904	Coaxial Cable Connector		SSS	1	14.00	182
M906	Cable Terminator	440	SSS	1	20.00	183
M907	Diode Clamp Connector	10.2	SSS	1	16.00	184
M908	Ribbon Connector		SSS	1	18.00	185
M909	Terminator		SSS	1	14.00	186
M910	Terminator		SSS	1	20.00	187
*M1103	2 Input AND Gates	80	SSS	1	14.00	188
*M1307	4 Input AND Gates	100	SSS	1	12.00	189

WIDTH: Single, Double, or Triple
HEIGHT: Single, Double, or Quad
LENGTH: Standard, Extended

Model #	Title	+5V Current in mA (max.)	Board Size	No. Slots	Price	Page
*W940	Wire Wrappable Module		EQD	8	70.00	192
*W941	Wire Wrappable Module		EPD	4	40.00	192
*W942	Wire Wrappable Module		EQD	8	140.00	192
*W943	Wire Wrappable Module		EDD	4	75.00	192
*W950	Wire Wrappable Module		EQD	8	65.00	192
*W951	Wire Wrappable Module		EDD	4	40.00	192
*W960	MSI Mounting Board		SSS	1	8.00	194
*W966	Wire Wrap Module		EQS	4	85.00	195
*W967	Wire Wrap Module		EQS	4	165.00	195
*W968	Collage Mounting Board		EQS	4	45.00	196
*W969	Collage Mounting Board		EDS	2	30.00	196
W970	Blank Module		SSS	1	4.00	197
W971	Blank Module		SDS	2	8.00	197
W972	Blank Module		SSS	1	4.00	197
W973	Blank Module		SDS	2	6.00	197
W974	Blank Module		SSS	1	9.00	197
W975	Blank Module		SDS	2	18.00	197
W979	Collage Mounting Board		SDS	2	20.00	200
W980	Module Extender		SSS	1	14.00	201
W982	Module Extender		ESS	1	18.00	202
*W984	Module Extender		EDS	2	30.00	203
W990	Blank Module		SSS	1	2.50	197
W991	Blank Module		SDS	2	5.00	197
W992	Blank Module		SSS	1	2.00	197
W993	Blank Module		SDS	2	4.00	197
W998	Blank Module		SSS	1	4.50	197
W999	Blank Module		SDS	2	9.00	197

WIDTH: Single, Double, or Triple
HEIGHT: Single, Double, or Quad
LENGTH: Standard, Extended

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