Super I/O Controller

User's Guide

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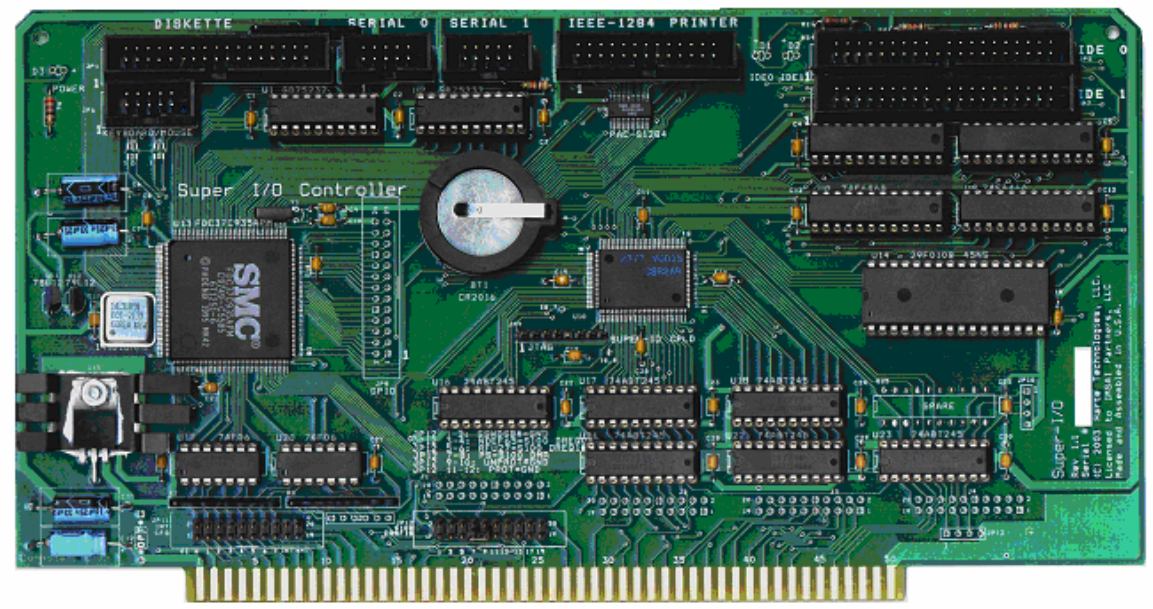

First Edition (February 2004)

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Table of Contents

1. Introduction

The HarteTec Super I./O Controller Board provides a complete I/O subsystem for the IEEE-696 bus. The Super I/O Controller supports 8-bit address decoding for compatibility with the original IMSAI 8080 and other S-100 bus systems as well as enhanced 16-bit address decoding supported by the MPU-C processor board in the IMSAI Series Two. The Super-I/O controller also supports DMA for floppy disk access via the MPU-C processor board on-board DMA controller. The Super-I/O controller does not support IEEE-696 Temporary Master Access (TMA.)

The Super I/O Controller provides the following features:

- Standard Microsystems Corporation (SMsC) FDC37C935APM Super I/O Controller.
- Support for two Floppy Diskette drives, in any combination:
- 3.5-inch 2.88MB, 1.44MB, 720KB.
- 5.25-inch 1.2MB, 360KB, DS/HD, DS/DD, SS/DD, SS/SD.
- 8-inch Single or Double-Density.
- Two NS16550-compatible UARTS.
- One IEEE-1284-compatible parallel port.
- PS/2-compatible keyboard/mouse controller.
- Two independent IDE channels supporting up to two IDE devices each.
- Battery backed real-time clock/calendar with non-volatile RAM.
- 128KB FLASH memory with banked memory support and selectable window size.

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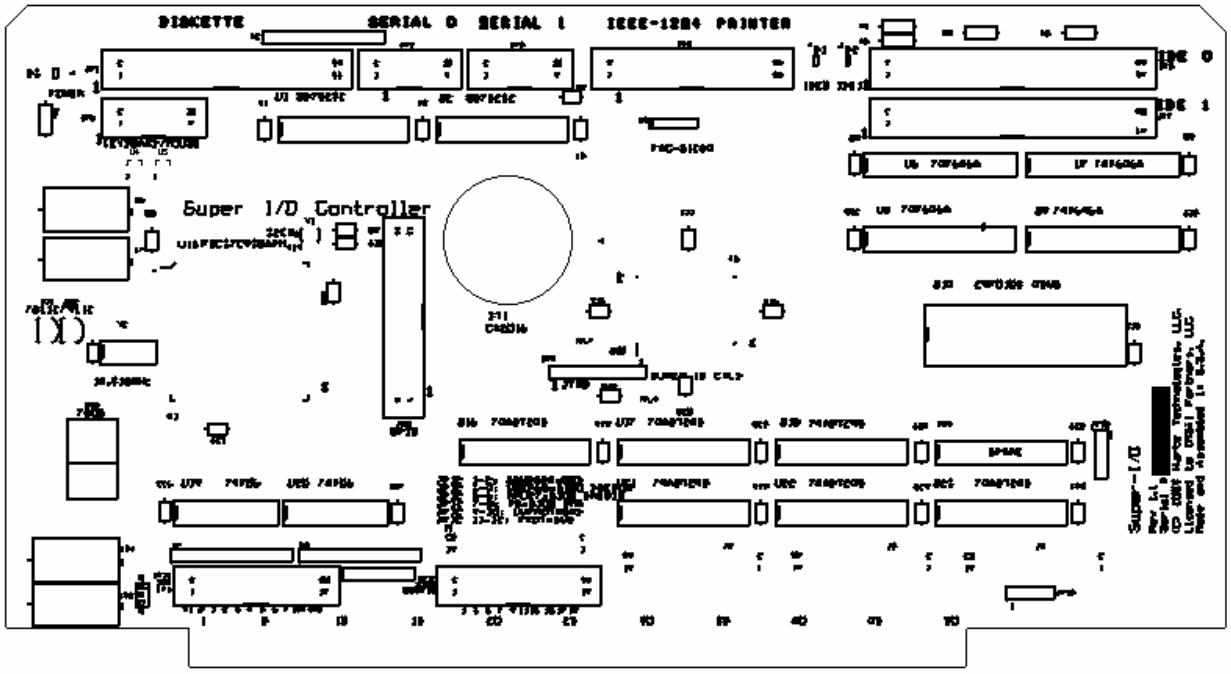


1.1. System Requirements

The Super-I/O controller is an S-100/IEEE-696 compatible controller card. Minimum system requirements are:

- Zilog Z80 CPU Board running at 4MHz or greater
- 64KB of RAM that supports PHANTOM.
- Power-on jump to address 0000H. (This is the Z80 default startup address.)
- Free I/O address space from 080H to 0FFH.

1.2. Super-I/O Controller Packing List

You should have received the following contents in your Super-I/O package. If any parts are missing, please contact: hharte@hartetec.com immediately.

One HarteTec Super-I/O Controller PC Board, fully assembled.
Two 2x5-pin header to DB9-P serial adapter cables.
One 2x13-pin header to DB25-S parallel adapter cable.
One floppy diskette cable.
One 40-pin IDE cable.
One DB9-S to DB9-S Serial Null Modem Cable
This manual
CP/M 3.0 Boot Diskette (720K 3.5” floppy diskette)

Additional information and source code are available from www.cpm80.com.

2. Hardware Installation

The Super-I/O controller may be installed in any available IEEE-696 bus slot. Slots closer to the rear of the chassis may be preferable to minimize cable routing issues.

Check jumper settings on the Super-I/O Controller with the tables in section 2.1. For legacy S-100 systems, the factory-default jumper settings should be sufficient for most applications. Make sure that a jumper is installed between pins 7 and 9. This allows the Super-I/O controller to operate without a DMA controller present in the system.

Install the 2x17-pin floppy diskette cable in the connector marked JP1.

1. Install two 2x5-pin header to DB9-P serial adapter cables in connectors marked JP2 and JP3.

2. Install the 2x13-pin header to DB25-S parallel adapter cable in the connector marked JP4.

3. Install the 2x20-pin IDE cable in the connector marked JP5.

4. Insert the Super-I/O Controller into a free IEEE-696 expansion slot.

5. Connect the floppy disk drive cable and IDE cable to PC-compatible devices. The installation media consists of a 720K 3.5" floppy diskette, so a 720K or 1.44M floppy disk drive should be connected as drive A: on the floppy drive cable.

6. Connect a serial cable to the serial port 0 9-pin connector. This is the console serial port. Default settings for this port are 9,600 baud, 8 data bits, one stop bit, and no flow control. The 9-pin connector for this port has the same pinout as a standard IBM AT serial port. If you are using a PC as a terminal, then the supplied "null modem" cable must be used between this port and the serial port on the PC. See section x.y for details on using HyperTerminal communications program under Windows, and section X.Z for details on using MS-DOS Kermit.

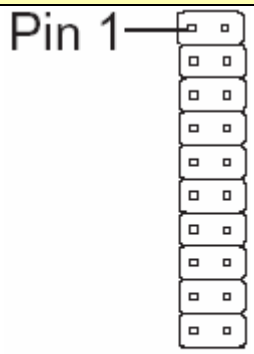
7. Power the system up, and if using a front-panel machine such as an IMSAI 8080, lift the RESET switch, and then depress the RUN switch. If using a machine without a front panel, the system should automatically reset and enter the run state. A sign-on message and prompt should appear on the serial terminal:

```
Super-I/O 8K MONITOR v1.01        S/N: xxxxxxxx

(c) 2002-2003 Harte Technologies, LLC.
(c) 1979-1983 Fischer-Freitas Company.
(c) 1977,1978 IMSAI Manufacturing Company.

%
```

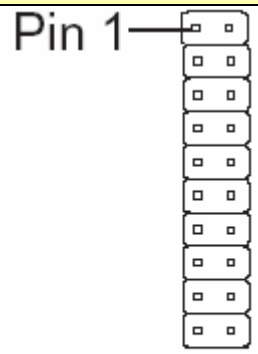
10. Congratulations! Hardware installation is now complete. If the prompt above does not appear, then re-check all connections and verify serial port settings on your serial terminal.

2.1. Hardware Configuration Options

Interrupt Configuration Jumper Block (JP11)

Jumper Block JP11	Description (When jumper is inserted)	Notes	
1-2	SMsC IRQ10 maps to IEEE-696 VI0	[DEFAULT]	
3-4	SMsC IRQ9 maps to IEEE-696 VI1	[DEFAULT]	
5-6	SMsC IRQ8 maps to IEEE-696 VI2	[DEFAULT]	
7-8	SMsC IRQ7 maps to IEEE-696 VI3	[DEFAULT]	
9-10	SMsC IRQ6 maps to IEEE-696 VI4	[DEFAULT]	
11-12	SMsC IRQ5 maps to IEEE-696 VI5	[DEFAULT]	
13-14	SMsC IRQ4 maps to IEEE-696 VI6	[DEFAULT]	
15-16	SMsC IRQ3 maps to IEEE-696 VI7	[DEFAULT]	
17-18	SMsC IRQ3 maps to IEEE-696 INT		
19-20	SMsC IRQ3 maps to IEEE-696 NMI		
Note: odd pins on Jumper block JP11 may be used as testpoints to their respective S-100 bus signals. Odd pins are connected to the S-100 bus, while even pins are connected to the Super I/O local bus.			

S-100 Bus Configuration Jumper Block (JP12)

Jumper Block JP12	Description (When jumper is inserted)	Notes	
1-2	S100 SSWDSB# tied to ground.		
3-4	IEEE-696 NDEF65 is S100_DREQ0	(MPU-C Specific)	
5-6	IEEE-696 NDEF66 is S100_DREQ1	(MPU-C Specific)	
7-8	S100 PS is S100_DMA	(MPU-C Specific)	
7-9	L_DMA tied to gound.	Necessary when the Super I/O board is used in a system without DMA. [DEFAULT]	
9-10	UNPROT tied to ground.		
11-12	PROT tied to ground		
14	SS Test Point		
16	RUN Test Point		
18	RFU27 Test Point		
20	PINTE Test Point		
Note: even pins on Jumper block JP12 may be used as testpoints to their respective S-100 bus signals. Even pins are connected to the S-100 bus, while odd pins are connected to the Super I/O local bus.			

3. Software Installation

The Super-I/O 8K Monitor provides the ability to examine and deposit memory locations, perform I/O operations, boot FLASH memory blocks, and do other general purpose testing and debugging operations. The Super-I/O 8K Monitor will be used to further verify correct system operation as follows:

1. Test system RAM memory:

```
% T 0000,BFFF <enter>
```

   The memory test may take several minutes, and will return silently to the '%' prompt if no errors are encountered. If any memory errors are detected, the address of the memory compare failures will be printed on the console. Although the system has 64K of RAM, we only test locations 0000H through 0BFFFH as the monitor resides in RAM from locations 0C000H to 0DFFFH.

2. Boot CP/M 3.0 from the floppy diskette:

```
% B 1<enter>
```

   This causes 8K FLASH memory block number 1 (block 0 is reserved for the Monitor) to be copied into locations 0000H through 1FFFH, and then a jump to 0100H is performed. FLASH memory block 1 contains the CP/M 3 Loader. After pressing enter, you should see the light on the A: drive turn on. The drive should seek to track 2, and begin loading CP/M 3.0 as follows:

```
CP/M V3.0 Loader
Copyright (C) 1998, Caldera Inc.

 BIOS3    SPR  EB00  0C00
 BDOS3    SPR  CA00  2100

 50K TPA

Common System Load
Common Load Complete
Banked System Load
Executing System


Super-I/O CBIOS v1.2 (C) 2002-2004 Harte Technologies, LLC.

A>
```

3. You now have a running CP/M 3.0 system. If you have two 3.5" floppy drives installed in your system, this would be a good time to make a backup copy of the

CP/M 3.0 distribution disk. Place a blank 720K diskette in the B: drive and proceed as follows:

```
A>pip b:=a:*.*

COPYING -
CPM3.SYS
CCP.COM
[…]

A>
```

4. Basic software installation is now complete. If you plan to use an IDE disk drive with the Super-I/O Controller, please continue installation with section 4.

4. IDE Drive Installation

The Super-I./O Controller supports up to four IDE devices per system. Each of the two IDE port connectors controls one master and one slave device. The Primary IDE controller is under CBIOS control to support IDE hard drives, including traditional hard drives, 2.5" hard drives, and FLASH memory cards. The CP/M CBIOS drivers use Logical Block Addressing (LBA) mode of the IDE drive to allow for efficient mapping of CP/M sectors and tracks to physical drive sectors. In order for CP/M to be able to address partitions on large IDE drives the concept of a physical "Block" was introduced. The physical block is comprised of 256 512-byte sectors, and is 128K bytes in length. CP/M supplies the 128K Block address as the "Track" number and each CP/M track is comprised of 256 sectors. Sectors are numbered 0 through 255.

A setup utility, `SETUP.COM`, is provided to help initialize, partition, and format IDE drives for use with CP/M. To set configure an IDE drive for the first time, follow this procedure:

1. Boot CP/M from a floppy disk and run `SETUP.COM`:

```
A>setup
S-100 Super I/O Setup Utility v1.0
(c) 2003-2004 Harte Technologies, LLC.

Current time is: 0/0/0, 0:0:0

Main Menu:

1. Set Date and Time
2. Configure IDE devices

Return to CP/M

? 2          (Choose Menu option 2 to Configure IDE devices.)
```

```
Current Device is: Device 0: FUJITSU MPA3026AT
        [Size: 2503MB, 20026 Blocks]


IDE Menu [Current Device: 0]

1. Show IDE Devices
2. Initialize Device
3. Change Geometry
4. Partition Device
5. Test Device (Write)
6. Test Device (Read)
7. Block Copy
8. Change Current Device

0. Return to Main Menu

? 2
```

(Choose menu option 2 to Initialize the selected device.)

```
Initialize IDE Device 0

Device initialization writes a new partition table onto the
device.
All data on the selected IDE device will be lost.

All data on IDE device 0 will be lost.
Do you wish to continue (Y/N)?

? y

Initialization Complete.

IDE Menu [Current Device: 0]

1. Show IDE Devices
2. Initialize Device
3. Change Geometry
4. Partition Device
5. Test Device (Write)
6. Test Device (Read)
7. Block Copy
8. Change Current Device

0. Return to Main Menu
? 4
```

(Choose menu option 4 to partition the IDE device)

```
Partition Table Entries
=======================

Num     Start   End     Type    Flags   Name
----------------------------------------------------------------------
No partitions defined.
Enter partition number [1-255]  :1
Enter starting Block [1-20026]          :1
Enter ending Block  [1-20026]           :490     (Partition is ~64MB)
Enter partition name [21 max]   : CP/M 3.0
Enter Partition Type [0-255]    : 1
Enter Partition Flags [0-255]: 0

Writing partition entry 1 to table.
Done.

Partition Menu:

1. Show Partition Table
2. Create/Modify Partition
3. Format Partition
4. Delete Partition

0. Return to IDE Menu

? 3                    (Choose Menu option 3 to format the partition)
```

```
Format Device 0 Partition

Formatting writes the format fill byte to all blocks in the
partition's directory.  If you select an ehaustive format, all
blocks in the partition will be filled.

Partition Table Entries
=======================

Num     Start   End     Type    Flags   Name
----------------------------------------------------------------
1)      1       490     1       0       CP/M 3.0
Which partition do you want to format? 1

Do you want an exhaustive format? (Y/N) n
Start Block: 1
End Block 490

All data on device 0 partition 1 "CP/M 3.0" will be lost.
Do you wish to continue? (Y/N) y
Formatting...

Block 3

Partition Menu:

1. Show Partition Table
2. Create/Modify Partition
3. Format Partition
4. Delete Partition

0. Return to IDE Menu

? 0

IDE Menu [Current Device: 0]

1. Show IDE Devices
2. Initialize Device
3. Change Geometry
4. Partition Device
5. Test Device (Write)
6. Test Device (Read)
7. Block Copy
8. Change Current Device

0. Return to Main Menu

? 0
```

```
Main Menu:

1. Set Date and Time
2. Configure IDE devices

0. Return to CP/M

? 0                                    (Return to CP/M)

Goodbye.
A>
```

Now that a partition has been created and formatted, you can copy CP/M files onto it. First, copy the CP/M Command Processor (CCP.COM) onto the hard drive. The CCP.COM file is distributed on the CP/M 3.0 Boot Disk with the SYS attribute set. This allows the CCP.COM file to be loaded regardless of what user area is selected. In order to copy CCP.COM, you must first remove the SYS attribute.

```
A>SET CCP.COM[DIR]
```

Next, copy CCP.COM to the hard drive.

```
A>PIP C:=A:CCP.COM
```

Finally, restore the CCP.COM SYS attribute on the Boot Disk, and also set the SYS attribute

```
A>SET CCP.COM[SYS]
A>C:
C>SET CCP.COM[SYS]
C>
```

Now, you may create a runtime Boot Floppy Disk by writing surun3-720k.img onto a floppy diskette following the steps outlined in Section 6. The runtime boot floppy disk is identical to the distribution disk, except that it loads the CCP.COM file from the C: drive during warm boot. This increases the responsiveness of the system. If the CCP.COM file on drive C: should be deleted or become damaged, it will be necessary to boot from the distribution diskette to correct the problem.

The latest disk image files may be downloaded from: www.cpm80.com

5. Copying Files Onto CP/M Diskettes

Files may be copied onto CP/M diskettes in the format used by the Super-I/O controller using the 22DISK program available from Sydex. This program must run under MS-DOS or Windows 95/98 "Reboot in DOS Mode." A download link for 22DISK v1.44 is provided at www.cpm80.com. Download and install 22DISK and then download the SUPERIO.DEF file which contains the disk definitions for the disk formats supported by the Super-I/O CP/M CBIOS. This definition file should be used in place of CPMDISKS.DEF supplied with 22DISK. Alternatively, you can download SUPERIO.D2 which is the source format of the disk definition file. This file may be added to the source definition file supplied with 22DISK and compiled into CPMDISKS.DEF using the GENINDEX utility supplied with 22DISK.

The following are disk definitions for the Super-I/O CP/M 3 CBIOS:

```
BEGIN SU3H  SUPER-I/O CP/M 3.5" DS/HD 160 tracks, 18spt
DENSITY MFM ,HIGH CYLINDERS 80 SIDES 2 SECTORS 18,512
SIDE1 0 1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18
SIDE2 1 1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18
ORDER SIDES
BSH 04h BLM 0Fh EXM 0 DSM 02CAh DRM 07Fh AL0 0C0h AL1 00h
OFS 1
END

BEGIN SU3D  SUPER-I/O CP/M 3.5" DS/DD 160 tracks, 9spt
DENSITY MFM ,LOW CYLINDERS 80 SIDES 2 SECTORS 9,512
SIDE1 0 1,2,3,4,5,6,7,8,9
SIDE2 1 1,2,3,4,5,6,7,8,9
ORDER SIDES
BSH 04h BLM 0Fh EXM 0 DSM 0162h DRM 07Fh AL0 0C0h AL1 00h
OFS 2
END

BEGIN SU5H  SUPER-I/O CP/M 5.25" DS/HD 160 tracks, 15spt
DENSITY MFM ,HIGH CYLINDERS 80 SIDES 2 SECTORS 15,512
SIDE1 0 1,2,3,4,5,6,7,8,9,10,11,12,13,14,15
SIDE2 1 1,2,3,4,5,6,7,8,9,10,11,12,13,14,15
ORDER SIDES
BSH 04h BLM 0Fh EXM 0 DSM 253h DRM 07Fh AL0 0C0h AL1 00h
OFS 1
END

BEGIN SU5D  SUPER-I/O CP/M 5.25" DS/DD 40 tracks, 9spt
DENSITY MFM ,LOW CYLINDERS 40 SIDES 2 SECTORS 9,512
SIDE1 0 1,2,3,4,5,6,7,8,9
SIDE2 1 1,2,3,4,5,6,7,8,9
ORDER SIDES
BSH 04h BLM 0Fh EXM 1 DSM 0AEh DRM 03Fh AL0 080h AL1 00h
OFS 2
END
```

6. Making CP/M Diskettes from Image Files

6.1. Procedure for Windows Operating Systems

CP/M Diskettes may be created from disk image files using the NTRawrite.exe utility. This utility is able to create image files from diskettes as well as make diskettes from image files. The Super-I/O CP/M Distribution diskette is contained on the image file `sucpm3-720k.img`. This section illustrates how to make a CP/M boot diskette from an image file under Windows NT, 2000, or XP.

Creating a diskette from an image file is a two-step process. First, a blank 720K 3.5-inch floppy must be formatted.

```
C:\>format a:/f:720
Insert new disk for drive A:
and press ENTER when ready...
The type of the file system is RAW.
The new file system is FAT.
Verifying 720K
Initializing the File Allocation Table (FAT)...
Volume label (11 characters, ENTER for none)?
Format complete.

      730,112 bytes total disk space.
      730,112 bytes available on disk.

        1,024 bytes in each allocation unit.
          713 allocation units available on disk.

           12 bits in each FAT entry.

Volume Serial Number is A85B-4E22

Format another (Y/N)? n
```

Next, the image file is written to the diskette using NTRawrite.exe:

```
C:\>ntrawrite -f sucpm3-720k.img -d a:
NTRawrite v1.0.1 by Blake Ramsdell
<bcr@users.sourceforge.net>

Please insert a diskette and press any key.
Copying image file sucpm3-720k.img to floppy drive A.
************************************]
Verifying image file sucpm3-720k.img with floppy drive A.
************************************]
Completed!
```

6.2. Procedure for Linux Operating Systems

This procedure is courtesy of Harold Bower:

To make CP/M Boot disks from the image file(s) on the CDROM, or downloaded from the Super-I/O web site in the Linux™ system, you do not use the NTRawrite utility, but standard programs provided with most, if not all, distributions.

The following procedures were tested and documented on an Athlon motherboard running TurboLinux Workstation 8.0 with an Epson dual-media floppy disk (3.5" as fd0 and 5.25" as fd1).

If you are in doubt about the validity of the 720/800kB floppy diskette with which you are working, it is best for bulk-erase it if you have the ability. This will remove residual inter-track "noise" and give the best results when the diskette is moved between drives. Next, you must format it to place the basic indexing data on the media. Insure that the index tab is closed (covering the hole and allowing writes). If you have a system where the 3.5" drive is in the second (fd1) position, substitute 'fd1' for 'fd0' in the following commands. Format by entering (as root):

```
fdformat /dev/fd0H720
```

When this is complete, write the image file to the diskette. The following command assumes that you will be using the image on the SuperIO CDROM mounted at /mnt/cdrom. If you are using another image, adjust the path/name as appropriate in the 'if=' argument in the command:

```
dd if=/mnt/cdrom/download/sucpm3-720k.img of=/dev/fd0H720 bs=512 count=1440
```

The diskette may now be removed from the Linux machine and used to boot your SuperIO-equipped machine.

7. Programming the FLASH ROM

The FLASH ROM may be programmed in-system under CP/M in order to update the MONITOR, boot loaders, and other code stored in the FLASH. In order to update the FLASH, you use the `FLASHPRO.COM` utility, along with a binary image file containing the new code to be burned into the FLASH.

The Super-I/O Controller contains an AMD 29F010B FLASH memory device. This device is capable of storing 128KB of information. The device is organized as eight sectors of 16KB each. The device may be erased as a whole, or individual sectors may be erased and reprogrammed. The Super-I/O MONITOR divides the FLASH into sixteen blocks of 8KB each. The first block, Block 0, contains the MONITOR itself, and subsequent blocks may be booted from the monitor using the 'B' command.

`FLASHPRO.COM` allows the user to selectively reprogram 8K blocks. Although an entire 16KB sector is erased and reprogrammed, the data for the block that is not to be reprogrammed is saved and programmed back into the FLASH along with the new selected block data.

When programming the FLASH, one or two 8K blocks may be programmed at a time. For even numbered blocks (Blocks 0, 2, 4, 6, 8, A, C, E) either 8K or 16K may be programmed. The amount of data to be programmed depends on the image file size. For odd numbered blocks (Blocks 1, 3, 5, 7, 9, B, D, F) only 8K images may be programmed.

`FLASHPRO.COM` usage is as follows:

```
FLASHPRO <filename.img> <b>
```

Where <filename> is the name of the binary image file to be programmed into the FLASH, and <b> is the starting Block number.

When programming FLASH blocks 0 and 1, it is very important that the operation succeeds. If the operation fails for any reason, the Super-I/O MONITOR and/or floppy disk boot loader will be corrupted. Before programming FLASH blocks 0 and 1, it is best to test the FLASH programming operation on another block to make sure that the erase/program/verify operation succeeds.

If you accidentally corrupt your FLASH device, you may download a HEX image file from www.cpm80.com and program it into the FLASH using a device programmer such as the Needhams Electronics EMP-21. Pre-programmed replacement FLASH devices are also available at www.cpm80.com for a nominal fee.

8. S-100 Processor and Memory Card Notes

8.1. S-100 Processor Cards

North Star ZPB-A

Power-on Jump Address must be set to 0000H:
POJ Address header at location E2 must be wired as follows:
Pins 9 through 16 connected to pin 8.
If you are using a non-North Star chassis, please consult the ZPB-A Manual for other board settings that may be necessary.
A copy of the manual can be found on the internet at:
http://www.imsai8080.com/computers/s100/northstar.html

Cromemco ZPU Card

1. CPU Speed must be set to 4MHz.
2. Jump address must be set to 0000H if the Jump Enable is selected (Factory default unless trace is cut.) To set the jump address to 0000H, the four-position DIP switch should be set to all ON (0 position on silk screen.)
3. RFSH ENAB may need to be jumpered depending on your RAM card. Some DRAM cards require this jumper to be installed.
4. A copy of the ZPU Manual can be found on the internet at:
   http://www.imsai8080.com/computers/s100/cromemco.html

Cromemco DPU Card:

POJ ADDR traces A15 and A14 must be cut on the back side of the board.

1. A copy of the *Cromemco 68000 Board Family Manual* can be found on the internet at: http://www.imsai8080.com/computers/s100/cromemco.html

California Computer Systems (CCS 2810):

Jumpers should be set as follows:

SER EN	OFF
ROM EN	OFF
M1 WAIT	ON (upper two pins)
JMP EN	OFF
PHANTOM	ON
REFRESH	Depends on Memory Card

2. CPU speed selection switch should be set at 4MHz.

California Computer Systems (CCS 2820):

RESET selection on silk screen may need to be modified to include PRST. This was necessary when running in a North Star HORIZON chassis, but may not be necessary in the CCS chassis.

CompuPro CPU-Z:

The CPU-Z operates at 2-,3-,4-, or 6-MHz depending on the crystal selection at X1 and the setting of S1-5. With a 16MHz crystal, the CPU-Z can operate at 2- or 4-MHhz. With a 24MHz crystal, the CPU-Z can operate at 3- or 6-MHz. Regardless of operating speed, M1 wait states need to be enabled to work with the Super-I/O. The CPU-Z is able to boot CP/M when running at 3-, 4-, or 6-MHz. For reliable 6-MHz operation, a fast memory card is required. CP/M will not boot at 2-MHz because the CPU cannot read from the floppy interface quickly enough to prevent FIFO under-runs.

1. DIP switches should be set as follows:

S1-1,2,3,4	Wait-state selection depends on memory cards. M1 wait state is necessary. See manual.
S1-5	OFF (4/6MHz operation)
S1-6,7	Don't care (unused)
S1-8	ON (Power-on-jump enable)
S2-1…8	OFF (Power-on-jump address)
S3-1,2,3,4	ON,OFF,OFF,OFF (ROM at address 08000H)
S3-5	ON (ROM Socket Disable)
S3-6	Don't care (ROM Base Page Only)
S3-7	ON (Jump on RESET enable)
S3-8	OFF (No vectored interrupts)

Compu/Time SBC-880:

Compu/Time SBC-880, Copyright 1980 Compu/Time (Also stenciled as QT "Quick and Timely" SBC+2/4), Etch on solder-side "SBC-780 Rev A". (Courtesy of Harold F. Bower.)

a. Jumpers should be set as follows:

A-B	Open
C-D-E	D-E Jumpered (MWRT generated by CPU and external systems)
Q-R and T-U	Both open (Disable power-on-jump and PHANTOM.)

b. Since the EPROM/RAM (U23) is not used, it may be removed.

c. Disable the On-board serial port, parallel port and timer by removing the following ICs:

U26	8131
U6	1489
U7	1488
U8	8251
U9	8253
U15	74347
U16	74374

The fixed on-board 1k RAM (2 x 2114) should be addressed to the top of memory (FC00-FFFF) by setting all positions of SW2 to "OFF"

Tarbell 3033

Must be set to 4MHz operation.

Ithaca Audio 1010 CPU

There are two versions of the IA 1010 CPU. One is marked Rev 1.1, and the other is marked Rev 2.0. Their jumper locations and settings differ slightly. Wire mods were taken from my boards, and may or may not be necessary for your CPU card. I don't know what these mods are for, or whether they are complete or not. Also, I may have missed some cuts that might be required to implement these mods. Proceed with them at your own risk.

1. DIP switches and jumpers should be set as follows:

U5-1	OFF for front-panel machines, ON to allow the CPU board to generate MWRT.
U28	Don't Care (on-board ROM address)
J1	Shorted (not marked on Rev 1.1 board. Located between U9 and U15.
J2	Short pins 2-3 (middle and lower posts.) Not marked on Rev 1.1 board. Located between U23 and U28.
J3	Between U8 and U9. A-B shorted (not found on Rev 1.1 board.) Note: J3 is also marked on the top right corner of the board near the CPA connector (U34.) This J3 actually refers to the pads 'B,' 'C,' and 'D' on the back side of the board.
J4	Shorted
J5	E-F shorted
J6	H-J shorted

Wire modifications:

Rev 2.0:

1	Wire between S-100 bus pin 67 and pads 'D' on back side of the board near CPA connector. Bots pads 'D' should be shorted together and connected to S-100 bus pin 67. This mod applies to Rev 1.1 also.
2	Wire between U36 pin 12 and U34 pins 9 and 10. This mod applies to Rev 1.1 also.

Rev 1.1:

1	Wire mods 1 and 2 as per Rev 2.0 board.
2	Cut trace connected to pin 67 at S-100 bus fingers.
3	Wire between S-100 bus pin 66 and U11 pin 7
4	Wire between U11 pin 6 and U pin U30 pin 28 (Z80 Refresh on pin 66.)

5	Wire between U7 pins 2 and 14.
6	Wire U22 pins 1, 14 and 10 together.
7	Wire U22 pins 4 and 11 together.

8.2. S-100 Memory Cards

General Notes

1. PHANTOM# Must be enabled and supported by your memory card.
2. Only 64K Cards, or combinations of cards totalling 64K are supported by the stock firmware/CBIOS. There is no reason why less memory couldn't be used, but this requires some minor modification to the monitor and CBIOS code.

North Star 64K HRAM

1. Does not support PHANTOM#, but works anyway. Make sure all 64K is enabled. North Star configured HRAMs typically have RAM from E800-EFFF disabled to make room for the MDS-AD disk controller.

A copy of the manual can be found on the internet at:
http://www.imsai8080.com/computers/s100/northstar.html

Digital Research (Tanner Computers) 64K SRAM

1. DIP switches should be set as follows:

S1	All OFF
S2 1-5	OFF
S2 6	ON (Full PHANTOM)
S2 7,8	OFF

CCS 64K DRAM Board

1. DIP switches should be set as follows:

CompuPro RAM-20 32K SRAM Board

These following settings are known to work, although other settings may also work depenging on your CPU board capabilities.

1. DIP switches should be set as follows:

S1	All ON (All banks enabled)
S2-1,2,3,4	RAM Base address (set to OFF for 0000H, or set to OFF,OFF,OFF,ON for 8000H)
S2-5	ON (No extended addressing)
S2-6	ON (PHANTOM Enabled)
S2-7,8	ON,OFF (RAM enabled after RESET)
S3	Don't care
S4	Don't care

2. Install 25LS2521 in position U11. Remove any ICs from U6 and U10.

CompuPro RAM-22 256K SRAM Board

This memory card requires the use of a CPU card which supports 24-bit addressing. The Comemco DPU card works fine with it; however, the ZPU does not. Grounding address lines A[23:16] on the S-100 bus may allow this card to work with 16-bit address CPU cards, although this has not been tested.

1. DIP switches should be set as follows:

S1	All ON (A[23:18] = 0)

CompuPro RAM-23 128K SRAM Board

This memory card requires the use of a CPU card which supports 24-bit addressing. The Comemco DPU card works fine with it; however, the ZPU does not. Grounding address lines A[23:16] on the S-100 bus may allow this card to work with 16-bit address CPU cards, although this has not been tested.

1. DIP switches should be set as follows:

S1	All ON (A[23:16] = 0)

Dual Systems DMEM 256KP Rev B 256K DRAM Board

This memory card appears to require the use of a CPU card which supports 24-bit addressing. The Comemco DPU card works fine with it; however, the ZPU does not. Grounding address lines A[23:16] on the S-100 bus may allow this card to work with 16-bit address CPU cards, although this has not been tested.

1. DIP switches should be set as follows:

SWA	All ON (Down) First 128K Bank at 000000H
SWB	All ON (Down) except SWB-2 OFF (Up) Second 128K Bank at 020000H
SWC-1 SWC-2…7 SWC-8	OFF (Down) I/O Ports 7EH, 7FH ON (Up) Don't Care

2. Jumpers should be set as follows:

VI0…VI7, NMI, ER	Open
PH	Installed
S…R	Open
P…L	Jumper between "L" and middle pin.

Sirton Computer Systems 64k Memory SRAM Board

1. Jumpers should be set as follows:

SWA	All ON (Down) First 128K Bank at 000000H
SWB	All ON (Down) except SWB-2 OFF (Up) Second 128K Bank at 020000H
SWC-1 SWC-2…7 SWC-8	OFF (Down) I/O Ports 7EH, 7FH ON (Up) Don't Care

2. Jumpers should be set as follows:

VI0…VI7, NMI, ER	Open
PH	Installed
S…R	Open
P…L	Jumper between "L" and middle pin.

8.3. S-100 CPU/Memory Compatibility Matrix

This matrix illustrates tested CPU/Memory combinations. If a box is contains a check ('√') mark, then the particular CPU/Memory combination has been tested with the Super-I/O controller. If a box contains 'Ø,' then the particular CPU/Memory combination is known not to work, at least not with the jumper/switch settings described above. If a box is empty, then this combination has not been tested.

		S-100 Memory Cards																
		North Star 64K HRAM	DRI/Tanner 64K	CCS 64K DRAM	Sirton 64K SRAM	Dual 256K DMEM	"S-100" 32K SRAM[1]	Super-RAM 32K	Compu-Pro Ram 20	Compu-Pro Ram 22	Compu-Pro Ram 23	IA 8K SRAM						
S-100 CPU Cards	Cromemco ZPU	√	√	Ø	√	Ø	√	√	√									
	Cromemco DPU	√	√	√	√	√	√	√	√	√	√							
	Northstar ZPB-A[2]		√	√	√	Ø	√	√	√									
	CCS-2810	√	√	√	√	Ø	√	√	√									
	CCS-2820[2]		Ø	√	√	Ø	Ø	Ø	√									
	IA-1010 Rev 1.1		√	Ø	√	Ø	Ø	Ø	Ø									
	IA-1010 Rev 2.0		√	Ø	√	Ø	√	√	√									
	Tarbell 3033		√															
	CompuPro CPU-Z (3MHz)		√	√	√		√	√	√									
	TDL ZPU																	
	OSM Z80A CPU																	

[1] This memory board does not support PHANTOM, so it must be addressed from 8000H-FFFFH to prevent conflicts with the Super-I/O on-board FLASH memory.

[2] Appears to exhibit RESET problem. Workaround: remove U16 pin 13 from socket to allow power-on RESET only. S-100 RESET will be disabled.

9. Configuring Common Communications Programs on the PC Platform

This section describes how to set up two common communications programs on the PC platform. MS-DOS Kermit can be used for MS-DOS, Windows 9x, Windows Me, Windows NT/2000/XP. HyperTerminal runs only under Windows platforms. ***Note that MS-DOS Kermit may not work with Universal Serial Bus (USB) to serial port converters.***

9.1. MS-DOS Kermit

MS-DOS Kermit v3.15 may be downloaded from www.cpm80.com/superio.html. It runs under MS-DOS, Windows 9x, Windows Me, Windows NT/2000/XP. MS-DOS Kermit is the preferred terminal program on the PC platform as it provides many features not available in HyperTerminal. In addition, it is directly compatible with CP/M Kermit-80 supplied on the CP/M 3.0 Boot Disk distributed with the Super-I/O controller.

C:\>msk315.exe
IBM-PC MS-DOS Kermit: 3.15 15 Sept 1997
Copyright (C) Trustees of Columbia University 1982, 1997.

Type ? or HELP for help

MS-Kermit>**set port 2** [the COM port that the Super-I/O console port is connected to]
MS-Kermit>set speed 9600
MS-Kermit>**c** [enter]

After typing 'c' and pressing enter, a terminal session will begin. At this point, you can power up the S-100 chassis, and you should see the Super-I/O Monitor Sign-on message:

Super-I/O 8K MONITOR v1.0 S/N: xxxxxxxx

(c) 2002-2003 Harte Technologies, LLC.
(c) 1979-1983 Fischer-Freitas Company.
(c) 1977,1978 IMSAI Manufacturing Company.

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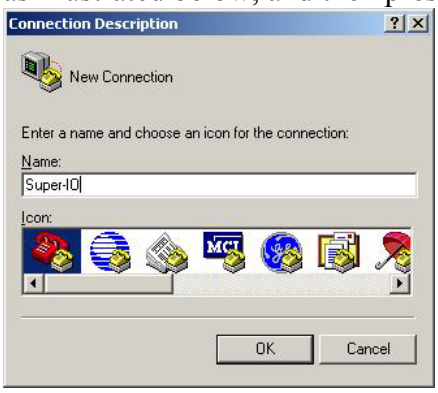
9.2. HyperTerminal

HyperTerminal is supplied with Microsoft Windows. The versions of HyperTerminal shipped with different releases of Windows differ, but in general, you want to configure HyperTerminal for 9600 Baud, no flow control. The following example is taken from HyperTerminal running under Windows 2000:

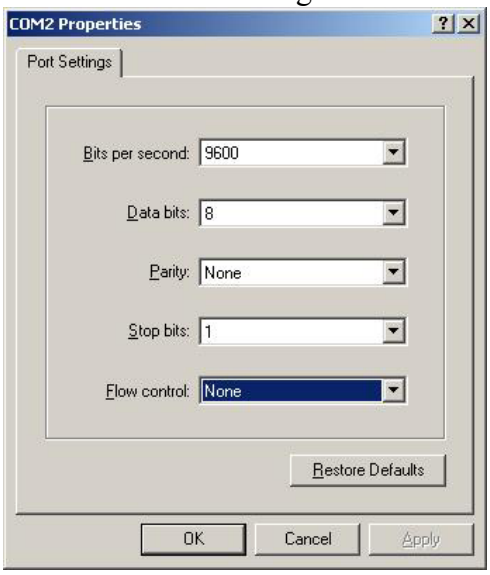
1. Open HyperTerminal and create a new connection. You may name the connection as illustrated below, and then press OK.



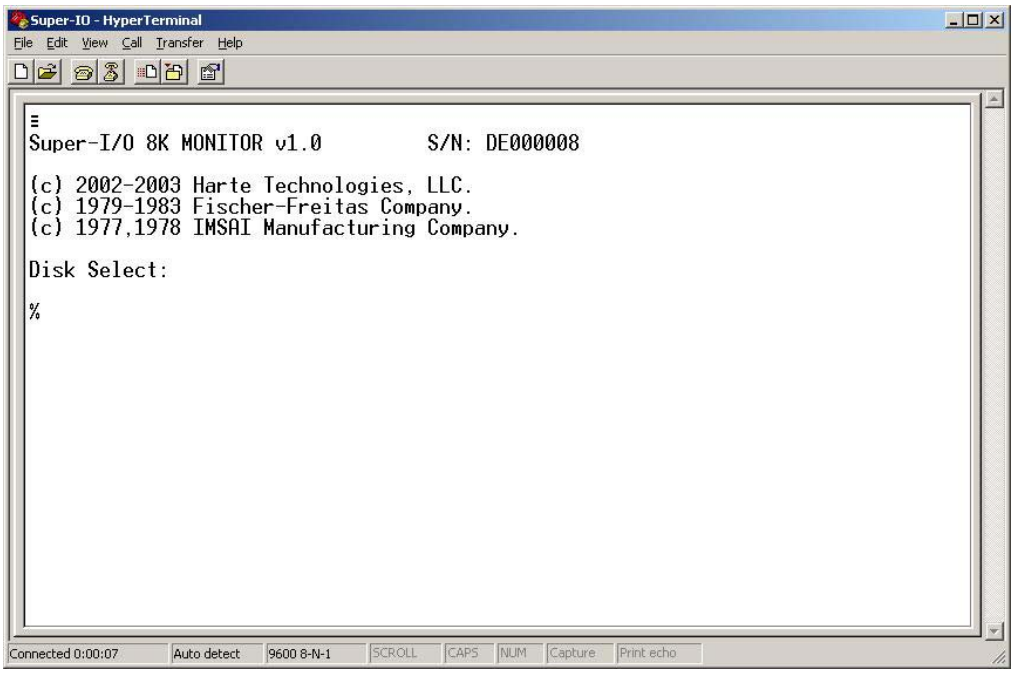
2. Next, select the COM port to which the Super-I/O console port is connected. In this example, the Super-I/O is connected to COM2. Then press OK.

3. Then, set the communications parameters as follows:
   Bits per second: 9600
   Data bits: 9
   Parity: None
   Stop bits: 1
   Flow-control: None

When finished selecting the communications parameters, press OK.



4. Finally, a terminal session starts. Power on the S-100 chassis, and the Super-I/O should sign on similar to the following:



10. References

1.SMSC FDC37C93xAPM Data Sheet, Standard Microsystems Corporation, 1996.

2.CP/M 3.0 System Guide, Digital Research, 1983.