VB1C ™ 64 CHARACTER VIDEO INTERFACE
S-100 Bus

INSTRUCTION MANUAL

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APPENDIX:

1.0 INTRODUCTION

The SSM VB1C provides a memory mapped video display for any S-100 bus compatible microcomputer.

The VB1C features such capabilities as 32 or 64 characters per line (switch selectable) by 16 lines, upper and lower case with descenders, Greek characters, graphic symbols, black-on-white or white-on-black display, 7 x 9 character matrix, and 1K on-board RAM.

The VB1C is fully compatible with the proposed IEEE 696 standard, with two exceptions: 1) the VB1C uses the 01 clock on bus pin 25 instead of the new $\overline{\text{PSTVAL}}$ signal; and 2) when the CPU reads data from the VB1C, data is transferred back without the use of the SMEMR and PDBIN signals.

We suggest that you read this entire manual before either starting assembly or use to improve your understanding of the board and make its set-up and use that much easier.

NOTES:

The VB1C meets the following IEEE 696 compliance levels: D8, M16, NI, T250, W0, SH.

All references to the PC board assume that the board has the 100-pin connector at the lower edge, and the component side (the side with the silk screen) is facing you.

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8080 and 8085 are trademarks of INTEL CORP., 3065 Bowers Avenue, Santa Clara, CA 95051.

2.0 ASSEMBLY INSTRUCTIONS

Refer to the Assembly Drawing in the APPENDIX during assembly and test procedures.

2.1 UNPACKING

[ ] Unpack and check each of the parts against the PARTS LIST provided.

It is a good idea to arrange the parts in a small tray or box to allow for easy identification and accessibility during assembly.

2.2 RESISTOR INSTALLATION

NOTE: Be sure that all resistors and diodes are flush against the PC board. This will insure proper socket installation. **DO NOT install R21 and R22 at this time.**

[ ] Install and solder SIX (6) 100 ohm (brown, black, brown) resistors at locations R1, 2, and 5-8.

[ ] Install and solder TEN (10) 2.7K ohm (red, violet, red) resistors at locations R4, 11-18, and 24.

[ ] Install and solder ONE (1) 1K ohm (brown, black, red) resistor at location R23.

[ ] Install and solder ONE (1) 220 ohm (red, red, brown) resistor at location R3.

[ ] Install and solder TWO (2) 470 ohm (yellow, violet, brown) resistors at locations R9 and 10.

2.3 DIODE INSTALLATION

[ ] Install and solder ONE (1) 1N270 germanium signal diode at location CR1. **Use caution in installing this component—the banded end (+) MUST be to the LEFT of the board.**

2.4 SOCKET INSTALLATION

NOTE: DO NOT install integrated circuits until specifically instructed to do so.

[ ] Install the 8, 14, 16, and 24 pin sockets on the printed circuit board. Orient pin 1 towards the top of the board or to the left, as applicable. See Figure 1 for information on locating Pin 1 on each socket.

CAUTION! DO NOT install a socket at location S1. A switch will be installed at this location in a later step.

Three (3)	8-pin sockets at U1-3
Nine (9)	14-pin sockets at U4,10-13,17,18,20,21
Twenty-five (25)	16-pin sockets at U6-8,14,19,22-29,31-42
Three (3)	24-pin sockets at U5,15,16

Socket Types

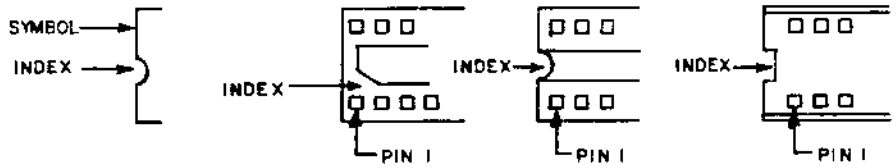


FIGURE 1

[ ] When all sockets are inserted, place a piece of stiff cardboard over the sockets to hold them in place and turn the board over to expose the reverse side.

[ ] On each socket, solder pin 1 and the pin diagonally opposite it to 'tack' (lightly solder) each socket in place. When all sockets are tacked in place, turn the board over and examine each socket to make sure it is flush against the board. If needed, reheat the pins and adjust any sockets not firmly mounted.

[ ] When all the sockets are properly seated, solder the remaining pins of each socket. **Do not overheat.**

2.5 CAPACITOR INSTALLATION

[ ] Install and solder TEN (10) 0.1 uf monolithic capacitors at locations C1, 2, 5-9, and 11-13.

[ ] Install and solder ONE (1) 47-56 pf disc capacitor at location C4.

[ ] Install and solder ONE (1) .0033 uf disc capacitor at location C17.

[ ] Install and solder TWO (2) 10 uf axial capacitors at locations C3 and C10. **Use caution in installing these components--C3 and C10 MUST have the positive (+) end to the RIGHT side of the board.**

[ ] Install and solder ONE (1) 4.7 uf axial capacitor at location C14. **Use caution in installing this component--C14 MUST have the positive (+) end to the LEFT side of the board.**

2.6 TRANSISTOR INSTALLATION

[ ] Install and solder ONE (1) 2N3904 transistor at location Q1. Again, use caution in installing this component; refer to Figure 2 for proper orientation. **Use caution that the lead closest to the bottom of the board DOES NOT touch R8.**

Top View

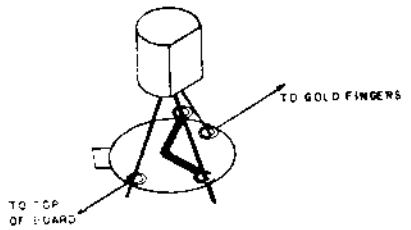


FIGURE 2

2.7 CRYSTAL INSTALLATION

[ ] Install and solder ONE (1) 12.44 MHz crystal at location Y1. Two holes have been provided on either side of the crystal to solder a strap over the crystal to hold it in place. Use a resistor lead to make this strap. **DO NOT overheat the crystal.**

2.8 REGULATOR INSTALLATION

[ ] Place TWO (2) 7805 regulators on the board so that the mounting hole in the regulator is in line with the hole in the board. Mark the leads for proper bending to match the holes in the board (allow for bend radius).

[ ] Bend the regulator leads to match the holes in the board.

[ ] If available, apply thermal compound to the back side of each regulator case (the side that will contact the heatsink). Use just a little thermal compound. **Too much is worse than none at all.**

[ ] Install and solder TWO (2) 7805 regulators at locations U9 and U30 so that the following order results from back to front: screw, PC board, heatsink, regulator, lock washer, and nut. Be sure that the regulators and heatsinks sit flat on the board and then solder all regulator leads.

2.9 CONNECTOR, HEADER AND SWITCH INSTALLATION

[ ] Install and solder ONE (1) 4-pin molex connector at location J1 such that the short pins are inserted in the PC board. Be sure that the teflon base sits flat against the board.

[ ] Install and solder ONE (1) 2-pin molex connector at location J2 such that the short pins are inserted in the PC board. Again, be sure that the teflon base sits flat against the board.

[ ] Install and solder ONE (1) 3-pin header at location E1-E3.

[ ] Install and solder ONE (1) 8-position DIP switch at location S1. Orient the switch with position 1 at the top of the board.

At this point the only parts yet to be mounted are the two power resistors and all the ICs. DO NOT INSTALL THESE PARTS AT THIS TIME.

3.0 FUNCTIONAL CHECK/IC INSTALLATION

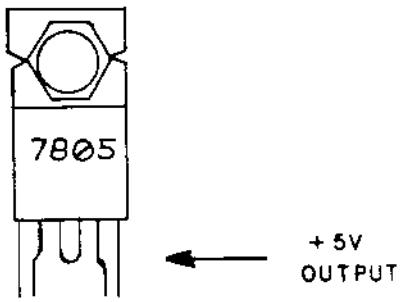
WARNING! DO NOT INSTALL OR REMOVE THE BOARD WITH POWER ON. DAMAGE TO THIS AND OTHER BOARDS COULD RESULT!

3.1 SHORT TEST

[ ] If an ohmmeter is available, measure the resistance between pin 50 (negative meter probe) and pin 1 (positive meter probe) on the edge connector, and verify a resistance of 20 ohms or greater. **If your reading is below 20 ohms, check your board for possible shorts.**

3.2 VOLTAGE CHECK

[ ] Apply power (+8V to +10V) to the board by plugging into the computer or by connection to a suitable power supply (with power turned off). Measure the outputs of the +5V regulators (U9 and U30). The voltage should be +5.0V (+/- 0.2V). If the regulator doesn't meet this test, check the board for shorts or errors. (See the figure below for the pin assignments of the regulator.)



CAUTION! WHILE IT HAS NEVER HAPPENED TO US, SHORTED REGULATORS HAVE BEEN KNOWN TO EXPLODE WITH POSSIBLE INJURY TO EYES AND HANDS. BETTER SAFE THAN SORRY—KEEP YOUR FACE AND HANDS CLEAR OF THE REGULATOR SIDE OF THE BOARD DURING THE INITIAL POWER-UP OF YOUR BOARD.

3.3 POWER RESISTOR INSTALLATION

[ ] Insert and solder TWO (2) 15 ohm 3-watt power resistors at locations R21 and R22. For improved cooling and to prevent the PC board from discoloring, mount these two resistors off the board about 1/8 inch.

3.4 VISUAL INSPECTION

[ ] Now, look over the board carefully. Check for solder bridges, cold solder joints, and unsoldered pins. Also, using the Assembly Drawing in the APPENDIX, check for improper part location or polarity. A few minutes of careful inspection could save hours in troubleshooting later.

3.5 IC INSTALLATION

[ ] Refer to the Assembly Drawing to install the following integrated circuits. **BE CERTAIN THAT PIN 1 OF EACH IC IS ORIENTED PROPERLY.** It is sometimes helpful to bend the leads of the IC's **SLIGHTLY** inward by placing the circuit on its side and applying firm pressure. This assures that the leads will be straight and makes it easier to install the device in the socket.

[ ] Install the following IC's as shown in the Assembly Drawing:

[ ] U4	7486
[ ] U17	74LS00
[ ] U18	7432
[ ] U23,28,34,35,40,41	74367
[ ] U42	DM8131

[ ] The following IC's are extremely sensitive to static electricity. Avoid touching the IC leads without first touching the PC board to make sure that both items are at the same static potential.

[ ] U24,25,26,27	2102AL-2
[ ] U36,37,38,39	

[ ] The VB1C can now be tested as a standard 1K memory board. A memory test program is provided in Section 6.6 for this purpose. Be sure to set the DIP switch (S1) to the desired setting before attempting any testing. Refer to Section 4.1 for information on addressing your board.

[ ] Install the following IC's as shown in the Assembly Drawing:

[ ] U1,2,3	75451
[ ] U5,15	74150
[ ] U6,7	74157
[ ] U8	74166
[ ] U10	74S04
[ ] U11,12,13,20	7474
[ ] U14,22,32,33	74193/74LS193
[ ] U19	74153
[ ] U21	7408
[ ] U29,31	74161

[ ] The following IC is extremely sensitive to static electricity. Avoid touching the IC leads without first touching the PC board to make sure that both items are at the same static potential.

[ ] U16	MCM66714

[ ] The VB1C can now be tested for proper video operation. A program is provided in Section 6.5 to display the ASCII character set plus the 64 different graphic characters.

4.0 SETTING UP YOUR VB1C

4.1 ADDRESSING

The VB1C occupies 1K bytes of the address space of the computer. By setting DIP switch S1, the user can locate his VB1C at any one of 64 different memory locations.

Switch: ON=Closed=0
OFF=Open=1

ADDRESS	A15	A14	A13	A12	A11	A10
0000-03FF	ON	ON	ON	ON	ON	ON
0400-07FF	ON	ON	ON	ON	ON	OFF
0800-0BFF	ON	ON	ON	ON	OFF	ON
0C00-0FFF	ON	ON	ON	ON	OFF	OFF
1000-13FF	ON	ON	ON	OFF	ON	ON
.						
.						
.						
>B000-B3FF	OFF	ON	OFF	OFF	ON	ON
.						
.						
>>E000-E3FF	OFF	OFF	OFF	ON	ON	ON
.						
.						
FC00-FFFF	OFF	OFF	OFF	OFF	OFF	OFF

> Address used by SSM 8080 Monitor V1.0 in 2708 EPROM
>> Address used by SSM Z-80 Monitor V1.10 in 2716 EPROM

4.2 32 OR 64 CHARACTERS PER LINE SELECTION

The VB1C has the capability to display either 32 or 64 characters per line. The selection is made by setting switch 1 position 2 to the desired line length.

64 characters/line = switch ON or closed
32 characters/line = switch OFF or open

4.3 GRAPHICS OR INVERSE VIDEO SELECTION

The VB1C is switched between two types of display by setting data bit 7 to a 0 or a 1. The display mode is determined by the setting of S1-1 as follows:

BIT D7	'VID REV'/ GRAPHICS	DISPLAY
0	ON	Alphanumerics on a black background
1	ON	2x3 matrix graphics, black background
0	OFF	Alphanumerics on a black background
1	OFF	Alphanumerics on a white background

4.4 GRAPHICS PATTERNS

If switch S1-1 (GRPH) is on and the byte you are writing into the VB1C has the most significant bit (bit D7) set to a one, the display will show a graphics pattern. The lower 6 bits of each byte will display as a 2 x 3 matrix on the video display.

LOWER SIX BITS	INTENSITY
0	white
1	black

The data bits are displayed in the following manner:

DATA BIT	POSITION
D0	Upper left
D1	Middle left
D2	Lower left
D3	Upper right
D4	Middle right
D5	Lower right

4.5 BLANKING/MSB CONTROL

The VB1C has a 3-pin header used to control the default value of the most significant bit of data read into the video display during a blanking operation. During reading or writing to the VB1C, the address lines of the on-board memory are logically tied to the S-100 bus and not to the video timing. The MSB of data during reading or writing may differ from that which would have been displayed under normal video conbittrol, so the screen will "sparkle" with periodic differences between old and new characters. The MSB can be forced to a zero value during reading and writing to give a more consistent state, rather than random, by using the 3-pin header.

- Connect E1 to E2 if you want random.
- Connect E2 to E3 if you want the MSB=0 (recommended for most applications.

5.0 THEORY OF OPERATION

5.1 GENERAL INFORMATION

The VB1C video interface is essentially a computer memory combined with an interface circuit that connects the memory to a video monitor. The memory data may be displayed in either alphanumeric form using the internal character generator, or in a direct form (graphics). Characters may be presented either white-on-black or black-on-white, if the graphics mode is not selected. Mixing characters and graphics is also possible.

The 66714 character generator can display 128 different characters. Other generators with different character sets are also available from Motorola (and from SSM on special volume orders).

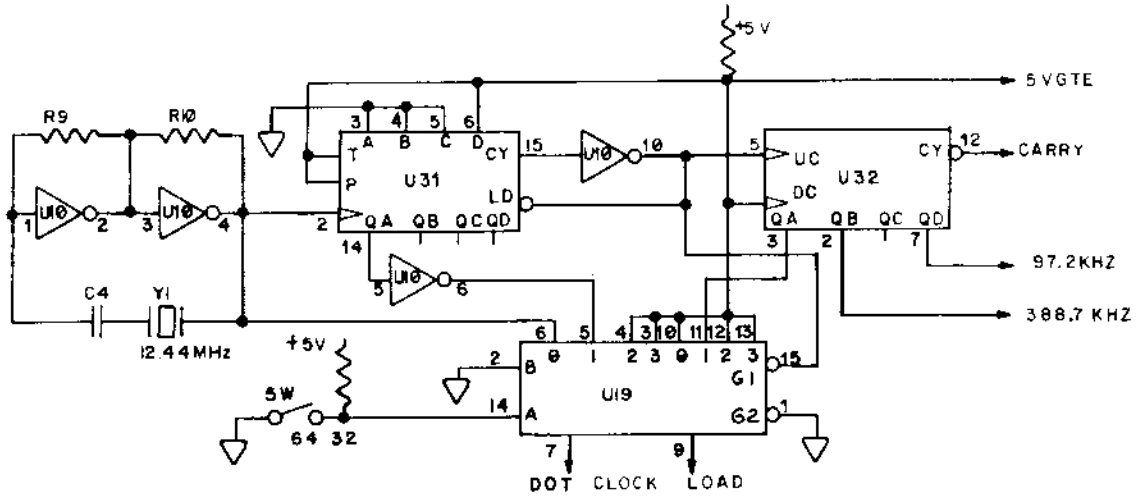
Sixteen lines of characters are produced and either 32 or 64 characters per line may be selected. Total memory consists of eight 1024-bit RAMs. Ten of the computer's memory address lines are connected to these RAMs through decoders, allowing the computer to selectively address each display position. The computer's remaining 6 address lines are used to set the starting address of the board within the entire memory space, as determined by DIP switch S1.

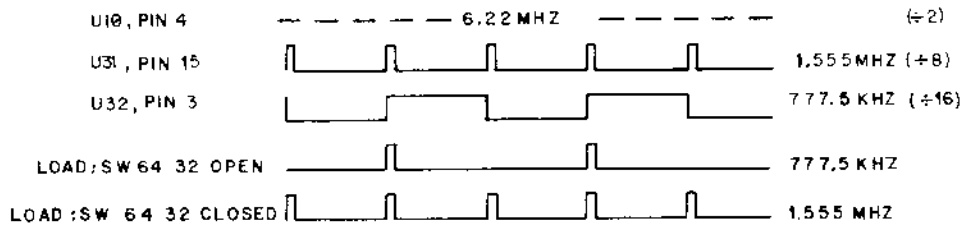
5.2 SYNC GENERATION

Figure 3 shows the 12.44 MHz crystal oscillator feeding two counters, U31 and U32. Counter U31 divides the 12.44 MHz signal by 8 and passes the resulting 1.5375 MHz signal to U32 for further division by 16. The DOT CLOCK is a square wave timing signal used in shifting out video. The LOAD signal is a pulse occurring once every 8 DOT CLOCKs. Both the DOT CLOCK and the LOAD signal are selected for either 32 or 64 characters-per-line operation. If the '32/64' switch is 'OPEN', the 6.22 MHz from U31 is selected to be the DOT CLOCK. If the '32/64' switch is 'CLOSED', 12.44 MHz from the oscillator is selected. For the LOAD signal, '32/64' switch 'OPEN' (32 characters) selects a 777.5 KHz signal, and '32/64' switch 'CLOSED' (64 characters) selects a +5V level. The LOAD signal is modified by the 1.550 MHz pulse signal from the output of U10 pin 10, to become a series of narrow pulses at either 777.5 KHz (32 characters) or 1.5550 MHz (64 characters).

The 97.2 KHz carry signal from U32 pin 7 is the input for the horizontal timing circuit shown in Figure 4. Both U11 and U20 are used to divide the 97.2 KHz from U32 by 6 to give a horizontal blanking signal at 16.2 KHz. U13 generates a delayed horizontal sync pulse from U21 pin 3, but only during horizontal blanking. U20 develops the horizontal drive signal. Waveforms are shown as aids to troubleshooting in Figures 3 thru 5.

In Figure 5, the BIT SELECTOR CLOCK (16.2 KHz) goes to the bit select counter U29. The outputs from U29 give the row select address for the character generator. When address 1110_2 is reached, U29 is loaded with 0000_2 on the next clock pulse to start a new cycle. The load signal is a negative pulse at 1079.9 Hz which is sent to U12 and vertical line counter U33. In addition to 4 bits of the RAM address, U33 puts out negative pulses at 60 Hz on CY. U12 derives negative pulses at 60 Hz for both VERT





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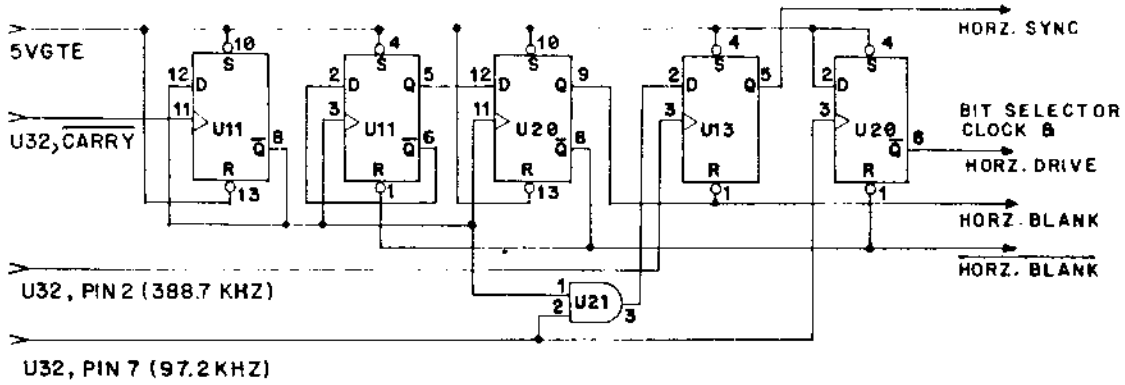
J.M.J. 8-21-80

FIGURE 3



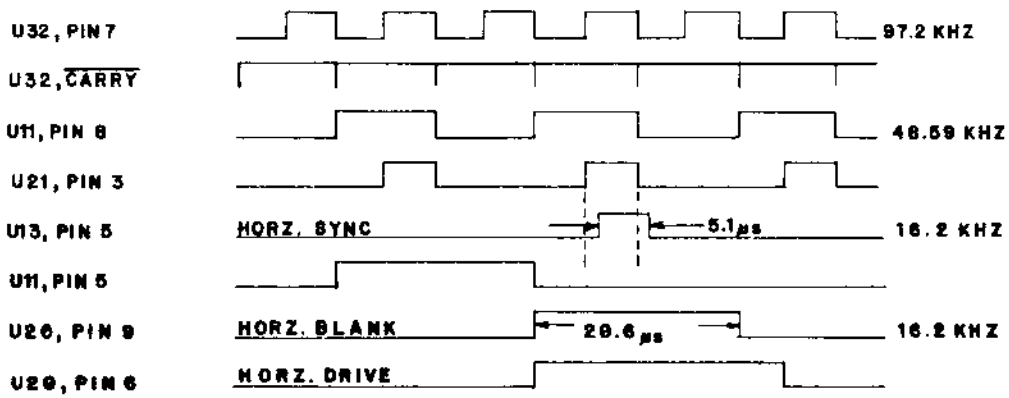
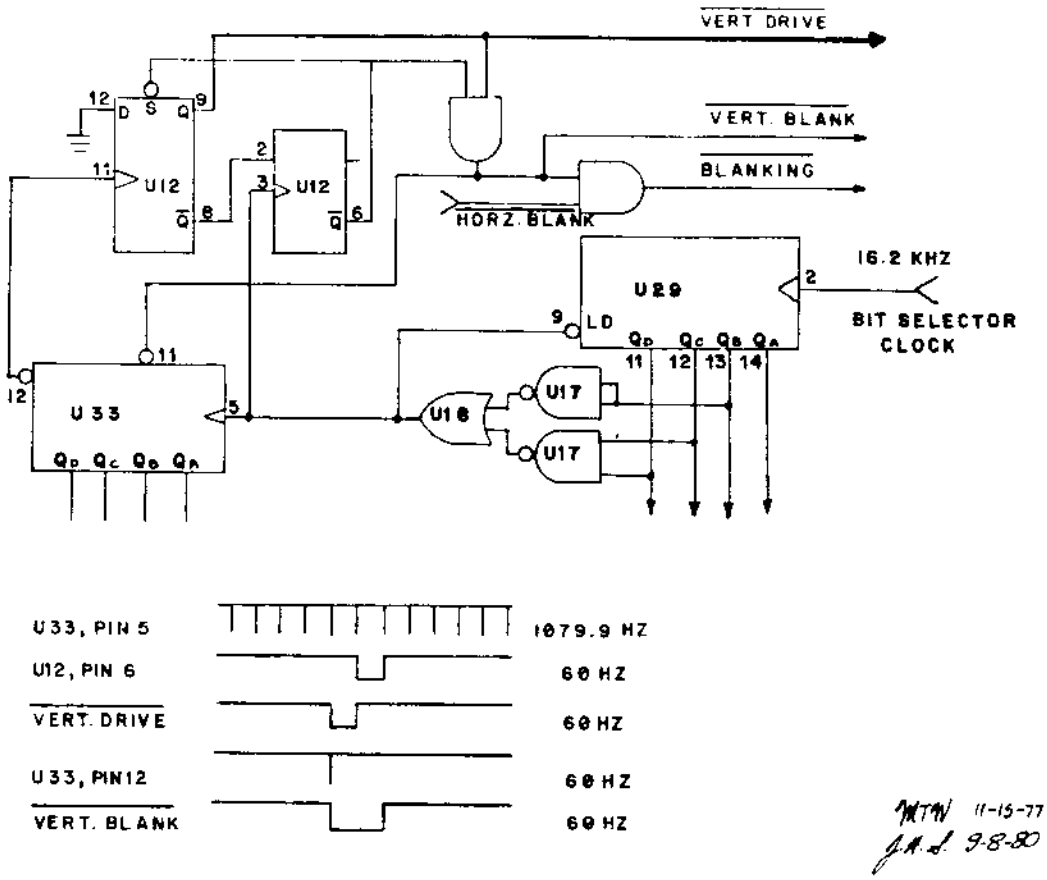


FIGURE 4



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J.M.J. 9-8-80

FIGURE 5

DRIVE (1 ms pulse width) and VERT BLANK (2 ms pulse width). VERT BLANK and HORIZ BLANK are combined by an AND gate to give a composite BLANKING signal. The other 6 bits of RAM address come from counters U14 and U22 which are reset by HORIZ BLANK. U22's clock is the LOAD signal from Figure 3.

5.3 ADDRESSING

The eight 1024-bit RAMs are addressed by the computer using address lines A0 thru A9. Address lines A10 thru A15 form a prefix to specify the board's address. This 6 bit prefix is set by switch S1 positions 3 thru 8; U42 compares the address sent by the computer with the setting of the switch. If the address matches, U42 pin 9 (SELECT) goes low, which actuates the 10 address gates (A0 thru A9), the output gates (DI0 thru DI7), and the write gate U17. When the SELECT signal is low, it also turns off the output gates of counters U14, U22, and U33. With the VB1C memory logically tied to the S-100 bus, the computer can store the data in the video board memory to be displayed. When the address from the computer is no longer valid, the SELECT line goes high and the memory is isolated again.

5.4 PICTURE FORMATION

When in the normal character display mode, the VB1C memory is continually addressed by counters U14, U22, and U33. The memory makes available an 8-bit data word for each location addressed. Only 7 bits go into the character generator to specify a character, or into the multiplexers U5 and U15 for graphics output. The output of the character generator and the output of the graphics multiplexers are sent into two data selectors, U6 and U7. If the GRAPHICS signal is low, U6 and U7 pass the graphics data from U5 and U15. If GRAPHICS is high, U6 and U7 pass the output of the character generator. In either case, the output of U6 and U7 is loaded into parallel-in/serial-out shift register U8. The data is then shifted out to the display monitor. The eighth bit (D7) of VB1C memory is a control bit whose function is determined by the VID REV/GRAPHICS switch (S1-1). When the switch is OPEN, GRAPHICS is high and the output of the character generator goes into parallel-in/serial-out shift register U8. Data bit D7 turns the video reverse on or off by setting U13. This controls the VIDEO REVERSE signal through U2. When VIDEO REVERSE is high, U4 inverts the output which produces a reversed video effect on the monitor.

If the VID REV/GRAPHICS switch is CLOSED, the VIDEO REVERSE signal is low, allowing the output of U8 to pass with no inversion.

Data bit D7 directly controls the GRAPHICS signal. If GRAPHICS is high, the character generator output is selected; if GRAPHICS is low, the graphics data is selected.

5.5 POWER SUPPLIES

A single +5 volt supply is used to operate the VB1C. The standard S-100 voltage of +8V to +10V is regulated by two 7805 regulators to provide the proper voltage on the board. R21 and R22 are power resistors used to keep the power dissipation low in the regulators. The typical current drain is 1.3A.

5.6 BLANKING

Blanking is performed on the VB1C during every CPU read or write operation to the video board's address. U4 pin 11 goes to a logic one each time the VB1C is addressed. U4 pin 11 is buffered by one inverter, U10 pins 12 and 13, to drive an RC timer formed by R24 and C17. The inverter U10 pin 12 provides a blanking signal, with R24 and C17 providing a turn-off delay for increased blanking time.

Blanking is used on the VB1C by forcing the video display to black during CPU accesses. The shift register U8 is cleared (set to black video) during blanking. C17 is discharged and U13 will be set if jumper E2 to E3 (see Section 4.5) has been installed. When the blanking signal is removed (U10 pin 12 goes high), C17 slowly charges to a logic one level and maintains a clear to U8 for an additional time period.

6.0 SOFTWARE

The following 4 programs are provided for use with the VB1C:

1. Video Board Driver
2. Video Board Driver Demonstration Routine
3. Graphics Interface Subroutines
4. Doodle Graphics Demonstration

NOTES:

a. All 4 programs assume the VB1C is addressed at E000-E3FF. This may be changed by altering the value to which 'VID' is EQUated.

b. All programs are written in 8080 assembly language and are executable on a Z-80, 8085, and the 8080.

Two other programs are provided for initial checkout of the VB1C:

1. Video Test Routine
2. Memory Test Routine

NOTE: These two programs assume that the VB1C is addressed at E000-E3FF. In the Video Test Routine this may be changed by altering the value to which 'VID' is EQUated. In the Memory Test program, 'START' specifies the beginning of VB1C memory and 'MEND' specifies the end.

6.1 VIDEO BOARD DRIVER

This is a complete driver routine for the VB1C, including cursor control, clear screen, carriage return, line feed, and cursor addressing.

The driver may be located in ROM or RAM, but three bytes pointed to by VDPTR and VDHLD must be in RAM. Characters to be output are expected in the C register.

```
                ;       VIDEO BOARD DRIVER


                ;       This subroutine facilitates the use
                ;       of the SSM VB1C and a video display
                ;       as a console output device.

                ;       ASCII characters presented to the
                ;       subroutine in the C register are
                ;       displayed on the screen. Certain
                ;       characters, listed below, receive
                ;       special treatment. All registers
                ;       are preserved by this subroutine.

                ;       LOC is the beginning address of the
                ;       subroutine. It may be in RAM or ROM.

3F00 =          LOC     EQU     3F00H

                ;       VID is the beginning address assigned
                ;       to the display RAM located on the VB1C
                ;       board.

E000 =          VID     EQU     0E000H

                ;       Three bytes of RAM are required for
                ;       housekeeping. These bytes must be
                ;       in an area unused by other programs.

3FF8 =          VDPTR   EQU     3FF8H   ;Cursor pointer
3FFA =          VDHLD   EQU     VDPTR+2 ;Character hold


                ;       Non-displayable characters

001A =          CS      EQU     1AH     ;Control Z
                                        ;Clear screen, home cursor
000E =          NL      EQU     0EH     ;Control N
                                        ;Down one line, clear line
000D =          CR      EQU     0DH     ;Carriage return
                                        ;Move cursor to the left margin


                ;       Optional cursor control characters

000B =          UP      EQU     0BH     ;Control K
000A =          DN      EQU     0AH     ;Control J
000C =          FW      EQU     0CH     ;Control L
0008 =          BK      EQU     08H     ;Control H
001E =          HM      EQU     1EH     ;Control ^
```

```
                ;       NORMAL ENTRY POINT

3F00                    ORG     LOC

3F00 E5         VDTTY:  PUSH    HL      ;Save HL
3F01 21F83F             LXI     H,VDPTR ;Address of cursor pointer

                ;       ALTERNATE ENTRY POINT
                ;       This entry point may be used if
                ;       the cursor pointer and character
                ;       hold are at locations other than
                ;       those specified on this listing.
                ;       The user must supply subroutine
                ;       entry code as follows:

                ;ENTR:  PUSH    H       ;Save HL
                ;       LXI     H,PNTR  ;Address of cursor pointer
                ;       JMP     ALTVD   ;Join this code

3F04 D5         ALTVD:  PUSH    D       ;Save DE
3F05 C5                 PUSH    B       ;Save BC
3F06 F5                 PUSH    PSW     ;Save AF
3F07 5E                 MOV     E,M     ;LPTR
3F08 23                 INX     H       ;
3F09 7E                 MOV     A,M     ;HPTR
3F0A E603               ANI     3       ;Convert to video
3F0C C6E0               ADI     VID SHR 8 ;RAM address
3F0E 57                 MOV     D,A
3F0F 23                 INX     H
3F10 46                 MOV     B,M     ;Character under cursor
3F11 EB                 XCHG            ;Pointer to HL
3F12 70                 MOV     M,B     ;Restore previous character

                ;       Identify input character

3F13 79                 MOV     A,C     ;New character
3F14 FE1A               CPI     CS
3F16 CA763F             JZ      VIDFF   ;Form feed
3F19 FE0D               CPI     CR
3F1B CA843F             JZ      VIDCR   ;Carriage return
3F1E FE0E               CPI     NL
3F20 CA8B3F             JZ      VIDLF   ;Line feed

                ;       The following instructions
                ;       (marked YYYY) may be removed
                ;       if cursor control is not
                ;       required.

3F23 FE0B               CPI     UP      ;YYYY
3F25 CADE3F             JZ      CRUP    ;YYYY
3F28 FE0A               CPI     DN      ;YYYY
3F2A CAE43F             JZ      CRDN    ;YYYY
```

```
3F2D FE0C               CPI     FW      ;YYYY
3F2F CA4C3F             JZ      CRRT    ;YYYY
3F32 FE08               CPI     BK      ;YYYY
3F34 CAEA3F             JZ      CRLT    ;YYYY
3F37 FE1E               CPI     HM      ;YYYY
3F39 CAF03F             JZ      CRHM    ;YYYY

                                ;       Displayable Characters

                        ;       The following instructions
                        ;       (marked XXXX) may be removed
                        ;       if sense switches are not
                        ;       to be used.

                        ;       Check for end of line

3F3C 7D                 MOV     A,L     ;XXXX
3F3D E63F               ANI     3FH     ;XXXX
3F3F FE3F               CPI     3FH     ;XXXX
3F41 C24B3F             JNZ     VIDB0   ;XXXX

                        ;       Ignore character if end of line
                        ;       and sense switch 2 equals a one

3F44 DBFF               IN      0FFH    ;XXXX
3F46 E602               ANI     2       ;XXXX
3F48 CA623F             JZ      VIDRT   ;XXXX
3F4B 71         VIDB0:  MOV     M,C
3F4C 010100     CRRT:   LXI     B,1

                        ;       Adjust cursor pointer

3F4F 09         CRADJ:  DAD     B

                        ;       Check for overflow

3F50 7C                 MOV     A,H
3F51 FEE4               CPI     (VID+1024) SHR 8
3F53 C2623F             JNZ     VIDRT
3F56 26E3               MVI     H,(VID+960) SHR 8
3F58 7D                 MOV     A,L
3F59 F6C0               ORI     0C0H
3F5B 6F                 MOV     L,A
3F5C CDB53F             CALL    ROLL0
3F5F C3683F             JMP     VIDR1

                        ;       Common exit code
                        ;       Normalize cursor pointer

3F62 7C         VIDRT:  MOV     A,H
3F63 E603               ANI     3
3F65 C6E0               ADI     VID SHR 8
```

```
3F67 67                 MOV     H,A
3F68 7E         VIDRL:  MOV     A,M     ;Character under cursor
3F69 367F               MVI     M,7FH   ;Cursor
3F6B EB                 XCHG            ;Pointer to DE
3F6C 77                 MOV     M,A     ;Character under cursor
3F6D 2B                 DCX     H
3F6E 72                 MOV     M,D     ;H pointer
3F6F 2B                 DCX     H
3F70 73                 MOV     M,E     ;L pointer

                ;       Restore registers and exit

3F71 F1                 POP     PSW
3F72 C1                 POP     B
3F73 D1                 POP     D
3F74 E1                 POP     H
3F75 C9                 RET

                ;       Process form feed
                ;       Fill screen with spaces
                ;       Move cursor to top left

3F76 2100E0     VIDFF:  LXI     H,VID
3F79 E5                 PUSH    H
3F7A 3620       VIDFC:  MVI     M,' '
3F7C 23                 INX     H
3F7D 7C                 MOV     A,H
3F7E FEE4               CPI     (VID+1024) SHR 8
3F80 FA7A3F             JM      VIDFC
3F83 E1                 POP     H

                ;       Process carriage return
                ;       Move cursor to the beginning
                ;       of the line

3F84 7D         VIDCR:  MOV     A,L
3F85 E6C0               ANI     0C0H
3F87 6F                 MOV     L,A
3F88 C3623F             JMP     VIDRT

                ;       Process line feed
                ;       Move cursor down one line,
                ;       Fill new line with spaces

3F8B D5         VIDLF:  PUSH    D
3F8C 114000             LXI     D,64
3F8F 19                 DAD     D
3F90 7C                 MOV     A,H
3F91 FEE4               CPI     (VID + 1024) SHR 8
3F93 C2CC3F             JNZ     VDLF3
```

```
                ;       Delay before wrapping
                ;       around screen

3F96 E5                 PUSH    H
3F97 210080             LXI     H,8000H
3F9A 2B         VDLF1:  DCX     H
3F9B 7C                 MOV     A,H
3F9C B5                 ORA     L
3F9D C29A3F             JNZ     VDLF1
3FA0 E1                 POP     H

                ;       The following instruction
                ;       (marked XXXX) may be removed
                ;       if sense switches are not
                ;       to be used

                ;       Wait until sense switch 1 equals
                ;       a one before wrap around

3FA1 DBFF       VDLF2:  IN      0FFH    ;XXXX
3FA3 E601               ANI     1       ;XXXX
3FA5 CAA13F             JZ      VDLF2   ;XXXX

                ;       Roll the whole display up one
                ;       line

3FA8 CDB53F             CALL    ROLL0
3FAB 7D                 MOV     A,L
3FAC F6C0               ORI     0C0H
3FAE 6F                 MOV     L,A
3FAF 26E3               MVI     H,(VID+960) SHR 8
3FB1 D1                 POP     D
3FB2 C3623F             JMP     VIDRT

                ;       Roll subroutine

3FB5 D5         ROLL0:  PUSH    D
3FB6 E5                 PUSH    H
3FB7 1100E0             LXI     D,VID
3FBA 2140E0             LXI     H,VID+64
3FBD 7E         ROLL1:  MOV     A,M
3FBE 12                 STAX    D
3FBF 3620               MVI     M,20H
3FC1 13                 INX     D
3FC2 23                 INX     H
3FC3 7C                 MOV     A,H
3FC4 FEE4               CPI     (VID+1024) SHR 8
3FC6 C2BD3F             JNZ     ROLL1
3FC9 E1                 POP     H
3FCA D1                 POP     D
3FCB C9                 RET
```

```
                ;       Fill new line with spaces

3FCC E5         VDLF3:  PUSH    H
3FCD 7D                 MOV     A,L
3FCE E6C0               ANI     0C0H
3FD0 6F                 MOV     L,A
3FD1 3620       VDLF4:  MVI     M,' '
3FD3 23                 INX     H
3FD4 7D                 MOV     A,L
3FD5 1D                 DCR     E
3FD6 C2D13F             JNZ     VDLF4
3FD9 E1                 POP     H
3FDA D1                 POP     D
3FDB C3623F             JMP     VIDRT


                ;       The following instructions,
                ;       along with those marked
                ;       YYYY above, may be removed
                ;       if cursor control is not
                ;       required.

                ;       Cursor control processing

3FDE 01C0FF     CRUP:   LXI     B,-64   ;YYYY
3FE1 C34F3F             JMP     CRADJ   ;YYYY
3FE4 014000     CRDN:   LXI     B,64    ;YYYY
3FE7 C34F3F             JMP     CRADJ   ;YYYY
3FEA 01FFFF     CRLT:   LXI     B,-1    ;YYYY
3FED C34F3F             JMP     CRADJ   ;YYYY
3FF0 210000     CRHM:   LXI     H,0     ;YYYY
3FF3 C3623F             JMP     VIDRT   ;YYYY

3FF6                    END
```

6.2 VIDEO BOARD DRIVER DEMONSTRATION ROUTINE

This routine in conjunction with the Video Board Driver can be used to create a "glass teletype".

NOTES:

a. The console assignments are defined in the following manner:

Status Port:	00H
Data Port:	01H
Data Available Bit:	01H

b. The routine must be located in RAM.

```
                ;       VDTTY DEMONSTRATION ROUTINE

                ;       LOC is the beginning address of the
                ;       routine. It must be in RAM.

3E00 =          LOC     EQU     3E00H

                ;       VID is the beginning address assigned
                ;       to the display RAM located on the VB1C
                ;       board.

E000 =          VID     EQU     0E000H

                ;       VDTTY is the video driver
                ;       routine.

3F00 =          VDTTY   EQU     3F00H

3E00 =          STACK   EQU     3E00H

                ;       Non-displayable characters

001B =          INV     EQU     1BH     ;Escape
001A =          CS      EQU     1AH     ;Control Z
000E =          NL      EQU     0EH     ;Control N
000D =          CR      EQU     0DH     ;Carriage return
000B =          UP      EQU     0BH     ;Control K
000A =          DN      EQU     0AH     ;Control J
000C =          FW      EQU     0CH     ;Control L
0008 =          BK      EQU     08H     ;Control H
001E =          HM      EQU     1EH     ;Control ^

                ;       Console Assignments
```

```
0000 =          CSTAT   EQU     00H     ;Console status port
0001 =          CDATA   EQU     01H     ;Console data port
0001 =          DAV     EQU     01H     ;Data available bit

3E00                    ORG     LOC

3E00 31003E     DEMO:   LXI     SP,STACK
3E03 CD4C3E     D1:     CALL    CI
3E06 E67F               ANI     7FH
3E08 4F                 MOV     C,A
3E09 FE1A               CPI     CS
3E0B CA453E             JZ      DISP1
3E0E FE0D               CPI     CR
3E10 CA453E             JZ      DISP1
3E13 FE0E               CPI     NL
3E15 CA453E             JZ      DISP1
3E18 FE0B               CPI     UP
3E1A CA453E             JZ      DISP1


3E1D FE0A               CPI     DN
3E1F CA453E             JZ      DISP1
3E22 FE0C               CPI     FW
3E24 CA453E             JZ      DISP1
3E27 FE08               CPI     BK
3E29 CA453E             JZ      DISP1
3E2C FE1E               CPI     HM
3E2E CA453E             JZ      DISP1
3E31 FE1B               CPI     INV
3E33 3A4B3E             LDA     BIT8
3E36 C2433E             JNZ     DISP
3E39 E680               ANI     80H
3E3B EE80               XRI     80H
3E3D 324B3E             STA     BIT8
3E40 C3033E             JMP     D1
3E43 B1         DISP:   ORA     C
3E44 4F                 MOV     C,A
3E45 CD003F     DISP1:  CALL    VDTTY   ;Call video board driver
3E48 C3033E             JMP     D1
3E4B 00         BIT8:   DB      0

                ;       Console input subroutine

3E4C DB00       CI:     IN      CSTAT   ;Input from status port
3E4E E601               ANI     DAV     ;Test for data available
3E50 C24C3E             JNZ     CI
3E53 DB01               IN      CDATA   ;Input data
3E55 C9                 RET

3E56                    END
```

6.3 GRAPHICS INTERFACE SUBROUTINE

The following graphics program will allow you to utilize the VB1C as a 128 x 48 graphics board.

NOTES:

a. Coordinate 0,0 is in the lower left corner of the display. This is in accordance with an X-Y graph.

b. The routine may be located in ROM or RAM.

```
;       GRAPHICS INTERFACE SUBROUTINES


;       These subroutines facilitate the
;       use of the SSM VB1C board and a
;       video display as a graphics diplay
;       device.

;       These subroutines treat the display
;       screen as a matrix of dots, 48 dots
;       high by 128 dots wide.  Each dot is
;       specified in terms of its vertical
;       coordinate(0-47) and its horizontal
;       coordinate(0-127).  Dot 0,0 is at
;       the lower left corner of the screen.

;       For best results, the display memory
;       should be initialized to 'FF' hex
;       prior to attempting graphics output.

;       ENTRY CONDITIONS:
;               H = VERTICAL COORDINATE
;               L = HORIZONTAL COORDINATE

;       EXIT CONDITIONS
;               A = DIFFERS BY SUBROUTINE
;               B = PRESERVED
;               C = BIT MASK FOR SPECIFIED DOT
;               DE= MEMORY ADDRESS OF DOT
;               H = VERTICAL COORDINATE
;               L = HORIZONTAL COORDINATE

;       H and L are converted(if necessary)
;       MODULO 48 and 128 respectively.
```

```
                        ;       LOC is the beginning address of
                        ;       these subroutines.  It may be in
                        ;       RAM or ROM.

3E80 =          LOC     EQU     3E80H

                        ;       VID is the beginning address assigned
                        ;       to the display RAM located on the VB1C
                        ;       board.

E000 =          VID     EQU     0E000H

3E80                    ORG     LOC


                        ;       The check subroutine sets the zero
                        ;       flag to indicate whether the specified



                        ;       dot is white or black. If the dot
                        ;       is currently, white the zero flag is
                        ;       set on; if the dot is black, the flag
                        ;       is set off.  The A register contains
                        ;       zero if the dot is white,and contains
                        ;       the bit mask if it is black.

3E80 CD9A3E     CHECK:  CALL    CNVRT
3E83 A1                 ANA     C
3E84 C9                 RET

                        ;       The white subroutine sets the
                        ;       specified dot white. Register
                        ;       A contains the new contents of
                        ;       the memory location.

3E85 CD9A3E     WHITE:  CALL    CNVRT   ;Convert
3E88 E6BF               ANI     0BFH    ;Clear unused bit
3E8A F680               ORI     80H     ;Set graphics bit
3E8C B1                 ORA     C       ;Set this dot
3E8D A9                 XRA     C       ;Clear this dot
3E8E 12                 STAX    D       ;Update byte
3E8F C9                 RET

                        ;       The black subroutine sets the
                        ;       specified dot black. Register
                        ;       A contains the new contents of
                        ;       the memory location.

3E90 CD9A3E     BLACK:  CALL    CNVRT   ;Convert
3E93 E6BF               ANI     0BFH    ;Clear unused bit
3E95 F680               ORI     80H     ;Set graphics bit
3E97 B1                 ORA     C       ;Set this dot
3E98 12                 STAX    D       ;Update byte
3E99 C9                 RET
```

```
                ;       The CNVRT subroutine performs
                ;       the coordinate to address-bit
                ;       mask conversion. Register A contains
                ;       the current contents of the memory
                ;       location.

3E9A C5         CNVRT:  PUSH    B

                ;       Normalize the coordinates

3E9B 7D                 MOV     A,L
3E9C E67F               ANI     7FH
3E9E 6F                 MOV     L,A
3E9F 7C                 MOV     A,H
3EA0 D630       D1:     SUI     48
3EA2 F2A03E             JP      D1


3EA5 C630       D2:     ADI     48
3EA7 FAA53E             JM      D2
3EAA 67                 MOV     H,A
3EAB E5                 PUSH    H

                ;       Convert coordinates to address
                ;       in DE

3EAC 44                 MOV     B,H
3EAD 4D                 MOV     C,L
3EAE 5C                 MOV     E,H
3EAF 1600               MVI     D,0
3EB1 210100             LXI     H,1
3EB4 19                 DAD     D
3EB5 29                 DAD     H
3EB6 29                 DAD     H
3EB7 19                 DAD     D
3EB8 29                 DAD     H
3EB9 29                 DAD     H
3EBA 19                 DAD     D
3EBB 54                 MOV     D,H
3EBC 7D                 MOV     A,L
3EBD E6C0               ANI     0C0H
3EBF 5F                 MOV     E,A
3EC0 19                 DAD     D
3EC1 19                 DAD     D
3EC2 29                 DAD     H
3EC3 29                 DAD     H
3EC4 78                 MOV     A,B
3EC5 94                 SUB     H
3EC6 47                 MOV     B,A
3EC7 3EC0               MVI     A,(VID+960) AND 0FFH
3EC9 93                 SUB     E
3ECA 5F                 MOV     E,A
3ECB 3EE3               MVI     A,(VID+960) SHR 8
```

```
3ECD 9A                 SBB     D
3ECE 57                 MOV     D,A
3ECF 79                 MOV     A,C
3ED0 1F                 RAR
3ED1 B3                 ORA     E
3ED2 5F                 MOV     E,A

                ;       GENERATE BIT MASK

3ED3 79                 MOV     A,C
3ED4 1F                 RAR
3ED5 78                 MOV     A,B
3ED6 17                 RAL
3ED7 4F                 MOV     C,A
3ED8 0600               MVI     B,0
3EDA 21E43E             LXI     H,DTAB
3EDD 09                 DAD     B


3EDE 7E                 MOV     A,M

                ;       PREPARE FOR EXIT

3EDF E1                 POP     H
3EE0 C1                 POP     B
3EE1 4F                 MOV     C,A
3EE2 1A                 LDAX    D
3EE3 C9                 RET

3EE4 04         DTAB:   DB      04H
3EE5 20                 DB      20H
3EE6 02                 DB      02H
3EE7 10                 DB      10H
3EE8 01                 DB      01H
3EE9 08                 DB      08H

3EEA                    END
```

6.4 DOODLE GRAPHICS DEMONSTRATION

This routine, when used in conjunction with the graphics interface subroutine, will provide the user with an electronic drawing board.

NOTES:

a. The Graphics Interface Subroutine must be present beginning at location 3E80H. This may be changed by altering the values to which 'CHECK', 'WHITE', and 'BLACK' are EQUated.

b. The console assignments are defined in the following manner:

Status Port:	00H
Data Port:	01H
Data Available Bit:	01H

```
                ;       DOODLE (GRAPHICS DEMO)

E000 =          VID     EQU     0E000H  ;Address of VBIC
3E00 =          STACK   EQU     3E00H   ;Set stack
3E80 =          CHECK   EQU     3E80H   ;Black/white check routine
3E85 =          WHITE   EQU     3E85H   ;Routine to set dot white
3E90 =          BLACK   EQU     3E90H   ;Routine to set dot black

                ;       Console Assignments
0000 =          CSTAT   EQU     00H     ;Console status port
0001 =          CDATA   EQU     01H     ;Console data port
0001 =          DAV     EQU     01H     ;Data available bit

3D00                    ORG     3D00H
3D00 31003E     DOODL:  LXI     SP,STACK

                ;       Clear video screen
3D03 2100E0             LXI     H,VID
3D06 36BF       D0:     MVI     M,0BFH
3D08 23                 INX     H
3D09 7C                 MOV     A,H
3D0A FEE4               CPI     (VID+1024) SHR 8
3D0C C2063D             JNZ     D0
3D0F C3153D             JMP     D2

3D12 22CD3D     D1:     SHLD    CURS
3D15 2ACD3D     D2:     LHLD    CURS
3D18 CD803E             CALL    CHECK
3D1B 1A                 LDAX    D
3D1C F680               ORI     80H
3D1E 32CF3D     D3:     STA     OLD

                ;       Flash cursor
3D21 3ACF3D     D4:     LDA     OLD
3D24 A9                 XRA     C
3D25 12                 STAX    D
3D26 0610               MVI     B,10H
3D28 CDBB3D             CALL    WAIT
3D2B C23A3D             JNZ     D5      ;Exit  if keyboard typed
3D2E 3ACF3D             LDA     OLD
3D31 12                 STAX    D
3D32 0620               MVI     B,20H
3D34 CDBB3D             CALL    WAIT
3D37 CA213D             JZ      D4

3D3A 3ACF3D     D5:     LDA     OLD
3D3D 12                 STAX    D
3D3E CDD03D             CALL    CI      ;Get ASCII character
3D41 FE42               CPI     'B'     ;Black?
3D43 CA743D             JZ      BLK
3D46 FE57               CPI     'W'     ;White?
3D48 CA7A3D             JZ      WHT
```

```
3D4B FE53              CPI     'S'     ;Save command?
3D4D CA803D            JZ      SAVE
3D50 FE47              CPI     'G'     ;Get command?
3D52 CA863D            JZ      GET
3D55 2C                INR     L
3D56 FE52              CPI     'R'     ;Move right?
3D58 CA123D            JZ      D1
3D5B 2D                DCR     L
3D5C 2D                DCR     L
3D5D FE4C              CPI     'L'     ;Move left?
3D5F CA123D            JZ      D1
3D62 2C                INR     L
3D63 24                INR     H
3D64 FE55              CPI     'U'     ;Move up?
3D66 CA123D            JZ      D1
3D69 25                DCR     H
3D6A 25                DCR     H
3D6B FE44              CPI     'D'     ;Move down?
3D6D CA123D            JZ      D1
3D70 24                INR     H
3D71 C3153D            JMP     D2

3D74 CD903E    BLK:    CALL    BLACK
3D77 C3153D            JMP     D2

3D7A CD853E    WHT:    CALL    WHITE
3D7D C3153D            JMP     D2

3D80 CD903D    SAVE:   CALL    NUM
3D83 C38A3D            JMP     SG

3D86 CD903D    GET:    CALL    NUM
3D89 EB                XCHG

3D8A CDAA3D    SG:     CALL    MOVE
3D8D C3153D            JMP     D2

               ;       Get a number between
               ;       0 & 9
3D90 CDD03D    NUM:    CALL    CI
3D93 D630              SUI     '0'
3D95 FA903D            JM      NUM
3D98 FE0A              CPI     10
3D9A F2903D            JP      NUM
3D9D 67                MOV     H,A
3D9E 2E00              MVI     L,0
3DA0 29                DAD     H
3DA1 29                DAD     H
3DA2 110004            LXI     D,STORE
3DA5 19                DAD     D
3DA6 1100E0            LXI     D,VID
3DA9 C9                RET
```

```
                        ;       Move a block of memory
3DAA 0604       MOVE:   MVI     B,4
3DAC 1A         MV1:    LDAX    D
3DAD E6BF               ANI     0BFH
3DAF 77                 MOV     M,A
3DB0 13                 INX     D
3DB1 2C                 INR     L
3DB2 C2AC3D             JNZ     MV1
3DB5 24                 INR     H
3DB6 05                 DCR     B
3DB7 C2AC3D             JNZ     MV1
3DBA C9                 RET

                        ;       Check keyboard & delay
3DBB C5         WAIT:   PUSH    B
3DBC CDDC3D     W1:     CALL    CSTS
3DBF B7                 ORA     A
3DC0 C2CB3D             JNZ     W2
3DC3 0D                 DCR     C
3DC4 C2BC3D             JNZ     W1
3DC7 05                 DCR     B
3DC8 C2BC3D             JNZ     W1
3DCB C1         W2:     POP     B
3DCC C9                 RET

3DCD 0000       CURS:   DW      0
3DCF 00         OLD:    DB      0

                        ;       CONSOLE INPUT SUBROUTINE

3DD0 DB00       CI:     IN      CSTAT   ;Check status
3DD2 E601               ANI     DAV     ;Is data available?
3DD4 C2D03D             JNZ     CI
3DD7 DB01               IN      CDATA   ;Get character
3DD9 E67F               ANI     7FH     ;Strip parity
3DDB C9                 RET

                        ;       CONSOLE STATUS SUBROUTINE

3DDC DB00       CSTS:   IN      CSTAT   ;Check status
3DDE E601               ANI     DAV     ;Is data available?
3DE0 D601               SUI     1
3DE2 9F                 SBB     A       ;Set flag
3DE3 C9                 RET

0400                    ORG     1024

0400            STORE:  DS      10240   ;Space for ten
                                        ;graphics pictures
                                        ;1024 bytes each
2C00                    END
```

6.5 VIDEO TEST ROUTINE

The following is a short program to display the character set plus the 64 different graphic characters available on the VBIC.

```
                ;       This simple program was designed to display
                ;       the output of the SSM VBIC video interface
                ;       board.

                ;       Written by David Bruce Maerzke

                ;       The upper half of the display shows the 64
                ;       unique graphic characters while the lower
                ;       half displays the ASCII character set.

                ;       NOTE: To select graphics mode the graphics
                ;       position of the dip switch, S1, must be
                ;       closed and data bit D7 set to a one.

E000 =          VID     EQU     0E000H  ;Video RAM address

0100                    ORG     100H    ;Starting address of routine

0100 2100E0             LXI     H,VID
0103 3EF0               MVI     A,0F0H
0105 06FF               MVI     B,0FFH
0107 BC         LOOP1:  CMP     H
0108 CA1001             JZ      PROG
010B 70                 MOV     M,B
010C 23                 INX     H
010D C30701             JMP     LOOP1
0110 2100E0     PROG:   LXI     H,VID
0113 0E09               MVI     C,09H
0115 3EFF               MVI     A,0FFH
0117 114000     LOOP2:  LXI     D,40H
011A 19                 DAD     D
011B 0D                 DCR     C
011C CA1C01     STUCK:  JZ      STUCK
011F 77         LOOP3:  MOV     M,A
0120 23                 INX     H
0121 23                 INX     H
0122 3D                 DCR     A
0123 1D                 DCR     E
0124 1D                 DCR     E
0125 CA1701             JZ      LOOP2
0128 C31F01             JMP     LOOP3
012B                    END
```

6.6 MEMORY TEST ROUTINE

The following memory test program performs a rotating bit test. If memory is good, location 'GORB' will contain a 00H. If memory fails, 'GORB' will contain the pattern that failed.

Location 'LAST' will be equal to 'MEND' if memory passes without an error. If memory fails, it will be equal to the address last tested.

```
                ;       Simple Memory Test
                ;       Written by Andrew Schneider
                ;       Modified by Malcolm Wright
                ;       Copyright 1977 by SSM

                ;       Set "START" to the starting address of
                ;       memory to be tested. Set "MEND" to the last
                ;       address of memory to be checked.

                ;       The program will stop (HALT) when complete
                ;       or if an error was found. "GORB" (good or
                ;       bad) will be set to 00H for good memory or
                ;       to the byte pattern that would not read or
                ;       write correctly into memory. "LAST" is the
                ;       location where the last address tested will
                ;       be saved. If memory is good, then LAST=MEND.

0100 =          BEGIN   EQU     0100H   ;Start of program
E000 =          START   EQU     0E000H  ;Beginning address
E3FF =          MEND    EQU     0E3FFH  ;Ending address

0100                    ORG     BEGIN
0100 2100E0             LXI     H,START
0103 11FFE3             LXI     D,MEND
0106 2B                 DCX     H
0107 23         LOOP:   INX     H
0108 3E7F               MVI     A,7FH
010A 07         CHECK:  RLC
010B 77                 MOV     M,A
010C BE                 CMP     M
010D C22001             JNZ     ERROR
0110 B7                 ORA     A
0111 FA0A01             JM      CHECK
0114 7B                 MOV     A,E
0115 BD                 CMP     L
0116 C20701             JNZ     LOOP
0119 7A                 MOV     A,D
011A BC                 CMP     H
011B C20701             JNZ     LOOP
011E 3E00               MVI     A,0
0120 322701     ERROR:  STA     GORB    ;If using an IMSAI front panel
                                        ;replace with       CMA
                                        ;                   OUT  0FFH
                                        ;to display byte on front panel.
0123 222801             SHLD    LAST
0126 76                 HLT
0127 00         GORB:   DB      0
0128 0000       LAST:   DW      0
012A                    END
```

7.0 TROUBLESHOOTING HINTS

1. Check for proper settings of the DIP switch.

2. Verify that all IC's are in the correct sockets.

3. Visually inspect all IC's to be sure that all leads are in the sockets. Be sure that the lead isn't under the IC or bent out from the socket.

4. Verify that the output voltage of each regulator is correct.

5. Inspect the back side of the board for solder bridges. If a trace looks suspicious, run a knife blade between the two traces.

6. If you have an addressing problem:

   a. Check U42 (8131) for addresses A10 thru A15.
   b. Check the inputs and outputs of address buffers U23, U35, and U40 for shorts as well as proper operation.

7. If you have problems with data output (consistent missing bits):

   a. Check inputs and outputs of buffers U28, U40, and U41 for shorts as well as proper operation.
   b. Check memory chips U24 thru U27, and U36 thru U39.

8. If you have a problem with horizontal sync:

   a. Check signals on U20, U31, U32, U19, and U10.

9. If you have a problem with vertical sync:

   a. Check signals on U12, U33, U29, and U17.

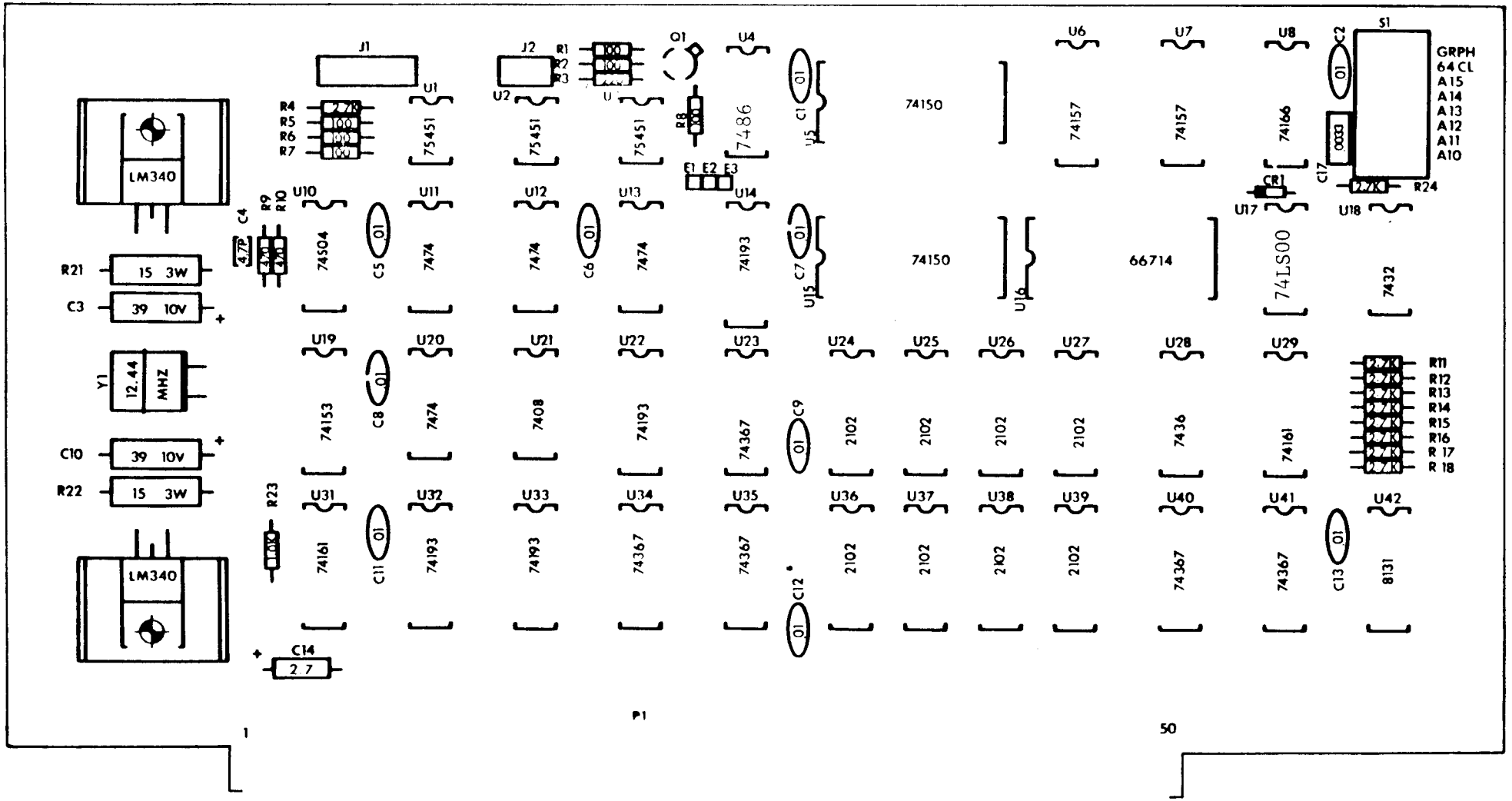
8.0 WARRANTY

SSM warrants its products to be free from defects in materials and/or workmanship for a period of ninety (90) days for kits and bare boards and one (1) year for factory assembled boards. In the event of malfunction or other indication of failure attributable directly to faulty workmanship and/or material, then, upon return of the product (postage paid) to SSM at 2190 Paragon Drive, San Jose, California 95131, "Attention: Warranty Claims Department", SSM will, at its option, repair or replace the defective part or parts to restore said product to proper operating condition. All such repairs and/or replacements shall be rendered by SSM without charge for parts or labor when the product is returned within the specified period of the date of purchase. This warranty applies only to the original purchaser.

This warranty will not cover the failure of SSM products which at the discretion of SSM shall have resulted from accident, abuse, negligence, alteration, or misapplication of the product. While every effort has been made to provide clear and accurate technical information on the application of SSM products, SSM assumes no liability in any events which may arise from the use of said technical information.

This warranty is in lieu of all other warranties, expressed or implied, including warranties of mercantability and fitness for use. In no event will SSM be liable for incidental and consequential damages arising from or in any way connected with the use of its products. Some states do not allow the exclusion or limitation of incidental or consequential damages, so the above limitation or exclusion may not apply to you.

IMPORTANT: Proof of purchase is necessary for products returned for repair under warranty. Before returning any product, please call our Customer Service Department for a return authorization number.



ASSEMBLY DRAWING

VBIC

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PARTS LIST

CHIP PACK

1	U17	74LS00	quad 2-input NAND gate
1	U10	74S04	hex inverter
1	U21	7408	quad 2-input AND gate
1	U18	7432	quad 2-input OR gate
4	U11,12,13,20	7474	dual D-type flip-flop
1	U4	7486	quad 2-input exclusive-OR
2	U5,15	74150	1-of-16 data multiplexer
1	U19	74153	dual 4-to-1 data multiplexer
2	U6,7	74157	quad 2-to-1 data multiplexer
1	U8	74166	8-bit shift register
4	U14,22,32,33	74LS193	binary up/down counter
2	U29,31	74161	binary 4-bit counter
6	U23,28,34,35,40,41	743677	hex bus driver
3	U1,2,3	75451	dual positive AND driver
1	U42	8131	6-bit comparator
1	S1	8 position DIP switch	

MEMORY PACK

1	U16	66714	Character generator
8	U24-27,36-39	21L02-2	1K x 1-bit static RAM

RESISTOR PACK

2	R21,22	15 ohm 3W	(no color code)
6	R1,2,5,6,7,8	100 ohm 1/4W 5%	(brown,black,brown)
1	R3	220 ohm 1/4W 5%	(red,red,brown)
2	R9,10	470 ohm 1/4W 5%	(yellow,violet,brown)
1	R23	1K ohm 1/4W 5%	(brown.black,red)
10	R4,11-18,24	2.7K ohm 1/4W 5%	(red,violet,red)

CAPACITOR PACK

1	C4	56 pf disc radial
1	C17	.0033 uf monolithic radial
10	C1,2,5,6,7,8,9,11,12,13	.1 uf monolithic filter capacitor
2	C3,10	10 uf 25V axial tantalum
1	C14	4.7 uf 20V axial electrolytic

DIODE PACK

1	Q1	2N3904
1	CR1	1N270

REGULATOR PACK

2	U9,30	7805 +5 volt regulators
1	Y1	12.44 MHz crystal
1		3x1 header strip
2		heatsinks
2		#6 hardware sets
1		mini-jumper

MOLEX PACK

1	J1	2 pin molex male connector
1	J2	4 pin molex male connector
1		2 pin molex shell
1		4 pin molex shell
6		molex pins

SOCKET PACK

3	8-pin sockets
9	14-pin sockets
3	24-pin sockets

MISCELLANEOUS PACK

25	16-pin sockets

MISCELLANEOUS

1	VB1C PC board
1	VB1C Instruction Manual
1	Warranty card

VB1C MANUAL REGISTRATION FORM

In our effort to continually upgrade our documentation, we would appreciate any feedback you may have concerning this manual. Please mail your comments and suggestions to SSM Customer Service at the address below.

COMMENTS AND CORRECTIONS ON THE SSM VB1C INSTRUCTION MANUAL

VB1C Serial Number _____

Name _____

Title _____

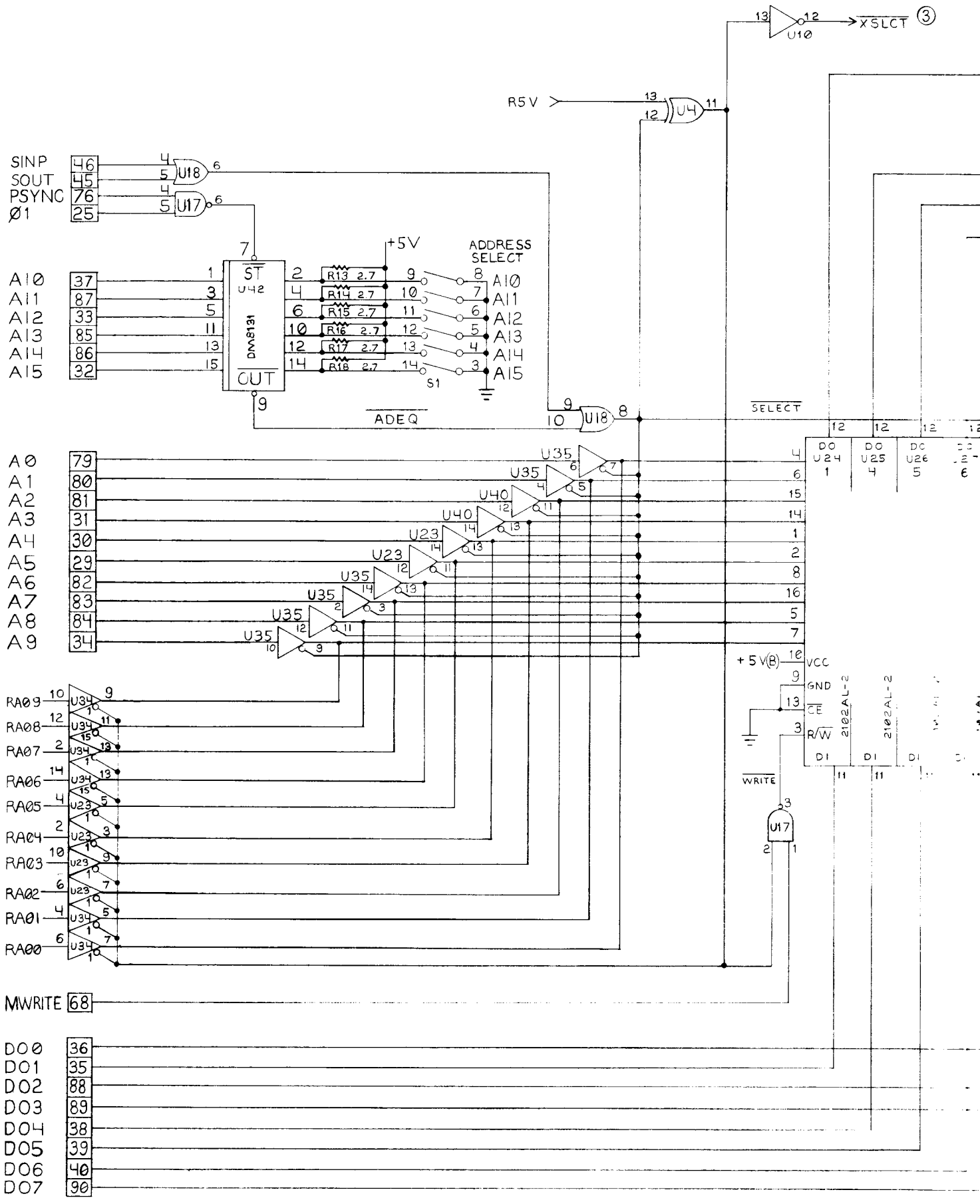
Company _____

Address _____

_____

Telephone (_____)_____

SEND TO: SSM MICROCOMPUTER PRODUCTS, INC.
2190 Paragon Drive
San Jose, California 95131
Attention: Customer Service Department



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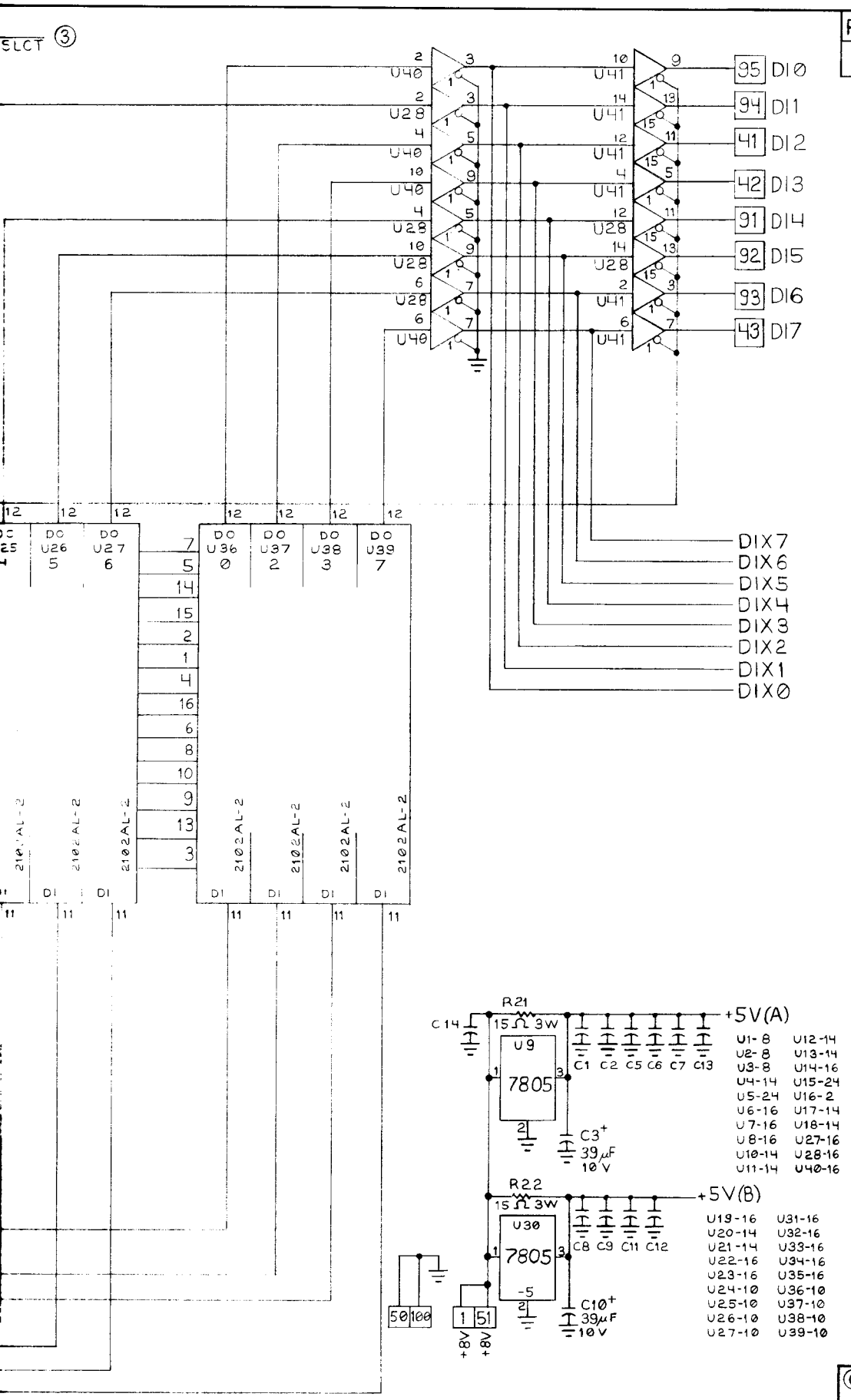
A	PRODUCTION RELEASE



③ SEE PAGE 2

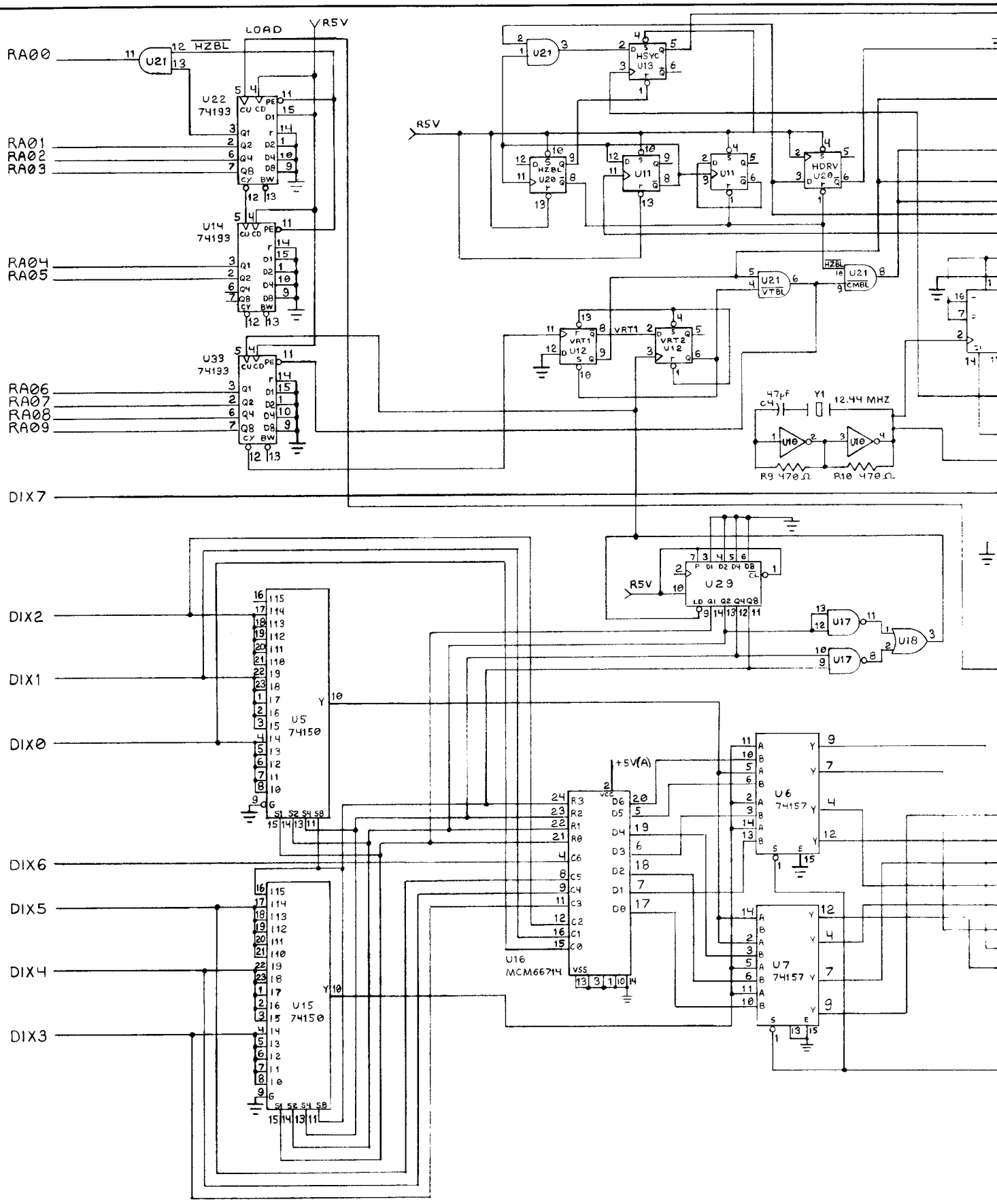
NOTES:
1. ALL RESISTORS ARE IN K OHMS UNLESS OTHERWISE NOTED.
2. ALL CAPACITORS ARE IN MICRO-FARADS UNLESS OTHERWISE NOTED.

SCALE: NONE	APPROVED BY: CHECKER: BS	DRAWN BY: J.A.T.	
DATE: 8-15-80	ENG: MTM MKT. & SALES: CS	REVISED	

SCHEMATIC, VIDEO INTERFACE — S-100

SHEET: 1 OF: 2

DRAWING NUMBER 1001-002

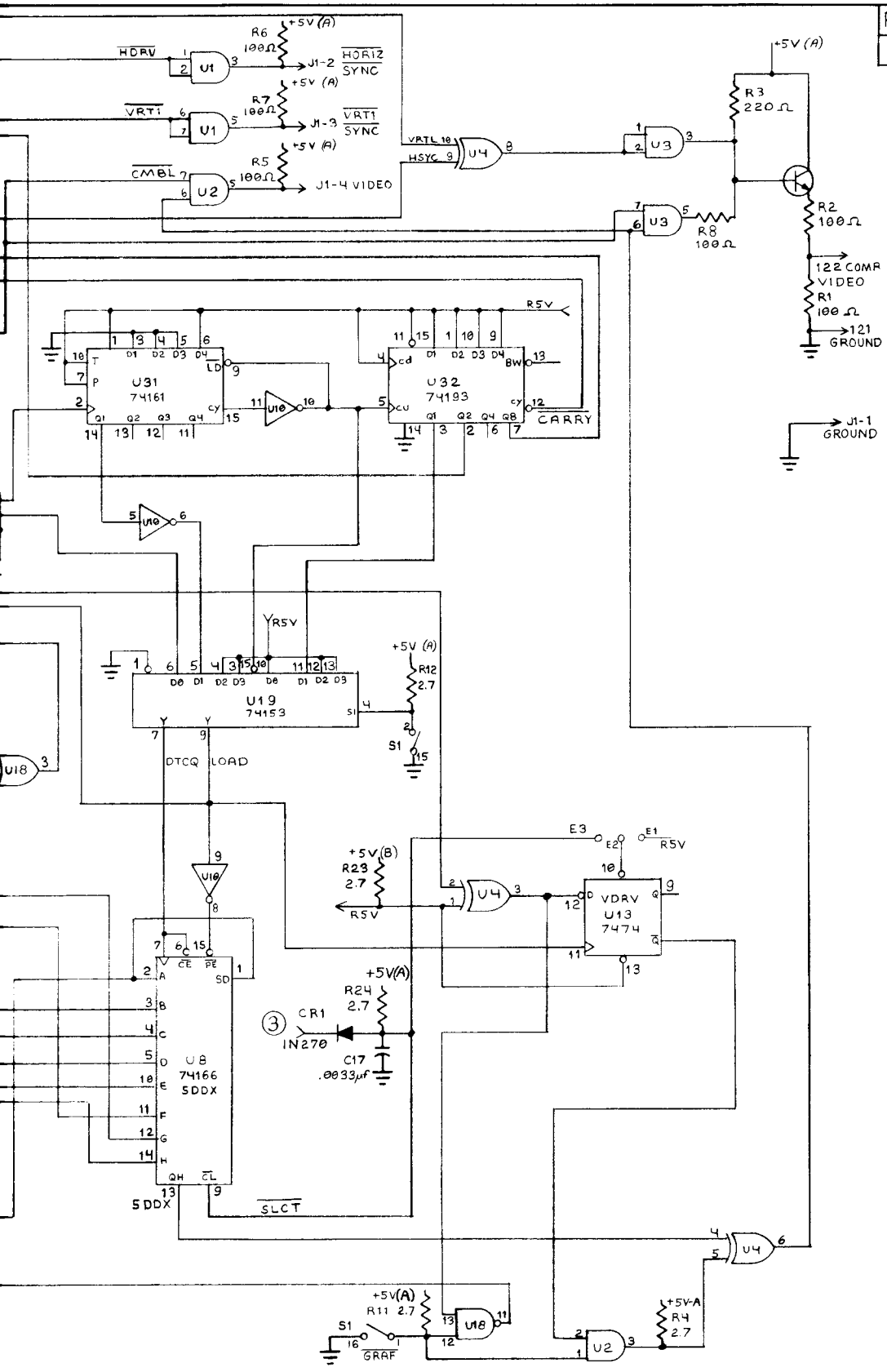


NOTES:

1. ALL RESISTORS ARE IN K OHMS UNLESS OTHERWISE NOTED.
2. ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE NOTED.

(3) CR1, $\overline{\text{SLCT}}$ FROM PAGE 1, U10, PIN 12, $\overline{\text{SLCT}}$.

REV.	DESCRIPTION
A	PRODUCTION RELEASE



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SCHEMATIC, VIDEO INTERFACE - S 100

SHEET: 2 OF: 2

DRAWING NUMBER 1001-002