MB64

64K Static RAM Board

User's Manual

MB64™ 64K STATIC RAM
S-100 Bus

USER'S MANUAL

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APPENDIX:

1.0 INTRODUCTION

The SSM MB64 represents a significant advance in low-cost, high-density, static memory boards. It incorporates such features as bank select, extended addressing, diagnostic LEDs, and a provision for battery backup.

The MB64 is configurable as two 32K byte bank-switched memory blocks, or 64K bytes of memory with standard or extended addressing. The MB64 can be disabled in 2K increments by the use of a Magic Mapping™ circuit to provide memory space for other memory-mapped devices within the computer system. This board is equipped to sense the phantom disable line to prevent hardware conflicts with auxiliary system boot ROMs on another 696 compatible board.

Features:

- Two 32K byte memory blocks
- Low power CMOS RAM chips (HM6116P)
- High speed access, approximately 150 nsec.
- Bank switching circuity to support MP/M, CROMIX, OASIS, etc.
- Extended addressing to support IEEE 696 products
- LED indicators for RAM select and bank select
- Low power consumption of less than 300 ma typical
- Up to 8K of the top 32K can be replaced with EPROM (2716 type) on-board
- Card ejectors
- Goldplated PCB edge connector

The board has been designed to conform to the proposed IEEE 696 standard.

Magic Mapping is a trademark of SSM Microcomputer Products, Inc.
CROMIX is a trademark of Cromemco, 280 Bernardo Avenue, Mountain View, CA.
OASIS is a trademark of Phase One Systems, 7700 Edgewater Drive, Oakland, CA.
MP/M is a tademark of Digital Research, P.O. Box 579, Pacific Grove, CA.

2.0 SETTING UP YOUR MB64

This section provides the information necessary to configure the MB64 to your particular application. Section 2.9 provides several example setups to assist you in performing this task. Be sure to also read Section 2.10, SWO OPTION, for proper read/write operation of the MB64 with your CPU.

NOTE: All of the following options (except BANK BIT) can be selected either by using supplied mini-jumpers or wire-wrapping.

2.1 MEMORY ADDRESSING

The MB64 is divided into two memory blocks of 32K bytes each. Block-A is physically located on the left half of the board; Block-B is physically located on the right half. Refer to the Memory Map in the APPENDIX for the address location of each memory chip.

Each 32K block can be addressed to either the lower or upper portion of the 64K memory space. Both 32K blocks can be addressed to the same address space if the MB64's Bank Select option is used and the bank bit for each block is different (refer to Section 2.3).

ADDRESS	BLOCK-B	BLOCK-A
Upper 32K	E17 to E18	E20 to E21
Lower 32K	E18 to E19	E21 to E22
Block Disabled	E18 open	E21 open

2.2 EXTENDED ADDRESSING

The MB64 is designed to support extended addressing (A16 thru A23) as defined in the proposed IEEE 696 standard. This will allow the MB64 to be placed on any 64K boundary within a maximum memory space of 16 megabytes.

The Extended Addressing option is enabled by connecting E26 to E27 for Block-A, and E29 to E30 for Block-B.

To select the extended address range which will enable the MB64, jumpers will be either installed or removed on the the header E1 thru E16 listed below.

Installing a jumper will provide a match when that particular address line is at a logic zero (low). Removing a jumper will provide a match when that particular address line is at a logic one (high).

Jumper installed = 0
Jumper removed = 1

ADDRESS (Hex)	A23 E9 E1	A22 E10 E2	A21 E11 E3	A20 E12 E4	A19 E13 E5	A18 E14 E6	A17 E15 E7	A16 E16 E8	ADDRESS RANGE
000000	0	0	0	0	0	0	0	0	1st 64K
010000	0	0	0	0	0	0	0	1	2nd 64K
020000	0	0	0	0	0	0	1	0	3rd 64K
030000	0	0	0	0	0	0	1	1	4th 64K
040000	0	0	0	0	0	1	0	0	5th 64K
FE0000	1	1	1	1	1	1	1	0	255th 64K
FF0000	1	1	1	1	1	1	1	1	256th 64K

When Extended Addresing is selected, Bank Select is disabled; therefore, Bank Select and Extended Addressing are **not possible together** for the same memory block.

2.3 BANK SELECT

To extend the amount of memory available for an 8-bit CPU, Bank Select can be used on the MB64. This memory management technique switches in and out a 64K bank of memory by writing to an I/O port. Multiple 32K blocks, on one or more MB64s, can be addressed to the same address space, but only **ONE** block will be active at a time. All bank control is done through port 40 Hex (or 41 Hex). When Bank Select is selected, extended addressing is disabled; therefore, bank select and extended addressing are not possible together on the same memory block.

2.3.1 Bank Select Enable

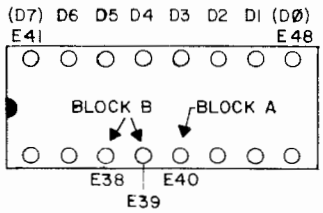
The two 32K blocks of memory on the MB64 can be individually bank selected. E26 thru E28 controls Block-A, while E29 thru E31 controls Block-B.

OPTION	BLOCK-A	BLOCK-B
Bank Select	E27 to E28	E30 to E31
Extended Addressing	E26 to E27	E29 to E30
Neither option	E27 open	E30 open

2.3.2 Bank Bit

One of 8 bits sent out to I/O port 40 Hex can be used to turn on (or off) a 64K bank of memory. If the data bit sent is a zero, the bank is disabled. If the data bit sent is a one, the bank is enabled.

All bank bit selection is through a 16 pin IC header. Pins E41 to E48 are data bits D7 thru D0, respectfully. Pin E40 is for banking Block-A, and pin E38 & E39 are for banking Block-B.



BANK BIT HEADER

Connect pins E38, E39 and E40 to the data bit desired by soldering a wire on the IC header. If only one bank bit is used for Block B, you can jumper E38 to E39. Be careful that pins E41 thru E48 **DO NOT SHORT TOGETHER.** Pins E41 thru E48 are the main S-100 bus' data output lines, and shorting them together may cause damage to other boards in your system.

2.3.3 Power-Up State

In a bank selected memory management system, one of the memory banks must be active on power-up to allow normal CPU operation. Each block on the MB64 can be set up to be enabled or disabled on reset (bus pin 75) of the computer.

POWER-UP STATE	BLOCK-A	BLOCK-B
Disabled	E35 to E36	E33 to E34
Enabled	E36 to E37	E32 to E33

If the Bank Select option is used on the MB64, the user **MUST** select one of the Power-Up options for each block. [**NOTE:** Reset must be generated on power-up of the computer during POC per the IEEE 696 standard.]

2.4 EPROM OPTION

The MB64 board is capable of supporting up to four 2716 EPROMs. Four IC sockets (U7, U14, U21, U28) have been provided with a jumper option to connect the Vpp (programming pulse) pin on the EPROM to +5 volts. The four IC sockets are addressed as the top 8K bytes of Block-B.

Address	RAM	ROM	Socket
1st 2K of 8K	E50 to E51	E49 to E50	U28
2nd 2K of 8K	E53 to E54	E52 to E53	U21
3rd 2K of 8K	E56 to E57	E55 to E56	U14
4th 2K of 8K	E59 to E60	E58 to E59	U7

[Remember that there are **NO** wait cycles generated by the MB64 for the EPROMs; therefore, the board cannot be run any faster than the EPROM's speed.]

2716 Manufacturers

NAME	PART	CURRENT		AVAILABLE SPEED
		STANDBY	READ	
Intel	2716	25ma (10ma Typ.)	100ma (57ma Typ.)	350ns to 650ns
NEC	UPD2716	25ma (10ma Typ.)	100 ma (57ma Typ.)	450ns
Motorola	MCM2716	25ma	100ma	250ns
AMI	S4716	25ma	100ma	450ns
Fujitsu	MBM2716	25ma	100ma	450ns
Hitachi	HN462716	35ma (21ma Typ.)	100ma (62ma Typ.)	450ns
National	NMC27C16	200ua	30ma (12ma Typ.)	450ns to 650ns

2.5 2K MEMORY DISABLE/MEMORY ORGANIZATION

The MB64 board is equipped with a special Magic Mapping circuit which allows the board to be disabled in 2K byte increments by simply removing the appropriate memory IC. This allows the user to free up memory space for memory-mapped devices such as disk interfaces, video boards, general I/O, ROM boards, etc.

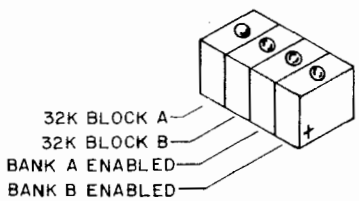
Magic Mapping relies on the **assumption** that the master CPU board has external pull-up resistors on the data input (DI) lines or the computer system has a **terminated bus.** The pull-up resistors on the DI bus will force the bus to "FF" Hex state, even if no S-100 board is present. Therefore, "FF" does not have to be transferred from the memory board to the data input bus. The code "FF" Hex is used internally by the MB64 to disable the ability to read the memory.

To determine which memory chip should be removed for a particular free address space, refer to the memory location map in the APPENDIX.

If the user wants to disable Magic Mapping for some reason, simply remove IC U44 (74LS30).

2.6 BOARD ENABLE INDICATOR

The MB64 has 4 memory state indicators at the top edge of the board. Two indicators show whether a 32K block of memory is selected. Two indicators show whether the bank for a block is enabled.



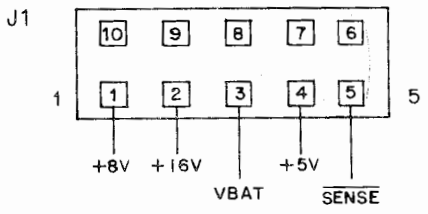
If the MB64 is set up for Bank Select (Section 2.3), both the block LED (label: ENA,ENB) and bank LED (label BNK A,BNK B) must be lit to read or write to the corresponding 32K bytes of memory.

2.7 BATTERY CONNECTOR J1

The MB64 is set up for a future battery backup piggyback board which will interface through connector J1. The connector J1 is used for:

- Battery power input (VBAT)
- Remote MB64 enable/disable (Sense)
- Off-board logic power (+5V)
- Battery charger power (+16V)
- General purpose power (+8V)

When no battery backup is connected to the MB64, J1 pin 5 to pin 6 (sense) must be shorted together to enable the MB64. Also, J1 pin 3 to in 4 must be connected to supply power to the memory chips when no battery power is available.



BATTERY CONNECTOR

2.8 SETUP FOR CROMIX

The MB64 can be set up to support the "User Memory" requirements of the CROMIX operating system by Cromemco. Under CROMIX, there can be up to 6 user memory boards of 64K bytes each. CROMIX requires bank-switched memory, with the upper 32K residing in the selected user space and also in the common memory bank (number 7).

The MB64 is split into two 32K banks called "A" and "B". Bank-A will be addressed to low memory range, while Bank-B will be addressed to the upper 32K range. Bank-B has two bank bit inputs (E38 & E39) so that it can be switched into two different banks per CROMIX. First, set up the MB64 for 64K with bank switching, and then select the bank bits for the user memory you are supporting. Typical setup is as follows:

64K Banked Slave Memory

CONNECT	COMMENT
E17 to E18	Enable upper 32K
E21 to E22	Enable lower 32K
J1-3 to J1-4	Enable memory power
J1-5 to J1-6	Enable MB64 (battery chip select)
E27 to E28	Enable Bank-A mode
E30 to E31	Enable Bank-B mode
E39 to E40	Set both bank bits the same
E35 to E36	Reset Bank-A to OFF
E33 to E34	Reset Bank-B to OFF
E24 to E25	Enable $\overline{SWO}$ signal
E38 to E41	Enable upper 32K at Bank 7

User Memory Setup

USER	CONNECT	CROMIX SIZE
1st	E40 to E47	One user system
2nd	E40 to E46	Two " "
3rd	E40 to E45	Three " "
4th	E40 to E44	Four " "
5th	E40 to E43	Five " "
6th	E40 to E42	Six " "

2.9 STANDARD SETUP

In this section we will try to show some standard configurations for the MB64.

2.9.1 64K memory, no options

CONNECT	COMMENT
E17 to E18	Enable upper 32K bytes
E21 to E22	Enable lower 32K bytes
J1-3 to J1-4	Enable memory power
J1-5 to J1-6	Enable MB64 (battery chip select)
E35 to E36	Reset Bank-A (turn off LED)
E33 to E34	Reset Bank-B (turn off LED)
E50 to E51	Set U28 as RAM
E53 to E54	Set U21 as RAM
E56 to E57	Set U14 as RAM
E59 to E60	Set U7 as RAM

2.9.2 60K memory with top 4K EPROM

CONNECT	COMMENT
E17 to E18	Enable upper 32K bytes
E21 to E22	Enable lower 32K bytes
J1-3 to J1-4	Enable memory power
J1-5 to J1-6	Enable MB64 (battery chip select)
E34 to E36	Reset Bank-A (turn off LED)
E33 to E34	Reset Bank-B (turn off LED)
E55 to E56	Set U14 as a ROM socket
E58 to E59	Set U7 as a ROM socket
E50 to E51	Set U28 as RAM
E53 to E54	Set U21 as RAM

Remove U7 and U14 RAM chips. Place first 2K of EPROM (2716) into socket U14. U14's socket is addressed at 0F000 Hex. Place second 2K of EPROM into socket U7. U7's socket is addressed at 0F800 Hex. Remember that the CPU's speed cannot be any greater than the access time of the on-board EPROMs unless wait states can be preset on the CPU or other 696 memory support boards.

2.9.3 Bottom 32K banked with top 32K master

CONNECT	COMMENT
E17 to E18	Enable upper 32K bytes
E21 to E22	Enable lower 32K bytes
J1-3 to J1-4	Enable memory power
J1-5 to J1-6	Enable MB64 (batter chip select)
E35 to E36	Reset Bank-A
E33 to E34	Reset Bank-B (turn off LED)
E27 to E28	Enable Bank-A mode
E40 to *	Select bank bit
E50 to E51	Set U28 as RAM
E53 to E54	Set U21 as RAM
E56 to E57	Set U14 as RAM
E59 to E60	Set U7 as RAM

* Select bank bit per Section 2.3.2.

This setup makes the top 32K of memory a permanent (non-banked) master, while the lower 32K of memory is bank selected. The lower 32K of memory is switched off during reset or power-up, but can be turned on if E35 to E36 is changed to E36 to E37.

2.9.4 Two 32K banks, lower address

CONNECT	COMMENT
E18 to E19	Enable lower 32K bytes (Block B)
E21 to E22	Enable lower 32K bytes (Block A)
J1-3 to J1-4	Enable memory power
J1-5 to J1-6	Enable MB64 (battery chip select)
E35 to E36	Reset Bank-A
E33 to E34	Reset Bank-B
E27 to E28	Enable Bank-A mode
E30 to E31	Enable Bank-B mode
E40 to *	Select bank bit for A
E39 to *	Select bank bit for B
E38 to E39	Strap up used input
E50 to E51	Set U28 as RAM
E53 to E54	Set U21 as RAM
E56 to E57	Set U14 as RAM
E59 to E60	Set U7 as RAM

* Select bank bit per Section 2.3.2.

2.9.5 48K banked slave memory

16K of memory (from Block-B) will be removed from the MB64 to make it a 48K only board.

CONNECT	COMMENT
E17 to E18	Enable upper 32K
E21 to E22	Enable lower 32K
J1-3 to J1-4	Enable memory power
J1-5 to J1-6	Enable MB64 (battery chip select)
E27 to E28	Enable Bank-A mode
E30 to E31	Enable Bank-B mode
E39 to E40	Set both bank bits the same
E38 to E39	Strap up used input
E38 to *	Select bank bit
E35 to E36	Reset Bank-A to OFF
E33 to E34	Reset Bank-B to OFF

* Select bank bit per Section 2.3.2.

Remove U6, U7, U13, U14, U20, U21, U28 and U35 from their sockets. This will disable the top 16K of memory with the help of Magic Mapping.

2.9.6 64K memory with extended addressing

CONNECT	COMMENT
E17 to E18	Enable upper 32K
E21 to E22	Enable lower 32K
J1-3 to J1-4	Enable memory power
J1-5 to J1-6	Enable MB64 (battery chip select)
E35 to E36	Reset Bank-A LED
E33 to E34	Reset Bank-B LED
E26 to E27	Enable extended addressing (A)
E29 to E30	Enable extended addressing (B)
*E1 thru E16	Select extended addressing code
E50 to E51	Set U28 as RAM
E53 to E54	Set U21 as RAM
E56 to E57	Set U14 as RAM
E59 to E60	Set U7 as RAM

* See Section 2.2 on Extended Addressing.

2.10 SWO OPTION

Some of the S-100 CPUs, and most of the IEEE 696 CPUs, are equipped with a write status signal called SWO. This signal can be used by the MB64 to control memory writing operations. If your CPU doesn't have this signal or the timing on this line is not correct, the SWO option can be disabled. Be sure to check your CPU for SWO (bus pin 97) and select the appropriate mode.

- Enable SWO for writing: Connect E24 to E25.
- Disable SWO for writing: Connect E23 to E24.

RECOMMENDED SETTING

Model	CPU	Manufacturer	Connect
CB1A	8080	SSM	E24 to E25
CB2	Z-80	SSM	E24 to E25
SCC	Z-80	Cromemco	E24 to E25
ZPU	Z-80	Cromemco	E24 to E25
ZPB	Z-80	Northstar	E23 to E24
-	Z-80	Dynabyte	E23 to E24
-	8080	WAMECO	E24 to E25
SBC-100	Z-80	SD Systems	E23 to E24
ZPU	Z-80	TDL	E24 to E25

3.0 THEORY OF OPERATION

3.1 32K MEMORY SELECT PROM

The selection of 32K bytes of memory is controlled by a 256 x 4 PROM which replaces several discrete logic ICs by acting as a memory-mapped truth table of the logic functions desired. The address lines and chip select pins of the PROM are used as inputs to the logic function, while the output pins equal the truth table solution.

The input PROM signals are as follows:

SINP [bus 46] = PROM chip select 2 (E2)
SOUT [bus 45] = PROM chip select 1 (E1)

BANK-A ENABLE	=	PROM, address	A7
BANK-B ENABLE	=	" "	A6
NOT ENABLE-A	=	" "	A5
NOT ENABLE-B	=	" "	A4
MAGIC MAPPING	=	" "	A3
SMEMR [bus pin 47]	=	" "	A2
PHANTOM [bus pin 67]	=	" "	A1
PDBIN [bus pin 78]	=	" "	A0

BANK-A or BANK-B ENABLE must be at a logic one to activate 32K of memory on the MB64. The NOT ENABLE lines are used to select the lower or upper 32K block of memory within a 64K boundary. The Magic Mapping line must be a logic one to enable a memory read. The PHANTOM line (per the proposed IEEE 696 standard) must be a logic one to **read** from or **write** into memory.

The output PROM signals are as follows:

32K SELECT-A	=	PROM data	3
32K SELECT-B	=	" "	2
OUTPUT ENABLE	=	" "	1
READ ENABLE	=	" "	0

The 32K SELECT lines from the PROM are used to control a 4-to-16 decoder which drives sixteen 2K RAM chips. The OUTPUT ENABLE line from the PROM goes to the $\overline{OE}$ pin on each RAM. The READ ENABLE line from the PROM controls a tri-state buffer to transfer data from the selected memory chip to the data input (DI) bus in the computer.

To select a 32K block of memory, we need BANK ENABLE and ADDRESS (NOT ENABLE); therefore:

32K BLOCK-A = BANK-A ENABLE and not NOT ENABLE-A
= $A7 \cdot \overline{A5}$

32K BLOCK-B = BANK-B ENABLE and not NOT ENABLE-B
= $A6 \cdot \overline{A4}$

To select one 32K block that does not conflict with the other 32K block, both conditions **MUST NOT** be true. Also, PHANTOM disable must be true to select anything.

32K SELECT-A (D3) = 32K BLOCK-A and not 32K BLOCK-B and PHANTOM
$= A7 \cdot \overline{A5} \cdot (\overline{A6 \cdot \overline{A4}}) \cdot A1$

32K SELECT-B (D2) = 32K BLOCK-B and not 32K BLOCK-A and PHANTOM
$= A6 \cdot \overline{A4} \cdot (\overline{A7 \cdot \overline{A5}}) \cdot A1$

To provide an OUTPUT ENABLE signal to the RAMs, first the CPU must be performing a memory fetch operation (SMEMR) and the 32K must be selected.

OUTPUT ENABLE (D1) = SMEMR and (32K BLOCK-A or 32K BLOCK-B)
$= A2 \cdot (A7 \cdot \overline{A5}) \oplus (A6 \cdot \overline{A4})$

To turn on the tri-state buffer (U43) to read memory, the read strobe (PDBIN) from the CPU must be true, as well as the Magic Mapping control line.

READ ENABLE (D0) = PDBIN and SMEMR and MAGIC and PHANTOM
and (32K BLOCK-A or 32K BLOCK-B)

$= A0 \cdot A2 \cdot A3 \cdot (A7 \cdot \overline{A5}) \oplus (A6 \cdot \overline{A4}) \cdot A1$

With these four equations for the data lines of the PROM, the following truth table can now be generated for the PROM.

TRUTH TABLE

ADDRESS (Hex)	A7	A6	A5	A4	A3	A2	A1	A0	D3	D2	D1	D0	DATA (Hex)	COMMENT
0	0	0	0	0	0	0	0	0	1	1	1	1	F	No condition met
1	0	0	0	0	0	0	0	1	1	1	1	1	F	
2	0	0	0	0	0	0	1	0	1	1	1	1	F	
3	0	0	0	0	0	0	1	1	1	1	1	1	F	
4	0	0	0	0	0	1	0	0	1	1	1	1	F	
5	0	0	0	0	0	1	0	1	1	1	1	1	F	
6	0	0	0	0	0	1	1	0	1	1	1	1	F	
7	0	0	0	0	0	1	1	1	1	1	1	1	F	
8	0	0	0	0	1	0	0	0	1	1	1	1	F	
9	0	0	0	0	1	0	0	1	1	1	1	1	F	
A	0	0	0	0	1	0	1	0	1	1	1	1	F	
B	0	0	0	0	1	0	1	1	1	1	1	1	F	
C	0	0	0	0	1	1	0	0	1	1	1	1	F	
D	0	0	0	0	1	1	0	1	1	1	1	1	F	
E	0	0	0	0	1	1	1	0	1	1	1	1	F	
F	0	0	0	0	1	1	1	1	1	1	1	1	F	
10	0	0	0	1	0	0	0	0	1	1	1	1	F	
11	0	0	0	1	0	0	0	1	1	1	1	1	F	
12	0	0	0	1	0	0	1	0	1	1	1	1	F	
13	0	0	0	1	0	0	1	1	1	1	1	1	F	
14	0	0	0	1	0	1	0	0	1	1	1	1	F	
15	0	0	0	1	0	1	0	1	1	1	1	1	F	
16	0	0	0	1	0	1	1	0	1	1	1	1	F	
17	0	0	0	1	0	1	1	1	1	1	1	1	F	
18	0	0	0	1	1	0	0	0	1	1	1	1	F	
19	0	0	0	1	1	0	0	1	1	1	1	1	F	
1A	0	0	0	1	1	0	1	0	1	1	1	1	F	
1B	0	0	0	1	1	0	1	1	1	1	1	1	F	
1C	0	0	0	1	1	1	0	0	1	1	1	1	F	
1D	0	0	0	1	1	1	0	1	1	1	1	1	F	
1E	0	0	0	1	1	1	1	0	1	1	1	1	F	
1F	0	0	0	1	1	1	1	1	1	1	1	1	F	
20	0	0	1	0	0	0	0	0	1	1	1	1	F	
21	0	0	1	0	0	0	0	1	1	1	1	1	F	
22	0	0	1	0	0	0	1	0	1	1	1	1	F	
23	0	0	1	0	0	0	1	1	1	1	1	1	F	
24	0	0	1	0	0	1	0	0	1	1	1	1	F	
25	0	0	1	0	0	1	0	1	1	1	1	1	F	
26	0	0	1	0	0	1	1	0	1	1	1	1	F	
27	0	0	1	0	0	1	1	1	1	1	1	1	F	
28	0	0	1	0	1	0	0	0	1	1	1	1	F	
29	0	0	1	0	1	0	0	1	1	1	1	1	F	
2A	0	0	1	0	1	0	1	0	1	1	1	1	F	
2B	0	0	1	0	1	0	1	1	1	1	1	1	F	
2C	0	0	1	0	1	1	0	0	1	1	1	1	F	
2D	0	0	1	0	1	1	0	1	1	1	1	1	F	
2E	0	0	1	0	1	1	1	0	1	1	1	1	F	
2F	0	0	1	0	1	1	1	1	1	1	1	1	F	

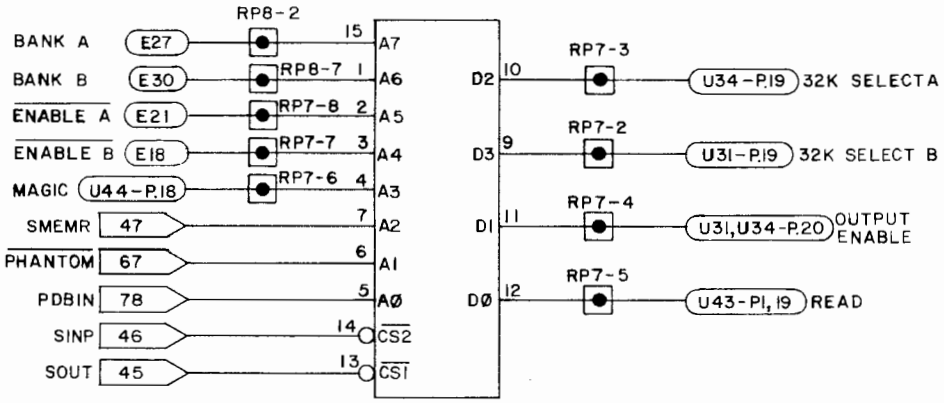
ADDRESS (Hex	A7	A6	A5	A4	A3	A2	A1	A0	D3	D2	D1	D0	DATA (Hex)	COMMENT
30	0	0	1	1	0	0	0	0	1	1	1	1	F	
31	0	0	1	1	0	0	0	1	1	1	1	1	F	
32	0	0	1	1	0	0	1	0	1	1	1	1	F	
33	0	0	1	1	0	0	1	1	1	1	1	1	F	
34	0	0	1	1	0	1	0	0	1	1	1	1	F	
35	0	0	1	1	0	1	0	1	1	1	1	1	F	
36	0	0	1	1	0	1	1	0	1	1	1	1	F	
37	0	0	1	1	0	1	1	1	1	1	1	1	F	
38	0	0	1	1	1	0	0	0	1	1	1	1	F	
39	0	0	1	1	1	0	0	1	1	1	1	1	F	
3A	0	0	1	1	1	0	1	0	1	1	1	1	F	
3B	0	0	1	1	1	0	1	1	1	1	1	1	F	
3C	0	0	1	1	1	1	0	0	1	1	1	1	F	
3D	0	0	1	1	1	1	0	1	1	1	1	1	F	
3E	0	0	1	1	1	1	1	0	1	1	1	1	F	
3F	0	0	1	1	1	1	1	1	1	1	1	1	F	
40	0	1	0	0	0	0	0	0	1	1	1	1	F	
41	0	1	0	0	0	0	0	1	1	1	1	1	F	
42	0	1	0	0	0	0	1	0	1	0	1	1	B	Write Block-B
43	0	1	0	0	0	0	1	1	1	0	1	1	B	Write Block-B
44	0	1	0	0	0	1	0	0	1	1	0	1	D	
45	0	1	0	0	0	1	0	1	1	1	0	1	D	
46	0	1	0	0	0	1	1	0	1	0	0	1	9	Ready to read B
47	0	1	0	0	0	1	1	1	1	0	0	1	9	Ready to read B
48	0	1	0	0	1	0	0	0	1	1	1	1	F	
49	0	1	0	0	1	0	0	1	1	1	1	1	F	
4A	0	1	0	0	1	0	1	0	1	0	1	1	B	Write Block-B
4B	0	1	0	0	1	0	1	1	1	0	1	1	B	Write Block-B
4C	0	1	0	0	1	1	0	0	1	1	0	1	D	
4D	0	1	0	0	1	1	0	1	1	1	0	1	D	
4E	0	1	0	0	1	1	1	0	1	0	0	1	9	Ready to read B
4F	0	1	0	0	1	1	1	1	1	0	0	0	8	Read Block-B
50	0	1	0	1	0	0	0	0	1	1	1	1	F	
51	0	1	0	1	0	0	0	1	1	1	1	1	F	
52	0	1	0	1	0	0	1	0	1	1	1	1	F	
53	0	1	0	1	0	0	1	1	1	1	1	1	F	
54	0	1	0	1	0	1	0	0	1	1	1	1	F	
55	0	1	0	1	0	1	0	1	1	1	1	1	F	
56	0	1	0	1	0	1	1	0	1	1	1	1	F	
57	0	1	0	1	0	1	1	1	1	1	1	1	F	
58	0	1	0	1	1	0	0	0	1	1	1	1	F	
59	0	1	0	1	1	0	0	1	1	1	1	1	F	
5A	0	1	0	1	1	0	1	0	1	1	1	1	F	
5B	0	1	0	1	1	0	1	1	1	1	1	1	F	
5C	0	1	0	1	1	1	0	0	1	1	1	1	F	
5D	0	1	0	1	1	1	0	1	1	1	1	1	F	
5E	0	1	0	1	1	1	1	0	1	1	1	1	F	
5F	0	1	0	1	1	1	1	1	1	1	1	1	F	

ADDRESS (Hex)	A7	A6	A5	A4	A3	A2	A1	A0	D3	D2	D1	D0	DATA (Hex)	COMMENT
60	0	1	1	0	0	0	0	0	1	1	1	1	F	
61	0	1	1	0	0	0	0	1	1	1	1	1	F	
62	0	1	1	0	0	0	1	0	1	0	1	1	B	Write Block-B
63	0	1	1	0	0	0	1	1	1	0	1	1	B	Write Block-B
64	0	1	1	0	0	1	0	0	1	1	0	1	D	
65	0	1	1	0	0	1	0	1	1	1	0	1	D	
66	0	1	1	0	0	1	1	0	1	0	0	1	9	Ready to read B
67	0	1	1	0	0	1	1	1	1	0	0	1	9	Ready to read B
68	0	1	1	0	1	0	0	0	1	1	1	1	F	
69	0	1	1	0	1	0	0	1	1	1	1	1	F	
6A	0	1	1	0	1	0	1	0	1	0	1	1	B	Write Block-B
6B	0	1	1	0	1	0	1	1	1	0	1	1	B	Write Block-B
6C	0	1	1	0	1	1	0	0	1	1	0	1	D	
6D	0	1	1	0	1	1	0	1	1	1	0	1	D	
6E	0	1	1	0	1	1	1	0	1	0	0	1	9	Ready to read B
6F	0	1	1	0	1	1	1	1	1	0	0	0	8	Read Block-B
70	0	1	1	1	0	0	0	0	1	1	1	1	F	
71	0	1	1	1	0	0	0	1	1	1	1	1	F	
72	0	1	1	1	0	0	1	0	1	1	1	1	F	
73	0	1	1	1	0	0	1	1	1	1	1	1	F	
74	0	1	1	1	0	1	0	0	1	1	1	1	F	
75	0	1	1	1	0	1	0	1	1	1	1	1	F	
76	0	1	1	1	0	1	1	0	1	1	1	1	F	
77	0	1	1	1	0	1	1	1	1	1	1	1	F	
78	0	1	1	1	1	0	0	0	1	1	1	1	F	
79	0	1	1	1	1	0	0	1	1	1	1	1	F	
7A	0	1	1	1	1	0	1	0	1	1	1	1	F	
7B	0	1	1	1	1	0	1	1	1	1	1	1	F	
7C	0	1	1	1	1	1	0	0	1	1	1	1	F	
7D	0	1	1	1	1	1	0	1	1	1	1	1	F	
7E	0	1	1	1	1	1	1	0	1	1	1	1	F	
7F	0	1	1	1	1	1	1	1	1	1	1	1	F	
80	1	0	0	0	0	0	0	0	1	1	1	1	F	
81	1	0	0	0	0	0	0	1	1	1	1	1	F	
82	1	0	0	0	0	0	1	0	0	1	1	1	7	Write Block-A
83	1	0	0	0	0	0	1	1	0	1	1	1	7	Write Block-A
84	1	0	0	0	0	1	0	0	1	1	0	1	D	
85	1	0	0	0	0	1	0	1	1	1	0	1	D	
86	1	0	0	0	0	1	1	0	0	1	0	1	5	Ready to read A
87	1	0	0	0	0	1	1	1	0	1	0	1	5	Ready to read A
88	1	0	0	0	1	0	0	0	1	1	1	1	F	
89	1	0	0	0	1	0	0	1	1	1	1	1	F	
8A	1	0	0	0	1	0	1	0	0	1	1	1	7	Write Block-A
8B	1	0	0	0	1	0	1	1	0	1	1	1	7	Write Block-A
8C	1	0	0	0	1	1	0	0	1	1	0	1	D	
8D	1	0	0	0	1	1	0	1	1	1	0	1	D	
8E	1	0	0	0	1	1	1	0	0	1	0	1	5	Ready to read A
8F	1	0	0	0	1	1	1	1	0	1	0	0	4	Read Block-A

ADDRESS (Hex)	A7	A6	A5	A4	A3	A2	A1	A0	D3	D2	D1	D0	DATA (Hex)	COMMENT
90	1	0	0	1	0	0	0	0	1	1	1	1	F	
91	1	0	0	1	0	0	0	1	1	1	1	1	F	
92	1	0	0	1	0	0	1	0	0	1	1	1	7	Write Block-A
93	1	0	0	1	0	0	1	1	0	1	1	1	7	Write Block-A
94	1	0	0	1	0	1	0	0	1	1	0	1	D	
95	1	0	0	1	0	1	0	1	1	1	0	1	D	
96	1	0	0	1	0	1	1	0	0	1	0	1	5	Ready to read A
97	1	0	0	1	0	1	1	1	0	1	0	1	5	Ready to read A
98	1	0	0	1	1	0	0	0	1	1	1	1	F	
99	1	0	0	1	1	0	0	1	1	1	1	1	F	
9A	1	0	0	1	1	0	1	0	0	1	1	1	7	Write Block-A
9B	1	0	0	1	1	0	1	1	0	1	1	1	7	Write Block-A
9C	1	0	0	1	1	1	0	0	1	1	0	1	D	
9D	1	0	0	1	1	1	0	1	1	1	0	1	D	
9E	1	0	0	1	1	1	1	0	0	1	0	1	5	Ready to read A
9F	1	0	0	1	1	1	1	1	0	1	0	0	4	Read Block-A
A0	1	0	1	0	0	0	0	0	1	1	1	1	F	
A1	1	0	1	0	0	0	0	1	1	1	1	1	F	
A2	1	0	1	0	0	0	1	0	1	1	1	1	F	
A3	1	0	1	0	0	0	1	1	1	1	1	1	F	
A4	1	0	1	0	0	1	0	0	1	1	1	1	F	
A5	1	0	1	0	0	1	0	1	1	1	1	1	F	
A6	1	0	1	0	0	1	1	0	1	1	1	1	F	
A7	1	0	1	0	0	1	1	1	1	1	1	1	F	
A8	1	0	1	0	1	0	0	0	1	1	1	1	F	
A9	1	0	1	0	1	0	0	1	1	1	1	1	F	
AA	1	0	1	0	1	0	1	0	1	1	1	1	F	
AB	1	0	1	0	1	0	1	1	1	1	1	1	F	
AC	1	0	1	0	1	1	0	0	1	1	1	1	F	
AD	1	0	1	0	1	1	0	1	1	1	1	1	F	
AE	1	0	1	0	1	1	1	0	1	1	1	1	F	
AF	1	0	1	0	1	1	1	1	1	1	1	1	F	
B0	1	0	1	1	0	0	0	0	1	1	1	1	F	
B1	1	0	1	1	0	0	0	1	1	1	1	1	F	
B2	1	0	1	1	0	0	1	0	1	1	1	1	F	
B3	1	0	1	1	0	0	1	1	1	1	1	1	F	
B4	1	0	1	1	0	1	0	0	1	1	1	1	F	
B5	1	0	1	1	0	1	0	1	1	1	1	1	F	
B6	1	0	1	1	0	1	1	0	1	1	1	1	F	
B7	1	0	1	1	0	1	1	1	1	1	1	1	F	
B8	1	0	1	1	1	0	0	0	1	1	1	1	F	
B9	1	0	1	1	1	0	0	1	1	1	1	1	F	
BA	1	0	1	1	1	0	1	0	1	1	1	1	F	
BB	1	0	1	1	1	0	1	1	1	1	1	1	F	
BC	1	0	1	1	1	1	0	0	1	1	1	1	F	
BD	1	0	1	1	1	1	0	1	1	1	1	1	F	
BE	1	0	1	1	1	1	1	0	1	1	1	1	F	
BF	1	0	1	1	1	1	1	1	1	1	1	1	F	

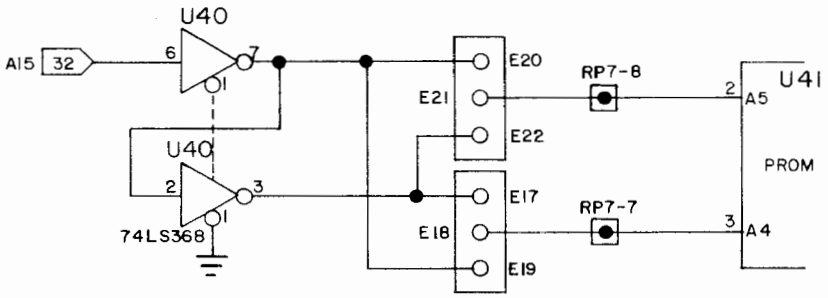
ADDRESS (Hex)	A7	A6	A5	A4	A3	A2	A1	A0	D3	D2	D1	D0	DATA (Hex)	COMMENT
C0	1	1	0	0	0	0	0	0	1	1	1	1	F	
C1	1	1	0	0	0	0	0	1	1	1	1	1	F	
C2	1	1	0	0	0	0	1	0	1	1	1	1	F	
C3	1	1	0	0	0	0	1	1	1	1	1	1	F	
C4	1	1	0	0	0	1	0	0	1	1	1	1	F	
C5	1	1	0	0	0	1	0	1	1	1	1	1	F	
C6	1	1	0	0	0	1	1	0	1	1	1	1	F	
C7	1	1	0	0	0	1	1	1	1	1	1	1	F	
C8	1	1	0	0	1	0	0	0	1	1	1	1	F	
C9	1	1	0	0	1	0	0	1	1	1	1	1	F	
CA	1	1	0	0	1	0	1	0	1	1	1	1	F	
CB	1	1	0	0	1	0	0	1	1	1	1	1	F	
CC	1	1	0	0	1	1	0	0	1	1	1	1	F	
CD	1	1	0	0	1	1	0	1	1	1	1	1	F	
CE	1	1	0	0	1	1	1	0	1	1	1	1	F	
CF	1	1	0	0	1	1	1	1	1	1	1	1	F	
D0	1	1	0	1	0	0	0	0	1	1	1	1	F	
D1	1	1	0	1	0	0	0	1	1	1	1	1	F	
D2	1	1	0	1	0	0	1	0	0	1	1	1	7	Write Block-A
D3	1	1	0	1	0	0	1	1	0	1	1	1	7	Write Block-A
D4	1	1	0	1	0	1	0	0	1	1	0	1	D	
D5	1	1	0	1	0	1	0	1	1	1	0	1	D	
D6	1	1	0	1	0	1	1	0	0	1	0	1	5	Ready to read A
D7	1	1	0	1	0	1	1	1	0	1	0	1	5	Ready to read A
D8	1	1	0	1	1	0	0	0	1	1	1	1	F	
D9	1	1	0	1	1	0	0	1	1	1	1	1	F	
DA	1	1	0	1	1	0	1	0	0	1	1	1	7	Write Block-A
DB	1	1	0	1	1	0	1	1	0	1	1	1	7	Write Block-A
DC	1	1	0	1	1	1	0	0	1	1	0	1	D	
DD	1	1	0	1	1	1	0	1	1	1	0	1	D	
DE	1	1	0	1	1	1	1	0	0	1	0	1	5	Ready to read A
DF	1	1	0	1	1	1	1	1	0	1	0	0	4	Read Block-A
E0	1	1	1	0	0	0	0	0	1	1	1	1	F	
E1	1	1	1	0	0	0	0	1	1	1	1	1	F	
E2	1	1	1	0	0	0	1	0	1	0	1	1	B	Write Block-B
E3	1	1	1	0	0	0	1	1	1	0	1	1	B	Write Block-B
E4	1	1	1	0	0	1	0	0	1	1	0	1	D	
E5	1	1	1	0	0	1	0	1	1	1	0	1	D	
E6	1	1	1	0	0	1	1	0	1	0	0	1	9	Ready to read B
E7	1	1	1	0	0	1	1	1	1	0	0	1	9	Ready to read B
E8	1	1	1	0	1	0	0	0	1	1	1	1	F	
E9	1	1	1	0	1	0	0	1	1	1	1	1	F	
EA	1	1	1	0	1	0	1	0	1	0	1	1	B	Write Block-B
EB	1	1	1	0	1	0	1	1	1	0	1	1	B	Write Block-B
EC	1	1	1	0	1	1	0	0	1	1	0	1	D	
ED	1	1	1	0	1	1	0	1	1	1	0	1	D	
EE	1	1	1	0	1	1	1	0	1	0	0	1	9	Ready to read B
EF	1	1	1	0	1	1	1	1	1	0	0	0	8	Read Block-B

ADDRESS (Hex)	A7	A6	A5	A4	A3	A2	A1	A0	D3	D2	D1	D0	DATA (Hex)	COMMENT
F0	1	1	1	1	0	0	0	0	1	1	1	1	F	
F1	1	1	1	1	0	0	0	1	1	1	1	1	F	
F2	1	1	1	1	0	0	1	0	1	1	1	1	F	
F3	1	1	1	1	0	0	1	1	1	1	1	1	F	
F4	1	1	1	1	0	1	0	0	1	1	1	1	F	
F5	1	1	1	1	0	1	0	1	1	1	1	1	F	
F6	1	1	1	1	0	1	1	0	1	1	1	1	F	
F7	1	1	1	1	0	1	1	1	1	1	1	1	F	
F8	1	1	1	1	1	0	0	0	1	1	1	1	F	
F9	1	1	1	1	1	0	0	1	1	1	1	1	F	
FA	1	1	1	1	1	0	1	0	1	1	1	1	F	
FB	1	1	1	1	1	0	1	1	1	1	1	1	F	
FC	1	1	1	1	1	1	0	0	1	1	1	1	F	
FD	1	1	1	1	1	1	0	1	1	1	1	1	F	
FE	1	1	1	1	1	1	1	0	1	1	1	1	F	
FF	1	1	1	1	1	1	1	1	1	1	1	1	F	



3.2 MEMORY ADDRESS SELECT

Memory address selection is provided by jumpers E17 thru E22. These jumpers allow the user to select the lower or upper 32K of memory within a 64K boundary by selecting the normal or inverted state of the A15 bus line. The input pins A4 & A5 must be a logic zero to enable 32K of memory.

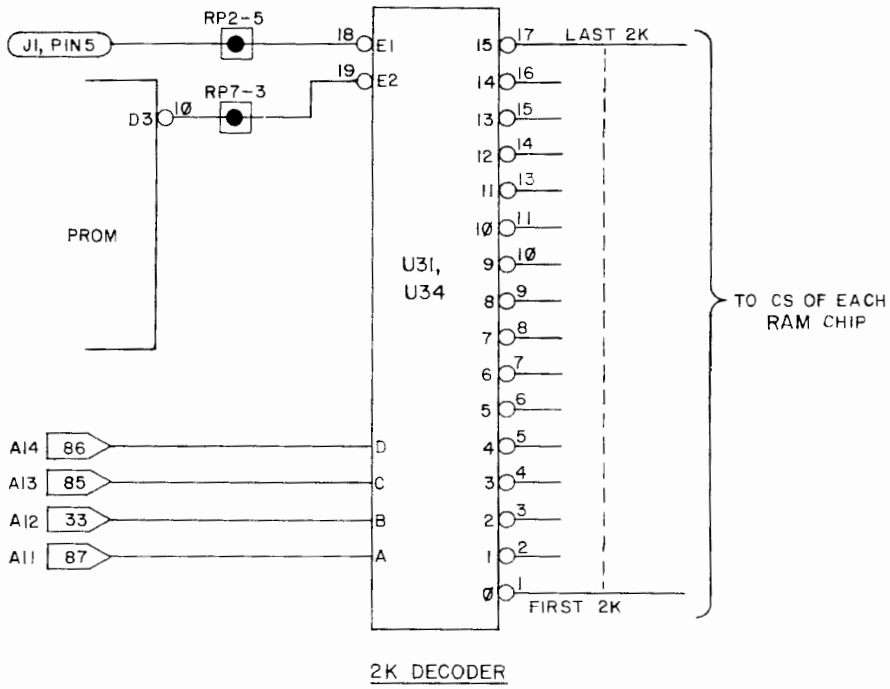


MEMORY ADDRESS SELECT

3.3 2K MEMORY DECODE

After the input conditions are met on the PROM per Section 3.1, one of the two 32K select lines (D3 or D2) goes low, enabling a 4-to-16 decoder IC (74LS154). The 4-to-16 decoder receives address lines A11 thru A14 as its input and therefore will decode down to every 2K memory increment within one 32K boundary. Each of the 16 outputs of the 74LS154 goes to the chip select pin of a memory IC within a memory block.

The 4-to-16 decoder has two enabling pins. While one enable pin goes to 32K Select, the other enable pin goes to the battery back-up connector J1. J1, pin 5, is used by the battery back-up option to protect the data within RAM from being changed while on battery power. Without battery back-up, this pin is normally grounded to enable the 4-to-16 decoder.



2K DECODER

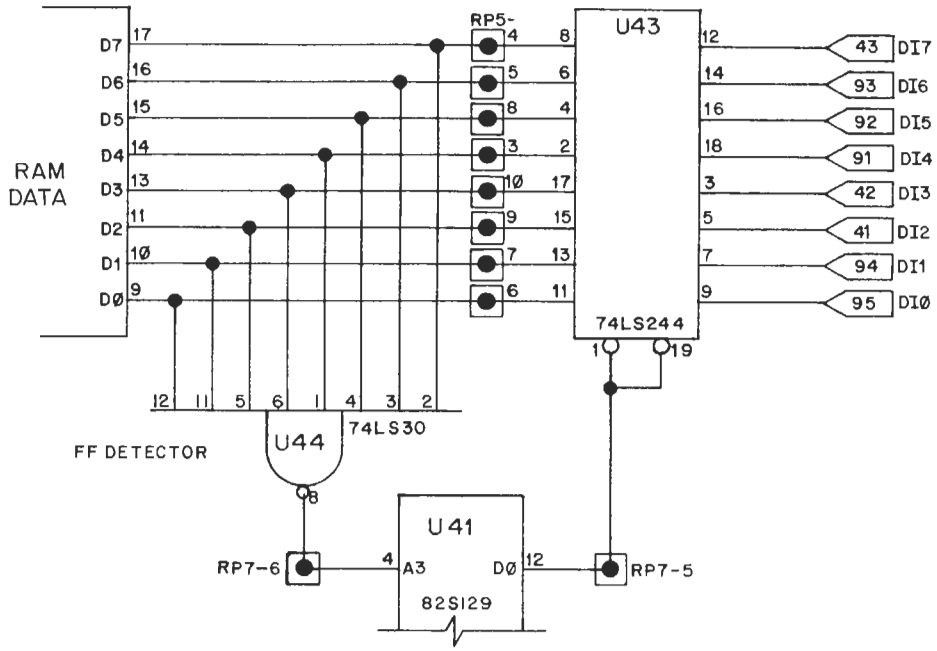
3.4 MAGIC MAPPING

Originally incorporated into the MB8A in 1977, the Magic Mapping circuit allows a socket on the memory board and its supporting circuitry to be disabled by simply removing the IC chip. The Magic Mapping circuit disables the tri-state buffer from driving the data input (DI) bus if the memory IC is removed. Memory space (in 2K increments) can be made available for memory mapped video, I/O, disks or ROM boards within the 64K of memory.

Magic Mapping relies on the **assumption** that the master CPU board has external pull-up resistors on the DI lines or the computer system has a **terminated bus.** The pull-up resistors on the DI bus will force the bus to "FF" Hex state, even if no S-100 board is present. Therefore, "FF" does not have to be transferred from the memory board to the DI bus.

U44 (74LS30) is an "FF" detector on the MB64. If an addressed memory chip puts out any Hex code except FF, then U44 outputs a one which will enable the read buffer (U43). If "FF" is detectd, the output tri-state buffer is turned off, allowing any external S-100 board to drive the DI bus.

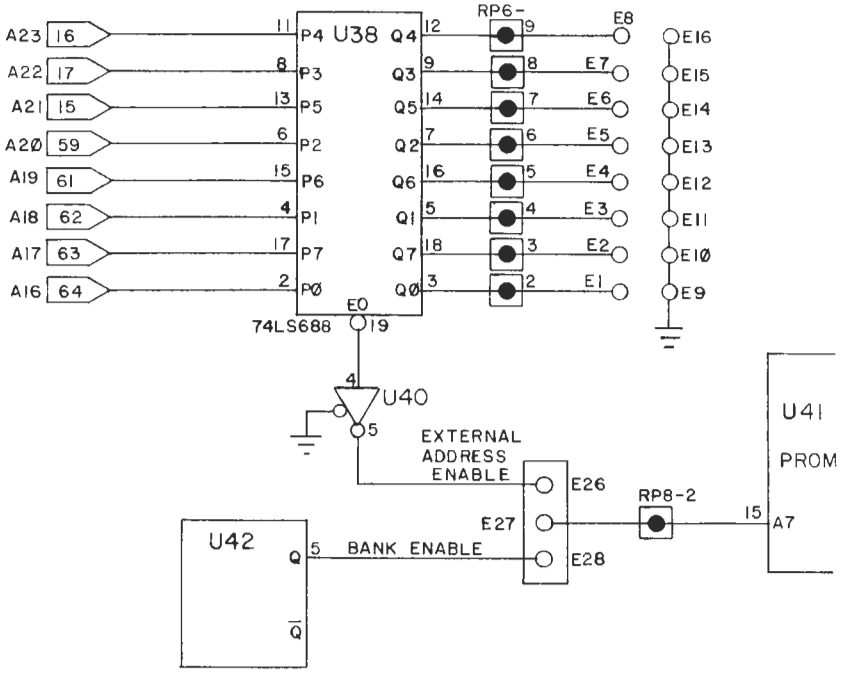
Magic Mapping allows for an entire 2K memory increment to be available for other memory boards or smaller areas by filling selected areas of RAM with "FF" Hex.



MAGIC MAPPING CIRCUIT

3.5 EXTENDED ADDRESSING

The proposed IEEE 696 standard for the S-100 bus has added 8 additional address lines, A16 thru A23, for up to 16 megabytes of memory. The MB64 has an on-board 8-bit comparator (U38) which can be set to enable/disable the memory per the state of the extended address lines. Input lines A6 & A7 of U41 (PROM) are used to enable or disable a 32K block of memory per the equations in Section 3.1.

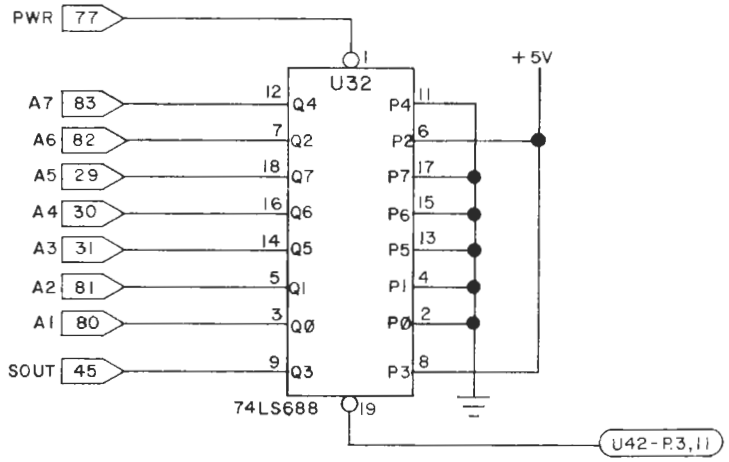


EXTENDED ADDRESS DECODER

3.6 BANK SELECT CIRCUIT

The bank select function is driven by I/O port 40 or 41 Hex. This function is used in memory management schemes to provide multiple layers of memory, all addressed at the **SAME** address space. Each banked memory board is turned on or off by the memory manager software, for each task to be executed, as scheduled under time or priority interrupts.

The I/O address decoder is one 74LS688 (U32) comparator. This IC puts out a negative pulse every time PWR, SOUT, and A1 thru A7 match the preset inputs on the other side of this comparator. Due to the lack of sufficient inputs to U32, A0 was not sensed, so the bank port address is 40 Hex and 41 Hex.

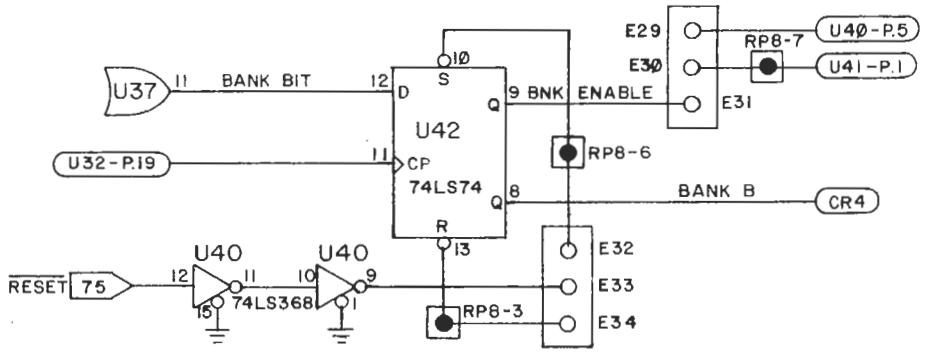


I/O ADDRESS DECODER

The bank select circuit is divided into two banks of 32K each. A bit within the byte sent to I/O port 40 Hex controls the activation of a bank. To save the user-selected bit for continuous bank control, a flip-flop (U41) is used for storage. The bit to be stored is selected by a 16-pin IC header. If the bit sent to the D-input of the flip-flop is a one, then the 32K block is enabled. If the bit sent is a zero, then 32K is disabled.

On power up in a bank-selected computer system, one memory bank is usually activated as the master. The flip-flop has been provided with jumper options to force the 32K block ON or OFF on power-up (POC) or reset. [**NOTE:** The proposed IEEE 696 standard requires Reset to be generated when the POC bus line is low.]

Jumpering E32 to E34 (E35 to E37) connects the computer's reset signal to the set input or clear input of the bank flip-flop.



BANK FLIP-FLOP

If jumper E32 to E33 (or E36 to E37) is connected, the memory block that flip-flop is controlling becomes a master bank on reset. If jumper E33 to E34 (or E35 to E36) is connected, the reset signal clears the "Q" output of the flip-flop and that memory block.

Two bank select indicators are provided on the MB64. Each flip-flop drives a LED to indicate if one of the 32K bank flip-flops are enabled.

3.7 BATTERY BACKUP

The MB64 is provided with a connector labelled J1 for an optional battery backup circuit. This battery option can maintain power to the memory chips for more than 5 hours, depending on the memory type and manufacturer used. For further information, please contact SSM for features and date of availability.

3.8 BUS INTERFACE

The MB64's memory chips are isolated from the S-100 bus by buffer ICs (74LS244, 74LS125, etc.) or general logic (74LS154, 82S129, etc.).

a. Address lines A0 thru A7 are buffered by U33 (74LS244).
b. Address lines A8 thru A10 are buffered by U39 (74LS244).
c. Address lines A11 thru A14 are isolated by U31 & U34 (74LS154).
d. Address line A15 is isolated by U40 (74LS368).
e. Address lines A16 thru A23 are buffered by U38 (74LS688).
f. Status lines SINP and SOUT are isolated by U41 (82S129).
g. The status line for memory read (SMEMR) is isolated by U41 (82S129).
h. The read strobe (PDBIN) is isolated by U41 (82S129).
i. The write strobe ($\overline{\text{PWR}}$) is isolated by U32 & U39 (74LS688 & 74LS125).
j. The read/write disable line (Phantom) is isolated by U4 (82S129).
k. The status line for writing (SWO) is isolated by U39 (74LS125).
1. The memory data is read via U43 (74LS244).
m. The memory data is written via U45 (74LS244).

The data buffer used during a read operation (U43) is controlled by the logic truth table within U41 (82S129) and issued on pin 12. U41, pin 12 will not provide a chip enable to U43 until the SMEMR, PDBIN, PHANTOM, A15, SINP and SOUT signals are in the correct state (see Section 3.1).

The data buffer used during a write operation (U45) is controlled by the buffer gate U39 (74LS125). To guarantee that the data is still present on the memory chip when the $\overline{WE}$ signal goes high, the write line (U39, pin 11) drives the RAM and U45 directly. (U45 provides 10 nanoseconds or greater delay before the data becomes invalid at the end of a write cycle which meets the manufacturer's specification of 0 nanoseconds of data hold time.)

4.0 MEMORY TEST PROGRAM

```
                ;       Simple Memory Test
                ;       Written by Andrew Schneider
                ;       Modified by Malcolm Wright
                ;       Coyright 1977 by SSM

                ;       Set "START" to the starting address of
                ;       memory to be tested.  Set "MEND" to the last
                ;       address of memory to be checked.

                ;       The program will stop (HALT) when complete
                ;       or if an error was found.  "GORB" (good or
                ;       bad) will be set to 00H for good memory or
                ;       to the byte pattern that would not read or
                ;       write correctly into memory.  "LAST" is the
                ;       location where the last address tested will
                ;       be saved.  If memory is good, then LAST=MEND.

8000 =          BEGIN   EQU     8000        ;Start of program
E000 =          START   EQU     0000H       ;Beginning of address
E3FF =          MEND    EQU     7FFFH       ;Ending address

8000                    ORG     BEGIN
8000 210000             LXI     H,START
8003 11FF7F             LXI     D,MEND
8006 2B                 DCX     H
8007 23         LOOP:   INX     H
8008 3E7F               MVI     A,7FH
800A 07         CHECK:  RLC
800B 77                 MOV     M,A
800C BE                 CMP     M
800D C22080             JNZ     ERROR
8010 B7                 ORA     A
8011 FA0A80             JM      CHECK
8014 7B                 MOV     A,E
8015 BD                 CMP     L
8016 C20780             JNZ     LOOP
8019 7A                 MOV     A,D
801A BC                 CMP     H
801B C20780             JNZ     LOOP
801E 3E00               MVI     A,0
8020 322780     ERROR:  STA     GORB        ;If using an IMSAI front panel
                                            ;replace with       CMA
                                            ;                   OUT  0FFH
                                            ;to display byte on front panel.
8023 222880             SHLD    LAST
8026 76                 HLT
8027 00         GORB:   DB      0
8028 0000       LAST:   DW      0
802A                    END
```

5.0 TROUBLESHOOTING

Some checkout of the MB64 can be done by just watching the LEDs on the board.

5.1 BANK SELECT TEST

If you have another memory board which will run your system, you can temporarily disable the MB64 to test the banking circuitry.

a. Remove jumpers from E17 to E22.

b. Make a test header for E38 to E48.

```
Connect E40 to E48 (Bit0)
Connect E39 to E47 (Bit1)
Connect E38 to E46 (Bit2)
```

c. Run the following routine (clear BANKS):

```
                ORG  100H
100  AF         XRA  A      ; SET BANK BYTE=0
101  D3,40      OUT  40H    ; SEND BYTE
103  C3,00,00   JMP  0      ; GO BACK TO CP/M
```

All LEDs of the MB64 should not be lit. This checks both halves of U42 for a zero.

d. Now run:

```
                ORG  100H
100  3E,01      MVI  A,1    ; SET BANK BYTE=1
102  D3,40      OUT  40H    ; SEND BYTE
104  C3,00,00   JMP  0      ; GO BACK TO CP/M
```

Only the LED labelled BNKA should be lit. This checks one-half of U42.

e. Now run:

```
                ORG 100H
100  3E,02      MVI A,2     ; SET BANK BYTE=2
102  D3,40      OUT 40H     ; SEND BYTE
104  C3,00,00   JMP 0       ; GO BACK TO CP/M
```

Only the LED labelled BNKB should be lit. This checks the other half of U42 and one input of U37.

f. Now run:

```
                ORG 100H
100  3E,04      MVI A,4     ; SET BANK BYTE=4
102  D3,40      OUT 40H     ; SEND BYTE
104  C3,00,00   JMP 0       ; GO BACK TO CP/M
```

Only the LED labelled BNKB should be lit. The checks the other input of U37.

g. Last, run:

```
                    ORG 100H   ; SELECT UNUSED BANK
100  3E,08          MVI A,8    ; SET BANK BYTE=8
102  D3,40          OUT 40H    ; SEND BYTE
104  C3,00,00       JMP 0      ; GO BACK TO CP/M
```

No LEDs on the MB64 should be lit.

5.2 BANK PRESET

If you have another memory board which will run your system, you can temporarily disable the MB64 to test the banking circuitry.

a. Remove jumpers from E17 to E22.

b. Install jumpers E35 to E36 and E33 to E34.

c. Push computer Reset. (DON'T LET THE SYSTEM BOOT.)

   No LEDs on the MB64 should be lit. This tests the reset inputs of U42.

d. Install jumpers at E36 to E37 and E32 to E33 now.

e. Push computer Reset.

   Both LEDs on the MB64 labelled BNKA & BNKB should be lit. This tests the set inputs of U42.

f. Install jumpers at E36 to E37 and E33 to E34.

g. Push computer Reset.

   One LED on the MB64 labelled BNKA should be lit. This tests that the set/reset inputs are not shorted between the halves of U42.

5.3 MEMORY ADDRESSING

If the MB64 is set up in one of the many standard configurations indicated in Section 2.9, the LED's ENA or ENB should be flashing dimly as the computer accesses the board. If there are no jumpers on E17 thru E22, the MB64 cannot be read.

By enabling half of the MB64 (32K), it should be possible to run user-defined memory tests. Jumper E18 to E19 to test memory block B as the first 32K and leave E21 open. Jumper E21 to E22 to test memory block A as the first 32K and leave E18 open.

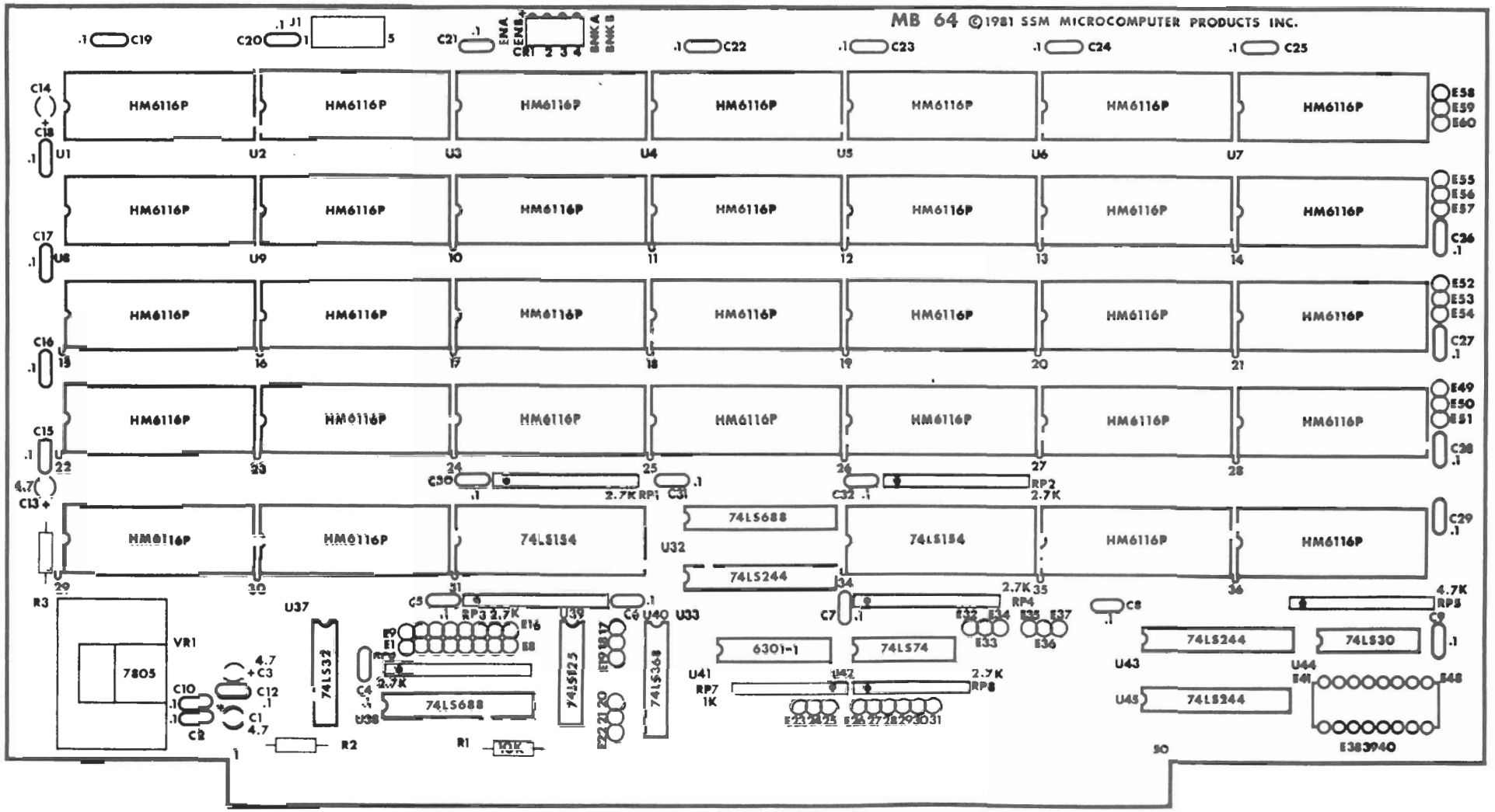
6.0 WARRANTY

SSM Microcomputer Products, Inc. warrants its products to be free from defects in materials and/or workmanship for a period of ninety (90) days for kits and one (1) year for factory assembled boards. In the event of malfunction or other indication of failure attributable directly to faulty workmanship and/or material, then, upon return of the product (postage paid) to SSM at 2190 Paragon Drive, San Jose, CA 95131, "Attention: Warranty Claims Department", SSM will, at its option, repair or replace the defective part or parts to restore said product to proper operating condition. All such repairs and/or replacements shall be rendered by SSM without charge for parts or labor when the product is returned within the specified period of the date of purchase. This warranty applies only to the original purchaser.

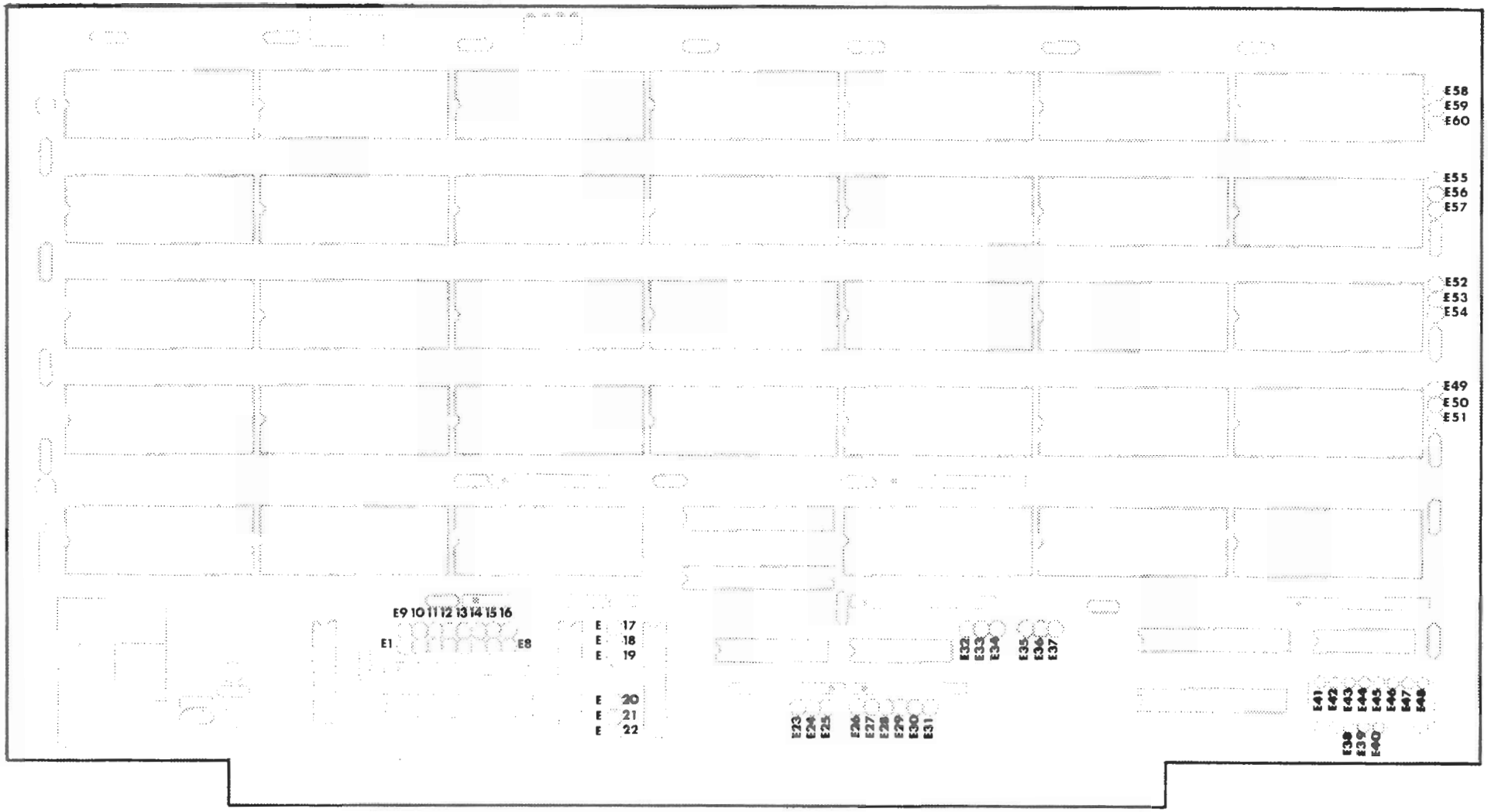
This warranty will not cover the failure of SSM products which at the discretion of SSM shall have resulted from accident, abuse, negligence, alteration, or misapplication of the product. While every effort has been made to provide clear and accurate technical information on the application of SSM products, SSM assumes no liability in any events which may arise from the use of said technical information.

This warranty is in lieu of all other warranties, expressed or implied, including warranties of mercantability and fitness for use. In no event will SSM be liable for incidental and consequential damages arising from or in any way connected with the use of its products. Some states do not allow the exclusion or limitation of incidental or consequential damages, so the above limitation or exclusion may not apply to you.

IMPORTANT: Proof of purchase is necessary for products returned for repair under warranty. Before returning any product, please call our Customer Service Department for a return authorization number.

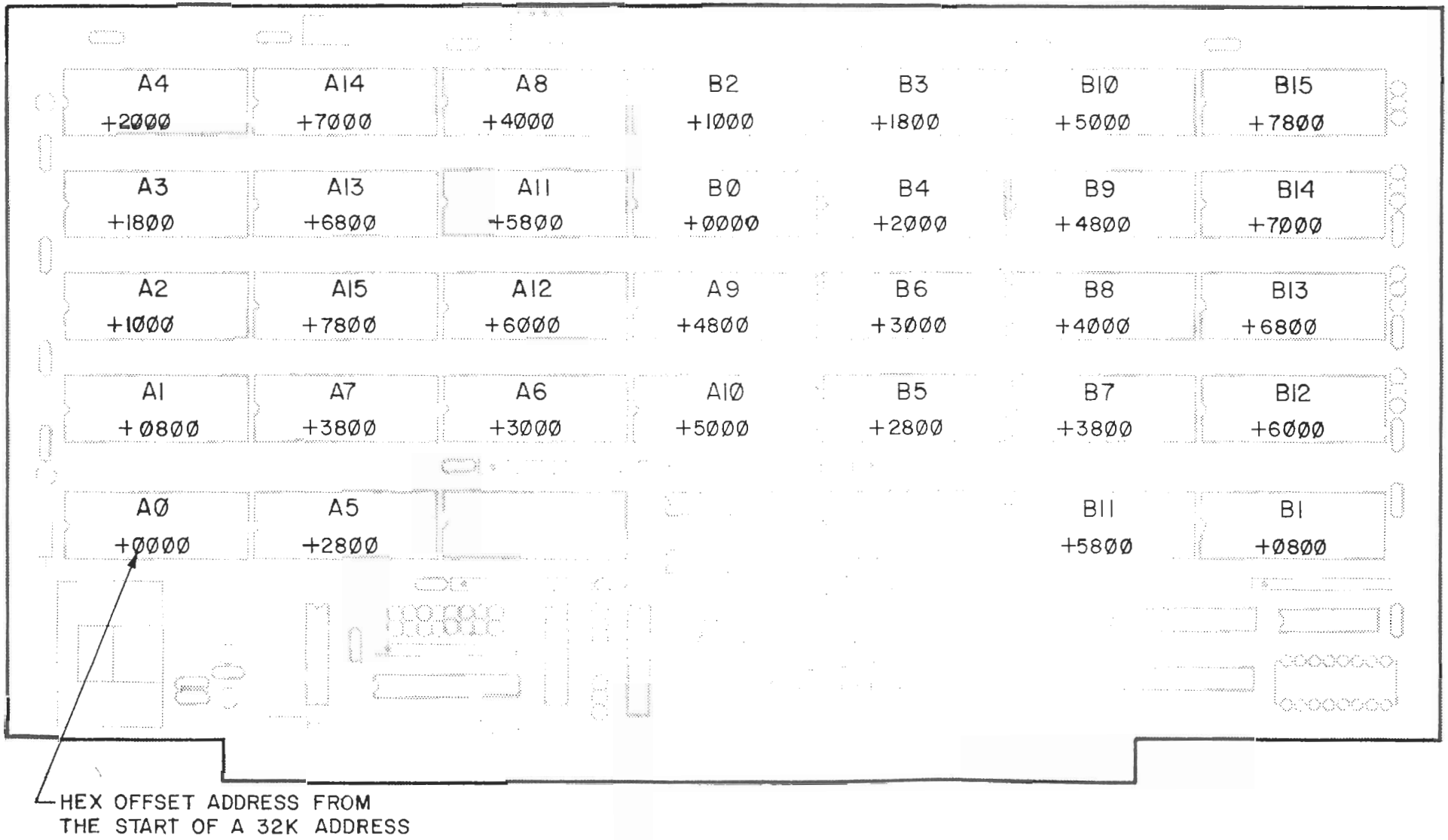


ASSEMBLY DRAWING



JUMPER DRAWING

A0 THRU A15 = CHIPS IN BLOCK A
B0 THRU B15 = CHIPS IN BLOCK B



MEMORY MAP

PARTS LIST

IC's

32	U1-U30, 35, 36	HM6116P	2K x 8 CMOS static RAM (150 ns)
2	U31, 34	74LS154	
2	U32, 38	74LS688	8-bit comparator
3	U33, 43, 45	74LS244	
1	U39	74LS125	
1	U40	74LS368	
1	U41	82S129	256 x 4 bipolar PROM (marked MB64-LE)
1	U42	74LS74	
1	U44	74LS30	
1	U37	74LS32	
1	VR1	7805	+5V voltage regulator

RESISTORS

1	R1	10K ohm 1/4W 5% (brown, black, orange)
5	RP1, 2, 3, 4, 6	2.7K ohm 10-pin SIP resistor network
1	RP5	4.7K ohm 10-pin SIP resistor network
1	RP8	2.7K ohm 8-pin SIP resistor network
1	RP7	1K ohm 8-pin SIP resistor network

CAPACITORS

4	C1, 3, 13, 14	4.7 uf DIP tantalum
27	2, 4-10, 12, 15-32	.1 uf monolithic capacitor

DIODES

4	CR1-4	LED Dialight 555-2007

SOCKETS

4	14-pin sockets
3	16-pin sockets
5	20-pin sockets
34	24-pin sockets

CONNECTORS

9	3 x 1 header strips
1	6 x 1 header strip
1	5 x 2 header strip
1	8 x 2 header strip

HARDWARE

1	#6 hardware set
1	Small heatsink
2	Card ejectors
19	Mini-jumpers
1	MB64 PC board
1	MB64 manual
1	Warranty card
1	16-pin IC header

HITACHI SERIES HM6116P

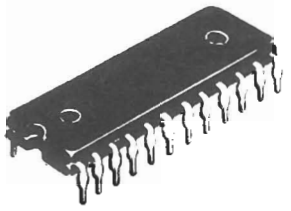
2048 X 8 BIT HIGH SPEED STATIC C MOS RAM

HITACHI

■ FEATURES

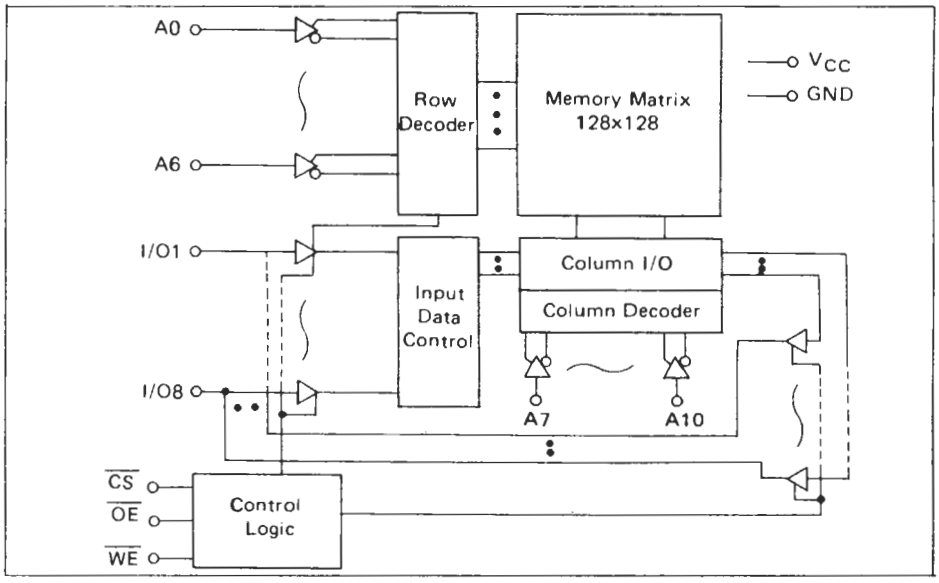
- Single 5V Supply and High Density 24 Pin Package
- High Speed: Fast Access Time ..... 120ns/150ns/200ns max.
- Low Power Standby and ..... 100μW typ. (Standby)
  Low Power Operation: ..... 180mW typ. (Operation)
- Completely Static RAM ..... No clock or Timing Strobe Required
- Directly TTL Compatible ..... All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

INDUSTRIAL STANDARD
24 pin (0.6 width)

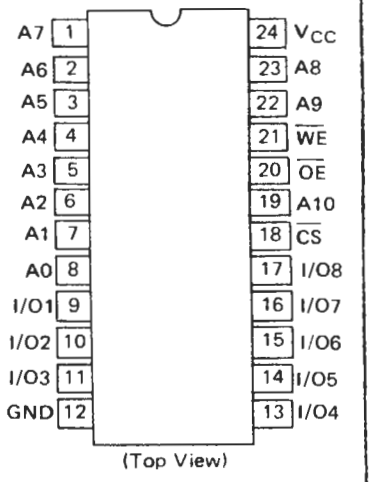


(DP-24)

■ FUNCTIONAL BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_{IN}	−0.5 to 7.0	V
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	−55 to 125	°C
Temperature Under Bias	T_{bias}	−10 to 85	°C
Power Dissipation	P_T	1.0	W

■ TRUTH TABLE

CS	OE	WE	Mode	V_{cc} Current	I/O Pin	Ref. Cycle
H	X	X	Not Selected	I_{SB}, I_{SBI}	High Z	
L	L	H	Read	I_{cc}	D_{out}	Read Cycle No. 1 ~ 3
L	H	L	Write	I_{cc}	D_{in}	Write Cycle No. 1
L	L	L	Write	I_{cc}	D_{in}	Write Cycle No. 2

NOTE: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Office regarding specifications.

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leqq Ta \leqq 70°C$)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
	GND	0	0	0	V	
Input High (logic 1) Voltage	V_{IH}	2.2	3.5	6.0	V	
Input Low (logic 0) Voltage	V_{IL}	*−1.0		0.8	V	*Pulse width: 50ns DC: V_{IL} min = 0.3V

■ DC AND OPERATING CHARACTERISTICS ($0°C \leqq Ta \leqq 70°C$, V_{CC} = 5V ± 10%, GND = 0V)

Parameter	Symbol	HM6116P-2			HM6116P-3/P-4			Unit	Test Conditions	Notes
		Min	Typ	Max	Min	Typ	Max			
Input Leakage Current	$\|I_{LI}\|$		1	10		1	10	μA	V_{CC} = MAX V_{IN} = GND to V_{CC}	
Output Leakage Current	$\|I_{LO}\|$			10			10	μA	CS = V_{IH} or OE = V_{IH} $V_{I/O}$ = GND to V_{CC}	
Operating Power Supply Current: DC	I_{CC}		40	80		35	70	mA	CS = V_{IL}, $I_{I/O}$ = 0mA	
Operating Power Supply Current:[1] DC	I_{CC1}		35			30		mA	V_{IH} = 3.5V, V_{IL} = 0.6V $I_{I/O}$ = 0mA	2
Average Operating Current[2]	I_{CC2}		40	80		35	70	mA	MIN cycle duty = 100%	
Standby Power Supply Current: DC	I_{SB}		5	15		5	15	mA	CS = V_{IH}	
Standby Power Supply Current:[1] DC	I_{SB1}		0.02	2		0.02	2	mA	CS ≧ V_{CC} − 0.2V V_{IN} ≧ V_{CC} − 0.2V or V_{IN} ≦ 0.2V	
Output Low Voltage	V_{OL}			*0.4			**0.4	V	*I_{OL} = 4mA **I_{OL} = 2.1mA	3
Output High Voltage	V_{OH}	2.4			2.4				I_{OL} = 1.0mA	

NOTES: 1. Typical limits are at V_{CC} = 5.0V, Ta = +25°C and specified loading.
2. Reference Only.
3. HM6116P-2: I_{OL} = 4.0mA, HM6116P-3/HM6116P-4: I_{OL} = 2.1mA

■ CAPACITANCE (Ta = 25°C, f = 1.0 MHz)[1]

Parameter	Symbol	Typ	Max	Unit	Conditions	Notes
Input Capacitance	C_{IN}	3	5	pF	V_{IN} = 0V	
Input/Output Capacitance	$C_{I/O}$	5	7	pF	$V_{I/O}$ = 0V	

NOTE: 1. This parameter is sampled and not 100% tested.

• AC TEST CONDITIONS

Input pulse levels:	0.8V to 2.4V
Input rise and fall times:	10 ns
Input and output timing reference levels:	1.5V
Output load:	1 TTL Gate and C_L = 100pF

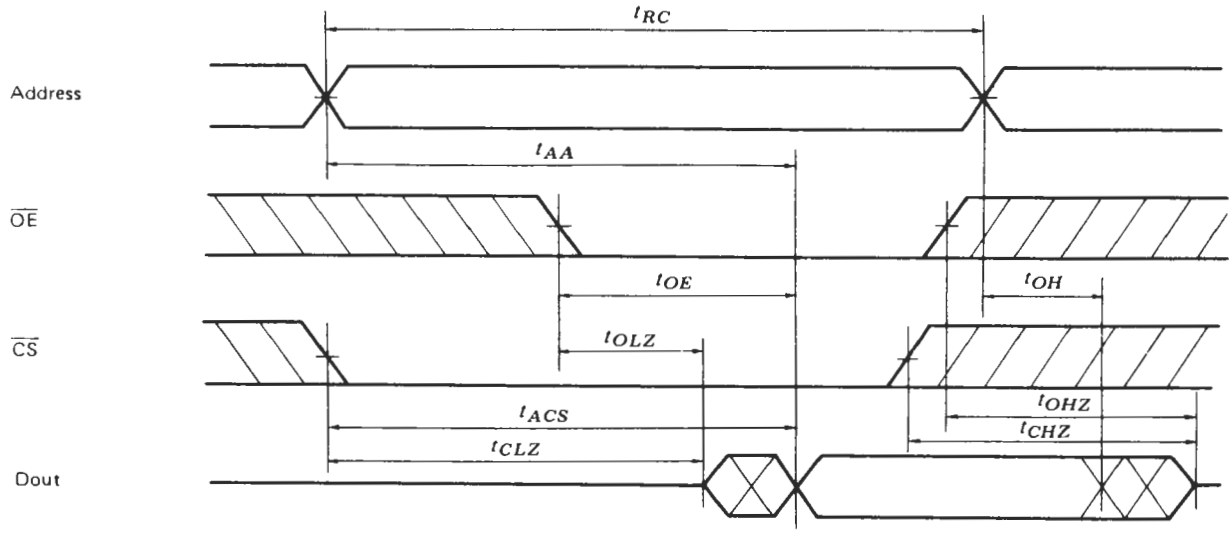
(Including scope & jig)

■ AC CHARACTERISTICS (Ta = 0°C to 70°C, V_{cc} = 5V ± 10% unless otherwise noted.)

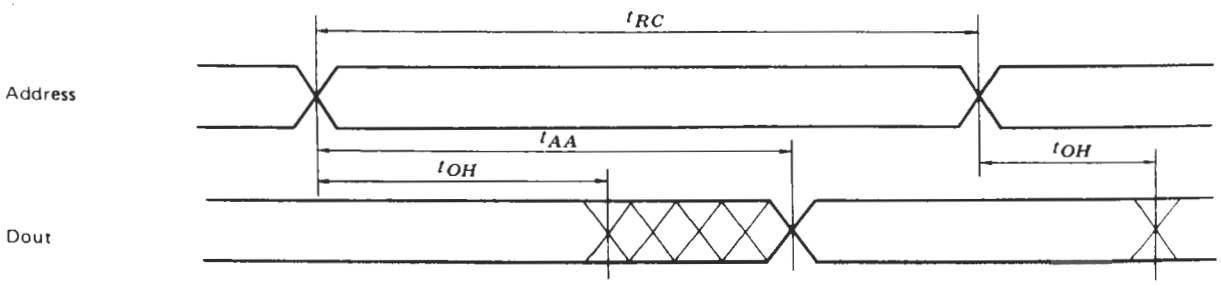
• **READ CYCLE**

Parameter	Symbol	HM6116P-2		HM6116P-3		HM6116P-4		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	120		150		200		ns
Address Access Time	t_{AA}		120		150		200	ns
Chip Select Access Time	t_{ACS}		120		150		200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10		15		15		ns
Output Enable to Output Valid	t_{OE}		80		100		120	ns
Output Enable to Output in Low Z	t_{OLZ}	10		15		15		ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10		15		15		ns

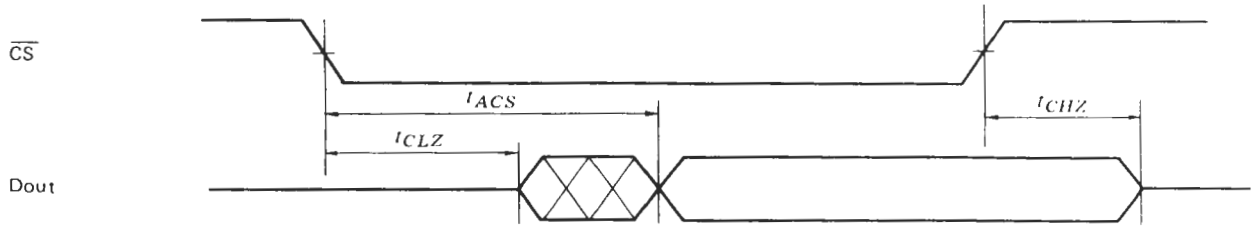
■ TIMING WAVEFORM OF READ CYCLE NO. 1[1, 5]



■ TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4, 5]



■ TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3, 4, 5]

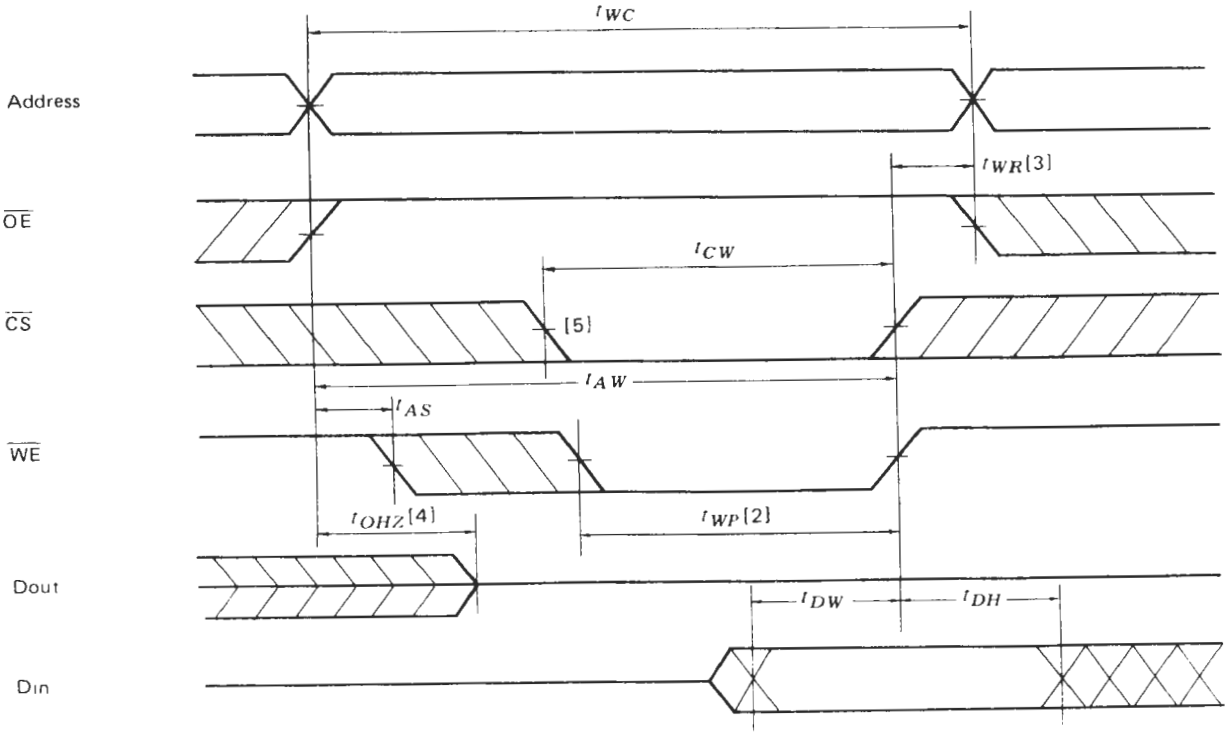


NOTES: 1. WE is High for Read Cycle.
2. Device is continuously selected, CS = V_{IL}
3. Address Valid prior to or coincident with CS transition Low.
4. When CS is Low, the address input must not be in the high impedance state.

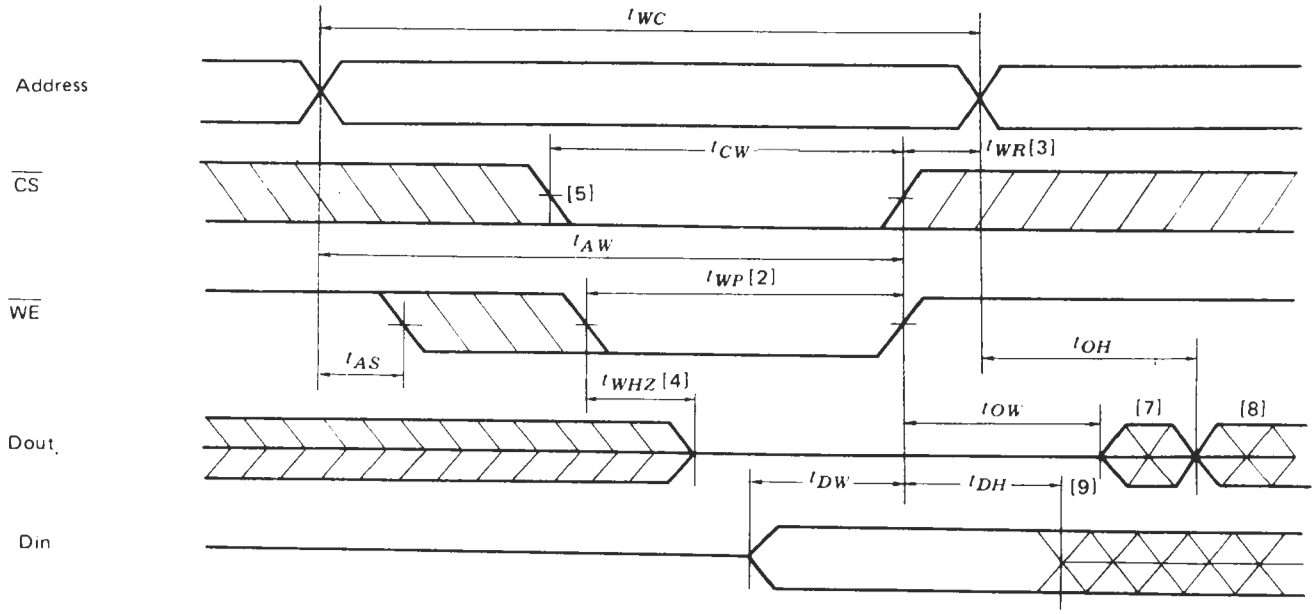
• WRITE CYCLE

Parameter	Symbol	HM6116P-2		HM6116P-3		HM6116P-4		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CS}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

■ TIMING WAVEFORM OF WRITE CYCLE NO. 1[1]



■ TIMING WAVEFORM OF WRITE CYCLE NO. 2[1, 6]



NOTES:
1. WE must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low CS and a low WE.
3. t_{WR} is measured from the earlier of CS or WE going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the CS low transition occurs simultaneously with the WE low transitions or after the WE transition, output remain in a high impedance state.
6. OE is continuously low. (OE = V_{IL})
7. D_{out} is the same phase of write data of this write cycle.
8. D_{out} is the read data of next address.
9. If CS is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

3-25-82
M.T. Wright

MPM Set-up
(48K Banked, 16K Top Common)

- 48K BANKED SLAVE MEMORY, Top 16K MEMORY COMMON.

Set up the MB64 per 2.9.5 except for the following:

a) Do NOT Remove ANY RAM CHIPS.
b) Do NOT jumper E30 to E31.
c) Set Top 8K for RAM.
   E50 to E51
   E53 to E54
   E56 to E57
   E59 to E60
d) Use spare OR-GATE for common RAM
   E31 to U37 pin 1 (74LS32)
   E30 to U37 pin 3
   U31 pin 20 to U37 pin 2