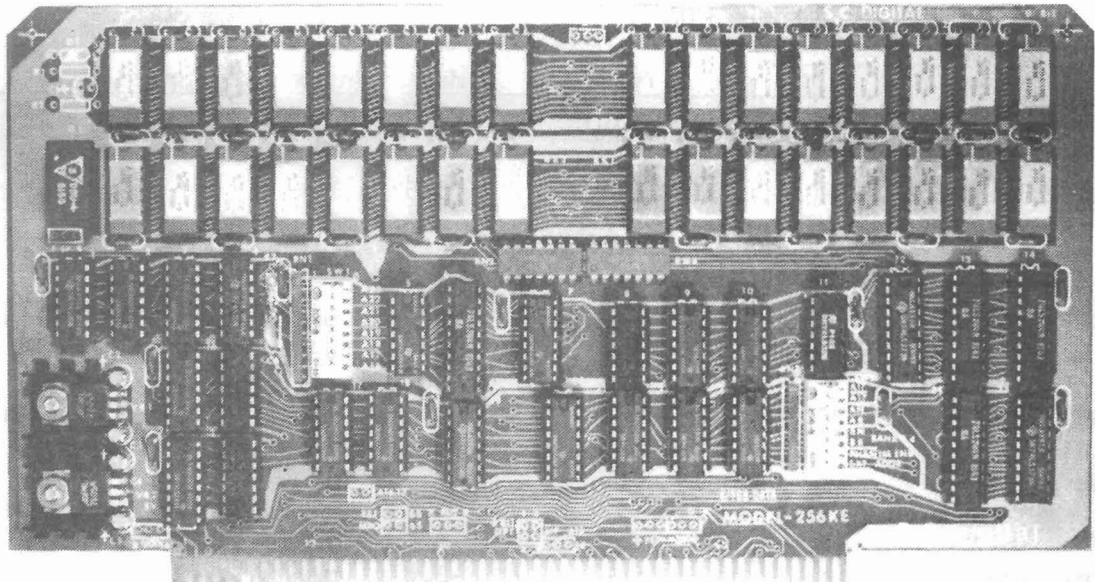
256KB/64KB DYNAMIC RAM



Model 256KE

Features:

* S-100 Bus compatible. Conforms to IEEE696/S100 Specifications(1).
* Cmpatible with 8 bit or 16 bit machines:
  Address: 16 or 24 bit Data: 8 or 16 bit
* Expandable capacity- up to 256kb using 64k by 1 DRAMs in 128kb steps, up to 64kb using 16k by 1 DRAMs in 32kb steps.
* Memory is organized in 2 blocks, each occupying ½ of the addressable space.
* SW settable A0 or A0* Selection of Most Significant Byte (MSB).
* Built in PHANTOM disable, SW selectable.
* Transparent Refresh using Delay Lines, with unlimitted DMA length capability. Volatility is immune to the duration of Wait States, Reset, or Halts.
* Fast Access Time- 180 nsec from SMEMR or PSYNC high. Will operate without wait states in Systems based: Z80/Z8000 to 6mhz, 8080,8085,8088,8086 to 8mhz clock.
* Accomodates both 128 cycle or 256 cycle refresh type of DRAMs.
* All lines Buffered, fully socketed, solder masks legends, Gold Contacts.

Contents

Note 1: This board should interface without difficulty to MITS 8080, INSAI, Cromemco, AlphaMicro, Seattle Computer Products, and similar microcomputer systems.

S. C. Digital
P.O. Box 906
Aurora, Illinois 60507
312-897-7749

Specifications 256K Dynamic Ram Board. Model 256KE

Electrical Characteristics

Parameters	Min	Typ(1)	Max	Units	Conditions
Power Supply Voltages	7.5		10.0	V	25 degree C
Power Supply Current		600		mA	@ 4mhz clock, 256KB
Signal Input Voltages	-0.5		5.5	V	
High level	2.0		5.5	V	
Low level	-0.5		0.8	V	
Hi Level Input Current					Vcc=5.25V
MRQ*,SXTRQ*,PHANTOM*			-0.8	mA	with 3.3k pullup resistor
All others(2)			20	uA	
Lo Level Input Current					
MRQ*,SXTRQ*,PHANTOM*			1.5	mA	with 3.3k pullup resistor
All others(2)			0.36	mA	
Output Buffers					
Hi Voltage Output	2.4	3.1		V	Vcc=5.25V
Lo " "		0.35	0.5	V	IOL=24mA
Hi Level Output Current			-2.6	mA	
Lo " " "			24	mA	

AC Characteristics

Read Time	180 nsec Max	Data valid from SMEMR or PSYNC high.
Read Cycle Time	250 nsec Min	
Write Time	250 nsec Min	Minimum cycle time.

Operating Temperature

Board is warrenteed to operate 5 to 65 degree C ambient with supplied DRAM chips.

Signal Requirement

This board requires MWRT to write into memory. For refresh purpose, it also requires at least one of the following for proper operation:

1) SM1
2) MRQ* and REFRESH*
3) REFRESH* alone which goes active at least 250 nsec from the leading edge of SMEMR or PSYNC active.

In case of 3), REFRESH* must occure frequently enough to meet DRAM requirement, that is at least 128 refreshes for every 2msec.

Note, Z80/Z8000 or 8080,8085,8088, 8086 based systems meet above requirement.

Dynamic Ram type

16K by 1= 4116, 64K by 1= 4164 128 or 256 cycle refresh, all with access time equal or faster than 150nsec.

Note 1; Typical is at 25 degree C.

Note 2: MWRT,PSYNC,SMEMR,SM1,PHLDA,SHLTA,RST*,Φ, A0 through A23,REFRESH*,RDY,XRDY.

Note 3: MRQ* and REFRESH* are not standard IEEE/696 signals but are provided by most of Z80 based CPU's including S. C. Digitals own cpu board, Model CPUI-Z80.

1. Operation

IC's are identified by numbers on the board. For clarity, they will called IC1, IC2,....etc throughout this writing.

Memory Organization

Memory consists of 32 of 64k by 1 (or 16k by 1) DRAMS (Dynamic Rams) chips organized in 4 banks of 64kb (or 16kb) each, Bank 1,2,3, and 4.
In 16 bit data format, the LSB (Least significant bit) A0 select the bank during 8 bit access (SXTRQ*=0) , while two banks are ganged in 16 bit access- bank 1&3, bank 2&4. (BK 1&3=Upper Byte, BK 2&4= Lower Byte)

Addressing

Switch position 1&2 of SW2 labeled A17 and $\overline{A17}$ enables Bank Groups 3&4 and 1&2, respectively. These bank groups occupy lower (BK1,2) and upper(BK3,4) half of the entire addressable space of this board.

Swithc AN of SW2 enables Bank group BK1&3 when A0* is asserted while BN enables BK2&4 when A0 is asserted. AR of SW2 enables bank group BK 1&3 when A0 is asserted while BR enables BK 2&4 when A0* is asserted

Note-normally AN and BN (or AR and BR) should be placed in logic 1 (SW position ON), together.

With AN & BN in logic 1, A0* actuates upper byte while
with AR & BR in logic 1, A0 actuates upper byte.

Extended address lines, A18 through A23 (or A16 thru A23 for 64KB) are compared by IC 18 and 19 with SW1 and this matching information together with absence of PHANTOM* (high level) and A17 or $\overline{A17}$ setting (On) enables its corresponding bank groups.

Data Format

In 8 bit data request (SXTRQ*=logic 0=high level), data lines DI's and DO's are unidirectional. With 16 bit request, (SXTRQ*=1) DI's and DO's are bidirectional with DI's handling lower bytes while DO's, upper bytes.

Memory Operation

Memory READ or WRITE is initiated by the rising edge of SMEMR or MWRT, respectively. This command is transmitted through IC3A, 2B to 2A where RAS and CAS are generated in conjuction with the digital delay line (DL) and the supporting circuitry, IC1,16,27.

If this initiation command arrives while the memory cycle is in progress, such as in refresh cycle, then, this command is stored in IC3A and delayed until the conclusion of the memory cycle. During this time, Wait States are inserted.

The data to or from the RAM is latched into IC 12 and 25 at each READ or WRITE and are presented to the bus on READ cycle.

Refresh

The DRAMS are refreshed by the board generated RAS only. Refresh address is supplied by the counter IC 5.

With Z80/Z8000, refresh begins with assertion of MRQ* and REFRESH*. In Z80, this occurs at the end of every instruction fetch cycle. In Z8000, this is programmable.

For non Z80/Z8000 (Z80-), such as 8080,8086..etc, the normal refresh is queued by SM1. Refresh cycle is generated at the end of SM1 or instuction fetch cycle.

When RST*, Wait State (which is signified by the absence of RDY or XRDY), Halt (SHLTA) or PHLDA (master acknowlege of bus request by such as DMA devices) are

present, the internal counter, IC 26 is actuated counting the clock pulses,Φ.

If no memory READ or WRITE occurs at the end of count, then the momory is refreshed. This insures memory nonvolatility by RST*, not RDY, SHALT (for non-Z80, only) or long waits between DMA's while the bus requesting device is holding the bus. In continuous DMA cycles, memory is refreshed at every memory access.

Extended Addressing and Phantom

Extended address lines A16 through A23 extends address lines to 24 bits from usual 16 bit (for 8 bit machines). Note A16 and A17 are used to specify the memory banks on 256KB board.

Assertion of PHANTOM* disables the board if SW2 position, PHANTM ENB (position 7) is in logic 1. This allows more than one memory devices to occupy the same address space by disabling such as this board.

2. Configuration

This section describes how to modify the board for your particular systems.

Address Setting

This board is designed to have two modes of operation for given DRAMS--the normal 16 bit data format and optional 8 bit format. The board can be made to latter mode by strap option labeled "8 BIT OPT" by cutting PCB connecting 1&4 and 2&3 and reconnecting 1&2 and 3&4.

In normal mode (16B data), SW2 setting covers following address ranges:

SW2 setting	Address range (256KB)		Address range(64KB)		
A17	B+20000	B+3FFFF	8000	FFFF	64KB-16K by 1 DRAMS
$\overline{A17}$	B+00000	B+1FFFF	0000	7FFF	256KB-64K by 1 DRAMS

Where address is hex and B is base address of A18 through A23 setting. Example, A23,A22,A21,A20,A19,A18=110010 then B=C80000

In 8 bit data mode (with 8BIT OPT connecting 1&2 and 3&4) SW2 setting corresponds:

SW2		Range (256KB)		Range (64KB)	
A17	AN	B+30000	B+3FFFF	C000	FFFF
	BN	B+20000	B+2FFFF	8000	BFFF
$\overline{A17}$	AN	B+10000	B+1FFFF	4000	7FFF
	BN	B+00000	B+0FFFF	0000	3FFF
A17	BR	B+30000	B+3FFFF	C000	FFFF
	AR	B+20000	B+2FFFF	8000	BFFF
$\overline{A17}$	BR	B+10000	B+1FFFF	4000	7FFF
	AR	B+00000	B+0FFFF	0000	3FFF

Note: For Z8000 based systems set AN=BN=1=ON
For 8086 based systems set AR=BR=1=ON
IMPORTANT: AN and AR or BN and BR should not be on at the same time.

Important: SW1 positions are in logic 1 when SW is open or off while SW2 positions are in logic 1 when SW is on.
SW1=logic 1=off SW2=logic 1=on

Extended Address

Extended address A16 through A23 is settable by SW1. For 256KB board, A16 and A17 settings have no meaning. To use the extended address, EXT. ADDR (position 8) or SW2 should be in logic 1.

Phantom

PHANTOM* (or memory diable) is enabled by SW2 position (9) labeled PHANTM ENB. This could be in logic 1. otherwise, PHANTOM* is ignored.

Strap Options

Strap options can be divided into two groups-first group is mainly to accomodate different processors while second is for 16k by 1 or 64k by 1 DRAMs.

a. Group 1 : Z80, PSY, RDY, MRQ, REF.

Z80/Z8000 based system with both MRQ* and REFRESH* available can have connections as: MRQ, REF connected and Z80-. Most Z80 based CPU boards, including our own, Model CPUI-Z80 provides these signals, even though it is not IEEE696 specified singals.

Memory read is initiated by SMEMR becoming active. If the system has steady state type (ig latched) at the begining of memory read cycle, then connect PSY+.

If your system doesn't have MRQ* and REFRESH* both, even though it is Z80/Z8000 based, or your system is non Z80/Z8000 based such as 8080,8085,8088,8086, then connect Z80- and open MRQ.

If your system uses pin 65 and pin 66 for other than MRQ*, REFRESH*, then connect Z80- and open MRQ as above.

Note: the board normally comes with MRQ open, and Z80-.

RDY: This board inserts wait state when read or write command arrives while the board is in memory cycle, such as in refresh. This type of situation do not arrise normally but can occure when DMA device is requesting Read right after write with 3 clock cycles for DMA. In some early S100 boards, RDY line is driven by non-open collector type of drivers. For such boards, you might have to reconnect RDY to X meaning RDY is connected to XRDY (pin 3).

b. Group 2

For 16k by 1 DRAMs, strap options and components placed as follows: 1. VDD to 16. 2. A16,17 connected. 3. A17, A15 connected to A15. 4. VR1 should have +12V regulator such as LM340T12, 7812, instead of +5V. 6. A7 should be connected to A7-. 7. Capacitors labeled as 1's (8 total) along memory chips should have 0.01uf,12V placed. 8. Caps labeled as 2's (16 total) should have 0.1uf, 35V placed. 9. R1, 680 ohm, ¼w placed. 10. D1, 1n5231, 5.1V, ½w Zener diode placed. 11. C1, 10uf, 25V placed.

For better reference, see chart below:

DRAMs	type	A16,7	A17,A15	A7	VR1	VDD	D1,C1,R1
64k by 1	4164	open	A17	+	+5V	8	none
16k by 1	4116	close	A15	-	+12V	16	see parts list

For 16k by 1, additional capacitors shold be places as mentioned as above, 7 & 8.

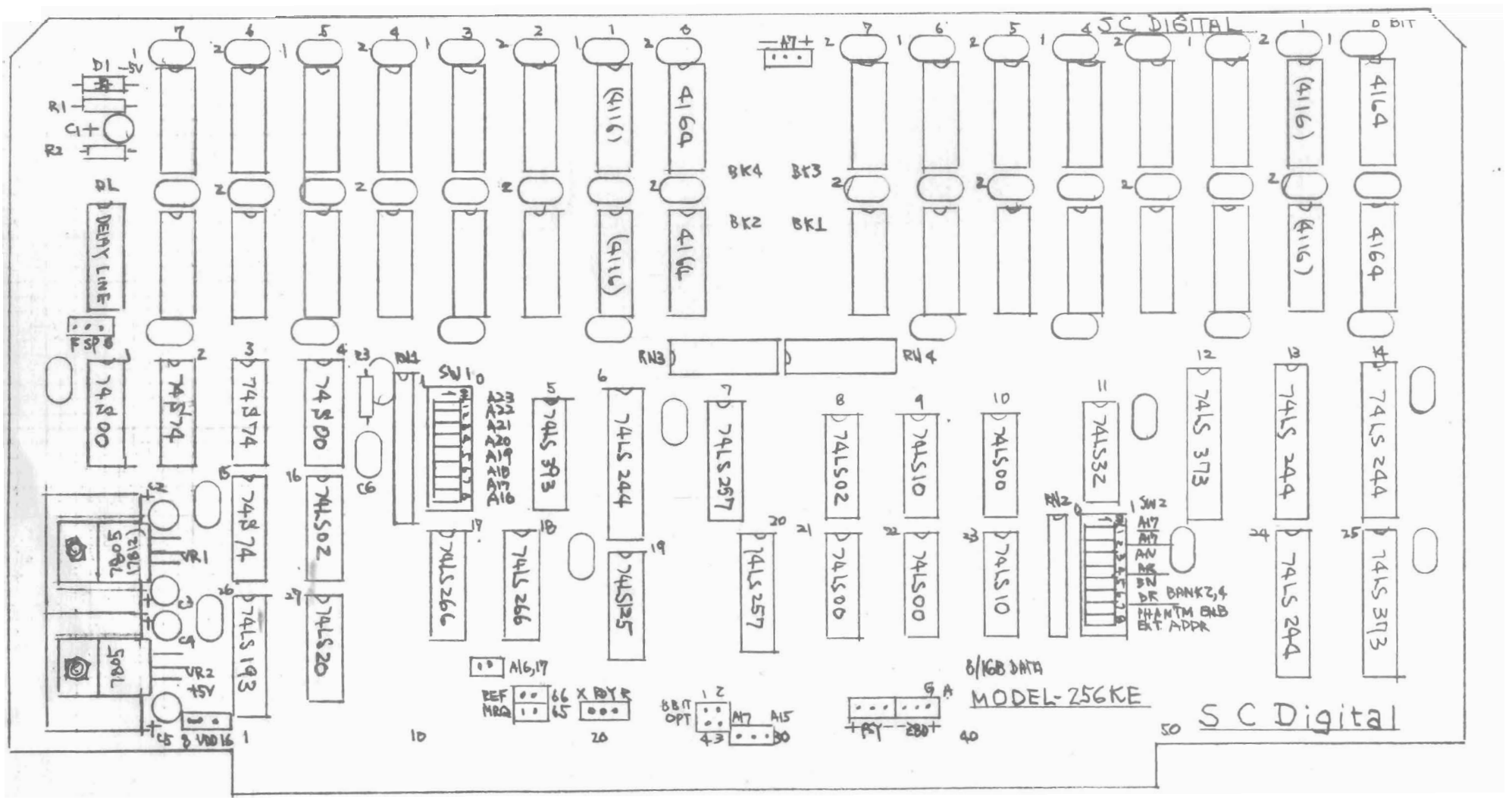
Repair Service

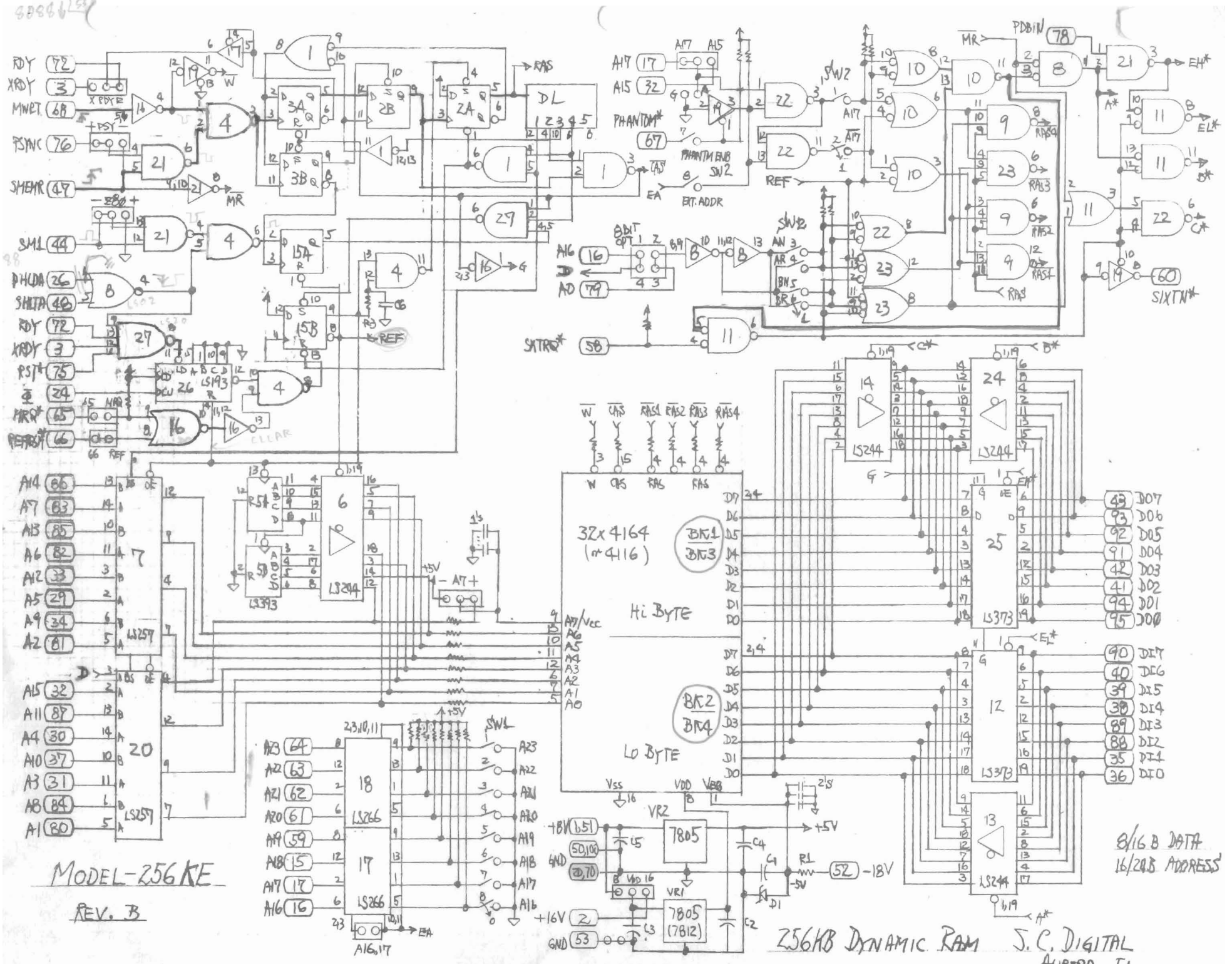
S. C. Digital will perform repair service for its products which are not under warrenty. Owner will be notified prior to any work done, if the cost to him exceeds $35 (excluding transpotation and Insurance cost).

Warrenty covers parts (SCD supplied parts, only), and labor. Owner must ship board or parts prepaid to SCD. SCD will prepay shipping back within the Continental U.S.

Parts List

Quan.	Part	ID
3	74LS00	10,21,22
2	74S00	1,4
2	74LS02	8,16
2	74LS10	9,23
1	74LS20	27
1	74LS32	11
2	74S74	2,3,15
1	74LS125	19
1	74LS193	26
4	74LS244	6,13,14,24
2	74LS257	7,20
2	74LS266	17,18
2	74LS373	12,25
1	74LS393	5
1	2.2k to 4.7k,9R 10pin sip	RN1
1	7R,8 pin	RN2
2	22 to 100 7R,14pin Dip	RN3,4
1	680 ¼w	R1
1	470 ¼W	R3
1	1N5231 5.1V	D1
1	7805(7812)	VR1
1	7805	VR2
1	Delay Line 5taps	DL
1	4.7-10uf,25V	C1
4	10uf,25V	C2,3,4,5
1	100pf	C6
18	0.01uf,25V	1
32	0.1uf,25V	
2	DIP SW,8Pos	SW1,2
18	14pin socket	
35	16pin socket	
6	20pin socket	
2	Heat sink,6-32 Screw,Nut	
1	PCB	




MODEL-256KE
REV. B
256KB DYNAMIC RAM
J.C. DIGITAL
AURORA, FL.
8/16 B DATA
16/20 B ADDRESS
32x4164
(or 4416)
Hi BYTE
LO BYTE
RDY
XRDY
MWRT
PSYNC
SHEMR
SMEL
PHLDA
SHLTA
PSYN
MRQ*
REFRQ*
RAS
CAS
W
REF
MR
EA
EXT. ADDR
PHANTOM*
PHANTM ENB
SW1
SW2
PDBIN
SIXTN*
SXTRQ*
+5V
+16V
-18V
GND
VR1
VR2
7805
7805 (7812)
LS244
LS373
LS257
LS266
LS393
LS193