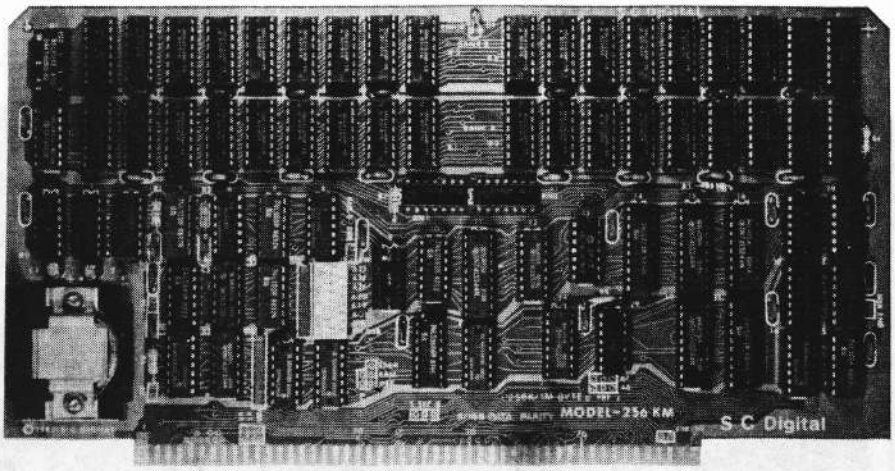
256K/1M DYNAMIC RAM MANUAL



Model 256KM

Features:

* S-100 Bus compatible. Conforms to IEEE696/S100 specifications (1).
* Compatible with 8 bit or 16 bit machines:
  Address: 16 or 24 bit. Data: 8 or 16 bit (via SXTRQ*).
* Accomodates either 64k by 1 or 256k by 1 DRAM chips.
* Parity bit per byte. Parity error returned to CPU via NMI*, VI's*, ERROR* and I/O read, LED(visual indication). Error resettable through I/O write. Return through interrupt line is Maskable. Choice of I/O ports (uses two ports): 7E&7F, 3E&3F, BE&BF or FE&FF, all in Hex.
* Memory is organized in 2 contiguous blocks, with each block occupying one half of the addressable space of 256Kbyte, or 1Megabyte, with provision to populate half of the board with memory chips.
* A0 or A0* selection of upper byte.
* Built in PHANTOM* disable, SW settable.
* Transparent Refresh using Delay Lines, with unlimitted DMA length capability. Volatility is immune to the duration of Wait States, Reset, or Halts. Frequency of Refresh is governed by internal clock.
* Fast Access Time: 175nsec from PSYNC & SMEMR, or PSYNC & PSTVAL* & SMEMR active(2). Will operate without wait states in systems based: 8080,8085,8088,8086,80186,80286,68000 to 8mhz, Z80,Z8000 to 6mhz.
* Accomodates both 128 cycle or 256 cycle refresh type of 64k by 1 DRAMs.
* All lines buffered, fully socketed, solder masks, legends, Gold contacts.

Contents:

Note 1: This board should interface without difficulty to MITS 8080, IMSAI, CROMEMCO, ALPH MICRO, Seattle Computer Products, Compupro, Lomas Data, Dual and similar Microcomputer Systems.

Note 2: 195nsec access time for PSYNC & PSTVAL*(leading edge sensitive) & SMEMR.

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Specifications 256K/1M Dynamic Ram Board. Model 256KM

Electrical characteristics

Parameters	Min	Typ(1)	Max	Units	Conditions
Power Supply Voltages	7.5		10.0	V	25 degree C
Power Supply Current		900		mA	256KB, 6mhz
Signal Input Voltages	-0.5		5.5	V	
High Level	2.0		5.5	V	
Low Level	-0.5		0.8	V	
Hi Level Input Current					Vcc=5.25V
SXTRQ*,PHANTOM*			-0.8	mA	3.3K pullup resistor
SMEMR,PDBIN,PSYNC			40	uA	
All others(2)			20	uA	
Lo Level Input Current					
SXTRQ*,PHANTOM*			1.5	mA	3.3K pullup resistor
SMEMR,PDBIN,PSYNC			0.72	mA	
All others(2)			0.36	mA	
Output Buffers					
Hi Voltage Output	2.4	3.1		V	Vcc=5.25V
Lo " "		0.35	0.5	V	IOL=24mA
Hi Level Output Current			-2.6	mA	
Lo " " "			24	mA	

AC Characteristics (using 150nsec memory chips)

Read Time	175nsec Max	Data valid from leading edge of SMEMR & PSYNC active
	195nsec Max	" " " " " " SMEMR & PSYNC & PSTVAL*
Read Cycle time	250nsec Min	
Write time	250nsec Min	Minimum cycle time
DMA Transfer	500nsec Min	or 2mega byte per second maximum

Operating Temperature

Board is warrenteed to operate 5 to 65 degree C ambient with supplied DRAM chips.

Signal Requirement

This board requires MWRT to write into memory (IEEE696 requirement).
For refresh purpose, it also requires SM1.

Dynamic Ram Type

64K by 1=4164, 128 or 256 cycle refresh, access time equal or better than 150nsec.
256K by 1=41256, 256 cycle refresh, access time equal or better than 150nsec.

Note 1: Typical is at 25 degree C.
Note 2: MWRT,PSTVAL*,SM1,PHLDA,SHLTA,RDY,XRDY,RST*,SINP,SOUT,A0 thru A23,PHI.

1. Operations.

Model 256KM is Dynamic Random Access Memory (DRAM) board designed to conform to IEEE696/S100 specifications. It can house 64K or 256K DRAM chips, making it 256kbyte or 1mega byte on board. It is capable of transfering 8 or 16 bit data at a time. This section is to explain how the board works.

Memory organization.

Memory consists of 36 DRAM chips, organized in 4 banks, Bank 1,2,3 and 4, and 1 parity for each bank. The LSB(least significant bit) of address line, A0, selects bank during 8 bit access which signified by SXTRQ*=0=hi level, while two banks are ganged in 16 bit data access, Bank 1&2 (called Bank A), Bank 3&4 (Bank B). Bank 1 and 3 handles low bytes while Bank 2 and 4, high bytes. Bank A covers one half of the addressable space while Bank B covers the other half.

Addressing.

The board is essentially a 256kbyte or 1mbyte block with a capability to disable half of the board via strap option "BNK B ENB". Address line A17 (or A19) selects Bank A or Bank B depending on whether A17 (or A19) is low or high level. SW position 7 (SW-7), labeled 'MB' enables to reverse the selection of Bank A or Bank B by A17 (or A19).

A Strap option labeled 'A0' enables to reverse the selection of high or low byte by Address line A0 in 8 bit access, to accomodate different 16 bit machines.

The rest of the extended address line A18 through A23 (or A20 through A23 for 256K DRAMs) are compared by IC24 and 25 with SW setting and this matching information, together with absence of PHANTOM*(high level), enables the board. MB specifies the Bank group-Bank A or Bank B.

Data Format.

During 8 bit data requests(SXTRQ*=logic 0=high level), data line DI's and DO's are unidirectional. With 16 bit requests, DI's and DO's are bidirectional with DO's handling low bytes while DI's, high bytes.

Memory Operations.

Memory READ or WRITE is initiated by leading edge of (PSYNC & SMEMR) or MWRT, respectively. The READ can be further modified by strap option 'PST'. For detail see below under memory read in second section.

Read or Write command is used to generated RAS and CAS at IC2A in conjuction with digital delay line(DL) and IC1. The data to and from the DRAM is latched into tIC14 & 31 at each Read or Write and presented to the bus on Read cycle in conjuction with PDBIN and SXTRQ*.

Refresh.

The DRAMs are refreshed by the board generated RAS only. Refresh address is furnished by a 8 bit binary counter, IC10.

Refresh is queued by SM1, but the frequency of refresh is controlled by the internal clock, IC5. During DMA transfers, refresh is queued by memory READ or WRITE, and again, the frequency of refresh is governed by the same way as SM1 case.

When RST*, Wait States (which is signified by the absence of RDY or XRDY) or HALT is present, the internal counter IC19 is activated, counting the clock pulses, PHI. If no memory activity occures at the end of count, then, refreshed is queued. This insures Memory non-volatility by RST*, not RDY, not XRDY, or SHLTA.

Extended Addressing and Phantom.

Extended address A16 through A23 extends the address lines to 24 bits from usual 16

bit. Note A16 and A17 (or A16 through A19 for 256K DRAMs) are to specify the memory banks, while A18 through A23 (or A20 through A23) are selectable by SW.

Assertion of PHANTOM* disables the board if SW position 8, PH DSB, is so actuated. This allows more than one momory device to occupy the same address space.

Parity.

Parity bit is generated and stored on each momory WRITE, one parity per byte basis. Parity is again generated on each READ and checked against the stored parity bit.

When error occures, this information is stored in a flip flop, IC32A. The parity ERROR flag readout is controlled by I/O ports (uses two ports but both fuctions same) and in 3 ways-I/O read, interrupt, or visual by LED.

Error return through interrupt line occures at the same time as the presence of data on memory READ. Presence of interrupt is sensed on last clock cycle for most microprocessors. For this reason, the actual interrupt can occure right after the read operation. One can use this fact to find the location of memory where error has occured.

2. Configurations

This section describes how to modify the board for your particular systems.

256K DRAMs

To use 256K DRAMs instead of 64K DRAMs, followings has to be done:

1) 74LS00 has be be inserted on IC9. 2) Strap labeled 'AD' should be cut.
3) Strap labeled 'RAM' shoud be conncted to 256K instead of 64K.
4) 256K by 1 DRAM chips (36 of them) inserted instead of 64K by 1 DRAM chips.

Address Setting.

This board is designed to cover contiguous 256Kbyte or its half for 64K DRAM's, or 1Mbyte or its half for 256K DRAM's. It is organized in two BANKs, BANK A & BANK B. SW position 7 labeled 'MB' places the banks in either upper or lower half. The corresponding bank and SW-7 setting is as follows:

MB (SW-7)	logic 1 (open)	logic 0 (on)
BANK A	lower	upper half
BANK B	upper	lower half

MSB=A17 for 64K DRAM
=A19 for 256K DRAM

As half populated board, memory chips should be placed on BANK A, and the strap option, 'BNK B ENB' cut at solder side.
As fully populated board, SW-7 position can be in logic 1 or logic 0 with logic 1 as prefered position.

Rest of the address setting should be as desired with logic 1=open.
When the board is populated with 256K DRAMs, A18 and A19 on SW has no meaning.

For 16bit address line machines (with global addressing), make sure no S100 bus lines that are reserved for the Extended Address lines are used. When this condition is met, one can assure A16 through A23 are all in high level. Set SW, assuming this fact, i.e. A17 through A23 in logic 1 (open).

A0 setting (Strap option) has special meaning for 16 bit data machines, only. For all 8 bit requests (SXTRQ*=logic 0=hi), A0 selects high or low bytes, as follows:

A0 strap	Cut (normal)	Connected
Even address(A0=0)	low byte	high byte
Odd address(A0=1)	high byte	low byte

For 8086 processors, A0 should be cut. This is way the board is supplied and in this configuration, conforms to IEEE696 spec. For some Z8000 machines, 'A0' should be connected.

Memory Read.

Initiation of memory READ cycle is at the leading edge of PSYNC & SMEMR active (normal mode). This can be modified by strap option labeled 'PST' connected. With 'PST' connected, it is at PSYNC & SMEMR & PSTVAL* active. active.

Memory read can be initiated by leading edge of PDBIN. For this option, disconnect from S in strap option 'SYC' and connect to B, and leave 'PST' not connected.

Phantom.

PHANTOM* is enabled by SW-8 labeled 'PH DSB'. This position should be in logic 0 (on), otherwise, PHANTOM* is ignored.

Parity.

Parity generation, checking and error recording on each memory READ cycle is done automatically. Error return, error flag reset, and masking on imterrupt line is done by software, via I/O ports. It uses two ports but both has same function. I/O port address is basically FE & FF hex with top two bits reversable by strap option labeled as A7 & A6. Board as comes has 7E & 7F hex.

Parity error can be returned to CPU via interrupt type or lines by strap option (normally all open), and they are: ERROR*, NMI*, VIO* through VI7*, or INT*. Only one jumper should be placed as desired.

Upon RESET, interrupt is masked out, disabling interrupt due to parity error. User has to enable interrupt via software by taking mask off. This can be done by I/O write bit 7=1 to the I/O port. Also, mask can be On (interrupt disabled) by I/O Write bit 7=0 to the I/O port. I/O Write to the ports resets the parity error flag.

Status of the parity error flag can be read by I/O Read: bit 7=1 if error. No other bit is significant.

By cutting trace 'MSK ENB' strap option, mask is always off.

Memory has to be 'scrubed' to have meaningful parity bit, after power up. This can be done by writing to every memory location that will be read.

Repair Service

Repair service is available at the factory for any products manufactured by S. C. Digital. For items under warrenty, there is no charge for this service. For repair of this board when it is no longer under warrenty, return the board to the address shown below with a check for $35. If the repair and return shipping can be accomplished for the amount, the work will be done and the board returned along with a check for any overpayment. If the cost of repair exceeds this amount, you will be notified before any work is done. Ship all returning board to:

S. C. Digital, Inc
1240 N. Highland Ave Suite 4
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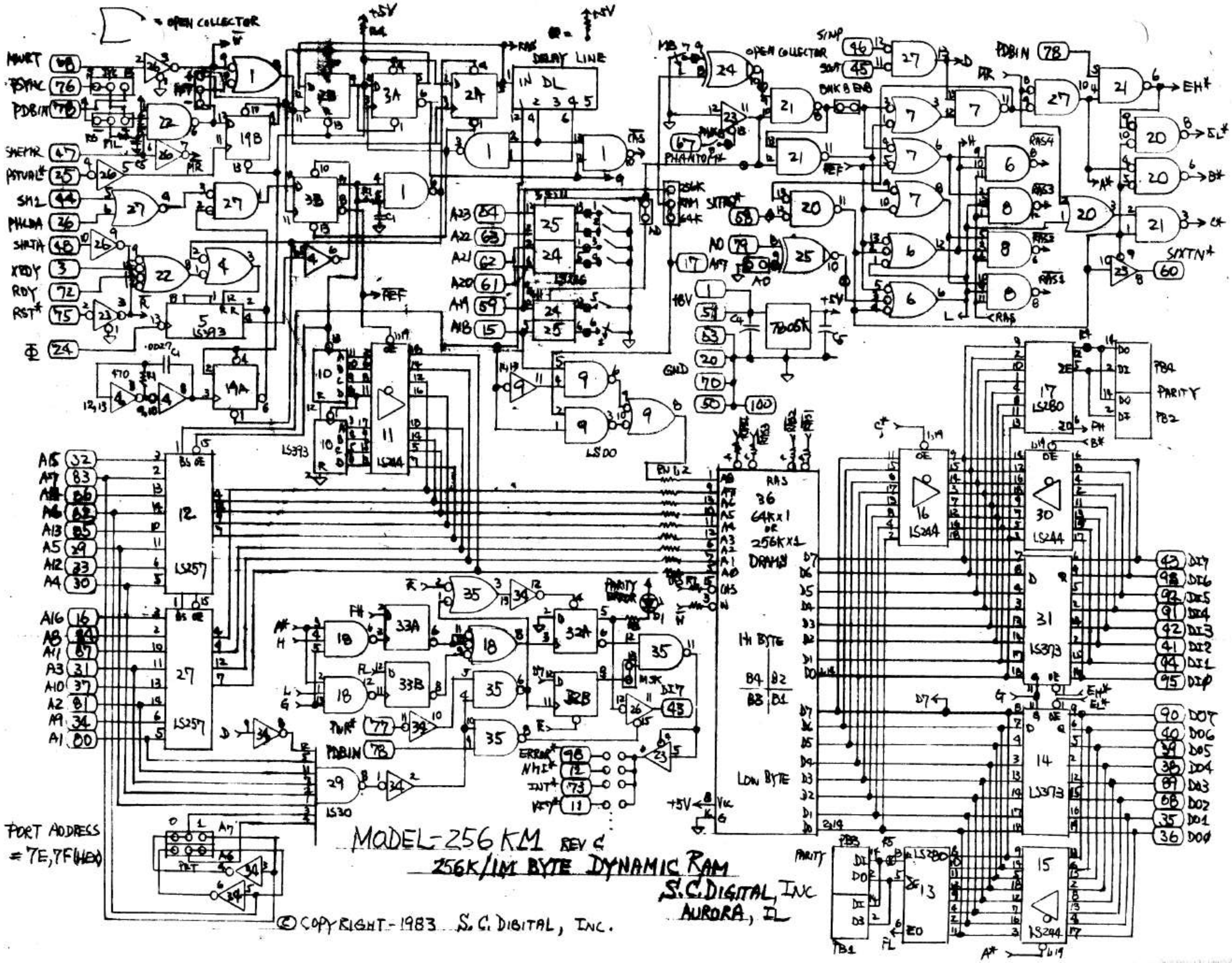
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