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MEASUREMENT systems & controls incorporated

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TITLE

TECHNICAL MANUAL

Model DM6400 Series, S-100 Dynamic Memory Boards

SIZE	DOCUMENT NUMBER	REV.
A	TM-DM6400 Series	A

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1.0 Memory Features

The memory board you have purchased from Measurement Systems & Controls is a state of the art product which incorporates features not normally found in similar memory products. The incorporation of these features has been the result of a thorough research of existing dynamic memories, as well as long and exhaustive conversations with dynamic memory users. We are very proud of the successful implementation of these ideas into our product, and firmly believe that these features differentiate us from the other memory board manufacturers. It is for this reason that they will be introduced and explained to you first before the theory of operation of the board is attempted.

Memory Interface

The memory board interfaces to the CPU through a 100 line computer bus, the S-100 BUS. Not all 100 lines are used with the memory board, nor have all lines been defined by the CPU suppliers.

The memory board follows the conventions established by early S-100 BUS users, as well as the latest attempt by the IEEE to standardize the S-100 BUS.

The following lines interface to the memory.

* 16 Data Lines
* 16 Address Lines
* 5 Status Lines
* 8 Control Lines
* 1 Clock Line ($\emptyset_2$)

DATA LINES - There are two groups of 8 data lines. Eight data lines are the input to the processor (DIØ-D17). Eight data lines are the output from the processor (DOØ-DO7).

ADDRESS LINES - Sixteen address lines are used to identify a particular address location within the memory. Sixteen lines are sufficient to address 65,536 locations in memory. Each location can store 8 bits of information, one BYTE. The memory board can store 65,536 bytes of information in its fully implemented version (DM6400).

STATUS LINES - The memory board utilizes the following Status Lines from the CPU board or from the Monitor Board.

* SMEMR (Memory Read)
* SM1 (M1 Status Line)
* SINTA (Interrupt Acknowledge)
* SINP (Input Operation from a peripheral, other than memory)
* SOUT (Output Operation to a peripheral, other than memory)

These signals are used to either control the operation of the memory or to disable it, during the times when the memory is not being used as part of a machine cycle. The utilization of these lines by the memory board will be defined later in other sections of this technical note.

CONTROL LINES - The memory board utilizes the following control lines:

* MWRITE (Memory Write)
* PDBIN (Processor Data Bus In)
* PSYNC (Processor Sync Pulse)
* PWAIT (Processor Wait)
* PHANTOM (Memory Disable)
* PRESET (Processor Reset)
* PRDY (Processor Ready Line)
* XRDY (Processor Ready Line)

These lines are used to start the read and write cycles of the memory. They are also used to make the processor wait for memory when operating with a floppy disc or slow memory. Their full characterization and interfacing to the memory will be given later.

CLOCK LINE - The 8080 microprocessor uses two (2) clocks to synchronize and reference all system signals, while the Z80 uses one. The IEEE, trying to resolve this compatibility problem between the major microprocessors in use today, defined a single synchronizing signal, called Phase two Clock ($\emptyset_2$). This signal corresponds to the Phase two Clock ($\emptyset_2$) defined for the 8080 microprocessor and to the Phase Clock (Φ) defined for the Z80 microprocessor. The DM6400 series memory boards use the IEEE convention and reference all external and internal timing signals to a single clock, $\emptyset_2$.

Signal Buffering

The DM6400 series memory boards use RC filters and buffers on the address and critical control lines. The purpose of the RC filters is to guarantee compatible operation of the memory board with 4 MHz CPU's on long, unterminated S-100 busses. The filters prevent false addressing and false memory timing on a long bus that characteristically exhibits voltage spikes and ringing.

The low power Schottky (LS) buffers minimize loading of bus source drivers and provide additional noise immunity by the use of Schmitt trigger devices. The input filters and LS buffers are compatible with both terminated and unterminated busses.

Internal Sync

The main memory clock CPO is generated by a crystal oscillator running at 25 MHz. The period of this frequency (T=40 nsec), defines the uncertainty of a timing event. This is important because most of the control signals on the BUS are pseudo-synchronized to this internal clock (CPO), by means of D-type Flip Flops. The internal signals are synchronized to the external BUS signals within a 40 nanosecond time window, the synchronism uncertainty window.

A special set of mnemonics has been generated to identify internal control signals, which were generated from external BUS signals. For instance:

* PSYNC is a BUS signal.
* PSYNCB is the Buffered internal signal.
* PSYNCBS is the Buffered and Synchronized internal signal.
* PSYNCBSD is the Buffered, Synchronized and Delayed internal signal.

These mnemonics will become meaningful when reviewing the Theory of Operation and the schematic logic diagram.

Memory Address Select/Deselect

The memory board is normally one of many boards associated with the CPU. Since the address lines go to every user on the BUS, address selection logic is provided to enable or disable sections of address spaces used by other boards. The Logic can:

* Select 4K bytes of memory at 16 distinct boundaries. (0000H, 1000H, . . .F000H)
* Select 8K bytes of memory at 8 distinct boundaries. (0000H, 2000H, . . .E000H)
* Select 16K bytes of memory at 4 distinct boundaries. (0000H, 4000H, 8000H, C000H)
* Select 32K bytes of memory at 2 distinct boundaries. (0000H, 8000H)

Whenever a portion of memory has been selected, the remaining is deselected. For instance, assume that the first 4K bytes starting at 0000H are selected. Then the remaining 60K bytes are not addressable. By the same token, 16K bytes starting at C000H can be selected, the remaining lower 48K bytes from 0000H to BFFFH are deselected.

A more useful feature is to be able to deselect portions of memory at will. This is accomplished by the MEMORY DESELECTION LOGIC, which is the same logic associated with the MEMORY SELECTION. The Logic can:

* Deselect 4K bytes of Memory at 16 distinct boundaries.(0000H, 1000H, . . . F000H)
* Deselect 8K bytes of memory at 8 distinct boundaries.(0000H, 2000H, . . .E000H)
* Deselect 16K bytes of memory at 4 distinct boundaries. (0000H, 4000H, 8000H, C000H)
* Deselect 32K bytes of memory at 2 distinct boundaries. (0000H, 8000H)

If a system has a 4K byte MONITOR, it can be placed anywhere in memory. The remaining 60K bytes are automatically selected. Larger portions of memory can be deselected and used to locate ROM's programmed with higher level languages (BASIC, FORTRAN IV, PASCAL, etc.).

Two dip switches, each one containing 4 switches, select or deselect memory. A CODE is associated with the selection/ deselection of a particular portion of memory. The CODE is entered by setting the switches to either a 1 (push the upper portion of the switch) or a 0 (push the lower portion of the switch).

The following abridged tables define all the valid codes for the Selection and Deselection Logic.

Description	SW-1 A B C D	SW-2 A B C D
16 - 4K byte BANKS	1 1 1 1	x x x x
8 - 8K byte BANKS	1 1 1 0	x x x 0
4 - 16K byte BANKS	1 1 0 0	x x 0 0
2 - 32K byte BANKS	1 0 0 0	x 0 0 0
Selection Code		
16 - 4K byte BANKS	0 1 1 1	x x x x
8 - 8K byte BANKS	0 1 1 0	x x x 0
4 - 16K byte BANKS	0 1 0 0	x x 0 0
2 - 32K byte BANKS	0 0 0 0	x 0 0 0
Deselection Code		

Consult the Appendix for a whole table containing the 60 valid CODES.

There are other times when it is desirable to deselect the whole memory, in order to prevent it from writing on the BUS or reading the BUS. The following cases are of interest.

* During a Power ON reset
* During a Reset cycle
* During a PHANTOM operation
* During an INPUT operation
* During an OUTPUT operation
* During an Extended WAIT operation
* During an INTERRUPT ACKNOWLEDGED operation

System Reset and Extended Wait States

It is imperative that dynamic memory devices be refreshed often enough to retain their data. Two cases where refresh is critical are during system reset or extended wait states.

System reset is initiated by depressing the reset button. This grounds BUS pin 75 (PRESET), causing all CPU operations to cease. When this occurs, a latch is set which disables reads or writes and enables internal refresh.

An extended wait state is caused when a memory or I/O asserts the PRDY or XRDY lines to the processor. The processor in turn generates PWAIT, indicating that the processor is waiting for the memory or I/O device to complete its function. This only becomes a refresh problem when the wait state extends for several microseconds, such as occurs with some types of floppy disk controllers or an IMSAI type front panel. The PWAIT signal is received from the bus and control logic times 5, Ø2 clocks. After the 5 clocks are counted, the logic compares this count with PRDY, XRDY or the reset latch and enables refresh until PRDY and XRDY are reset and the reset latch is cleared. The reset latch is cleared by the first normal refresh generated after the processor starts up again. This assumes that the first instruction after a reset will not come from the dynamic RAM board.

Phantom Line Operation

After a power ON or system reset it is usually desirable to have a monitor board or bootstrap PROM take control of the system operation. However, most CPU's will commence execution at location 0000H, an area usually occupied by RAM. One way to avoid conflict between the RAM and the monitor or PROM is to set BUS pin 67, the PHANTOM line, to a low condition. When this line is low, the output buffers to the DI bus are disabled. However, memory cycles continue to take place. This will allow the monitor or PROM to move data into RAM while the PHANTOM line is low.

If pin 67 on your system is not used for this function, jumper area E should be cut and pad 16 wired to pad 14 for a pull up.

I/O and Interrupt Mode Selection

During I/O and Interrupt Acknowledge cycles it is necessary to disable the output buffer of the RAM. However, the RAM will continue to execute reads and refreshes.

When any of these inputs are asserted, the SELECT signal will go low. The absence of board select disables the output buffers to the DI bus as well as the output of the optional wait state generator.

SINTA (BUS pin 96) is also received and is used to disable board select. If BUS pin 96 does not function for interrupts in your system, cut the etch at jumper area D and wire pad 12 to pad 13, disabling this signal.

DMA Compatibility

DMA operations involve an exchange of bus control between the processor card and an I/O device. The processor responds by raising pin 26 (PHLDA) granting control to the I/O device. The I/O device must then assert the necessary processor signals while removing the corresponding processor outputs from the bus. This will generally involves pulling low, BUS pins 19 (CCDSBL), 22 (ADDR DSBL), and 23 (DODSBL). BUS pin 18 (STAT DSBL) will generally not be pulled low by any but the most complex DMA controllers, as these signals are not required to control memory operations.

Whatever signals are disabled from the processor must be enabled from the DMA controller. It is important to the memory board that the minimum amount of bus noise be generated by this exchange. The best way is for the DMA controller to execute the following sequence of operations when PHLDA is received:

1. Assert all signals to be disabled (in their inactive state).
2. Pull the appropriate disable pins to remove the processor from the bus.
3. Generate the appropriate signals to perform the memory cycles necessary.
4. Raise the disable pins.
5. Remove all outputs being generated by the DMA board, including PHOLD.

The timing signals necessary to drive the memory board are minimal. For memory writes, a PSYNC signal is not necessary as long as the MWRITE signal (BUS pin 68) is at least 350 ns wide.

For memory reads, a PSYNC is required if the memory board is set up for an 8080 processor; in this case the PSYNC causes the read operation. For memory read with a Z80 processor, the operation may be initiated by either PSYNC or RDENSEL (Header 1, pin 9) which will be jumpered to either SMEMR or PDBIN, according to what kind of Z80 processor you are using. The data read will appear on the DI bus as long as RDENSEL is asserted and the board is otherwise selected.

For an 8080, refresh is enabled on each PDBIN ANDed with $\overline{\text{Ø2}}$. For Z80's, refresh is enabled after each M1 read. The refresh oscillator is designed to refresh more often than necessary 91 KHz actual versus 64 KHz required) in order to allow some refreshes to be skipped. However, skipping too many in any one 2 ms period can potentially cause loss of data.

2.0 Theory of Operation

The design of the memory board is centered around the 4116 dynamic RAM chip, organized as 16K x 1 bit. Thirty-two of these devices are required for a 64K x 8 bit memory array and are arranged as four rows of 16K x 8 bits. The lower 14 bits (A0-A13) of the 16 bit address are used to directly address each of the four rows of memory and the highest 2 address bits (A14, A15) are decoded to determine which of the four rows is actually being addressed.

The 4116 has seven address inputs and requires a multiplexer to decode all 14 address inputs. The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ inputs to the 4116 are used to multiplex the row and column addresses, each seven bits long, into the 4116 to construct a 14 bit actual address. The $\overline{\text{WR}}$ input determines whether the RAM is being read from ($\overline{\text{WR}}$ is logic 1) or written into ($\overline{\text{WR}}$ is logic Ø).

Data being read by the CPU is available from the 4116 on its Data out (DO) line and is latched into Z35, a tri-state device, at the appropriate time. Z35 is enabled onto the S-100 bus by the ANDing of the read signal (either PDBIN or SMEMR, depending on the particular CPU board used) and SEL. SEL is generated whenever the memory board is selected.

Data to be written into memory is buffered by Z34, a line receiver and connects directly to the 4116 data in (DI) input.

The memory circuit contains three distinct timing cycles-memory read, memory write and memory refresh. The first two cycles require the 16 bit address from the S-100 bus while the refresh cycle uses an internally generated 7 bit counter address which

refreshes each memory location in succession. Z36 performs the necessary address multiplexing previously discussed and also contains the refresh counter. During the read or write cycle, the REFEN input to Z36 is a logic 0 and the seven address output lines (MA0-MA6) contain either the row (lower 7 address lines) or column (upper 7 address lines) address for the 4116 depending upon the state of the ROWEN input to Z36. When REFEN is a logic 1, MA0-MA6 are the output of a seven bit counter which contains the refresh address. (Only seven address bits are needed for refresh corresponding to the 128 rows of memory internal to the 4116. Each time a single row is addressed, an entire column corresponding to 128 bits is refreshed.)

The $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WR}}$ signals necessary for the 4116 as well as REFEN and ROWEN are generated by Z42. Z42 in turn requires a set of timing pulses, generated by Z47. A description of this timing follows for the three different memory cycles. The actual details of the three memory cycles vary slightly depending on the type of CPU board used. All 8080 CPU boards function the same. However, depending on the particular Z80 CPU board used, the timing will vary slightly. Refer to the appropriate timing diagram.

8080 and Z80 Operations

A read cycle is initiated by the rising edge of PSYNC for the 8080 and either SM1 for a Z80 M1 cycle or RDENB (PDBIN or SMEMR) for a Z80 M2-M5 cycle. Z46A, Z46B, Z45C, and Z51B detect and latch the rising edge of these signals. When $\overline{\text{MBUSYBS}}$ (Z51B-6) is set to a logic 0, START (Z43D-8) goes to a logic 1. This removes the clear from shift register Z47 and sets its shift right input to a logic 1. At the next rising edge of the 25 MHz clock, T1 (Z47-3) goes to a logic one. T1 is an input to Z42 and sets one of the four $\overline{\text{RAS}}$ lines to a logic 0 depending on address bits A14 and A15. (These two address lines are decoded by Z42 into one of the four $\overline{\text{RAS}}$ outputs.) The falling edge of $\overline{\text{RAS}}$ latches the row address into the appropriate RAMs. The next rising edge of the clock (40 ns later) causes T2 (Z47-4) to be a logic 1. ROWEN becomes a logic 0 causing Z36 to output the column address. Forty nanoseconds later T3 (Z47-5) goes to a logic one, setting $\overline{\text{CAS}}$ to a logic 0. This latches the column address into the RAMs. During a read operation, the R/$\overline{\text{W}}$ input to Z42 is a logic one. When either T6, T7, or T8 occurs, depending on the type of CPU board, $\overline{\text{WR}}$ (Z42-10) is set to a logic 1 and the 4116 completes a read cycle. When MBRSEL (either T7 or T8) goes to a logic 1, MBUSYBS is set to a logic 1, initializing Z51B for the next read cycle.

Z80 (4 MHz)

The write cycle for all Z80 CPU boards operating at 4 MHz is similar to the read cycle just described. For 4 MHz memory board operation, the occurance of either SM1, RDENB, or PSYNCSEL will cause the start of a memory cycle. For a write operation, PSYNCSEL is the only signal that occurs. The rising edge of PSYNCSEL causes START to go high with the succeeding generation of RAS and CAS just as described for the read cycle. The only differences in the timing is that before MBRSEL occurs, causing the resetting of MBUSYBS to a logic 1, AMWRITEB (addressed write signal) occurs and is ORed with MBUSYBS to generate START. Thus the START signal stays high until MWRITEB goes to a logic 0. This allows either T6 or T7, depending upon the CPU board used, to clock T4 of Z42 which in turn samples its R/W input, now a logic 0. The R/$\overline{WR}$ output of Z42 goes to a logic 0 and causes the addressed RAMs to do a write operation.

Z80 (2 MHz)

The write cycle for a 2 MHz Z80 CPU board is very similar to the cycle just described except that PSYNCSEL is a logic 1 (by header selection) and is not used to START a memory cycle. Only the AMWRITEB signal itself is used with the write cycle starting with the occurance of its rising edge. All succeeding timing is as before. The reason for this difference is that at 2 MHz AMWRITE is wide enough that PSYNC is not needed to stretch the write cycle timing.

8080

The 8080 write cycle is identical to the Z80 at 2 MHz with one exception. PSYNC is used to START both the memory read and write cycles. As a result, before AMWRITE occurs a false read cycle is performed with no consequences since the output data buffer, Z35 is disabled during a write cycle. (RDENB is not generated). The succeeding AMWRITE generated START executes a valid write operation.

Refresh

The refresh cycle is performed transparently to all CPU boards by executing the refresh operation during an unused time in the CPU timing. For all Z80 CPU boards this occurs after the trailing edge of SM1 and for all 8080 CPU boards this occurs after the leading edge of the ANDing of PDBIN and $\overline{\emptyset_2}$. Once the refresh cycle is started, it is identical for all Z80 and 8080 CPU boards.

Refresh must occur for all 128 rows of each RAM within 2 milliseconds if all data is to be retained. Thus one of the 128 rows must have a refresh memory cycle performed at least every 15.6 usec. The free running oscillator, Z54, runs at a frequency of 91 KHz and causes a refresh cycle to occur approximately every 11 usec. When REFCK (Z54-3) goes to a logic 1, it signals Z42 that a refresh operation needs to occur. Z42 responds by making RREQ (Z42-20) a logic 0. This signal is inverted by Z59B and enables Z55C. Z50C, Z50D and Z55B detect the trailing edge of SM1 or the leading edge of the ANDing of PDBIN and $\emptyset_2$ (depending on the header selection). If PRESET and PWAIT are inactive, then REFENA (Z55B-6) causes a refresh cycle to start. The output of Z55D is delayed 40 ns by Z50B and generates ERG (Z50B-6)(early refresh grant). This signal is clocked into Z51A 40 ns later and generates REFG (Z51A-9) (refresh grant). REFG signals Z42 to generate a refresh cycle when T1, T2, T3, etc. are generated. REFG also enables the refresh counter in Z36 to increment by one. REFG (Z51A-7) causes START (Z43D-8) to go to a logic 1 which begins the generation of T1, T2, T3, etc. as for a read cycle. However, Z42 is set for a refresh operation and causes all four RAS outputs to go to logic 0. CAS and R/WR are not generated and as a result a single row of 128 bits in all 32 RAMS is refreshed. When T6 (Z47-11) is generated, Z51A is reset, and is ready for the beginning of another refresh cycle.

Address Selection & Data Output Control

Besides the above described memory operations, there are peripheral circuits that perform other functions. One circuit is the address selection/deselection logic. If other memory (either RAM or ROM) resides in the CPU memory space, a means is needed to disable the memory board when these other memories are addressed. Z39 compares the address set on the four upper address bits of switch SW1 with the address switch settings of SW2. Depending on how these two switches are set, memory may be addressed as (16) 4K banks, (8) 8K banks, (4) 16K banks or (2) 32K banks on HEX address boundaries 0000, 1000, 2000, . . F000. If SW1A is set to a one (up position), then memory may be selected in these bank combinations. If SW1A is set to a zero (lower position) then memory may be deselected in these bank combinations. When the memory is selected, SEL (Z44B-6) is a logic 1. This allows the RDENB signal to enable the tri-state driver of Z35, putting data out to the CPU at the correct time for its read operation.

The CPU timing events which will disable the memory board from outputting data are SINTA, PRESET, PHANTOM, SOUT, and SINP. These signals are ORed by Z53A, Z44B, and other associated gates to cause SEL to be a logic 0, thus disabling the output tri-state driver.

Another function of the peripheral logic is to allow refresh operations to continue during a CPU PRESET or CPU controlled floppy disc data transfer. Whenever PRESET (for a reset function) or PWAIT (for a floppy disc data transfer) are active, the refresh cycles are allowed to continue independent of the other S-100 bus timing signals normally used to determine the refresh timing. PRESET AND PWAIT are ORed by Z61B and after a fixed time delay determined by shift register Z52, will enable nand gate Z55D. Whenever RREQ (Z42-20) is a logic zero, the above described refresh cycle will occur. However, Z54 completely determines when refresh will occur. The delay introduced by Z52 is necessary to allow the memory circuits to complete any memory read or write cycle that may have started just before the occurrance of PRESET or PWAIT.

Wait State Generator

A wait state generator is designed for memory board operations at clock frequencies above 4 MHz, and consists of shift register, Z48, and tri-state drive Z59A and Z59F. By selecting the appropriate header connection, PSYNC is delayed in time and drives Z59F which generates PRDY. However, PRDY will only be generated if the memory board is selected. SEL, through Z59A turns the tri-state output of Z59F on.

Control and Address Line Filters

RC input filters and buffers are used on the address and critical control lines to prevent voltage spikes and bus ringing from causing false timing signals to occur. The design of the input filters and buffers assure compatible operation on an S-100 bus that is either terminated or unterminated.

3.0 Appendices

1. Appendix A - Header connections to select for a CPU board.

2. Appendix B - PC board jumper selections.

3. Appendix C - Memory address select and deselect switch tables.

4. Schematic

5. Timing Diagrams

6. Parts List

7. Memory Board Layout

APPENDIX A
HEADER CONNECTIONS

Two headers on the memory board allow the user to customize the timing of the control logic to interface with as many 8080 and Z80 CPU boards as possible. Table 1 is a list of the control signals which are connected on headers number 1 and 2. Table 2 contains a list of header signals on the left hand side of the table which are normally wired to various possible control signals shown on the right hand side. Table 3 is a wiring list for header numbers 1 and 2 for various types of CPU boards running at either 2 or 4 MHz. The majority of the available CPU board types are listed in this table. However, in the event that you may own a CPU board that is not listed, a description of the various header selections, in conjunction with the theory of operation and timing diagrams will allow you to correctly wire the headers.

Header No. 1

1. RDEN to SMEMR or PDBIN
   The read enable signal (RDEN) is used to enable the tri-state output buffer, Z35, and in the case of the Z80, it is used to start a memory M2-M5 read cycle. For all 8080 CPU boards, PDBIN is the correct timing signal. For Z80 CPU boards either SMEMR or PDBIN is used, depending on the particular CPU design. Whichever of the two signals uses the Z80 $\overline{RD}$ output signal directly or through some combinational logic (no one shots) is the correct signal to use.

2. START1SEL to $\overline{RDENB}$ or PU-3
   The START1SEL signal is connected to $\overline{RDENB}$ for all Z80 CPU's and is used to start a memory M2-M5 read cycle. This signal is not needed for a 8080 CPU, board resulting in the START1SEL to PU-3 (pull up resistor) connection.

3. REFEN to $\overline{SM1B}$ or 8080REF
   Refresh enable (REFEN) determines when in time a refresh cycle is to be initiated. For all Z80 CPU's, $\overline{SM1B}$ is used and for all 8080's, 8080REF is used.

4. START2SEL to $\overline{SM1B}$ or PU-3
   The START2SEL signal is connected to $\overline{SM1B}$ for all Z80 CPU's and is used to start a memory M1 read cycle. This signal is not needed for an 8080 CPU, resulting in the START2SEL to PU-3 connection.

5. MBRSEL to T6, T7, T8
   MBRSEL determines when the end of a memory read cycle occurs by resetting Z51B for all CPU boards. In addition, for all Z80's operating at 4 MHz, MBRSEL must be selected such that it occurs after AMWRITEB for the correct execution of a memory write cycle.

6. T4SEL to T6, T7, T8
   T4SEL clocks, on its rising edge, the T4 input of Z42 which samples the R/$\overline{W}$ input (Z42-7). This signal is selected to occur near the middle of the pulse, AMWRITEB.

7. OBCKSEL to T8 or START
   The output buffer clock select (OBCKSEL) is used to clock valid data into output buffer, Z35, during a read cycle. For any 8080, T8 is used. For any Z80, START is used.

Header No. 2

1. PSYNCSEL to PSYNCB, D1, D2, D3, or PU-2
   The different PSYNCSEL options allows the memory timing to be adjusted for the different ways each of the CPU boards generate PSYNC. In the case of all 8080 CPU's, PSYNC needs to be delayed in time such that the starting of a memory read cycle occurs after the 8080 address lines have settled. For all Z80 CPU's operating at 2 MHz, PSYNC is not used. Z80 CPU's @ 4 MHz such as the Northstar and Vector Graphics which generate PSYNC by ORing MREQ with IORQ and then using the Q output of a D flip flop, clocked by Ø, require PSYNCSEL to connect to PSYNCB. Z80 CPU's @ 4 MHz such as CROMEMCO and Ithaca Audio, which generate PSYNC by ORing IORQ with the ANDing of MREQ and RFSH require that PSYNC be delayed in time such that the generation of the timing signals T6, T7, or T8 (used for MBRSEL and T4SEL) occur near the middle of the pulse, AMWRITEB.

2. DSRSEL to PSYNCB or $\overline{\text{PSYNCB}}$
   Delay shift register select (DSRSEL) allows either PSYNCB or $\overline{\text{PSYNCB}}$ to be the input to shift register, Z48. All 8080 CPU boards and Z80 CPU's such as Cromemco, Ithaca Audio and others that generate PSYNC by similar means, require the use of $\overline{\text{PSYNCB}}$. Z80 CPU's such as Northstar, Vector Graphics and others that generate PSYNC by similar means, require the use of PSYNCB.

3. WAITSEL to D5, D6, D7, D8, or INVOUT
   WAITSEL is used to generate a single wait state for greater than 4 MHz operation. Depending on the particular CPU board used, a different tap on shift register Z48 is required. If DSRSEL is connected to PSYNCB, INVOUT is not used. However, if DSRSEL connects to PSYNCB, then WAITSEL connects to INVOUT and INVIN connects to the appropriate delay tap on Z48. This assures the correct polarity for WAITSEL.

4. INVIN to $\overline{\text{PSYNCB}}$, D3, D4, D5, D6, or D7
   See the description for WAITSEL.

HEADER SIGNAL NAMES

PIN	HEADER NO. 1	HEADER NO. 2
1	RDENB	WAITSEL
2	START1SEL	INVOUT
3	PU-3	INVIN
4	START2SEL	PU-2
5	SM1B	PSYNCB
6	REFEN	DSRSEL
7	8080 REF	PSYNCB
8	---	D1
9	RDEN	PSYNCSEL
10	SMEMR	D2
11	PDBIN	D3
12	START	D4
13	OBCKSEL	D5
14	T8	D6
15	MBRSEL	D7
16	T7	D8
17	T4 SEL	
18	T6	

TABLE 1

HEADER SELECTIONS

Header No. 1

1.	RDEN	to	SMEMR or PDBIN
2.	START1SEL	to	RDENB or PU-3
3.	REFEN	to	SM1B or 8080 REF
4.	START2SEL	to	SM1B or PU-3
5.	MBRSEL	to	T6, T7, or T8
6.	T4SEL	to	T6, T7, or T8
7.	OBCKSEL	to	T8 or START

Header No. 2

1.	PSYNCSEL	to	PSYNCB, D1, D2, D3, or PU-2
2.	DSRSEL	to	PSYNCB or PSYNCB
3.	WAITSEL	to	D5, D6, D7, D8, or INVOUT
4.	INVIN	to	PSYNCB, D3, D4, D5, D6, or D7

TABLE 2

TABLE 3

CPU TYPE	HEADER #1		HEADER #2	
	Pin No. From-To	Function	Pin No. From-To	Function
8080 @ 2 MHz	2-3	(START1SEL=PU)	1-2	(WAITSEL=INVOUT)
	4-3	(START2SEL=PU)	3-15	(INVIN=D7)
	9-11	(RDENSEL=PDBIN)	6-7	(DSRSEL=PSYNCB)
	15-14	(MBRSEL=T8)	9-11	(PSYNCSEL=D3)
	13-14	(OBCKSEL=T8)		
	6-7	(REFSEL=8080REF)		
	17-14	(3480T4=T8)		
NORTH STAR VECTOR GRAPHIC TDL @ 2 MHz	4-5	(START2SEL=$\overline{\text{SM1B}}$)	1-16	(WAITSEL=D8)
	9-10	(RDENSEL=SMEMR)	6-5	(DRSEL=PSYNCB)
	15-16	(MBRSEL=T7)	9-4	(PSYNCSEL=PUL)
	6-5	(REFSEL=SM1B)		
	13-12	(OBCKSEL=START)		
	2-1	(START1SEL=$\overline{\text{RDENB}}$)		
	17-16	(3480T4=T7)		
NORTH STAR TDL @ 4 MHz	4-5	(START2SEL=$\overline{\text{SM1B}}$)	1-13	(WAITSEL=D5)
	9-10	(RDENSEL=SMEMR)	6-5	(DRSEL=PSYNCB)
	15-16	(MBRSEL=T7)	9-5	(PSYNCSEL=PSYNCB)
	6-5	(REFSEL=SM1B)		
	13-12	(OBCKSEL=START)		
	2-1	(START1SEL=$\overline{\text{RDENB}}$)		
	17-16	(3480T4=T7)		
CROMEMCO @ 2 MHz	4-5	(START2SEL=$\overline{\text{SM1B}}$)	1-2	(DWAIT=INVOUT)
	9-10	(RDENSEL=SMEMR)	3-15	(INVIN=D7)
	15-16	(MBRSEL=T7)	6-7	(DRSEL=$\overline{\text{PSYNCB}}$)
	6-5	(REFSEL=SM1B)	9-4	(PSYNCSEL=PUL)
	13-12	(OBCKSEL=START)		
	2-1	(START1SEL=$\overline{\text{RDENB}}$)		
	17-16	(3480T4=T7)		

TABLE 3 (Cont'd)

CPU TYPE	HEADER #1		HEADER #2	
	Pin No. From-To	Function	Pin No. From-To	Function
CROMEMCO @ 4 MHz	4-5	(START2SEL=$\overline{\text{SM1B}}$)	1-2	(WAITSEL=INVOUT)
	9-10	(RDENSEL=SMEMR)	3-11	(INVIN=$\overline{\text{D3}}$)
	15-16	(MBRSEL=$\overline{\text{T7}}$)	6-7	(DRSEL=PSYNCB)
	6-5	(REFSEL=SM1B)	9-8	(PSYNCSEL=D1)
	13-12	(OBCKSEL=$\overline{\text{START}}$)		
	2-1	(START1SEL=$\overline{\text{RDENB}}$)		
	17-16	(3480T4=T7)		
ITHACA AUDIO @ 2 MHz	4-5	(START2SEL=$\overline{\text{SM1B}}$)	1-2	(WAITSEL=INVOUT)
	9-11	(RDENSEL=PDBIN)	3-15	(INVIN=$\overline{\text{D7}}$)
	15-16	(MBRSEL=$\overline{\text{T7}}$)	6-7	(DRSEL=PSYNCB)
	6-5	(REFSEL=SM1B)	9-4	(PSYNCSEL=PUL)
	13-12	(OBCKSEL=$\overline{\text{START}}$)		
	2-1	(START1SEL=$\overline{\text{RDENB}}$)		
	17-16	(3480T4=T7)		
ITHACA AUDIO @ 4 MHz	4-5	(START2SEL=$\overline{\text{SM1B}}$)	1-2	(WAITSEL=INVOUT)
	9-11	(RDENSEL=PDBIN)	3-7	(INVIN=$\overline{\text{PSYNCB}}$)
	15-16	(MBRSEL=$\overline{\text{T7}}$)	6-7	(DRSEL=PSYNCB)
	6-5	(REFSEL=SM1B)	9-10	(PSYNCSEL=D2)
	13-12	(OBCKSEL=$\overline{\text{START}}$)		
	2-1	(START1SEL=$\overline{\text{RDENB}}$)		
	17-16	(3480T4=T7)		
VECTOR GRAPHIC @ 4 MHz	4-5	(START2SEL=$\overline{\text{SM1B}}$)	1-13	(WAITSEL=D5)
	9-10	(RDENSEL=SMEMR)	6-5	(DRSEL=PSYNCB)
	15-16	(MBRSEL=$\overline{\text{T7}}$)	9-5	(PSYNCSEL=PSYNCB)
	6-5	(REFSEL=SM1B)		
	13-12	(OBCKSEL=$\overline{\text{START}}$)		
	2-1	(START1SEL=$\overline{\text{RDENB}}$)		
	17-18	(3480T4=T6)		

APPENDIX B
PC BOARD JUMPER SELECTIONS

Jumper Selection Areas

A Pads 1, 2, 3, 4
B Pads 5, 6, 7
C Pads 8, 9, 10
D Pads 11, 12, 13
E Pads 14, 15, 16

A: Extended PWAIT Selection for Floppy Disc Interface

The memory board is delivered with the extended PWAIT circuit enabled for Z80 operation with floppy disc. For the correct 8080 floppy disc interface, it is necessary to cut the etch on the rear of the board between pads 2 and 4 and to jumper a wire between pads 1 and 4. Pad 3 is not normally used. The PWAIT signal is used to enable refresh operation during the extended wait states of a CPU controlled floppy disc data transfer.

B: WAIT STATE GENERATOR Enable/Disable

The memory board is delivered with the wait state generator disabled (pad 6 connected to 7). If it is necessary to enable one wait state, the etch on the rear of the PC board between pads 6 and 7 must be cut and a wire added between pads 5 and 7.

C: Full 64K Address Select

When working with floppy disc operating systems, it may become necessary to select all 64K of memory. To do this the etch between pads 9 and 10 must be cut and a wire added between pads 8 and 10. The board is pre-wired to use the select/deselect switches.

D: SINTA Enable/Disable

The memory board is delivered with SINTA enabled (pad 11 connected to 13) and allows a CPU generated SINTA signal to deselect the memory board. This is accomplished by causing the output data buffer to go to the tri-state condition. To prevent the SINTA signal from deselecting the memory board, the etch on the rear of the PC board between pads 11 and 13 must be cut and a wire added between pads 12 and 13.

APPENDIX C (Cont'd)

4K BANK DESELECTION		DESELECTION CODE	
Starting Address	Ending Address	SW-1 ABCD	SW-2 ABCD
0000H	0FFFH	0111	0000
1000H	1FFFH	0111	0001
2000H	2FFFH	0111	0010
3000H	3FFFH	0111	0011
4000H	4FFFH	0111	0100
5000H	5FFFH	0111	0101
6000H	6FFFH	0111	0110
7000H	7FFFH	0111	0111
8000H	8FFFH	0111	1000
9000H	9FFFH	0111	1001
A000H	AFFFH	0111	1010
B000H	BFFFH	0111	1011
C000H	CFFFH	0111	1100
D000H	DFFFH	0111	1101
E000H	EFFFH	0111	1110
F000H	FFFFH	0111	1111

8K BANK DESELECTION		DESELECTION CODE	
0000H	1FFFH	0110	0000
2000H	3FFFH	0110	0010
4000H	5FFFH	0110	0100
6000H	7FFFH	0110	0110
8000H	9FFFH	0110	1000
A000H	BFFFH	0110	1010
C000H	DFFFH	0110	1100
E000H	FFFFH	0110	1110

16K BANK DESELECTION		DESELECTION CODE	
0000H	3FFFH	0100	0000
4000H	7FFFH	0100	0100
8000H	BFFFH	0100	1000
C000H	FFFFH	0100	1100

32K BANK DESELECTION		DESELECTION CODE	
0000H	7FFFH	0000	0000
8000H	FFFFH	0000	1000

APPENDIX C
ADDRESS SWITCH SELECTIONS FOR MEMORY SELECT AND DESELECT

4K BANK SELECTION		SELECTION CODE	
Starting Address	Ending Address	SW-1 ABCD	SW-2 ABCD
0000H	0FFFH	1111	0000
1000H	1FFFH	1111	0001
2000H	2FFFH	1111	0010
3000H	3FFFH	1111	0011
4000H	4FFFH	1111	0100
5000H	5FFFH	1111	0101
6000H	6FFFH	1111	0110
7000H	7FFFH	1111	0111
8000H	8FFFH	1111	1000
9000H	9FFFH	1111	1001
A000H	AFFFH	1111	1010
B000H	BFFFH	1111	1011
C000H	CFFFH	1111	1100
D000H	DFFFH	1111	1101
E000H	EFFFH	1111	1110
F000H	FFFFH	1111	1111

8K BANK SELECTION		SELECTION CODE	
0000H	1FFFH	1110	0000
2000H	3FFFH	1110	0010
4000H	5FFFH	1110	0100
6000H	7FFFH	1110	0110
8000H	9FFFH	1110	1000
A000H	BFFFH	1110	1010
C000H	DFFFH	1110	1100
E000H	FFFFH	1110	1110

16K BANK SELECTION		SELECTION CODE	
0000H	3FFFH	1100	0000
4000H	7FFFH	1100	0100
8000H	BFFFH	1100	1000
C000H	FFFFH	1100	1100

32K BANK SELECTION		SELECTION CODE	
0000H	7FFFH	1000	0000
8000H	FFFFH	1000	1000

E: $\overline{\text{PHANTOM}}$ Enable/Disable

The PC board is delivered with the $\overline{\text{PHANTOM}}$ line enabled causing the memory board to be deselected whenever the $\overline{\text{PHANTOM}}$ line is low. To disable this feature, cut the etch on the rear of the PC board between pads 15 and 16 and add a wire between pads 14 and 16.

PARTS LIST REVISION D

S-100 Dynamic Ram
Models: 6400, 4800, 3200, 1600

ITEM	DESCRIPTION	QTY	REMARKS
1	74S00N IC, Quad 2 input nand gate	2	
2	74S04N IC, Hex inverter	1	
3	74S08N IC, Quad 2 input and gate	1	
4	74S11N IC, Triple 3 input and gate	1	
5	74LS13N IC, Dual 4 input nand gate	1	
6	74LS14N IC, Hex schmitt-trigger inverter	2	
7	74LS132 IC, Quad 2 input nand gate	1	
8	7485N IC, 4 Bit comparator	1	
9	74S112N IC, Dual J-K FF	1	
10	74164N IC, 8 Bit serial shift register	3	
11	74S175N IC, Quad D-FF	2	
12	74LS244N IC, Octal line driver/rcvr	1	
13	M5K4116P-3 16k x 1 Dynamic ram	*	* Qty 32 for 6400; Qty 24 for 4800; Qty 16 for 3200; Qty 8 for 1600
14	74LS373N IC, Octal transparent latch	1	
15	74368N IC, hex bus driver	1	
16	MC3480L IC, Memory controller	1	Motorola
17	MC3242AP (P3242) IC, Memory addr. mux	1	Mototola (Intel)

Measurement Systems & Controls Inc.
867 North Main Street
Orange, CA 92668
Tel: (714) 633-4460

PARTS LIST REVISION D

S-100 Dynamic Ram
Models: 6400, 4800, 3200, 1600

ITEM	DESCRIPTION	QTY	REMARKS
18	LM555CN IC, Timer	1	
19	LM340T-12 (LM7812CT) +12V Regulator	1	
20	LM340T-5.0 (LM7805CT) +5V Regulator	1	
21	LM79L05ACZ (LM320LZ 5.0) -5V Regulator	1	
22	1N4001 Diode	1	
23	CM2105-25MHz ±.05% Crystal oscillator	1	Crystek
24	HS371-220 Heatsink	2	Ahamtor
25	308AG40D 8 Pin socket, Augat	1	
26	314AG40D 14 Pin socket, Augat	10	
27	316AG40D 16 Pin socket, Augat	*	* Qty 37 for 6400; Qty 29 for 4800; Qty 21 for 3200; Qty 13 for 1600
28	318AG40D 18 Pin socket, Augat	1	
29	ICN 203 SG 20 Pin socket, Robinson Nugent	2	
30	324AG40D 24 Pin socket, Augat	1	
31	328AG40D 28 Pin socket, Augat	1	
32	616-CGI 16 Pin header	1	
33	618-CGI 18 Pin header	1	
34	0.1 uF 50V Disc ceramic capacitor	84	

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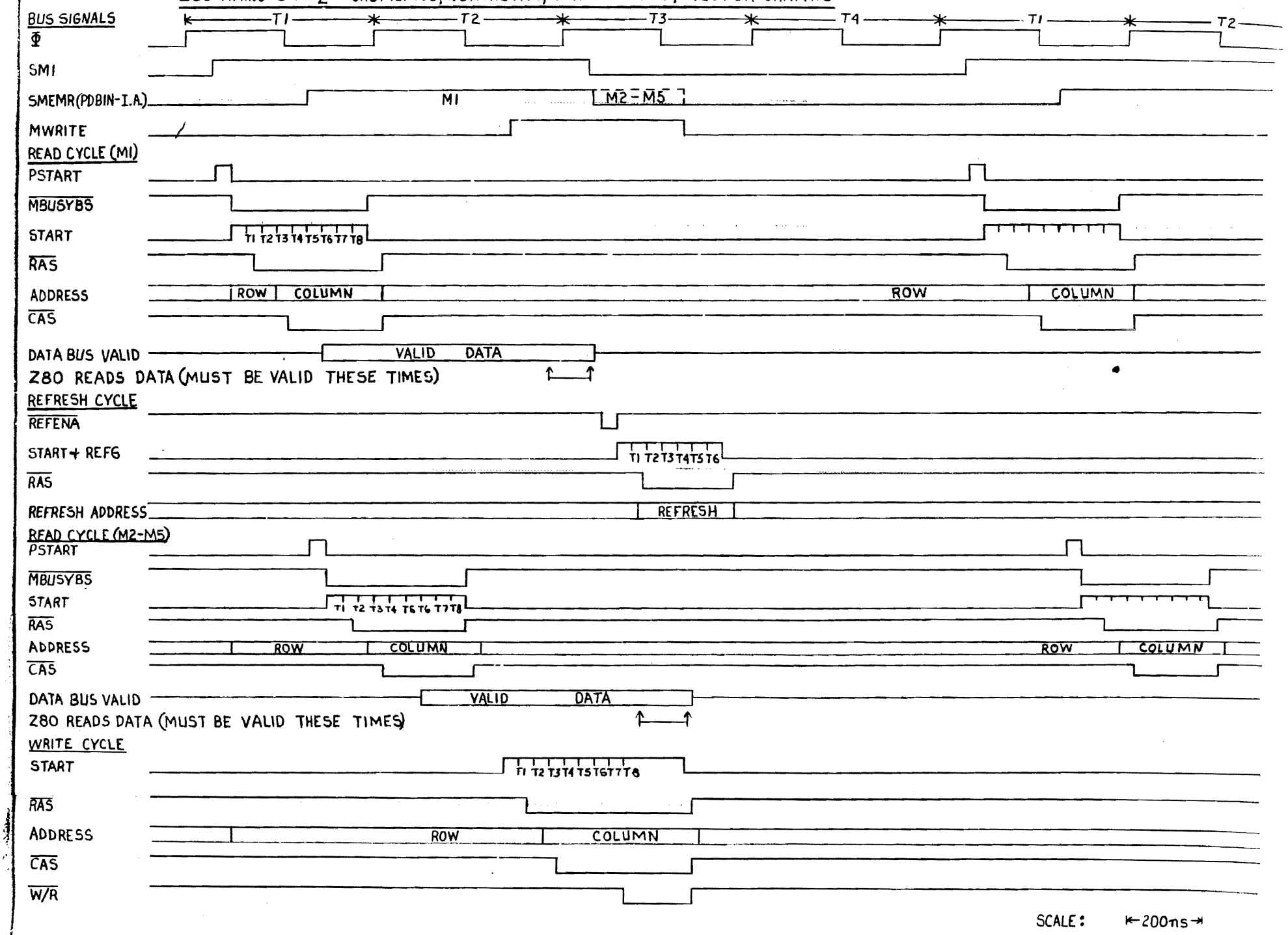
PARTS LIST REVISION D

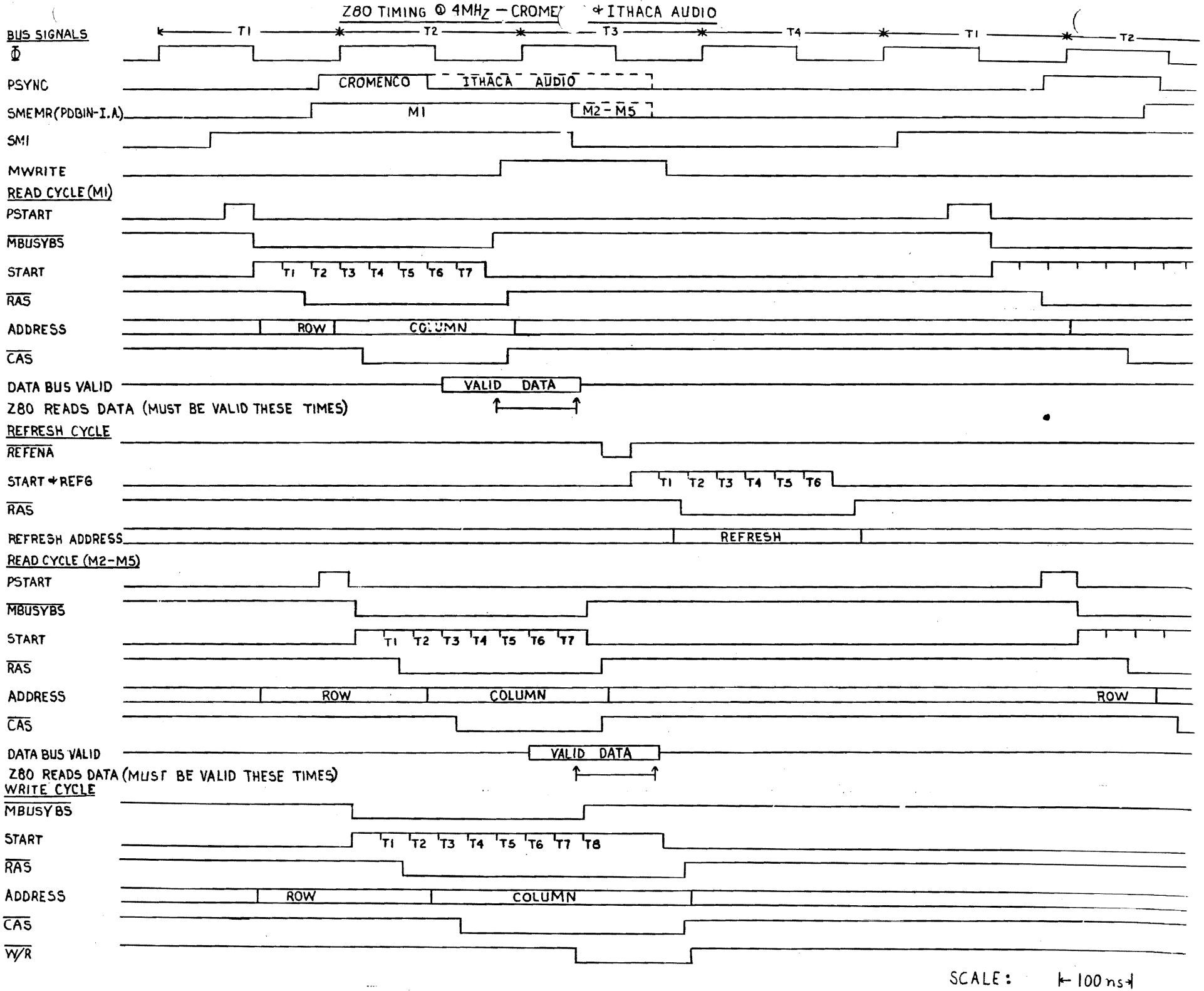
S-100 Dynamic Ram
Models: 6400, 4800, 3200, 1600

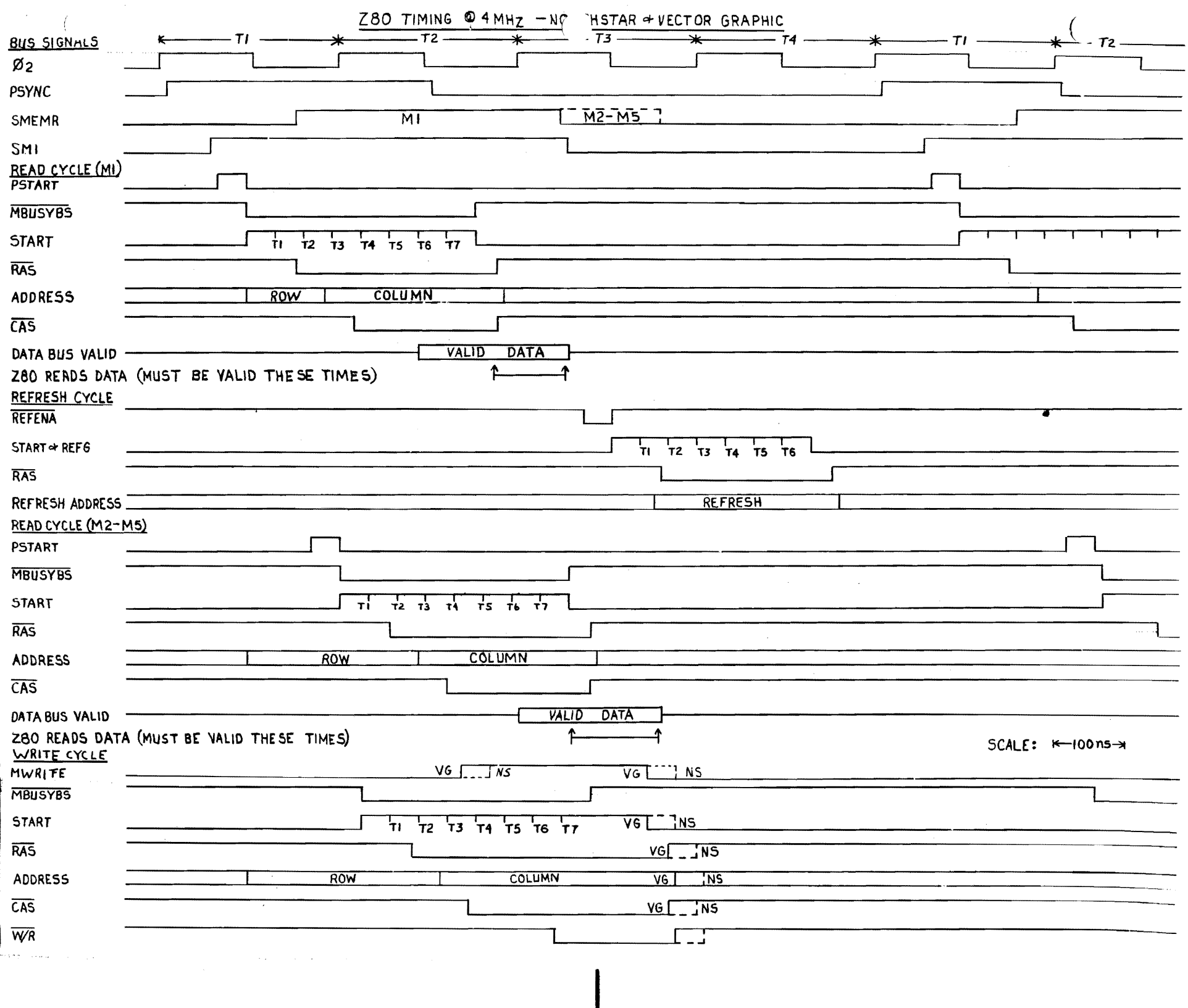
ITEM	DESCRIPTION	QTY	REMARKS
35	6.8 uF 35V Dipped tantalum capacitor	14	
36	47 pf CK12BX470K Ceramic capacitor	21	
37	390 pF CM05FD391J03 ±5% capacitor	1	
38	22 Ohm Resistor, 5% ¼W Carbon comp.	13	
39	68 Ohm Resistor, 5% ¼W Carbon comp.	1	
40	200 Ohm Resistor, 5% 1/8 W Carbon comp.	21	
41	1K Resistor, 5% ¼W Carbon comp.	3	
42	9.1K Resistor, 5% ¼W Carbon comp.	1	
43	10K Resistor, 5% ¼W Carbon comp.	2	
44	76C04 DIP switch 4-SPDT	2	Grayhill
45	ECI-6102-3-5-4 Bus bar	5	Eldre Components Inc.

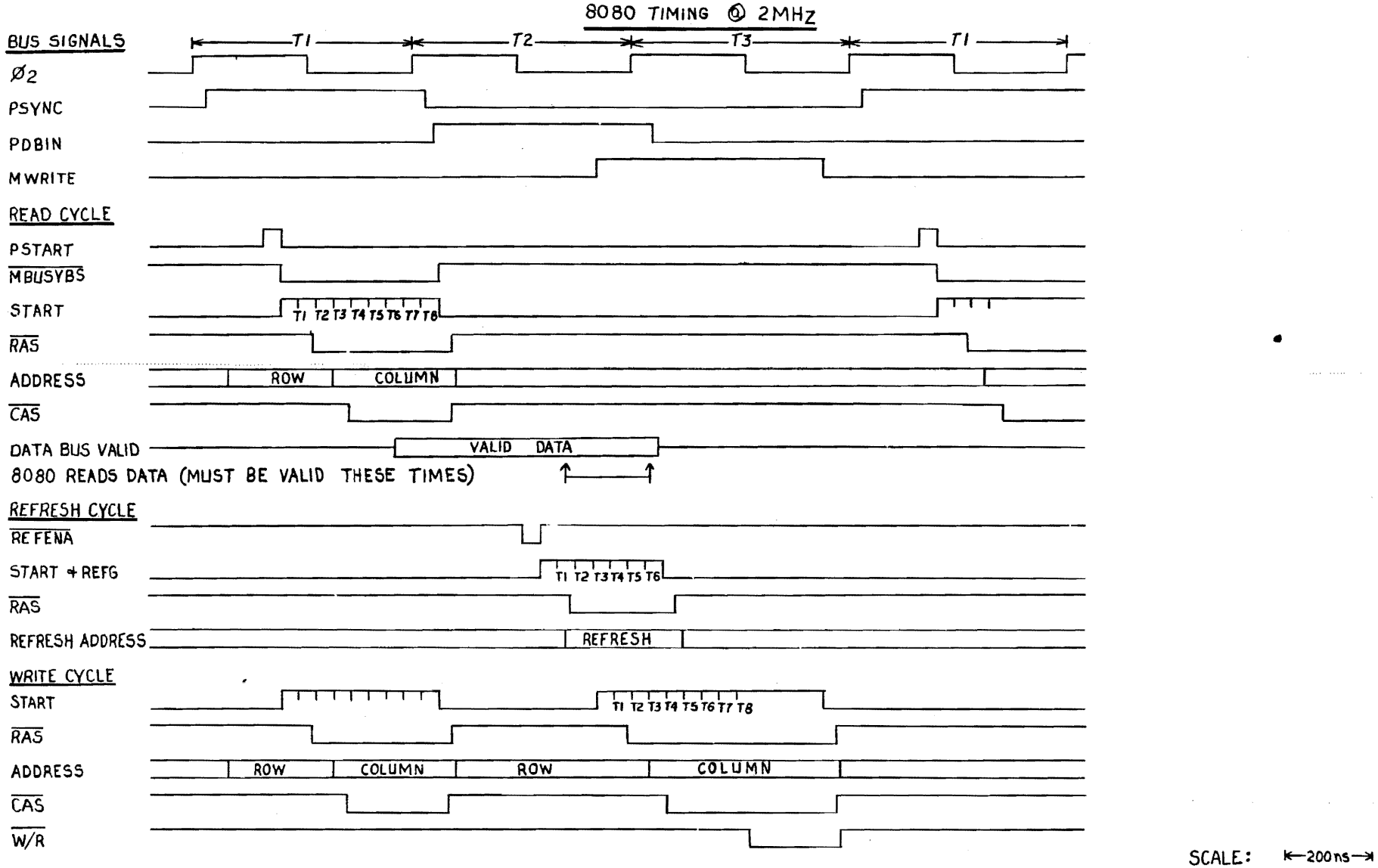
Measurement Systems & Controls Inc.
867 North Main Street
Orange, CA 92668
Tel: (714) 633-4460

Z80 TIMING @ 2MZ – CROMEMCO, NORTHSTAR, ITHACA AUDIO, VECTOR GRAPHIC




Z80 TIMING @ 4MHz — CROMEMCO & ITHACA AUDIO
BUS SIGNALS
T1
T2
T3
T4
T1
T2
Φ
PSYNC
CROMENCO
ITHACA AUDIO
SMEMR(PDBIN-I.A)
M1
M2-M5
SM1
MWRITE
READ CYCLE (M1)
PSTART
MBUSYBS
START
T1 T2 T3 T4 T5 T6 T7
RAS
ADDRESS
ROW
COLUMN
CAS
DATA BUS VALID
VALID DATA
Z80 READS DATA (MUST BE VALID THESE TIMES)
REFRESH CYCLE
REFENA
START-REFG
T1 T2 T3 T4 T5 T6
RAS
REFRESH ADDRESS
REFRESH
READ CYCLE (M2-M5)
PSTART
MBUSYBS
START
T1 T2 T3 T4 T5 T6 T7
RAS
ADDRESS
ROW
COLUMN
ROW
CAS
DATA BUS VALID
VALID DATA
Z80 READS DATA (MUST BE VALID THESE TIMES)
WRITE CYCLE
MBUSYBS
START
T1 T2 T3 T4 T5 T6 T7 T8
RAS
ADDRESS
ROW
COLUMN
CAS
W/R
SCALE: ←100ns→


Z80 TIMING @ 4 MHz — NO CHSTAR & VECTOR GRAPHIC
BUS SIGNALS
T1
T2
T3
T4
T1
T2
Ø2
PSYNC
SMEMR
M1
M2-M5
SM1
READ CYCLE (M1)
PSTART
MBUSYBS
START
T1 T2 T3 T4 T5 T6 T7
RAS
ADDRESS
ROW
COLUMN
CAS
DATA BUS VALID
VALID DATA
Z80 READS DATA (MUST BE VALID THESE TIMES)
REFRESH CYCLE
REFENA
START & REFG
T1 T2 T3 T4 T5 T6
RAS
REFRESH ADDRESS
REFRESH
READ CYCLE (M2-M5)
PSTART
MBUSYBS
START
T1 T2 T3 T4 T5 T6 T7
RAS
ADDRESS
ROW
COLUMN
CAS
DATA BUS VALID
VALID DATA
Z80 READS DATA (MUST BE VALID THESE TIMES)
SCALE: ←100ns→
WRITE CYCLE
MWRITE
VG NS
VG NS
MBUSYBS
START
T1 T2 T3 T4 T5 T6 T7
VG NS
RAS
VG NS
ADDRESS
ROW
COLUMN
VG NS
CAS
VG NS
W/R


8080 TIMING @ 2MHz
BUS SIGNALS
T1
T2
T3
T1
Ø2
PSYNC
PDBIN
MWRITE
READ CYCLE
PSTART
MBUSYBS
START
T1 T2 T3 T4 T5 T6 T7 T8
RAS
ADDRESS
ROW
COLUMN
CAS
DATA BUS VALID
VALID DATA
8080 READS DATA (MUST BE VALID THESE TIMES)
REFRESH CYCLE
REFENA
START + REFG
T1 T2 T3 T4 T5 T6
RAS
REFRESH ADDRESS
REFRESH
WRITE CYCLE
START
T1 T2 T3 T4 T5 T6 T7 T8
RAS
ADDRESS
ROW
COLUMN
ROW
COLUMN
CAS
W/R
SCALE: ←200ns→