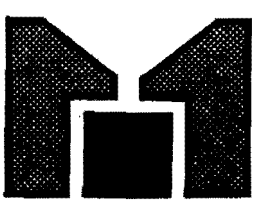
MACROTECH

MI-286

Technical Manual



MACROTECH International Corp.
9551 Irondale Ave.
Chatsworth, CA 91311

MI-286 Z80/80286 DUAL PROCESSOR

Reference Manual - Rev. 2.0

(Preliminary)

Macrotech International Corporation
9551 Irondale Avenue
Chatsworth, California 91311
(818) 700-1501

APPLICATION NOTES CONCERNING THE MI-286 DUAL PROCESSOR

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*
* T H I S A P P L I C A T I O N N O T E
*
* supersedes all earlier notes. Any items contained
* in earlier applications notes which do not appear in
* this one, may be disregarded as no longer applicable
*
****

01NOV84 - for PCBA Rev 2.0

* * * QUICKCHEK * * *

IF YOU'VE PLUGGED YOUR BOARD IN, AND SUSPECT THAT ALL IS NOT WELL, **READ THIS FIRST.**

Leave all MI-286 jumper settings as they were. As shipped from the factory, the MI-286 will run in any "Compupro-style" environment.

Ensure that Sys Support 1 - U28 pin 4 has been disabled. See item #1 (below).

Install the MI-286 board near the center of the chassis. MI-286 uses FAST TTL to drive the S-100 bus, the signal "rise-time" is much faster than your system is accustomed to. The bus terminator does its job best when the CPU board is installed about halfway between the front and back slots.

Disable "wait-states" on other boards. Other boards in the system (such as System Support 1 or Interfacer 3) should have a maximum of one (1) wait state selected. The MI-286 itself, performs a "modified I/O cycle" which runs properly with any peripherals encountered to date.

Users of RAM-16 cards must have resistor R1 currently installed as a 560-ohm resistor (green-blue-brown). Many RAM-16's were originally shipped with 4.7K-ohm resistors in this position. The value of 560-ohms was given by an engineer at the RAM-16 manufacturer.

8-16 USERS: Lately, some MP/M users have been experiencing odd failures under MP/M 8-16 using COMPUPRO **SW!.CMD** Version 3.5 and above. Specifically, multiple users may experience an 'UNINITIALIZED INTERRUPT' when one user calls up an 8-bit program. This error is NOT due to the MI-286 CPU board, although it may occur with greater frequency when the MI-286 is installed.

SW! Version 3.9, however, does not tolerate the MI-286 at all, and responds with the message 'SWITCH: CPU 8085/88 required....' (or similar wording). MACROTECH is currently evaluating the problem, but in the interim we suggest that you rename the SW!.CMD as SW!.SAV and copy another older SW!.CMD earlier than release 3.5 to you operating diskette. The acceptable versions of SW!.CMD are identifiable by their length. The SDIR command will reveal the older (acceptable) SW!.CMD files as 36 records in size, whereas the newer (3.5 and above) versions are only 29 records long. Unfortunately, the older versions do not properly support all 8-bit applications, but again, this is not due to the hardware.

These suggestions have been found to be **effective** for those customers who find that they cannot simply "drop it in and go!"

* * * END QUICKCHEK * * *

- DISCUSSION -

(1) - A previously published modification to the Compupro System Support 1 concerning operation with a Compupro 8086 CPU board must also be implemented with the MI-286. On the System Support 1:

- Remove IC at U28 (7406) from its socket.
- Bend IC leg (pin) 4 out slightly so that when re-inserting the IC into its socket, pin 4 will not make contact with its receptacle.
- Re-insert IC U28.

- Also, the MI-286 Rev 2.0 will not run with more than 1 wait-state selected ON THE SYSTEM SUPPORT 1 BOARD. Some of the System Support 1 boards currently in the field have 7 waits selected. Select 1 or 0 waits by turning OFF position 1, 2, and 3 of S1 (along right edge of Sys Sup 1)

(2) - Modified I/O timing has been provided to satisfy those LSI devices normally associated with the system I/O operations whose AC timing characteristics specify a large (500 - 700 nanosecond) interstitial rest period. This modification eliminates any requirement for "do nothing" software instructions between I/O operations and for this reason, it is recommended that the timing modification be left in place.

Users of the MI-286 who feel that the I/O devices in their systems will not require the modified I/O timing provided by the MI-286 Rev 2.0, may effectively disable the modification by moving jumper switch J24 to the right.

(3) - Math co-processor speed may be increased slightly (14-24%) by making the following modification:

- on the back of the board, cut the trace to C12 (80287) pin 32 NEAR PIN 32 (this signal must remain attached to pin 37.)

- jumper C12.32 to C14.13 (16Mhz clock)

(4) - Clarification of items contained in the PRELIMINARY MI-286 REFERENCE MANUAL.

- Page 3 - 1, item 3.

The factory default setting for J15 is "top". This means that the Memory Manager Port value is reset to all 0's whenever the system is powered-on or when system RESET is active (S-100 pin 75). This

normally occurs when the RESET button on the front panel is depressed.

- Page A1 - 3, DEFAULT JUMPER SETTINGS (illustration)

  Jumper J12 is shown set to the TOP (Power-on-jump enabled). This SHOULD BE set to the BOTTOM (Power-on-jump disabled).

  Jumper J24 is not included in the illustration. It is located near the bottom of trhe board, just below J23. This jumper is normally installed to the left in order to incorporate the MACROTECH proprietary I/O cycle modification. See item #2 for a discussion on the disabling of this jumper.

- Page 2 - 1, WAIT STATE GENERATION

  The Revision 2.0 MI-286 board supports 0 to 2 wait states on M1 (instruction fetch) cycles and 0 to 1 wait state on other memory cycles, contrary to the "0-1" claim for M1 cycles on page 2 - 1.

- Page 2 - 1, WAIT SELECTION

  Jumpers J2 and J3 are re-defined on the Revision 2.0 CPU board as follows:

J2	J3	M1 waits	Memory waits
RT	RT	0	0
RT	LT	1	0
LT	RT	1	1
LT	LT	2	1

(5) - The following problems/restrictions are necessitated by errata in the currently released version of the Intel 80286 processor. Here is an excerpt from the MIPO NEWS PRODUCT INFO letter dated January 1984, concerning the current release ("B-1", "B-2, and "B-3" steppings) of the 80286 processor:

"If the 80286 executes a POPF instruction in either Real Address Mode, or Protected Mode with CPL $\leq$ IOPL, then a pending maskable interrupt (the $\overline{\text{INTR}}$ pin active) may be improperly recognized after executing the POPF instruction even if maskable interrupts were disabled before the POPF instruction and the value popped had IF=0."

"Two additional wait states (after the read-data

is valid) added to all memory-data-read bus cycles will eliminate the errata, but will incur a performance penalty."

The remainder of item (5) concerns the effects on MI-286 operation caused by this error.

At present, the use of "byte-wide" memory in the system is restricted. 8-bit memory may only be used by:

- the Z80H processor
- the 80286 processor where NO use is made of the POPF instruction
- unrestricted provided that jumper J7B (see item #6) is installed to the left (memory-data-reads with 2 wait states) and the system memory has an access time of less than 120nS as measured on the S-100 bus from the leading edge of pSTVAL* (most any static memory).

NOTE: The MI-286 will run without ANY memory waits selected provided the following conditions are met:

- 16 bit memory is always used for the stack (any stack).
- Stack alignment is always on an even boundary (i.e. no odd addresses permitted for stack offset value).

(6) - A modification has been added to the MI-286 board in order to better handle the step 'B' error noted in item #5 above. The ability to add two wait states to all memory data reads (as opposed to memory instruction reads) has been added. This feature will normally be ENABLED as the board is shipped from the factory, by setting jumper J7B to the LEFT. It may be DISABLED by moving the shorting jumper at position J7B to the RIGHT. Refer to the discussion contained in item #5 above as to the reasons for this option.

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References.

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INTRODUCTION

The Macrotech dual cpu board (MI-286) provides a bridge from existing S-100 cpu technology to the future virtual addressing capabilities of the Intel 80286 microprocessor. Just as the advent of dual 8085/8088 boards provided the ability to use both 8 bit and 16 bit applications software, the MI-286 will continue this bridge to the protected memory mode while at the same time offering increased processing power and speed.

The MI-286 offers an upward compatible step into the future. The Z80H operating at 8Mhz and the 80286 operating at 6Mhz represent todays state of the art in both 8 and 16 bit microprocessors.

The MI-286 provides the ability to easily replace an existing dual cpu board with little or no modifications to the hardware or software presently in use. Immediate gains result from the higher throughput capabilites of the 80286 and future gains will result with the newer operating systems presently in development that will use the virtual memory capabilities of the 80286.

Mathematical calculations using floating point as well as bcd high precision arithmetic are supported by the optional 80287 coprocessor. This enhancement is upward compatibile from the 8087 in use with the earlier Intel microprocessors.

Numerous user settable jumpers on the MI-286 allow the configuration of the board for replacement purposes while the design has carefully included all the requirements for future use of the board.

The onboard I/O is jumper selectable for port assignment and provides the ability to select the active processor (Z80H or 80286), wait state selection, power on jump options and the processor reset options.

Factory delivered settings of the jumpers provides complete replacement for the Compupro 85/88 cpu board. Appendix 1 describes the details of plug replacement in this case.

The 4 memory management modes (default, virtual, Z80 primary, 286 primary) are provided to meet today's dual CPU configurations, tomorrow's virtual addressing configurations and for the systems specialist, creative dual processor configurations.

The default mode provides a present day compatibility for many of the '816' operating systems as well as the independent single processor configurations such as CP/M 2.2 and CP/M 86.

The virtual mode recognizes the current development of operating systems that exploit the 80286 protected memory capability with its well defined multitasking address spaces.

Specialty operating systems such as large database data acquisition systems, matrix manipulating systems and high performance graphics systems are not bound by the standard environment configurations that require rigid memory space assignment. The creative systems designer should carefully consider the unique ability of the Z80 primary or 80286 primary modes. The ability of the primary processor to maintain a specific memory space for its operations while at the same time manipulating the operating address space of the secondary processor, can open up the full 16 megabyte address space without the specific use of virtual addressing with its predefined implementation techniques.

ON-BOARD I/O

The MI-286 is equipped with on-board I/O to provide software control of the following features:

1. Processor swap
2. Memory management mode selection
3. Memory manager address selection
4. Configuration jumpers

In order to assure full dual processor swap/memory manager compatibility while avoiding conflict with the fixed port assignments required by the 80287 numeric co-processor, the two on-board I/O addresses are organized as two sequential odd-numbered ports, typically set to FD and FF (hex). The 80287 is accessed through even numbered ports F8, FA, FC.

PORT SELECTION

Eight bit (256 port) I/O addressing is used for the MI-286 on-board I/O. The six most significant bits, A7 - A2 are set to define the I/O base address. This scheme permits setting the I/O base on any 4-byte boundary, although only the two odd addresses in sequence are used by the MI-286. The two even addresses in the assigned sequence are free to be used by the other devices in the system if the optional 80287 numeric co-processor is not installed, or if the I/O base address is set to a non-standard value that will not conflict with the 80287 I/O address space (F8 thru FC).

PORT DEFINITIONS

When the six-bit value of the I/O base address is defined, the following relationships apply:

ADDRESS	I/O READ	I/O WRITE
IOBASE + 0	Not used	Not used
IOBASE + 1	Processor swap	Load memory manager port
IOBASE + 2	Not used	Not used
IOBASE + 3	Configuration jumper status	Set memory manager mode

The example below is for IOBASE set to 1111 11XX (FC hex).

ADDRESS	I/O READ	I/O WRITE
FC	Not used	Not used
FD	Processor swap	memory manager address port
FE	Not used	Not used
FF	Configuration jumper status	Set memory manager operating mode

PROCESSOR SWAP

At power-up or reset the Z80 processor will be in control of the bus. When control is to be passed to the 80286, an I/O Read from IOBASE + 1 is executed. When the 80286 wishes to relinquish control back to the Z80, it will execute an input instruction for port IOBASE + 1. All subsequent inputs from IOBASE + 1 will result in passing control from the currently active processor to the inactive one.

MEMORY MANAGER PORT

Either processor can set the memory management latch value by executing a byte output to the memory manager port (IOBASE + 1). The value written to this port will represent the upper 4 or 8 bits of one or both processors, depending on the memory management mode in effect at the time. The memory manager latch is initialized to zero at power-up and optionally each time a reset occurs.

CONFIGURATION JUMPERS

Two Berg jumpers have been provided on the MI-286 that can be read by either processor through I/O port IOBASE + 3. The status of SW1 and SW0 appears on data bits D1 and D0 when this port is read. This feature is included as a convenience to the systems programmer for whatever use he may choose and has no dedicated purpose.

MEMORY MANAGEMENT MODE CONTROL

The MI-286 supports four operational modes for control of the upper address lines to provide the system programmer with optimal memory management flexibility. The memory management mode can be invoked by either processor at any time by issuing a byte output with a value of 0 to 3 to IOBASE + 3. The dual cpu compatible default mode is invoked at power-up or reset, and remains in effect until IOBASE + 3 is written with a new value. The four memory management addressing modes are defined as follows:

MODE 0 - Default mode

MODE 1 - Virtual mode

MODE 2 - 286 primary mode

MODE 3 - Z80 primary mode

MODE	PROCESSOR	A23-20	A19-16	A15-A0
0	Z80	Latch	Latch	Direct
	286	Latch	Direct	Direct
1	Z80	Latch	Latch	Direct
	286	Direct	Direct	Direct
2	Z80	Zero	Latch	Direct
	286	Latch	Direct	Direct
3	Z80	Latch	Latch	Direct
	286	Zero	Direct	Direct

In the above table, the address bit values are defined as Zero, Direct or Latch. If the table entry is defined as Direct, the appropriate address bits on the bus are obtained directly from the address bus of the active processor. If the table entry is defined as Zero, the address bits on the bus are forced to zero. If the table entry is defined as Latch, the address bits on the bus follow the value that was last output to the memory management latch or to zero if the latch is still in the reset condition.

DMA ADDRESSING

For older DMA devices that generate only the lower 16 address bits, the MI-286 will generate the upper 8 bits of the DMA address from the current memory management mode and latch when the 16/24 bit DMA addressing jumper is set to 16-bit DMA. The factory default setting is for full 24-bit DMA devices with the jumper set for 24-bit DMA addressing (J16 installed up).

MWRT ENABLE

The MI-286 generates the MWRT signal for use by other boards on the bus. If MWRT is generated by any other board, the MWRT enable jumper should be set to disabled. The factory default setting is enabled (J17 installed left).

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WAIT STATE GENERATION

The MI-286 features a flexible wait generation scheme to permit each processor to operate at optimal speed without affecting the speed of the other processor. Wait states are selected separately for the Z80H and the 80286 as follows:

* 0-1 wait for Z80 M1 cycles
* 0-1 wait for Z80 memory cycles
* 0-1 wait for Z80 I/O cycles
* 0-3 waits for 286 memory cycles
* 0-3 waits for 286 I/O cycles

A single wait state is asserted in all Z80 interrupt acknowledge cycles to assure proper operation with Intel-type interrupt controllers.

The chart below outlines the jumper settings for wait state selection.

Z80 WAIT SELECTION

JUMPER	POSITION	OPERATION
J1	Left	I/O waits selected
	Right	I/O waits not selected
J2	Left	Memory waits selected
	Right	Memory waits not selected
J3	Left	M1 waits selected
	Right	M1 waits not selected

286 WAIT SELECTION

J4 POSITION	J5 POSITION	NUMBER OF WAIT STATES
Right	Right	0 I/O waits
Left	Right	1 I/O wait
Right	Left	2 I/O waits
Left	Left	3 I/O waits

J6 POSITION	J7 POSITION	NUMBER OF WAIT STATES
Right	Right	0 Memory waits
Left	Right	1 Memory wait
Right	Left	2 Memory waits
Left	Left	3 Memory waits

RESET OPTIONS

A number of reset options are provided on the MI-286 to support a wide range of system requirements. The target application will dictate the parameterization of these options when used in a configuration other than the default setting as supplied by the factory. The reset options are defined as follows:

1. SYSTEM CLEAR OPTION

System Clear is the master reset signal for all processors and all devices requiring initialization on the MI-286. System Clear is always invoked in the power-up interval but optional to the user for system reset. This option is available for use in turnkey type applications where operator access to system reset may not be desired once the system is in operation after power-up. When J9 is set to the bottom position, System Clear will be asserted each time the reset pin (pin 75) is activated. Note that deselecting reset for System Clear operation does not assure that other reset options are automatically disabled. Each reset option must be independently set for proper operation. The factory default setting for System Clear is J9 to the bottom position (reset enabled).

2. POWER-ON-JUMP OPTION

The MI-286 provides the capability of jumping to any 256 byte boundary at power-up or optionally on reset. If reset is to invoke the Power-On-Jump feature, set jumper J12 to the top position. To disable this option, set J12 to the bottom. Note that this feature can only be active if the System Clear reset option is enabled (J9 set to bottom position). Otherwise, the setting of J12 will have no effect when reset is asserted. The factory default setting for the Power-On-Jump reset option is enabled (J12 to the top).

3. CLEAR MEMORY MANAGER PORT OPTION

This option is not dependent on the System Clear option setting. If it is desired to clear the Memory Manager Port (set to all zeroes) each time a system reset is activated, set jumper J15 to the top. Otherwise, the factory default setting is enabled (J15 to the bottom).

4. RESET Z80-ON-SWAP OPTION

Some applications may require a known starting address each time the Z80 acquires control of the bus. The Reset Z80-On-Swap option together with the Power-On-Jump option will allow the Z80 to start executing code on any 256 byte boundary in the full 16 megabyte address space when the Z80 primary address mode is in operation and Clear Memory Manager Port option is disabled. If it is desired to reset the Z80 each time it relenquishes control, set jumper J8 to the bottom position. This option is disabled (J8 to the top) in the default configuration.

5. RESET 286-ON-SWAP OPTION

This option is the counterpart to the Z80 Reset-On-Swap option with the exception that the Power-On-Jump option cannot be used in conjunction with it (the Power-On-Jump feature is dedicated for use with the Z80 processor only). This feature can be implemented to start 286 program execution near the top of any megabyte boundary in the 16 megabyte address space at XFFFF0H when the 286 primary address mode is in operation and the Clear Memory Manager Port on reset option is disabled. If this option is desired, set jumper J13 to the top. The default configuration is disabled (J13 to the bottom).

MI-286 JUMPER SUMMARY

1. Z80 WAIT SELECTION

JUMPER	POSITION	OPERATION
J1	Left	I/O waits selected
	Right	I/O waits not selected
J2	Left	Memory waits selected
	Right	Memory waits not selected
J3	Left	M1 waits selected
	Right	M1 waits not selected

2. 286 WAIT SELECTION

J4 POSITION	J5 POSITIONS	NUMBER OF WAIT STATES
Right	Right	0 I/O waits
Left	Right	1 I/O wait
Right	Left	2 I/O waits
Left	Left	3 I/O waits

3.

J6 POSITION	J7 POSITION	NUMBER OF WAIT STATES
Right	Right	0 Memory waits
Left	Right	1 Memory wait
Right	Left	2 Memory waits
Left	Left	3 Memory waits

4. RESET OPTIONS: J8 & J9

Jumper	Description	Installed Up	Installed down
J8	Reset Z80 on swap	Disabled	Enabled
J9	System clear with reset	Disabled	Enabled

5. CONFIGURATION SWITCHES

Jumper	Description	Installed Up	Installed Down
J10	SW1 Status	DI1 = 0	DI1 = 1
J11	SW0 Status	DI1 = 0	DI0 = 1

6. RESET OPTIONS

Jumper	Descriptions	Installed Up	Installed Down
J12	Power-on-Jump	Enabled	Disabled
J13	Reset 286 on swap	Enabled	Disabled
J14	Jump-on-Reset	Enabled	Disabled
J15	Clear memory manager port on reset	Enabled	Disabled

7. 16/24 BIT DMA ADDRESSING

Jumper	Description	Installed Up	Installed Down
J16	16/24 Bit DMA	24-bit DMA	16-bit DMA

8. MWRT ENABLE

Jumper	Description	Installed Left	Installed Right
J17	MWRT	Enabled	Disabled

9. I/O BASE ADDRESS SELECTION : J18-J23

Jumper	Description	Installed Left	Installed Right
J18	I/O base addr-bit6	A6 = 0	A6 = 1
J19	I/O base addr-bit7	A7 = 0	A7 = 1
J20	I/O base addr-bit5	A5 = 0	A5 = 1
J21	I/O base addr-bit3	A3 = 0	A3 = 1
J22	I/O base addr-bit4	A4 = 0	A4 = 1
J23	I/O base addr-bit2	A2 = 0	A2 = 1

10. SPARE JUMPER

Jumper Description

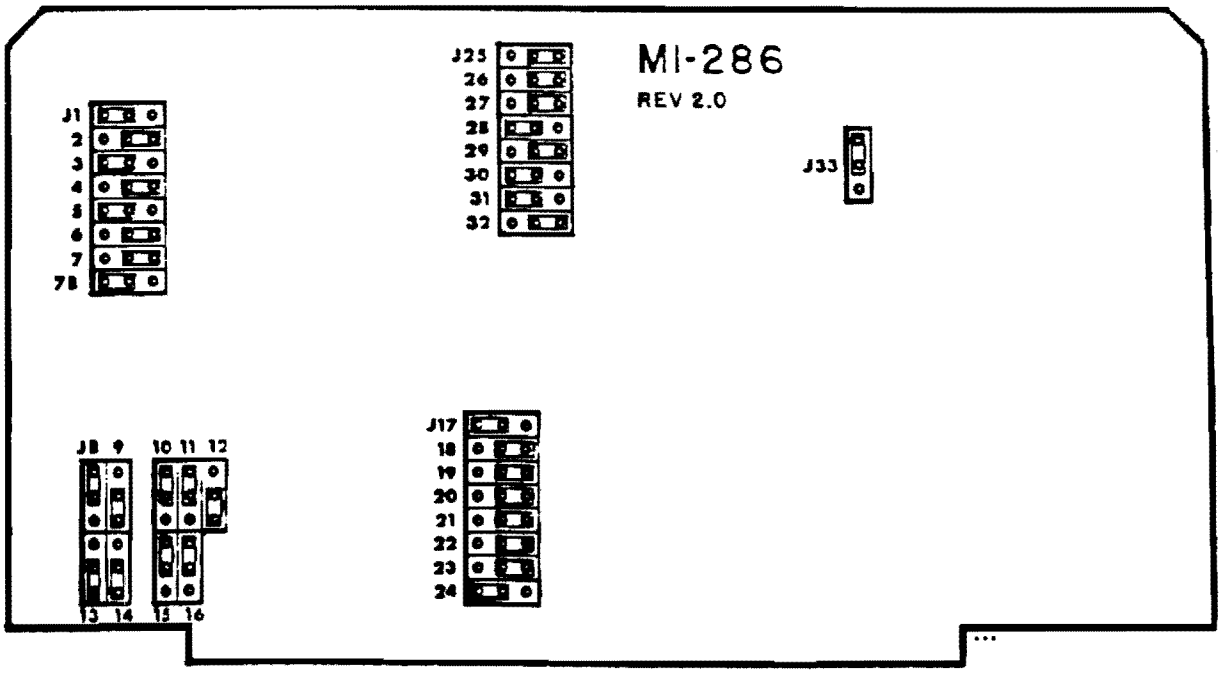
J24 Modified I/O cycle (Must be installed left in all Compu-Pro enviroments).

11.POWER-ON-JUMP ADDRESS SELECTION: J25-J32

Jumper	Description	Installed Left	Installed Right
J25	POJ addr-bit15	S15 = 0	S15 = 1
J26	POJ addr-bit14	S14 = 0	S14 = 1
J27	POJ addr-bit13	S13 = 0	S13 = 1
J28	POJ addr-bit12	S12 = 0	S12 = 1
J29	POJ addr-bit11	S11 = 0	S11 = 1
J30	POJ addr-bit10	S10 = 0	S10 = 1
J31	POJ addr-bit9	S9 = 0	S9 = 1
J32	POJ addr-bit8	S8 = 0	S8 = 1

12.Z80 FREQUENCY SELECTION

Jumper	Description	Installed Up	Installed Down
J33	Z80 Clock Frequency	8 MHZ	2 MHZ



DEFAULT JUMPER SETTINGS

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MI-286 BASIC ASSEMBLY

BILL OF MATERIALS

ITEM NO.	QTY.	MACROTECH P/N	DESCRIPTION
1	1	200202	PAL, 16L8A
2	1	200203	PAL, 16R4A
3	2	200204	PAL, 16R8A
4	2	200205	PAL, 20L10CN
5	4	100100	F74F00, QUAD 2-INPUT **NAND** GATE
6	3	100115	F74F02, QUAD 2-INPUT **NOR** GATE
7	5	100101	F74F04, HEX INVERTER
8	5	100102	F74F08, QUAD 2-INPUT **AND** GATE
9	2	100116	F74F10, TRIPLE 3-INPUT **NAND** GATE
10	3	100104	F74F32, QUAD 2-INPUT **OR** GATE
11	12	100106	F74F74, DUAL D-TYPE FLIP-FLOP
12	1	100107	F74F138, DECODER/DEMULTIPLEXER
13	3	100109	F74F157, DATA SELECTOR/MULTIPLEXER
14	1	100111	F74F244, OCTAL BUFFER (3-STATE)
15	2	100117	F74F245, OCTAL TRANSCEIVER (3-STATE)
16	1	100112	F74F257, DATA SELECTOR/MULTIPLEXER
17	4	100114	F74F373, LATCH/FLIP-FLOP
18	1	100323	F74LS04
19	1	100301	F74LS74
20	3	100305	F74LS125
21	1	100321	F74LS175
22	1	100318	F74LS221
23	1	100322	F74LS273
24	1	200403	CRYSTAL, 16.0 MHZ
25	1	200401	CRYSTAL, 12.0 MHZ, HC 18
26	1	200402	CRYSTAL, 4.0 MHZ
27	1	200103	8 BIT COMPARATOR, AM25LS2521
28	2	400512	RESISTOR, 10K OHM, 1/4W
29	4	400500	RESISTOR, 1K OHM, 1/4W
30	1	400506	RESISTOR, 150 OHM, 1/4W
31	3	400508	RESISTOR, 330 OHM, 1/4W
32	4	400501	RESISTOR, 1.5K OHM, 1/4W
33	33	400304	CAPACITOR, CERAMIC, .1MF, 50V
34	2	400301	CAPACITOR, CERAMIC, .01MF, 50V
35	2	400313	CAPACITOR, CERAMIC, 330PF, 50V
36	3	400316	CAPACITOR, CERAMIC, 470PF, 50V
37	1	400317	CAPACITOR, CERAMIC, 15PF, NPO
38	1	400318	CAPACITOR, CERAMIC, 27PF, NPO
39	3	400306	CAPACITOR, 10MF
40	1	400309	CAPACITOR, 47PF

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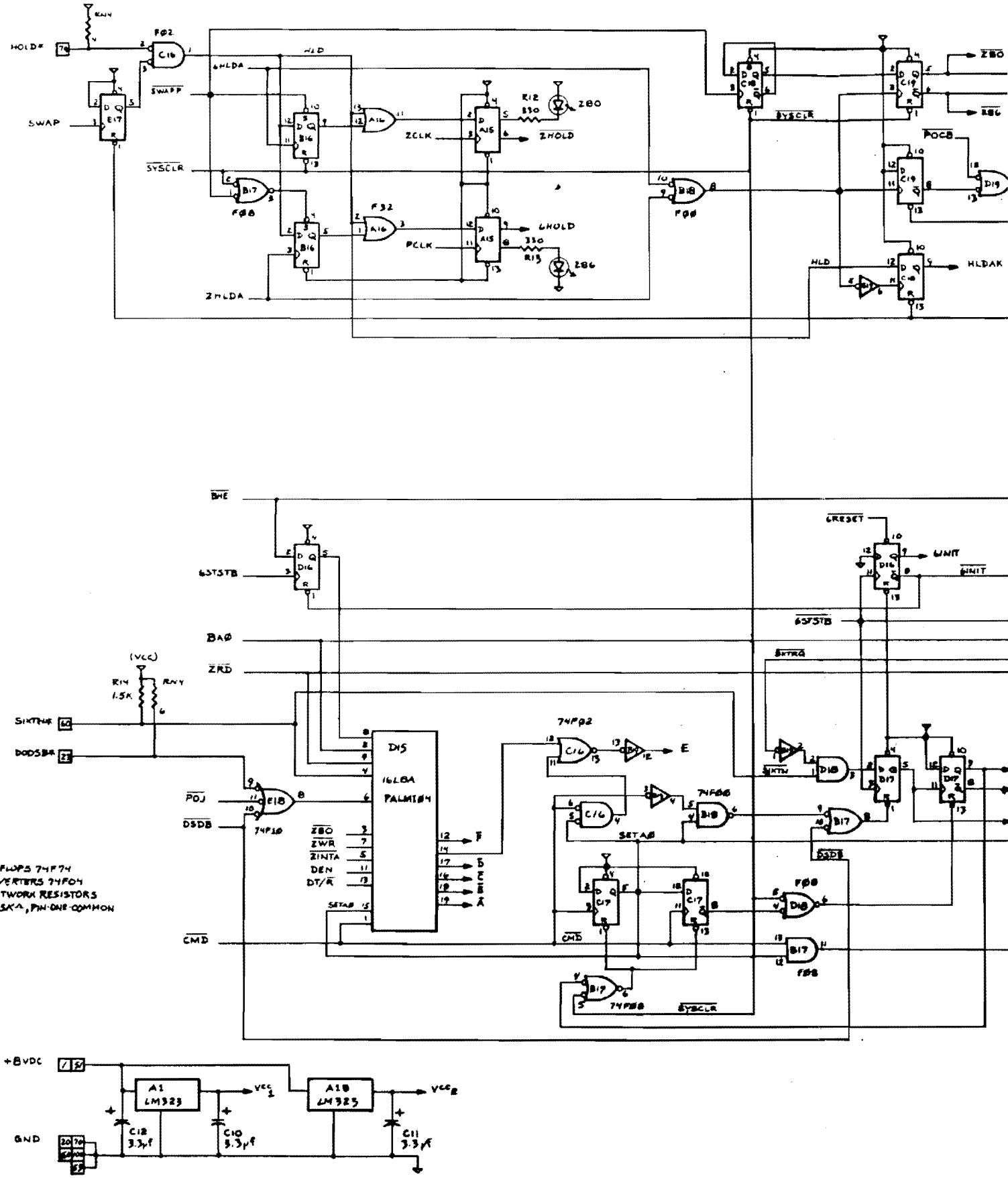
MI-286 BASIC ASSEMBLY

BILL OF MATERIALS

(continued)

ITEM NO.	QTY.	MACROTECH P/N	DESCRIPTION
41	1	200106	MICROPROCESSOR, Z80 H
42	1	400703	DIODE, 1N914
43	2	400702	LED, PC MOUNT, CQV-34-4 SQU
44	2	600304	JACK WAFER POST, 3-PIN
45	4	600307	JACK WAFER POST, 6-PIN
46	6	600308	JACK WAFER POST, 7-PIN
47	3	600309	JACK WAFER POST, 8-PIN
48	1	200310	MICROPROCESSOR, C80286-6 S40093
49	1	200311	CLOCK GENERATOR, D82284 S40095
50	1	200312	BUS CONTROLLER, D82288 S400154
51	2	200503	REGULATOR, STEEL, LM323N
52	1	500508	SOCKET, LEADLESS
53	2	600501	HEAT SINK, 423-TO-3
54	1	600502	HEAT SINK, .315
55	2	600108	EXTRACTOR
56	1	300312	PRINTED CIRCUIT BOARD w/HOLTITE SOCKETS


HOLD#
SWAP
SWAPP
SYSCLR
6HLDA
HLD
ZCLK
PCLK
ZHOLD
6HOLD
ZHLDA
R12
330
R13
330
Z80
Z86
F00
F02
F32
F08
POCB
HLDAK
BHE
63STSTB
BA0
ZRD
(VCC)
R14
1.5K
R44
SIXTNR
DODSB#
POJ
DSDB
CMD
74F10
74F02
74F86
74F08
D15
16L8A
PALM16H
ZBO
ZWR
ZINTA
DEN
DT/R
SETAB
6RESET
UNIT
6INIT
6STRQ
SIXTN
ALL D-FLIPS 74F74
ALL INVERTERS 74F04
ALL NETWORK RESISTORS
1.5K-Ω, PIN-ONE-COMMON
+8VDC
GND
A1
LM323
A18
LM323
VCC1
VCC2
C12
3.3μf
C10
3.3μf
C11
3.3μf