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1.0 GENERAL INFORMATION

1.1 Introduction

The MEGARAM has been designed to meet the need for a high performance low cost dynamic RAM for the S100 bus. With today's sixteen bit microcomputers capable of addressing up to 16 Mbytes of system memory, use of static RAM becomes prohibitive. MEGARAM addresses the need for high density, high performance and low cost.

The LSI bipolar RAM controller (TMS4500/TMS4501) removes all problems associated with earlier dynamic RAM designs. The RAM array continues to be refreshed even during extended HOLD or RESET conditions and eliminates any DMA conflicts.

The inclusion of parity allows the system to use error recovery procedures to prevent data corruption or retry the data access. The board is designed to minimize refresh overhead.

The MEGARAM utilizes the extended addressing of the IEEE-696 specification to provide address decoding up to 16 Mbytes of memory space. No bank select option is provided and the CPU must provide all 24 bits of address for the board to function properly.

An option to interleave memory boards has been designed into the board. When two or more boards are utilized using this option, there should be no wait states encountered because of refresh conflicts.

In order to take advantage of interleaved operation, two boards of the same memory size configuration are required.

2.0 PREPARATION FOR USE

2.1 Introduction

This section provides instructions for preparing the MEGARAM board for use in the particular user environment. Before installing the MEGARAM in your system, the user should be familiar with this entire manual.

2.2 Unpacking and Inspection

Carefully unpack the box that the memory was shipped in. Compare the contents of the box against the packing slip and notify LOMAS DATA PRODUCTS, INC. or your Dealer immediately if there are any discrepancies. Save the box and packing material in the event that service is required. Each board is sealed in a plastic bag which contains the board and registration card for the board. The registration card lists the configuration that the board was shipped from LOMAS DATA PRODUCTS as. Boards that were shipped in one configuration (ie 256k or 512k) are not guaranteed in any other configuration. Insure the board you received matches the configuration listed on the registration card. If there is a discrepency contact LOMAS DATA PRODUCTS or your dealer.

If it becomes necessary to return the board for any reason, it should be shipped post paid, insured. Call first for a Return Authorization number (RA). If the package you receive is damaged when received, open it in the presence of the carrier or notify him immediately of the damage. All shipments are insured for the purchased value. LOMAS DATA PRODUCTS, INC. should also be notified to begin processing the claim.

2.3 Installation Considerations

The RAM is designed to be IEEE 696 (S-100) Bus compatible. Be aware that Pins 20, 53 and 70 in addition to Pins 50 and 100 are ground connections. If there is a conflict with any older board in your system, this conflict must be resolved.

2.4 Power Requirements

The MEGARAM has the following power requirements:

256K MEGARAM	1.5 amps at 8 volts
512K MEGARAM	2.0 amps at 8 volts
1 Mbyte MEGARAM	2.0 amps at 8 volts
2 Mbyte MEGARAM	2.75 amps at 8 volts

2.5 Cooling Requirements

The MEGARAM dissipates a maximum of 30 Watts in its maximum configuration with

maximum bus voltages. When used in an enclosure that restricts normal air flow around the board, sufficient cooling must be provided to prevent the temperature inside the enclosure from exceeding 50 C.

2.6 Jumper Assignments

When received your board is setup for use in an LDP (8088/80286) system as the first board in the system. Address selection of the board is accomplished with a shunt on JP12. There are a total of 6 shunts that may be installed for address selection. The following is the correspondence of address to jumper:

JP12 1-2	A23
JP12 3-4	A22
JP12 5-6	A21
JP12 7-8	A20
JP12 9-10	A19
JP12 11-12	A18

Table 2.6 provides the jumpering information for the first 8 of each population of MEGARAM.

TABLE 2.6
MEGARAM ADDRESS JUMPERING INFORMATION

BOARD ADDRESS RANGE	1-2	3-4	5-6	7-8	9-10	11-12
256K MEMORY BOARDS						
000000-03FFFF	X	X	X	X	X	X
040000-07FFFF	X	X	X	X	X	O
080000-0BFFFF	X	X	X	X	O	X
0C0000-0FFFFF	X	X	X	X	O	O
100000-13FFFF	X	X	X	O	X	X
140000-17FFFF	X	X	X	O	X	O
180000-18FFFF	X	X	X	O	O	O
1C0000-1FFFFF	X	X	X	O	O	O
512K MEMORY BOARDS						
000000-07FFFF	X	X	X	X	X	O
080000-0FFFFF	X	X	X	X	O	O
100000-17FFFF	X	X	X	O	X	O
180000-1FFFFF	X	X	X	O	O	O
200000-27FFFF	X	X	O	X	X	O
280000-2FFFFF	X	X	O	X	O	O
300000-37FFFF	X	X	O	O	X	O
380000-3FFFFF	X	X	O	O	O	O
1 MBYTE MEMORY BOARDS						
000000-0FFFFF	X	X	X	X	O	O
100000-1FFFFF	X	X	X	O	O	O
200000-2FFFFF	X	X	O	X	O	O
300000-3FFFFF	X	X	O	O	O	O
400000-4FFFFF	X	O	X	X	O	O
500000-5FFFFF	X	O	X	O		
O O						
600000-6FFFFF	X	O	O	X	O	O
700000-7FFFFF	X	O	O	O	O	O
2 MBYTE MEMORY BOARDS						
000000-1FFFFF	X	X	X	O	O	O
200000-3FFFFF	X	X	O	O	O	O
400000-5FFFFF	X	O	X	O	O	O
600000-7FFFFF	X	O	O	O	O	O
800000-9FFFFF	O	X	X	O	O	O
A00000-BFFFFF	O	X	O	O	O	O
C00000-DFFFFF	O	O	X	O	O	O
E00000-FFFFFF	O	O	O	O	O	O

X = SHUNT INSTALLED O = SHUNT REMOVED

2.6.1 OTHER JUMPERS

JP1

JP1	1-2	4501 CONTROLLER WITH 256K DRAMS
JP1	2-3	4500/4501 WITH 64K DRAMS

JP2

JP2	1-2	4501 CONTROLLER WITH 256K DRAMS
JP2	2-3	4501 CONTROLLER WITH 64K DRAMS

JP3

The normal position for JP3 is pin 2 to pin 3. If you are getting occasional memory errors, they may be corrected in many cases by inverting the phase of the bus clock to the controller chip. The phase is inverted by changing the shunt to positions 1 and 2 for the jumper.

JP4

JP4	1-2	For all boards except LIGHTNING 286
JP4	2-3	For LIGHTNING 286

JP5

JP5 pin 1 to 2 always in. Used only for testing.

JP6

JP6 pin 1 to 2 always in. Used only for testing.

JP7, JP8, JP9

Jumpers 7, 8 and 9 are used to adjust the refresh rate to the CPU clock rate. If your processor has a 4 Mhz or faster clock rate, the jumpers are correct as shipped.

JP7	2-3
JP8	1-2
JP9	1-2

For CPU BOARDS clock rates below 4MHZ

2 to 3 Mhz	JP7 2-3, JP8 2-3, JP9 1-2
3 to 4 Mhz	JP7 2-3, JP8 1-2, JP9 2-3

JP10

JP10 enables address lines to the address comparator. The positions of these shunts are dependent on board population.

JP10	1-2	3-4	5-6

256K BOARDS	X	X	X
512K BOARDS	X	X	O
1 MBYTE BOARDS	X	O	O
2 MBYTE BOARDS	O	O	O

X = SHUNT INSTALLED O = SHUNT REMOVED

JP11

PIN 1-2 FOR TMS4500
PIN 2-3 FOR TMS4501

JP12

See table 2.6

JP13

Used with interlaced operation. See appendix.

JP14

WAIT STATE GENERATOR

JP14 pin 1 must be jumpered to one of the other pins 2 thru 9. The pins correspond to the following wait states.

WAIT STATES	PIN NUMBER
0	2
1	3
2	4
3	5
4	6
5	7
6	8
7	9

Boards are shipped with no wait states. When used with the LIGHTNING 286 one memory wait state must be jumpered on the CPU board and 0 on the memory board.

JP15

Shunt for interleave option only, see appendix.

JP16

INTERRUPT JUMPERS

INTERRUPT REQUEST	PIN 1
VIO	PIN 3
VI1	PIN 4

VI2	PIN 5
VI3	PIN 6
VI4	PIN 7
VI5	PIN 8
VI6	PIN 9
VI7	PIN 10
NMI	PIN 11
ERROR	PIN 2

JP17

JP17 selects which signal is used as ALE, pSYNC or PSTVAL. For LOMAS DATA PRODUCTS boards, pSTVAL is normally used by jumpering JP17 pin 1 to pin 2. For COMPUPRO products pSYNC should be used by wire-wrapping bus pin 76 to pin 2 of JP17. In some systems pSTVAL must be qualified by PSYNC, this may be selected by shunting JP17 pin 2 to pin 3.

2.7 Parity Error Indicators

The parity error indicators will light when a parity error is encountered. If your system does not go through an initialization of memory at power up, it will be normal for the parity indicators to be lit. If your operating system does not support parity memory it will be normal for the parity lights to be lit.

3.0
PRINCIPLES OF OPERATION

3.1 Introduction

This chapter is a brief description of the operation of the RAM board. It is assumed that the reader is familiar with the operation of dynamic RAM's and with general logic.

3.2 Refresh Request Generation

The RAM board will refresh the dynamic RAM under one of two conditions, a time out of the internal timer in the 4500/1 or a refresh request on pin 43 of the 4500/1. The internal timer in the 4500/1 provides failsafe refreshing of the RAM under any circumstances. The external refresh request is provided to help synchronize the memory to the system and minimize wait states due to refresh cycles. This is accomplished by generating a refresh request whenever a bus cycle occurs without selecting memory. This will happen whenever an I/O cycle occurs or whenever another memory is accessed. One half of U76 is used to generate this request. The flip-flop is set by the falling edge of pSYNC when the memory is not selected. The flip-flop is reset by the first RAS after it is set, which indicates that a refresh cycle has been initiated.

3.3 Memory Cycle Initialization

Memory cycles are initiated by a combination of two signals, ALE and SELECT*. ALE is a jumper selectable signal. It may be either the bus signal pSYNC or a signal generated by the PAL (Programmable Array Logic). Normally pSYNC is the selected signal. SELECT* is a signal generated by a combination of an address match and the correct bus status indicating that the present bus cycle is a memory cycle. Memory write cycles are early write cycles allowing the memory data input and output pins to be connected together. When ALE goes from its high state to a low state, if SELECT* is low, a memory cycle is initiated. Because a memory cycle is not started until the falling edge of ALE and it is not known whether a refresh cycle will be required or the access will be allowed to proceed, READY is set low when the board is selected and pSTVAL is high (in some systems pSYNC is substituted for pSTVAL). If the access is allowed instead of a refresh cycle, the READY line is set high with the first rising edge of BCLK. In most systems this will prevent a memory wait state from being inserted except during memory refresh collisions.

3.4 Memory Select Generation

The memory address comparison is performed by U77. Because the MEGARAM may be populated to different sizes, JP10 provides for allowing or disallowing addresses A18 thru A20 to the comparator as is appropriate for the configuration being used. When the appropriate shunt is installed the address is enabled to the comparator and when it is removed the address comparator is pulled to a high logic level by a resistor in RN1. The other input to the

comparator is from JP12. There are six shunts on JP12 which correspond to the address lines A18 thru A23. When a shunt is installed the matching address line is expected to be low in order to match and when it is removed the address line must be high to match. The comparator input from JP12 is pulled high by a resistor in RN1 or RN2 when the shunt is removed.

3.5 Buffer Control

The data input and output buffers are controlled primarily by the logic programmed into the PAL, U81. The following table defines when each of the buffers is enabled by the type of cycle being performed.

TABLE 3.7

CYCLE TYPE	BUFFERS ENABLED
16 BIT READ	U88,U85
16 BIT WRITE	U88,85
8 BIT EVEN WRITE	U85
8 BIT ODD WRITE	U87
8 BIT EVEN READ	U86
8 BIT ODD READ	U88

3.6 Parity Generation

Parity is generated and checked by U82 for the even bytes and by U84 for the odd bytes. The DIR signal is asserted for write cycles. This signal enables the parity bit to the RAM I.C. for writing into the RAM during a write cycle. When DIR is not asserted the output of the parity RAM's is enabled into the parity generator/checker. PARITY STB* clocks the parity status into the flip-flops of U74 during read cycles when the board is selected. Parity is always checked on a 16 bit word whether an 8 or 16 bit read is taking place. This requires that the whole memory be initialized with write cycles at power up to prevent false parity error indications. A separate parity error light for even and odd bytes is provided. Once set, the parity status is latched and will not clear until the system is reset.

4.0 GUARANTEE

4.1 General Terms

The LDP RAM has been carefully designed to meet all specifications of the IEEE-696 specification for the S100 bus. If after reading the manual you are unable to configure the memory for proper operation in your system call LOMAS DATA PRODUCTS for assistance. No refunds will be given after 15 days from shipment. **IF YOU PURCHASED YOUR BOARD THROUGH A DEALER YOU MUST CONTACT THE DEALER FOR A REFUND.** To return any board for repair or refund a return authorization must be obtained first. Warranties on boards damaged in shipment are void. It is the responsibility of the customer to instigate a claim against the shipper to recover any damages. All boards are shipped insured for the amount of the purchase.

4.2 Limited Warranty Information

LOMAS DATA PRODUCTS will repair or replace, at our option, any parts found to be defective in either materials or workmanship for a period of one year from date of invoice. Defective parts must be returned to LOMAS DATA PRODUCTS for replacement.

If a defective part causes a LOMAS DATA PRODUCTS product to operate improperly during the 1 year warranty period, we will service it free(original owner only) if delivered and shipped at owner's expense to and from LOMAS DATA PRODUCTS. If improper operation is due to an error or errors on the part of the purchaser, there may be a repair charge. The purchaser will be notified of any anticipated charges.

We are not responsible for damages caused by use of solder intended for purposes other than electronic equipment construction, failure to follow printed instructions, misuse or abuse, unauthorized modifications, use of our products in applications in other than those intended by LOMAS DATA PRODUCTS, theft, fire, or accidents.

Return to the purchaser of a fully functioning unit meeting all advertised specifications in effect as of the date of purchase is considered to be complete fulfillment of all warranty obligations assumed by LOMAS DATA PRODUCTS. This warranty covers only products marketed by LOMAS DATA PRODUCTS and does not cover other equipment used in conjunction with products from LOMAS DATA PRODUCTS.

ANY USER UPGRADE OF MEMORY CONFIGURATION VOIDS THE WARANTY. BOARDS RETURNED TO LOMAS DATA PRODUCTS FOR REPAIR IN CONFIGURATIONS OTHER THAN THAT WHICH WAS SHIPPED, WILL BE CHARGED FOR REPAIR AT THE CURRENT LABOR RATE PLUS PARTS. WARRANTY REPAIR WILL NOT BE PERFORMED FOR ANY BOARD FOR WHICH WE HAVE NOT RECEIVED A REGISTRATION CARD.

Prices and specifications are subject to change without notice, owing to the volatile nature and pricing structure of the electronics industry.

APPENDIX

MEMORY INTERLEAVING

MEGARAM has been designed so that memory cycles may be interleaved between two boards when two boards of the same configuration are used in the system. This is possible for boards in 256K, 512K and 1Mbyte configurations. The jumpering for each configuration is shown below:

256K BOARDS

REMOVE SHUNTS ON JP15 AND JP10 PIN 5 AND 6
WIRE WRAP:
JP15 PIN 1 TO JP10 PIN 6
JP15 PIN 2 TO JP10 PIN 5
ALL OTHER JUMPERING STAYS THE SAME

512K BOARDS

REMOVE SHUNTS ON JP15 AND JP10 PIN 3 AND 4
WIRE WRAP:
JP15 PIN 1 TO JP10 PIN 4
JP15 PIN 2 TO JP10 PIN 5
ALL OTHER JUMPERING STAYS THE SAME

1MBYTE BOARDS

REMOVE SHUNTS ON JP15 AND JP10 PIN 1 AND 2
WIRE WRAP:
JP15 PIN 1 TO JP10 PIN 2
JP15 PIN 2 TO JP10 PIN 1
ALL OTHER JUMPERING STAYS THE SAME