JADE COMPUTER PRODUCTS

Presents

THE BIG-Z

S-100 BUS MICRO PROCESSOR BOARD

4901 WEST ROSECRANS BLVD., HAWTHORNE, CALIFORNIA, 90250

THE BIG-Z

TABLE OF CONTENTS

I. FEATURES

On board 2704/2708/2716/2532 EPROM can be addressed on any 1K, 2K, or 4K boundary.■ Power-on jump directly to on-board EPROM.■ Optional wait state for on-board EPROM.■ On-board EPROM may be used in shadow mode (access only after power-on or reset). Allows full 64K RAM memory to be used.
Automatic MEM WRITE generation if front panel is not used. Disabled if front panel is connected.■ DMA Capability■ 2 or 4 MHz operation■ Latched data output bus provides additional data hold time for reliable operation with all device types.■ Straight-through address and data paths provide improved read access times for I/O and memory devices.■ On-board USART for sychronous or asynchronous RS232 operation.
Baud rate generator provides all standard baud rates.■ USART can be assigned to any group of four I/O addresses (only two are used)■ Reverse channel capability on USART allows use with buffered peripherals or devices with "not-ready" indication.■

II. BOARD ASSEMBLY

1) Install chip sockets at U4, U5, U6, U7, U8, U10, U14, U15, U17, U18, U20, U21, U22, U25, U16, U26, U27, U28, U29, U30, U32, U35, U36, U37, U38, U39, U40, and U41.
2) Install 1.5 uf capacitor at C16.
3) Install .1 uf capacitors at C26, C1, C2, C3, C4, C5, C6, C7 C8, C9, C10, and C11.
4) Install 7805/LM340T5 Regulator at VR4.
5) Install 100 uf capacitor at C22.
6) Install 100 pf capacitor at C24.
7) Install 10 pf capacitor at C23.
8) Install 1 uh coil at L1.
9) Install 330 resistor at R5.
10) Install 1K resistor at R4.
11) Install 2.7K resistor at R2.
12) Install 4.7K resistors at R1, R7, R8, R9, and R3.
13) Install crystal at Y1 (18 MHz or 32 MHz).
14) Install capacitor at 25 (56 pf 2 MHz or 20 pf 4 MHz)
15) Install IC's and resistor modules in locations shown in parts list.
Note: L1, C25, and C26 are needed only if Y1 is an overtone type crystal.

PARTS LIST

Common Parts:

Part Numbers	Description
U6, U17, U25, U29, U35	
U36, U37, U38, U39	74367/8097/8T97 hex TS buffer
U10, U22	7400 quad 2 input NAND
U4	7410 triple 3 input NAND
U7, U41	7432 quad 2 input AND
U14	7432 quad 2 input OR
U8	7402 quad 2 input NOR
U5	74121 One Shot
U15, U18, U30	7404 hex inverter
U20	7474 dual D flip-flop
U26, U27, U40	7475 quad transparent latch
U28, U32	4.7K resistor module
R1, R7, R8, R9, R3	4.7K resistor
R2	2.7K resistor
R4	1K resistor
R5	330 resistor
L1	1 uh coil
C23	10 pf capacitor
C24	100 pf capacitor
C22	100 uf capacitor
C26, C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C16	1.5 uf capacitor
VR4	7805/LM340T5 5 volt regulator

2 MHz Parts:

Part Numbers	Description
U16	Z-80 processor
U21	8224 clock generator
Y1	18 MHz crystal
C25	56 pf capacitor

4 MHz Parts:

Part Numbers	Description
U16	Z-80A 4MHz processor
U21	8224 B 4MHz clock generator
Y1	36 MHz crystal
C25	20 pf capacitor

EPROM parts:

Part Numbers	Description
U33	8 positon dip switch
U34	8131 6 bit comparator
VR1	7905 -5 volt regulator
VR3	7812 +12 volt regulator
C17, C18, C19	1.5 uf capacitor
C12, C13, C15	1 uf capacitor

USART Parts:

Part Numbers	Description
U1, U23	8 position dip switch
U3	8251 USART
U2	MC14411 baud rate generator
U24	8131 6 bit comparator
U9	1489 RS232 receiver
U12	1488 RS232 driver
Y2	1.8432 MHz crystal
VR3	7812 +12 volt regulator
VR2	7912 -12 volt regulator
C17, C20, C21	1.5 uf capacitor
C13, C14, C15	1 uf capacitor
R6	22 meg resistor

Options

A. 2 MHz operation
Install:
1) 18 MHz crystal at Y1
1 uh coil at L1
.1 uf cap at C26
56 pf cap at C25
3) Jumper from U to S.

B. 4 MHz operation
Install:
1) 36 MHz crystal at Y1
2) If overtone type crystal, then:
1 uh coil at C26
20 pf cap at C25
3) Jumper from U to T.

C. On board EPROM:
Install:
8 position switch module at U33.
24 pin chip socket at U13.
16 pin chip socket at U34
8131 IC at U34.
2704/2708/2716/2516/2532 EPROM at U13

2704/2708 EPROM
1) Install 7905 regulator at VR1.
Install 7812 regulator at VR3 (used for USART also).
2) Install 1.5 uf capacitors at C19, C18, and C17.
Install .1 uf capacitors at C13, C15, and C12.
3) Set switch 1 on U33 to off.
Set switch 8 on U33 to on.
4) Select EPROM address from table III-1 and set switches on U33 as shown.

TMS 2716 EPROM
1) Install 7905 regulator at VR1.
Install 7812 regulator at VR3, (used for USART also)
2) Install 1.5 uf capacitors at C19, C18, and C17.
Install .1 uf capajcitors at C13, C15, and C12.
3) Install jumpers:
A to C
D to B
4) Set switch 1 and 7 on U33 to on. Set switch 8 on U33 to off.
5) Select EPROM Address from table III-2 and set switches on U33 as shown.

INTEL 2716/TMS 2516 EPROM
1) Cut etch L to E.
Cut etch F to M.
2) Install jumper from D to M.
Install jumper from C to B.
Install jumper from I to A.
3) Set Switch 1 and 7 on U33 to on.
Set switch 8 on U33 to off.
4) Select EPROM address from table III-2 and set switches on U33 as shown.
Install jumper from +5 to E.

INTEL 2732/TMS 2532 EPROM
1) Cut etch L to E.
Cut etch F to M.
Cut etch G to H.
2) Install jumper from D to M.
Install jumper from C to B.
Install jumper from G to E.
Install jumper from H to I.
3) Set switch 1, 2, and 7 on U33 to on.
Set Switch 8 on U33 to off.
4) Select EPROM address from table III-3 and set switches on U33 as shown.
Install jumper from A to I.

D. No EPROM and no power-on jump:
Set swich 7 and 8 on U23 to off.

E. Power-on jump:
Note: An EPROM must be on the board to use the power-on jump option.
Set switch 8 on U23 (if installed) to on.
Jumper U23 pin 8 to 9 if switch not installed.

F. EPROM wait state:
Note: An EPROM must be on the board to use this option.
Set switch 7 on U23 (if installed) to on.
Jumper U23 pin 7 to 10 if switch not installed.

G. USART option:
1) Install:
28 pin socket at U3
24 pin socket at U2
16 pin socket at U24
14 pin sockets at U9 and U12
8 position dip switch at U1 and U23
8251A IC at U3
MC14411 IC at U2
8131 IC at U24
1489 IC at U9
1488 IC at U12
1.8432 MHz crystal at Y2
22 Meg resistor at R6
7912 regulator at VR2
7812 regulator at VR3, (used for EPROM also)
1.5 uf capacitors at C20, C21, and C17
.1 uf capacitors at C14, C15, and C13.
2) Set one switch on U1 to desired baud rate, (silk screened next to U1 switches) and set all other switches on U1 to off.
3) Select desired I/O port address from table III-4 and set switches on U23 as shown.

H. Shadow EPROM option:
1) Cut etch J to K.
2) Install EPROM as shown in option C.
3) Enable power-on jump as shown in E.
When the system is powered-up, or rreset is activated, the processor will run code from the EPROM. The processor will continue running from the EPROM until a jump occurs to thje address range selected by the switches on U33. Note that the program in the EPROM should be assembled to run in an address range other than the one selected by U33. When the jump to the address range selected by U33 is detected, the EPROM will no longer be accessed, and is transparent to the system. The program in the EPROM may be assembled to run in any address range, (as long as it is different from the one selected by U33). Program function is not affected by the address range the program is assembled to run at. However, the first instruction to be executed must be at the starting address of a valid address range (as selected from charts III-1, III-2, or III-3) for the EPROM being used.

Table III-1 2704/2708 EPROM Address Select (U33)

Address Range	SW3 A15	SW6 A14	SW4 A13	SW5 A12	SW2 A11	SW7 A10
0000-03FF	X	X	X	X	X	X
0400-07FF	X	X	X	X	X	
0800-0BFF	X	X	X	X		X
0C00-0FFF	X	X	X	X		
1000-13FF	X	X	X		X	X
1400-17FF	X	X	X		X	
1800-1BFF	X	X	X			X
1C00-1FFF	X	X	X			
2000-23FF	X	X		X	X	X
2400-27FF	X	X		X	X	
2800-2BFF	X	X		X		X
2C00-2FFF	X	X		X		
3000-33FF	X	X			X	X
3400-37FF	X	X			X	
3800-3BFF	X	X				X
3C00-3FFF	X	X				
4000-43FF	X		X	X	X	X
4400-47FF	X		X	X	X	
4800-4BFF	X		X	X		X
4C00-4FFF	X		X	X		
5000-53FF	X		X		X	X
5400-57FF	X		X		X	
5800-5BFF	X		X			X
5C00-5FFF	X		X			
6000-63FF	X			X	X	X
6400-67FF	X			X	X	
6800-6BFF	X			X		X
6C00-6FFF	X			X		
7000-73FF	X				X	X
7400-77FF	X				X	
7800-7BFF	X					X
7C00-7FFF	X					

X = switch on

Table III-1 (continued)

Address Range	SW3 A15	SW6 A14	SW4 A13	SW5 A12	SW2 A11	SW7 A10
8000-83FF		X	X	X	X	X
8400-87FF		X	X	X	X	
8800-8BFF		X	X	X		X
8C00-8FFF		X	X	X		
9000-93FF		X	X		X	X
9400-97FF		X	X		X	
9800-9BFF		X	X			X
9C00-9FFF		X	X			
A000-A3FF		X		X	X	X
A400-A7FF		X		X	X	
A800-ABFF		X		X		X
AC00-AFFF		X		X		
B000-B3FF		X			X	X
B400-B7FF		X			X	
B800-BBFF		X				X
BC00-BFFF		X				
C000-C3FF			X	X	X	X
C400-C7FF			X	X	X	
C800-CBFF			X	X		X
CC00-CFFF			X	X		
D000-D3FF			X		X	X
D400-D7FF			X		X	
D800-DBFF			X			X
DC00-DFFF			X			
E000-E3FF				X	X	X
E400-E7FF				X	X	
E800-EBFF				X		X
EC00-EFFF				X		
F000-F3FF					X	X
F400-F7FF					X	
F800-FBFF						X
FC00-FFFF						

X = switch on

Table III-2 2716/2516 EPROM Address Select (U33)

Address Range	SW3 A15	SW6 A14	SW4 A13	SW5 A12	SW2 A11
0000-07FF	X	X	X	X	X
0800-0FFF	X	X	X	X	
1000-07FF	X	X	X		X
1800-1FFF	X	X	X		
2000-27FF	X	X		X	X
2800-2FFF	X	X		X	
3000-37FF	X	X			X
3800-3FFF	X	X			
4000-47FF	X		X	X	X
4800-4FFF	X		X	X	
5000-57FF	X		X		X
5800-5FFF	X		X		
6000-67FF	X			X	X
6800-6FFF	X			X	
7000-77FF	X				X
7800-7FFF	X				
8000-87FF		X	X	X	X
8800-8FFF		X	X	X	
9000-97FF		X	X		X
9800-9FFF		X	X		
A000-A7FF		X		X	X
A800-AFFF		X		X	
B000-B7FF		X			X
B800-BFFF		X			
C000-C7FF			X	X	X
C800-CFFF			X	X	
D000-D7FF			X		X
D800-DFFF			X		
E000-E7FF				X	X
E800-EFFF				X	
F000-F7FF					X
F800-FFFF					

X = switch on

Table III-3 2732 EPROM Address Select (U33)

Address Range	SW3 A15	SW6 A14	SW4 A13	SW5 A12
0000-0FFF	X	X	X	X
1000-1FFF	X	X	X	
2000-2FFF	X	X		X
3000-3FFF	X	X		
4000-4FFF	X		X	X
5000-5FFF	X		X	
6000-6FFF	X			X
7000-7FFF	X			
8000-8FFF		X	X	X
9000-9FFF		X	X	
A000-AFFF		X		X
B000-BFFF		X		
C000-CFFF			X	X
D000-DFFF			X	
E000-EFFF				X
F000-FFFF				

X = switch on

Table III-4 USART Address Select (U23)

Address Range	SW1 A7	SW2 A6	SW3 A5	SW4 A4	SW5 A3	SW6 A2
00-01	X	X	X	X	X	X
04-05	X	X	X	X	X	
08-09	X	X	X	X		X
0C-0D	X	X	X	X		
10-11	X	X	X		X	X
14-15	X	X	X		X	
18-19	X	X	X			X
1C-1D	X	X	X			
20-21	X	X		X	X	X
24-25	X	X		X	X	
28-29	X	X		X		X
2C-2D	X	X		X		
30-31	X	X			X	X
34-35	X	X			X	
38-39	X	X				X
3C-3D	X	X				
40-41	X		X	X	X	X
44-45	X		X	X	X	
48-49	X		X	X		X
4C-4D	X		X	X		
50-51	X		X		X	X
54-55	X		X		X	
58-59	X		X			X
5C-5D	X		X			
60-61	X			X	X	X
64-65	X			X	X	
68-69	X			X		X
6C-6D	X			X		
70-71	X				X	X
74-75	X				X	
78-79	X					X
7C-7D	X					

X = switch on

Table III-4 (continued)

Address Range	SW1 A7	SW2 A6	SW3 A5	SW4 A4	SW5 A3	SW6 A2
80-81		X	X	X	X	X
84-85		X	X	X	X	
88-89		X	X	X		X
8C-8D		X	X	X		
90-91		X	X		X	X
94-95		X	X		X	
98-99		X	X			X
9C-9D		X	X			
A0-A1		X		X	X	X
A4-A5		X		X	X	
A8-A9		X		X		X
AC-AD		X		X		
B0-B1		X			X	X
B4-B5		X			X	
B8-B9		X				X
BC-BD		X				
C0-C1			X	X	X	X
C4-C5			X	X	X	
C8-C9			X	X		X
CC-CD			X	X		
D0-D1			X		X	X
D4-D5			X		X	
D8-D9			X			X
DC-DD			X			
E0-E1				X	X	X
E4-E5				X	X	
E8-E9				X		X
EC-ED				X		
F0-F1					X	X
F4-F5					X	
F8-F9						X
FC-FD						

X - switch on

IV. Circuit Description

The Z-80 address bus is driven to the S100 bus by U35, U36 and a portion U25. The ADDSB signal on pin 22 will tri-state the address bus for DMA or maintenance functions when driven low.

The S100 DI (data in) bus is provided to the Z-80 during read memory or I/O input cycles by U38 and a portion of U29. The DI bus receivers are disabled when a write memory or I/O output cycle is performed. They are also disabled by the following conditions:

1) SSWDSB low at pin 53.
2) RUN and SS low at pins 71 and 21.
3) EPROM selected during memory read operation.
4) USART selected during I/O operation.
5) Power-on jump enabled and Power-on latch (2 sectins of U10) is set.

The Z-80 data bus is provided to the S100 data out (DO) bus for memory write or I/O output cycles by U37 and part of U25. The DODSB signal on pin 23 will tri-state the data out bus for DMA or maintenance functions when driven low.

The Z-80 clock and reset signals are generated by U21. The crystal and tank circuit used allow operation at 2 or 4 MHz. When the RESET signal on pin 75 is driven low, U21 provides a reset signal to the Z-80 and the power-on jump latch if used. This signal is provided to the S100 bus as POC at pin 99. Pin 75 is held low mementarily during power-up due to the time it takes to charge C22. 01 and 02 signals are provided to the S100 bus on pins 24 and 25. The S100 bus 2 MHz CLOCK signal on pin 49 is derived from 02 directly for 2 MHz operation and is divided down by U21 for 4 MHz operation.

The Z-80 WAIT signal is activated by the following conditions:

1) XRDY on pin 3 going low.
2) PRDY on pin 72 going low.
3) First 02 clock cycle after EPROM is selected when EPROM wait state is enabled, (U20).

EPROM wait state is enabled, (U20). PWAIT on pin 27 will go high to indicate when the Z-80 wait signal is enabled.

The following S100 signals are derived form the Z-80 RD, WR, IORQ, MRQ, M1, and RFSH signals:

1) SOUT + WR and IORQ (output to I/O port).
2) SINP + RD and IORQ (input from I/O port).
3) SMEMR + RD and MRQ (read memory).
4) MWRT + WR and MRQ (write memory).
5) PWR + WR and MRQ (processor is outputing data).
6) INTA + M1 and IORQQ (interrupt acknowledge).
7) PDBIN + RD or INTA (processor inputing data).
8) RFSH + RFSH (refresh access request).
9) MRQ + MRQ (memory access request).
10) SM1 + M1 (processor fetching instruction op code).
11) SWO + RD and INTA (processor not inputing data). This signal is used as an early indication that a write operation will take place.
12) PSYNC +IORQ or MRQ and RFSH (valid memory or I/O access). The PSYNC signal is only high during the first part of a memory or I/O cycle due to multi U5. This signal is provided for S100 bus devices that look at status information during the first portion of a cycle as per 8080 device conventions. SINP, SMEMR, and SWO are latched by PSYNC on U40 before being placed on the S100 bus to make look like 8080 status signals.

The STADSB signal on pin 18 will tri-state the SOUT, SINP, SMEMR, SWO, and SM1 signals when it is driven low. The CCDSB signal on pin 19 will tri-state the PDBIN, INTA, PSYNC, nd PWR signals when it is driven low. When a front panel is not used, the RUN signal from the processor board. When a front panel makes RUN low, the MWQRT signal is tri-stated to allow the front panel circuitry to perform writes to memory with its own MWRT signal.

The Z-80 BUSRQ signal is activated when the PHOLD signal on pin 74 is driven low. The Z-80 tri-states its data and address busses and generates BUSAK low in response to BUSRQ. BUSAK is provided to the S100 bus as HLDA on pin 26 to acknowledge that the processor is in a "hold" condition. HLTA is provided as HLTA on pin 48 whenever the Z-80 is executing a halt instruction.

The INT signal on pin 73 will cause the Z-80 maskable interrupt request to become active when driven low.

The EPROM (U13) is selected by the power-on jump latch (2 sections of U10) after it is set by the reset signal. The address bus is compared to switch settings of U33 by comparator U34. When the selected address range is detected the power-on latch is reset by the comparator output. The comparator output will also select the EPROM when the shadow EPROM option is not installed. The EPROM is accessed only when memory is requested.

The lower portion of the address bus is compared to the switch settings of U23 by comparator U24. When the selected address range is detected during an I/O operation, the USART (U3) is enabled. The USART derives its transmit and receive clock from the baud rate generator U2. The desired clock rate is selected by switch module U1. All the clocks are 16 times the baud rate indicated. The USART should be programmed for 16X clocks. Refer to vendor data for detailed programming information on the 8251. The transmit data (TXD), receive data (RXD), and reverse channel (RVC) signals are provided at connector socket U19.

JADE Z-80 KIT

PACK #1
1 Z-80 CPU
1 8224
1 18 MHz Crystal
1 56pf Disc Cap

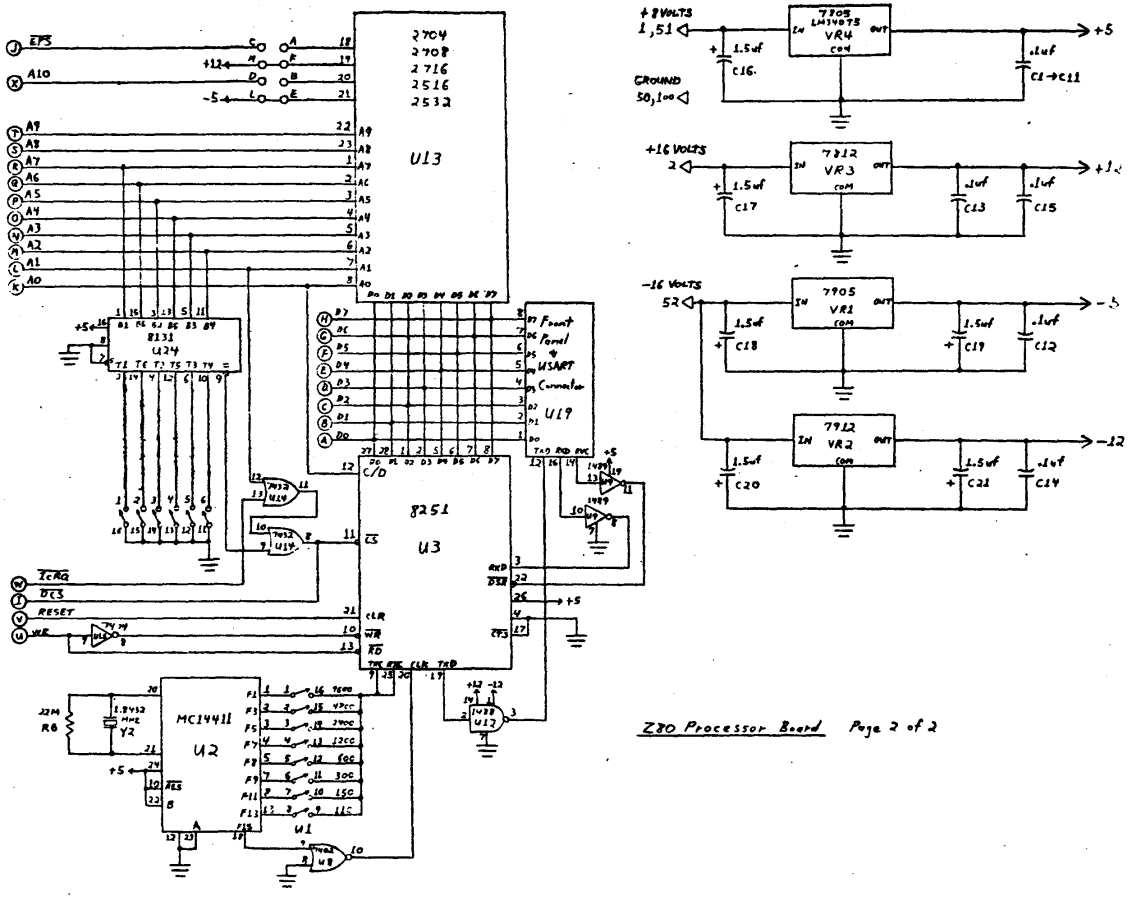
PACK #2
1 Z80A CPU
1 8224-4
1 36MHz Crystal
1 20pf Disc Cap

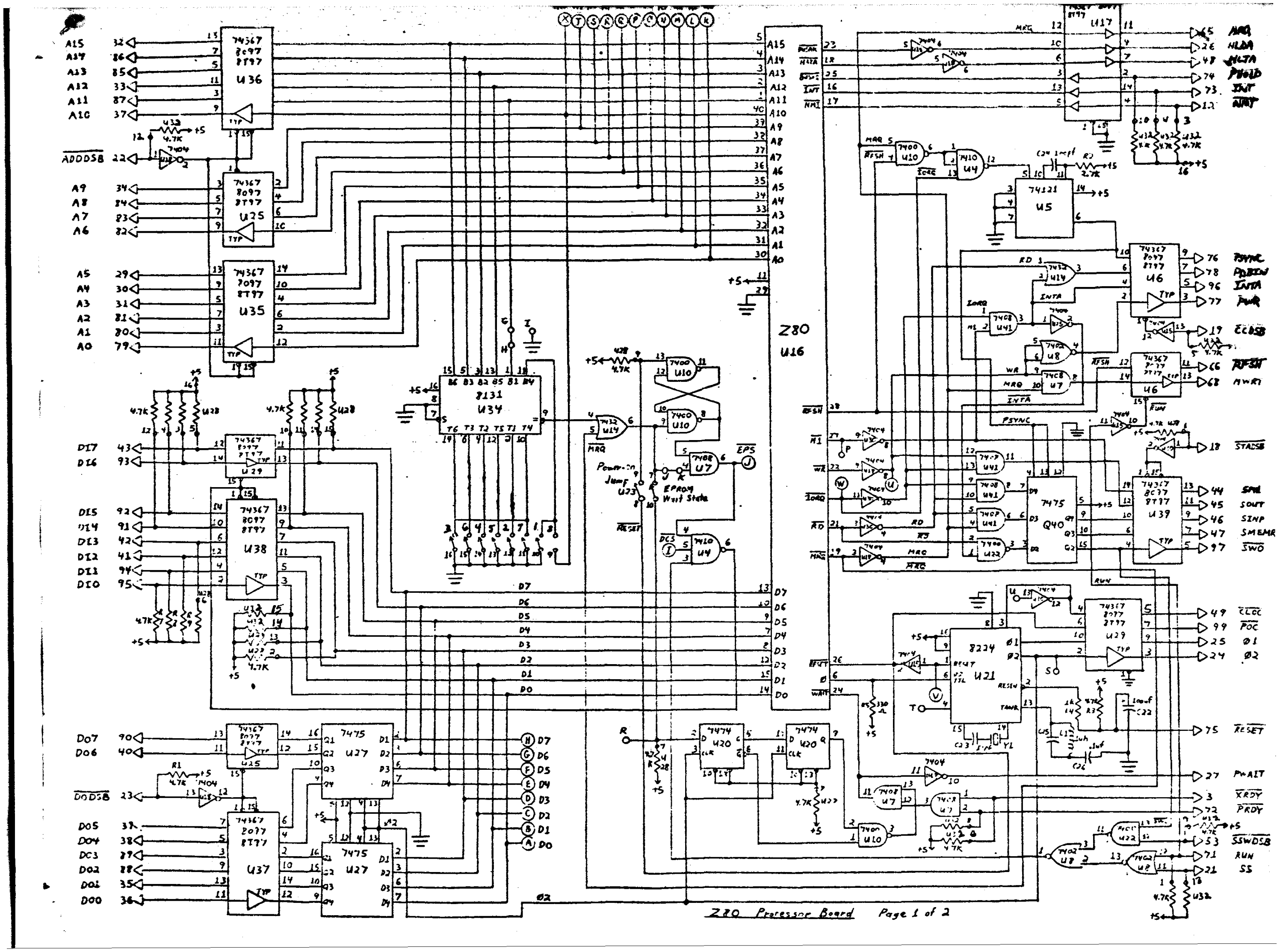
PACK #3
2 7400
1 7402
3 7404
2 7408
1 7410
1 7432
1 7474
3 7475
1 74121
9 74367/8097/8T97
2 DM8131
1 8251
1 MC14411
1 1488
1 1489
1 LM320T-5/7905
1 LM320T-12/7912
1 LM340T-5/7805
1 LM340T-12/7812
3 8 Postion Dip Switch

PACK #4
1 330 ohm ¼W 5%
1 1K
1 2.7K
5 4.7K
1 22meg./20meg.
2 4.7K 16 pin 15 res. Resistor Pack
16 .lmf Disc
6 1.5/1.8mf Disc
1 10pf Disc
1 100pf Disc
1 100mf 25U Axial Electrolytic
1 1Uh Coil

PACK #5
17 14 pin Lo Pro Sockets
12 16 pin Lo Pro Sockets
2 24 pin Lo Pro Sockets
1 40 Pin Lo Pro Sockets

PACK #6
1 373 Heatsink
4 6-32 Hex Nut
4 6-32 x ¾" Screw
4 6-32 Lockwasher


2704
2708
2716
2516
2532
U13
8251
U3
8131
U24
MC14411
U2
U19
Front Panel & USART Controller
+8 VOLTS
1,51
7805
VR4
+5
GROUND
50,100
+16 VOLTS
2
7812
VR3
+12
-16 VOLTS
52
7905
VR1
-5
7912
VR2
-12
1.5uf
.1uf
C16
C17
C18
C19
C20
C21
C1→C11
C13
C15
C12
C14
EPS
A10
+12
-5
TxRq
DC3
RESET
WR
RD
CLR
CS
C/D
Z80 Processor Board
Page 2 of 2



Z80 Processor Board Page 1 of 2