P.O. BOX 2119
CANYON COUNTRY, CA 91351

A/D/A

ANALOG TO DIGITAL
AND
DIGITAL TO ANALOG

CONVERTER BOARD

USER MANUAL

I/O TECHNOLOGY

52748-900

A / D / A

ANALOG TO DIGITAL
AND
DIGITAL TO ANALOG

CONVERTER BOARD

P/N 52748-900

U S E R M A N U A L

Revision 6, 5/84

INPUT/OUTPUT TECHNOLOGY, INC.

25327 AVENUE STANFORD, UNIT 113 VALENCIA, CA. 91355

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1.0 Introduction and General Information

We thank you for selecting the A/D/A (Analog to Digital and Digital to Analog) Converter Board and we hope that you find our product to your satisfaction.

The A/D/A Board design provides maximum flexibility and capability to operate in existing 8-bit S-100 systems and in the 8/16-bit IEEE-696 systems.

The 8 channels of A/D and 8 channels of D/A make the A/D/A Board a versatile tool in an unlimited range of analog applications.

All of our products are manufactured to high standards thus providing you with a reliable and low maintenance product. We have compiled this voluminous manual to provide maximum information, procedures and data so to enable the user to fully utilize the on-board features.

1.1 General Information

1.1.1 Receiving Inspection

Carefully inspect the module or kit for signs of damage during shipment. Also check packing list to insure that contents correspond with list.

Should any discrepancies or damage be found, please notify us at once, describing the discrepancy, so that we can take appropriate action.

1.1.2 Factory Service

Factory Service is available for in-warranty and out-of-warranty boards.

In order to utilize INPUT/OUTPUT TECHNOLOGY, INC. services, it is required that you obtain an authorizaton number. Upon receipt of the factory service authorization number, package the unit (preferably in original container to prevent damage during shipment) and return postpaid to:

INPUT/OUTPUT TECHNOLOGY, INC.
UNIT 113
25327 AVENUE STANFORD
VALENCIA, CA.
91355

Under separate correspondence, send information of shipment and description of problem. We suggest that you insure the package: if you do not want us to insure the return shipment, please specify in your correspondence.

1.1.3 Replacement Parts

Replacement parts are available from INPUT/OUTPUT TECHNOLOGY, INC. upon request. When requesting in-warranty parts, you must return the faulty part: this excludes resistors, capacitors, jumper connectors and edge connectors. This will enable us to analyze faulty part(s) for type and cause(s) of failure.

1.1.4 Warranty

Because of the diversity of conditions and hardware under which this product may be used, no warranty of fitness for particular purpose is offered. INPUT/OUTPUT TECHNOLOGY, INC. assumes no liability whatsoever from use or sale of this product.

All INPUT/OUTPUT TECHNOLOGY, INC. modules have a 3 month warranty. For specifics of warranty see page 1-4.

The user shall restore the A/D/A board to the original factory configuration prior any in or out-of-warranty repair service can be rendered by INPUT/OUTPUT TECHNOLOGY, INC..

1.1.5 Life Support Policy

INPUT/OUTPUT TECHNOLOGY, INC.'s products are not authorized for use as critical components in life support devices or systems without the express written approval of INPUT/OUTPUT TECHNOLOGY, INC.. As used herein:

1. Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

1.1.6 Tools and Supplies

The tools and supplies required to configure the A/D/A Board are as follows:

-Wire Wrap Tool, i.e., O.K. Machine and Tool makes several types for AWG 30 .025 in. square post.
-AWG 30 wire.
-25W Soldering Iron
-60/40 Rosin Flux Solder

INPUT/OUTPUT TECHNOLOGY, INC.
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VALENCIA, CA.
91355

I M P O R T A N T

PLEASE FILL OUT AND RETURN TO
INPUT/OUTPUT TECHNOLOGY, INC. SO THAT WE MAY KEEP YOU
INFORMED OF ALL CHANGES AND PROVIDE YOU WITH
ADDITIONAL INFORMATION AS IT BECOMES AVAILABLE

REGISTERED OWNER_____

ADDRESS_____

CITY_____STATE_____ZIP_____

PURCHASED FROM_____DATE PURCHASED_____

CITY_____STATE_____ZIP_____

MODEL #52748-_____-_____ SERIAL #_____

OPTIONAL:

THIS PRODUCT WILL BE USED IN_____

MY COMPUTER IS_____USED IN INDUSTRY

_____USED IN BUSINESS

_____A HOBBY COMPUTER

HOW DID YOU HEAR ABOUT THIS PRODUCT:
IF MAGAZINE AD, PLEASE SPECIFY NAME_____

_____

WHY DID YOU BUY OUR PRODUCT RATHER THAN COMPETITORS?

_____

COMMENTS (USE OTHER SIDE IF MORE SPACE NEEDED)

1.2 A/D/A Board Specifications

1.2.1 A/D Characteristics

Resolution..... 12 Bits

Converson Time..... 12 µsec.

Dynamic Channel Sample Rate (Nom.)..... 50 KHz

Input Channels..... 8 Single Ended
(Under Program Control) or 4 Differential or Mixed

Input Voltage Range..... ±10V
(Protected Inputs)

Gain Steps..... X.5, X2, X8, X32
(Under Program Control)

Input Impeadance..... Greater than 10 MΩ

Offset Voltage..... Less than 1 LSB*

Other A/D Features:

*-Auto Offset voltage correction using dedicated 8-Bit DAC in A/D converter under full software control.
-Optional current input mode on-board selectable for any channel.
-'Conversion Complete' signal thru interrupt and/or status word read.
-A/D Channel Address tag contained with each converted word (upper byte).

1.2.2 D/A Characteristics

Resolution..... 12 Bits

Settling Time..... 2 µsec.

Dynamic Channel Refresh Rate (Nom.)..... 250 KHz

Output Channels..... 8 Single Ended

Type of Outputs:
Bipolar Voltage..... ±10, ±5, ±2.5V
Unipolar Current..... 0-10 MA
(Jumper Selectable) 0-20 MA
0-40 MA
0-80 MA

Programmable Reference Levels..... 10, 5, 2.5V

Voltage Load Current..... 2 MA

Output Impeadance (Voltage)..... 0.25 Ω

Other D/A Features:

-All Outputs set to 0.V at Power-On.
-Auto Refresh for each D/A channel using on-board Dual-Ported RAM.
-Two Page Dual-Ported RAM may be used for rapid D/A set up, i.e. calibration or test waveform.
-Auto Refresh with software override on individual D/A channel for maximum waveform control.

1.2.3 Support Circuitry Characteristics

-8/16-Bit Access using I/O Port or Memory Mapped Data Transfers.
-24 Bit Extended Addressing with Extended Address Disable Logic.
-Phantom Select Logic and SIXTEEN Acknowledge Status Logic.
-'PHOLDA' Status Select Logic for DMA Applications.
-No Wait Cycles Requried.
-Fully Socketed.

1.2.4 Physical Characteristics

Dimensions..... 5.125 in. H x .10 in. W x .5 in. Max. D

Weight..... 12 oz.

1.2.5 Input Power Requirements

8 VDC Input..... 950 ma. Max

18 VDC Input..... 100 ma. (NOM)*

-18 VDC Input..... 80 ma. (NOM)*

*Quiescent level

1.3 Parts List

ITEM	QUANTITY	DESCRIPTION	SCHEMATIC DESIGNATION
1 ( )	1 ( )	P.C. Board	P/N 52748-9XX
2 ( )	1 ( )	24 Pin Socket	U28
3 ( )	15 ( )	20 Pin Socket	U2, U3-U11, U16, U17, U27, U31, U41
4 ( )	12 ( )	16 Pin Socket	U12, U19, U20, U22-U24, U29, U32-U34, U39, U42
5 ( )	10 ( )	14 Pin Socket	U13-U15, U18, U21, U25, U35-U36, U40
6 ( )	4 ( )	8 Pin Socket	U1, U26, U37-U38
7 ( )	3 ( )	2.2 KΩ, 1/4W, 5%	R1-R3
8 ( )	4 ( )	2.2 KΩ X 7 SIP, 5%	RP1 - RP4
9 ( )	2 ( )	80.0 KΩ, 1/4W, .1%	R17, R22
10 ( )	3 ( )	20.0 KΩ, 1/4W, .1%	R16, R21, R34
11 ( )	9 ( )	10.0 KΩ, 1/4W, .1%	R18, R23, R24, R32, R33, R35, R38, R42, R53
11A( )	6/3 ( )	10.0 KΩ/5.0KΩ 1/4W, .1%	[R12, R13], [R14, R15], [R19, R20]
12 ( )	2 ( )	5.0 KΩ, 1/4W, .1%	R26, R25
13 ( )	2 ( )	2.5 KΩ, 1/4W, .1%	R41, R54
13A( )	6/3 ( )	2.5 KΩ/1.25KΩ 1/4W, .1%	[R28A, R28B] [R27A, R27B] [R43, R44]
14 ( )	2 ( )	4.3 KΩ, 1/4W, 5%	R29, R30
15 ( )	1 ( )	1 MΩ, 1/4W, 5%	R39
16 ( )	1 ( )	150 Ω, 1/4W, 5%	R56
16A( )	1 ( )	470 Ω, 1/4W, 5%	R57

* [ ] Paralleled resistor pairs may be supplied as single equivalent values

1.3 Parts List (continued)

ITEM	QUANTITY	DESCRIPTION	SCHEMATIC DESIGNATON
17 ( )	16 ( )	0.1 µF, 20 VDC Disk or Monolithic Capacitor	C1, C5, C6, C7, C10, C11, C17, C18 C22, C24, C26-C29 C31, C32
18 ( )	6 ( )	.01 µF, 20 VDC Disk or Monolithic Capacitor	C3, C23, C25 C30, C33, C34
19 ( )	4 ( )	120 pF, 20 VDC Disk or Mica Capacitor	C21, C34A CX1, CX2
20 ( )	1 ( )	470 pF, 20 VDC Disk or Mica Capacitor	C19
21 ( )	4 ( )	2.2 µF - 6.8 µF, 20 VDC min.Tantalum Capacitor	C8, C12, C14, C20
22 ( )	2 ( )	2.2 µF - 6.8 µF 8 VDC min. Tantalum Capacitor	C2, C4
22A( )	9 ( )	2200 pF, 35 VAC Polystyrene Capacitor	CA1-CA9
23 ( )	19 ( )	Single Row Header Pins .100 in spacing	J2, J4, J6-J9
24 ( )	49 ( ) PAIRS	Double Row Header Pins .100 in spacing	J1, J3, J5, J11, J13-J17
25 ( )	30 ( ) PAIRS	Double Row Header Right Angle Pins .100 in spacing	CA, CB
26 ( )	1 ( )	74LS02 I.C.	U21
27 ( )	4 ( )	74LS74 I.C.	U13, U15, U18, U31
28 ( )	1 ( )	74LS86 I.C	U14
29 ( )	1 ( )	74LS163 I.C.	U19
30 ( )	1 ( )	74LS174 I.C	U12
31 ( )	1 ( )	74LS240 I.C.	U4

1.3 Parts List (continued)

ITEM	QUANTITY	DESCRIPTION	SCHEMATIC DESIGNATION
32 ( )	2 ( )	74LS244 I.C.	U9, U11
33 ( )	1 ( )	74LS157 I.C.	U20
34 ( )	3 ( )	74LS289 I.C.	U32, U33, U34
35 ( )	1 ( )	74LS373 I.C.	U6
36 ( )	5 ( )	74LS374 I.C.	U7, U8, U10, U16, U30
37 ( )	2 ( )	25LS2521 I.C.	U2, U3
38 ( )	1 ( )	75452 I.C.	U1
39 ( )	2 ( )	PAL16L8 I.C.	U5, U7
40 ( )	1 ( )	DG508A I.C.	U42
41 ( )	4 ( )	DG509 I.C. or MUX-24	U22, U23, U24, U39
42 ( )	1 ( )	DM2504 I.C.	U28
43 ( )	3 ( )	LF347B I.C. or MC34004B	U35, U36, U40
43A( )	1 ( )	LF347B I.C.	U25
44 ( )	2 ( )	Am6012 I.C.	U27, U41
45 ( )	1 ( )	DAC-08 I.C.	U29
46 ( )	1 ( )	REF-01 I.C. MC1404-10	U38
47 ( )	1 ( )	CMP-01 I.C.	U26
48 ( )	1 ( )	LF398 I.C.	U37
49 ( )	8 ( )	2N2222A Transistor	Q1-Q8
50 ( )	20 ( )	1N914A Diode	CR1-CR16, CR18-CR21
50A( )	2 ( )	1N966B Zener Diode	CR16A, CR17
50B( )	2 ( )	1N6263 Schotky Diode	CR23A,CR23B
51 ( )	1 ( )	20.0K Potentiometer	R57
52 ( )	1 ( )	LM323K, 5V, 3A Regulator	VR1

1.3 Parts List (continued)

ITEM	QUANTITY	DESCRIPTION	SCHEMATIC DESIGNATION
53 ( )	1 ( )	7815, 15V, .5 A Regulator	VR2
54 ( )	1 ( )	7915, -15V, .5 A Regulator	VR3
55 ( )	1 ( )	TO-3 Style Heatsink	--
56 ( )	2 ( )	TO-220 Style Heatsink	--
57 ( )	1 ( )	LED (Diode)	CR22
58 ( )	2 ( )	Laminated Bus Bar (15 pin)	--
59 ( )	2 ( )	3/8 in. Machine Screw	--
60 ( )	2 ( )	1/2 in. Machine Screw	--
61 ( )	4 ( )	Lock Washer	--
62 ( )	4 ( )	Nut	--
63 ( )	2 ( )	Card Ejector Handle	--
64 ( )	2 ( )	Locking pin for Item 63	--
65 ( )	1 ( )	28-30 GA. Wire 4.5 in.	--
66 ( )	1 ( )	Twisted Pair Wire 28-30 GA., 3.5 in.	--
67 ( )	1 ( )	26-30 GA. Wire	R55 Shorting Jumper
68 ( )	14 ( )	Shorting Plugs	--

2.0 Assembly and Check-Out

The assembly portion of the manual was not available at the time this manual was released. When available all registered users will be forwarded a copy of this section at no charge.

You may utilize the sample software procedures in section 8.0 for functional check-out of the board.

2.1 Factory Configuration

The factory assembled and tested A/D/A Board has been configured as follows:

J2 pin 1 to 2	Extended Address Field Disabled (A16 thru A23)
J4 pin 1 to 2	High Byte Address Field Disabled (A8 thru A15)
J8 pin 2 to 3	I/O Mode for writing to the board is selected
J9 pin 1 to 2	I/O Mode for reading from the board is selected
J8 pin 1 to 8 and J8 pin 4 to 5	Base Address of 80 Hex is selected
J13 and J14 All jumpers	All D/A channels are set for voltage output

The above base address selection will enable direct execution of the sample Basic programs without any modifications to the code.

3.0 Theory of Operation

3.1 A/D Section

For the following discussion refer to Figure 3.1 A/D Section Block Diagram and Section 10 Schematics.

3.1.1 Input Protection Networks

The eight analog inputs incorporate a protection network composed of a fuse device (optional), clamp diodes CR1 through CR16 and zener diodes CR16A and CR17. Input voltages in excess of ± 16.5 volts will be clamped and if sufficient current is available the fuse will be blown. This protects the A/D/A from serious damage resulting from excessive input voltage.

3.1.2 Multiplexer

The analog switches U22 and U23 are controlled from command latch U16 to select the desired channel and to control whether that channel will be received singly or as a differential pair.

3.1.3 Gain Select Circuit

The gain select curcuit is composed of analog switch U24, op-amps U25(A,B), and resistors R12 through R22. Gain is selected by the GSEL0 and GSEL1 bits from control latch U16.

3.1.4 Track and Hold Amplifier

This amplifier prevents slewing of the desired channel during convert time. It is permitted to track the input voltage for a period of time. Then it holds a constant voltage at the comparator input during the time of the conversion.

3.1.5 Voltage Reference

This reference (U38) is a stable voltage source which is used to define the full scale voltages of all A/D and D/A conversions performed by the A/D/A. It has a fine adjust potientiometer which should not be adjusted by the user unless a precision voltmeter (± 0.01%) is available.

3.1.6 Successive Approximation Register and Comparator

These parts U27, U28, and U37 are involved in a binary search during convert time.

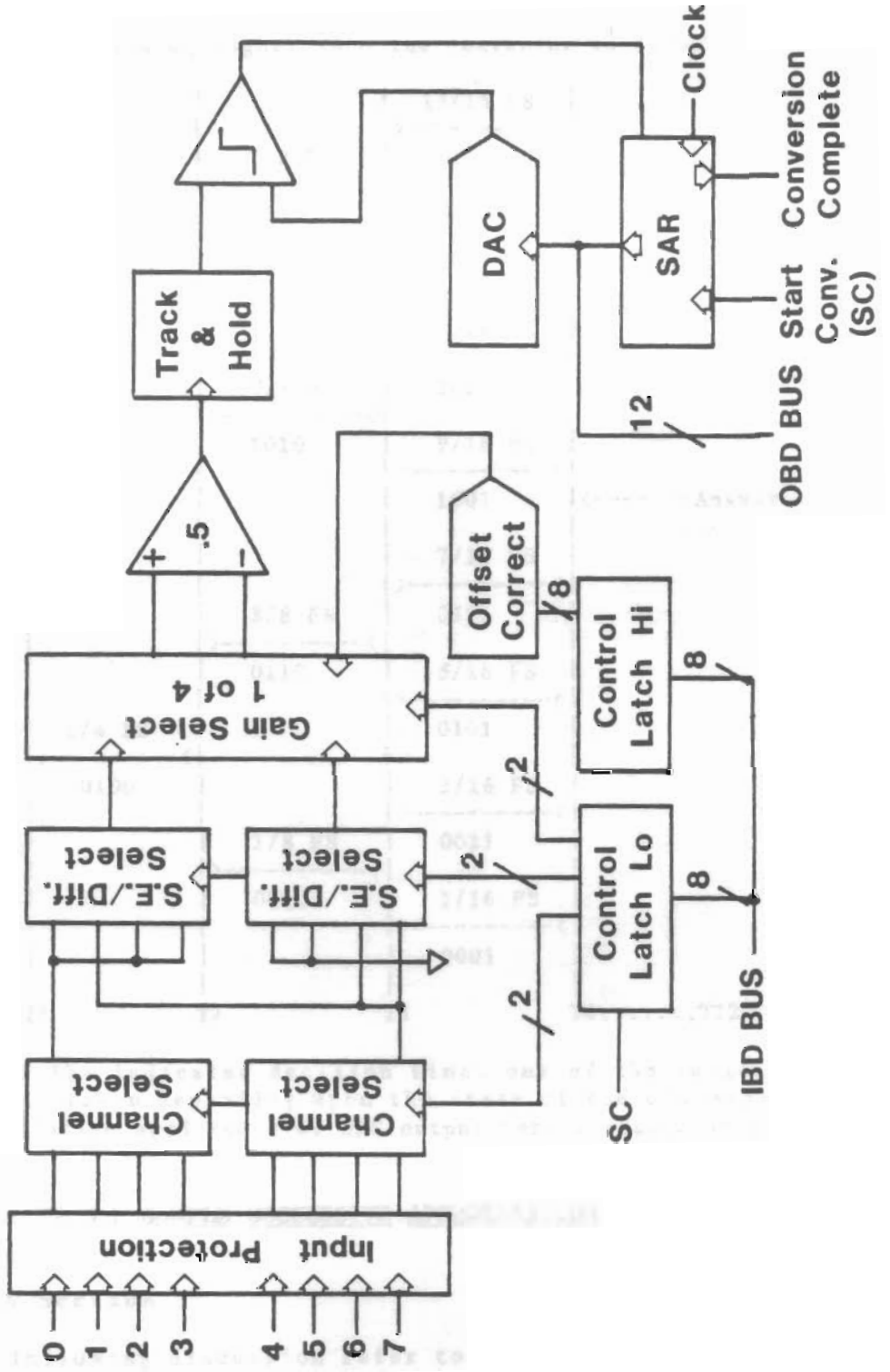
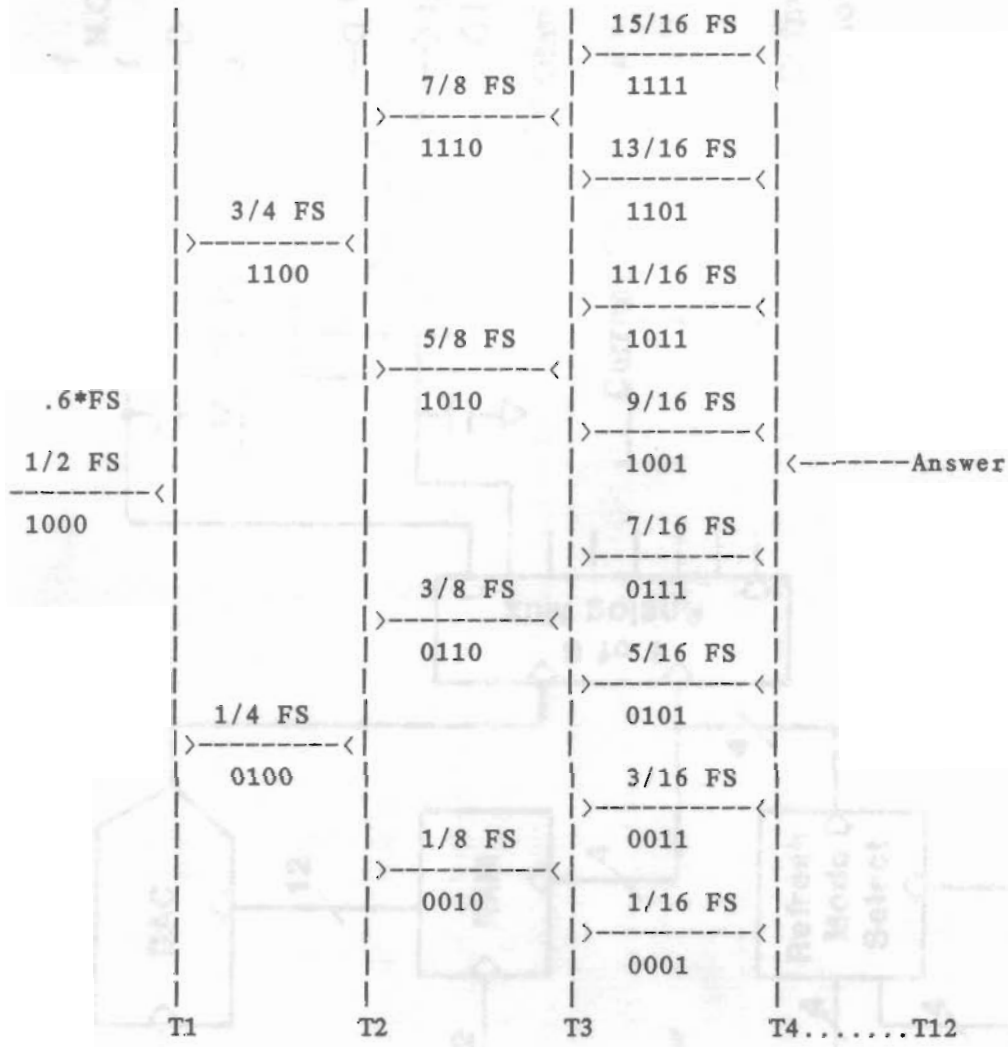


FIGURE 3.1 A/D SECTION BLOCK DIAGRAM

The first four bits of this algorithm will be shown here in Figure 3.2 for the benefit of those unfamilar with successive approximation techniques.

Assume that the analog signal into the converter is at 0.6 * FS.



At each of the indicated decision times one of the indicated branches is taken depending upon the state of the comparator. i.e. the relative amplitudes of DAC output versus analog input.

FIGURE 3.1 **SAMPLE SUCCESSIVE APPROXIMATION SEARCH**

3.2 D/A Section

For the following discussion refer to Figure 3.3 D/A Section Block Diagram.

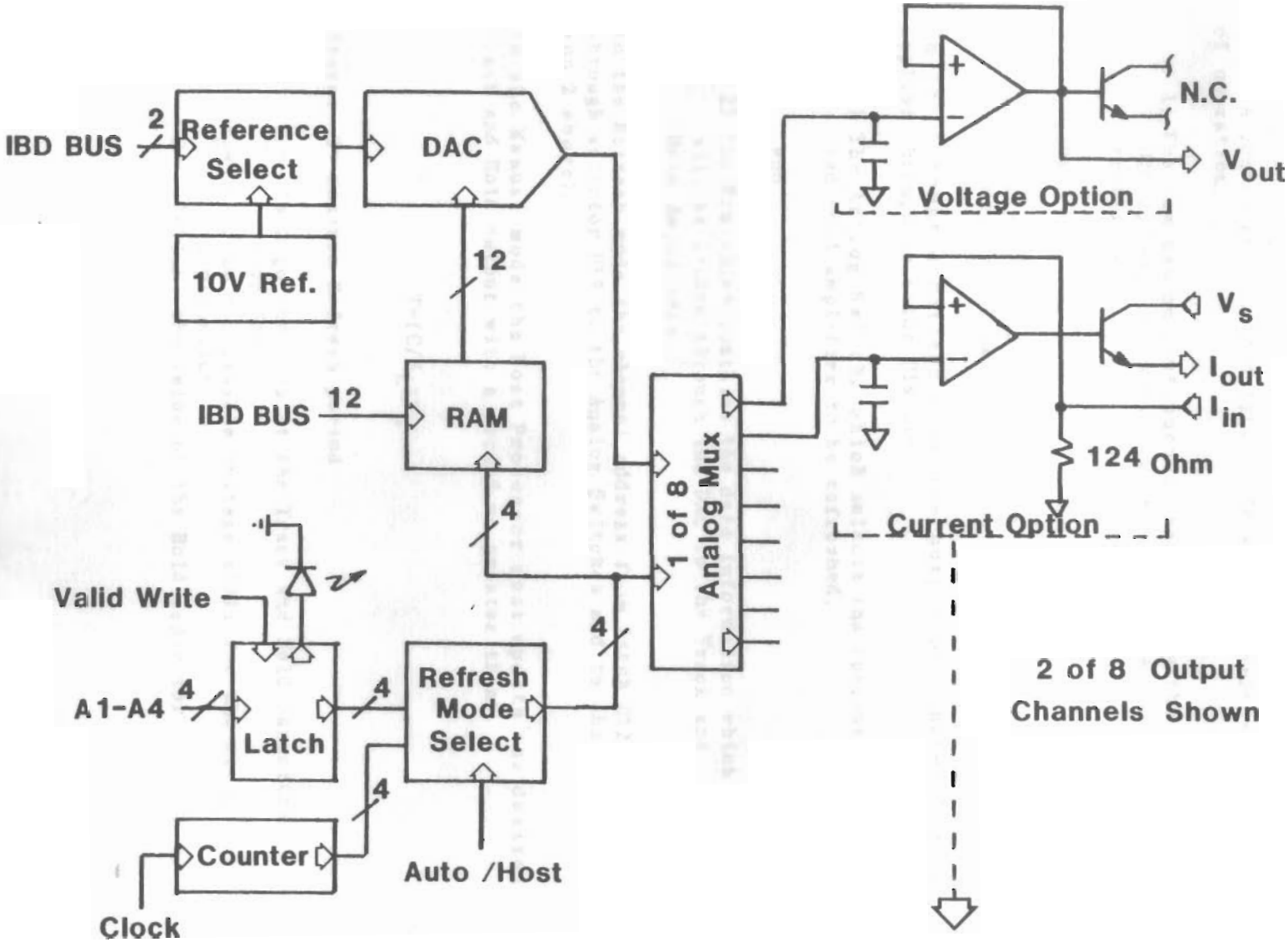


FIGURE 3.3 D/A SECTION BLOCK DIAGRAM

3.2.1 Data Buffer

A 12-bit Ram (U32-U34) receives binary data from the host system data bus. The contents of this Ram is then presented to the 12-bit D/A converter U41. This type of data input supports two modes of operation:

1) The ram can be continuously recycled by the counter U20 to keep the output track and hold amplifiers refreshed,

   or

2) For tighter control of a given output, this burden may be assumed by the host processor.

In the Automatic Refresh mode the output of counter U20 is applied through selector U19 to:

1) The Analog Switch, which selects the current Track and Hold amplifier to be refreshed,

   and

2) The Ram which contains the data information which will be loaded through the DAC to the Track and Hold Amplifiers.

In the Refresh mode the channel address from latch U12 is applied through selector U19 to the Analog Switches and to the Ram (see 1 and 2 above).

In the Manual mode the Host Processor must update the desired Track and Hold output with a period no greater than

$$T=(C/I_L)V_S$$

Where: T= maximum Refresh period

I_L= leakage currents at the Track and Hold capacitor (typ 5nA)

V_S= maximum permissable voltage shift for the given application

C= .0022μF, the value of the Hold capacitor

3.2.2 Programmable References

Op-Amp U40, analog switch U39, and resistors R34-36 control the reference voltage applied to the DAC U41 through R42. The latch U31 is loaded with a two-bit code which selects one of four reference levels. (10V, 5V, 2.5V, and 0V).

NOTE: At power on 0V is selected for the reference.

3.2.3 Analog Outputs

Eight analog outputs are provided by Track and Hold amplifiers composed of analog switch U43 and Quad op-amps U35 and U36. These analog outputs are offered with a considerable number of options with regards to configuration. (See A/D configuration section 6.0.)

3.3 Digital Section

The eight-bit data buses are recieved and converted to a 16-bit input by U6 through U11. These latches and buffers are controlled by PAL'S* (Programmable Array Logic) U5 and U17 and the Address Decoders U2 and U3. This structure is designed to support either 8 - or 16-bit data transfers according to the proposed IEEE-696 specification.

*PAL™ is a trademark of Monolithic Memories.

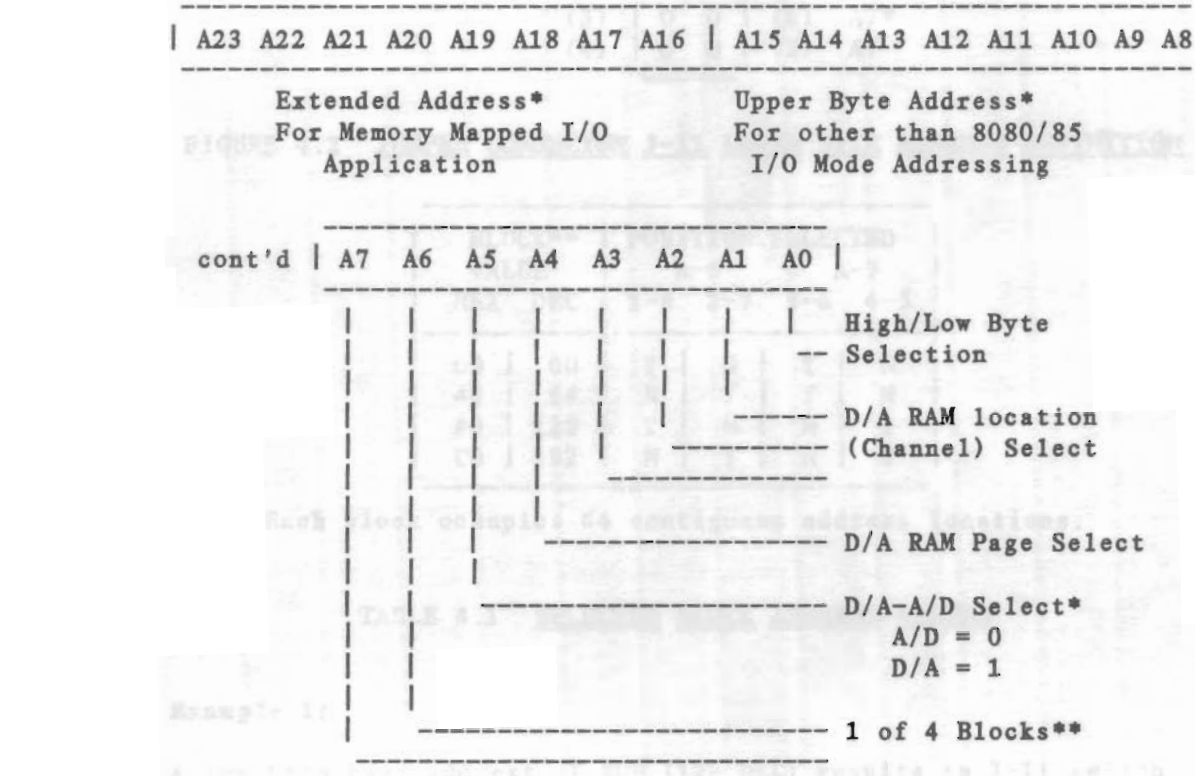
4.0 Board Configuration

The configuration process described herein should be followed in order presented in this manual. For quick look-up of specific configuration refer to the index in front of this manual.

4.1 Addressing

Addressing of the A/D/A Board is accomplished through jumper selections of an upper byte, lower byte and an extended byte address value. In addition the user may select I/O or Memory Mapped I/O operation as discussed in Section 4.2.

In order to understand the selection process described in the subsequent paragraphs refer to Figure 4.1 for clarification.



* When A/D is selected bits A3 thru A1 are don't care.
** Established thru hardware configuration using jumper connectors.

FIGURE 4.1 A/D/A ADDRESSING STRUCTURE

As can be seen in Figure 4.1 the A/D/A Board may be addressed using 8, 16 or 24 bit long address fields. The user must make the proper selections and/or deselections using the on-board jumper connectors for proper operation as described in subsequent paragraphs.

4.1.1 Lower Byte Address Selection

The lower address byte is selected using jumper connector J-11. Only address bits A7 and A6 are user selectable thus allowing the board to reside in any one of four possible address blocks. It should be noted that the upper address byte selection described in next paragraph allows for an additional 256 possible blocks/locations, providing the CPU can support such addressing modes.

Refer to Figure 4.2 for jumper connector J-11 pin definition and Table 4.1 for the corresponding block address values.

FIGURE 4.2 JUMPER CONNECTOR J-11 LOWER BYTE ADDRESS DEFINITION

BLOCK** VALUE		POSITION SELECTED			
		A-6		A-7	
HEX	DEC	1-8	2-7	3-6	4-5
00	00	Y	N	Y	N
40	64	N	Y	Y	N
80	128	Y	N	N	Y
C0	192	N	Y	N	Y

** Each block occupies 64 contiguous address locations.

TABLE 4.1 SELECTED BLOCK ADDRESS VALUES

Example 1:

A low byte base address of 80H (128 DEC) results in J-11 switch settings as shown in Figure 4.3 and occupies addresses 80H thru BFH.

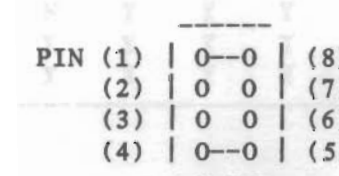


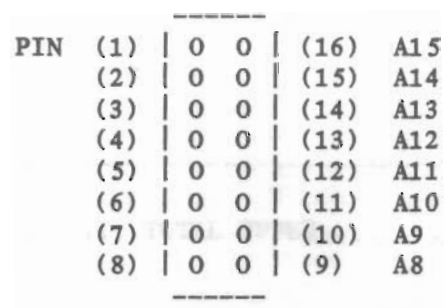
FIGURE 4.3 J-11 SAMPLE JUMPER CONFIGURATION FOR 80H/128D

4.1.2 Upper Byte Address Selection

The upper byte address selection applies only to processors that utilize more then 8-bits of address in their I/O addressing modes, i.e. non 8080/8085 processors or when using the Memory Mapped I/O mode.

Figure 4.4 defines jumper connector J-3 pin assignment and Table 4.2 defines the hex and decimal equivalents for these selections.

When this address option is not being utilized it must be disabled thru jumper connector J-4 as shown in next paragraph.



NOTE: No jumper indicates corresponding address bit as high (1).
Jumper in place indicates corresponding address bit as low (0).

FIGURE 4.4 JUMPER CONNECTOR J-3 UPPER BYTE SELECT PIN DESIGNATIONS

DECIMAL VALUE	MSB 1-16	2-15	3-14	4-13	5-12	6-11	7-10	LSB 8-9	HEX VALUE
0	Y	Y	Y	Y	Y	Y	Y	Y	0000
256	Y	Y	Y	Y	Y	Y	Y	N	0100
512	Y	Y	Y	Y	Y	Y	N	Y	0200
1024	Y	Y	Y	Y	Y	N	Y	Y	0400
2048	Y	Y	Y	Y	N	Y	Y	Y	0800
4096	Y	Y	Y	N	Y	Y	Y	Y	1000
8192	Y	Y	N	Y	Y	Y	Y	Y	2000
16,384	Y	N	Y	Y	Y	Y	Y	Y	4000
32,768	N	Y	Y	Y	Y	Y	Y	Y	8000

TABLE 4.2 UPPER ADDRESS BYTE JUMPER CONNECTOR J-3 PIN DESIGNATIONS

Example 2: A high byte base address of 8200H (33,280 DEC) results in J-3 jumper setting as shown in Figure 4.5. The jumper configuration was based on calculations shown in Table 4.3.

DECIMAL VALUE	MSB 1-16	2-15	3-14	4-13	5-12	6-11	7-10	LSB 8-9	HEX VALUE
____								Y	____
512							N		0200
____						Y			____
____					Y				____
____				Y					____
____			Y						____
____		Y							____
32,768	N								8000

33,280.....TOTAL UPPER.....8200

TABLE 4.3 **SAMPLE UPPER BYTE ADDRESS CALCULATION**

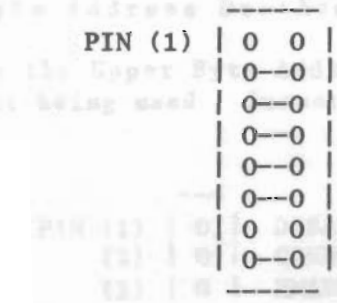


FIGURE 4.5 **J-3 SAMPLE JUMPER CONFIGURATION FOR 8200H (33,280 DEC)**

For convenience, an Upper Byte Address calculation/configuration worksheet is provided in Table 4.4.

DECIMAL VALUE	MSB 1-16 2-15 3-14 4-13 5-12 6-11 7-10 LSB 8-9	HEX VALUE
------	--	------
------	--	------
------	--	------
------	--	------
------	--	------
------	--	------
------	--	------
------	--	------
------	.....TOTAL UPPER.....	------

TABLE 4.4 **UPPER BYTE ADDRESS CALCULATION FORM**

4.1.2.1 Upper Byte Address Deselection

It is required that the Upper Byte Address selection logic be disabled if it is not being used. Jumper connector J-4 as shown in Figure 4.6 below.

```
        ___
PIN (1) | O |  DISABLE
    (2) | O |  COMMON
    (3) | O |  ENABLE
        ___
```

MAKE PROPER SELECTION TO COMMON PIN (2)

FIGURE 4.6 **JUMPER CONNECTOR J-4 UPPER ADDRESS BYTE ENABLE/DISABLE**

4.1.3 Extended Address Selection/Deselection*

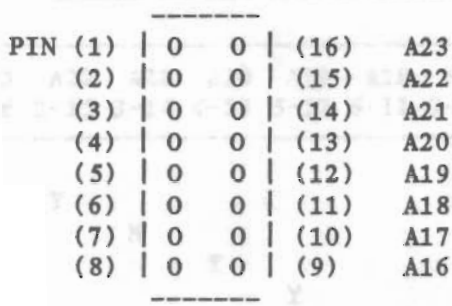
The purpose for this selection is to accommodate the extended addressing range as defined in IEEE-696 when using the Memory Mapped I/O mode. Namely, the standard 16 address lines are expanded to 24, thus allowing for greater addressing range. If your system does not support extended addressing skip to paragraph 4.1.3.2 Deselection.

*Deselection applies to most 8-bit processors, i.e., Z-80, 80/85, etc., or when operating in the I/O mode.

4.1.3.1 Extended Byte Address Selection

This addressing is accomplished via jumper connector J-1 and J-2. Figure 4.7 and Table 4.5 define the J-1 connector jumper pin-out and their corresponding magnitude designations, respectively.

J-2 provides the enable for the extended addressing and it must be enabled as shown in next paragraph.



Note: No jumper indicates corresponding address bit as high (1).
Jumper in place indicates corresponding address bit as low (0).

FIGURE 4.7 JUMPER CONNECTOR J-1 PIN DEFINITION

DEC ROW VALUE	A23 1-16	A22 2-15	A21 3-14	A20 4-13	A19 5-12	A18 6-11	A17 7-10	A16 8-9	HEX ROW VALUE
00 000	Y	Y	Y	Y	Y	Y	Y	Y	0 0000
65,536	N								1 0000
131,072		N							2 0000
262,144			N						4 0000
524,288				N					8 0000
1,048,576					N				10 0000
2,097,152						N			20 0000
4,194,304							N		40 0000
8,388,608								N	80 0000

TABLE 4.5 JUMPER CONNECTOR J-1 EXTENDED ADDRESS DEFINITION

The extended address has no effect on other jumper selections, except that it provides an extension to the already preselected upper and lower values described in previous paragraphs.

Example 3: Table 4.6 and Figure 4.8 show how the extended address range is being calculated and configured. In similar fashion, Example 1 upper and lower values could be extended using the herein described procedure.

For convenience, an extended calculation/configuration worksheet is provided as shown in Table 4.7.

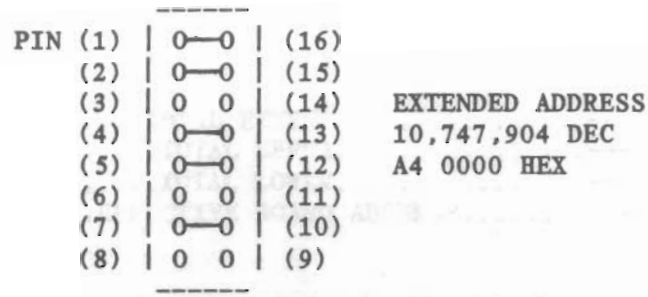


FIGURE 4.8 **SAMPLE JUMPER J-1 ADDRESS ASSIGNMENT**

DEC ROW VALUE	A23 1-16	A22 2-15	A21 3-14	A20 4-13	A19 5-12	A18 6-11	A17 7-10	A16 8-9	HEX ROW VALUE
_____	Y								_____
_____		Y							_____
262,144			N						4 0000
_____				Y					_____
_____					Y				_____
2,097,152						N			20 0000
_____							Y		_____
8,388,608								N	80 0000

10,747,904.....TOTAL EXTENDED.....A4 0000

TABLE 4.6 **SAMPLE EXTENDED ADDRESS**

DEC ROW VALUE	A23 1-16	A22 2-15	A21 3-14	A20 4-13	A19 5-12	A18 6-11	A17 7-10	A16 8-9	HEX ROW VALUE
	--								
		--							
			--						
				--					
					--				
						--			
							--		
								--	

--------.....TOTAL EXTENDED.....--------
--------.....TOTAL UPPER.....--------
--------.....TOTAL LOWER.....--------
--------.....EFFECTIVE BOARD ADDRESS.....--------

TABLE 4.7 **EXTENDED ADDRESS CALCULATION FORM**

4.1.3.2 Extended Byte Address Deselection

It is required that the extended addressing option be disabled if your system does not support extended addressing. Failure to disable this option may cause erroneous operation of the address decode logic, and thus improper operation of the board.

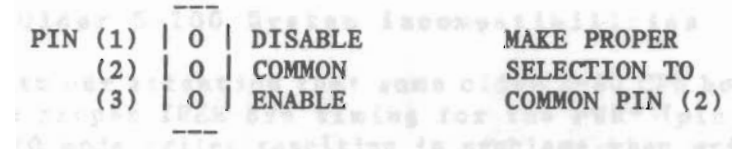


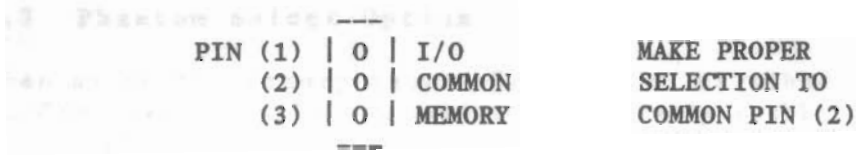
FIGURE 4.9 **EXTENDED ADDRESS DISABLE/ENABLE JUMPER CONNECTOR J-2**

4.2 Data Transfer Mode Selection

The A/D/A Board is capable of operating (i.e. transfering data to and from the board) in the I/O and/or the Memory Mapped I/O mode. The above modes are analogous to INPUT/OUTPUT AND PEEK/POKE instructions in the Basic programming language.

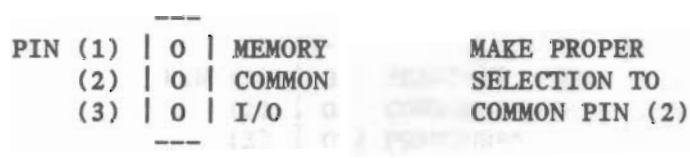
Since separate jumper connectors are provided for read and write board access selections the user may elect to use a mixed mode of operation thus allowing for Memory Mapped writes and I/O reads or vice versa.

The normal mode of operation requires that the read and write transfer modes be the same. See Figure 4.10 and 4.11 for the Read and Write jumper connector configuration selection respectively.



NOTE: To select I/O transfer mode jumper pins 1 to 2.

FIGURE 4.10 **READ MODE SELECT JUMPER CONNECTOR J-9 PIN DEFINITION**



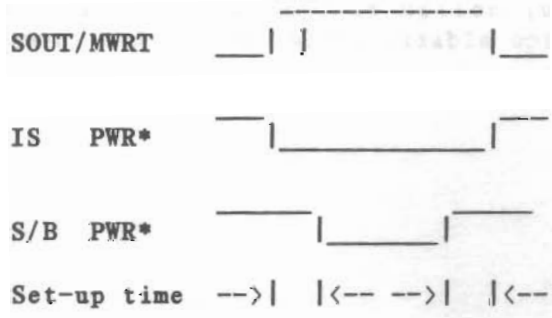
NOTE: To select I/O transfer mode jumper pins 2 to 3.

FIGURE 4.11 **WRITE MODE SELECT JUMPER CONNECTOR J-8 PIN DEFINITION**

4.2.1 Older S-100 System Incompatibilities

It came to our attention that some older Z-80 CPU boards do not generate proper IEEE-696 timing for the PWR* (pin 77) signal during I/O mode writes resulting in problems when writing to the board i.e. during D/A updates.

The problem is caused by the lack of sufficient set-up time for the PWR* signal with respect to the SOUT/MWRT status signals as shown below.



We recommend that you rectify this problem at the bus level or using one of the procedures in Section 7.8. Refer to the latest IEEE-696 specification for the required set-up times.

4.3 Phantom Select Option

When using the Memory Mapped I/O option described in 4.2 the PHANTOM signal may be utilized to selectively enable or disable the board. Refer to your operating system requirements, i.e. Power-On Bootstrap loaders, monitors, etc. Figure 4.12 defines the connector jumper configuration.

For I/O mode of operation with upper address byte enabled connect pins 3 to 2 of jumper connector J-6. Note that the PHANTOM signal is active low, i.e. when at logic 0 (0.V to .8V).
The Phantom option is disabled when the upper address byte is dis-on jumper J-4.

```
          ---
PIN (1) | O | PHANTOM*
    (2) | O | COMMON
    (3) | O | PHANTOM**
          ---
```

* Board functions disabled when PHANTOM* signal active low.
** Board functions enabled when PHANTOM* signal active low.

FIGURE 4.12 **PHANTOM POLARITY SELECT JUMPER CONNECTOR J-6 PIN DEFINITION**

4.4 DMA Operation

A DMA operation option is supported by the A/D/As select logic, i.e. the user may select the desired activity level for the PHLDA signal, thus providing for operation (1) only during DMA (2) only when not in DMA or (3) in both (at all times).

The DMA control option is disabled when the extended address is disabled on jumper J-2.

This selection is accomplished thru jumper connector J-7 as shown in Figure 4.13. To disable this option jumper pins 2 to 4 of jumper connector J-7. The above disable option connection yields operation at all times.

Jumper 1 TO 4 for operation only during DMA.
Jumper 2 TO 4 for operation at all times (normal).
Jumper 3 TO 4 only when not in DMA.

FIGURE 4.13 **DMA OPERATION SELECTION JUMPER CONNECTOR J-7 PIN DEFINITION**

4.5 16/8 Bit Operation

No jumper selections are required to operate the A/D/A Board in the IEEE-696 16-bit mode.

Selections between the 16 and 8 bit transfer modes are accomplished using bus signal SXTRQ* on pin 58 of the bus connector.

NOTE 1: BYTE MODE WRITE: When writing to the A/D/A in the Byte Mode, it is required that the high byte be written first, followed by the lower byte. To reverse this procedure you may, (1) Order custom U5 and U17 I.C., (2) Invert the A0 address line.

This should not be confused with the IEEE-696 low / high byte transfers, since it applies only to boards which do not respond to the SXTN acknowledge signal. In such cases an IEEE-696 CPU would transfer the data in a low then high byte sequence.
In our case, the A/D/A board responds with the proper 16 acknowledge sequence and will perform 16-bit data transfers.

NOTE 2: NON IEEE-696 / OLDER S-100 SYSTEM USERS. Insure that no signal is connected to the above pin 58 or improper board operation will result. Active termination i.e. pull-up is O.K., but no active low or ground can be connected to this pin.
If you are not sure, the 16 bit operation may be disabled by lifting pin 5 of ICs U5 and U17 at the I.C. socket. Do not break off the pins so that you may be able to re-activate this function.

4.6 Address Verify Indicator

To aid the user in the address configuration process, a LED (Light Emitting Diode) was placed in the D/A RAM/Channel Address circuit on-board the A/D/A. When all of the above address selections or deselections are properly installed and the correct address was output by the host processor, the LED 'Verify Indicator' will be ON or OFF depending on which channel was addressed/selected.

D/A channels 2, 3, 6 and 7 will turn the 'Verify Indicator' ON and the remaining D/A channels 0, 1, 4, 5 will turn it OFF.
A/D channel control will have no effect on the LED operation.

The Power-On state of the LED should be ignored, since no clear is being provided to the latch during that state.

Random LED illumination may occur in some systems during DMA. This is attributed to toggling control lines during DMA bus transfers (Master to Slave and/or vice versa). If this condition exists and causes problems a 'board DMA lock-out' can be easily incorporated using the provided I/O code logic. See Section 4.4 DMA Operation, except note that jumper J7 is enabled only with 16 bit address field applications. To use this option with 8-bit address fields jumper J7 pin 3 to pin 2 of one of the address disable/enable jumpers (J2 or J4).

5.0 A/D Operation

The Analog to Digital section of the A/D/A Board is controlled via software command words output to the A/D section, and by reading the converter data word when the conversion is complete. It should be noted that the A to D operation is totally independent of the D/A section. As shown in Figure 4.1, Bit 5 of the board's address word enables access to the A/D section when it is set to logic 0.

The resulting addresses for the A/D section based on the lower byte address setting shall be as shown in Table 5.0. For clarity bits A3 thru A1 (don't cares) are set to 0. Note that only bits 5-7 and 0 are used in address decoding by the A/D/A thus 8 other possible addresses (based on states of A1-A3) will write to the A/D/A and all will perform the same task. See Table 4.1.

J-11 SETTING		A/D LOWER ADDRESS BYTE*			
HEX	DEC	UPPER		LOWER	
00	(00)	01	(01)	00	(00)
40	(64)	41	(65)	40	(64)
80	(128)	81	(129)	80	(128)
C0	(192)	C1	(193)	C0	(192)

TABLE 5.0 **A/D LOWER BYTE ADDRESS FIELD FOR J-11 SELECTIONS**

The above A/D lower byte address field can be used directly providing the upper and extended address bytes are disabled and the board is operating in the I/O transfer mode.

The A/D section is operated by outputing a control word or 2 control bytes to the board's control latch.

The contents of the control word shall depend upon the functions the user has selected to be performed by the A/D converter.

5.1 A/D Control Word

Prior to start of any conversion sequence a control word must be sent to the A/D control latch specifying:

1. Channel #
2. Single or differential mode
3. Gain for the above

The lower byte portion of the control word needs to be sent each time a conversion is required, where, the upper byte needs to be sent only once.

Note, that in 16-bit operation all information must be included each time a conversion is desired.

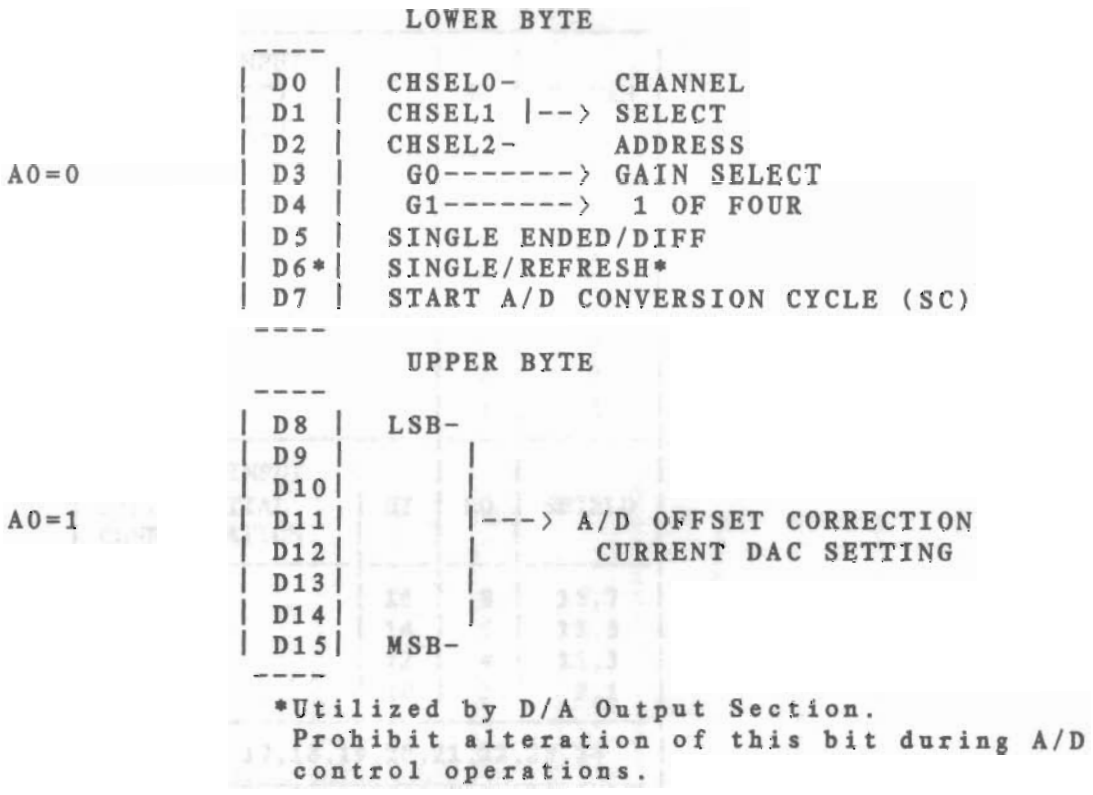


FIGURE 5.1 **CONTROL WORD BIT DEFINITION**

5.1.1 Channel Selection

The channel selection is performed by presetting the desired channel number in bit field D0-D2, see Figure 5.2.

CHSEL2	CHSEL1	CHSEL0	CHAN #
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

FIGURE 5.2 **CHANNEL ADDRESS FIELD DEFINITION**

5.1.1.1 Input Connector Pin Designation [CA]

The input signal interconnections for connector CA are as shown in Table 5.1 below.

CHANNEL INPUT SINGLE ENDED CONFIGURATION	HI	RETURN
0	16	15
1	14	13
2	12	11
3	10	9
4	8	7
5	6	5
6	4	3
7	2	1

CHANNEL INPUT DIFFERANTIAL CONFIGURATION	HI	LO	SHIELD
0	16	8	15,7
1	14	6	13,5
2	12	4	11,3
3	10	2	9,1

GROUND 17,18,19,20,21,22,23,24
+12 VDC 25,26

TABLE 5.1 INPUT CONNECTOR [CA] PIN DEFINITION

5.1.2 Single Ended/Differential Selection

The respective (D5) bit must be set as follows:

0 = Single ended operation (8 channel)
1 = Differential operation (4 channel)

See Figure 5.1.

5.1.3 Gain Selection

Any 1 of 4 gain levels may be selected for a channel. The standard gain levels provided by the A/D/A Boards are controlled by bit D3 and D4 of the control word (see Figure 5.1) and are as shown in Figure 5.3.

D4 G1	D3 G0	GAIN LEVEL
0	0	X .5
0	1	X 2
1	0	X 8
1	1	X 32

FIGURE 5.3 **GAIN LEVEL FIELD DEFINITION**

5.1.4 Input Level Restrictions vs. Gain

The maximum signal level which may be accurately converted by the A/D section is $V_{IN}(Max.) = 5V/Gain$.

Example 1: An input signal with $\pm$.6V max is to be sampled.

The following gain loops are available:

$\pm$.6V x 0.5 = $\pm$ 0.3V O.K
$\pm$.6V x 2 = $\pm$ 1.2V O.K.
$\pm$.6V x 8 = $\pm$ 4.8V O.K.
$\pm$.6V x 32 = $\pm$19.2V NOT ALLOWED

Since best data conversion with most resolution steps is achieved when the max. input signal level is equal to the max input level of the DAC the user should take this into consideration especially when external buffers with gain are available on the input signal lines.

For applications which require gains other then the above, a customization procedure is provided in Section 7.

5.1.5 Start Conversion Command

The Start Conversion (SC) command is issued by the user when a conversion is desired. The SC command is generated by writing a logic 1 into bit position D7 of the control word. (See Figure 5.1). When the conversion is completed (12 microseconds later) an interrupt is generated and the conversion complete (CC) bit of the A/D Conversion Data Word (see Figure 5.4) is set.

After detection of CC a new SC command may be issued before reading of the lower byte result (A0=0). Note that if the lower byte is not read within next 11 microseconds, the result will be destroyed by the upcoming conversion result.

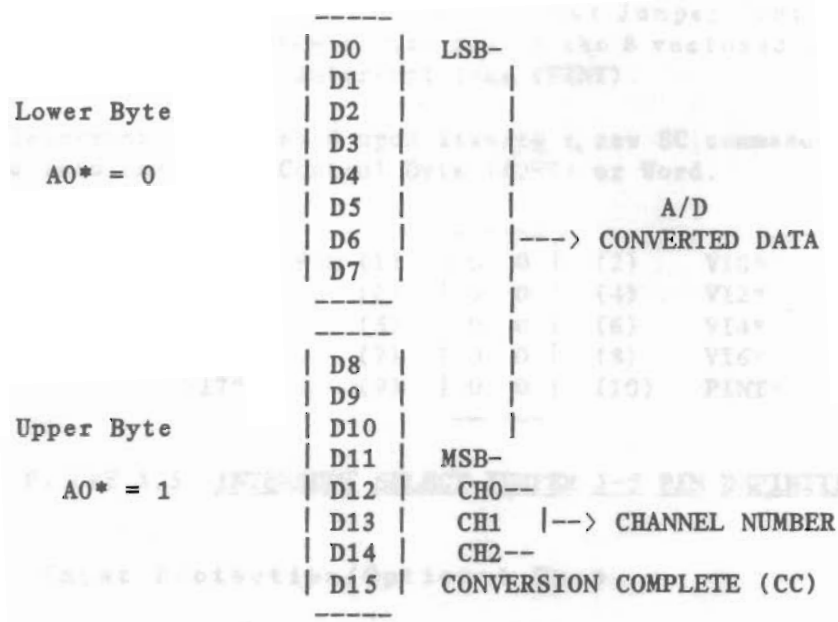
As long as a logic 1 is present in bit position D7 of the control word and a write is being performed to the control word another conversion cycle will be initiated. When changing channels or

gain loops, the SC bit should be reset (0). This step will provide sufficient settling time in the gain and multiplexer stages. Alternate approach is to change channels with the SC bit set and discard the first reading after each change (code efficient).

5.1.6 Conversion Data Word Read

For the following discussion, refer to Figure 5.4., Conversion Data Bit Pattern. In addition to the 12 bits of converted data the A/D/A Board places four additional bits of information in the remaining bits of the 16-bit word or the upper byte (1st read byte). Namely, channel number consisting of a three bit field and the CC status bit.

The encoded channel number is useful in data reduction processing.



* A0 - Significant during byte read operations, don't care when 16-bit read is performed.

FIGURE 5.4 A/D CONVERSION DATA WORD BIT PATTERN

During Status polled operation the user need to read only the lower byte and check for the condition of the CC bit, i.e. when 0 the A/D converter is in process when 1 the conversion is complete and valid data word may be read.

5.1.7.1 Conversion Complete

As described in previous paragraph bit D15 of the converted data word contains the CC status bit.

The CC status bit or the CC interrupt serves as A/D Status indication to the system. Upon receipt of any one of the above two indicators the converted data may be read by the CPU. Sixteen bit systems perform a single read where 8 bit systems perform a double byte read. The A/D/A read logic has been designed in such a way that the user may read the data continuously, i.e. monitor the CC status bit setting during polled operation (not in interrupt driven systems).

5.1.7.2 Conversion Complete Interrupt

Another approach is to utilize the CC interrupt option of the A/D/A Board.

The CC interrupt is provided on pin 1 of the J-5 jumper connector as shown in Figure 5.5, Interrupt Select Jumper Configuration. The user has the option to use one of the 8 vectored interrupts or the main processor interrupt line (PINT).

The interrupt is released upon issuing a new SC command or by any write into the Lower Control Byte (A0=0) or Word.

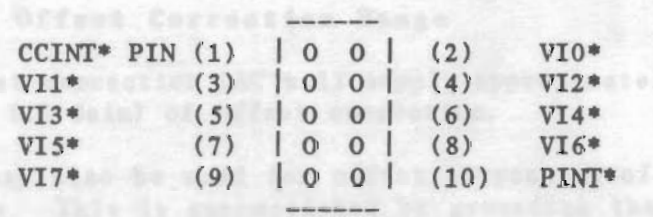


FIGURE 5.5 INTERRUPT SELECT JUMPER J-5 PIN DEFINITION

5.2 Input Protection/Optional Fuse

See Section 3.1.1, Input Protection Network. The user may at his option cut the thin etch between the pads marked F1-F8 and install fuses if his application so warrants.

The following is a list of subminiature Pig-Tail fuses made by Bussman Manufacturing Division which may be installed in component positions F1 thru F8:

BUSS # GLN, 1/100 A
GFA, 1/100 A

The above fuses are available from I/O TECHNOLOGY. Call for price and delivery.

5.3 Current Input Option

The A/D input channels may be configured by the user to accept unipolar current input, such as from popular industrial Unipolar

current output generating equipment/sources.

Namely, each of the 8 input channels contains a place for a terminating (load or sink) resistor. These resistors are R4 thru R11 for channels 0 thru 7 respectively.

The only consideration for the size of the resistor is that it handle the load dissipation and that the voltage across the resistor does not exceed 10V.

5.4 A/D Offset Voltage Nulling

The A/D/A has incorporated a programmable offset voltage correction circuit using a dedicated 8-bit D/A circuit. This dedicated circuit injects current under Program Control into the Summing Junctions of the input op-amps thus eliminating offset errors.

The procedure for offset voltage nulling is as shown in flowchart of Figure 5.7, Auto-Zero Procedure. Software subroutine Auto-Zero listed in Section 8.0 performs these steps.

5.4.1 Input Offset Correction Range

The input offset correction DAC will supply approximately 40 mV (Full Scale at 0.5 Gain) of offset correction.

This feature may also be used for offset correction of external Buffers/OP-Amps. This is accomplished by grounding the input(s) of the external devices and executing the Auto-Zero sub-routine.

When using the input offset correction at large gains, it may be necessary to increase the value of R39 to obtain smaller incremental steps for the offset correction.

A 2 to 4 MΩ resistor will work fine at higher gains but may not provide sufficient correction at gain of .5, or if you are using this feature to correct large source and cable loss errors.

Due to the low DAC reference level necessary to obtain this small full scale, the Offset Correction DAC's settling time is affected (approx. 25 µsec.). This must be taken into consideration when switching between channels of different gains which may require different offset correction values. On the other hand, the above will not be a factor when switching between channels of same gain or same offset correction level.

5.5 Data Field Input Level Conversion

To convert the 12-bit binary data word to a floating point decimal value refer to Table 5.2, A/D Data Field Definition. In addition the specific channel gain levels must be known (multiplication factor) in order to make the proper conversion.

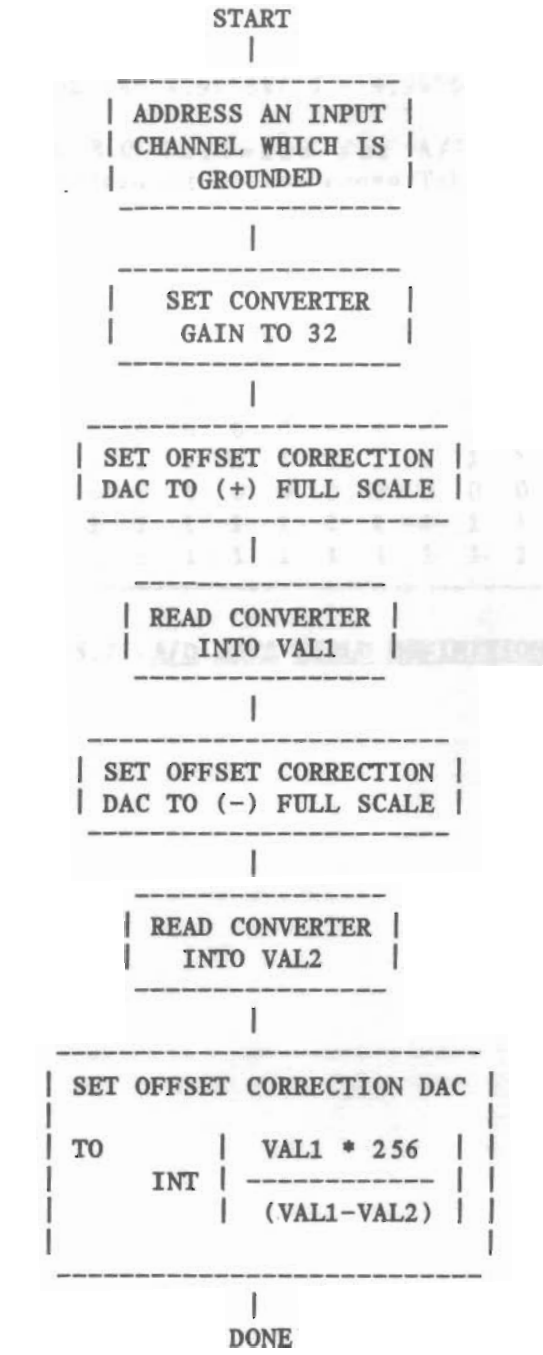


FIGURE 5.7 **AUTO ZERO PROCEDURE**

Example 1: Assume a gain of .5 was set on channel 1 and the 12 bit data field read all is (FFFH).

The actual input then was 4.9988V/.5 = 9.9976V.

Refer to Section 8.0 Software for A/D data conversion algorithm/programs according to the above Table 5.2.

OUTPUT SCALE	MSB 11	10	9	8	7	6	5	4	3	2	1	LSB 0	OUTPUT VOLTAGE
+FULL SCALE	1	0	0	0	0	0	0	0	0	0	0	0	+4.9988
+FULL-LSB	1	0	0	0	0	0	0	0	0	0	0	1	+4.9964
+ZERO	1	1	1	1	1	1	1	1	1	1	1	1	+0.0012
-ZERO	0	0	0	0	0	0	0	0	0	0	0	0	-0.0012
-FULL-LSB	0	1	1	1	1	1	1	1	1	1	1	0	-4.9964
-FULL SCALE	0	1	1	1	1	1	1	1	1	1	1	1	-4.9988

TABLE 5.2 **A/D DATA FIELD DEFINITION**

6.0 D/A Section Operation

The D/A circuitry of the A/D/A Board operates independently of the A/D circuitry described in the previous section.

The following paragraphs shall sequentially describe the operation and the required set-up procedures for the A/D Section.

6.1 Voltage/Current Output Selection

Before using the board's D/A Section the user must select the type of output desired for each of the channels. Jumper connectors J-13, J-14 and J-16 are used to make the proper output type selections.

In addition jumper connectors J-15 and J-17 are provided to supplement the current output options on each channel. It should be noted that no restrictions exist on which channel can be current or voltage.

Before making any selections, see Figure 6.1, Jumper Connector J-13 thru J-17 Pin Orientation.

A summary of jumper selections for voltage and output options is listed in Table 6.1.

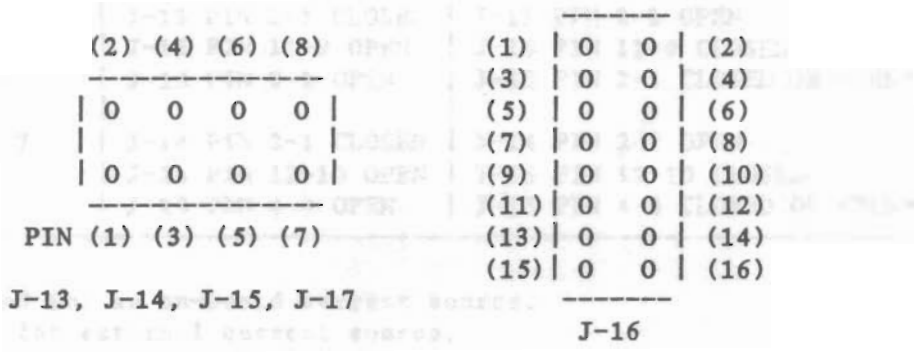


FIGURE 6.1 **JUMPER CONNECTOR J-13 THRU J-17 PIN ORIENTATION**

CHAN. #	VOLTAGE OUTPUT	CURRENT OUTPUT
0	J-14 PIN 8-7 CLOSED	J-14 PIN 8-7 OPEN
	J-16 PIN 4-2 OPEN	J-16 PIN 4-2 CLOSED
	J-17 PIN 4-3 OPEN	J-17 PIN 4-3 CLOSED OR OPEN*
1	J-13 PIN 8-7 CLOSED	J-13 PIN 8-7 OPEN
	J-16 PIN 15-13 OPEN	J-16 PIN 15-13 CLOSED
	J-15 PIN 6-5 OPEN	J-15 PIN 6-5 CLOSED OR OPEN*
2	J-14 PIN 6-5 CLOSED	J-14 PIN 6-5 OPEN
	J-16 PIN 8-6 OPEN	J-16 PIN 8-6 CLOSED
	J-17 PIN 6-5 OPEN	J-17 PIN 6-5 CLOSED OR OPEN*
3	J-13 PIN 6-5 CLOSED	J-13 PIN 6-5 OPEN
	J-16 PIN 7-5 OPEN	J-16 PIN 7-5 CLOSED
	J-15 PIN 8-7 OPEN	J-15 PIN 8-7 CLOSED OR OPEN*
4	J-14 PIN 4-3 CLOSED	J-14 PIN 4-3 OPEN
	J-16 PIN 16-14 OPEN	J-16 PIN 16-14 CLOSED
	J-17 PIN 8-7 OPEN	J-17 PIN 8-7 CLOSED OR OPEN*
5	J-13 PIN 4-3 CLOSED	J-13 PIN 4-3 OPEN
	J-16 PIN 16-14 OPEN	J-16 PIN 16-14 CLOSED
	J-17 PIN 8-7 OPEN	J-17 PIN 8-7 CLOSED OR OPEN*
6	J-13 PIN 2-1 CLOSED	J-13 PIN 2-1 OPEN
	J-16 PIN 11-9 OPEN	J-16 PIN 11-9 CLOSED
	J-15 PIN 2-1 OPEN	J-15 PIN 2-1 CLOSED OR OPEN*
7	J-14 PIN 2-1 CLOSED	J-14 PIN 2-1 OPEN
	J-16 PIN 12-10 OPEN	J-16 PIN 12-10 CLOSED
	J-15 PIN 4-3 OPEN	J-15 PIN 4-3 CLOSED OR OPEN*

* Closed for an on-board current source.
  Open for external current source.

TABLE 6.1 **D/A VOLTAGE/CURRENT CONFIGURATION FOR JUMPER CONNECTORS J13, J14, J15, J16 AND J17.**

6.2 Power-On Condition

When power is first applied to the host system the POC (Power-On-Clear) signals is used by the A/D/A Board's initialization circuitry which sets all of the 8 D/A output channels to '0'.

This condition shall persist as long as the board is not addressed. A single write command into the command latch will enable the channel refresh mode from the RAM designated values. This condition allows for the user to preset all of the 8 channel output levels in the on-board Dual-ported RAM prior to removing

the 0V power-on condition (since the RAM normally contains random values after power-on).
The method of presetting the desired channel output levels will be discussed separately in Section 6.

The power-on condition should not be confused with the RESET condition, such as from a RESET pushbutton or front panel reset. Once the RAM values have been output into the channels, a reset will not alter the output levels.

The POC is normally applied when power is first applied to the computer/CPU.

6.3 RAM Location Vs. Channel Allocation

The on-board dual-ported RAM contains two pages of 8 channel data words. Only one page is being sequenced thru at a time. The user must make the appropriate software command to change the page(s).

Address Bit A4 is used by the A/D/A Board as the page steering bit, i.e. if last written value had its address bit A4=0, then the data from page 0 will be used for output conversion and vise versa.

Table 6.2 shows the relation between the channels and their corresponding RAM locations, i.e. to change channel 1 output level from existing level, the user outputs a word (2 bytes) to the corresponding RAM location.

CHANNEL #	RAM ADDRESS A3	A2	A1	PAGE 0 A4=0	PAGE 1 A4=1
0	0	0	0	12 BIT DATA	12 BIT DATA
1	0	0	1	"	"
2	0	1	0	"	"
3	0	1	1	"	"
4	1	0	0	"	"
5	1	0	1	"	"
6	1	1	0	"	"
7	1	1	1	"	"

TABLE 6.2 RAM/CHANNEL DATA ADDRESS ALLOCATION

6.3.1 Output Connector Pin Designations

The following Table 6.3 lists the corresponding output pins for each of the voltage and current output channels.

CHANNEL #	VOLTAGE HIGH	VOLTAGE RTN*	CURRENT HIGH	CURRENT RTN**
0	16	15	33	34
1	29	30	31	32
2	18	17	11	12
3	27	28	19	20
4	7	8	13	14
5	24	23	9	10
6	5	6	3	4
7	22	21	25	26

* Uses On-Board Analog GND.
** Uses current source line.

TABLE 6.3 **D/A CONNECTOR CB PIN DESIGNATIONS**

6.4 Refresh Vs. Single Channel Operation

The D/A channel operation allows for two types of updating the 8 on-board sample and hold circuits.

As described in paragraph 6.1 during power-on all channels are preset to 0 and held there in the Auto Refresh mode (the default condition). In the Automatic Refresh mode the 8 sample/hold amplifiers are sequentially loaded from the selected Page of Ram. In the single channel operation the user controls the refresh rate by sequencing the corresponding channel addresses under software control. A logic 1 in bit position D6 of the command word will enable the single channel operation. Such channel control may be required for applications where maximum waveform control is desired.

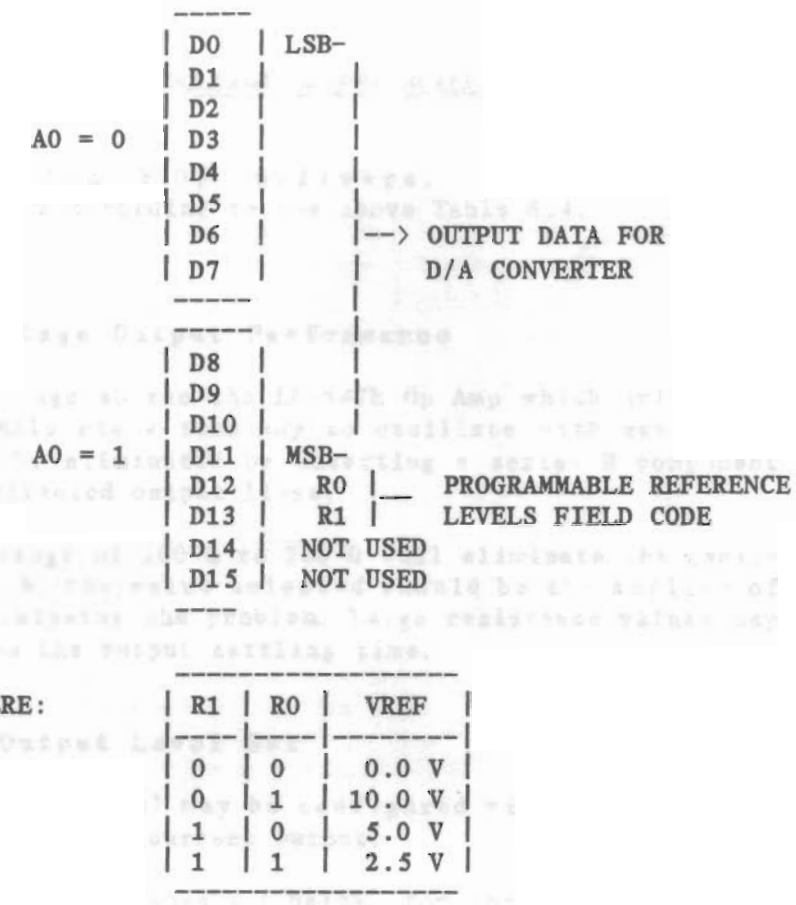
A logic 0 in bit position D6 of the command word will invoke the 8 channel automatic Refresh operation. See Figure 5.1, Control Word Bit Definition.

When operating in the Refresh mode, each output line will contain digital noise that may or may not have to be filtered depending on the application. The noise is constant and of low duty cycle and it is generated by the multiplexer (U-42) as the channels are being switched on and off. In most applications, such as audio, meter movements and mechanical devices this noise is easily tolerable and normally does not have to be filtered. For applications that can not tolerate this noise a simple low pass filter can be constructed (see section 11.0 Fig. 11.2 Low Pass Filter) using a minimum number of components.

6.5 Programmable Reference Levels

The maximum D/A analog output levels may be preset to ±10.V, ±5.0V and ±2.5V under software control. Note that each reduction in reference level provides a corresponding reduction in the bit weight for maximum output level resolution.

These programmable reference levels are set by outputting the corresponding field code in bit positions D12 and D13 of the channel output word. See Figure 6.2, D/A Output Word Bit Definition, for specific field bit code assignments.



WHERE:

R1	R0	VREF
0	0	0.0 V
0	1	10.0 V
1	0	5.0 V
1	1	2.5 V

FIGURE 6.2 D/A OUTPUT WORD BIT DEFINITION

6.6 Voltage Output Level Set

In order to obtain the proper output voltage level, the user must convert desired level into inverse offset binary.
It should be noted that the D/A design generates a symetrical voltage about zero. Refer to Table 6.4, Voltage Output Scale, for corresponding LSB/Max. value definitions at three different voltage reference levels. Note: when comparing the above table to manufacturers specifications, note that the on-board RAM has inverted outputs.

OUTPUT SCALE	MSB BIT POSITION* LSB 11 10 9 8 7 6 5 4 3 2 1 0	REFERENCE VOLTAGE 10V	5V	2.5V
+FULL	0 0 0 0 0 0 0 0 0 0 0 0	+9.9976	+4.9988	+2.4994
+FULL-LSB	0 0 0 0 0 0 0 0 0 0 0 1	+9.9927	+4.9964	+2.4982
+ZERO	0 1 1 1 1 1 1 1 1 1 1 1	+0.0024	+0.0012	+0.0006
-ZERO	1 0 0 0 0 0 0 0 0 0 0 0	-0.0024	-0.0012	-0.0006
-FULL-LSB	1 1 1 1 1 1 1 1 1 1 1 0	-9.9927	-4.9964	-2.4982
-FULL	1 1 1 1 1 1 1 1 1 1 1 1	-9.9976	-4.9988	-2.4994

*Signifies input to the RAM.

TABLE 6.4 **BIPOLAR VOLTAGE OUTPUT SCALE DEFINITION**

Refer to Section 8.0, Software, for conversion algorithms/programs according to the above Table 6.4.

6.6.1 D/A Voltage Output Performance

When used as voltage source the LF-347B Op Amp which drives the D/A output channels has a tendency to oscillate with capacitive loads. This can be eliminated by inserting a series R component in each of the effected output lines.

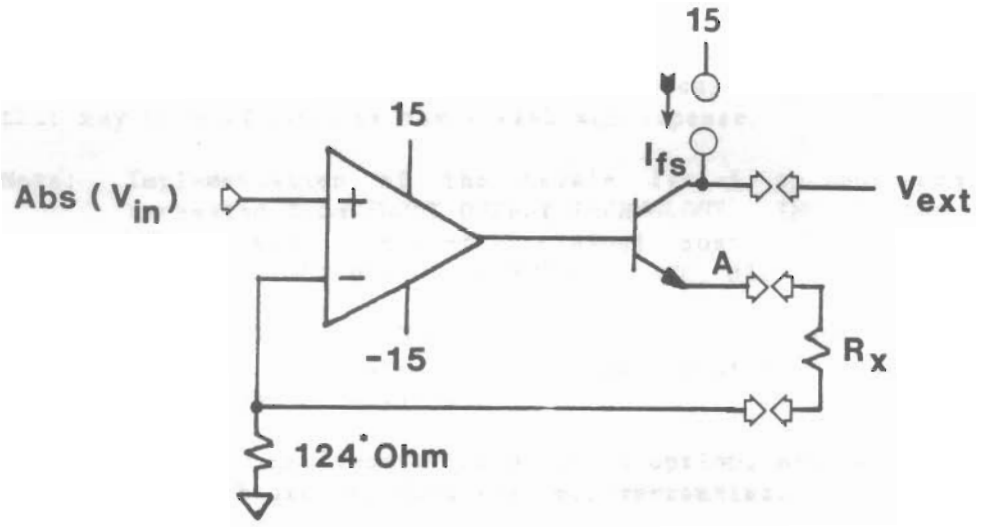
A value in the range of 100 Ω to 700 Ω will eliminate the oscillations. Although, the value selected should be the smaller of values which eliminates the problem. Large resistance values may have an effect on the output settling time.

6.7 Current Output Level Set

The D/A output channel(s) may be configured via simple jumper connections for unipolar current output.

Refer to Table 6.1 and Figure 6.3 below for the required jumper connections.

For the following discussion refer to the electrical diagram shown in Figure 6.3, Typical Current Output Configuration.



* One of R45 thru R52

FIGURE 6.3 **CURRENT OUTPUT CONFIGURATION**

The following equations represent calculations for determination of the Max. load resistor Rx at three full scale current levels.

$$V_A = I_{FS} * (124\Omega + R_X)$$

V_A max. = 10V

Therefore :

R_X max. for I_{FS} of 20mA is

$R_X = V_A$ max./20 mA - 124Ω

= 376Ω

R_X max. for I_{FS} of 40mA is

R_X max. = (10V/40mA) - 124Ω

= 126Ω

R_X max. for I_{FS} of 80 mA is

R_X max. = (10V/80mA) - 124Ω

= 1Ω

7.0 Customizing the A/D/A Board

The following paragraphs shall describe customizing procedures that may be performed at users risk and expense.

Note: Implementation of the herein listed options can be requested from INPUT/OUTPUT TECHNOLOGY, INC. by the original buyers only at a minimal cost. For specifics contact INPUT/OUTPUT TECHNOLOGY, INC. directly.

INPUT/OUTPUT TECHNOLOGY, INC. does not guarantee any performance characteristics for any of the below listed customization options.

Improper implementation of these options may cause damage to the board and thus void all warranties.

The user shall restore the A/D/A Board to the original factory configuration prior any in or out-of-warranty repair service can be rendered by INPUT/OUTPUT TECHNOLOGY INC.

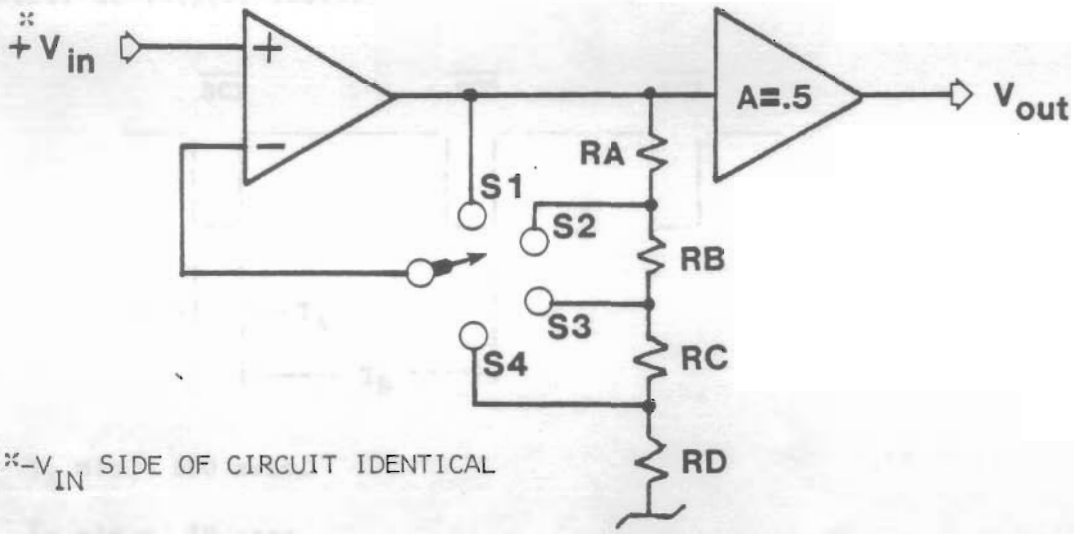
7.1 Customizing the Gain Network

If gain loop values other than those provided on the standard A/D/A Board are requried, the user may modify the gain loop network to achieve other gain values. Extreme caution should be exercised when removing the old resistors or the board may be permanently damaged.

A list of resistor values is provided in Table 7.1 to achieve the specified gain values. It should be noted that the gain loop, especially in the differential mode, requires that the resistors be balanced preferably to .1%.
For applications which require different gain levels, the user may develop his own set of resistor values per the schematic diagram and list of corresponding equations for the A/D gain network shown in Figure 7.1.

R17, R22	R16, R21	R19 || R15	R20, R14	R12 || R13 || R12	GAIN VALUES
89199Ω	8.91KΩ	891Ω		200Ω	500, 50, 5, .5
190KΩ	9KΩ	900Ω		200Ω	1000, 100, 10, .5

TABLE 7.1 CUSTOM GAIN LOOP VALUES



G(S1) = .5

G(S2) = .5{1+2[RA/(2RB+2RC+RD)]}

G(S3) = .5{1+2[(RA+RB)/(2RC+RD)]}

G(S4) = .5{1+2[(RA+RB+RC)/RD]}

WHERE: RA = R17, R22
RB = R16, R21
RC = R19||R20, R15||R14
RD = R12||R13||R18

VOUT = $-[V_{IN} * G(S)]$
VOUT = ± 5 V MAX

FIGURE 7.1 A/D GAIN NETWORK EQUATIONS

7.2 External SC Trigger Source Generation

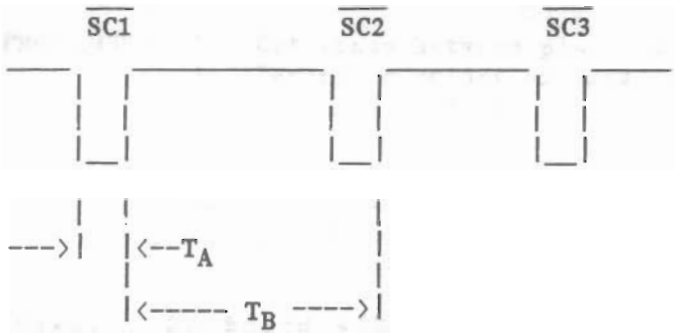
As described in 5.1.4, the SC signal and its resulting SC trigger source must be generated by the host system software. In actuality the SC trigger is the write strobe's (positive) edge for the command latch.

Some applications may require continuous sampling, i.e. 100 samples per channel and so on.

The user may therefore supply an external SC signal trigger source and connect it directly to the input of the SC command synchronizing network (U15-pin 11) thus generating automatic multiple SC signals. Operation in interrupt driven configuration for the CC signal is now required since the resulting SC commands are asynchronous with the system software commands.

The SC trigger source signal shall meet the minimum timing requirements specified in Figure 7.2, External SC Timing Requirements.
In this mode of operation the user still has full control over

the A/D conversions by controlling the SC control bit (D15), i.e. when low the conversions will be inhibited, when high the conversions will take place after each rising edge of the external SC trigger source.



T_A min = 500 nsec.

T_B min = 20 µsec.

FIGURE 7.2 **EXTERNAL SC CLOCK SIGNAL TIMING REQUIREMENTS**

7.3 Reduce A/D Conversion Time Thru an External Clock

The A/D/A Board A/D conversion clock frequency of 1 MHz is developed from the system's 2 MHz signal available on pin 49 of the bus connector.

The above 1 µsec. clock period will yield the specified 12 µsec. conversion time. Faster conversion time may be achieved by providing an external clock source for the A/D converter clock. Since the maximum clock frequency is a function of several on-board components, operating environment and configuration the max. clock frequency must be developed by the user on a trail and error basis for best results (keep in mind that the DAC Min. conversion time is 250 nsec.).

The external clock source should be connected to jumper connector J-18 as shown in Figure 7.3, External A/D Clock Source Configuration.

The only requirements for the external A/D clock source is that it be:

1. TTL level
2. Referenced to A/D/A digital ground at the 5V regulator or at pins 99 and 100 of the bus connector.

PROCEDURE:
1. Cut trace between pins 2-3.
2. Jumper or solder external clock source to pin 2 of J-18.

FIGURE 7.3 **JUMPER CONNECTOR J-18, EXTERNAL A/D CLOCK SOURCE CONFIGURATION**

7.3.1 Alternate On-Board A/D Clock Source

As shown in Figure 7.3 above, J-18 pin 1 has a 500 KHz clock source.

If conversion time of 12 µsec. is not desirable, i.e. rather a slower conversion time of 24 µsec. is sufficient, then the jumper connector may be configured to provide this option.

PROCEDURE:
1. Cut connecting trace between pins 2 and 3 of J-18.
2. Jumper or solder pins 1 to 2 of J-18.

7.4 Unipolar Voltage Input Option

If a unipolar voltage input is desired, the user may modify the A/D circuitry to provide for such input characteristics to the converter.

Unipolar operations requires appropriate changes to the data conversion algorithm of Section 8.0 presently written for bipolar input levels. Refer to Table 7.2, Unipolar Input Voltage Scale Definition.

The Auto-Zero algorithm of Figure 5.7 will not work in the Unipolar Mode.

A simple Auto-Zero routine may be accomplished by stepping the offset correction DAC thru its full range at an increment of 1 LSB and recording the DAC value which yields the best zero A/D input result.

OUTPUT SCALE	MSB 11	10	9	8	7	6	5	4	3	2	1	LSB 0	INPUT VOLTAGE
FULL	1	0	0	0	0	0	0	0	0	0	0	0	4.9988
FULL-LSB	1	0	0	0	0	0	0	0	0	0	0	1	4.9975
LSB	0	1	1	1	1	1	1	1	1	1	1	0	0.0012
ZERO	0	1	1	1	**1**	**1**	1	1	1	1	**1**	1	0.0000

TABLE 7.2 **UNIPOLAR INPUT VOLTAGE SCALE DEFINITION**

7.4.1 Unipolar A/D Input Hardware Modifications

A selection jumper is provided on the solder side of the board to select between Bipolar and Unipolar input mode.
The jumper connections are located directly under U27 on the solder side of the board. This jumper is factory configured for Bipolar input mode as shown in Fig.7.3A below.

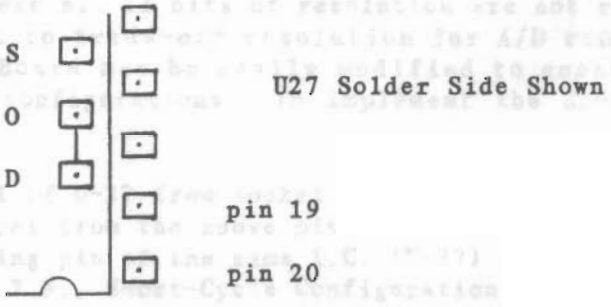


FIGURE 7.3A **BIPOLAR/UNIPOLAR INPUT JUMPER SELECTION**

To implement the unipolar input mode of operation perform the following steps:

1. Cut the short trace between pads O and D
2. Solder short jumper from pads O to S

7.4.2 Unipolar Input Data Reduction Improvement

When operating in the optional Unipolar mode, a significant reduction in the number of software steps required to obtain the final binary value can be obtained by incorporating the following hardware modifications:

1. Lift U28 pin 23 from socket and re-insert I.C. in it's socket.

2. On solder side of the board solder a short jumper from U28 pin 21 to U28 pin 23.

The resulting data will read from the A/D/A board as shown in TABLE 7.2A below.

OUTPUT SCALE	MSB 11	10	9	8	7	6	5	4	3	2	1	LSB 0	INPUT VOLTAGE
FULL	0	0	0	0	0	0	0	0	0	0	0	0	4.9988
FULL-LSB	0	0	0	0	0	0	0	0	0	0	0	1	4.9975
LSB	1	1	1	1	1	1	1	1	1	1	1	0	0.0012
ZERO	1	1	1	1	1	1	1	1	1	1	1	1	0.0000

TABLE 7.2A **MODIFIED UNIPOLAR INPUT VOLTAGE SCALE DEFINITION**

7.5 Reduce A/D Conversion Time by Reduction in Resolution (Short Cycling)

In applications where all 12 bits of resolution are not required, the user may elect to trade-off resolution for A/D conversion time. The A/D/A Board may be easily modified to accommodate lesser resolution configurations. To implement the Short-Cycle option:

1. Lift pin 1 of U-27 from socket.
2. Place jumper from the above pin 1 to the corresonding pin of the same I.C. (U-27) per Table 7.3., Short-Cycle Configuration.
3. Make jumper as short as possible.

RESOLUTION BITS	CONV. TIME* µSEC.	JUMPER TO PIN
11	11	11
10	10	10
9	9	9
8	8	8
7	7	7
6	6	6
5	5	5
4	4	4

*Based on 1MHz on-board source.
Also, see Paragraph 7.3.

TABLE 7.3 **SHORT CYCLE CONFIGURATIONP**

7.6 Increase D/A Channel Refresh Rate

The standard 500 KHz refresh rate generated for the RAM and analog MUX addressing is developed from the 2 MHz bus signal provided on pin 49 of the bus connector. The 500 KHz rate is further divided by two resulting in an actual analog output channel mux rate of 250 KHz.

If faster channel Refresh Rate is required the user may increase the channel Refresh Rate by providing an external D/A clock source.

The exact frequency can only be determined by the user application on a trial by error basis.

In order to supply an external D/A clock signal source, the clock must meet the following restrictions:

1. TTL level.
2. Signal must be referenced to A/D/A's logic ground (see paragraph 7.3).

To connect the external clock source, see Figure 7.4 below.

PROCEDURE:
1. Cut trace between pin 1 and 2.
2. Jumper or solder external clock source to pin 2 of J-19.

FIGURE 7.4 **JUMPER CONNECTOR J-19 EXTERNAL D/A CLOCK SOURCE CONFIGURATION**

7.7 Unipolar D/A Voltage Output

If a unipolar voltage output is desired, the user may modify the D/A circuitry to provide such output characteristics. Unipolar operation requires appropriate changes to the data conversion algorithm presently designed for bipolar operation. See Table 7.4, Unipolar Voltage Scale Definition.

OUTPUT SCALE	MSB 11	10	9	8	7	6	5	4	3	2	1	LSB 0	OUTPUT VOLTAGE 10V	5V	2.5V
+FULL	0	0	0	0	0	0	0	0	0	0	0	0	9.9976	4.9988	2.4994
+FULL-LSB	0	0	0	0	0	0	0	0	0	0	0	1	9.9951	4.9975	2.4981
LSB	1	1	1	1	1	1	1	1	1	1	1	0	0.0024	0.0012	0.0006
ZERO	1	1	1	1	1	1	1	1	1	1	1	1	0.0000	0.0000	0.0000

*Represents input logic level to the RAM.

TABLE 7.4 UNIPOLAR OUTPUT VOLTAGE SCALE DEFINITION

7.7.1 Unipolar D/A Output Hardware Modification

To implement the unipolar output option the following steps must be performed:

1. Short resistors R43 and R44
   OR, remove R43 and R44 and solder shorting wires in place.
2. Cut trace between R43 and R44 and CR20 as shown in Figure 7.5.
3. Solder in jumper as shown in Figure 7.5.
4. Remove resistor R41.

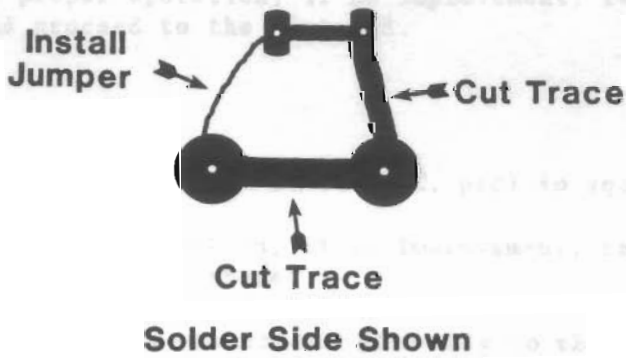


FIGURE 7.5 TRACE CUT AND JUMPER INSTALLATION FOR UNIPOLAR OUTPUT VOLTAGE OPTION

7.8 Pal I.C. Update (U5-4)

This updated version of the U5 Programmable Array Logic Device (PAL) contains two optional circuits that can be used with processor boards that do not have proper IEEE-696 timing or if you have experienced problems using the board in the memory mapped address mode.

The problem occurs mostly during writes to the D/A channels when in refresh mode, causing improper channel output levels.

The modified PAL contains the following features:

MOD. A. A circuit for generating new PWR* signal:

PWR* = PWR*(pin 77) + ϕ (pin 24)

MOD. B. Same as above except uses different phase of the clock

PWR* = PWR*(pin 77) + $\overline{\phi}$ (pin 24)

To eliminate the above problem select the U5 circuit options as described below.

MOD. A:

-On solder side of board cut short trace between square pads 'T' and 'V' (located between U6 and U7).
-Solder jumper from U5 pin 15 which is connected to the square pad 'P' (under U6) to square pad 'V'.

-Check for proper operation, if no improvement, remove above jumper and proceed to the next mod.

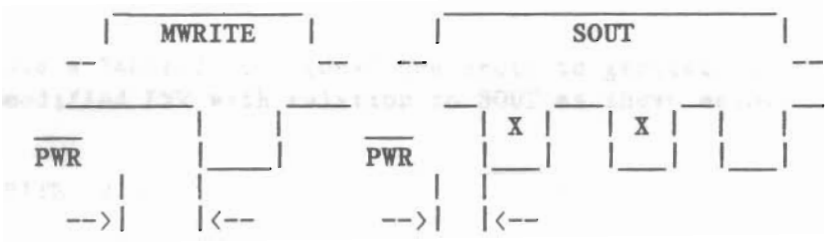
MOD. B:

-Solder jumper from U5 pin 14 (at I.C. pad) to square pad 'V'.

-Check for proper operation, if no improvement, remove above jumpers and reconnect trace.

DO NOT solder any connections directly to the S-100 connector finger.

The resulting waveforms for the above mods are as shown below:



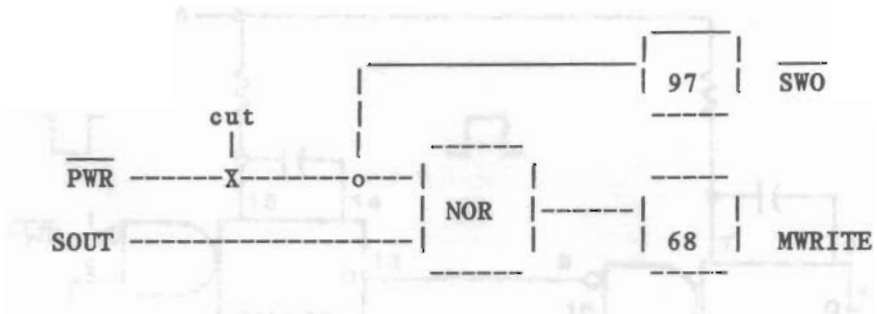
The following is a list of modifications, which were given to us by users that have experienced this problem.

I. Software MOD

1. Send Hi-byte with previous channel's Hi-byte data.
2. Send Hi-byte with current channel's data.
3. Send Lo-byte with current channel's data.

Comment: Requires additional software processing which may or may not be afforded with slow processors.

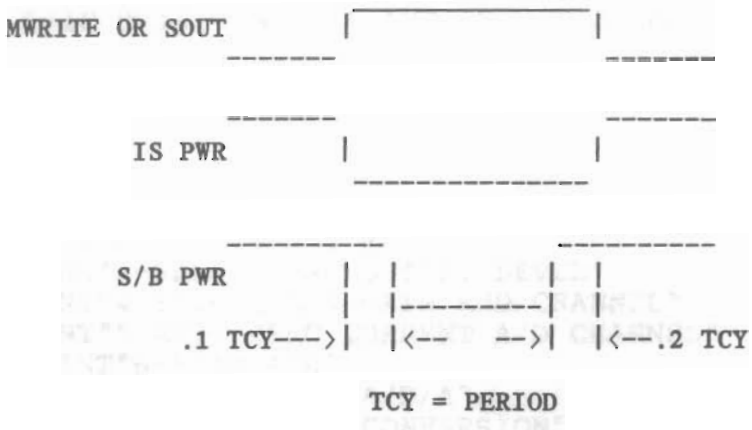
II. Hardware MOD for MWRITE on Host CPU Board or Bus



Comment: MWRITE's falling edge delay should not exceed 30 nsec. after the raising edge of PWR .
If greater, than IEEE-696 timing will not be met.
Do not use this mod, if not familiar with the bus timing requirements.

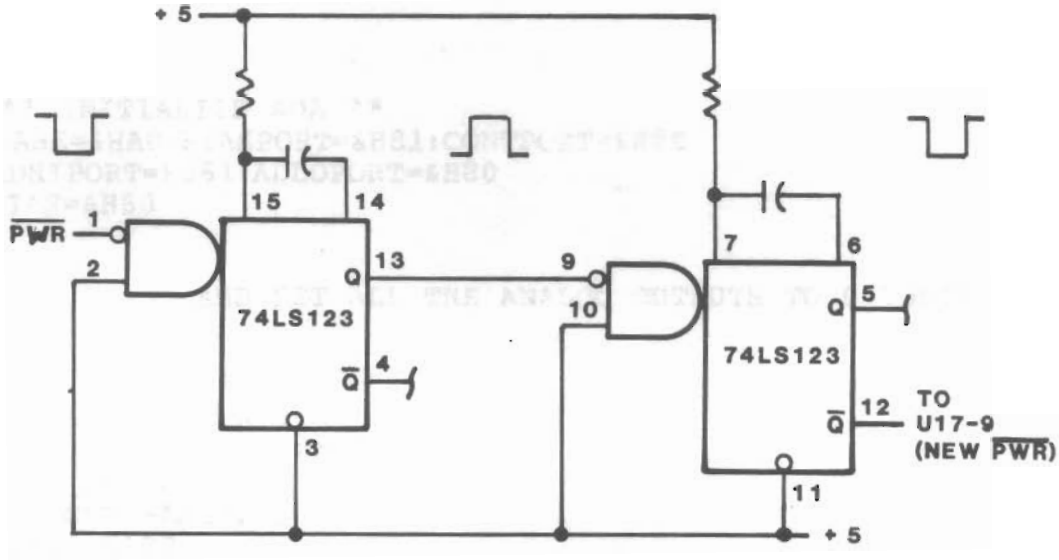
III. Hardware MOD to decrease the width of PWR in relation to MWRITE or SOUT, mostly in older non-IEEE-696 Z-80 CPU boards.

Use a 74LS123 I.C. (dual-one shot) to generate a modified PWR with relation to SOUT as shown below:



TCY = PERIOD

Comment: Will not work when system has boards which assert wait cycles unless the mod is done on-board the A/D/A board.



8.0 Software

The following BASIC program is offered as a collection of examples as to how the A/D/A may be exercized. Specific programs as well as programming languages will depend upon the users application.

```
    THIS PRINTS A MENU AND SERVES AS AN INDEX TO THE PROGRAM

25 GOSUB 160:' INITIALIZE A/D/A
30 '** MENU **
40 PRINT:PRINT:PRINT
50 PRINT"1-SETUP DAC CONTROL MODE"
60 PRINT"2-SELECT DAC REF"
70 PRINT"3-SELECT DAC OUTPUT LEVEL"
80 PRINT"4-SELECT A/D GAIN AND CHANNEL"
90 PRINT"5-AUTO ZERO CURRENT A/D CHANNEL"
100 PRINT"6-READ A/D"
110 PRINT"7-INITALIZE A/D/A"
115 PRINT"8-CONTINOUS CONVERSION"
120 INPUT;Q
130 PRINT
140 ON Q GOSUB 250,410,330,540,1000,2000,160,1130
150 GOTO 30

        DEFINE THE PORTS THAT ARE USED BY THE A/D/A

160 '** INITIALIZE ADA **
170 BASE=&HA0:BIASPORT=&H81:CONTPORT=&H80
171 ADHIPORT=&H81:ADLOPORT=&H80
171 BIAS=&H80

              AND SET ALL THE ANALOG OUTPUTS TO 0 VOLTS

180 CTRL=&H0:GOSUB 2150
190 REF=1:DACDAT=&H7FF
200 FOR I=0 TO 7
210 OUTPORT=BASE+2*I
220 GOSUB 2120
230 NEXT I
```

```
        THEN THE USER MAY BEGIN TO EXERICIZE THE D/A

240 RETURN


  THIS WILL SPECIFY WHETHER THE ANALOG OUTPUTS WILL BE AUTO
REFRESHED OR WHETHER THEY WILL BE REFRESHED UNDER PROGRAM CONTROL.


250 '** SELECT DAC CONTROL MODE **
260 PRINT "SPECIFY SINGLE CHANEL CONTROL OR 8-CHANEL REFRESH"
270 INPUT "TYPE 1 FOR SINGLE OR 8 FOR REFRESH";CTL
280 IF CTL<>1 AND CTL<>8 THEN 250
290 IF CTL=8 THEN CTRL=CTRL AND &HBF
300 IF CTL=1 THEN CTRL=CTRL OR &H40
310 GOSUB 2150
320 RETURN


   THIS WILL LOAD A SPECIFIC OUTPUT LEVEL FOR A GIVEN DAC.


330 '*** SPEC OUTPUT VALUE TO A GIVEN DAC ***
340 INPUT"WHICH DAC DO YOU WISH TO CHANGE";I
350 PRINT "SPECIFY OUTPUT LEVEL FOR CHANNEL #";I;" IN % OF FULL SCALE."
360 INPUT V1
365 IF ABS(V1)>100 THEN PRINT"THAT'S OVER 100%.  TRY AGAIN":GOTO 350
370 V1=-V1
380 OUTPORT=BASE+2*I:DACDAT=INT(V1*2048/100)
382 IF DACDAT=2048 THEN DACDAT=2047
385 DACDAT=(DACDAT AND &HFFF) XOR &H800
390 GOSUB 2120
400 RETURN


  THIS WILL ASK THE OPERATOR FOR THE DESIRED REFERENCE VOLTAGE
          AND INVOKE THE SUBROUTINE WHICH OUTPUTS IT.


410 '** SPEC REF LEVEL FOR DACS **
420 PRINT "SPECIFY CHANEL REFERENCE LEVEL"
430 PRINT "SELECT 10 OR 5 OR 2.5 OR 0 VOLTS"
440 INPUT V2
450 IF V2<>10 AND V2<>5 AND V2<>2.5 AND V2<>0 THEN 410
460 IF V2=10 THEN REF=1
470 IF V2=5 THEN REF=2
480 IF V2=2.5 THEN REF=3
490 IF V2=0 THEN REF=0
```

```
500 LSB=V2/2048
510 OUTPORT=BASE
520 GOSUB 2120
530 RETURN
```

THIS WILL ASK THE OPERATOR WHAT GAIN AND WHICH A/D CHANNEL WILL BE USED AND ACTS ACCORDINGLY.

```
540 '** A/D GAIN AND CHANNEL SELECT ***
550 INPUT"WHICH CHANNEL DO YOU WISH TO SPECIFY";CHSEL
560 PRINT "SPECIFY GAIN OF .5 OR 2 OR 8 OR 32 FOR CHANEL ";CHSEL
570 INPUT GAIN
580 IF GAIN<>.5 AND GAIN<>2 AND GAIN<>8 AND GAIN<>32 THEN 560
590 IF GAIN=.5 THEN GSEL=0
600 IF GAIN=2 THEN GSEL=1
610 IF GAIN=8 THEN GSEL=2
620 IF GAIN=32 THEN GSEL=3
625 LSBAD=5/(2^11*GAIN)
630 INPUT "SPECIFY 1 FOR SINGLE-ENDED OR 2 FOR DIFF.";MODE
640 MODE=MODE-1:IF MODE>1 THEN 630
650 CTRL=(CTRL AND &HC0) OR &H80 OR MODE*&H20 OR GSEL*8 OR CHSEL
660 GOSUB 2150
670 RETURN
```

THIS IMPLEMENTS THE AUTO ZERO ROUTINE DISCUSSED IN??? AND PRINTS OUT THE NECESSARY CORRECTION VALUE.

```
1000 '** AUTO ZERO ROUTINE ***
1010 BIAS=0
1020 GOSUB 2150
1040 GOSUB 2000
1050 DTA1=DTA:BIAS=&HFF
1060 GOSUB 2150
1070 GOSUB 2000
1080 BIAS=INT(DTA1*256/(DTA1-DTA)+.5)
1090 GOSUB 2150
1100 GOSUB 2000
1110 PRINT BIAS
1120 RETURN
```

THIS LOOP CONTINOUSLY READS THE A/D.

```
1130 '** CONTINOUS CONVERSION **
1140 GOSUB 2000
1150 GOTO 1140
```

THIS WILL READ THE A/D AND PRINT THE RESULTS AT THE CONSOLE.

```
2000 '** READS THE A/D AND OUTPUTS TO THE CRT ***
2005 CTRL=CTRL AND &H7F:GOSUB 2150
2010 CTRL=CTRL OR &H80:GOSUB 2150
2020 HIGH=INP(ADHIPORT)
2025 I=INT(HIGH/16) AND 7
2030 IF HIGH AND &H80=0 THEN 2020
2040 HIGH=HIGH AND &HF
2050 LOW=INP(ADLOPORT)
2060 ADDAT=HIGH*256+LOW
2065 ADDAT=ADDAT XOR &HFFF
2070 IF (ADDAT AND &H800)=0 THEN ADDAT=(ADDAT AND &HFFF) ELSE
     ADDAT=(ADDAT OR &HF000)
2080 DTA=ADDAT*LSBAD+LSBAD/2
2095 PRINT USING "INPUT CONVERSION FOR CHANNEL # IS ##.##### VOLTS
     ---- HEX - \  \";I,DTA,HEX$(ADDAT AND &HFFF)
2110 RETURN
```

THIS SUBROUTINE LOADS THE NECESSARY PORTS WITH THE D/A DATA AND REF.

```
2120 '** OUTPUT CONTROL AND DATA TO DACS **
2130 OUT OUTPORT+1,REF*16 OR INT(DACDAT/256):OUT OUTPORT,DACDAT MOD 256
2140 RETURN
```

THIS SUBROUTINE LOADS THE NECESSARY PORTS WITH THE CONTROL BYTE AND WITH THE OFFSET CORRECTION BYTE.

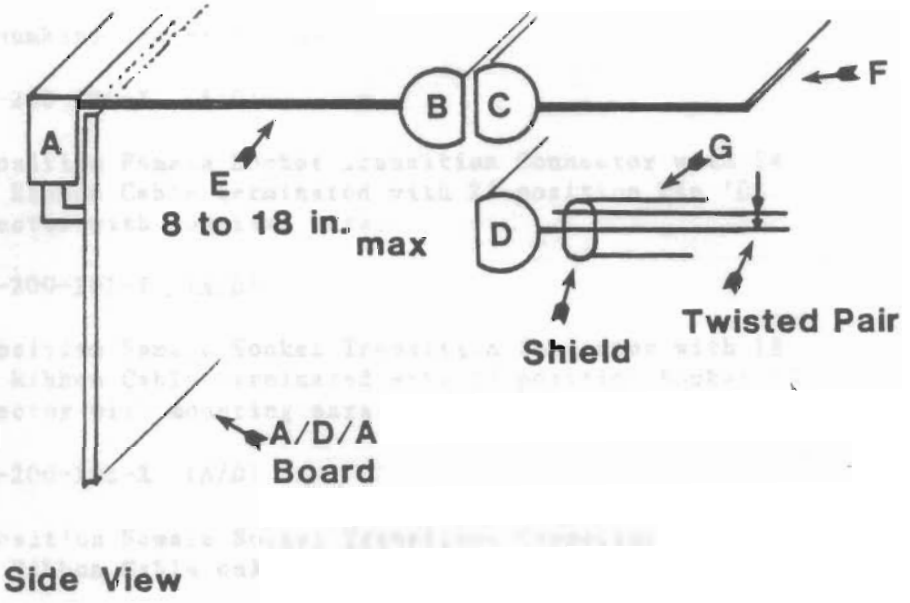
```
2150 '** OUTPUT CONTROL WORDS TO ADA
2160 OUT BIASPORT,BIAS:OUT CONTPORT,CTRL
2170 RETURN
```

9.0 External Cable Configuration

External cable configuration is of great importance when using the A/D/A Converter Board, i.e. improper interconnect configuration may yield erroneous results.

The A/D and D/A edge connector layout has been given consideration to ease the user's interconnecting task.

As shown in Figure 9.1, Interconnect Philosophy, the user has several options when configuring the interconnect cables outside of the host system/mainframe.



A - Board transition connector (socket)
B - Chassis disconnect 'D' type (socket)
C - Chassis mating 'D' type (pin) for flat ribbon cable.
D - Same as above except solder connect
E - Ribbon cable (twisted pair) preffered
F - Twisted pair ribbon cable
G - Twisted shielded pairs (soldered)

FIGURE 9.1 INTERCONNECT PHILOSOPHY

As shown in Figure 9.1, the board edge interconnection should be a short 8 in. (max.) flat ribbon cable (preferably with twisted pairs) with a transition connector at the board's side, terminated with a Delta ('D') type connector.

The 'D' connector is normally mounted to the rear wall of the mainframe. The mating side 'D' connector should be preferably for solder type connections allowing for various shielding configurations. If shielding is not of importance a flat ribbon cable with twisted pairs may be utilized. Woven Inc. makes a twisted pair cable with 2 in. parallel access strip spaced at 18 in. intervals allowing for mass termination connectors.

Low cost interconnect cables similar to those above are available from INPUT/OUTPUT TECHNOLOGY, INC..

The part numbers are as follows:

P/N 52748-200-100-X (A/D)

26 position Female Socket Transition Connector with 18 inch Ribbon Cable terminated with 25 position Pin 'D' Connector with mounting ears.

P/N 52748-200-101-X (A/D)

26 position Female Socket Transition Connector with 18 inch Ribbon Cable terminated with 25 position Socket 'D' Connector with mounting ears.

P/N 52748-200-102-X (A/D)

26 position Female Socket Transition Connector with 18 inch Ribbon Cable only.

P/N 52748-200-131-X (D/A)

34 position Female Socket Transition Connector with 18 inch Ribbon Cable terminated with 37 position socket 'D' Connector with mounting ears.

P/N 52748-200-132-X (D/A)

34 position Female Socket Transition Connector with 18 inch Ribbon Cable only.

P/N 52748-200-133-X (D/A)

34 position Female Socket Transition Connector terminated with two 25 position socket 'D' Connectors with mounting ears.

For pricing information refer to latest INPUT/OUTPUT TECHNOLOGY, INC. PRICE LIST or call INPUT/OUTPUT TECHNOLOGY, INC. for price and delivery.

9.1 External Cable Shielding Considerations

Cable shielding can be extremely helpful or more likely requried when operating in a noisy environment. Ability to shield from radiated/emissive RF sources can be achieved by providing high common mode rejection and shielding as follows:

1. Use twisted pairs for all signals.
   Use the below twist approaches, as provided on the A/D/A connector pin layout.

   a. Signal with ground.

   b. Signal with power.

   c. Differential high with low side.

2. Shield twisted pairs as required.

3. Provide overall shield for above item 2) twisted shielded pairs for best shielding effectiveness.

Shielding techniques are described in many publications and therefore will not be discussed herein.

9.2 CA and CB Connector Specification

A list of several manufacturer's part numbers is provided in Table 9.1.

CONNECTOR	MANUFACTURED	PART NUMBER	TYPE
CA	CANNON I.T.T.	G08D26A3BKAA	FR
	3M	3399-6026 OR 7026	FR
	SMK, LTD.	W-F-2050	FR
	BERG/DUPONT	65846-019	CR
	ROBINSON NUGENT	IDS-26NPK-SR-X	FR
	T and B ANSLEY	609-2601M	FR
CB	3M	3399-6034 OR 7034	FR
	BERG/DUPONT	65846-022	CR
	ROBINSON NUGENT	IDS-34NPK-SR-X	FR
	T and B ANSLEY	609-3401M	FR

FR - Flat Ribbon
CR - Crimp

TABLE 9.1 CA AND CB TRANSITION CONNECTOR MANUFACTURER'S PART NUMERS

10.0 Schematics and Component Layout

The assembled and tested board or kit utilizes quality components for best performance and reliability.

Should it be necessary to replace Out-of-Warranty faulty component(s), the service technician must insure that the replacement is done using identical type parts as provided on the board or the kit. Refer to Figure 10.1, Component Layout, for the correct component schematic designation.

If you are unable to obtain the required part(s), consult INPUT/OUTPUT TECHNOLOGY, INC. on substitute parts. Board peculiar parts may be purchased from INPUT/OUTPUT TECHNOLOGY, INC. directly: write or call for price and delivery.

10.1 Legend

Figure 10.1: **A/D/A Board Component Layout**

Figure 10.2 thru 10.5: **A/D/A Board Schematics**

10.1.1 Component Orientation

Exercise caution when placing components into their respective sockets, especially in the analog (TOP half) portion of the board. Not all I.C.'s are oriented with pin 1 pointing to the top of the board.

Incorrect orientation will damage the I.C. and may also damage other I.C.s.

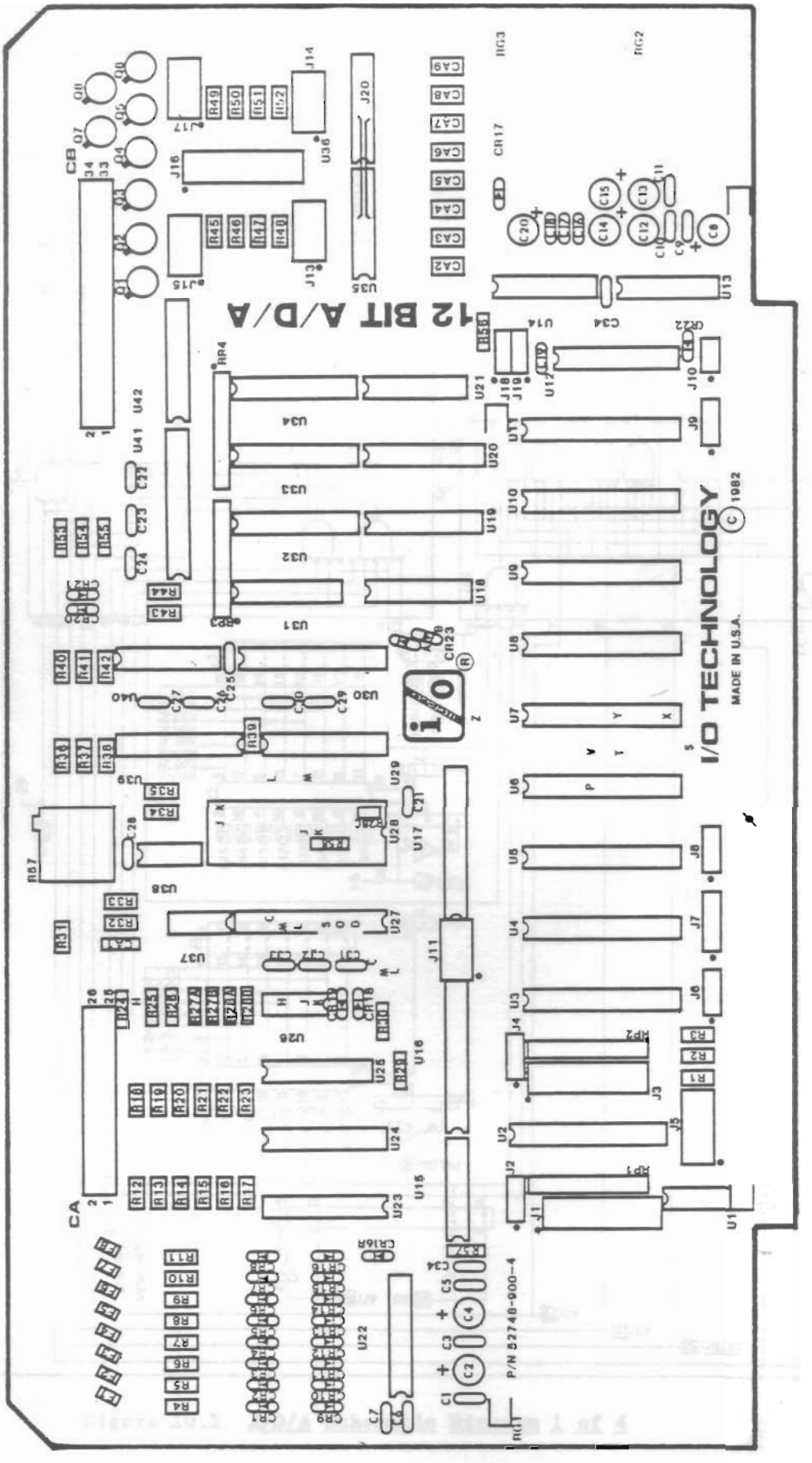


Figure 10.1 **A/D/A Board Component Layout**

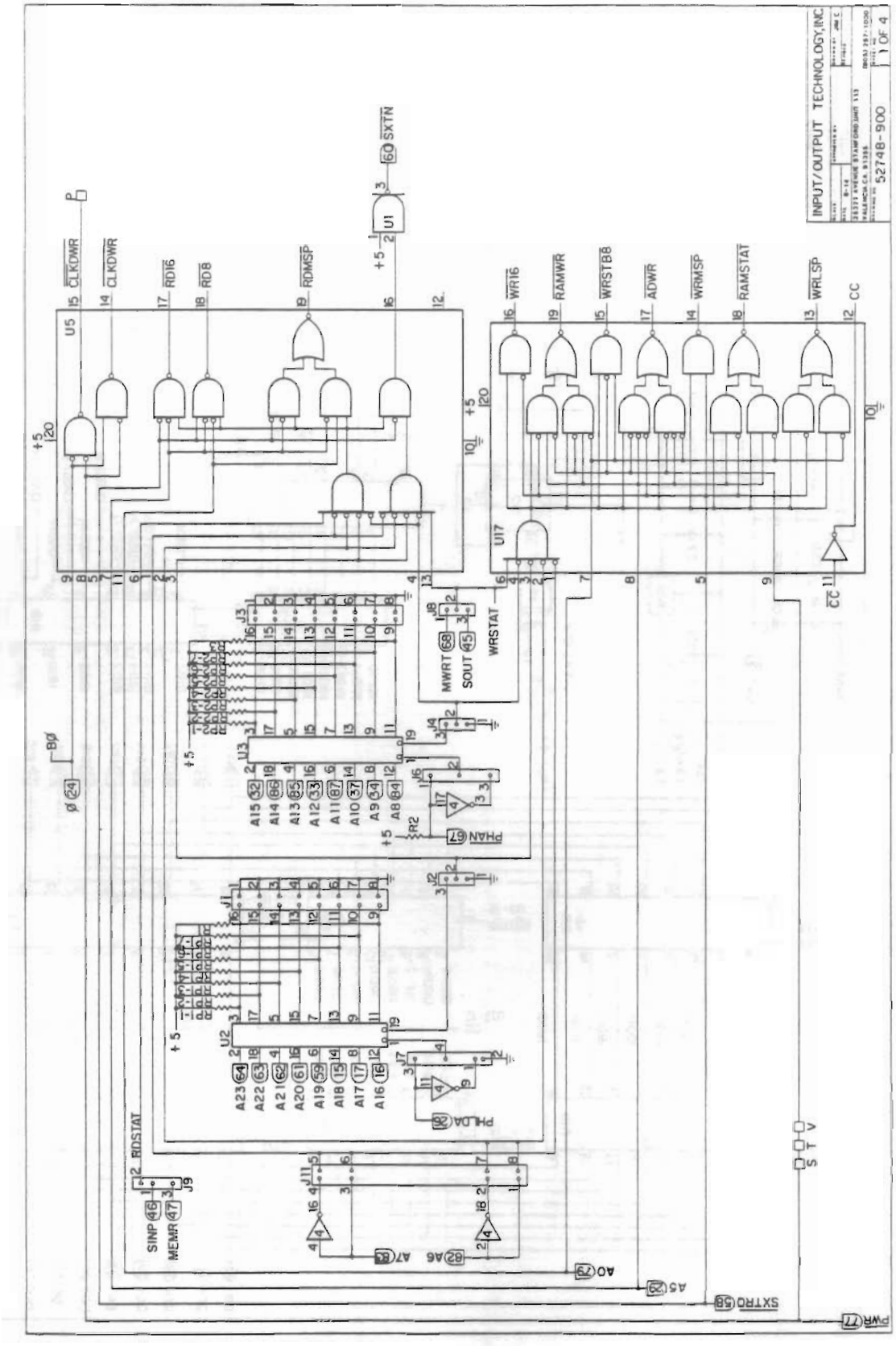


Figure 10.2 A/D/A Schematic Diagram 1 of 4

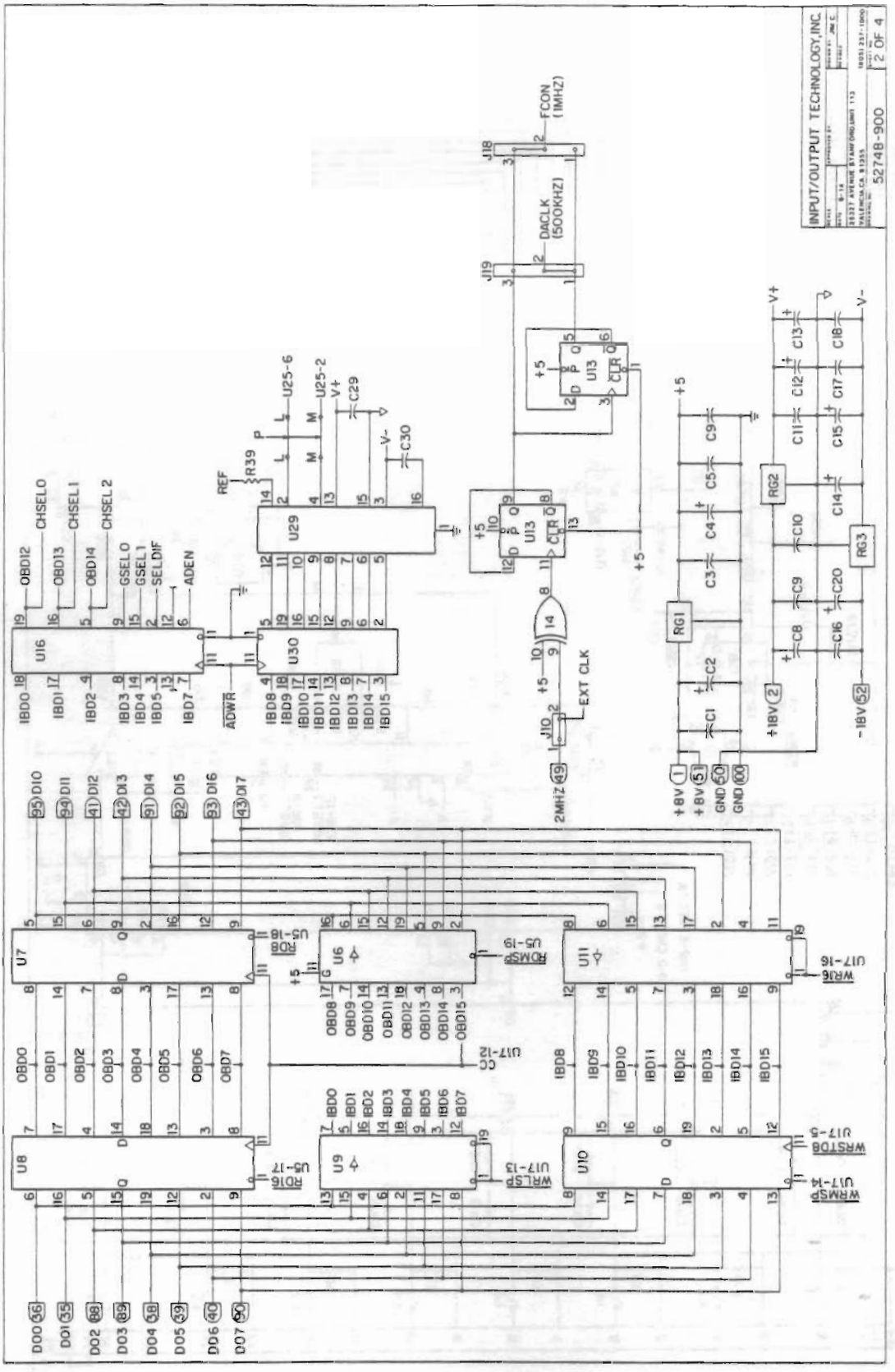


Figure 10.3 A/D/A Schematic Diagram 2 of 4

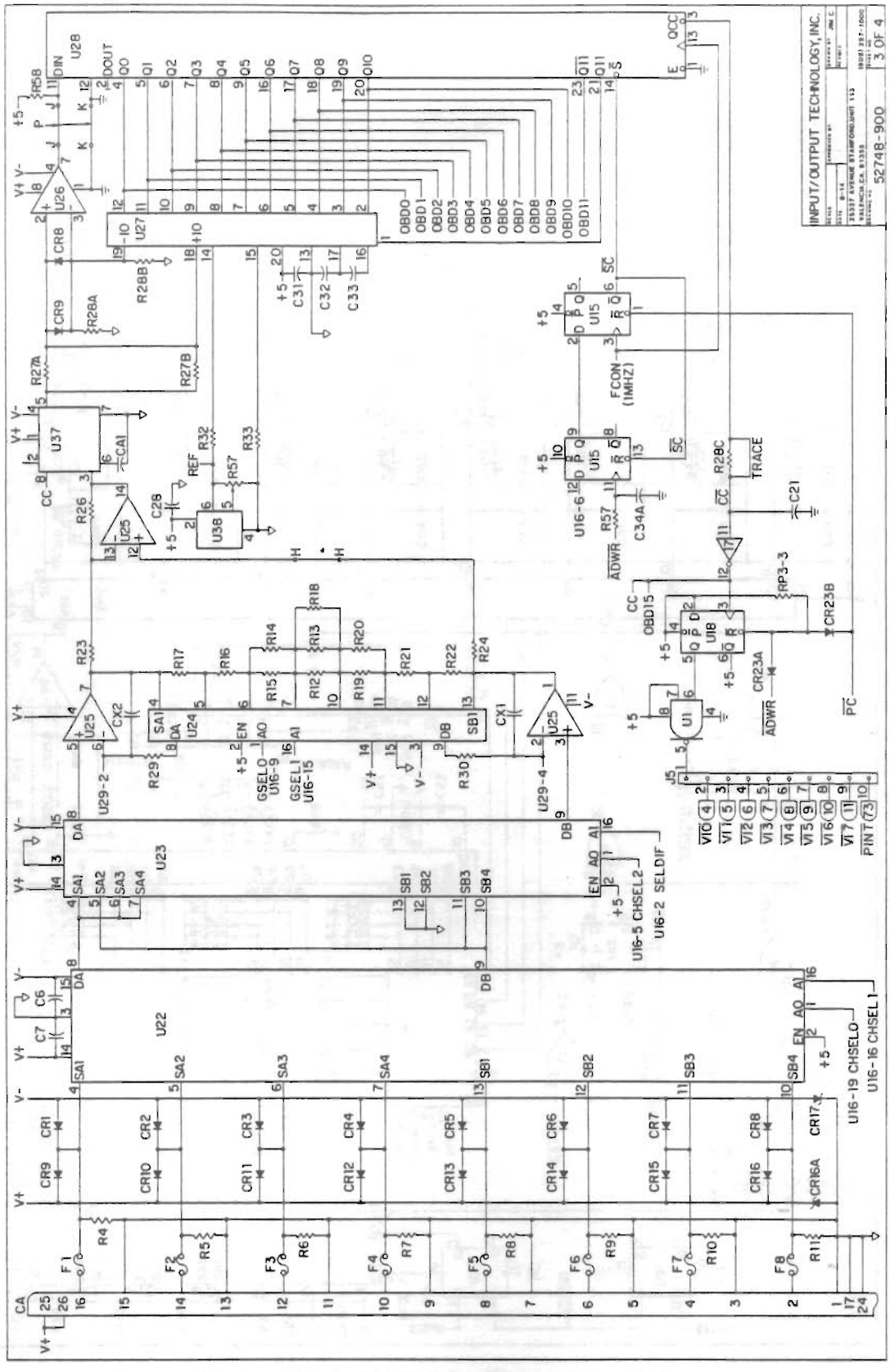


Figure 10.4 A/D/A Schematic Diagram 3 of 4

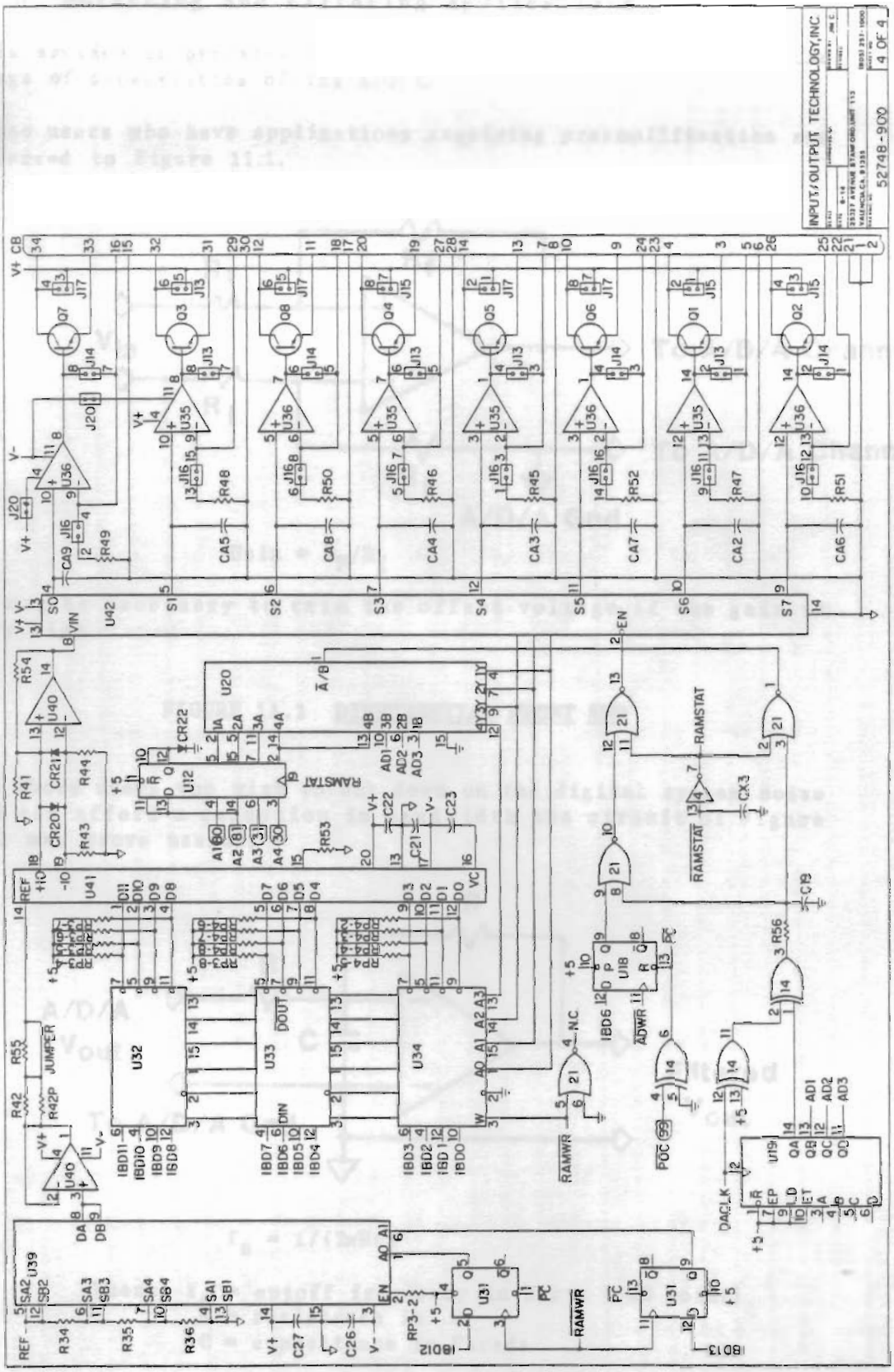
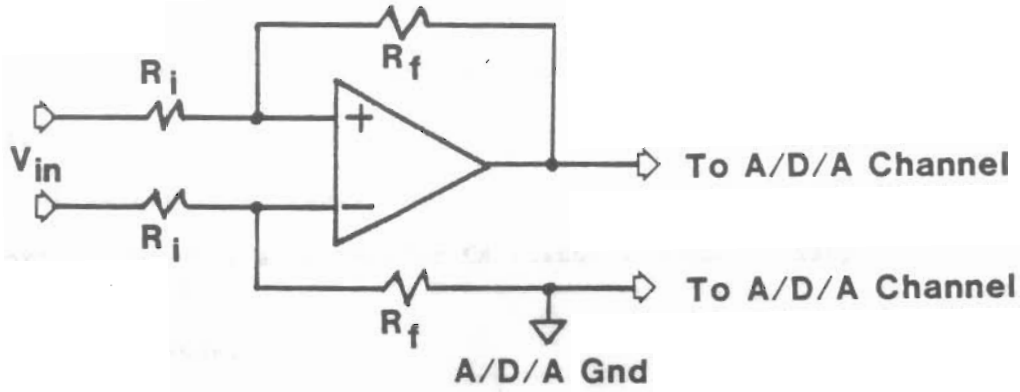


Figure 10.5 A/D/A Schematic Diagram 4 of 4

11.0 Buffering and Filtering Applications

This section is prepared for those users who wish to expand the range of capabilities of the A/D/A.

Those users who have applications requiring preamplification are referred to Figure 11.1.

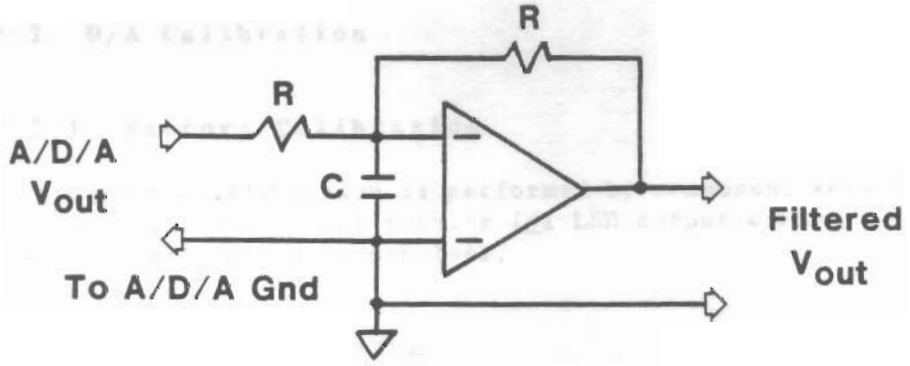


Gain = R_F/R_I

It may be necessary to trim the offset voltage if the gain is very high.

FIGURE 11.1 **DIFFERENTIAL FRONT END**

For those users who wish to cut down on the digital system noise and can afford a reduction in bandwidth the circuit of Figure 11.2 may prove useful.



$$f_c = 1/(2\pi RC)$$

Where: f_c = cutoff frequency in Hertz (3dB point)
R = resistance in Ω
C = capacitance in Farads

FIGURE 11.2 **FILTER**

12.0 Calibration

12.1 A/D Calibration

A/D calibration should be performed at the highest gain that the channels will be used at.

Procedure:

1. Allow 10-15 minutes for board temperature to stabilize.
2. Select A/D channel 0.
3. Select Differential Mode.
4. Short (to ground) at connector CA channels 0 and 4 using 2 shorting plugs.
5. Auto-zero channel 0.
6. Remove channel 0 shorting plug jumper.
7. Connect channel 0 to a precision voltage source, set at (FULL SCALE - 1/2 LSB), i.e. (9.995 at gain of .5)
8. Select continuous conversion on A/D channel 0.
9. Adjust Potentiometere R57 to obtain bit toggling (50% duty cycle is ideal) from FULL SCALE TO FULL SCALE - LSB, i.e., at gain of .5 this would be 9.992 <--> 9.997.

The A/D section is now calibrated.

12.2 D/A Calibration

12.2.1 Factory Calibration

At factory the calibration is performed by component selection of U40, U35 and U36 for best results (±1 LSB output error), after A/D calibration is complete.

12.2.2 User Calibration

If the D/A output error (after the A/D calibration) is greater than ± 1 LSB the user can (a) adjust the output thru software compensation or (b) hardware calibrate the D/A. Should A/D section calibration be not required, then you can use R57 to calibrate the D/A (adjust for full scale).Although this will cause the A/D to be out of cal anywhere from 1 to 2 bits.

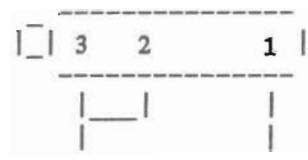
D/A Hardware calibration is accomplished as follows:

1. Solderthe specified resistor on solder side of the board across R42 (parallel).

   R42P = 1/8W, 510K, 5% METAL FILM (25-50ppm/^{o}C)

2. Remove jumper in location R55.

3. Solder the specified potentiometer on the component side of the board in location R55. Before installing short pins 2 to 3 as shown below. Place so that the adjustment screw is to the left.



   R55 = 500Ω, 100ppm/^{o}C, 10-25 turns, i.e. Allen Bradley 94P501

4. Select single D/A channel operation.

5. Select 10V D/A reference.

6. Select D/A channel 0.

7. Select full scale output on D/A channel 0.

8. Adjust R55 to obtain 9.9975 $\pm$ .5 LSB on output D/A channel 0.