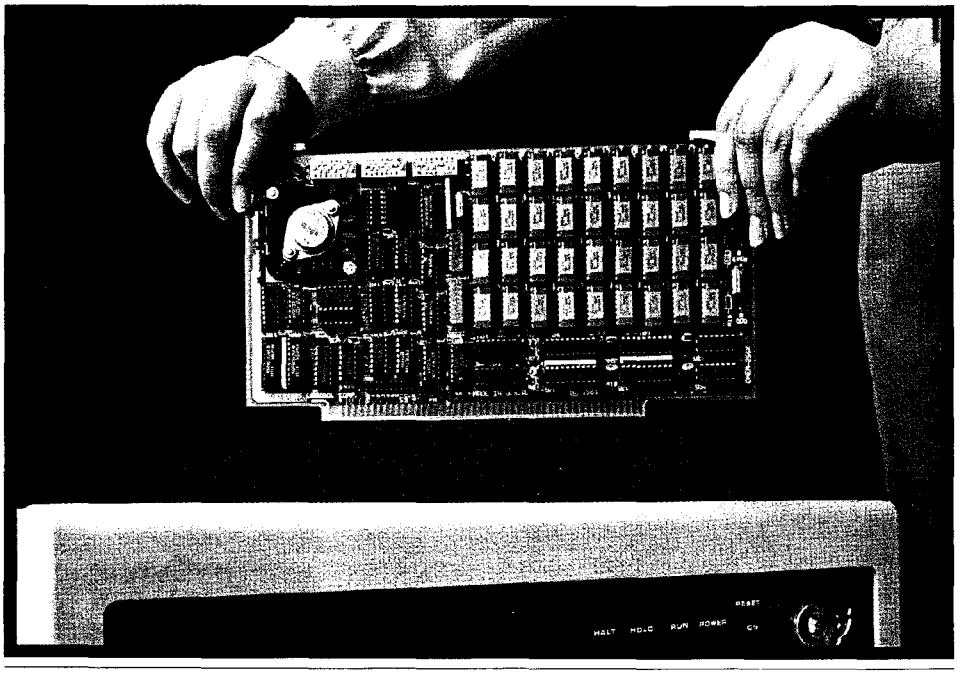
INDUSTRIAL GRADE CARDS FOR THE IEEE-696 / S-100 BUS



POWER AND RELIABILITY

DUAL SYSTEMS CORPORATION

DUAL

system reliability / system integrity

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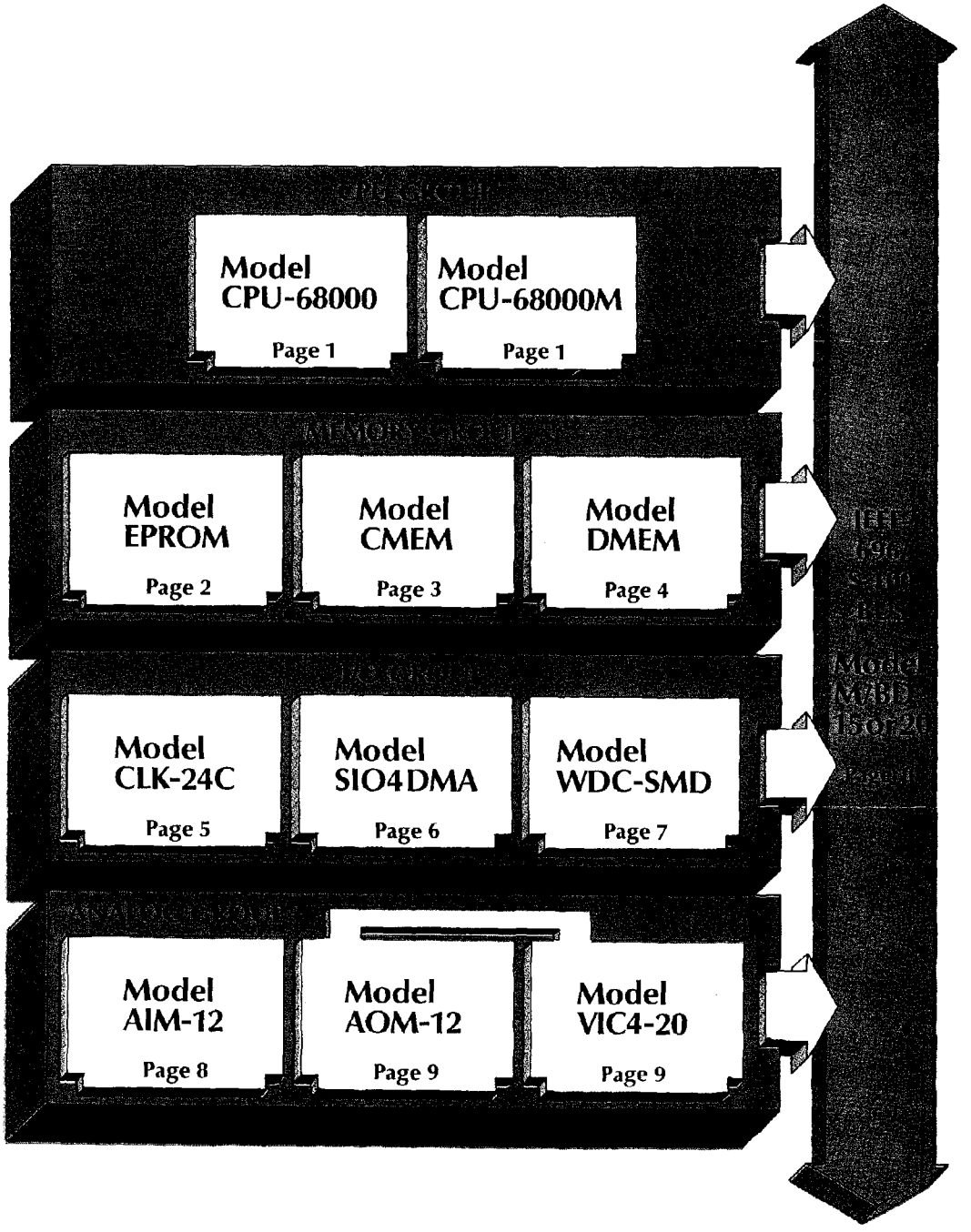
Contents



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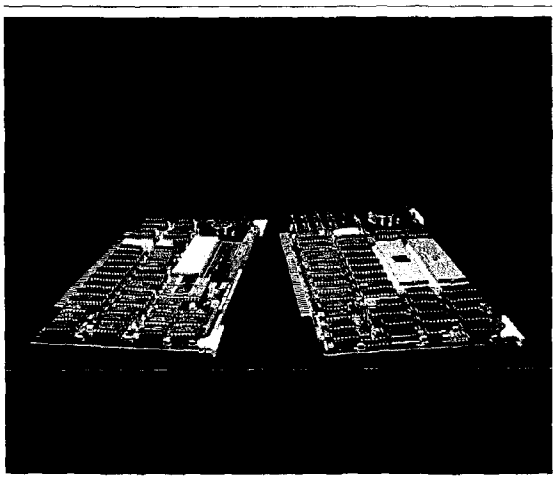
Model CPU-68000

Model CPU-68000

- ☐ MC 68000 processor, 8MHz operation
- ☐ 16 megabyte address space
- ☐ 8KB of on-board ROM containing Motorola MacsBug monitor
- ☐ Strictly follows IEEE-696/S-100 specification
- ☐ Fast memory accesses. No S-100 wait states required when using 4MHz memory.
- ☐ Two powerful interrupt modes: IEEE autovector mode and device-supplied interrupt vector mode.
- ☐ 168-hour burn-in.



Model CPU-68000M

- ☐ Memory management version of CPU-68000, 8MHz operation.
- ☐ Motorola MC68451 MMU
- ☐ Multi-user/multi-tasking
- ☐ Segmented memory management
- ☐ Selectable mapped and unmapped address space
- ☐ 168-hour burn-in.

Model CPU-68000M L10

- ☐ Identical to CPU-68000M above except for operation at 10 MHz.

The most powerful S-100 based CPU cards available, the CPU-68000 and CPU-68000M both utilize a Motorola 16-bit 68000 microprocessor. The CPU-68000 is designed to be a powerful, low-cost, software and hardware development tool, and is backed by Dual Systems' outstanding hardware and software support.

Both CPU-68000 boards conform to the IEEE-696/S-100 standard and will operate with all existing 8-bit peripherals and with memories which meet the IEEE-696/S-100 standard for 16-bit data transfers. They both feature fast 8MHz processor operation, 4MHz bus transfers, 24-bit addressing to access 16 Mbytes of memory directly, and internal 32-bit architecture for computing power comparable to middle/high level minicomputers.

The CPU-68000 includes an 8K byte ROM monitor. The monitor allows memory display, breakpoints, execution trace, traps, downloading programs from other systems, and fifty more basic commands.

The CPU-68000M maintains all of the features of the basic CPU. The on-board ROM is replaced with the MC68451 Memory Management Unit featuring 32 segments of flexible mapping of memory to a user-defined base address, including segment-to-segment protection as well as user-to-system protection.

The CPU-68000M L10 is identical to the CPU-68000M except for component changes that provide operation at 10MHz.

Specifications: *Common to CPU-68000 and CPU-68000M*

Processor: Motorola MC68000.
Clock: 8MHz (10MHz for CPU-68000M L10).
Bus: Meets all requirements of IEEE-696/S-100.
Address Bus: 24 bits; conforms to IEEE-696 extended addressing specifications (16 megabytes). Includes 64K I/O address space.
Data Bus: 16-bit bidirectional data transfers.
Control: Configured as busmaster, provides TMA protocol per IEEE-696. Provides automatic 8/16-bit data path selection for mixed memory configurations (requires 16-bit memory for program execution).
Status Indicators:
RUN (Green LED) HALT (Red LED) HOLD (Yellow LED)
PC Board: Industrial grade epoxy fiberglass (TYPE FR-4), solder masked both sides, screen component legend, plated through holes, gold plated edge connector fingers.
Power Consumption: 950mA nominal @ 8 volts, as per IEEE standards.
User-Selectable Options: A0 line of address bus may be jumpered for high byte or low byte.
Phantom line may be asserted while in USER mode. Example: disk controller may be disabled while not in SYSTEM mode.
Up to 192 interrupt vectors when using device-supplied interrupt vectors.
Relocatable boot and exception vectors.

Specifications: Board dependent

Memory Management Unit
CPU-68000M: Segmented memory management with 256 byte to 16 megabyte variable segment size using Motorola MC68451 (Replaces ROM)
CPU-68000: Not available
ROM
CPU-68000M: Not available
CPU-68000: 8KB of 2732 available. Motorola MacsBug Monitor provided

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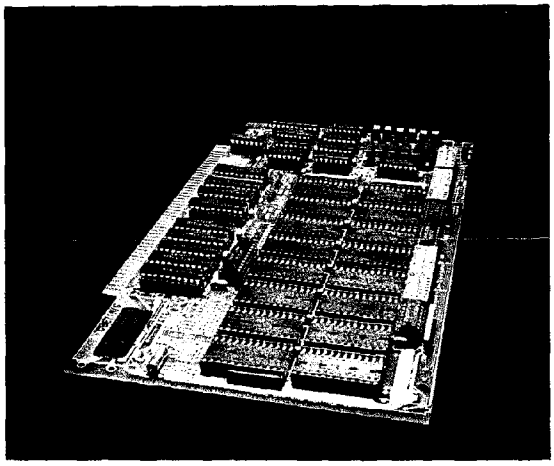
32/64K EPROM/ROM BOARD WITH 16-BIT DATA PATHS

Model EPROM

IEEE 696/S-100 EPROM BOARD DESIGNED FOR 16-BIT COMPUTERS

- ☐ 8- or 16-bit data transfers.
- ☐ Full IEEE 696/S-100 compliance.
- ☐ Runs with 68000, Z-8000, 8086, 16000 and other 16-bit processors.
- ☐ Accepts industry-standard 2716 EPROMS or 2732 EPROMS.
- ☐ 64Kb RAMS may be mixed with 2716 EPROMS, allowing use as RAM/EPROM board.
- ☐ Operates with 8-bit systems, if successive bytes are stored in alternate EPROM chips.
- ☐ Up to 64K on a single board.
- ☐ Extended memory addressing through 24-bit address lines, as well as standard 16-bit addressing.
- ☐ Switch selectable base address on any 4K boundary.
- ☐ 4K blocks of memory may be enabled or disabled by means of a dip switch.
- ☐ On board switch-selectable wait state generator allows operations in 2-8 megahertz systems.
- ☐ Rigorous quality control, including 168-hour burn-in.



The EPROM-32/64K EPROM/ROM board provides for permanent (non-volatile) storage of up to 64K bytes of data. The sixteen on-board sockets accept either industry-standard 2716 or 2732 EPROMS.

The EPROM-32/64K may also be used as a RAM board when type 6116 RAM ICs are installed, in place of 2716 EPROMS. RAMS and EPROMS (type 2716 only) may be mixed, allowing the board to function as a 32KB RAM/ROM board.

Depending on the state of the SXTRQ (sixteen request) line on the IEEE 696/S-100 bus, data may be read from the EPROM-32/64K either a byte at a time, or as 16-bit words. EPROMS/ROMS are installed in pairs, one in the upper row on the board, and one in the lower row. When a 16-bit data transfer is required, the most significant 8 bits are read from one row while the least significant 8 bits are read simultaneously from the other row. [If an 8-bit transfer is required, data is read from either the upper row or the lower depending on whether A0 is high (ODD ADDRESS) or low (EVEN ADDRESS).]

Specifications

Full IEEE Standard 696/S-100 compliance.

Power: 0.6A typical, 1.2A maximum when board is fully loaded with 2732 EPROMS. Operates with 8 volts nominal.

Access Time: Board access time is equal to access time of added EPROM or ROM chips plus 50nS. Example: Board access time is 400nS when loaded with 350nS EPROMS.

Wait States: 0 or 1 wait state (switch selectable).

Address Selection: 24-bit extended addressing or 16-bit global addressing. All addressing is selectable by DIP switches.

Data Transfers: 8-bit or 16-bit. High order (M.S.) byte (during 16-bit transfers) can be jumper selected to have either odd or even address (during 8-bit transfers).

Operating Temperature: 0°C to 55°

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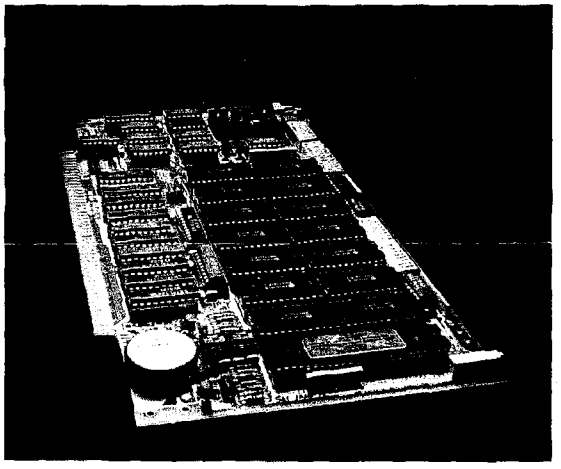
NON-VOLATILE CMOS MEMORY 8K-16K-32K WITH LITHIUM BATTERY

Model CMEM

RELIABLE NON-VOLATILE MEMORY ON STANDARD IEEE 696/S-100 CARD; 8- OR 16-BIT DATA PATHS

- ☐ Up to 32K on a single board.
- ☐ Holds data for 3-10 years with the power off, using on-board lithium battery.
- ☐ Fast: Runs at up to 6MHz for both 8- and 16-bit systems.
- ☐ 220 nanosecond access time, no wait states required.
- ☐ Extended memory through 24-bit address lines.
- ☐ Bank select.
- ☐ Software-programmable write protect window.
- ☐ Powerfail interrupts.
- ☐ Switch-selectable addressing on 4K boundaries.
- ☐ Rigorous testing, including 168-hour burn-in and 1000 cycle volatility test.



These CMOS memory boards store programs and data in a non-volatile medium. These memory modules with battery backup are guaranteed to keep programs and data intact for 3-10 years with the factory supplied battery.

The Dual Systems CMEM series of memory modules do not sacrifice performance for non-volatility. These modules have a 220 nanosecond access time, and run at full speed up to 6MHz with no wait states. The CMEM series of memories are compatible with Cromemco, North Star, CCS and all other S-100 computers, as well as the new IEEE-696/S-100 compatible 16-bit processor boards.

Applications

The CMEM modules are useful in a wide variety of applications where it is necessary to store data and programs in high-speed memory, even with the power turned off. Applications include industrial controllers, remote data acquisition systems and high-reliability systems which would otherwise require disk or tape storage.

Software Programmable Write Protected Areas*

With the Dual Systems CMEM modules, you can write-protect part of the memory, while allowing the rest of memory to be written.* This allows parts of a program, or selected data, to be changed without any risk of accidentally writing over other data which must be protected. With this safety feature, the DUAL CMEM boards can be made to behave virtually like EPROM boards, while retaining the high-speed and instant writability of a RAM board.

Power-Fail Interrupt

The CMEM memory boards contain an on-board circuit for generating interrupts when a power failure is detected, enabling the system to store critical data before the main power supply voltage fails.

Easy to Use with 8-Bit and 16-Bit Systems

Data path widths of either 8-bits or 16-bits are selected automatically in systems which conform to the new IEEE-696/S-100 standard. Boards run in 8080, Z-80, 8085, 8086, Z8000, 16000 and 68000 systems.

*Patent Pending

Specifications

IEEE standard 696/S-100 bus: Meets all specifications of the S-100 bus.

Power: 700 milliamperes nominal during operations at 25°C. Standby power 2 microamps nominal per 8K of memory at 25°C. Operates with 8 volts nominal, or with on-board battery supply during standby.

Access Time: 220 nanoseconds, guaranteed to run with IEEE-696/S-100 6 megahertz systems.

Addressing: Switch selectable addressing on 4K byte boundaries. Base address is dip switch selectable. 4K blocks may be disabled.

Models:

CMEM-8K (8K Bytes)
CMEM-16K (16K Bytes)
CMEM-32K (32K Bytes)

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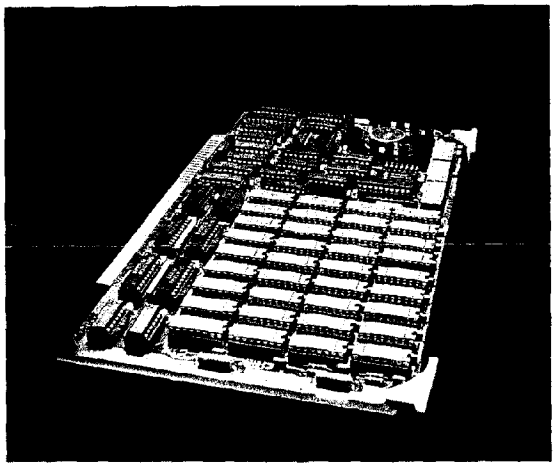
256K HIGH DENSITY DYNAMIC MEMORY Model DMEM

HIGHLY RELIABLE, HIGH DENSITY MEMORY ON STANDARD IEEE 696/S-100 CARD WITH 8- OR 16-BIT DATA PATHS

- ☐ A full 256K Bytes on a single board.
- ☐ 8- or 16-bit data transfers as requested with optional configuration of left/right byte.
- ☐ Two independently addressable 128K Byte regions using the IEEE 696 24-bit extended addressing.
- ☐ FAST: Runs at 4MHz for both 8- and 16-bit systems.
- ☐ 230 nanosecond access time, no S-100 wait states required.
- ☐ Parity checking on each byte.
- ☐ Parity checking error options:
  - pulsed vectored interrupt.
  - latched vectored interrupt.
  - bus error signal generation.



- ☐ Uses 64Kb dynamic memory chips with large cell geometry for lowest soft error rate in the industry.
- ☐ Indicators for activity (green) and error (red).
- ☐ Transparent refresh allows operations without wait states or arbitration delays.
- ☐ Low power consumption– 4 Watts nominal.
- ☐ Refresh maintained during processor reset.
- ☐ Rugged industrial card with 168-hour burn-in period, during which the board undergoes continuous testing.

As with all DUAL products, the DMEM is designed and constructed for extreme reliability. 100% dynamic burn-in for for 168 hours at elevated temperatures is standard procedure for all of DUAL's boards.

The DMEM board is the highest density memory board available for the IEEE 696/S-100 bus. Its fully featured characteristics make it useable in both 8- and 16-bit systems. The DUAL SYSTEMS DMEM modules do not sacrifice performance for density. The modules have a 230 nanosecond access time, and run at full speed in up to 4MHz IEEE 696/S-100 systems with no wait states – even in fast mode.

Data integrity for each board is guaranteed with the added byte parity check bit. The DMEM maintains even parity on even numbered bytes and odd parity on odd numbered bytes. Red and green LED indicators facilitate monitoring of operation. Each board is put through an intensive computer actuated testing procedure throughout burn-in and prior to shipment.

The DMEM-256KP is organized as two 128Kb blocks of memory with each block switch-selectable on 128Kb boundaries. The built-in refresh scheme does not require any processor overhead and is transparent to the CPU.

Nominal power consumption is four Watts, assuring that the board will run at moderate temperatures and provide a large margin of safety.

Applications

The DMEM is an ideal companion to the DUAL CPU/68000 series of CPU cards in any IEEE 696/S-100 compatible mainframe.

The memory, with 24-bit addressing can be used in any 8- or 16-bit system where large amounts of ultra-reliable dynamic memory are required.

Specifications

IEEE 696 Bus Compliance: Slave D1/D16 M24 VI F4 T230.
Access Time: 230nsecs, pSTVAL to DI.
Cycle Time: 750ns, including transparent refresh.
Wait States: None required nor provided.
Address Selection: By DIP switches to any 128K byte boundary.
Data Transfers: 8- or 16-bit. In 16-bit transfers, the standard configuration supports the most recent IEEE proposal with respect to odd and even-numbered bytes. (Odd numbered byte is on the DO Bus.) An optional configuration supports the older proposal.
Power: The +8V supply is regulated on board to +5V. Current at 4/3 Mfetches/sec. is 965ma typ., 1450ma max. Current with all references to other boards is 835ma typ., 1250ma max. No connection to +18V or −18V supplies.
Operating Temperature: 0 to 55 degrees Celsius.
Models: DMEM-256KP (256K Bytes with parity)

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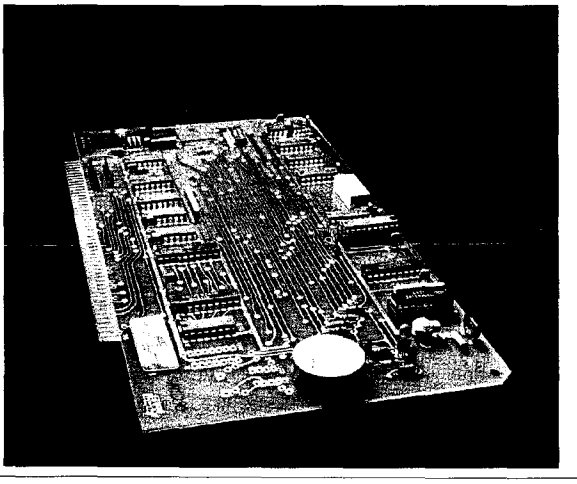
CLOCK-CALENDAR MODULE WITH LITHIUM BATTERY

Model CLK-24C

NEWEST CLOCK CHIP TECHNOLOGY ON AN IEEE STANDARD 696/S-100 CARD

- ☐ Features LSI CMOS chip
- ☐ Day, date, hours, minutes and seconds
- ☐ 12- or 24-hour time format
- ☐ On-board battery backup
- ☐ Three year minimum operation without resetting
- ☐ Uses longlife Lithium battery
- ☐ Low power dissipation in standby mode
- ☐ Vectored interrupt capabilty
- ☐ Leap year identification
- ☐ Dip switch selectable port address
- ☐ Precision quartz crystal clock time base
- ☐ Rigorous quality control, including 168-hour burn-in.



Battery Back-up Guaranteed for Three Years

The CLK-24C clock-calendar module is delivered in operation powered by the on-board battery. This long-life lithium battery will operate for at least three years, and more typically five to eight years with or without power on.

All this is made possible by a new LSI CMOS clock chip which maintains the correct time with standby power requirements of less than 90uW.

Simplified Programming

Programming the clock module in either BASIC or assembly language is straightforward. Unlike previous clock chips, which require lengthy programs, CLK-24C can be programmed with minimal software. Because the CMOS chip is designed specifically for microprocessor systems, standard I/O instructions can be used to set and read both time and date. Program listings in 8080 assembly language and BASIC for simple time and date readout are included in the manual.

SAT	08/15/80	3:55

Applications

The clock module can be used in a wide variety of applications. It can control an automatic sequence of events, such as turning on pumps, lights or heaters at predetermined times, or it can initiate data logging at set intervals. This board lends itself to any application requiring time interval sequencing as well the ability to continue keeping time with main power off.

Specifications

IEEE-696/S-100 standard: Meets all standards of the IEEE 696/S-100 bus

Power: 30μA max at VCC = 3.2v standby (battery supply). 150 mA typical at VCC = 8 volts operating.

Accuracy: Quartz crystal 32.768KHz ± 20 ppm max. Guaranteed accurate to within 50 seconds per month.

Addressing: Base address: dip switch programmable, I/O mapped Data register: base address +0. Control register: base address +1.

Vectored interrupt capabilities: Can be jumper selected to interrupt on 1/1024 second, 1 second, 1 minute or 1/64 second.

Temperature: Rated for operation at greater than 130°F.

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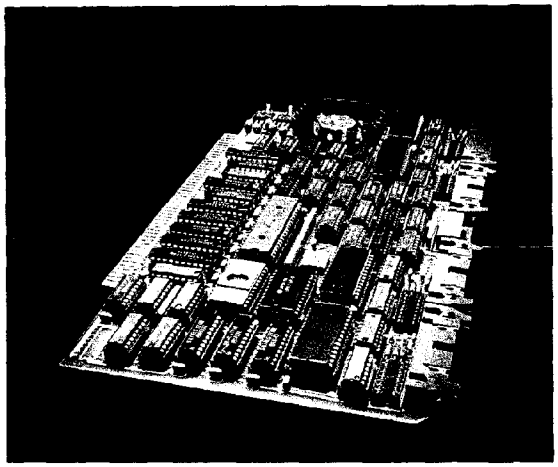
INTELLIGENT FOUR PORT SERIAL I/O Model SIO4-DMA

THE MOST ADVANCED SIO BOARD AVAILABLE FOR THE IEEE 696/S-100 BUS

- ☐ 256 bytes of FIFO buffer for input characters
- ☐ DMA transfers for output
- ☐ 24 bits of memory address, with no restrictions on boundaries
- ☐ Can be connected to RS-232 terminals or modems
- ☐ RS-232 drivers and receivers conform fully to specification
- ☐ Control-S/Control-Q protocol supported
- ☐ Printers with "Buffer Full" signal lines supported
- ☐ USARTs accessible directly for special functions
- ☐ Limited synchronous mode capability
- ☐ Program selectable Baud rate
- ☐ Occupies only 16 I/O addresses
- ☐ Rugged industrial card with 168-hour burn-in period, during which the board undergoes continuous testing.



The SIO4-DMA is an intelligent, high performance, four-port serial input/output board. It conforms to the IEEE-696/S-100 specification but is also designed to work with older S-100 processors. The board is intended to be used with asynchronous terminals or printers in multi-user systems and has the necessary features to work with modems. A limited synchronous mode capability adds flexibility.

All input data to the SIO4-DMA passes through a 256-byte FIFO buffer, removing the requirement for fast response time from the operating system and avoiding the possibility of "lost" characters.

On output, the SIO4-DMA reads characters directly from the S-100 machine's memory by DMA and transfers them to the serial port. This can reduce the operating system overhead for output operations several hundred times. The board is capable of a full 24-bit address range and will increment over any address boundary.

Baud rate is independently selectable on each channel by program. Sixteen of the most popular speeds are provided.

Applications

The SIO4-DMA is the first S-100 serial interface board designed specifically to reduce operating system overhead in multi-user systems. The tasks normally performed by the operating system to handle serial input and output are assisted by intelligence built into the microcomputer (8085A) assisted SIO4.

Specifications

Bus Compatibility: The SIO4-DMA is compatible with the IEEE 696/S-100 specifications as defined in January 1982 and is suitable for systems with up to 8MHz clocks. The SIO4-DMA is also intended to be compatible with many older S-100 computers.

IEEE 696/S-100 Compliance: M24, VI, TM, F8, W1-16. Number of wait states depends on S-100 clock rate and state of SIO4-DMA when accessed.

Address Selection: I/O address selected by DIP switch. Eight bits of I/O address are decoded.

Operating Power: The maximum power consumption is:
+8 Volts @ 1.3 Amps
+16 Volts @ 0.1 Amps
−16 Volts @ 0.1 Amps

RS-232 Compliance: All RS-232 drivers and receivers conform to the RS-232 specification. The SIO4-DMA can simulate either a modem (DCE) or terminal (DTE) for connection to a terminal or modem respectively.

Synchronous Mode: In the synchronous mode the external clock signal determines receive baud rate. A transmit clock is provided by the SIO4-DMA at the selected baud rate.

Baud Rates: The following baud rates are available:

45.5	1200	134.5	4800
50	1800	150	9600
75	2000	300	19200
110	2400	600	38400

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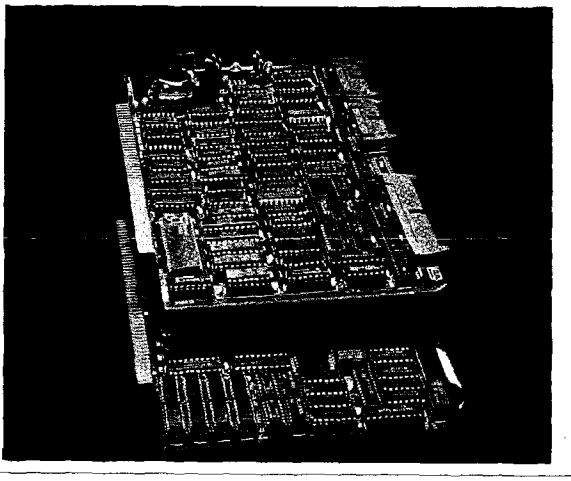
SMD HARD DISK CONTROLLER Model WDC-SMD

SPECIALLY TAILORED FOR HIGH THROUGHPUT REQUIRED BY UNIX™ SYSTEMS

- ☐ Controls one or two industry-standard SMD drives
- ☐ Disk data rate can be up to ten megabits per second
- ☐ Supports drives with any number of heads up to 128
- ☐ Supports drives with up to 2,048 cylinders
- ☐ Allows up to 255 sectors per track
- ☐ User-selectable sector sizes of 256, 512, 1024 or 2048 bytes
- ☐ Overlapped seeks supported
- ☐ Supports the following instructions:
  - Read up to 65,535 blocks
  - Write up to 65,535 blocks
  - Write with verify
  - Verify only
  - Seek (required for overlapped seeks only)
  - Format track
  - Set drive parameters
  - Read drive parameters



- ☐ Transfer rates •Write to disk (including DMA transfer times):
  Peak: 2.5 megabytes per second (DMA transfer rate)
  Sustained: 560,000 bytes per second
  Read from disk:
  Peak: 2.5 megabytes per second (DMA rate)
  Sustained: 800,000 bytes per second
  Note: Sustained times are measured during multiple track read or write operations on a system with 5MHz bus clock.
- ☐ Transfers are 16-bit wide (board set must be used in systems capable of 16-bit transfers).
- ☐ Conforms to IEEE-696 specifications
- ☐ Lookahead buffer enhances speed when reading a string of adjacent blocks.

The WDC-SMD is designed to offer the highest data throughput practically possible in a disk controller with a single-track buffer.

All sectors on a track transfer within essentially a single disk rotation, regardless of the place on the track over which the head first settles and regardless of the order in which the sectors are encountered by the head. For example, if the WDC-SMD is asked to read sectors 3 through 20 on a track, and the head first settles (after seeking) in the middle of sector 8, the controller transfers sectors 9 through 20 first, and then reads sector 3-8 when these sectors pass under the head. In this way the controller guarantees that the complete track is transferred within a single rotation from the time the first readable sector header is encountered. Conventional controllers can take up to two rotations to do the same transfer. Transfers between disk and system memory can occur at full disk speed (assuming other components in the system permit this) due to a two-port, full-track 64-K byte buffer memory. No interleaving is required.

The WDC-SMD offers the lowest conceivable system overhead. Full-track buffer control and multi-sector transfers are all fully automatic, and require no operating system overhead. Also, logical-to-physical translation and automatic switching over track and head boundaries are handled completely by the WDC-SMD. In fact, any size transfers, from one sector to a full-system-memory transfer can be accomplished with only four instructions from the system:

1. Whether a READ or WRITE is desired.
2. The STARTING DISK BLOCK to be transferred.
3. The STARTING DMA ADDRESS in the system memory.
4. The NUMBER OF BLOCKS to be transferred.

The operating system needs to do nothing else. The WDC-SMD will generate an interrupt when the transfer has been completed.

16-Bit throttled DMA data transfers allow the highest possible throughput, and minimize bus latency for other devices.

Each WDC-SMD controller can control up to two industry standard SMD disk drives, and can command overlapped seeks on these drives.

Channel-driven command interface simplifies communication between the operating system and disk controller.

APPLICATIONS

Large, heavily loaded multi-user systems, where several users are simultaneously performing disk-intensive operations, such as compiles, data base management functions and loading of large programs which cause the system to swap. In particular, systems running UNIX* require high disk throughput for reasonable system performance.

High-throughput data logging applications where predictable and fast disk availability is needed.

Digital voice storage

Animation and other video applications in which a series of several hundred frames are computed, and then must be displayed in rapid succession, to create a moving picture.

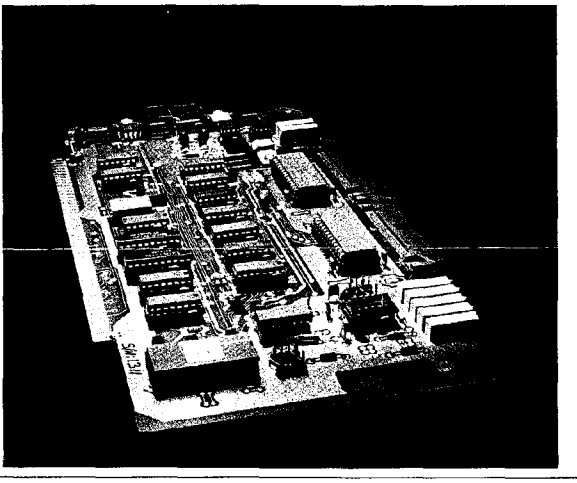
Systems with virtual memory.

*UNIX is a trademark of Bell Laboratories.

12-BIT A-TO-D CONVERTER Model AIM-12

RELIABLE (IEEE 696/S-100) ANALOG-TO-DIGITAL CONVERTER

- ☐ 12-bit resolution and accuracy
- ☐ 25 microsecond typical conversion time.
- ☐ 32-channels single-ended; 16 channels differential.
- ☐ High-speed sample and hold amplifier.
- ☐ Instrumentation amplifier with resistor-selectable gain optional, Gain = 1 to 1,000.
- ☐ Precision analog multiplexer.
- ☐ BASIC and Assembly program provided.
- ☐ User-selectable input ranges.
- ☐ Operates over 0 to 70°C temperature range.
- ☐ High stability, low-noise operation.
- ☐ 168-hour burn-in.



The AIM-12 is a high-reliability module for applications requiring dependable high-speed analog-to-digital conversion. Amplifier gain selection and multi-channel inputs are for user convenience.

Input voltage ranges are jumper programmable on the board. Accurate conversion of rapidly changing signals is obtained using a high-speed sample and hold amplifier.

Each board is addressable with onboard DIP switches, and multiple boards may be used for taking data from many inputs.

Applications

The AIM-12 is designed for applications in the laboratory and in industry for general use in converting analog signals to digital information. The on-board amplifier permits a wide variety of input signals to be accommodated without further signal conditioning. Data may be sampled at rates up to 30 KHz.

The instrumentation amplifier is gain programmable by the selection of one resistor, permitting direct conversion of high-level signals as well as low-level signals from such sensors as level indicators, strain gauges, pressure transducers and pH electrodes.

Specifications

Function: High-speed, multiplexed analog-to-digital data acquisition module with IEEE 696/S-100 bus interface.

Analog Inputs: Number of Inputs to Multiplexer: 32 single-ended or 16 differential. Input Voltage Range (Full-scale range without instrument amplifier option): −10 to +10V, 0V to +10V, −5V to +5V, jumper selectable. With instrumentation amplifier set at G = 100, full-scale range is 0 to 100mV or −50mV to +50mV. Flexible intermediate ranges provided.

Maximum Signal Input Voltage: ±10V.

Precision Instrumentation Amplifier Available Gains: (Programmable with one resistor): 1 to 100. CMRR at gain of 100: 114dB. CMRR at gain of 1: 80dB.

Noise: Level dependent on system; signal averaging often useful for sub-millivolt signal levels.

Input Impedance: Differential Input Impedance: $>10^9\Omega$. Common Mode Input Impedance: $>10^{10}\Omega$

Accuracy: Resolution and accuracy of 12 bits. Non-linearity error: ±½ L.S.B.* No missing codes over temperature range 0 to 70°C. *Measured over ±9V.

Stability: Tempco of Gain: 30 ppm F.S.R./°C. Tempco of Offset ADC: 5 ppm F.S.R./°C. Input Offset Voltage Diff. Amp.: 1.0 mV max (0.5 mV typ). Input Offset vs Temp. Diff. Amp.: 2μV/°C max.

Temperature: Rated for operation up to 130°F.

Signal Dynamics: A-to-D Conversion Time: 25μsec. typ. (35μsec. max) Multiplexer Settling Time: 1.9μsec. (10V step to 0.02%). Diff. Amp. Slew Rate, 10v/μsec. at unity gain. Sample and Hold Aperture: 50 nanoseconds. Sample and Hold Acquisition Time, 10V − 0.01%, G = 1, C_H = .001μF: 5μsec.

Addressing: Base Address: DIP Switch Programmable, I/O Mapped, status Register Address: Base Addrs + 0. Input Control Register Address: Base Addrs + 0. Output Data Register Address: Base Addrs + 2,3.

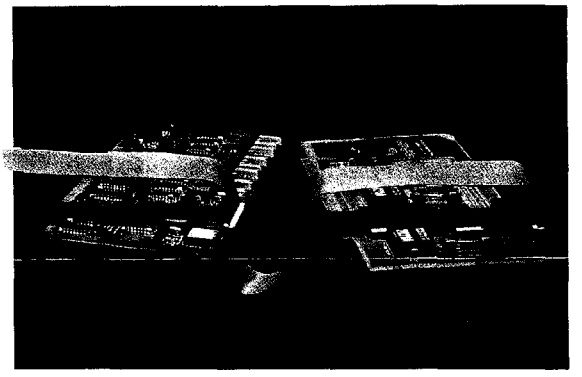
Power Requirements: 0.6A max. at +8V. 100 mA max. at +18 and −18V.

Models: AIM-12, standard input modules.
AIM-12B, input modules without instrumentation amplifier.

Model AOM-12 Model VIC4-20

4-CHANNEL, HIGH PRECISION DIGITAL-TO-ANALOG CONVERTER FOR IEEE-696/S-100 SYSTEMS

- ☐ 12-bit ± ½ L.S.B. accuracy over full 0 to 70°C temperature range.
- ☐ Voltage outputs of 0 to 10 volts, ±5 volts, and ±10 volts, jumper selectable.
- ☐ Short-circuit protection on all voltage outputs.
- ☐ Switch-programmable port base address selection allows use of multiple boards.
- ☐ Choice of straight binary or two's complement notation
- ☐ All outputs may be reset to zero volts during powerup.
- ☐ 168-hour burn-in.



CONVERTS VOLTAGE OUTPUTS FROM AOM-12 INTO FOUR SEPARATE 4-20MA CURRENT OUTPUTS

- ☐ 4-20 mA current outputs for industry-standard controls
- ☐ Overvoltage protection on all current output.
- ☐ Full 12-bit performance.
- ☐ 12-bit ± ½ L.S.B. accuracy over full 0 to 70°C temperature.
- ☐ Transient protection per ISA standards.
- ☐ Low drift, .01%/°C.

The AOM-12 analog output module is a 12-bit, 4-channel digital-to-analog (D-to-A) converter which converts digital commands from the computer into analog voltages.

Analog Connections

Analog voltage outputs leave the AOM-12 through a rugged 34-pin male PCB header located at the top of the board. The header is arranged with alternate ground wires between all output lines to minimize crosstalk between channels.

Software

The AOM-12 is simple to use and may be controlled using the "OUT" instruction in either BASIC or Assembly Language. Multiple AOM boards may be used in a system.

The VIC4-20 is a voltage-to-current converter module which provides industry-standard 4-20 mA current outputs when used in conjunction with the AOM-12. It converts the 0-10V AOM-12 output to a 4-20 mA output.

Analog Connections

The analog current outputs leave the VIC4-20 through a rugged 34-pin male PCB header located at the top of the board. The header is arranged with alternate ground wires between all output lines to minimize crosstalk between channels.

Specifications: Model AOM-12

Analog Outputs: Number of channels: 4. Output Voltage Ranges: −10V to +10V, 0V to +10V, −5V to +5V. Output Impedance (d.c.): 0.05Ω typical. Short Circuit Duration: Indefinite short-to-ground tolerated without damage.

Accuracy (0 to 70°C): Resolution: 12 bits. Linearity Error: ±¼ L.S.B. typical, ±½ L.S.B. maximum. Differential Linearity Error: ±½ L.S.B. typical, ±¾ L.S.B. maximum. Guaranteed monotonic over full 0 to 70°C temperature range.

Conversion Speed: Settling Time to ±0.01% of F.S.R. for F.S.R. Change of −0V to 10V Range or −5V to 5V Range: 3μsec. typical. −10V to 10V Range: 5 μsec. typical.
For 1 L.S.B. Change: 1.5 μsec. typical.
Slew Rate: 10V/μsec. min., 15V/μsec typical.

Drift (0 to 70°C): Total Bipolar Drift – including gain, offset and linearity drifts: ±20 ppm F.S.R. per °C.

Total Error –
- Bipolar Output Ranges: ±0.08% F.S.R. typical, ±0.10% F.S.R. maximum.
- Unipolar Output Ranges: ±0.06% F.S.R. typical, ±0.15% F.S.R. maximum.
- Gain Error: ±15 ppm/°C typical, ±30 ppm/°C maximum.
- Unipolar Offset: ±1 ppm/°C typical, ±3 ppm F.S.R./°C maximum
- Bipolar Offset: ±5 ppm F.S.R./°C typical, ±10 ppm F.S.R./°C maximum.

Temperature: Rated for operation to 130°F.

Specifications: Model VIC4-20

Signal Input Voltage Range: 0 to 10 Volts.
Signal Output (for V supply = +15V) 4 to 20 mA with 0 to 500Ω maximum internal impedance.
Dynamic Response
Slew Rate: 2.5 mA/microsecond.
Settling Time: 24 microseconds for 10V step.

Power Supply: Standard +15V to +18V (IEEE 696/S-100), or +10V to +32V optional.
Temperature Range: −25°C to +85°C, rated conservatively at 0 to 70°C.
Non-Linearity: .025% Max.

DUAL SYSTEMS CORPORATION DUAL system reliability / system integrity

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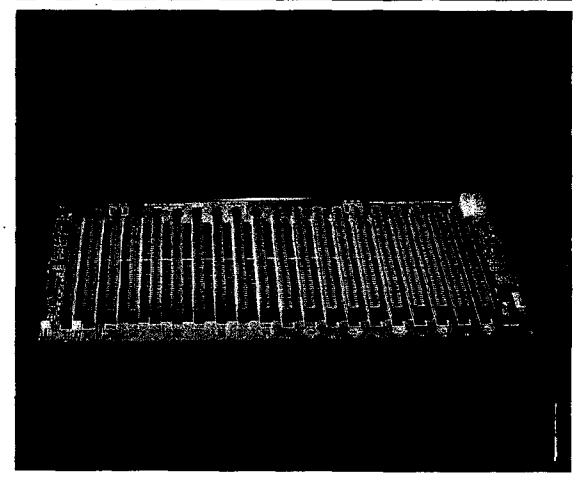
HIGH SPEED MULTILAYER BACK PLANES Models M/BD-15 & 20

15 and 20-SLOT BACK PLANES FOR IEEE-696/S-100 BOARDS

- ☐ Multilayer construction with two internal ground planes provides exceptionally low noise and true transmission line characteristics.
- ☐ Schottky diode termination on critical strobe lines prevents undershoot more effectively than conventional resistive termination.
- ☐ Very high quality, low inductance connectors used for low noise operation, durability under frequent insertions and high retention force.
- ☐ Board thickness of 0.093″ provides high rigidity.
- ☐ Fifteen or twenty IEEE 696/S-100 slots on 0.75″ centers with standard mounting holes.
- ☐ Pull-ups on tri-state and open collector lines to guarantee a default to logic 1 state.
- ☐ De-bounced $\overline{\text{RESET}}$ signal provided on board
- ☐ Useful front panel LED outputs provided on board. See specifications below.



Dual's motherboards feature ruggedness, long-term reliability and low-noise operation. Highest quality components are used throughout. Four-layer construction with two internal-ground planes and Schottky-diode termination on critical strobe lines make possible high speed operation with minimum noise.

SPECIFICATIONS

Power Input: +8V @ 30A MAX
+18V @ 5A
−18V @ 5A

Power Connector: AMP 350 219-1; mates with AMP 1-480285-0

De-Bounced $\overline{\text{RESET}}$: External momentary contact closure of two leads generates $\overline{\text{RESET}}$ on PIN 75 of all connectors. Two leads leave board through MOLEX 09-75-1021; mates with MOLEX 09-50-3021

Power-On Indication: External connection of LED to two leads provides power-on indication (tied to +8V supply). Two leads leave board through MOLEX 09-75-1021; mates with MOLEX 09-50-3021

System Status Indication: Six sets of two leads leave board through BERG 14-Pin Stick, Part Number 65507-414; mates with AMP 2-87499-1. Each set of leads attaches to external LED to indicate the following:
PIN 44 sMI (Instruction Fetch Cycles)
PIN 48 sHLTA (Status Halt Acknowledge)
PIN 72 $\overline{\text{RDY}}$ (Presence of Wait States)
PIN 74 $\overline{\text{HOLD}}$ (DMA in Progress)
PIN 76 sSYNC (CPU Run State)
+8V Power (Redundant to Separate Power-On Indication)

Control Lines using Schottky Diodes:
PIN 12 NMI*
PIN 24 Ø
PIN 25 pSTVAL*
PIN 26 pHDLA
PIN 49 CLOCK
PIN 68 MWRT
PIN 73 INT*
PIN 74 HOLD*
PIN 76 pSYNC
PIN 77 pWR*
PIN 78 pDBIN

Dimensions: M/B D-20: 16.81″ x 9.00″. Mechanically and electrically interchangeable with Godbout 20-slot M/B ASM with this exception: Godbout's connectors 1 and 2 are separated by 1.067″ and connectors 2 through 20 are separated by 0.75″; Dual's connectors 1 through 20 are separated by 0.75″. M/B D-15: 13.00″ x 9.00″

*Denotes active low signal per IEEE-696 specification.

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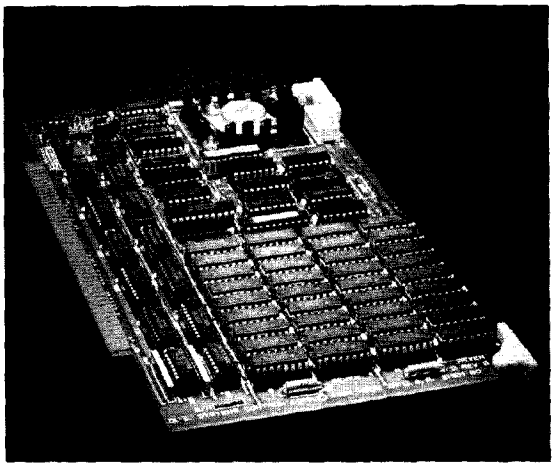
1 MEGABYTE OR 256K BYTE DYNAMIC RAM EACH WITH PARITY CHECKING

Models EMEM-1MB EMEM-256K

HIGHLY RELIABLE, HIGH-DENSITY DYNAMIC RAM IN TWO CAPACITIES ON STANDARD IEEE 696/S-100 BOARD WITH PARITY ERROR CHECKING AND 8- OR 16-BIT DATA PATHS.

- ☐ One megabyte on a single board: Model EMEM-1MB.
- ☐ Alternatively, 256K bytes on the same board: Model EMEM-256K.
- ☐ 8- or 16-bit data transfers as requested.
- ☐ Uses the IEEE 696/S-100 24-bit extended addressing.
- ☐ FAST: Runs at 6 MHz for both 8- and 16-bit systems.
- ☐ 220 nanosecond access time; 330 nanosecond cycle time. No S-100 wait states, except during refresh.
- ☐ Parity checking on each byte. Latched vectored interrupt can be enabled or disabled under software control.
- ☐ Indicator lights for activity (green) and error (red).
- ☐ Low power consumption — 10 watts nominal.
- ☐ Refresh maintained during processor reset.
- ☐ Rugged industrial board with 168-hour burn-in period with continuous testing.



As with all DUAL products, the EMEM is designed and constructed for extreme reliability. 100 percent dynamic burn-in for 168 hours at elevated temperatures is standard procedure for all of DUAL's boards.

The EMEM board is the highest density memory board available for the IEEE 696/S-100 bus. Its fully featured characteristics make it useable in both 8- and 16-bit systems. The DUAL SYSTEMS EMEM boards do not sacrifice performance for density. Each board runs at full speed in IEEE 696/S-100 systems up to 6 MHz (subject to the access time requirements of the system), with no wait states except during refresh. Refresh is maintained during processor reset.

Data integrity for each board is guaranteed with the added byte-parity check bit. Jumper selection is provided so that an error will cause any of the eight vectored interrupts, or non-maskable interrupts. The EMEM maintains even parity on even-numbered bytes and odd parity on odd-numbered bytes. Red and green LED indicators facilitate monitoring of operation. Each board is put through an intensive, computer-actuated testing procedure throughout burn-in and prior to shipment.

Nominal power consumption is 10 watts, assuring that the board will run at moderate temperatures and provide a large margin of safety.

Applications

The EMEM is an ideal companion for the DUAL CPU-68000 series of processor boards in any IEEE 696/S-100 compatible system.

The memory, with 24-bit extended addressing, can be used in any 8- or 16-bit system where large amounts of highly reliable dynamic memory are required.

Specifications

Bus Compatibility: Fully IEEE 696/S-100 compatible.

Access Time: 220 nanoseconds, pSTVAL to DI.

Cycle Time: 330 nanoseconds; requires 175 nanoseconds after end of strobe.

Wait States: 0 to 3 wait states inserted automatically during refresh.

Address Selection: By DIP switches to any 1M byte boundary for EMEM-1MB or any 256K byte boundary for EMEM-256KB.

Data Transfers: 8- or 16-bit. In 16-bit transfers, the standard configuration supports the IEEE standard with respect to odd- and even-numbered bytes.

Power: The +8V supply is regulated on board to +5V. Current at 1.33M fetches per second is 965 milliamperes typical, 1450 milliamperes maximum. Current with all references to other boards is 835 milliamperes typical, 1250 milliamperes maximum. No connection to +18V or −18V supplies.

Operating Temperature: 0 to 55 degrees Celsius.

Models and Capacities:

- ☐ EMEM-1MB: 1 megabyte (1,048,576 bytes = 524,288 words) with one parity bit per data byte.
- ☐ EMEM-256KB: 256 kilobytes (262,144 bytes = 131,072 words) with one parity bit per data byte.

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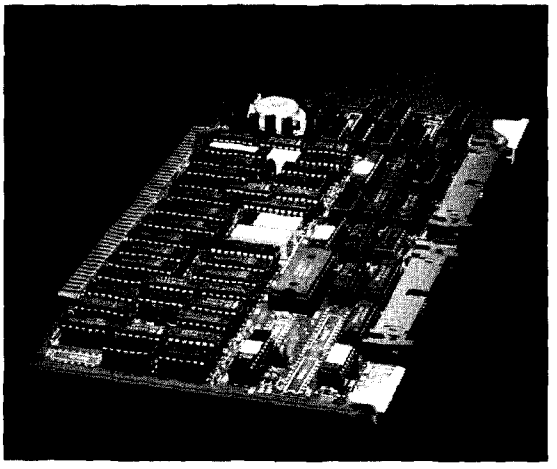
9-TRACK TAPE CONTROLLER WITH FIFO BUFFERING ON DMA TRANSFERS

Model TCON

NINE-TRACK TAPE CONTROLLER SUPPORTING INDUSTRY-STANDARD IBM-ANSI FORMATTER INTERFACE AND DMA ON READ AND WRITE.

- ☐ Standard IEEE 696/S-100 bus compatibility.
- ☐ Standard IBM-ANSI 9-track formatter interface.
- ☐ Performs DMA on read and write to tape.
- ☐ Uses the IEEE 696/S-100 full 24-bit addressing on DMA transfers.
- ☐ 8-bit data on DMA transfers.
- ☐ 8- or 16-bit I/O decoding, jumper selectable.



- ☐ 512-byte FIFO buffering of data on read and write to prevent overruns when DMA cycles are delayed due to bus contention.
- ☐ Simple-to-use control using 8 I/O ports (switch selectable).
- ☐ Supports Cipher Micro-streamer extended inter-record-gap option.
- ☐ Works in S-100 systems up to 6 MHz.
- ☐ Supports tape densities up to 6250 BPI.

The TCON is a board used to connect an S-100 system to a 9-track tape drive. Any tape drive using the IBM-ANSI 9-track formatter interface may be used. The primary design feature of the board is a 512-byte FIFO buffer that stores DMA data temporarily in the event of bus contention; the use of the buffer avoids loss of data during transfers in multi-user systems.

TCON adapts itself simply to a variety of tape drives. Tape speed (inches per second, or IPS) and density (bits per inch, or BPI) are user-selectable. TCON will operate with tape drives with speeds up to 100 IPS and tape densities of 6250 BPI. Data transfers are byte-wide. All TCONs receive 168 hours of burn-in at elevated temperatures and are checked in operation with a 9-track drive prior to shipment.

Specifications

Bus Compatibility: Meets all standards of the IEEE 696/S-100 bus.

Power: +8V supply is regulated on board to +5V. Maximum current drain is 1.8 amperes.

Address Selection: The I/O address is selected by DIP switches. A jumper option determines whether 8 or 16 bits of the I/O address will be decoded.

Tape Interface: The industry-standard IBM-ANSI tape formatter interface is supported. Tape densities up to 6250 BPI and tape speeds up to 100 IPS can be supported.

Mating Connectors: 3M 3425-600 or Winchester 61-1150-00 are suitable for connecting the TCON to a 50-conductor ribbon cable.

Data Transfer: Data is transferred on both read and write by DMA using full 24-bit extended addressing.

Data Buffering: Data transfers are buffered on both read and write by a 512-byte FIFO buffer which prevents overruns when DMA is delayed by bus contention.

Operating Temperature: 0 to 55 degrees Celsius.

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