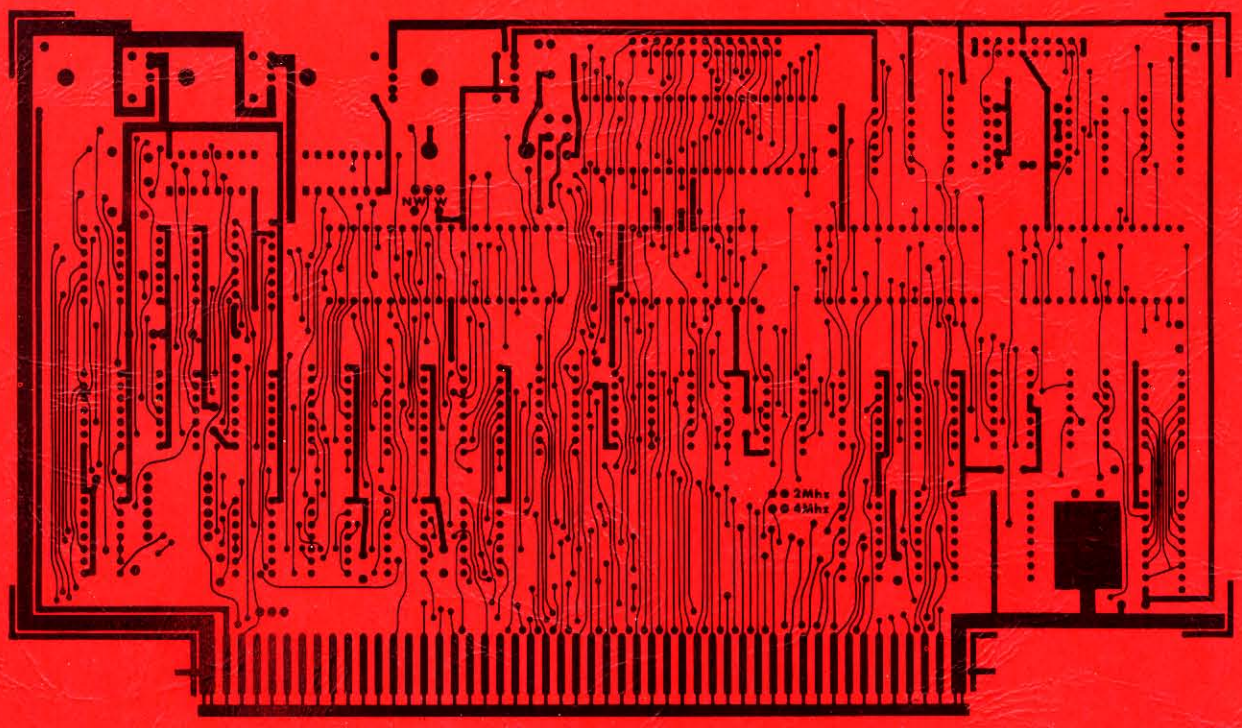
DP-CPU

OPERATION MANUAL



- 2 – 4 MHz JUMPER SELECT
- POWER ON JUMP TO EPROM
- 2 SERIAL 3 PARALLEL PORTS
- MEMORY MANAGEMENT ON A16 & A17
- M1 WAIT STATE OPTION
- INDEPENDENT BAUD RATES 50 to 19,600

DELTA PRODUCTS

15392 Assembly Ln.,
Huntington Beach,CA 92649
Tel: (714) 898-1492

DELTA

Telex: 681-367 DELTMAR HTBH

DEALER:

DELTA PRODUCTS DP-CPU-B ADDENDUM

As you will notice, DELTA PRODUCTS is in the process of changing our CPU design. The new product will be referred to as the DP-CPU-B.

Several changes in appearance will be noted. Please refer to the enclosed parts layout pictorial to orient yourself during the following paragraphs.

CHANGES THIS REV;

1. PROGRAMABLE BAUD RATE:

The 8116 can now be written into under software control of the Z-80 at Port 0BH to set the baud rate without removing the board from the computer. The lower 4 bits program the CPU-B serial channel A and the upper 4 bits program channel B. The old baud rate switch may be read through IO Port 0BH. The 1.83 DP monitor prom reads this 8 bit switch and loads the 8116 accordingly. Your boot or system initializations software may choose to use these 8 bits (or some part of them) to signal other things to the system.

2. POWER ON JUMPER DISABLE:

Jumper J9 when placed in the up position will cause the Z-80 to go to system RAM after a reset.

3. E PROM DISABLE:

Jumper J6 when placed in the left position will permnently disble the E Prom. When enabled the Prom may be used exactly as it has been in the past.

4. 2 MHZ/4 MHZ JUMPER:

The jumper (J2) enabling you to switch from 2 to 4 MHZ is now at the top of the board. See pictorial for new locations.

5. VECTORED INTERRUPT RESPONSE:

A header at the top of the board (11A) connects the various interrupt and timing capabilities of the Zilog CTC timer chip (11B) to their chosen destinations. Boards without a "B" designation on the back side of the board under the baud rate crystal do not have the CTC functions implimented yet and should be used as "A" boards as far as vectored interrupts or CTC functions are concerned.

6. IO PORT ADDRESSES:

The IO ports will be addressed at ports 0-F when Jumper J7 is in the right hand position, and 10H to 1FH when the Jumper is in the left hand position.

TABLE OF CONTENTS

An examination of any of these particular areas should answer most questions regarding the operation of the CPU.

If any additional questions should arise, please write the factory at:

DELTA PRODUCTS, INC.
15392 Assembly Ln.,
Huntington Beach,CA 92649
Tel: (714) 898-1492

Section 1.0

GENERAL DESCRIPTION

The DP CPU is a multipurpose control card designed to run on the S-100 buss with a minimum of additional circuitry.

The product was designed in 1977 and put into production with some modification in 1978. A typical business or personal computer system can be configured with only three cards and a motherboard.

1. DP CPU-A
   - Z80 Central Processor
   - 2 Serial Programmable RS-232 IO Ports
   - 1 8255 24 Bit Parallel IO Port
   - M1 Wait State for 160% thruput enhancement with 450ns memory
   - 2708 or 5 Volt 2716 Power on Jump Eprom
   - Memory Management on A16 & A17

2. DP 32K-A
   - 32K multi-addressable memory featuring additional address lines A16 & A17 for parallel or extended addressing to 256K

3. DP DSK-A
   - Single or double density floppy disk controller using WD-1791 LSI chip. Works with Shugart, Siemens, Calcomp, Persci, etc. single or double sided drives.

4. DP MTH-A
   - 10 Slot shielded S-100 motherboard. Measures 10 x 7.5 inches. Mounts on stand-offs or rails.

Section 2.0

SERIAL IO BAUD RATE SELECT

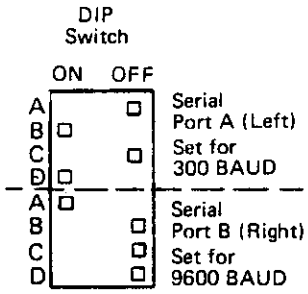
The ports for the Serial IO are: A Status = 1 A Data = Ø (on the left)
B Status = 3 B Data = 2 (on the right)

The 8 position DIP switch at the lower right hand corner of the board is broken into two 4 bit sections. The upper 4 bits select the IO baud for the left 8251 and the lower 4 bits select the baud for the right.

The switches are used in a binary pattern to set the rates as follows:

X = OFF O = ON

Baud	D	C	B	A
50	O	O	O	O
75	O	O	O	X
110	O	O	X	O
134.5	O	O	X	X
150	O	X	O	O
300	O	X	O	X
600	O	X	X	O



Baud	D	C	B	A	
1200	O	X	X	X	
1800	X	O	O	O	
2000	X	O	O	X	
2400	X	O	X	O	
3600	X	O	X	X	
4800	X	X	O	O	
7200	X	X	O	X	
9600	X	X	X	O	
19200	X	X	X	X	(Special Fast) (8251)

NOTE: Make sure when using the above chart that the positions we show correspond to the type of switch you have on the board. Some models of switches have the 'ON' to the opposite side.

The 8251 can be programmed under software control to do a number of things. A copy of the tech sheet on the chip can be found in the appendix. The following code can be used to initialize what might be a 'normal' mode for the 8251. (The chip must be initialized or it will do nothing.)

```
MVI A, ØAAH     ;Load A
OUT Ø3          ;Initialize Port B
OUT Ø1          ;Initialize Port A
MVI A, 40H      ;Load A
OUT Ø3          ;With Internal Reset
OUT Ø1          ;Write to Both Ports
```

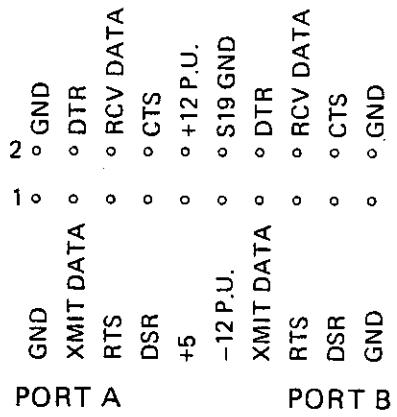
8251 Status Flags (when you input status port, this is what byte will mean):

Bit:	Ø7	Ø6	Ø5	Ø4	Ø3	Ø2	Ø1	Ø0	
	DSR	SY	FE	OE	PE	TXE	RXR	TXR	⇦ Output bit (RDY when Hi)
							⇧		Input bit (RDY when Hi)

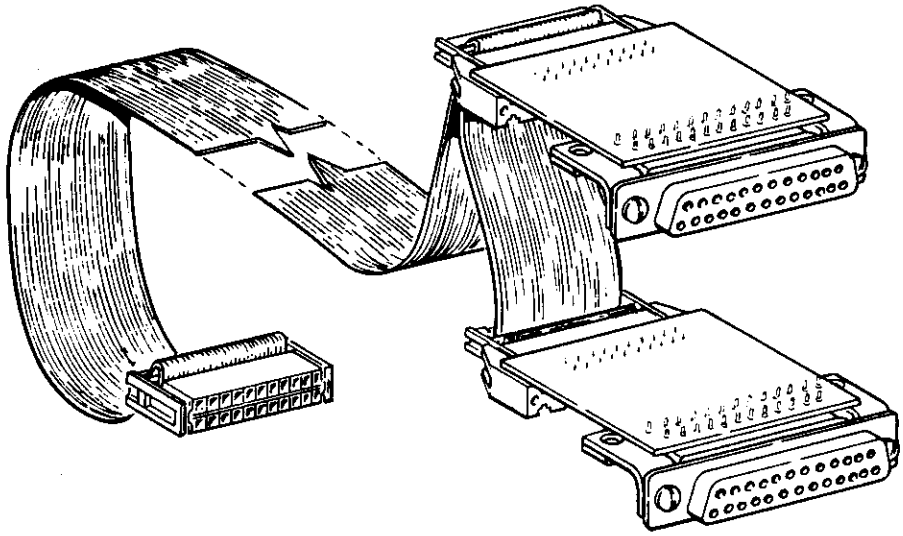
Section 2.2

PIN OUT OF SERIAL CONNECTOR

The pin out of the RS-232 connector (on the right) is as follows:



As an option we can supply a 26 pin ribbon connector with two connectors on one end and one on the other. When mated with a pair of our STOD PC boards a neat interface to a standard 'D' RS-232 connector (chassis mount) may be realized. The set up looks like this:



The cost of the above lash-up is $32.00. Sorry the price is high but if you will total the price on all the connectors (5) and the PC boards (2) plus the ribbon and labor, you will find it's the best that can be done.

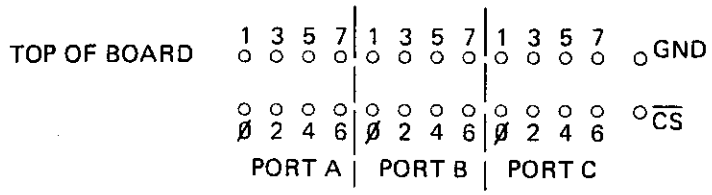
Section 3.0 and 3.2

PARALLEL INTERFACE AND PIN OUT OF PARALLEL CONNECTOR

Parallel 8255 IO Port.

The Ports decoded for operation are: Port A = Ø4H B = 05H C = 06H CMD = 07H

The Parallel 8255 pin-out is as follows:



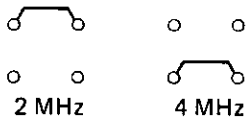
The 8255 chip tech sheet can be found in the appendix.

This chip is programmable in so many configurations that it is not possible to offer an adequate operational guide. Basically the device has three 8 bit ports, A, B, and C. A can be simultaneously input and output. B can be commanded to be an input or an output. C can be part in, part out or linked with A & B (4 bits each) for handshaking. We have included in the pinout the CS (chip select) line to the 8255. It may have some use in certain applications where buffers are remotely attached to the fairly weak output of the device.

Section 4.0

2 MHZ TO 4 MHZ JUMPER SELECT

The DP CPU will run at 2 MHz or 4 MHz, as selected by jumper J2. This jumper is to the right near the bottom of the board. Coordinates: 10-D

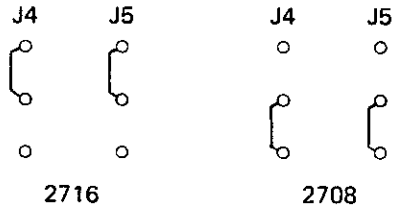


NOTE: The clock signal that appears on the bus is always 2 MHz, regardless of the speed at which the CPU is running.

Section 5.0

2716 TO 2708 EPROM SELECT

The DP Z80 CPU is designed for use with either a 2708 or a 5V only type of 2716 (Intel, Mostek). To select an Eprom move both jumpers J4 and J5 (near the top next to the 8255) to the upper position for a 2716 and to the lower position for a 2708.



The Eprom always occupies F800 – FFFF when enabled whether a 2708 or a 2716 is used.

If it is desired the DP CPU can be modified for use with the TI 2716 (+5V, -5V, +12V). The 2708/2716 jumpers should be in the 2708 position. Pins 18 and 20 are affected. Pin 18 is PD/PGM on the 5V part and CS on the TI part. Pin 20 is CS on the 5V part and A10 on the TI 2716. Therefore the following changes must be made on IC 8B.

From Pin	To Pin	
IC 8B 18	GND	Cut these traces at IC 8B
IC 8B 20	CS	
IC 8B 18	IC 9C p6	Install these jumpers on the back of the board
IC 8B 20	IC 5B p40	

Section 6.0

VECTORED INTERRUPT RESPONSE

The Z-80 CPU has three methods of responding to an interrupt. The DP CPU supports all three modes. They are: Model Ø, an instruction can be placed on the buss; Mode 1, restart to ØØ38H; Mode 2, upon initialization an upper page vector is loaded into the Z-80 I register. At interrupt response time, Z-80 will respond with an M1 + IOREQ (an impossible normal combination). At this time the lower page address (which will be added to the upper page previously stored in I register) should appear on the data buss. The Z-80 will use these two bytes to point to a software address where the address of the interrupt routine is to be found.

SECTION 7.0

POWER ON JUMP CIRCUIT

The DP CPU has an unusual and totally effective method of starting a computer after reset. Conceptually the 2708 or 2716 Eprom 'appears' at ØØØØH for the purpose of initializing the CPU. The Eprom may then be 'moved' to the last 2 K of ram and jumped to. What happens is the CPU executes a few instructions at ØØØØ, and jumps to itself at 62 K. It then does a 'read' of an IO port which changes the on-board addressing structure. After inputing port ØA the Eprom may only be read at F800, not every 2 K boundary as was the case before.

Here is some sample code that works:

```
ORGØF8ØØH

        JMP F803        ;These three bytes will be executed at ØØØØH
        IN ØAH          ;"Moves" Eprom, this is now F803
        MVI A, ØAAH     ;Load Accumulator
        OUT Ø3A         ;Initialize IO Port
                        ***JUMP TO RAM HERE***
        MVI A, Ø1H      ;Load Accumulator
        OUT Ø9H         ;Remove Eprom
```

The Eprom may be left in the computer memory space at 62 K at all times or removed by writing a Ø1H into IO Port 9. Writing a ØØH into IO Port 9 will bring it back. Ram and Eprom may exist simultaneously at either the initial ØØØØ reset location or at the subsequently directed F800 location. Memory writes or IO functions are not disturbed by the co-existence of the Eprom, only memory reads. By writing the correct code into Port 9, the Eprom may be toggled in and out disabling the ability to read from adjacent RAM.

The CPU is currently supplied without an Eprom to keep the cost low. If you should wish a program on a prom, we will burn one for a charge of $15.00 and supply the prom for an additional $10.00 (2708). We will type in up to 50 Bytes of code for this amount. Any size program will be burned providing it is supplied to us on a CPM compatible disk as a Hex file. We will guarantee the burn but you must guarantee the code.

To disable Power On Jump to Eprom:

> Cut the trace from IC 13C, p 13 to IC 10C, p 11 (as shown) and install a jumper from pin 13, IC13 to ground (pin 7 on 13). With this modification, the Eprom can still be accessed normally from F800H to FFFF Hex, and it can also be enabled through IO port ØA Hex.

Section 8.0

MEMORY MANAGEMENT CIRCUIT

Memory Management Lines A16 and A17.

The Proposed IEEE S-100 standard has assigned buss pins 16 and 17 to be extended address bits A16 and A17 respectively. The DP CPU has an on board IO latches decoded to enable setting these lines to enable parallel banks of memory.

The DP Mem 32K memory boards will respond to this type of memory management scheme enabling 256K to exist on any given S-100 buss with no conflict.

To set or reset the address lines A16 and A17 simply output the desired bit pattern on IO port ØØH. Bit Ø controls A16 and Bit 1 controls A17 and bits 2 through 7 are ignored.

Examples: To select the lowest 64K block of memory,

```
MVI A,ØØH
OUT ØØH        A16=Ø, A17=Ø
```

To select the highest 64K block of memory,

```
MVI A,Ø3H
OUT ØØH        A16=1, A17=1
```

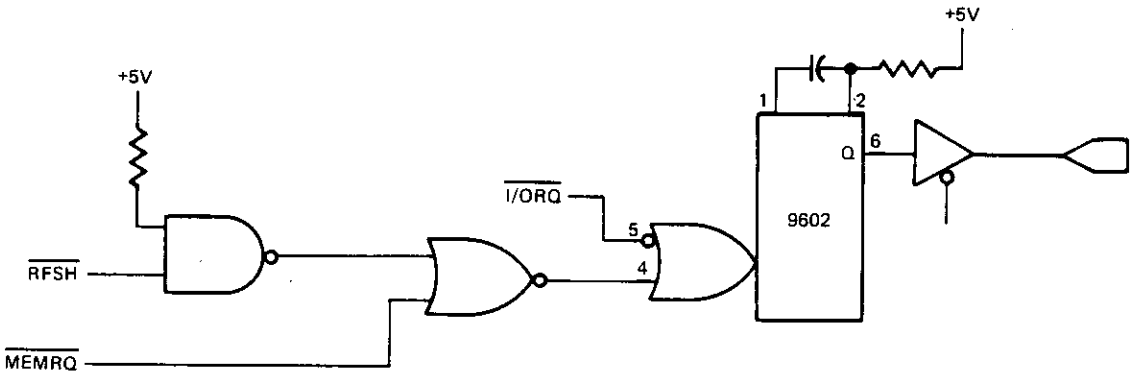
NOTE: A16 & A17 must be initialized in software to the desired levels after each system reset.

Section 9.0

P-SYNC GENERATOR

P-SYNC is a signal output by an 8080 to indicate that CPU status can be latched off the data bus.

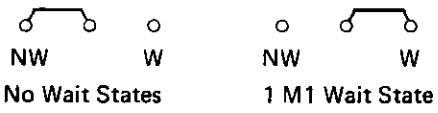
This signal is not produced on the Z80, and therefore must be simulated in order to make a CPU S-100 compatible. This is done as accurately as possible by generating a P-SYNC on every $\overline{MREQ}$ that is not a $\overline{RFSH}$ and on every I/O operation. This circuitry is provided on the DIR Z80 CPU.



Section 10.0

WAIT STATE ON M1 CIRCUIT

Jumper J1 allows the user to insert Ø or 1 wait state to each instruction fetch (M1) cycle. J1 is located in the left third of the board near the top.



To get the best system performance at a low cost, it is highly advisable to run the CPU at 4 MHz with 450ns memory and one M1 wait state. The M1 wait state adds only one clock cycle (250ns) to each instruction and the shortest instruction is four clock cycles long. Therefore, the worst case improvement in system throughput is 160%, with a typical speed improvement of about 180%.

Section 11.0

DELTA PRODUCTS MONITOR

Upon reset the CPU will initialize port IO Port 2 and sign on. It will start at ØØØØ, locate top of RAM and put its stack there. The DP monitor will respond to the following commands:

D = DUMP
Enter beginning address, ending address. A beginning address and a 'CR' will display 15 lines automatically. A 'CR' for a beginning address will enter ØØØØ.

L = LOAD
Enter beginning address. 'CR' steps through memory. A '.' (period) stops entry.

M = MOVE
Enter source address, destination address, block length in Hex.

F = FILL
Enter starting address, ending address, character to fill.

V = VIEW
ASCII Dump to Monitor. + up one line, - down one line, 'CR' = 512 Bytes, Space bar = out.

G = GO
Enter destination address.

H = HEX STRING LOCATE
Enter starting address, ending address, string to locate.

SPECIALS: (* = not in 2708 [1K] version)

* R = READ
Cassette, Tarbell format. Enter destination address, block length in 1/4 K (255 Byte) segments. Will report "E" if checksum error.

* W = WRITE
Write to cassette, Tarbell format. Enter source address, block length in 1/4 K (255 Byte) segments. "W" will appear after write.

Control 'C' will execute Tarbell type floppy disc boot routine. Failure to boot will fall into trace function with error code in register A. (1 K version will report only 1771 error.)

* TRACE TYPE register dump may be enabled by placing a JMP to F815 (C3 15 F8) at 0038. Place a FF at the location in the program where the break-point is desired. In the act of executing a RST (ØFFH) the CPU will push the current program counter onto the stack. It will be recovered by the trace routine and printed on the screen.

The following is an Entry jump table at the beginning of the prom:

```
F800  C3 XX XX  JMP MONINZ   ;INITIALIZE ROUTINE
F803  C3 XX XX  JMP MONTR    ;MONITOR W/O INIZ
F806  C3 XX XX  JMP CONIN    ;CONSOLE INPUT ROUTINE
F809  C3 XX XX  JMP CONOUT   ;CONSOLE OUTPUT ROUTINE
F80C  C3 XX XX  JMP LIST     ;PRINTER DRIVER
F80F  C3 XX XX  JMP CASIN    ;TARBELL CASSETTE
F812  C3 XX XX  JMP CASOUT   ;TARBELL CASSETTE
F815  C3 XX XX  JMP TRACE    ;TRACE OUTPUTS REGS ON SCREEN
F818  C3 XX XX  JMP CONST    ;KEYBOARD STATUS
F81B  C3 XX XX  JMP INHX     ;HEX INPUT TO BINARY [A REG]
F81E  C3 XX XX  JMP OUTHX    ;BINARY TO HEX OUTPUT [B REG]
F821  C3 XX XX  JMP INADR    ;2 HEX BYTES TO BINARY [H&L]
F824  C3 XX XX  JMP ADOUT    ;ADDRESS TO CONOUT [H&L]
```

Note:

Version 1.82 and later of the DP monitor will sign on with a Hex address on the last line.

This is where the monitor has put its stack. If this address is less than the top of your current memory size, the monitor has encountered an error at that location. The monitor reads a Byte starting at Zero, compliments it, writes it out, reads it and compares it to what it wrote, if same it writes original byte back and goes on. When it detects write errors it puts its stack there, assuming it has found the top of Ram.

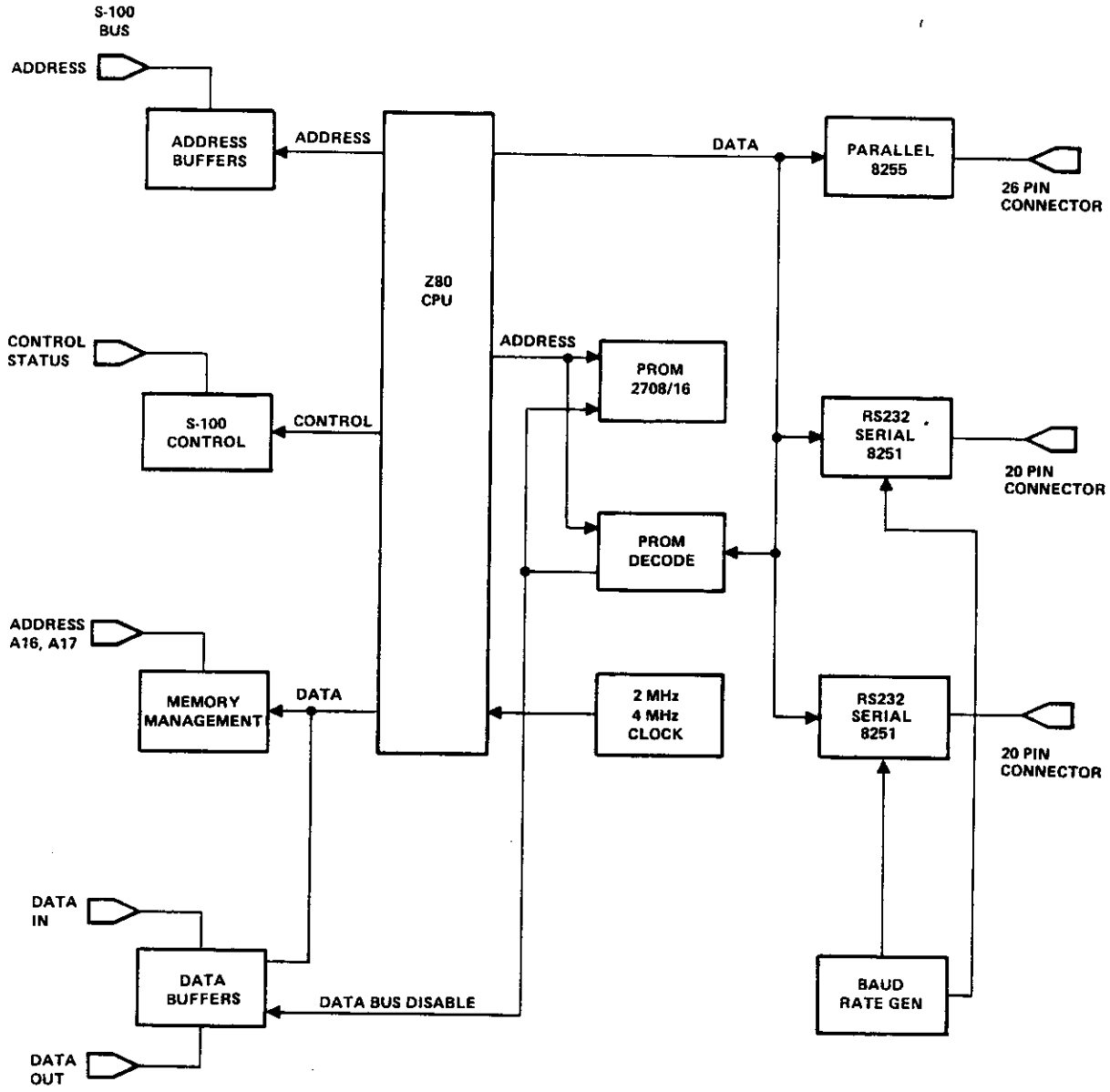
Filling memory with 55 Hex or AA Hex and resetting will do a quick and dirty alternate bit memory test.

Version 1.83 in later will output a constant string of Asterisks if it can find no memory.

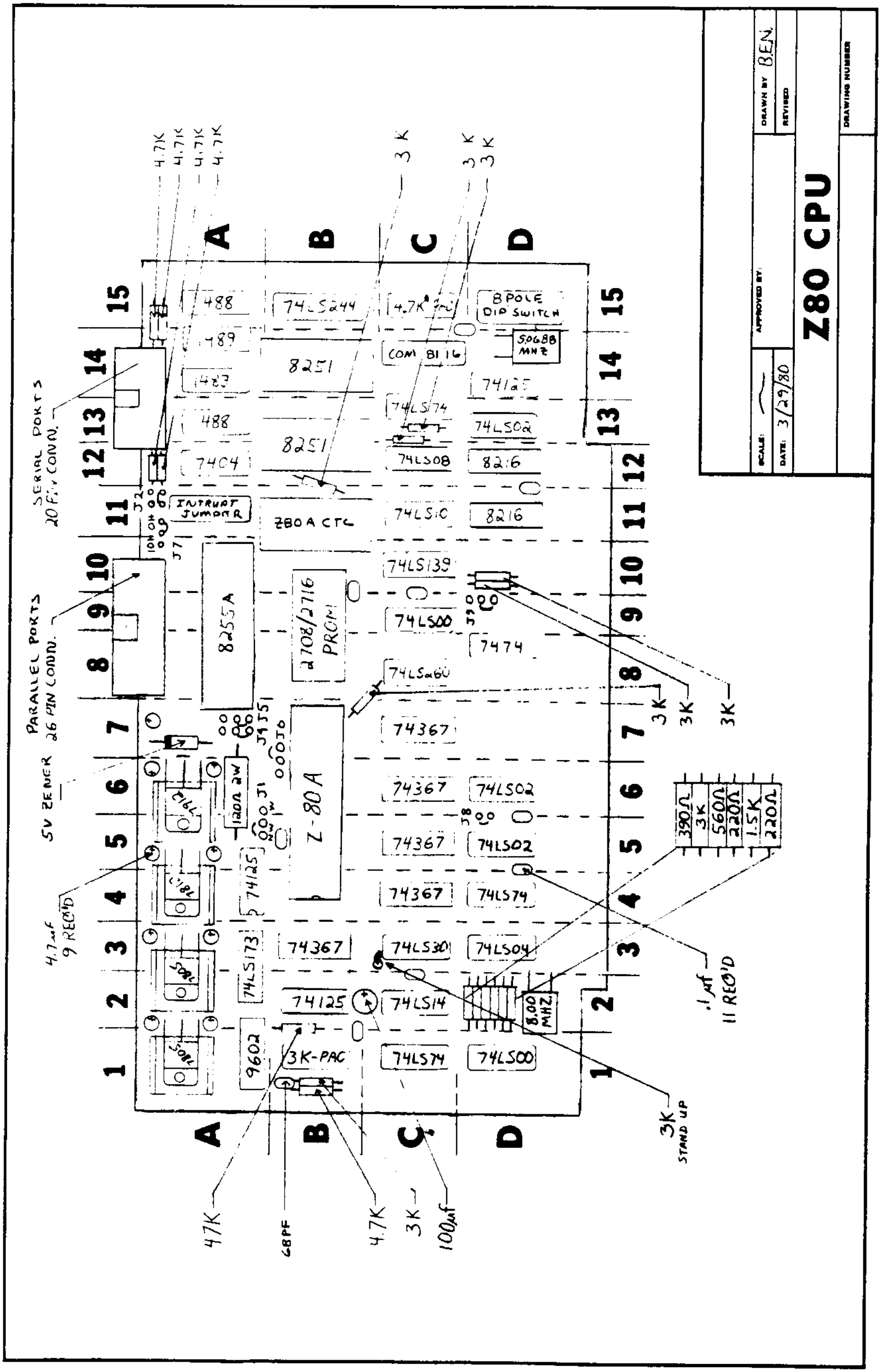
Section 12.0

DEDICATED ON BOARD IO PORTS

Port	Function	R/W
0	UART A, Data	(RW)
1	UART A, Status, CMD	(RW)
2	UART B, Data	(RW)
3	UART B, Status, CMD	(RW)
4	8255 A	(RW)
5	8255 B	(RW)
6	8255 C	(RW)
7	8255 CMD	(W)
8	Memory Management	(W)
9	Enable/Disable Prom	(RW)
A	Reset Address Decode	(RW)
B-F	(Unavailable to off board use)	

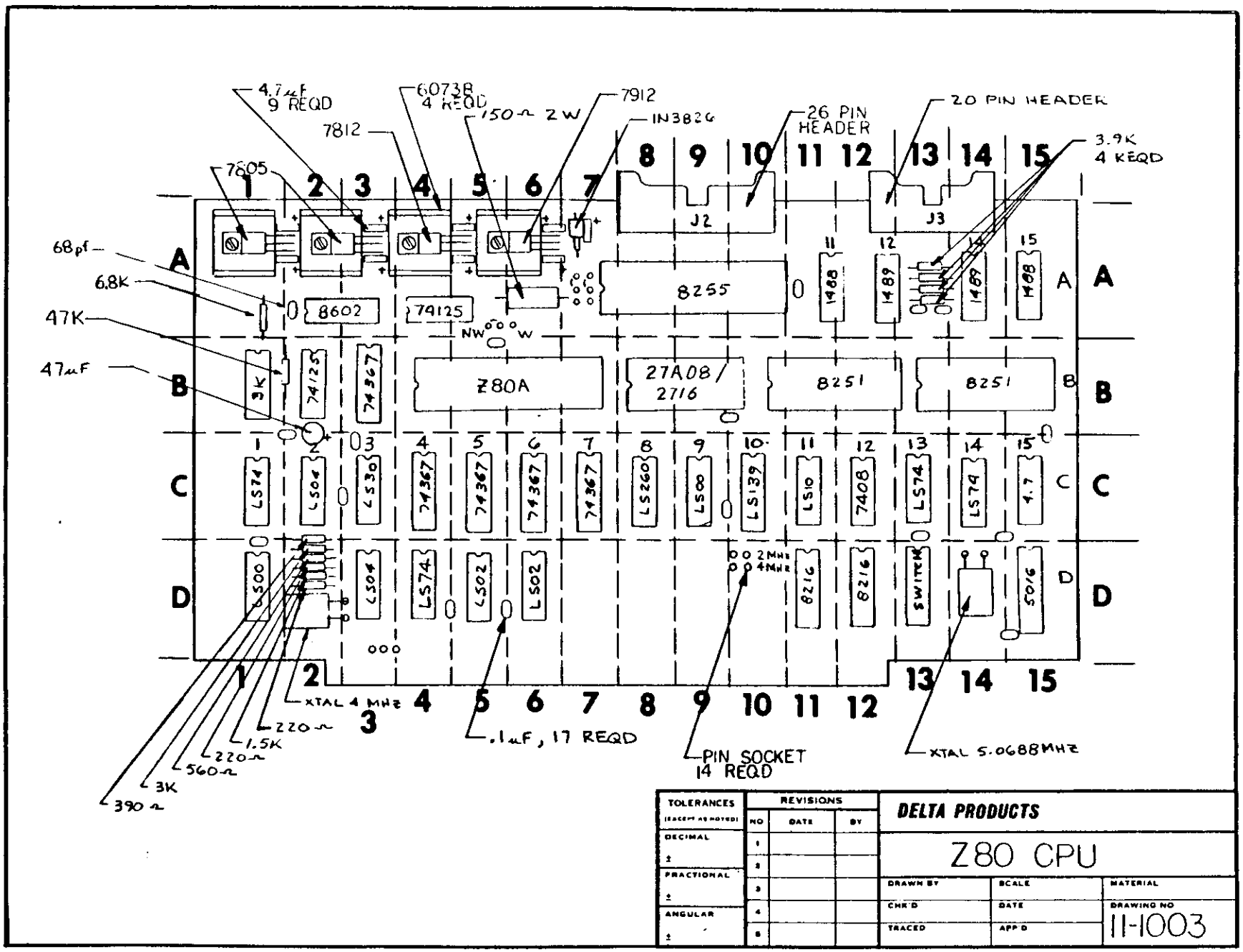


BLOCK DIAGRAM

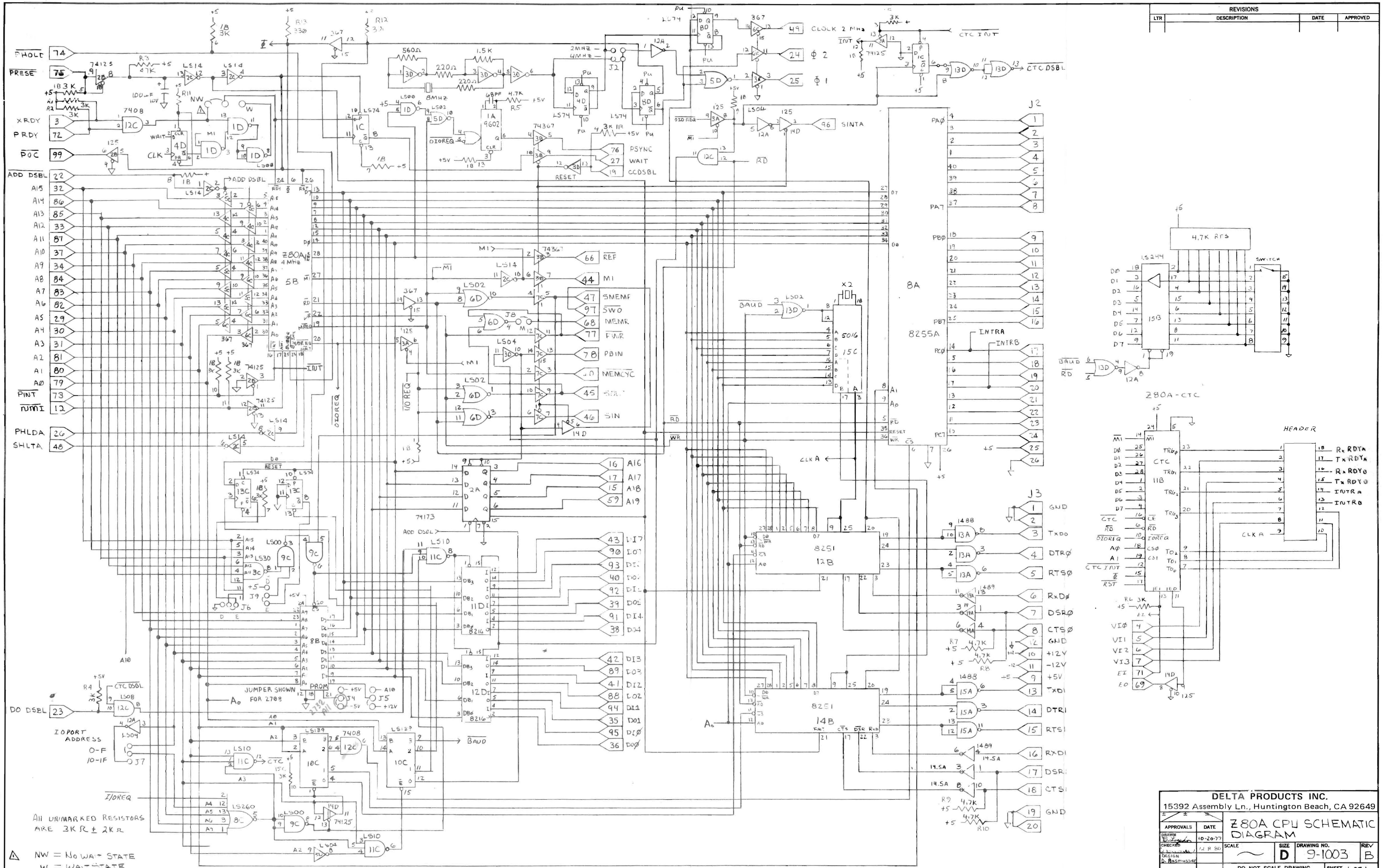

Z80 CPU
DRAWN BY BEN
REVISED
APPROVED BY:
SCALE:
DATE: 3/29/80
DRAWING NUMBER
SERIAL PORTS 20 PIN CONN.
PARALLEL PORTS 26 PIN CONN.
5V ZENER
4.7uf 9 REQ'D
.1uf 11 REQ'D
3K STAND UP
47K
68PF
4.7K
3K
100uf
4.7K
3K
488
489
74LS244
8251
8251
4.7K
COM 8116
8 POLE DIP SWITCH
5.0688 MHZ
74125
74LS74
74LS02
7404
74LS08
8216
INTRUPT JUMPER
Z80A CTC
74LS10
8216
74LS139
8255A
2708/2716 PROM
74LS00
7474
74LS260
74367
74367
74LS02
Z-80A
74367
74LS02
74125
74367
74LS74
74LS173
74367
74LS30
74LS04
74125
74LS14
8.00 MHZ
9602
3K-PAC
74LS74
74LS00
120Ω 2W
390Ω
3K
560Ω
220Ω
1.5K
220Ω
A
B
C
D
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

Z80 CPU PARTS LIST

PART NO.	DESCRIPTION	QTY	LOCATING COORDINATES
CP100	BOARD	1	
8251	IC	2	B11-15
8255	IC	1	A8-10
Z80A	IC	1	B4-7
STD4	4MHZXTAL	1	D2
STD506	XTAL	1	D14
6073B	HEATSINK	4	A1-6
7805	REG	2	A1-2
7812	REG	1	A4
7912	REG	1	A6
609-2002	ANSLEY	1	A13
609-2602	ANSLEY	1	A9
341808	SWITCH	1	D13
950CP	PIN	7	
3.9KRES	RES	4	A13
.1BYCAP	CAP	17	D5
475MT	TANT	9	A1-7
150-2RES	RES	1	A6
47KRES	RES	1	B2
390RES	RES	1	D2
3KRES	RES	1	D2
560RES	RES	1	D2
220RES	RES	2	D2
1.5KRES	RES	1	D2
19620	TANTCAP	1	B2
440SCR	SCREW	4	A1-4
440NUT	NUT	4	A1-4
1N3826	DIODE	1	A7
314A302	RPAK	1	B1
314A472	RPAK	1	C15
COM5016	IC	1	D15
8216	IC	2	D11,12
7404	IC	1	D3
7402	IC	2	D5,D6
74LS74	IC	3	C1,C13,C14
74LS00	IC	2	D1,C9
7408	IC	1	C12
74LS10	IC	1	C11
74LS139	IC	1	C10
74LS260	IC	1	C8
74367	IC	5	B3,C4-7
7430	IC	1	C3
74LS14	IC	1	C2
74125	IC	2	A4,B2
MC1488	IC	2	A11,15
MC1489	IC	2	A12,14
40PSOC	SOCKET	1	
28PSOC	SOCKET	2	
16PSOC	SOCKET	9	
24PSOC	SOCKET	1	
14PSOC	SOCKET	22	
18PSOC	SOCKET	1	
8602	IC	1	A2
7474	IC	1	D4
929834-01R	1X36 AP	1	
4.7KRES	RES	1	A1
CK68PF	CAP	1	A2



PARTS LAYOUT



12/80 Form#S-100CPU

APPENDIX A

Insert here

Intel 8251A/S2657

Programmable Communications Interface

APPENDIX B

Insert here

Intel 8255A/8255A-5

Programmable Peripheral Interface

15392 ASSEMBLY LANE., HUNTINGTON BEACH, CA 92649
(714) 898-1492 TELEX: 881-367 DELTMAR HTBH