# UNIVERSAL FLOPPY DISK CONTROLLER
# UFDC-1

## TECHNICAL INFORMATION
## AND
## USER MANUAL

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# SECTION I

## FUNCTIONAL DESCRIPTION

### GENERAL

The UFDC-I interfaces to the IEEE/696 S-100 bus and provides for connecting up to four floppy disk drives. The drives may be any combination of 51/4 and 8 inch drives with ANSI standard interfaces. Single or double density and single or double sided drives are supported as well. Figure 1 is a block diagram of the UFDC-I. The UFDC-I utilizes the Western Digital 1795 Floppy Disk Controller chip.

The UFDC-I synchronizes the processor to disk data transfers by means of wait states. When the data register of the 1795 is addressed by the CPU (detected by I/O port decode) the CPU is put into a wait state until the UFDC-I signals that it is ready for a data transfer. The 1795 contains a control/status register, a track register, and a sector register in addition to the read/write data register. It performs the functions associated with reading and writing bit serial data on the floppy disk drives. The 1795 also performs functions associated with positioning the disk heads and locating data sectors on the disk and also provides for formatting blank disks.

The UFDC-I contains an external control port and a status port. The control port is used to activate the drive select logic, to select a drive for access by the 1795. The density and disk side are also selected by the control port. The control port can enable or disable the wait state circuitry. The status port provides information about the disk drives to the system. Option jumpers are included to describe the physical characteristics of each selected disk drive. The option jumpers for the drive selected by the control port will be visable at the status port. The jumpers indicate if the drive is 5 1/4 or 8 inch, and indicates the step rate value for head movement on that drive. Additional signals are provided to indicate drive and 1795 interface status.

The UFDC-I uses all digital data circuitry for write pre-compensation and read data separation. A synchronous clock distribution scheme is used so that the 1795 and all data circuitry clocks are derived from the same source. The clock used by the 1795 and the data separator will be determined by the 5/8 option jumper for the selected drive, and by the single/double density signal from the control port.

It is recommended that you read this manual through once to becomefamiliar with the product and its capability before trying to install it.

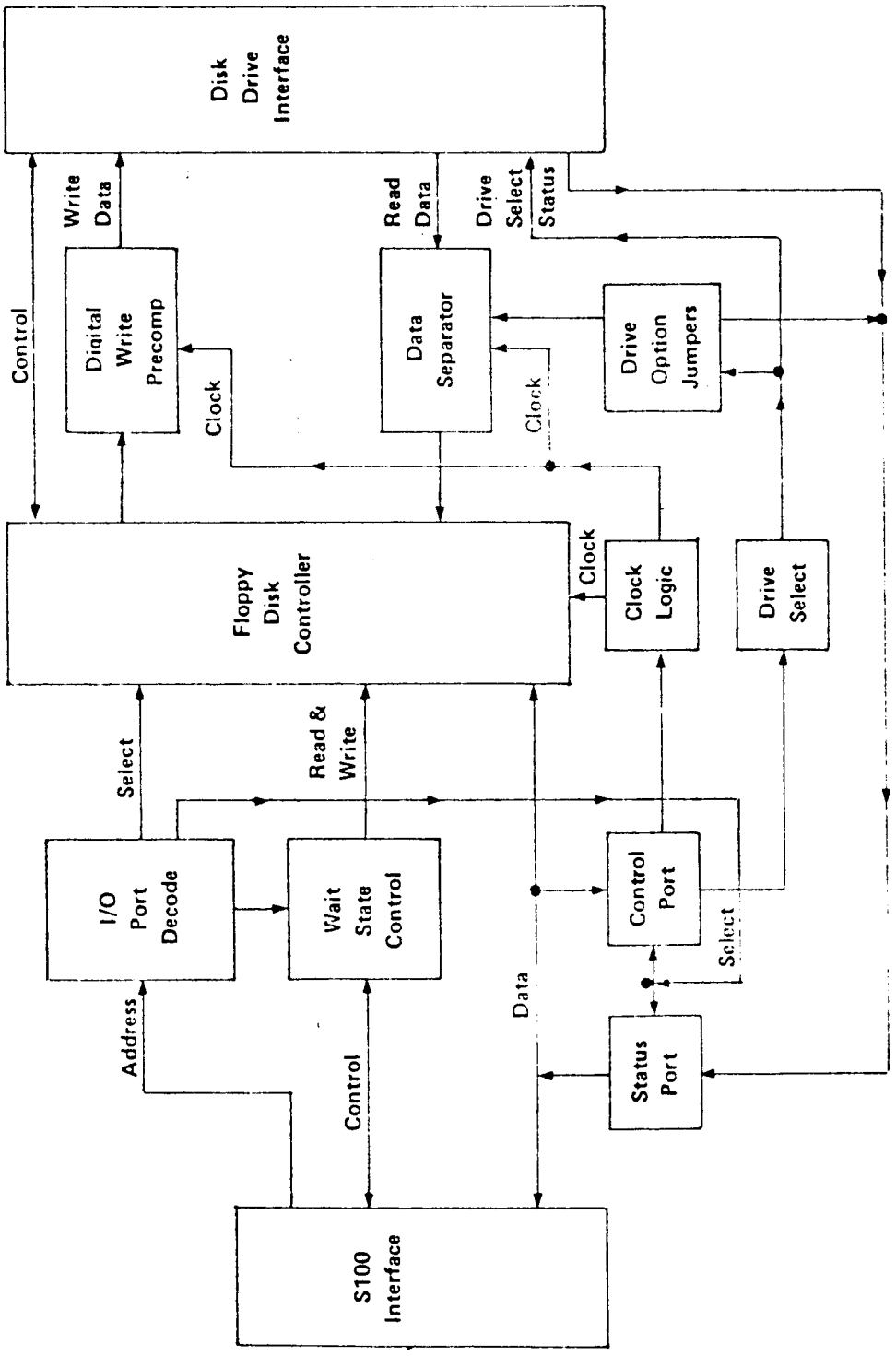


Figure 1. UFDC-I Block Diagram

# SECTION II

## SYSTEM MONITOR/BIOS

### INTRODUCTION

Provided with the UFDC-I is a 8" CP/M compatable, single density floppy disk. This disk contains the following programs:

| PROGRAM | SOURCE | OBJECT |
|---|---|---|
| Monitor/BIOS | CTVIII.ASM | |
| Disk formatter | FMTIII.ASM | FMTIII.COM |

These programs are written in TDL Z80 CP/M Disk Assembler Version 2.21.They can be modified to work with other Z80 assemblers.The source code listing of the MONITOR/BIOS is provided in Appendix B.

Our goal when writting the MONITOR/BIOS was to contain it to 2K of memory. This allows the MONITOR/BIOS to reside in a 2716 type EPROM compatable with many CPU boards including our SBC880 Z80 processor board. The code as written contains Z80 operators and will not run with 8080 processor boards. To do so would require modification and possibly additional memory space.

The MONITOR/BIOS has vectors set to work with SBC880 CPU board options. If you are using another CPU board, the terminal and printer routines would most likley have to be modified. The printer routine was written for a Centronic parallel interface.

The CP/M BIOS routine contains all required code for single/double density operation. It also includes deblocking routines for sector sizes of 256, 512, and 1024 bytes.

The BIOS assumes that an EPROM will be used to contain its code, therefore, the cold boot loader function has been placed in the BIOS code. The disk sector normally required by CP/M to contained this code is not needed. This sector will now contain a set of tables (placed there by the disk format program FMTIII) that will allow a great deal of flexability in reading different IBM 3740 soft sectored formats without modifying the BIOS routines. Disks created on other systems can be read in two ways:

1. A set of tables can be written on the disk using the format program (FMTIII). Note that if a cold boot loader was on that disk it will be destroyed when the tables are written to the disk.

2. A disk with a set of tables already written on it can be logged on the drive. Then the disk can be replaced with the one that is to read. Note that CP/M will not allow you to write on this disk.

The format program can be modified to write formats other

than those contained in the program. The following formats are currently available:

5 1/4" drive 40 track single density single side.
5 1/4" drive 40 track double density single side.
5 1/4" drive 35 track single density single side.
5 1/4" drive 35 track double density single side.
51/4"drive 96 track double density double side 512bytes per sector.
8 inch drive single density single side.
8 inch drive double density single side.
8 inch drive double density double side.

The MONITOR/BIOS and the UFDC-I were designed with flexability in mind. Flexability in adding and deleting different drive types (5 1/4 and 8 inch), and drives with different step rates without having to change the software BIOS each time. Flexability also in being able to read and write different IBM standard formats from other systems.

As you learn more about the MONITOR/BIOS and the UFDC-I you will see the value in the approach that was taken. There are however, limitations bounded by the capabilities of the WD 1795 controller and the IBM 3740 and System 34 disk formats.

## CAPABILITIES

The MONITOR/BIOS was designed to be a ROM based MONITOR/BIOS that supports the following features:

1. Built in diagnostics.
2. Mixed disk drive types (any combination of up to four 8" or 5 1/4" drives).
3. Mixed format types:
   Single or double density
   Sector size of 128, 256, or 1024 bytes.
4. Supports 2.2 CP/M with 64K of RAM.
5. Generation of system disks.
6. No cold start loader required (system boot is contained in ROM.
7. Fast system boot (uses multipal sector reads and does not load BIOS code).
8. Complete BIOS in ROM (all I/O drivers usable at power-on and do not have to be booted).
9. Efficient deblocking routines perform full sector access look-ahead to prevent unecessary pre-read operations.

The MONITOR/BIOS requires the first track (track 0) of all disks used to be formatted in single density 128 byte sectors (18 sectors for 5 1/4" disk and 26 sectors for 8" disk). The first sector (sector 1) must contain disk drive tables for use by CP/M and the MONITOR/BIOS. The tables are placed on the disk by the format program FMTIII.COM provided on the SYSTEM disk. The format of these tables are defined as follows:

| BYTE NO | DESCRIPTION |
|---|---|
| 0 & 1 | CP/M sectors per track(CP/M sector = 128 bytes) |
| 2 | CP/M block shift factor |
| 3 | CP/M block mask |
| 4 | CP/M extent mask |
| 5 & 6 | CP/M blocks per disk |
| 7 & 8 | Number of CP/M directory entries |
| 9 | CP/M allocation vector 0 |
| 10 | CP/M allocation vector 1 |
| 11 & 12 | CP/M directory check vector size |
| 13 & 14 | CP/M system track offset |
| 15&16 | Bytes per physical sector (used by MONITOR/BIOS) |
| 17 | Tracks per disk (used by MONITOR/BIOS) |
| 18 | Bit 7 - 1 = Double density<br>0 = single density<br>Bit 2 - 1 = Hard sector<br>0 = Soft sector<br>Bit 1 - 1 = Double side<br>0 = Single side<br>Bit 0 - 1 = 8" disk<br>0 = 5 1/4" disk |
| 19 | Physical sectors on one side of track. (used by MONITOR/BIOS) |
| 20 - 127 | CP/M sector translation table (used by MONITOR). Sector addresses 1 thru 127 equal side 0 of track. Sector addresses 129 thru 255 equal side 1 of track. Sector addresses 0 and 128 are invalid and should not be used. |

For detailed information on individual table items refer to your CP/M manual.

The MONITOR/BIOS as written has been configured to run from the on-board EPROM (2716 type) of the COMPUTIME SBC880 CPU board in a 64k RAM system. If you are using the SBC880 the switches should be set as follows: Switch 6 of SW3 should be ON and switches 1, 2, 3, 4, and 5 of SW3 should be OFF. Switches 2, 4, and 5 of SW1 should be ON and switches 1, 3, and 6 of SW1 should be OFF. Switches 1, 2, 3, 4, 5, and 6 of SW2 should be ON to select the on-board RAM to start at address zero. A 9600 baud RS232 terminal is required by the MONITOR and should be connected to connector J1.

The MONITOR/BIOS when used with a SBC880 CPU board and terminal is all that is required for operation of the MONITOR/BIOS, and may be used to diagnose problems on other boards in the system.

Diagnostic routines are provided in the MONITOR/BIOS for the purpose of debugging the controller and the disk drives used in your system. The MONITOR/BIOS will abort disk commands when a non

recoverable error condition is detected. Disk reads and writes will be tried 10 times before an error is reported. A disk error abort, results in the disk parameters being displayed on the terminal. The disk parameters consist of the current disk, track, sector, last command issued, and the last results obtained from the UFDC-I.

With the power-on jump option enabled on the CPU board the MONITOR/BIOS will be executed when the system is powered up. It will be re-initialized each time the system is reset. The MONITOR/BIOS prompts for input from the console by displaying "/" on the terminal. Input errors are indicated by displaying "*" on the terminal. All MONITOR/BIOS commands are entered as a single upper case letter followed by parameters as required by the commands. Command entry is terminated by entering a return. When the designated command has completed the MONITOR/BIOS displays the input prompt "/'. The S, B, L, & P commands perform functions prior to a return being entered. All other commands wait for additional input before attempting execution.

Parameters are entered as hexadecimal values using the ASCII characters 0,1,2,3,4,5,6,7,8,9,A,B,C,D,E, and F. Parameters are separated by commas or spaces.

Following is a list of commands:

A — Assign and select a disk drive for use
SAMPLE A0

B — Boot CPM
SAMPLE B

D — Display contents of memory in HEX & ASCII
SAMPLE D200,300

F — Fill memory with a constant value
SAMPLE F100,400,FF

G — GOTO user program
SAMPLE G100

I — Input from an I/O port
SAMPLE I2C

J — Destructive memory test
SAMPLE J400,C000

L — Load track data to RAM
SAMPLE L1000

M — Move block of memory
SAMPLE MF000,F800,1000

O — Output to I/O port
SAMPLE O2C,55

P Show value of disk parameters
SAMPLE P

S Substitute or examine memory
SAMPLE S100

T Seek a track
SAMPLE T3

V Verify memory against memory
SAMPLE VF000,F400,1000

## DETAILED COMMAND DESCRIPTION

A. This command assigns a disk drive for use by the "T" and "L" commands of the MONITOR. The command "A0" would select disk drive 0 (A for CPM) to be active for MONITOR usage. The B command automatically select drive 0 and ignores anypreviously entered "A" command.

B. This command will load the system portion of CPM from the disk into memory and then transfer BIOS vectors to memory that point to the MONITOR I/O routines. All the 2.2 CPM disk tables and scratch RAM areas are defined to allow operation with 8", and/or 5 1/4" single/double density, single sided disk. Up to 4 drives are allowed. Once CPM is set up in memory it wil be executed and will sign on with the CPM prompt "A>". This command does an automatic selection of drive "0" before booting CPM. Once CPM is entered the MONITOR can only be reactivated by pressing the system RESET switch or by powering off and on again. The command "B" when entered with a CPM system disk in drive "0" will cause CPM to be booted and sign on with "A>".

D. This command accepts a start and end address as parameters. The contents of memory from the start address up to the end address will be displayed in hexadecimal and ASCII on the terminal device. The command D100 200 would cause the contents of memory from 100 through 200 to be displayed on the terminal. The start and end address will be adjusted to the nearest 16 byte boundry that includes the requested memory range. For example, the command D10F,1F1 would display memory from 100 TO 200.

F. This command accepts a start address, end address, and a data value as parameters. The data value will be written to memory at the start address through the end address. The command F100,200,55 would fill the memory starting at address 100 through address 200 with the data pattern 55.

G. This command will accept a branch address. The command G100 would jump the processor to address 100 and begin execution of the program at that point.

I. This command accepts an I/O port address and displays the result of an input from the designated port. The command I2C

would display the result of an input instruction at I/O port address 2C.

J. This command accepts a start address and an end address as input parameters and tests the memory starting at the start address through the end address. The command J0,BFFF will test memory at address 0 through BFFF. Testing of memory will continue until the command is aborted. Pressing any input key on the terminal device will abort the command. The memory test performed is destructive, however, the stack and MONITOR storage memory may be overwritten without affecting operation of the test portion of the routine. The stack is only used by the routine while it is displaying a detected error. The address of the error is displayed followed by the expected data contents and the actual data contents. Testing will resume after an error is reported. A tally is incremented after each pass through the memory. The data pattern is formed by an exclusive OR of the tally and the upper and lower bytes of the current memory address. A complete write of the data pattern is performed followed by a READ/VERIFY test for each pass through the memory.

L. This command reads the current track from the currently active disk drive and includes all gap, address an data marks, ID fields, data fields, and CRC characters. It is primarily intended for use as a diagnostic tool. An input parameter is accepted to define the starting memory address to place the track data. The data may be scanned by using the "D" command. The command L1000 would read the current track from the currently assigned disk to memory starting at memory address 1000. If a disk is not active or the disk is not ready, the command will do an error abort and display the disk parameters. A disk may be selected for use by using the "A" command. A track is selected by using the "T" command. This command reads both sides of a double sided disk. Side 0 of track is read first and followed by a read of side 1. The entire track or cylinder is read into memory.

M This command accepts three parameters. The start address of the source data to be moved is entered first followed by the ending address of the source data to be moved. The third parameter is the start address of the destination for the data block being moved. The MONITOR will begin moving data from the starting source address to the starting destination address and the addresses will be incremented as each byte of data is moved from the source to the destination. This process will continue until the end address of the source data is reached. The command M100,200,400 will move the block of data at address 100 through 200 to address 400 through 500.

O. This command accepts an I/O port address and a data byte. The command will cause the data value to be output to the designated I/O address. The command O2C,55 would output the value 55 to I/O port address 2C. The maximum data value is FF.

P. This command will display all disk parameter information. This information is also displayed anytime A disk error is

detected when attempting to execute a command that uses disk. The command "P" would cause the MONITOR to display the current disk drive track, sector, last command issued, and the last results obtained from the controller.

S. This command accepts a memory address as a parameter. The MONITOR will display the data contained at that address if the space bar or comma is pressed on the terminal device. Successive memory locations may be displayed by continually pressing the space bar or comma. If data is entered on the keyboard after displaying amemory location, that data will be written to the location just displayed when the space bar or comma is pressed. The contents of the next location is displayed after the old location is rewritten. The command is terminated by entering a return. The command S100 would display the contents of the memory at address 100 when the space bar or comma is pressed. The contents of this location could be modified by typing data at this time followed by pressing the space bar or comma. Entering a return would terminate the command.

T. This command accepts a parameter to determine which track to seek on the disk. The command T4C will cause a seek to track 4C. The desired drive must be selected and a properly formatted disk in the drive or a disk error abort will occur. A drive is selected by using the "A" command.

V. This command accepts three parameters. The start address of the first memory block and the end address of the first memory block are followed by the start address of a second memory block. The two memory blocks are compared to one another and any differences are displayed on the terminal. No display would indicate that the two blocks of data contained identical data. The command V100,200,300 would compare the block of data from 100 to 200 to the block of data at 300 to 400. Any differences would be displayed on the terminal.

## OPERATING HINTS

All MONITOR command entries are terminated by entering a carriage return. If an entry error occurs you will be notified by a "*" being displayed. The "/" prompt from the MONITOR must be present before the MONITOR will accept commands to be executed. If you make an error entering a command just re-enter it correctly after the "*" is displayed. All the command parameters are entered as hexadecimal values with a maximum value of FF for an 8 bit value and FFFF for a 16 bit value. If more hexadecimal numbers than needed are entered the MONITOR will accept the last ones entered and ignore all the others. For example if 1234567 was entered as an address the MONITOR would ignore the 123 and the address accepted by the MONITOR would be 4567. Note that accessing I/O ports 28 through 2F using the "O" command could affect operation of the MONITOR and these I/O port addresses should be avoided. The MONITOR executes at addresses F800 through FFFF. Any user memory at these addresses will be ignored. It is not necessary to disable these external memory devices while the MONITOR is in

use. However, the MONITOR will be unable to access external memory from address F800 through FFFF. The on-board RAM functions in a similar fashion to the MONITOR EPROM when accessed. Any external memory at addresses 0000 through 03FF will be ignored by the CPU board. This feature is useful when debugging an inoperative memory board. The on-board RAM is selected to be at address 0 through 3FF and is used to hold the MONITOR stack. Test programs may be typed into RAM at address 100 through 3FF to help diagnose the failing memory board in addition to using the "J" command.

The disk diagnostic routines will prove invaluable in getting your disk drives and controller operational if problems develop in these devices. When running under control of the MONITOR, full visability is provided to all disk error conditions that occur. The "I" and "O" commands are sometimes useful to activate the disk controller I/O ports directly (port addresses 98 through 9F). Test programs may be entered from the MONITOR to aid in diagnosing disk problems. This is usually done to loop on a failing function. This is about the only way signals on the drive or controller can be viewed on an osciliscope. This process is eased by coding calls to the various MONITOR subroutines to perform the desired functions. Test programs may use any of the BIOS jump vectors as convienient entry points to these functions. All routines that perform disk functions usually return with the zero flag reset (= 0) if an error was detected. The test program can simply ignore this condition and continue to activate the desired functions.

# SECTION III

# INSTALLATION

## Installing the UFDC-I

You should have received the following:

1. UFDC-I floppy disk controller.
2. SYSTEM disk containing CTVIII (MONITOR/BIOS) and FMTIII format program files.
3. UFDC-I Technical Information and Users manual
4. Optional CP/M 2.2 and CP/M manuals.
5. Optional 2716 EProm containing monitor code (SBC880 CPU).

To install the UFDC-I proceed as follows:

1. Select proper drive characteristics by installing option jumpers for drive type and step rates using the following table. Defaults are 8" drives and 3ms step rates. No jumpers required.

| STEP RATES | JUMPER OPTIONS S0 | S1 | 5/8 | |
|---|---|---|---|---|
| 3ms | OUT | OUT | OUT | |
| 6ms | IN | OUT | OUT | 8" |
| 10ms | OUT | IN | OUT | DRIVES |
| 15ms | IN | IN | OUT | |
| 6ms | OUT | OUT | IN | |
| 12ms | IN | OUT | IN | 5 1/4" |
| 20ms | OUT | IN | IN | DRIVES |
| 30ms | IN | IN | IN | |

| 5/8 JUMPER OPTION |
|---|
| OUT =8" DRIVE |
| IN= 5 1/4" DRIVE |

2. Place the UFDC-I card in your system with power off. Be carefulnot to place the card in backwards, sever damage could occur and void your warranty. Next cable the disk drives to J2 (5 1/4") and/or J3 (8").

3. Install the UFDC-I monitor EPROM (or your own version in EProm) on the CPU board and test it.

4. Perform circuit card test proceedures included under the trouble shooting proceedures in this section.

5. Place the SYSTEM disk in drive 0 (CP/M drive A) and type A0 (selects drive 0).

6. Type T0 and the monitor will step the head on drive 0 to track 20 (hex). Type A0 and the disk head will return to track 0 to log on the disk drive. If an error occurs, check the step rate jumpers installed in step 1. The

drive will not function correctly if the selected step rate is wrong.

7. Type A0 to log on drive A. Type L100 and the track image will be read into memory. Type D100,280 to view the first part of the track on your terminal. All gaps, ID and data fields will be displayed. If this test fails you have a read problem with your drive. Check all drive and UFDC-I options.

8. Type B. Instructions will appear on your terminal and are repeated in steps 9 and 10. If a failure occurs referto the troubleshooting guide.

9. Remove the SYSTEM disk from drive A.

10. Insert a disk in drive A containing a CP/M image configured for 20K of memory . This must be a single density IBM format disk. The standard CP/M distributed 8 inch disk contains a CP/M image of the proper type. If your disk has the wrong size CP/M image you will have to generate one of the proper size using MOVCPM and SYSGEN. Some vendors supply a modified version of MOVCPM that locates he CP/M image at lower memory addresses to make room fo a larger BIOS. If you have a modified MOVCPM, it will not accept a memory size of 20K. Consult the vendors literature and locate the minimum valid memory size and use this to construct a CP/M image. This should result in a usable CP/M image.

11. Press the return key and the CP/M prompt A> should appear on the terminal. If the CP/M image is the wrong size return to step 10 to create a usable CP/M image. If you do not have a disk with the CP/M image on it you may purchase one from COMPUTIME.

12. After the CP/M prompt A> appears, proceed to run MOVCPM by typing the following on the terminal:

    MOVCPM 60 *

    If your MOVCPM program is modified you will have to make allowance for the memory offset. For example, if you entered 22K as the minumum memory size value in step 10 you would enter 62K instead of 60K at this point.

13. The message "READY FOR SYSGEN OR SAVE 34 CPM60.COM" will appear on the terminal. You should now enter at the terminal:

    SAVE 34 CPM60.COM

14. Remove the CP/M release disk from drive A.

15. Put the SYSTEM disk in drive A.

16. Type on the terminal FMTIII CPM60.COM and press the return key. This will load the format program.

17. Remove the SYSTEM disk from drive A.

18. Put the CP/M release disk back in drive A.

19. When the menu appears, make selection A. This is the command to read the CP/M image you have just created into memory.

20. Remove the CP/M release disk from drive A and place a scratch disk in drive A. THIS IS IMPORTANT ! If you write a bad CP/M image on the CP/M release disk you may have to obtain a new copy. To provide protection you are now going to format the scratch disk and use this disk from now on.

21. Make selection F. This is the command to format a disk. Next make selection 4 (8 inch single side single density). Next select the A drive for formatting. Answer Y to the erase all message if you are sure you have a scratch disk in drive A. The disk in drive A will now be formatting.

22. When the disk has finished formatting and the menu appears, make selection C. This is the command that will place the new CP/M image on a selected disk that was just formatted. Select the A drive.

23. To return to CP/M make selection E. The CP/M image you have created should have booted and signed on. If the CP/M prompt fails to appear you may have the wrong size CP/M image. Repeat steps 8 through 23 and pay special attention to the memory size entered in steps 10 and 1 if you have a modified version of MOVCPM.

24. Remove the disk from drive A and place the SYSTEM disk in drive A.

25. Type at the terminal FMTIII and press the return key.

26. Remove the SYSTEM disk from drive A and place the scratch disk containing the new CP/M image in drive A.

27. Make selection R. This will read the CP/M image from the selected disk drive into memory. Select drive A.

28. Remove the scratch disk from drive A and set it aside. Place another scratch disk in drive A and make the following selections from the terminal:

    G (command to format the disk and write a CP/M image)
    4 (selects 8 inch single side single density. You may

alter this selection and pick any desired format)
A (selects drive A for formatting)

29. When the menu reappears remove the scratch disk from drive A and set it aside. Place the next disk to be formatted in drive A and make the following selection:

    G (command to format a disk, uses the parameters entered in step 28)

    Repeat this step until you have an adequate supply of formatted CP/M disks.

30. With the FMTIII program still active place the CP/M release disk in drive A. Make selection W. This will write disk tables only on the disk after you have selected disk drive A.

31. The process of writing tables to disks should be performed on all the disks that you will want to use with your new CP/M system. It is required that your disks be formatted in the standard single or double density IBM format before being used on your new CP/M system. Other formats are usable provided that they are compatable with the menu selections in the FMTIII program. When in doubt, stick with the standard single density format. Proceed as follows: Enter at the terminal

    W (command to write tables to disk)
    4 (selects 8 inch single side single density. You may use other formats selections if they match the format of the disk)

    Remove the disk from drive A and set it aside. Insert the next disk in drive A and repeat the same process until all the disks have tables placed on them.

32. At this point you should copy the SYSTEM disk, the CP/M release disk, and all disks containing existing programs and files. Refer to your CP/M documentation for instructions on using PIP.

You are now ready to use your new CP/M system. Be sure to place the original system disk and CP/M release disk in a safe place. Use copies of the original disks for any work you are doing.

Troubleshooting Procedures

Controller registers and data paths:

1. Reset system.
2. Enter O9D,55 (outputs 55 to track register).
3 Enter I9D (inputs track register). The value displayed should be 55.
4. Enter O9E,AA (output AA to sector register).

5. Enter I9E (inputs sector register). The value displayed should be AA.
6. Enter O9F,FF (outputs FF to data register).
7. Enter I9F (inputs data register). The value displayed should be FF.
8. Enter O9F,0 (outputs 00 to data register).
9. Enter I9F (inputs data register). The value displayed should be 00.

Drive select logic:
Requires pullups or drives connected on DRVSEL signals.

1. Reset the system. DRVSEL1/, 2/, 3/, and 4/ should be high.
2. Enter O98,0 (outputs 00 to control port). The ignal DRVSEL1/ should be low.
3. Enter O98,1 (outputs 01 to control port). The ignal DRVSEL2/ should be low.
4. Enter O98,2 (outputs 02 to control port). The signal DRVSEL3/ should be low.
5. Enter O98,3 (outputs 03 to control port). The signal DRVSEL4/ should be low.
6. Enter O98,4 (outputs 04 to control port). DRVSEL1/, 2/, 3/, and 4/ should be high.

Wait state logic:

1. Reset the system.
2. Enter O98,80 (outputs 80 to control port). This enables the wait circuits.
3. Enter I9C (inputs from the controller status register). This insures that INTRQ is reset.
4. Enter I9F (inputs from the data register). The processor should hang in a wait state trying to access the data register at IO address 9F hex.
5. Reset the system or enter O98,0 and the wait state should be removed to allow the CPU to run normally.
6. Enter I9F (inputs from the data register). The CPU should not hang.

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## SECTION IV

## COMMAND DESCRIPTION

### INTRODUCTION

The information contained in this section has been extracted from the Western Digital data sheet for the WD179X controller. If you desire more detail than contained in this section refer to the data sheet.

The 1795 will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off. The one exception is the Forced Interrupt command. The Busy status bit is set whenever a command is being executed. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion the commands are divided into four types summarized as follows:

| | | BITS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| TYPE | COMMAND | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| I | Restore | 0 | 0 | 0 | 0 | h | V | r1 | r0 |
| I | Seek | 0 | 0 | 0 | 1 | h | V | r1 | r0 |
| I | Step | 0 | 0 | 1 | u | h | V | r1 | r0 |
| I | Step In | 0 | 1 | 0 | u | h | V | r1 | r0 |
| I | Step Out | 0 | 1 | 1 | u | h | V | r1 | r0 |
| II | Read Sector | 1 | 0 | 0 | m | F2 | E | F1 | 0 |
| II | Write Sector | 1 | 0 | 1 | m | F2 | E | F1 | a0 |
| III | Read Address | 1 | 1 | 0 | 0 | 0 | E | 0 | 0 |
| III | Read Track | 1 | 1 | 1 | 0 | 0 | E | 0 | 0 |
| III | Write Track | 1 | 1 | 1 | 1 | 0 | E | 0 | 0 |
| IV | Force Interrupt | 1 | 1 | 0 | 1 | I3 | I2 | I1 | I0 |

Note: Bits shown in TRUE form.

### TYPE I COMMANDS FLAG SUMMARY

Head Load Flag (Bit 3)
- h = 0 Unload head at beginning
- h = 1 Load head at beginning

Verify Flag (Bit 2)
- V = 0 No verify
- V = 1 Verify on destination track

Stepping Motor Rate (Bits 1-0)

| CLK | | 2MHz | 2MHz | 1MHz | 1MHz |
|---|---|---|---|---|---|
| r1 | r0 | DD | SD | DD | SD |
| 0 | 0 | 3ms | 3ms | 6ms | 6ms |
| 0 | 1 | 6ms | 6ms | 12ms | 12ms |
| 1 | 0 | 10ms | 10ms | 20ms | 20ms |
| 1 | 1 | 15ms | 15ms | 30ms | 30ms |

Update Flag (Bit 4)
u = 0 No update
u = 1 Update track register

TYPE II & III COMMANDS FLAG SUMMARY

Multiple Record Flag (Bit 4)
m = 0 Single record
m = 1 Multiple records
Data Address Mark Flag (Bit 0)
a0 = 0 FB (Data Mark)
a0 = 1 FB (Deleted Data Mark)
15ms Delay (Bit 2)
E - 0 No 15ms delay
E = 1 15ms delay
Side Select Flag (Bit 1)
F1 = 0 Select side 0
F1 = 1 Select side 1
Sector Length Flag (Bit 3)

| | SECTOR LENGTH FIELD | | | |
|---|---|---|---|---|
| | 00 | 01 | 10 | 11 |
| F2 = 0 | 256 | 512 | 1024 | 128 |
| F2 = 1 | 128 | 256 | 512 | 1024 |

TYPE IV COMMAND FLAG SUMMARY

Interrupt Condition Flags (Bits 3-0)
I0 = 1 Not-Ready to Ready transition
I1 = 1 Ready to Not-Ready transition
I2 = 1 Index pulse
I0-I3 = 1 Terminate with no interrupt

TYPE I COMMANDS

Type I commands include the Restore, Seek, Step, Step In, and Step Out commands. Each of the Type I commands contain a rate field (r0r1), which determines the stepping motor rate.

Type I commands contain a head load flag (h) that determines if the head is to be loaded at the beginning of the command. If h=1 the head is loaded at the beginning of the command. If h=0 the head is unloaded. Once the head is loaded it will remain engaged until the 1795 receives a command that specifically unloads it. If the 1795 is idle for 15 revolutions of the disk, the head will be automatically unloaded.

Type I commands also contain a verification flag (V) that determines if a verification operation is to take plaqe on the selected track. If V=1 a verification is performed. If V=0 no verification will occur.

During verification, the head is loaded and after an internal 15ms delay, the first encountered ID field is read off the disk. The track address of the ID field is then compared to the track register; if there is a match and a valid CRC, the verification is complete an interrupt is generated and the Busy status bit is reset. If there is not a match but there is a valid ID CRC, an interrupt is generated and Seek Error Status bit is set and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC Error status bit is set and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after four revolutions of the disk, the operation will be terminated and an interrupt generated.

The Step, Step In, and Step Out commands contain an update flag (u). When u=1 the track register is updated by one for each step. When u=0 the track register is not updated.

The Side Select Output (SSO) is not affected during Type I commands and an internal side compare does not take place when the (V) flag is on.

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 0 input is sampled. If it indicates that the Read-Write head is positioned over track 0, the track register is loaded with zeros and a interrupt is generated. If the input is not active, stepping pulses at the rate indicated by r0r1 are issued until the input indicates that the head is on track 0. At this time the track register is loaded with zeros and an interrupt is generated. If the input does not indicate track 0 after 255 stepping pulses, the operation will be terminated, an interrupt generated and the Seek Error status bit is set. A verification operation takes place if the (V) flag is set. The (h) bit allows the head to be loaded at the start of the command.

SEEK

This command assumes that the track register contains the track number of the current position of the Read-Write head and the Data Register containes the desired track number. The track register will be updated and the stepping pulses issued in the appropriate direction until the contents of the track register are equal to the contents of the Data register. A verification operation takes place if the (V) flag is set. The (h) flag allows the head to be loaded at the start of the command.

STEP

Upon receipt of this command one stepping pulse is issued to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r0r1 field a verification takes place if the (V) flag is set. If the (u)

flag is set, The track register is updated. The (h) flag allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP IN

Upon receipt of this command one stepping pulse is issued in the direction towards track 76. If the (u) flag is set the track register is incremented by one. After a delay determined by the r0r1 field, a verification takes place if the (V) flag is set. The (h) flag allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP OUT

Upon receipt of this command one stepping pulse is issued in the direction of track 0. If the (u) flag is set the track register is decremented by one. After a delay determined by the r0r1 field, a verification takes place if the (V) flag is set. The (h) flag allows the head to be loaded at the start of the command.

TYPE II COMMANDS

The Type II commands are the Read Sector and the Write Sector commands. Prior to loading the Type II command into the command register, the host computer must load the sector register with the desired sector number. Upon receipt of the Type II Command, the Busy status bit is set. If the E flag = 1 (this is the normal case) the head is loaded and after a 15ms delay the HLT input is sampled. If the E flag is 0, the head is loaded and HLT is sampled with no 15ms delay.

When an ID field is located on the disk the track number on the ID field is compared with the track register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, The Sector Number of the ID field is compared with the Sector Register. If there is not a sector match, the next encountered ID field is read and comparidons again made. If the ID field CRC is correct, the data field is then located and will either be written into, or read from depending upon the command. An ID field with a track number, sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set and the command is terminated with an interrupt.

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m=0, a single sector is read or written and a interrupt is generated at the completion of the command. If m=1 multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The 1795 will continue to read or write multiple records and update the sector register

until the sector register exceeds the number on the track or until the Force Interrupt command is loaded into the command register, which terminates the command and generates an interrupt. If the Sector Register exceeds the number of sectors on the track, the Record-Not-Found status bit will be set.

The Type II commands also contain side select compare flags. When F1=0, no side comparison is made. When F1=1, the LSB od the side number is read off the ID field of the disk and compared with the contents of the (S) flag. If the (S) flag compares with the side number recorded in the ID field, the ID search continues. If a comparison is not made within 5 index pulses, the interrupt is generated and the Record-Not-found status bit is set.

The Read Sector and Write Sector commands include a (b) flag, in conjunctiopn with the sector length byte of the ID field, allows different byte lengths to be implemented in each sector. For IBM compatability the (b) flag should be set to one. The (s) flag allows direct control over the side select output and is set or reset at the beginning of the command depending on the value of this flag.

READ SECTOR

Upon receipt of the Read Sector command, the head is loaded, the Busy Status bit is set, and when an ID field is ecountered that has the correct track, sector, side number, and CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the Record-Not-Found Status bit is set and the operation is terminated.

When the first byte of the data field has been shifted through the Data Shift Register (DSR), it is transfered to the Data Register (DR), and a Data Request (DRQ) is generated. When the next byte is accumulated in the DSR, it is transfered to the DR and another DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transfered, that character is lost and the Lost-Data Status bit is set. This sequence continues until the complete data field has been sent to the computer. If there is a CRC error at the end of the data field, the CRC Error Status bit is set and the command is terminated (even if it is a multiple record command).

At the end of the read operation the type of Data Address Mark encountered in the data field is recorded in the status register as shown below:

| STATUS BIT 5 | |
|---|---|
| 1 | Deleted Data Mark |
| 0 | Data Mark |

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded and the Busy Status bit is set. When an ID field is encountered that has the correct track, sector, side number and correct CRC, a DRQ is generated. The 1795 counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate output is made active if the DRQ is serviced i.e., the DRQ has been loaded by the computer. If DRQ has not been serviced, the Write Gate is made active and the six bytes of zeros in single density and 12 bytes in double density are then written to disk. At this time the Data Address Mark is written on the disk as determined by the (a0) field of the command shown below:

| a0 | Data Address Mark (Bit 0) |
|---|---|
| 1 | Deleted Data Mark |
| 0 | Data Mark |

The 1795 then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing, the Lost Data Status bit is set and a byte of zeros is written on disk and the command is terminated. After the last data byte has been written on the disk the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The Write Gate output is then deactivated.

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command the head is loaded and the Busy Status bit is set. The next encountered ID field is then read in from the disk and the six data bytes of the ID field are assembled and transfered to the DR. A DRQ is generated for each byte. The six bytes of the ID field are shown below:

| TRACK ADDR | SIDE NUMBER | SECTOR ADDRESS | SECTOR NUMBER | CRC 1 | CRC 2 |
|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | 5 | 6 |

Although the CRC characters are transfered to the computer, the 1795 checks for validity and the CRC error status bit is set if there is a CRC error. The track address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the Busy Status bit is reset.

READ TRACK

Upon receipt of the Read Track command the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. As each byte is assembled it is transfered to the Data Register and the Data Request is generated for each byte. NO CRC checking is performed. Gaps are included in the input data stream. The accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command the interrupt is activated. An internal side compare is not performed during a Read Track command.

WRITE TRACK

Upon receipt of the Write Track command the head is loaded and the Busy Status bit is set. Writting starts with the leading edge of the first encountered index pulse and continues until the next index pulse at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy. The Lost Data Status bit is set and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from FB to FE is about to be transfered from the DR to the DSR in FM or by receipt of F5 in MFM.

TYPE IV COMMAND

FORCED INTERRUPT

This command can be loaded into the command register at any time. If there is a current command under execution the command will be terminated and an interrupt will be generated when the condition specified in the I0 through I3 field is detected. The interrupt conditions are shown below:

I0 = Not-Ready-To-Ready Transition
I1 = Ready-To-Not-Ready Transition
I2 = Every Index Pulse
I3 = Immediate Interrupt (requires reset, see note)

NOTE: If I0-I3 = 0, there is no interrupt generated but the current command is terminated and the Busy Status bit is reset. This is the only command that will enable the immediate interrupt to clear on a subsequent Load Command Register or Read Status Register.

STATUS DESCRIPTION

Upon receipt of any command except the Forced Interrupt, the Busy Status bit is set and the rest of status bits are updated or cleared for the new command. If the Forced Interrupt command is received when there is a current command under execution the Busy Status bit is reset and the rest of the status bits are unchanged. If the Forced Interrupt is received when there is not a current command under execution the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case status reflects the Type I commands. The format of the status register is shown below:

| BITS | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 |

Status varies according to the type of command being executed.

STATUS REGISTER SUMMARY

| BIT | TYPE I COMMANDS | READ ADDRESS | READ SECTOR | READ TRACK | WRITE SECTOR | WRITE TRACK |
|---|---|---|---|---|---|---|
| S7 | NOT RDY | NOT RDY | NOT RDY | NOT RDY | NOT RDY | NOT RDY |
| S6 | Write Protect | 0 | 0 | 0 | Write Protect | Write Protect |
| S5 | Hd Load | 0 | Rec-Type | 0 | WR Fault | WR Fault |
| S4 | Seek Err | RNF | RNF | 0 | RNF | 0 |
| S3 | CRC Err | CRC Err | CRC Err | 0 | CRC Err | 0 |
| S2 | Track 0 | Lost data | Lost data | Lost data | Lost data | Lost data |
| S1 | Index | DRQ | DRQ | DRQ | DRQ | DRQ |
| S0 | Busy | Busy | Busy | Busy | Busy | Busy |

STATUS FOR TYPE I COMMANDS

| BIT NAME | MEANING |
|---|---|
| S7 NOT READY | This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR |
| S6 PROTECTED | When set, indicates Write Protect is activted. |
| S5 HEAD LOADED | When set it indicates the head is loaded and engaged. |
| S4 SEEK ERROR | When set the desired track was not verified. This bit is reset to 0 when updated. |
| S3 CRC ERROR | CRC encountered in ID field. |
| S2 TRACK 00 | When set indicates Read/Write head is positioned to track 0. |
| S1 INDEX | When set indicates index mark detected from drive. |
| S0 BUSY | When set command is in progrees. When reset no command is in progress. |

STATUS FOR TYPE II AND III COMMANDS

| BIT NAME | MEANING |
|---|---|
| S7 NOT READY | This bit when set indicates the drive is not ready. The Type II and III commands will not execute unless the drive is ready. |
| S6 WRITE PROTECT | On Read Record not used. On Read Track not used. On any Write it indicates a Write Protect. This bit is reset when updated. |
| S5 RECORD TYPE/ WRITE FAULT | On Read Record it indicates the record-type code from the data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write indicates a write fault. This bit is reset when updated. |
| S4 RECORD NOT FOUND (RNF) | When set indicates that the desired track, sector, or side were not found. This bit is reset when updated. |
| S3 CRC ERROR | If S4 is set an error is found in one or more ID fields; otherwise it indicates error in data field. Bit is reset when updated. |
| S2 LOST DATA | When set indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated. |
| S1 DATA REQUEST | This bit is a copy of the DRQ output. When set indicates the DR is full on a Read operation or the DR is empty on a Write operation. Bit is reset to zero when updated |
| S0 BUSY | When set command is under execution. When reset no command is under execution. |

## FORMATTING THE DISK

Formatting the disk is a relativley simple programming task. It is accomplished by positioning the head over the desired track and issuing the Write Track command. Upon receipt of the Write Track command the 1795 raises the DRQ. At this point in time the data register is loaded with the desired data to be written on the disk. For every byte of information to be written on the disk a data request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the 1795 detects a data pattern of F5 through FE in the data register, this is interpreted as Data Address Marks with missing clocks or CRC generation. For instance, in FM an FE pattern will be interpreted as an ID address mark (DATA-FE, CLK-C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 through FE must not appear in the gaps, data fields, or ID fields. Also CRC's must be generated by an F7 pattern. Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

### IBM 3740 FORMAT - 128 BYTE SECTOR

Shown below is the IBM single density format with 128 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the Data register with the following values. For every byte to be written, there is one Data Request.

| Number of Bytes | Hex Value Of Byte Written |
|---|---|
| 40 | FF (or 00) |
| 6 | 00 |
| 1 | FC (Index Mark) |
| 26* | FF (or 00) |
| 6 | 00 |
| 1 | FE (ID Address Mark) |
| 1 | Track Number |
| 1 | Side Number (00 or 01) |
| 1 | Sector Number (1 thru 1A) |
| 1 | 00 |
| 1 | F7 (2 CRC's Written) |
| 11 | FF (or 00) |
| 6 | 00 |
| 1 | FB (Data Address Mark) |
| 128 | Data (IBM uses E5) |
| 1 | F7 (2 CRC's Written) |
| 27 | FF (or 00) |
| 247** | FF (or00) |

* Write bracketed field 26 times
** Continue writting until 1795 interrupts out-Approx. 247 bytes.

## IBM SYSTEM 34 FORMAT 256 BYTE SECTOR

Shown below is the IBM double density format with 256 byte sector. In order to format a diskette the user must issue the Write Track command and load the Data register with the following values. For every byte to be written, there is one Data Request.

| Number of Bytes | Hex Value of Bytes Written |
|---|---|
| 80 | 4E |
| 12 | 00 |
| 3 | F6 |
| 1 | FC (Index Mark) |
| 50* | 4E |
| 12 | 00 |
| 3 | F5 |
| 1 | FE (ID Address Mark) |
| 1 | Track Number (0 thru 4C) |
| 1 | Side Number (0 or 1) |
| 1 | Sector Number (1 thru 1A) |
| 1 | 01 |
| 1 | F7 (2 CRC's Written) |
| 22 | 4E |
| 12 | 00 |
| 3 | F5 |
| 256 | Data |
| 1 | F7 (2 CRC's Written) |
| 54 | 4E |
| 598** | 4E |

* Write bracketed field 26 times.
** Continue writting until 1795 interrupts out. Apprx. 598 bytes.

## NON IBM FORMATS

Variations in the IBM format are possible to a limited extent if the following requirements are met. Sector size must be a choice of 128, 256, 512, or 1024 bytes. Gap size must be according to the following table. Note that the Index Mark is not required by the 1795. The minimum gap sizes shown are that which is required by the 1795, with PPL lock up time, motor speed variation, etc., adding additional bytes.

| | FM | MFM |
|---|---|---|
| Gap I | 16 bytes FF | 32 bytes 4E |
| Gap II | 11 bytes FF | 22 bytes 4E |
| * | 6 bytes 00 | 12 bytes 00 |
| Gap III | 10 bytes FF | 24 bytes 4E |
| | | 3 bytes A1 |
| ** | 4 bytes 00 | 8 bytes 00 |
| Gap IV | 16 bytes FF | 16 bytes 4E |

* Byte counts must be exact.
** Byte counts are minimum, except exactly 3 bytes of A1 must be written.

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## SECTION V

## CIRCUIT DESCRIPTION

### S100 Interface

The reader can refer to the proposed IEEE 696 standard if a detail description of each interface signal is desired. The following signals are used:

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 72 | RDY | When driven low, places the CPU in a wait state. Used to synchonize data transfer between the CPU and the UFDC-I. |
| 79 | A0 | Address Bus. Used in conjunction with SINP and SOUT to address I/O ports on the UFDC-I. Address bits 3 through 7 are used to select the UFDC-I board for access and A0, A1, and A2 select one of the I/O ports |
| 80 | A1 | |
| 81 | A2 | |
| 31 | A3 | |
| 30 | A4 | |
| 29 | A5 | |
| 82 | A6 | |
| 83 | A7 | |
| 24 | 02 | CPU clock. Used to time the removal of the wait state (see RDY) from the CPU. |
| 99 | POC | Power on clear. Resets the floppy disk controller chip and the external control port. All disks are deselected when the external control port is reset. |
| 77 | PWR | Processor write strobe. Used as a timing reference for I/O writes to the UFDC-I. |
| 36 | DO0 | Data output bus. Data is output from the CPU to the UFDC-I on this bus. |
| 35 | DO1 | |
| 38 | DO2 | |
| 39 | DO3 | |
| 38 | DO4 | |
| 39 | DO5 | |
| 40 | D06 | |
| 90 | DO7 | |
| 95 | DI0 | Data input bus. Data is input to the CPU from the UFDC-I on the bus. |
| 94 | DI1 | |
| 41 | DI2 | |
| 42 | DI3 | |
| 91 | DI4 | |
| 92 | DI5 | |
| 93 | DI6 | |
| 43 | DI7 | |

| | | |
|---|---|---|
| 46 | SNIP | Status input. Used by the UFDC-I to control all data transfers to the host from the board on the data input bus (DI0 to D17). |
| 45 | SOUT | Status output. Used in conjunction with PWR to control all data transfers from the host to the UFDC-I on the data output bus (DO0 to DO7). |

All S100 signals are received by the bus type receiver devices that have hysteresis at their inputs for noise rejection. Signals are received by U23, U8, U24, U25, and U26. The RDY signal is driven by U9 (an open collector device). The Data Input Bus (DI0 to DI7) is driven by portions of U25 and U26 (tri-state devices).

I/O Port Decode

The I/O port addresses of the UFDC-I are HEX 98 through 9F. These addresses are detected by comparator U23. S100 address bits A3 through A7 are input to the "B" (bus) inputs of U23 (these inputs have hysteresis for noise rejection). The address bits are then compared to the "A" inputs (TTL compatible) which are jumpered for the proper address range. When the A = B output goes active (low) it indicates the address is in the proper range to access the UFDC-I. SINP or SOUT must be active (I/O cycle requested) before an actual access will take place.

Wait State Control

The inhibit signal out of U18 pin 5 will become active if all the following conditions exist at the same time:

1. Bits zero thru seven of the S-100 address bus equal hex 9F.
2. WAITEN/ is active (low) at the control port output (U19 pin 10 ).
3. INTRQ is inactive (low). This indicates the 1795 is not at the end of a read or write operation.
4. DRQF isinactive (low). This indicates the 1795 is not ready to transfer data.

The inhibit signal, when active will prevent SINP from activating RE/ (pin 4) of the 1795 (U14). It will also prevent WE/ (pin 2 of U14) from being actvated by SOUT and PWR/. When inhibit goes active during an I/O cycle, (SINP or SOUT active) U4 is set on the next rising edge of the 02 clock. The output of U4 pin 9 will lower the RDY line on the S-100 bus and wait states will occur in the system CPU. When the 1795 is ready to transfer disk data the signal DRQ will become active. This causes the following events to occur:

1. Inhibit (U18 pin 5) becomes inactive (low) after DRQF is active (U4 pin 5).
2. RE/ or WE/ will go active (low) to request the desired

read or write data transfer at the 1795.

3. U4 pin 9 becomes inactive (low) at the next rising edge of the 02 clock. This raises the RDY signal at the S-100 bus and removes the "wait" condition from the CPU.
4. At the end of the I/O cycle DRQF is made inactive (U4 pin 5) by the trailing edge of SINP or SOUT. This enables the wait circuitry for the next CPU cycle.

## Control Port

The control port is a hex D flip flop (U19). The data bus bits that are tied to the "D" inputs of the flip-flops are as follows:

| Bits | Function |
|---|---|
| 7 | 1 = Enable wait circuits |
| | 0 = Disable wait circuits |
| 6 | 1 = Single density |
| | 0 = Double density |
| 5 | 1 = Side 0 |
| | 0 = Side 1 |
| 4 | Not used |
| 3 | Not used |
| 2 | 0 = Enable drive select |
| | 1 = Disable drive select |
| 1 & 0 | 00 = Drive 1 01 = Drive 2 |
| | 10 = Drive 3 11 = Drive 4 |

NOTE: The polarity of the 0 and 1 states of the control port signals are given relative to the S-100 data output bus. Internal control port signals are inverted.

## Drive Select

Half of decoder U12 is used to decode the lower 3 bits of the control port to provide drive select signals to the floppy disk interface. Bit 2 on the control port will enable or disable drive select signals at the output of the decoder. When the decoder is enabled by bit 2, bits 0 and 1 determine which one of the 4 drive selects will be made active. When one of the drive select signals is active it will select the option jumper buffers (U5 and U6) associated with that drive. The 5/8 jumper selects the proper clocks for operation with 5 1/4" or 8" disk drives. The step-rate jumpers (S0 and S1) indicate the step-rate required by the selected drive. The 5/8 jumper directly activates the 1795 and data separator clocks and the needs no action from software. The step-rate jumpers are read in by softwar at the status port and are appended to all controller commands that perform head movement (restore, seek, step in, etc).

## Status Port

The status port is an octal buffer (U20) that provides the following signals to the data bus as input data:

| Bits | Function |
|---|---|
| 7 | 1 = The 1795 has completed an operation and needs attention. |
| | 0 = No 1795 operation is in progress or the operation has not completed. |
| 6 | 1 = No disk drive is selected (drive select disabled), or a selected drive does not exist. When a selected drive exists the head is not positioned on track 0. |
| | 0 = The selected drive has its head positioned on track 0. |
| 5 | 1 = The head load timer has been activated (timing out). |
| | 0 = The head load timer is inactive. |
| 4 | 1 = The head of the selected drive is loaded. |
| | 0 = A head unload is requested. |
| 3 | 1 = Not used. |
| 2 | 1 = 5 1/4" disk drive is selected or no drive selected. |
| | 0 = 8" disk drive is selected. |
| 1 & 2 | 00 = 3ms step rate for 8" drives and 6ms for 5 1/4" drives. |
| | 01 = 6ms step rate for 8" drives and 12ms for 5 1/4" drives. |
| | 10 = 10ms step rate for 8" drives and 20ms for 5 1/4" drives. |
| | 11 = 15ms step rate for 8" drives and 30ms for 5 1/4" drives. |

## Clock Logic

The master 16MHz clock is provided by clock oscillator U16 and is divided down to 8, 4, 2, and 1MHz clocks by counter U22. The 4MHz clock is used by the digital write pre-compensation circuit. the 2Mhz or 1MHz clock is selected for use by the 1795 in one section of multiplexor U21. The 5/8 signal controls selection of the clocks (5 selects 1 MHz and 8 selects 2MHz). The 8 Mhz clock is provided to the data separator circuitry.

## Floppy Disk Controller

The controller chip (U14) is a Western Digital FD1795-02. The 1795 contains all circuitry to provide read, write, head positioning, and formatting functions for IBM standard single or double density disks. Refer to the data sheets for the 1795 to obtain detail information. Information concerning programming is contained in the application section.

## Digital Write Precompensation

The serial write data is delayed by shift register U28 which is clocked by the 4MHz clock. When the head is located on the outer tracks of the disk (GT43 active at U14 pin 29), the early and late signals are enabled at U27 to select delayed or early serial data. The delaying of write data occurs as follows:

| TG43 | Early | Late | Type of Delay |
|---|---|---|---|
| 0 | X | X | Nominal Delay |
| 1 | 0 | 0 | Nominal Delay |
| 1 | 1 | 0 | 250ns Earlier Than Nominal |
| 1 | 0 | 1 | 250ns Later Than Nominal |

Data Separator

The digital data separator used is the FDC 9216 (U1) from Standard Microsystems Corporation. This chip contains a clock divider and data separator that are programmed by the CD0 and CD1 inputs. The CD0 and CD1 inputs are controlled by one half of the decoder U12, one nand gate (U10 pins 8, 9, & 10), and an inverter (U3 pins 8 & 9). The 5/8 and DD/SD (Double Density and Single Density select) signals are input to the decoder and control the data separator as follows:

| 5/8 | DD/SD | CD1 | CD0 | Operation Type |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | Single Density 8" |
| 0 | 1 | 0 | 0 | Double Density 8" |
| 1 | 0 | 1 | 0 | Single Density 5 1/4" |
| 1 | 1 | 0 | 1 | Double Density 5 1/4" |

The data separator provides the separated data to pin 7 of the 1795 (U14) and the separated clock to pin 26 of the 1795. Read data from the disk is synchronized and shaped by U2 prior to being input to the data separator. U2 acts as a digital multi to provide a 125ns active low data pulse which is required by the data separator. U2 also synchronizes the data pulses with the 8 MHz data separator clock to provide additional reliability of the data separation function.

Disk Drive Interface

Signals to the disk drive interface are buffered by open collector drivers U7 and U9. Input signals from the disk drive interface arereceived by U8 and U3 which have hysteresis type inputs for noise rejection. Following is a summary of disk drive signals and functions:

| Signal | 8" | 5 1/4" | Function |
|---|---|---|---|
| GT43/ | Pin 6 | N/A | 1 = Normal write current.<br>0 = Select low write current for inner tracks of disk. |
| HLD/ | Pin18 | Pin 16 | 1 = Remove head from disk surface. On 5 1/4 drives the motor is stoped.<br>0 = Load head against disk surface. On 8" drives a 35ms head load delay timer is triggered when this |

| | | | |
|---|---|---|---|
| | | | signal becomes active. On 5 1/4" drives the motor is started and a 1 second head (motor) delay timer is triggered when this signal becomes active. |
| WD/ | Pin 38 | Pin 22 | Bit serial write data to the selected disk drive (see WGATE/). |
| STEP/ | Pin 36 | Pin 22 | Step pulse. Active low pulse on this output will cause the head on the selected disk drive to step in or out 1 track. Signal DIR determines the direction of head movement. |
| DIR | Pin 34 | Pin 18 | Used in conjunction with STEP/ to control the direction of head movement on the selected disk drive.<br>1 = Out (away from the center of the disk).<br>0= In (towards the center of the disk). |
| WGATE/ | Pin 40 | Pin 24 | 1 = Write circuitry disabled.<br>0 = Write (and erase) circuitry enabled. |
| WPROT/ | Pin 44 | Pin 28 | 1 = Disk in selected drive is not write protected.<br>0 = Disk in selected drive is write protected. |
| INDEX | PIN 20 | Pin 8 | Active low pulses on this signal occur once every revolution for the selected disk when a disk is present in the drive and the motor is running. |
| TRK0/ | Pin 42 | Pin 26 | 1 = Head of the selected drive is not positioned on track zero.<br>0 = Head of the selected drive is positioned on track zero. |
| RDY/ | Pin 22 | N/A | 1 = The selected drive is not ready.<br>0 = The selected drive is ready for disk operations. 5 1/4" disks are always made to appear ready to the 1795. |
| RD/ | Pin 46 | Pin 30 | Bit serial read data from the selected disk drive. |
| SIDESEL | Pin 14 | Pin 32 | Selects the side of the disk (head) to be used for disk |

accesses.
1 = Side 0 (single side disk)
0 = Side 1 (double side disk)

| | | | |
|---|---|---|---|
| DRVSEL1/ | Pin 26 | Pin 10 | One of these four drive select |
| DRVSEL2/ | Pin 28 | Pin 12 | signals will go low to select |
| DRVSEL3/ | Pin 30 | Pin 14 | disk drive for access by the |
| DRVSEL4/ | Pin 32 | N/A | UFDC-1. |

## I/O PORT ADDRESSING

| HEX ADDRESS | OP TYPE | DESCRIPTION |
|---|---|---|
| 98-9B | OUTPUT | D0,D1= DRIVE SELECT<br>00 = Drive A<br>10 = Drive B<br>01 = Drive A<br>11 = Drive D<br>D4 = Side Select<br>D6 = Single Double Density Select<br>D7 = Wait Enable |
| 98-9B | INPUT | D0 = Step Rate 0 Jumper<br>D1 = Step Rate 1 Jumper<br>D2 = 5/8 Jumper<br>D5 = HLD<br>D6 = TRK 0<br>D7 = INTRQ |
| 9C | INPUT | FDC Chip Status |
| 9C | OUTPUT | FDC Chip Command |
| 9D | IN/OUT | Track Register |
| 9E | IN/OUT | Sector Register |
| 9F | IN/OUT | Data Register |

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# APPENDIX A

## DISK DRIVE JUMPER LIST

OLIVETTI 801/802

The jumpers on the drive are not marked very well so I will describe their approximate location and their arrangement.

Set the drive in front of you with the circuit board up, and the front of the drive at the top.

Jumper, Jumper block 15 (at the upper left of the circuit card).
Cut, jumper wire E (just to the right of jumper block 15).
Jumper block 66 (two rows of IC'S down from JB 15) as follows:

```
1 2
3 4
5 6
7 8      JUMPER 2-4, JUMPER 6-8
```

Jumper block 89 (just below JB 66) as follows:

```
1  2  3
4  5  6
7  8  9
10 11 12      JUMPER 8-11
```

Jumper block 159 (just to the left of the 50 pin edge connector) jumper 1-2.

Jumper block 128J (just above the 50 pin edge connector) as follows:

```
1  2  3  4  5  6  7  8
9  10 11 12 13 14 15 16
17 18 19 20 21 22 23 24
```

Jumper 4-12 for drive #1
Jumper 3-11 for drive #2
Jumper 2-10 for drive #3
Jumper 1-9 for drive #4

Shunt block SH155 (just above the 50 pin edge connector) as follows:

| Z | I | A | B | X | H | R | S |
|---|---|---|---|---|---|---|---|
| O | O | O | C | C | C | C | C |
| P | P | P | L | L | L | L | L |
| E | E | E | O | O | O | O | O |
| N | N | N | S | S | S | S | S |
| | | | E | E | E | E | E |
| | | | D | D | D | D | D |

Jumper block 94 (just above and to the left of the edge connector) as follows:

```
                                    8   7
          1    2    3    4         5   6
```

Jumper 5-8, jumper 7-6

Set the jumper on the UFDC-I for a 3MS step rate (no jumper required).

Jumper wires "F","M","C" and "D" are intact.

The three resistor termination packs are installed in the last drive connected to the interface cable only.

SHUGART 801R

JUMPER LIST

| | |
|---|---|
| DC | OPEN |
| D | OPEN |
| C | JUMPER |
| R | TRACE INTACT |
| S | TRACE INTACT |
| I | TRACE INTACT |
| DS | OPEN |
| HL | OPEN |
| A | JUMPER |
| B | OPEN |
| X | JUMPER |
| T1 | JUMPER |
| T2 | JUMPER ON LAST DRIVE ON CABLE |
| T3 | JUMPER ON LAST DRIVE ON CABLE |
| T4 | JUMPER ON LAST DRIVE ON CABLE |
| T5 | JUMPER ON LAST DRIVE ON CABLE |
| T6 | JUMPER ON LAST DRIVE ON CABLE |
| DS1 | |
| DS2 | |
| DS3 | SELECT ONE DRIVE SELECT JUMPER |
| DS4 | |

The 801R drive is specified to step at 10 MS track to track. Jumper the step rate on the UFDC-I board as described in SEC III of this manual.

QUME DDT-8

JUMPER LIST

OPTIONAL I/O JUMPERS
2S - OPEN
DC - OPEN
D - OPEN
C - JUMPERED

T4U - OPEN
HA - OPEN
GND - OPEN

Y - OPEN
DL - OPEN
DS - OPEN
GND - OPEN

PROGRAMMABLE SHUNT
A - SHORTED
B - SHORTED
X - OPEN
R - SHORTED
I - SHORTED
Z - SHORTED
L - SHORTED

DRIVE SELECT
DS1 - DRIVE1
DS2 - DRIVE2  SELECT ONE DRIVE SELECT JUMPER
DS3 - DRIVE3
DS4 - DRIVE4

The two terminator resister packs are to be installed in the last drive only.

The DDT-8 track to track step rate is 3MS. No jumpers are required on the UFDC-I for step rate. 3MS is the default for the jumpers.

MPI B51 5 1/4 INCH DRIVES

PROGRAMMABLE SHUNT

HS - OPEN
DS0 - DRIVE SELECT
DS1 - DRIVE SELECT  OPEN ALL DS OPTIONS EXCEPT THE ONE SELECTED
DS2 - DRIVE SELECT
MUX - OPEN
DS3 - DRIVE SELECT
HM - SHORTED

The terminator resister pack is only required on the last drive. It is located next to the programmable shunt.

The MPI B51 track to track step rate is 6MS. No jumpers are required for step rate on the UFDC-I. You will have to put a jumper in the 5/8 option in order to select 5 1/4 inch drive.

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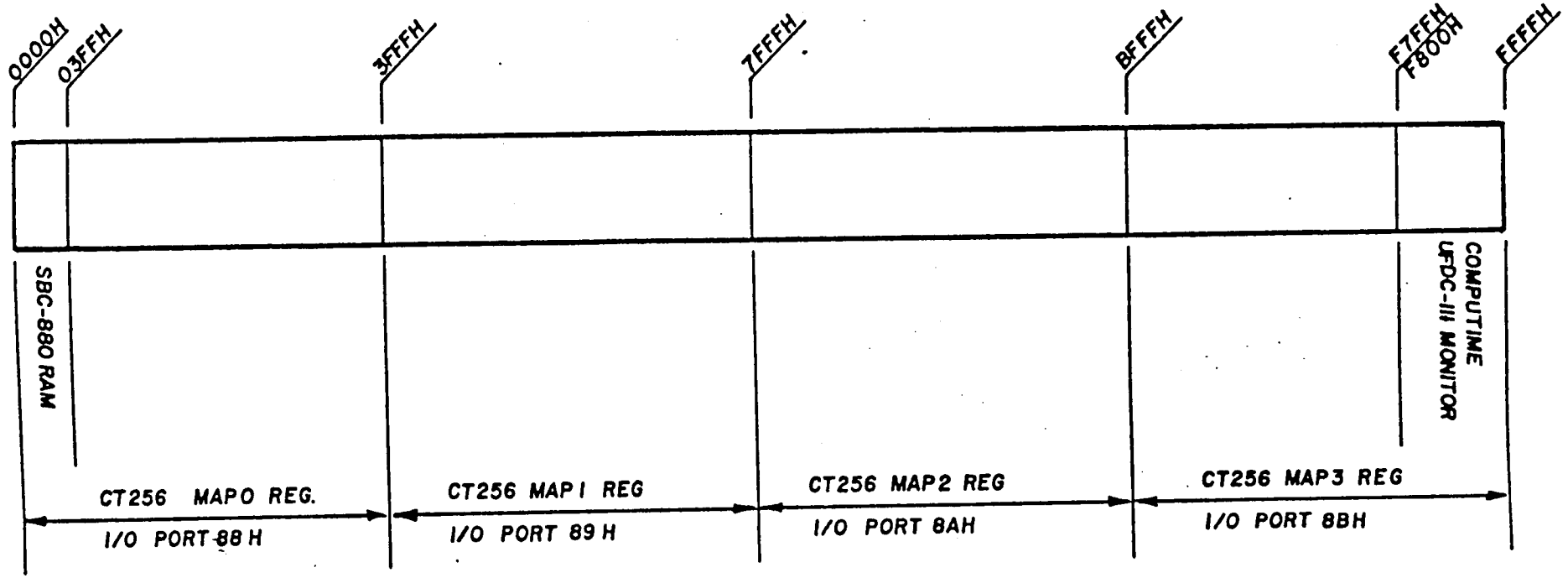
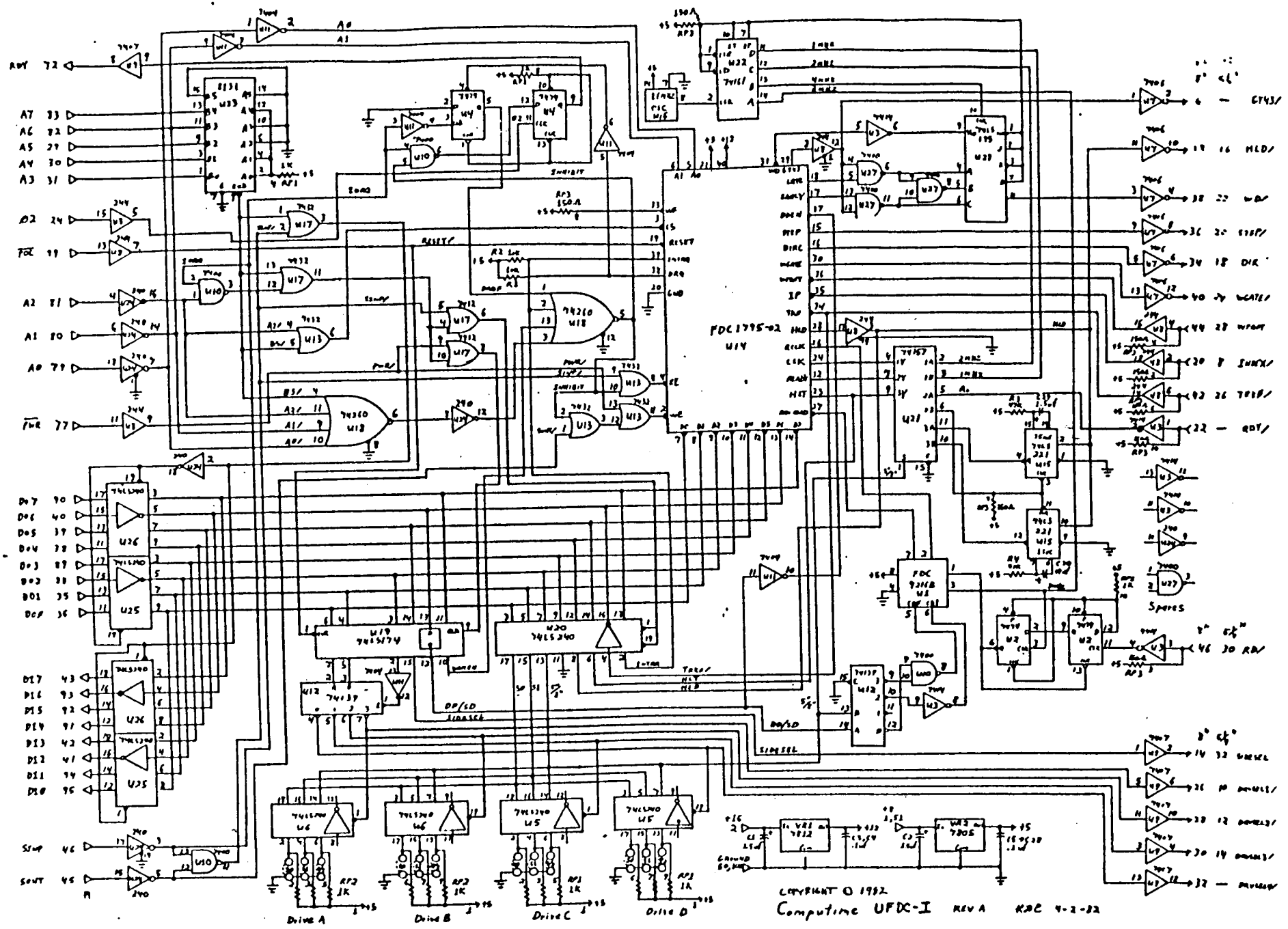
# APPENDIX B

## MONITOR LISTING INCLUDING FLOPPY DISK BIOS FOR CP/M 2.2




| | I/O PORT LOCATIONS | | |
|---|---|---|---|
| | SBC-880 PORTS | | UFDC-I PORTS |
| 28H | TIMER Ø | 9BH | CONTROL REGISTER 1 |
| 29H | TIMER 1 | 9BH | STATUS REGISTER 1 |
| 2AH | TIMER 2 | 9CH | DISK STATUS |
| 2BH | TIMER CONTROL/STATUS | 9CH | DISK COMMAND |
| 2CH | PARALLEL IN/OUT | 9DH | DISK TRACK |
| 2DH | PARALLEL IN/OUT | 9EH | DISK SECTOR |
| 2EH | CONSOLE DATA | 9FH | DISK DATA |
| 2FH | CONSOLE CTL/STATUS | | |

| TOLERANCES | REVISIONS | | | STANDARD SYSTEM MEMORY MAP |
|---|---|---|---|---|
| DECIMAL ± | NO | DATE | BY | |
| FRACTIONAL ± | 1 | | | |
| ANGULAR ± | 2 | | | |
| | 3 | | | DRAWN BY RJS / SCALE NONE / MATERIAL |
| | 4 | | | CHK'D / DATE / DRAWING NO |
| | 5 | | | TRACED / APP'D |


FDC1795-02
U19
Drive A
Drive B
Drive C
Drive D
Spares
COPYRIGHT © 1982
Computime UFDC-I REV A RDC 9-2-82

# UFDC-I

## ASSEMBLY INSTRUCTIONS

IMPORTANT

Read through the instructions before you start assembly. If anything seems unclear of difficult, contact us for advice before proceeding to build this kit. The following instructions will assume that the builder has prior experience in building electronic kits and has knowledge in digital electronics. If you do not have this experience it is recommended that you find an experienced person to help you in the assembly and check out of this board.

PREPARATION

You will need a clean, dry and well lit workspace in which to assemble your kit. If possible, try to find someplace where the parts can stay undisturbed in case you do not finish the assembly all at once. You will need the following tools:

1. A light soldering iron, 15 to 25 watts with a fine tip
2. Fine guage solder with resin flux core. NOT acid flux.
3. Silicon Greese Heat Sinking compound.
4. A pair of sharp diagonal cutters.
5. A medium size screwdriver.
6. A piece of styrofoam.

The following items are optional, but useful.

1. A magnifying glass for examining solder joints and looking for short circuits.
2. A desoldering tool or braid. Better still, take care that you put the components in right the first time. Removing them can be very difficult.
3. Lead former or a pair of needle nose pliars.

PRECAUTIONS

The integrated circuits (ICs) in this kit are susceptible to damage from static electricity. There is no cause to worry if afew precautions are taken:

1. Use the sockets supplied with this kit. Never solder the ICs directly to the board. Keep the ICs in their protective packing until you are ready to plug them in their sockets.
2. Never insert or remove the ICs or do any soldering with power applied to the board.
3. Use a soldering iron with a properly grounded tip.
4. Carpets and clothing of man-made materials, and synthetic soles on shoes, are prone to building up a static charge. Ground yourself by touching a large object, preferably metallic, prior to touching the ICs. If you do get a shock, try changing your clothing.

## COMPONENT IDENTIFICATION

Before you start assembly, check the components against the parts list and make sure you know what each part is and where it is located on the board. Some parts need to go in a certain direction:

1. The ICs have one end identified by a notch, and/or a spot or dimple next to pin 1. Note that all of the ICs on this board, except for U14, face the same way on the board, i.e. with their notches towards the right side of the board. U14 has its notch towards the top of the board. The IC sockets do not have to go in a particular way, you might like to put the bevelled corner on some sockets or the end with the notch or semicircle the same way as the notches on the ICs.
2. The electrolytic capacitors C1, C2, C29 and C30 will contain designators on their package. Normally this will be a + symbol, however, be sure that proper polarity is observed when installing these devices.
3. The resistor packs RP1, RP2 and RP3 have a common end marked with a dot or notch. These should go towards the end marked with the double line.
4. The 16MHz crystal oscillator must match the notched end on the board at U16. This mark on the oscillator package may be a dot, or a circled M if it is a Motorola part. Extra care should be used when installing this part as failure to properly install the crystal could result in serious damage to the kit.
5. The remainder of the resistors and capacitors may be put in either way.

## CIRCUIT BOARD ASSEMBLY

The circuit board is supplied with one side printed with all the component locations. This is the side that the components go on. All soldering is done on the other side which is coated with a green solder resist that keeps the solder away from where it is not needed. The exception is the edge connector which should be kept free of solder to ensure a reliable connection to the mother board. Inspect the PC board for shorts by holding it up to strong light. We suggest you assemble the components in the following order:

A handy trick to help you is to insert all of the sockets into the board first, then place a flat piece of styrofoam firmly against the tip of the board. Turn it over, holding the styrofoam piece tightly against the board. Press the board down, forcing the sockets into the styrofoam. Now solder alternating corner pins of the IC sockets to hold them in place. Turn the board over and inspect it to determine that all ICs are down flat. If you find any that are not down flat, melt the solder joints at the corners and press it down against the board. Make sure all pins are sticking through the board and then solder them in place.

## 1. IC SOCKET INSTALLATION

Installing IC sockets in their proper locations is easiest if you start with the larger sockets first and finish with the smallest. If you follow this order, sockets should not be placed in the wrong positions. Socket installation should be as follows:

A) () One 40 pin socket at location U14

B) () Seven 20 pin sockets at locations:

| | |
|---|---|
| () U5 | () U6 |
| () U8 | () U20 |
| () U24 | () U25 |
| () U26 | |

C) () Seven 16 pin sockets at locations:

| | |
|---|---|
| () U12 | () U15 |
| () U19 | () U21 |
| () U22 | () U23 |
| () U28 | |

D) () Eleven 14 pin sockets at locations:

| | |
|---|---|
| () U2 | () U3 |
| () U4 | () U7 |
| () U9 | () U10 |
| () U11 | () U13 |
| () U17 | () U18 |
| () U27 | |

E) () One 8 pin socket at location U1

## 2. RESISTOR INSTALLATION

A) () Install two 47K resistors (yellow, violet,orange) at locations R3 and R4. The R3 and R4 locations can be found between U15 and U21. Solder them in place.

B) () Install two 10K resistors (brown, black, orange) at locations R1 and R2. The R1 and R2 locations can be found on the right side of U14. Solder them in place.

## 3. SIP RESISTOR INSTALLATION

A) () Install the two 1K SIP resistors at locations RP1 and RP2. The RP1 and RP2 locations are above U5 and U6. Be sure to observe polarity when installing these SIP resistors. The end of the SIP resistor marked with a dot or a notch should be aligned towards the end marked with the double line on the PC board.

B) () Install the 150 ohm SIP resistor at location RP3. The RP3 location is above U8. Be sure to observe polarity when installing this SIP resistor. The end of the SIP resistor marked with a dot or a notch should be aligned towards the end marked with the double line on the PC board.

## 4. CAPACITOR INSTALLATION

A) () Install twenty-eight .1 uf capacitors and solder them in place at the following locations:

| | | |
|---|---|---|
| () C3 | () C12 | () C21 |
| () C4 | () C13 | () C22 |
| () C5 | () C14 | () C23 |
| () C6 | () C15 | () C24 |
| () C7 | () C16 | () C25 |
| () C8 | () C17 | () C26 |
| () C9 | () C18 | () C27 |
| () C10 | () C19 | () C28 |
| () C11 | () C20 | |
| () C12 | () C21 | |

No polarity need be observed when installing these capacitors.

B) () Install three 1.5 uf tantalum capacitors and solder in place at locations:

| | | |
|---|---|---|
| () C1 | () C2 | () C29 |

**Be sure to observe proper polarity when installing these capacitors.**

C) () Install 47 uf electrolytic capacitor and solder in place at location C30. **Be sure to observe proper polarity when installing these capacitors.**

## 5. VOLTAGE REGULATOR INSTALLATION

A) () **Prior to installing VR1, place a drop of silicon greese heat compound on the reverse side of the 7812 to insure proper heat transfer during operation.** Following the application of the silicon greese, install VR1 using the 6/32 screw and nut. Solder in place. Note: A heat sink is not needed with this part.

B) () **Prior to installing VR2, place a drop of silicon greese heat compound on the reverse side of the 7805 to insure proper heat transfer during operation.** Following the application of the of the silicon greese, install the 7805 voltage regulator at VR2 with the heat sink. Tighten the

regulator and heat sink down with the 6/32 screw and nut and solder in place.

## 6. CRYSTAL INSTALLATION

A) () Install the 16MHz crystal oscillator at location U16. This 16MHz crystal oscillator package must match the notched end of the board at U16. This may be a dot or a circled M if a Motorola part. ****** NOTE **** FAILURE TO OBSERVE PROPER POLARITY POSITIONING OF THIS CRYSTAL PACKAGE CAN RESULT IN SEVERE DAMAGE TO THE UFDC BOARD.********

## 7. MISCELLANEOUS

A) () Install the 34 pin header at location J2. Solder in place.

B) () Install the 50 pin header at location J3. Solder in place.

C) () Install the wire wrap pins for Drives A, B, C, and D. The holes for these wire wrap positions are located just above RP1 and RP2.

## 8. TESTING

The completed board should now be check very thoroughly for stray blobs of solder, cold solder joints, leads not trimmed, etc. Also make sure that all components are in the right locations and placed in in the correct direction. Make sure that there are no shorts on the board that could seriously damage your system. Before installing the ICs in the sockets plug the board into your system on an extender card and check for proper voltages at the output (pin o) of the regulators VR1 and VR2. You should have +5 volts at VR2 and +12 volts at VR1. If you do not have the correct voltages, inspect the board for solder bridges, cold solder joints etc. Be sure that C1 and C2 are in correctly. Make sure any problems found are corrected before proceeding.

## 9. IC INSTALLATION

Install the ICs in their sockets. Be careful putting the ICs in their sockets so as not to bend any pins under the packages. Observe the proper positioning of pin one at all times. A major source of problems are ICs in the wrong location, bent pins or ICs put in incorrectly.

Following the initial testing of the boards voltages, installation of the ICs in their sockets should be as follows:

| | | |
|---|---|---|
| () U1 - 9216 | () U10 - 7400 | () U19 - 74LS174 |
| () U2 - 74LS74 | () U11 - 7404 | () U20 - 74LS240 |
| () U3 - 7414 | () U12 - 74139 | () U21 - 74LS [illegible] |
| () U4 - 74LS74 | () U13 - 7432 | () U22 - 74LS161 |
| () U5 - 74LS240 | () U14 - FDC1795-02 | () U23 - 8131 |
| () U6 - 74LS240 | () U15 - 74LS221 | () U24 - 74LS240 |
| () U7 - 7406 | () U16 - 16MHZ CRYSTAL | () U25 - 74LS240 |
| () U8 - 74LS244 | () U17 - 7432 | () U26 - 74LS240 |
| () U9 - 7407 | () U18 - 74LS240 | () U27 - 7400 |
| | | () U28 - 74LS195 |

You have completed the assembly of the UFDC-I. If you took care in building this kit you can expect the board to function when it is inserted into the S-100 bus in your system provided you have operational software that is compatable with this controller.

Refer to the user manual for further installation instructions.

# PARTS LIST

## RESISTORS

| LOCATION | VALUE | MARKINGS | (MFG) |
|---|---|---|---|
| R1 R2 | 10K | Brown Black Orange | |
| R3 R4 | 47K | Yellow Violet Orange | |

## RESISTOR PACKS

| | | | |
|---|---|---|---|
| RP1 RP2 | 1K | 10-1-102 10 PIN SIP | (BOURNS) |
| RP3 | 150 OHM | 10-1-151 10 PIN SIP | (BOURNS) |

## CAPACITORS

| | | | |
|---|---|---|---|
| C1 C2 C29 | 1.5uf | Tantalum radial leads 25V | |
| C3-C28 | .1uf | 104Z | |
| C30 | 47uf | Electrolytic | |

## ICs

| | | | |
|---|---|---|---|
| U1 | 9216 | Data Separator | (SMC) |
| U2 U4 | 74LS74 | Dual D Flip Flop | |
| U3 | 7414 | Hex Schmitt Trigger | |
| U5 U6 U20 U24 U25 U26 | 74LS240 | Octal Inv Bus/line Drvr | |
| U7 | 7406 | Hex Buffer | |
| U8 | 74LS244 | Octal 3 Stat Drvr | |
| U9 | 7407 | Hex Buffer | |
| U10 U27 | 74LS00 | Quad 2-IN NAND | |
| U11 | 74LS04 | Hex Inverter | |
| U12 | 74139 | Dual 1 0f 4 Dcodr/Dmxlr | |
| U13 U17 | 74LS32 | Quad 2-IN OR Gate | |
| U14 | 1795B-02 | Floppy disk controller | (WD) |
| U15 | 74LS221 | Dual Mono Multi | |
| U18 | 74LS260 | Dual 5-IN NOR Gate | |
| U19 | 74LS174 | Hex D Flip Flop W/CLR | |
| U21 | 74LS157 | Quad 2-IN Mltplxr | |
| U22 | 74LS161 | 4-Bit BI Cntr Async | |
| U23 | 8131 | 8-Bit Comparitor | |
| U27 | 74LS195 | 4-Bit Shift Reg | |
| U16 | 16MHz | Crystal Oscillator | (MOTOROLA) |

## REGULATORS

| | | |
|---|---|---|
| VR1 | 7812 | +12 Volt Regulator |
| VR2 | 7805 | +5 Volt Regulator |

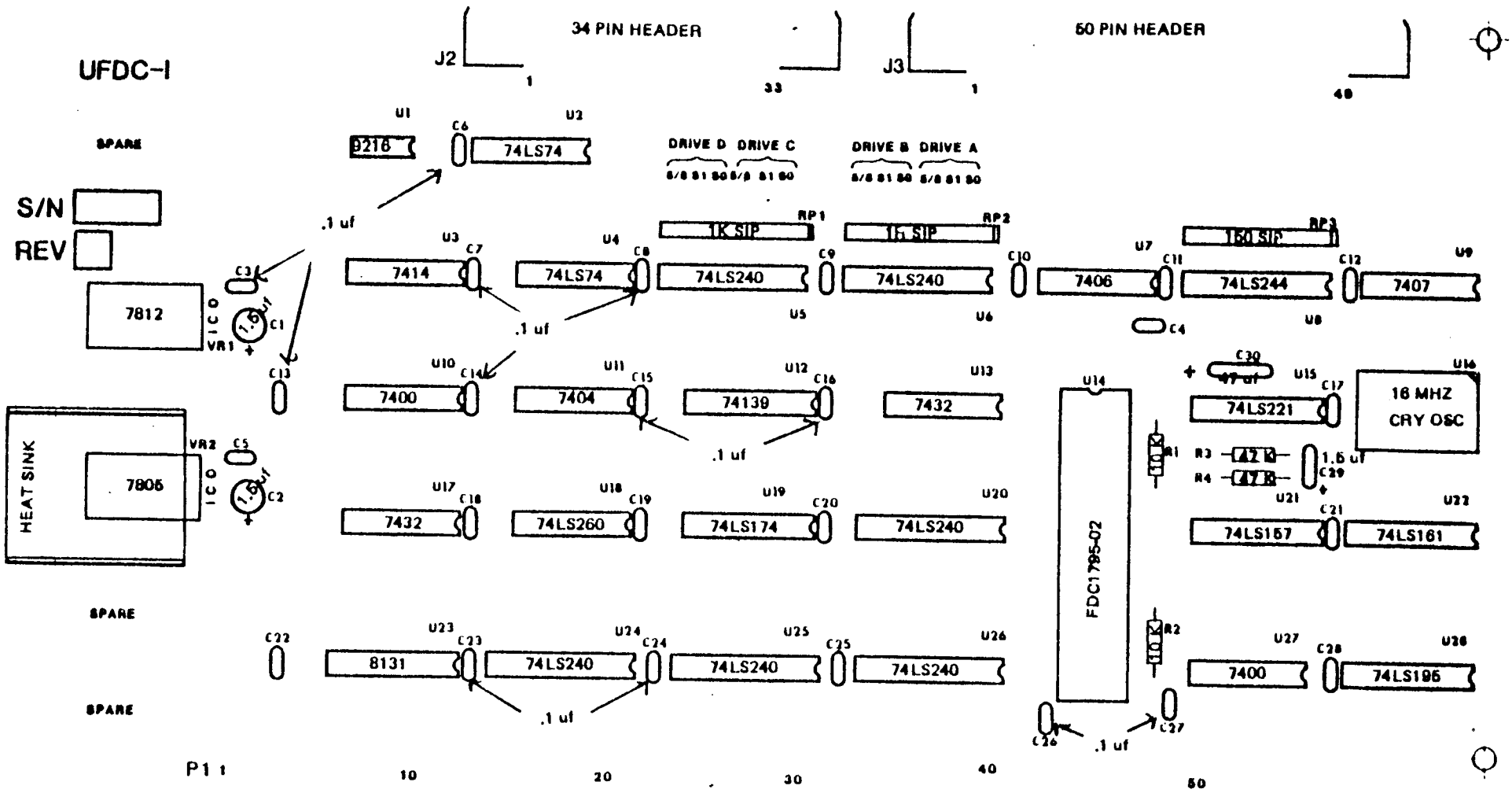
## OTHER COMPONENTS

| | | |
|---|---|---|
| VR2 | HEAT SINK | |
| J2 | HEADER | 34 Pin Header |

| | | |
|---|---|---|
| J4 | HEADER | 50 Pin Header |
| VR1 | 6/32 3/8" | Screw |
| VR1 | 6/32 1/4" | Nut |
| VR2 | 6/32 3/8" | Screw |
| VR2 | 6/32 1/4" | Nut |
| 24 | WW PINS | Wire Wrap Pins |

SOCKETS

| | | |
|---|---|---|
| 1 | 40 PIN | Low profile |
| 7 | 20 PIN | Low profile |
| 7 | 16 PIN | Low profile |
| 11 | 14 PIN | Low profile |
| 1 | 8 PIN | Low profile |


UFDC-I
34 PIN HEADER
J2
1
33
50 PIN HEADER
J3
1
49
SPARE
S/N
REV
7812
VR1
C3
C1
C13
HEAT SINK
7805
VR2
C5
C2
SPARE
SPARE
P1 1
10
20
30
40
50
U1
9216
C6
U2
74LS74
.1 uf
DRIVE D
DRIVE C
DRIVE B
DRIVE A
RP1
1K SIP
RP2
1K SIP
RP3
150 SIP
U3
7414
C7
U4
74LS74
C8
C9
U5
74LS240
U6
74LS240
C10
U7
7406
C11
C4
U8
74LS244
C12
U9
7407
.1 uf
U10
7400
C14
U11
7404
C15
U12
74139
C16
U13
7432
.1 uf
U14
FDC1795-02
C30
47 uf
U15
74LS221
C17
U16
16 MHZ
CRY OSC
R1
10K
R3
47 K
R4
47 K
1.6 uf
C29
U17
7432
C18
U18
74LS260
C19
U19
74LS174
C20
U20
74LS240
U21
74LS157
C21
U22
74LS161
R2
10K
C22
U23
8131
C23
U24
74LS240
C24
U25
74LS240
C25
U26
74LS240
.1 uf
C26
C27
U27
7400
C28
U28
74LS196