COMPU/TIME

CT256-I DYNAMIC RAM MEMORY BOARD

REFERENCE MANUAL

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1.0 Features Overview

The CT256-I dynamic RAM memory board represents a significant advance in memory size and memory management capability for 8-bit, S-100 organized systems. The CT256-I supports the following advanced features:

- 64K Bytes to 256K Bytes using 64K X 1 DRAM memory chips

- 256K Bytes to 1M Byte using 256K X 1 DRAM memory chips

- Full IEEE-696 S100 bus support, including:

  . 24 bit addressing
  . Phantom mode option
  . Error trap option

- Memory management capability to allow the addressing of a full one megabyte of RAM for systems generating only a 16-bit address

- Memory mapping on 16K or 64K boundaries

- Flexible parity generation and detection capabilites:

  . Parity latch and LED error indicator
  . Optional interrupt on parity error
  . Optional error trap on parity error
  . Parity available on input status port

- Refresh cycles performed transparently to system

- Refresh during processor wait states or reset can be enabled through a jumper option, allowing use with systems incorporating a front-panel.

- Onboard M1 wait state generator allows use of the CT256-I in systems with clocks up to 6 MHz.

- Board operates at 4 MHz with no wait states.

- Options provided for use of 200ns or 150ns RAMs.

6.0 System Limitations

The CT256-I was designed for optimum performance in systems using 8-bit processors. There is never contention between processor access to memory and refresh cycles as the memory always performs a refresh during the instruction decoding period when the processor is not using the bus. Many 16-bit processors and some advanced 8-bit processors (e.g. Intel 8088) perform an instruction pre-fetch in parallel with the previous opcode decoding. The CT256-I will not operate in this environment due to the contention for memory that would arise.

2.0 CT256-I Organization and Functional Overview

The CT256-I consists of three functional modules: the Bus Interface logic, the Memory Control logic, and the Memory Array itself. These modules will be discussed from a functional viewpoint in this section, their application will be discussed in following sections.

2.1 Bus Interface Overview

The bus interface logic provides for signal conditioning and decoding both from and to the system bus. The CT256-I uses the PWR/ (the "/" character indicates a signal that is active in the logic 0 state), M1, MREAD, and SOUT S-100 signals to derive the majority of the internal timing chain. The PWR/ signal in particular is used to initiate the memory write cycle.

The S-100 Data-In and Data-Out lines are buffered from the bus and the Data-In (with respect to the processor) lines are latched as well. This latching of the data to be read by the processor allows refresh to occur internally while the processor completes a read cycle.

The POC/ signal is brought onto the CT256-I to clear the parity latch and to potentially allow refresh to continue while the system is in a reset state. The RDY and XRDY lines are also brought in to detect the presence of wait states, and to allow refresh during these states to continue.

All 24 S-100 address lines are brought onto the CT256-I, however lines A14 through A19 are available for jumpered options (see section 3.0, Configuration Options). The CT256-I also has the capability of generating A16 through A19 from a 16-bit address, and these additional address lines can be made available to the bus for cascading up to three additional CT256-Is.

Four I/O ports are used by the CT256-I for loading the map registers and for reading their contents, these ports are fixed at addresses 88H-8BH. The operations allowed on the map registers will be detailed in section 5.0.

2.2 Memory Control Logic Overview

The memory control logic is used to sequence the memory array through the proper states to allow read, write, and refresh cycles to occur. The majority of this function is provided by the DP8409 Multi-Mode Dynamic RAM Controller/Driver chip. This chip has several modes of

operation, however the modes which are used on the CT256-I are mode 4 for read and write cycles, and mode 0 for external refresh requests.

Using mode 4 on the DP8409 allows all dynamic RAM access timing parameters to be controlled externally. This is done so that these timing parameters can be optimally generated by digital delay lines onboard the CT256-I. To provide the optimal memory cycle times for either 150ns or 200ns RAM chips, a jumper is installed enabling the proper delay output from the delay lines (see section 3.0).

Refresh timing is also provided externally in mode 0, this allows refresh to occur transparently to the system. Transparent refresh is accomplished by detecting a fetch (M1) cycle and automatically initiating a refresh cycle after the fetch data has been latched to the Data-In lines. Refresh during reset or extended wait states is provided as a jumperable option and is accomplished through an independent refresh timer.

2.3 Memory Array and Parity Logic Overview

The memory array consists of from 9 to 36 dynamic RAM chips and two parity generators/checkers. Either 64K X 1 or 256K X 1 DRAM chips with industry standard JEDEC pinout may be used for the RAM array. The array is organized as four banks of 9 bits, 8 bits of data plus one parity bit.

Parity is automatically generated during write cycles and stored in the ninth bit of each bank. Even parity is generated and stored in this implementation. During read cycles the parity stored when the byte was written is compared with the parity of the byte being read and an error bit is latched if the compare fails. This parity error bit will light the parity error LED on the card edge and will be available as bit 7 from the status port. An output to the status port with bit 7 low will reset the parity latch, as will a system reset.

3.0 Configuration Options

The CT256-I provides considerable flexibility in configuration through the use of jumperable options. These options allow the CT256-I to be configured to meet the memory requirements for almost any application. The followingparagraphs will detail the options available and give some jumper connections for typical applications.

JP 1-6: located above U24 at left bottom of board.

These jumpers determine the compare value input to the extended address comparator at U24. Connecting the jumper will cause a compare to 0 to be true, leaving the jumper open will cause a compare to 1 to be true. Jumper 1 inputs the compare value for address line A23, jumper 2 inputs the compare value for address line A22, jumper 3 inputs the compare value for address line A21, jumper 4 inputs the compare value for address line A20, jumper 5 inputs the compare value for address line A19, jumper 6 inputs the compare value for address line A18.

These jumpers only need to be installed for systems that generate a full 24 bit address, and where more than one CT256-I is used.

JP 7and 8: located below U24 at left bottom of the board.

These two jumpers determine whether or not address lines A18 and A19 will be used in the extended address comparison. This would be the case in a system using 64K X 1 RAMs and using more than one CT256-I. For a system using 256K X 1 RAMs, connect C to B for both JP7 and 8 and connect A to B for JP5 and 6. For a system using only one CT256-I, these jumpers are not used.

JP 9: located at the bottom left next to U24

This jumper is used to direct the output of the extended address comparator to the board select circuit and subsequently to the chip select input of the DP8409 DRAM Controller. If only one CT256-I board is to be used in the system, connect B to C; this effectively removes the extended address comparator from the logic, and the 8131 at U24 can be physically removed if desired. If more than one CT256-I board is to be used in the system, connect A to B.

JP 10 and 11: located below U1 in the center of the board

These jumpers determine the source of the row 8 and column 8 inputs to the DP8409. Row 8 and column 8 are only used for 256K X 1 DRAMs. Jumpering A to B allows the inputs to come from the map register bits MA18 and MA19; in a system with extended addressing, JP 7 and 8 position A should be jumpered to JP 10 and 11 position B to provide a direct addressing capability.

JP 12 and 13: located right of U1 in the center of the board

These jumpers determine the bank select inputs to the DP8409. Jumpering JP 12 A to B will select extended address bit A17 as the input to the high order bit of the two bank select bits. Jumpering JP 12 C to B will select map register address bit MA17 as the input. This applies as well to JP 13, extended address bit A16, map register address bit MA16, and the low order bank select input bit. For a minimal system of one bank of 64K DRAMs, jumper C to B and remove the 74170s at U7 and U8. This will always select bank 3.

JP 14 and 15: located right of U1 in the center of the board

These jumpers determine the column 6 and column 7 inputs to the DP8409. In systems with extended address capability, connect A to C for both JP 14 and JP 15. For systems using 16 bit addresses, connect C to B for both JP 14 and JP 15.

JP 16: located at the bottom of the board under memory chip A1

This jumper either enables or disables the output of the onboard wait state generator to the RDY line of the S-100 bus. Connect position A to B only if the CT256-1 is to be used in a system with a 6 MHz system clock.

JP 17: located at the top right between U4 and U5

This jumper either enables or disables the onboard optional refresh timer. This timer can provide memory refresh cycles during extended wait states or system resets. This option is usually enabled, to do so connect position A to B.

JP 18: located at the top right between U2 and U3

This jumper allows the selection of the memory cycle time for either 150ns or 200ns DRAM chips. If your board uses 150ns chips, connect position C to B; if your board uses 200ns chips, connect position A to B.

The Parity Error Flag: located just above U13

The parity error flag is available to be jumpered to any of eight vectored interrupt lines on the S-100 bus, or to the NMI/, INT/, or TRAP lines on the bus. Whether or not an interrupt is to be generated on parity error, and which interrupt is to be asserted is an implementation dependent option.

4.0 Typical Jumper Configurations

The following four sections will give the jumper connections for four typical memory board configurations. This is by no means an exhaustive presentation of the possible configurations for the CT256-I.

4.1 64K Minimal Configuration.

This configuration represents the smallest amount of memory which may be supported by the CT256-I. This configuration is composed of nine 64K X 1 DRAMs, providing 64K bytes of RAM with parity. The DRAM chips should be placed in bank D on the board.

Jumpers JP1 through JP8: not used (U24 may be removed)

Jumper JP9: Connect B to C

Jumpers JP12 and JP13: Connect B to C

Jumpers JP14 and JP15: Connect A to B

Jumper JP16: Connect only in 6MHz system

Jumper JP17: Connect A to B for transparent refresh

Jumper JP18: Connect A to B for 200ns DRAMs, otherwise connect B to C for 150ns DRAMS.

This configuration does not make use of the memory management capabilities of the CT256-I, therefore the 4 X 4 register file chips at U7 and U8 should be removed so that their outputs will be pulled high.

4.2 256K Configuration using 64K X 1 DRAMs

This configuration employs a fully populated CT256-I in a system providing a 16-bit address. The CT256-I generates address bits A16 and A17 from the map registers. Using this configuration the board will occupy contiguous memory addresses from hex 00000 to 3FFFF.

Jumpers JP1 through JP8: Open (not used)

Jumper JP9: Connect B to C

Jumpers JP12 through JP15: Connect B to C

Jumper JP16: Connect only in 6MHz system

Jumper JP17: Connect A to B for transparent refresh

Jumper JP18: Connect A to B for 200ns DRAMs, otherwise connect B to C for 150ns DRAMS.

The register file at U7 which ususally provides mapped address bits A18 and A19 is not used in this configuration and should be removed.

4.3 256K Configuration Using 64K Bank Select

This configuration provides 256K bytes of RAM using a bank switching method to allow compatibility with software which may expect this memory organization. This configuration does not use the low order two bits of the map registers; this should be considered when determining the map register contents (refer to section 5.0).

Jumpers JP1 through JP8: Open (not used)

Jumper JP9: Connect B to C

JumpersJP10and JP11: Connect A to B

Jumpers JP12 and JP13: Connect B to C

Jumpers JP14 and JP15: Connect A to B

Jumper JP16: Connect only in 6MHz system

Jumper JP17: Connect A to B for transparent refresh

Jumper JP18: Connect A to B for 200ns DRAMs, otherwise connect B to C for 150ns DRAMS.

The register file at U7 which ususally provides mapped address bits A18 and A19 is not used in this configuration and should be removed.

4.4 128K Configuration in 64K System

This configuration can be employed in a system with a 64K address space and not requiring a full 256K of memory. This configuration utilizes 64K X 1 DRAMs which should be placed in banks C and D on the board.

Jumpers JP1 through JP8: Not used

Jumper JP9: Connect B to C

Jumpers JP10 and JP11: Open

Jumper JP12: Open

Jumpers JP13 through JP15: Connect B to C

Jumper JP16: Connect only in 6MHz system

Jumper JP17: Connect A to B for transparent refresh

Jumper JP18: Connect A to B for 200ns DRAMs, otherwise connect B to C for 150ns DRAMS.

4.5 1 Megabyte Configuration using 256K X 1 DRAMs

This configuration represents the maximum amount of memory which may be supported by the CT256-I board. This configuration uses 256K X 1 dynamic RAM chips which should be available in 1983. This configuration assumes that a 24-bit address is generated by the system.

Jumper JP1 through JP4: Connect so as to place the address space of this board in an unoccupied region of memory.

Jumper JP5 and JP6: Connect A to B

Jumper JP7 and JP8: Connect B to C

Jumper JP9: Connect A to B

Jumpers JP10 and JP11: Connect JP10 position B to JP7 position A, connect JP11 position B to JP8 position A

Jumpers JP12 through JP15: Connect A to B

Jumper JP16: Connect only in 6MHz system

Jumper JP17: Connect A to B for transparent refresh

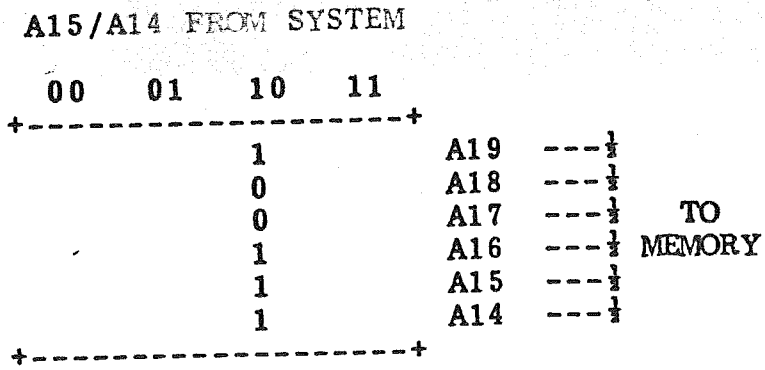
Jumper JP18: Connect A to B for 200ns DRAMs, otherwise connect B to C for 150ns DRAMS.

The above configurations are only examples, careful consideration of the memory requirements of your application may lead to the use of alternate configurations. Consult the schematic drawings in Appendix III and sections 3.0 and 5.0 when choosing alternate configurations.

5.0 Memory Management and Programming Considerations

The CT256-I provides the capability of mapping any 16K block of memory in its 256K address space onto any 16K block in a 64K address space. This allows an 8-bit processor generating a 16-bit address to use a full 256K of RAM (1 Megabyte with 256K X 1 DRAMs).

This mapping is accomplished by writing a map vector to the mapping registers through I/O ports 88H through 8BH. These mapping registers are organized as 4 words of 6 bits. The low-order 6 bits written to each I/O port will generate corresponding addresses A14 through A19 during memory access to the CT256-I. Which address map vector is output as A14 - A19 is determined by system address lines A14 and A15. This is best illustrated graphically:



The figure above indicates that if the system generates an address in which A15 is 1 and A14 is 0 (the range from 8000 - BFFFH) the map vector '100111' will be output as A19 - A14 on the memory address bus. This map vector would have been written to I/O port 8AH as the value 27H (the high order two bits would be zero). By writing values from 00 - 3FH to I/O port 8AH, the entire 1 MB of memory could be windowed in 16K increments through system addresses 8000 - BFFFH.

The above discussion holds true as well for the other three mapping registers, which can map the entire CT256-I memory into the other three 16K blocks of a 64K address space (0000 - 3FFFH, 4000 - 7FFFH, and C000 - FFFFH). It should be noted that only four of the six map vector bits are used in a 256K system, the high-order two bits corresponding to address lines A18 and A19 are not used and do not need to be written to the mapping registers.

5.1 Reading the Mapping Registers

The great flexibility offered by the use of the address mapping registers to generate extended addresses has resulted in a slight increase in the complexity of reading

these registers. The read select lines for the register files which comprise the mapping registers are derived from system address lines A14 and A15; therefore, to read these registers it is required that the appropriate bits be placed on lines A14 and A15 while performing an I/O input on the status latch.

The Z80 microprocessor provides this facility through the register addressed input instruction. This instruction places the value of the B register on system address lines A8 through A15, while placing the I/O port address on address lines A0 through A7. The figure below illustrates how reading of the contents of the mapping registers may be accomplished.

To Read the Contents of the Mapping Register at:	Load Register B With:
88 H	00 H
89 H	40 H
8A H	80 H
8B H	C0 H

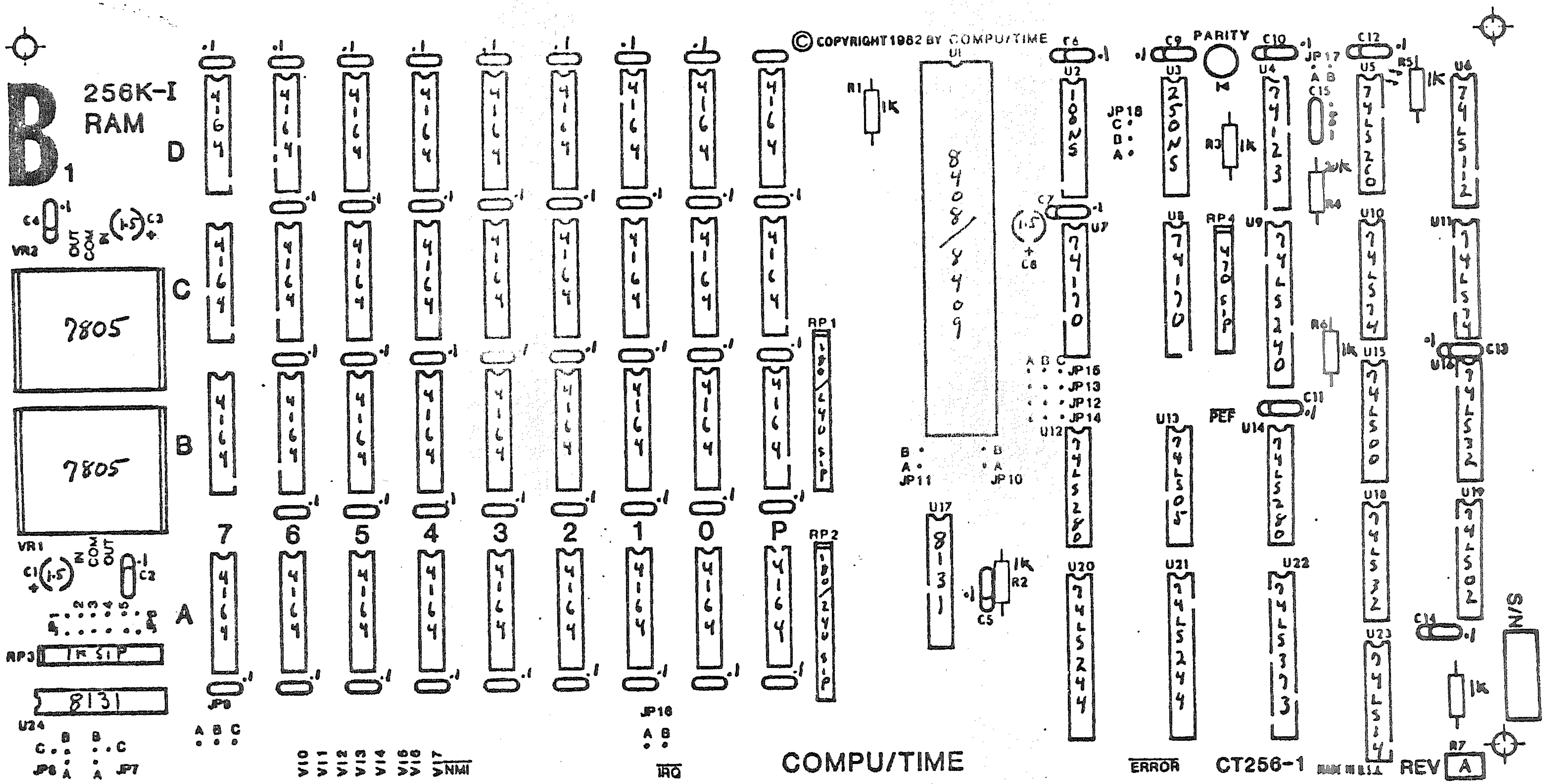
For example, to read the contents of the mapping register written to at I/O port 89H, execute the following instructions:

```
MVI     B,40H
MVI     C,89H
INP     A
```

This will place the value of the mapping register in the accumulator, and set the appropriate flags. The other mapping registers can be read in a similar fashion.

Note:
Any time a read operation is performed on one of the mapping registers the value of the parity error flip-flop will be returned in bit 7 (the high-order bit). A write to any of the mapping registers with bit 7 low will automatically reset the parity error flip-flop.

APPENDIX I


B1
256K-I RAM
© COPYRIGHT 1982 BY COMPU/TIME
PARITY
COMPU/TIME
CT256-1
REV A
ERROR
S/N
7805
7805
8131
8408/8409

APPENDIX II

CT256-I

Assembly Instructions

Construction of the CT256-I from the bare board is intended for those who have experience in electronic assembly. If you do not have this experience we strongly suggest you obtain help in assembling this board.

Be sure you have the proper tools available: a soldering iron (20 W, 700 degree optimum tip temperature), Rosin Core solder (preferably 63/37), diagonal cutters, a flat blade screw driver and needle nose pliers.

CAUTION
USE EYE PROTECTION WHILE SOLDERING OR CUTTING WIRE

1. ( ) Check the parts received against the parts list (Appendix I). Some kits for smaller memory configurations may not have all of the DRAM chips or sockets indicated. If anything is missing contact Compu/Time and report the shortage.

2. ( ) Install the following sockets in the locations indicated, but DO NOT solder them at this time.

   14 pin sockets at: U5,U10-16,U18,U19,U23

   16 pin sockets at: U4,U6,U7*,U8*,U17,U24*,install 16 pin sockets in the memory array beginning with bank D. 64K Byte boards should use bank D alone.

   20 pin sockets at: U9,U20,U21,U22

   24 pin sockets at: U1, this is a 48 pin chip socket consisting of two 24 pin sockets.

   After all of the sockets have been inserted place a flat piece of cardboard or styrofoam over the sockets and turn the board over. Now solder alternate corner pins of each socket, i.e. pins 1 and 9 of a 16 pin socket. After this has been done for each socket, turn the board over and inspect each socket to determine that it has been seated flat against the board. If this is not the case, re-heat the two soldered pins while pressing down on the socket.

   Now solder the remaining pins of each socket. Do this carefully as the density of the board makes it easy to miss soldering a pin. After you have soldered all the pins, inspect each connection for solder bridges and cold joints.

3. ( ) Install the four SIP resistor packs in the

locations indicated on the board (RP1 - RP4). These packs are NOT interchangeable, be sure to install them properly. The resistor packs can be soldered to the board by a method like that used for the IC sockets.

4. ( ) Install and solder the six 1K resistors at locations R1-3 and R5-7.

5. ( ) Install and solder the 47K resistor at R4.

6. ( ) Install and solder the .001 uf capacitor at C15.

7. ( ) Install the two 5 volt regulators and heatsinks at VR1 and VR2 according to the following procedure: insert a 6-32 machine screw through the board from the solder side, place the heatsink over the screw and align it with the pattern on the board, place the regulator on the screw with the flat side of the regulator against the heatsink, place a lockwasher and #6 nut on the screw and tighten snugly without forcing. Carefully, using needle nose pliers, bend the leads of the regulator such that they can be inserted into the solder holes labeled "IN", "GND", and "OUT". Solder the leads to the board. Repeat this procedure for both regulators.

8. ( ) Install and solder three 1.5 uf tantalum capacitors at C1, C3, and C8. Be sure to observe the proper polarity of these caps as silk-screened on the board.

9. ( ) Install and solder .1 uf capacitors at C2, C4, C5-7, C9-14, and in the circled solder pads above the DRAM chip sockets.

10. ( ) Install and solder the parity error LED at LED1, the flat side of the LED indicates the cathode (negative) lead of the LED. Be sure to observe polarity.

11. ( ) Install and solder the wire-wrap pins or header pins in the locations JP1 - JP18.

Before continuing with the insertion of the ICs in the sockets, inspect the board carefully for shorts or opens caused by solder bridges or cold solder joints. Now insert the un-populated board into your system and check for the proper supply voltages. Pin 16 of U6 should show a voltage of 5 V plus or minus 0.5 V with respect to system ground. Check for 5 volts at pin 8 of the DRAMs also. If either of these checks fail to give the proper voltage, re-check the board for soldering errors. If both checks give the proper voltage continue with IC insertion.

All integrated circuits on this board (except U24) should be inserted with pin 1 toward the top of the board (away from the bus connector).

12. ( ) Carefully insert the DP8409 DRAM controller in the 48 pin socket at U1. Apply pressure evenly to the chip as it is being inserted.

13. ( ) Install the 100ns digital delay line at U2, the dot on the delay line indicates pin 1. Solder in place.

14. ( ) Install the 250ns digital delay line at U3. Solder in place.

15. ( ) Insert the following ICs at the indicated locations:

IC	Location
74123	U4
74260	U5
74112	U6
74170	U7*
74170	U8*
74LS240	U9
74LS74	U10
74LS74	U11
74280	U12
7406	U13
74280	U14
74LS00	U15
74LS32	U16
DM8131	U17
74LS32	U18
74LS02	U19
74LS244	U20
74LS244	U21
74LS373	U22
7414	U23
DM8131	U24*

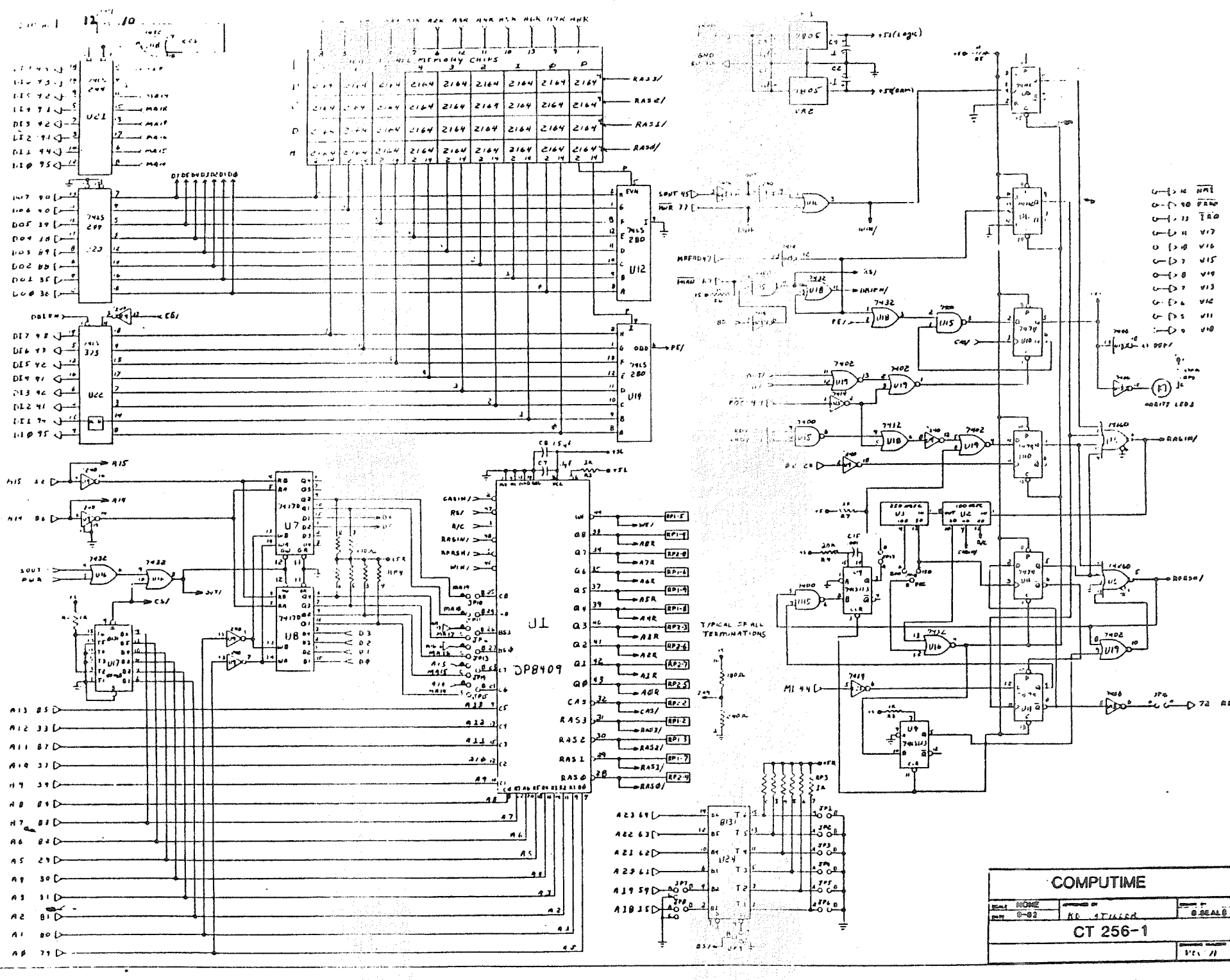
This completes the assembly of the CT256-I memory board.

* This part and associated socket may not be supplied with boards ordered with less than 256K of memory.

PARTS LIST

Part Number	Quantity	Description
C1,C3,C8	3	1.5 uf Tantalum Capacitor
C2,C4-7,C9-14, All filter caps above DRAMs	53	.1 uf Ceramic Disc Capacitor
C15	1	.001 uf Ceramic Disc Capacitor
R1-3,R5-7	6	1K ohm, 1/4 watt Resistor
R4	1	47K ohm, 1/4 watt Resistor
RP1,RP2	2	180/240 ohm SIP Resistor Pack
RP3	1	1K ohm SIP Resistor Pack
RP4	1	470 ohm SIP Resistor Pack
U1	1	DP8409 DRAM Controller/Driver
U2	1	100ns Digital Delay Line
U3	1	250ns Digital Delay Line
U4	1	74123 Dual One-Shot
U5	1	74260 Dual 4-In NOR
U6	1	74112 Dual JK Flip-Flop
U7,U8	2	74170 4X4 Register File
U9	1	74LS240 Octal Inverting Buffer
U10,U11	2	74LS74 Dual D Flip-Flop
U12,U14	2	74280 Parity Generator/Checker
U13	1	7406 Hex Inverter, Open Collector
U15	1	7400 Quad NAND Gate
U16,U18	2	7432 Quad OR Gate
U17,U24	2	DM8131 Hex Comparator
U19	1	7402 Quad NOR Gate
U20,U21	2	74LS244 Octal Buffer/Driver

U22	1	74LS373 Octal Latch
U23	1	7414 Hex Schmidt Trigger Inverter
VR1,VR2	2	7805 5 Volt Regulator (TO 220)
	9-36	2164/4164 64K X 1 DRAM Memory ICs
LED1	1	LED Parity Error Indicator
	11	14 pin Sockets
	42	16 pin Sockets
	4	20 pin Sockets
	2	24 pin Sockets (comprise U1)
	50	Wire-Wrap Pins/Headers
	2	Heatsinks
	2	6-32 Screws, Lockwashers, & Nuts


64K RAM MEMORY CHIPS
U21
U12
U14
U22
U7
U8
U1
DP8409
U24
COMPUTIME
CT 256-1