PROMBLASTER II

MANUAL

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3/11/84

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I. Introduction

The ads PROMBLASTER II is an S-100 compatible EPROM programming board. It appears to the computer as four I/O ports. The address, data and the amplitude and timing of the various programming pulses for each different EPROM size and family are controlled by software. Either 1k, 2k, 4k, 8K, 16k or 32k, 24 or 28 pin EPROMS may be programmed. The PROMBLASTER II has an on-card switching regulator to provide the high voltage for programming EPROMS. A one millisecond timing reference is also provided for controlling programming pulse widths. An elevated VCC capability has been added to provide Fast-Programming via manufacturer-supplied algorithms for some 8K and larger EPROMS. The ads PROMWRITER software provides full feature control of the PROMBLASTER II and is available under CP/M or OS9.

II. Configuring the PROMBLASTER II

1. The ads PROMBLASTER II is designed to work in a 1 MHZ system. For use in faster systems the onboard wait state generator must be used. If you require zero, one, two, three or four wait states for 1, 2, 4, 8 or 10 MHZ systems install the necessary jumper (WAIT STATES - 0,1,2,3,4) and select which of the two S-100 ready lines your system requires with jumper pRDY or xRDY.

2. The ads PROMBLASTER II may be used with standard (8 bit) or extended (16 bit) device addresses. For use in extended device address systems, use jumper (OP1 - A). For use in standard device address systems, use jumper (OP1 - B).

3. The ads PROMBLASTER II may be used with I.E.E.E. 696 or pre-standard CPU's. It is important to understand the differences in order to correctly configure the board. Most of the differences in timing occur in the operation of the pSTVAL* signal (pin 25). Many CPU's provide a clock signal, PHI 1, in place of pSTVAL* on the bus. This is acceptable as long as there is only one negative edge during the pSYNC interval that occurs after the address and status lines are valid. This is shown below:

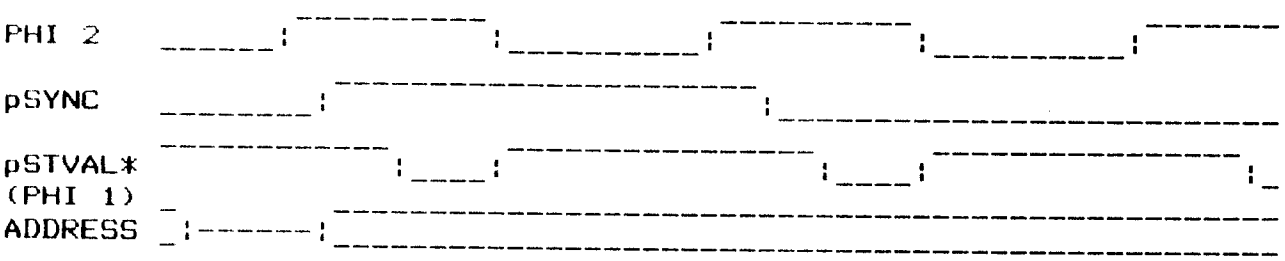


Figure 1. I.E.E.E 696 TIMING

Many PHI 1 signals don't meet this criterion. In the sample timing shown below there is a negative edge on PHI 1 during pSYNC

when the address and status lines are not valid. This can cause erroneous device selects and improper operation. For those CPU's that don't provide a correct pSTVAL* or PHI 1 signal a jumper has been provided to allow the use of PHI 2. As shown below, clocking the device select on the negative edge of PHI 2 during pSYNC provides correct timing:

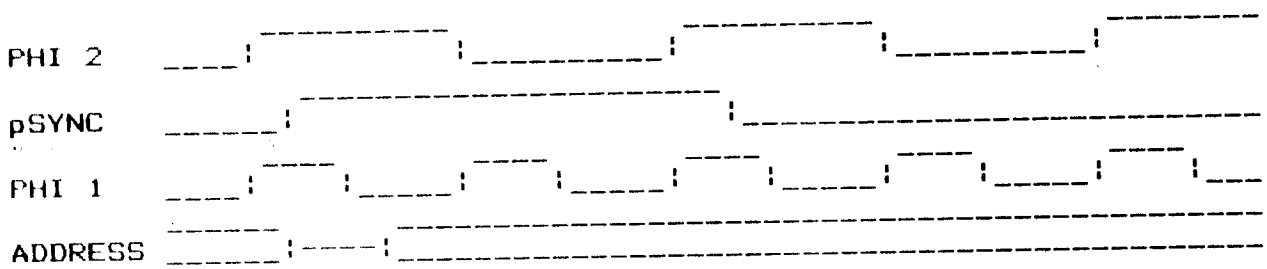


Figure 2. PHI 2 TIMING

There are also problems in the use of the PHI 2 signal. Some CPU's don't provide valid address and status prior to the negative edge of PHI 2 during pSYNC. For these cases a jumper is provided to allow the negative edge of pSYNC to clock the PROMBLASTER II. In all of the above cases the pSYNC signal was used to qualify the device select clock signal. However when pSYNC is used as the clock this qualification must be defeated. An example of this timing is shown below:

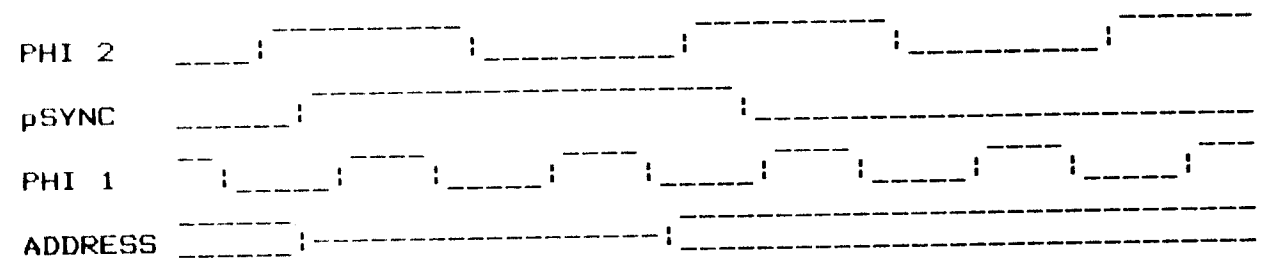


Figure 3. pSYNC TIMING

The desired clock signal is selected with OP2. The OP2-A jumper should be used when your CPU provides a correct pSTVAL* or PHI 1 signal that operates as per figure 1 above. The OP2-B jumper should be used when your CPU does not provide a pSTVAL* or a compatible PHI 1 signal, but has a PHI 2 signal that occurs during pSYNC after the address and status lines are valid. The OP2-D jumper allows you to choose the other edge of the PHI 2 clock by inverting this signal's sense. The OP2-C jumper should be used with those systems where the address and status lines are not valid during PHI 1 or PHI 2 but go valid prior to the end of pSYNC.

The desired clock qualifier signal is selected with OP3. The OP3-A jumper should be used with OP2-A, OP2-B or OP2-D to allow clocking only during the pSYNC interval. The OP3-B jumper

should be used with the OP2-C clock to always qualify the pSYNC clock signal.

4. The ads PROMBLASTER II provides an optional ground jumper for pin 53 on the S-100 bus. On some pre-standard CPU's pin 53 is the Sense Switch Disable line (SSDSB*). The I.E.E.E. 696 standard eliminates SSDSB* and defines pin 53 as an extra ground line. The OPT GND jumper on the PROMBLASTER II allows pin 53 to be a ground when connected or unaffected when disconnected.

5. The current shortage of LS logic has required us to provide jumpers for some of the IC locations to allow equivalent part substitutions. Jumpers JU1 and JU2 must be installed if devices U12 and U11 respectively are [redacted] [redacted] 74LS688 or 74LS689 comparators. Jumpers JU1 and JU2 must not be installed if devices U12 and U11 respectively are 74LS682, 74LS683, 74LS684 or 74LS685 comparators. If your PROMBLASTER II was purchased Assembled and Tested these jumpers should be correct for the parts installed in U11 and U12.

6. The PROMBLASTER II is now ready for use within your system. Select the group of four I/O addresses you want the board to respond to with switch S2. If you are using the extended device address option, you must also set switch S1 to the desired device page address. An open switch corresponds to a '1'. S2-6 is the most significant bit for the group of four I/O addresses, and S1-8 is the most significant bit for the extended device address. S2-7 and S2-8 are not used.

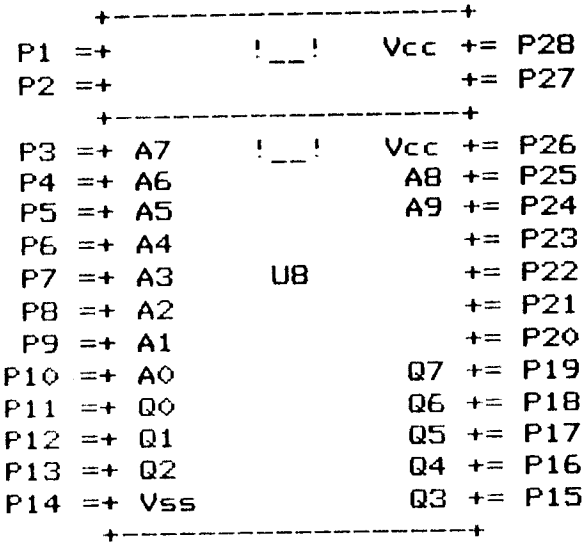
7. Install the board and verify that your computer and other I/O devices function normally.

III. Using the ads PROMBLASTER II

The ads PROMBLASTER II is controlled through four I/O ports. These are:

I/O Address	Read Function	Write Function
+ 00	Prom data in	Prom data out
+ 01	Not used	Prom A0-A7
+ 02	Timer status	Prom A8-A9, mode
+ 03	Reset timer	Prom hi volt control

In the following tables and descriptions the numbers P1-P28 refer to the pins on the device programming socket U8. Most EPROMs are functionally equivalent on many of their pins as shown on the following page:



I/O address + 00 provides an eight bit data path to or from the programming socket U8. Data written to I/O address + 00 is latched and is presented to the EPROM data outputs when enabled. Reading from I/O address + 00 causes the data present on the EPROM data outputs to be input to the CPU.

I/O addr	B7	B6	B5	B4	B3	B2	B1	B0	
+00	P19	P18	P17	P16	P15	P13	P12	P11	READ/WRITE

I/O address + 01 provides an address function. Data written to I/O address + 01 is latched and is presented to the EPROM programming socket U8 on the A0 through A7 pins.

I/O addr	B7	B6	B5	B4	B3	B2	B1	B0	
+01	P3	P4	P5	P6	P7	P8	P9	P10	WRITE

I/O addresses + 02 and + 03 are combined timing, address and voltage control ports. Data written to I/O address + 02 enables/disables the data to the EPROM, controls the levels at three pins of U8 programming socket, supplies A8 - A9 and selects a programming voltage MODE as well. Data written to I/O address + 03 enables/disables the A0-A7 lines to the EPROM, and controls the levels at six pins of U8. Reading from I/O address + 02 causes the status of the one millisecond reference to be returned to the CPU on bit 7. Reading from I/O address + 03 causes the one millisecond timing reference to be restarted. To minimize the number of control bits needed, the voltages on the pins of U8 have been encoded such that two bits of I/O address + 02 set the MODE of operation for many of the remaining bits. This is detailed in the tables on the following page:

I/O addr +02 & +03 WRITE FUNCTIONS

I/O addr	B7	B6	B5	B4	B3	B2	B1	B0	P28	P1	
	data		+5v	+5v		+5v					M
+02	out	1	P27	P2	1	P21	A9	A8			O
	dsbl		0v	0v		0v					D
	addr	+5v	+5v	+5v	+25v	+25v	+5v	1	+5v	+25v	E
+03	out	P23	P22	P20	P23	P22	P26				3
	enbl	0v	0v	0v	B6	B5	0v	0	+5v	+5v	
	data		+5v	+5v		+5v					M
+02	out	1	P27	P2	0	P21	A9	A8			O
	dsbl		0v	0v		0v					D
	addr	+5v	+5v	+5v	+21v	+21v	+5v	1	+6v	+21v	E
+03	out	P23	P22	P20	P23	P22	P26				2
	enbl	0v	0v	0v	B6	B5	0v	0	+5v	+5v	
	data		+5v	+5v		+5v					M
+02	out	0	P27	P2	1	P21	A9	A8			O
	dsbl		0v	0v		0v					D
	addr	+5v	+5v	+5v	+21v	+21v	+5v	1	+5v	+21v	E
+03	out	P23	P22	P20	P23	P22	P26				1
	enbl	0v	0v	0v	B6	B5	0v	0	+5v	+5v	
	data		+5v	+5v		+5v					M
+02	out	0	P27	P2	0	P21	A9	A8			O
	dsbl		0v	0v		0v					D
	addr	+5v	+5v	+5v	+12v	+12v	+5v	1	+6v	+12v	E
+03	out	P23	P22	P20	P23	P22	P26				0
	enbl	0v	0v	0v	B6	B5	0v	0	+5v	+5v	

I/O addr +02 READ FUNCTIONS

I/O addr	B7	B6	B5	B4	B3	B2	B1	B0	
	1 msec timer status	test circuit status			nu	nu	nu	nu	READ
+02		0	0		no HV on P1, P22 or P23				
		0	1		12.5v on P1, P22 or P23				
		1	0		21v on P1, P22 or P23				
		1	1		25v on P1, P22 or P23				
				0	5v on P28				
				1	6v on P28				

I/O addr +03 READ FUNCTIONS

I/O addr	B7	B6	B5	B4	B3	B2	B1	B0	
+03	Reset 1 millisecond timer								READ

Before an EPROM can be put into U8 the socket must be setup with the correct voltage configuration, the data outputs must be disabled, the address inputs should be disabled, and the chip select pin for the part should be made inactive. This is accomplished be loading the correct bit patterns into I/O addresses + 02 and +03. After placing the correct EPROM into U8, it may be read by latching the desired address into A0 - A7 via I/O address +01, setting up A8 - A?? via I/O addresses +02 and +03 and enabling the address to the EPROM. This is followed by making the desired chip select and/or output enable line active, again via I/O addresses +02 and +03, and then reading the data from the EPROM via I/O address +00.

Programming an EPROM involves more steps. After placing the EPROM into a properly configured U8 socket, the desired address is setup as for reading above. The EPROM must now be placed into programming mode. For single supply parts this may be as simple as raising the Vpp pin to +25v, +21v or +12.5v. For Fast-Programming the VCC on the part may have to be switched to +6v. The data to be programmed is latched into I/O address +00 and is enabled to the U8 socket. A programming pulse varying from one to fify milliseconds is then supplied to the EPROM. After this pulse, the data is disabled, a new address is supplied, and the process repeats. Single supply EPROMS may be programmed at any location randomly. Fast-Programming parts require an interactive algorithm that monitors the location's programability and supplies the appropriate overprogram pulse. A software example for Intel 2716 +5v EPROMS may be found in the Appendix.

IV. Helpful Hints

After writing PROMBLASTER II software, check out its operation with a scope or multimeter first. Observe the relationship, amplitude and timing of the signals present on the programming socket U8 before attempting to read or program your part. It is very easy to toggle the incorrect bit causing the PROMBLASTER II to apply the wrong voltage to the wrong pin. This may result in damage to the EPROM and/or PROMBLASTER II. Mode 3 is used for all 1k, 2k, and some 4k and 8k EPROMS. Mode 1 is provided for newer 4k and older 8k parts that require a +21v programming pulse. NOTE: THE LOWER SUPPLY VOLTAGES WILL ONLY BE PRESENT AT U8 WHEN THE ADDR OUT ENBL BIT 7 OF THE CONTROL REGISTER IS SET IN MODES 2, 1 & 0. A HALF SECOND DELAY SHOULD BE USED BEFORE ANY PROGRAMMING IS ATTEMPTED. Modes 2 and 0 are for

the newer larger EPROMS that utilize an elevated VCC of +6v and lower programming voltages of +21v and +12.5v for Fast Programming techniques. Note that through proper control it should be possible to read 24 and 28 pin ROMS as well, provided that you know the mask-programmed chip select levels.

The ads PROMWRITER software is a package written in 8080 assembly language for execution under CP/M. A version written in 'C' is also available. It provides the capability of programming 26 different EPROMS 1K, 2K, 4K, 8K, 16K and 32K parts, both 24 and 28 pin packages when used with the ads PROMBLASTER II. Some EEPROMS and single-chip microcomputers may be programmed as well. Commands are provided to read, program and verify EPROMS with optional offsets. Memory load, examine, display and sum functions as well as CP/M .HEX file load and store operations are also provided.

V. Parts List

Quantity	Indetifiers	Part	Description
	- INTEGRATED CIRCUITS -		
2	U15,U18	74LS02	QUAD 2 IN NOR
2	U17,U21	74LS04	HEX INVERTER
2	U13>U14	7406	HEX INVERTER OC HV
1	U19	74LS08	QUAD 2 IN AND
2	U10,U16	74LS27	TRIPLE 3 IN NOR
1	U22	74LS109	DUAL J-K* FLIP FLOP
1	U23	74LS195	QUAD SHIFT REGISTER
1	U9	74LS155	DUAL 2 TO 4 DECODER
2	U1>U2	74LS244	OCTAL BUS BUFFER
1	U7	74LS273	OCTAL D FLIP FLOP W/CLR
1	U25	74LS368	HEX BUS INVERTER W/3 S
3	U3,U4,U6	74LS374	OCTAL D FLIP FLOP W/3 S
2	U11>U12	-74LS682/683-	OCTAL COMPARATOR W/PULLS
		or 74LS684/685	OCTAL COMPARATOR
		[redacted]	
		or 74LS688/689	OCTAL COMPARATOR W/JU1,2
1	U20	-MC14020B	14 STAGE BINARY COUNTER
1	U26	TL497	SWITCHING REGULATOR
2	VR1>VR2	-LM340T-5	5V TO-220 REGULATOR
		or MC7805	" "
1	VR3	-LM340T-8	8V TO-220 REGULATOR
		or MC7808	" "
	- TRANSISTORS & DIODES -		
7	Q9>Q15	-2N2222/PN2222-	NPN GP TRANSISTOR
8	Q1>Q8	2N4403	PNP GP TRANSISTOR
13	CR1>CR13	1N4001	1A 50 PIV DIODE
1	Z1	-6.8v 1.5W-	Micro Semi 1N5921 Zener
2	Z2>Z3	-10v 500mW-	1N5240B Zener
2	Z4>Z5	-5.1v .5W-	1N5231B Zener

Parts List continued

	- RESISTORS		
1	- R69	- 2.7 OHM	- 1 WATT 5% RESISTOR
1	- R35	- 4.7 OHM	- 2 WATT 5% RESISTOR
2	- R63,R66	- 150 OHM	- 1/4 WATT 5% RESISTOR
1	- R34	- 220 OHM	- 1/4 WATT 5% RESISTOR
1	- R33	- 750 OHM	- 1/4 WATT 5% RESISTOR
8	-R3,R9>R10,R14	-1.2K OHM	- 1/4 WATT 5% RESISTOR
	- R24,R28	- " "	- " "
	- R77>R78	- " "	- " "
1	- R71	-1.21KOHM	- 1/4 WATT 1% RESISTOR
8	- R2,R4,R6,R8	-2.2K OHM	- 1/4 WATT 5% RESISTOR
	-R15>R16,R25,R41	" "	- " "
5	- R32,R40	-3.0K OHM	- 1/4 WATT 5% RESISTOR
	- R50>R51,R62	- " "	- " "
5	- R1,R5,R7,R12	-3.3K OHM	- 1/4 WATT 5% RESISTOR
	- R21	- " "	- " "
3	- R22,R29>R30	-4.7K OHM	- 1/4 WATT 5% RESISTOR
2	- R17>R18	-5.1K OHM	- 1/4 WATT 5% RESISTOR
4	- R19,R31	- 10K OHM	- 1/4 WATT 5% RESISTOR
	- R68,R74	- " "	- " "
1	- R11	-22.6KOHM	- 1/4 WATT 1% RESISTOR
3	- R23,R26>R27	- 24K OHM	- 1/4 WATT 5% RESISTOR
1	- R70	-24.9KOHM	- 1/4 WATT 1% RESISTOR
2	- RN1>RN2	- 47K OHM	- 10 PIN SIP RESISTOR
1	- R76	-118K OHM	- 1/4 WATT 1% RESISTOR
2	- R75,R13	-120K OHM	- 1/4 WATT 5% RESISTOR
	- CAPACITORS & COILS		
1	- C17	- 10 PFD	- CERAMIC DISC CAPACITOR 50V
1	- C13	- 330 PFD	- CERAMIC DISC CAPACITOR 50V
1	- C38	- 470 PFD	- CERAMIC DISC CAPACITOR 50V
1	- C16	-.002 UFD	- CERAMIC DISC CAPACITOR 50V
23	- C3,C4,C7,C10	- .01 UFD	- CERAMIC DISC CAPACITOR 50V
	- C12,C14	- " "	- " "
	- C20>C23	- " "	- " "
	- C25>C37	- " "	- " "
5	- C6,C8,C9,C11	- 4.7 UFD	- 35V TANTALUM CAPACITOR
	- C15	- " "	- " "
6	- C1>C2,C5	- 10 UFD	- 35V ALUMINUM CAPACITOR
	- C18>C19,C39	- " "	- " "
1	- L1	-200UH .2A-	MILLER 5254 INDUCTOR
1	- L2	-6.8MH .2A-	INDUCTOR SUPPLY LM3

Parts List continued

	- MISCELLANEOUS	-	
2	- S1,S2	-	- 8 POSITION DIP SWITCH
3	-	-	- THM6106 TO-220 HEATSINK
37	-	-	- BERG MINI-JUMP PINS
9	-	-	- BERG MINI-JUMPS
8	- U1>U4	-	- 20 PIN I.C. SOCKET
	-U6>U7,U11>U12	-	- " "
5	- U9,U20,U22	-	- 16 PIN I.C. SOCKET
	- U23,U25	-	- " "
10	- U10,U13>U19	-	- 14 PIN I.C. SOCKET
	- U21,U26	-	- " "
1	- U8	-	- 28 PIN L.I.F./Z.I.F. SOCKET
1	- LED	-	- RED LIGHT EMITTING DIODE 20MA
1	-	-	- 40 PIN RT. ANGLE HEADER
3	-	-	- 6-32 X 3/8 MACHINE SCREW
3	-	-	- 6-32 MACHINE SCREW NUT

VI. Theory of Operation

The ads PROMBLASTER II requires +8vdc and +16vdc from the I.E.E.E. 696 bus for its power supplies. The +8vdc is requlated by VR1, C7, C8 and C18 to provide +5vdc for the TTL & CMOS logic. It is also requlated by VR2, CR14, C9, C10 and C19 to provide +5.7vdc for the EPROM configuration logic. The +16vdc is requlated by VR3, C1, C3, C5 and C6 to provide +8vdc for the EPROM configuration logic and the DC to DC converter U26.

The high voltage required to program EPROMs is not available on the I.E.E.E. 696 bus. It is generated by a DC to DC converter formed by C2, C11, C12, C13, C14, C15, R69, R70, R71, L1, L2 and U26. This forms a step-up switching regulator with the frequency of operation controlled by C13 and the voltage sampled across R71 compared with an internal 1.2v reference. The resulting output voltage is filtered by C11 and C12 and current limited by R69 then supplied to the EPROM configuration logic.

The reset circuitry uses a portion of U19 to or the two I.E.E.E. 696 bus reset signals; POC* and SLAVE CLR*. The resulting signal clears the PROMBLASTER control register U7 and the device select flop U22. This tri-states the address and data lines to the programming socket U8 and resets any high voltages on the EPROM type-specific pins.

The I/O device cycle on the I.E.E.E. 696 bus is controlled by U9, U10, U11, U12, U16, U17, U21 and U22. The group of four device numbers set by switches S1 are compared with A2-A7 by U11. When a match is found, and the comparator is enabled by either sINP or sOUT via U18 it provides an enable signal to the section

of U10 driving the device select flop U22. If an extended address option is selected via OP1 the page address set by switches S2 are compared with A8-A15 by U12. This provides an additional enable to U10. The signals pSTVAL*, PHI 2, PHI 2~ or pSYNC may be selected to clock the device select flop U22 via clock option OP2. The data inputs to U22 may be qualified by pSYNC via OP3, U10 and U16.The qualified I/O cycle address match or mismatch is clocked into U22 to control a PROMBLASTER bus cycle.

A bus cycle wait-state generator is formed by U14, U21, U23 and U25. The four bit shift register U23 is cleared by pSYNC and clocked (shifted) by PHI 2. Taps are supplied to the I.E.E.E. 696 as either pRDY or xRDY via U25 when the PROMBLASTER is selected.

The device address A0-A1 is decoded by dual decoder U9 when enabled by a device select from U22. One half of U9 is strobed by the I.E.E.E. 696 data input strobe, pDBIN. The other half is strobed by the data output strobe, pWR* via U17. Thus depending on A0-A1 of the I/O read cycle, data input strobes are provided to; enable the U8 device data bus for input via U2, input the status of the one millisecond timer and test circuits via U25 or reset the one millisecond timer. Depending on A0-A1 of the I/O write cycle data output strobes are provided to; latch data to be provided to the device socket U8, latch address lines A0-A7 for the U8 socket, latch A8-A9 and the PROMBLASTER II mode bits and some of the EPROM configuration logic inputs into U6, or latch the remaining voltage control and EPROM configuration logic inputs into U7. Write cycles also enable the data output buffer U1 to supply bus data to U3, U4, U6 and U7.

The ads PROMBLASTER II contains EPROM configuration logic that is software controlled to provide the necessary high voltage and current signals on the type-specific pins of the programming socket U8. This logic operates in one of four modes determined by the state of bits 6 & 3 of the latch U6. Modes 0 and 2 are provided for Fast-Programming the newer larger parts, 8K and up.

Modes 0 and 2 are decoded by U10 and U17 and when activated by bit 0 of control latch U7 enables the elevated VCC to P28 on U8. The +6vdc VCC is generated by a shunt regulator formed by R35, C4 and Z1 which regulates the +8vdc from VR3 when enabled by R3, R4, Q2 and U13.

Mode 0 is decoded by U17 and U18 when u6's outputs are enabled by U7 bit 7 being set and is used to lower the output voltage of the DC to DC converter U26 via R11, R13, R19, Q5 and U14 by switching another resistor R11 in parallel with the voltage sensing resistor R70. This causes the high voltage to ramp down to +13.5v in about a half-second for the newest high density EPROMs.

Modes 1 and 2 are decoded by U14, U15, and U19 when U6's outputs are enabled by U7 bit 7 being set and is used to lower the output voltage of the DC to DC converter U26 via R74, R75, R76, Q8 and U14 by switching another resistor R76 in parallel

with the voltage sensing resistor R70. This causes the high voltage to ramp down to +22v in about a half-second.

Mode 3 is not explicitly decoded but is the default mode of operation. High voltage pulses can be provided on pins 1, 23, and 22 of the device programming socket U8 to supply VPP for different EPROMs. TTL logic levels can be provided on pins 2, 26, 27, 23, 22, 21 and 20 to be used as additional address lines or chip selects for different EPROMs. The high voltage levels applied to a pin disable the TTL logic '0' level drivers.

A timer is provided on card to allow software to control the pulse widths of the applied voltage levels. The 2 MHZ utility CLOCK signal on the I.E.E.E. 696 bus is divided by 2 via U22 to 1 MHZ for reliable +5v CMOS operation and then counted by a 14 stage counter U20. The eleventh stage output goes high after 1024 counts (one millisecond) and then goes low after 1024 counts then repeats. This signal is available as an interrupt via U14 and U19 or as an input that may be polled via U18, U19 and U25. The timer (counter) is reset by a I/O read operation via U9, U13, U18, U21, R68 and C16. The time constant supplied by R68 and C16 insures an minimum RST pulse width for reliable +5v CMOS operation.

A limited self-test capability is obtained by 'OR'ing the voltages present on programming socket U8 pins P1, P22 and P23 via CR5, CR1 and CR12 respectively. This voltage is applied to a Zener ladder with taps at specific voltages. Devices R21>R23, R26>R27, R29>R31, C38 and Q11>Q14 encode the detected voltage into a two bit code that is pollable by reading I/O address+2 bits 5 and 6. In addition an elevated VCC detection capability is provided by R14, R24 R28, Z5 and Q15. This detector is pollable by reading I/O address+2 bit 4.

The output of the test circuitry is monitored by R25, R33>R34, Q6, U19 and LED to provide a visual feedback of any high-voltage present on the programming socket U8. This LED drive is also available on the Prom Extender connector which contains all of the signals present on U8 and some additional voltages.

VII. Appendix - a software example

The following is a 8080 code example for the ads PROMBLASTER II. It allows programming, verifying, and reading of INTEL 2716 EPROMS. After assembly and loading, it is invoked via DDT. After execution at the various entry points in the function table, control is returned to DDT with a RST 07 instruction. The result of the function is returned in the Z flag. A non-zero Z flag indicates successful completion of the function jumped to. Note that the PROMBLASTER II I/O routines maintain a RAM copy of the I/O port's status to allow setting and resetting of individual bits. This code segment is presented as an example of PROMBLASTER II control software. Full feature PROMBLASTER II control is available with the ads PROMWRITER software.

```
                ; ADS PROMBLASTER INTEL 2716 EXAMPLE
                ;
  C0 =          PRMBAS  EQU     0C0H    ;PROMBLASTER BASE PORT #
                ;
0100                    ORG     0100H
                ;
0100 CD6701             CALL    CONFIG  ;CONFIGURE PROMBLASTER FOR I2716
0103 FF                 RST     7       ;CALL DDT
0104 CDDA01             CALL    CHECK   ;CHECK I2716 FOR UNBURNED STATE
0107 FF                 RST     7       ;CALL DDT
0108 CD6A01             CALL    PROGRM  ;PROGRAM I2716 FROM -> TO
010B FF                 RST     7       ;CALL DDT
010C CD8F01             CALL    VERIFY  ;VERIFY I2716 FROM -> TO
010F FF                 RST     7       ;CALL DDT
0110 CDB501             CALL    READ    ;READ I2716 FROM -> TO
0113 FF                 RST     7       ;CALL DDT
0114 C30000             JMP     0       ;CALL CP/M
                ;
                ; RAM DEFINITIONS
                ;
0117 0000       FROM:   DW      0       ;FROM LOCATION
0119 0000       TO:     DW      0       ;TO LOCATION
011B 0000       POFF:   DW      0       ;PROM OFFSET
011D 00         PRDT:   DB      0       ;PROMBLASTER DATA PORT SAVE
011E 00         ADLO:   DB      0       ;PROMBLASTER ADDR LOW SAVE
011F 00         ADHI:   DB      0       ;PROMBLASTER ADDR HI SAVE
0120 00         VCTL:   DB      0       ;PROMBLASTER VOLTAGE CONTROL SAVE
                ;
                ; PROMBLASTER I/O ROUTINES
                ;
0121 DBC0       PRDTIN: IN      PRMBAS
0123 C9                 RET
                ;
0124 D3C0       PRDTOT: OUT     PRMBAS
0126 C9                 RET
                ;
0127 321E01     ADLOOT: STA     ADLO
012A D3C1               OUT     PRMBAS+1
012C C9                 RET
                ;
012D 47         ORADHI: MOV     B,A
012E 3A1F01             LDA     ADHI
0131 B0                 ORA     B
0132 321F01     ADHIOT: STA     ADHI
0135 D3C2               OUT     PRMBAS+2
0137 C9                 RET
                ;
0138 47         ANADHI: MOV     B,A
0139 3A1F01             LDA     ADHI
013C A0                 ANA     B
013D C33201             JMP     ADHIOT
                ;
0140 DBC1       RSVCTL: IN      PRMBAS+1
0142 C9                 RET
                ;
```

```
0143 47        ORVCTL: MOV     B,A
0144 3A2001            LDA     VCTL
0147 B0                ORA     B
0148 322001    VCTLOT: STA     VCTL
014B D3C3              OUT     PRMBAS+3
014D C9                RET
               ;
014E 47        ANVCTL: MOV     B,A
014F 3A2001            LDA     VCTL
0152 A0                ANA     B
0153 C34801            JMP     VCTLOT
               ;
0156 CD6001    WAITIM: CALL    RSTTIM
0159 CD6301    WAITLP: CALL    CHKTIM
015C D25901            JNC     WAITLP
015F C9                RET
               ;
0160 DBC3      RSTTIM: IN      PRMBAS+3
0162 C9                RET
               ;
0163 DBC2      CHKTIM: IN      PRMBAS+2
0165 17                RAL
0166 C9                RET
               ;
               ; CONFIGURE THE PROGRAMMING SOCKET - U8
               ;
0167 =         CONFIG  EQU     $
0167 C30002            JMP     I2716C  ;INTEL 2716
               ;
               ; PROGRAM I2716 FOR FROM -> TO LOCATIONS
               ;
016A =         PROGRM  EQU     $
016A 210010            LXI     H,1000H ;FROM=1000H
016D 221701            SHLD    FROM    ;*
0170 21FF17            LXI     H,17FFH ;TO=FROM+2048
0173 221901            SHLD    TO      ;*
0176 =         PROGLP  EQU     $
0176 CD2802            CALL    I2716P  ;PROGRAM @ FROM
0179 2A1901            LHLD    TO      ;Q-FROM = TO?
017C EB                XCHG            ;*
017D 2A1701            LHLD    FROM    ;*
0180 7C                MOV     A,H     ;*
0181 BA                CMP     D       ;*
0182 C28801            JNZ     NXTP    ;*
0185 7D                MOV     A,L     ;*
0186 BB                CMP     E       ;*
0187 C8                RZ              ;RETURN IF FROM = TO
0188 =         NXTP    EQU     $
0188 23                INX     H       ;FROM = FROM +1
0189 221701            SHLD    FROM    ;*
018C C37601            JMP     PROGLP  ;CONTINUE PROGRAMMING
               ;
               ; VERIFY I2716 FOR FROM -> TO LOCATIONS
               ;
018F =         VERIFY  EQU     $
```

```
018F 210010             LXI     H,1000H         ;SETUP FROM
0192 221701             SHLD    FROM            ;*
  95 21FF17             LXI     H,17FFH         ;SETUP TO = FROM + 2048
v198 221901             SHLD    TO              ;*
019B =          VERILP  EQU     $
019B CD8002             CALL    I2716V          ;VERIFY I2716 @ FROM
019E C0                 RNZ                     ;ERROR @ FROM
019F 2A1901             LHLD    TO              ;ADVANCE FROM, FROM=TO?
01A2 EB                 XCHG                    ;*
01A3 2A1701             LHLD    FROM            ;*
01A6 7C                 MOV     A,H             ;*
01A7 BA                 CMP     D               ;*
01A8 C2AE01             JNZ     NXTV            ;*
01AB 7D                 MOV     A,L             ;*
01AC BB                 CMP     E               ;*
01AD C8                 RZ                      ;RETURN IF DONE
01AE =          NXTV    EQU     $
01AE 23                 INX     H               ;FROM = FROM +1
01AF 221701             SHLD    FROM            ;*
01B2 C39B01             JMP     VERILP          ;CONTINUE VERIFYING
                ;
                ; READ I2716 FOR FROM -> TO LOCATIONS
                ;
01B5 =          READ    EQU     $
01B5 210010             LXI     H,1000H         ;SETUP FROM
01B8 221701             SHLD    FROM            ;*
01BB 21FF17             LXI     H,17FFH         ;SETUP TO = FROM +2048
01BE 221901             SHLD    TO              ;*
  C1 =          READLP  EQU     $
01C1 CD8902             CALL    I2716R          ;READ I2716 @ FROM
01C4 2A1901             LHLD    TO              ;ADVANCE FROM, FROM=TO?
01C7 EB                 XCHG                    ;*
01C8 2A1701             LHLD    FROM            ;*
01CB 7C                 MOV     A,H             ;*
01CC BA                 CMP     D               ;*
01CD C2D301             JNZ     NXTR            ;*
01D0 7D                 MOV     A,L             ;*
01D1 BB                 CMP     E               ;*
01D2 C8                 RZ                      ;RETURN IF DONE
01D3 =          NXTR    EQU     $
01D3 23                 INX     H               ;FROM=FROM + 1
01D4 221701             SHLD    FROM            ;*
01D7 C3C101             JMP     READLP          ;CONTINUE READING
                ;
                ; CHECK I2716 FOR FROM -> TO UNBURNED LOCATIONS
                ;
01DA =          CHECK   EQU     $
01DA 210010             LXI     H,1000H         ;SETUP FROM
01DD 221701             SHLD    FROM            ;*
01E0 21FF17             LXI     H,17FFH         ;SETUP TO
01E3 221901             SHLD    TO              ;*
01E6 =          CHEKLP  EQU     $
01E6 CD9102             CALL    I2716U          ;CHECK I2716 @ FROM FOR UNBURN
 1E9 C0                 RNZ                     ;RETURN IF NOT
 1EA 2A1901             LHLD    TO              ;ADVANCE FROM, FROM = TO?
```

```
01ED EB                 XCHG                            ;*
01EE 2A1701             LHLD    FROM                    ;*
01F1 7C                 MOV     A,H                     ;*
01F2 BA                 CMP     D                       ;*
01F3 C2F901             JNZ     NXTC                    ;*
01F6 7D                 MOV     A,L                     ;*
01F7 BB                 CMP     E                       ;*
01F8 C8                 RZ                              ;RETURN IF DONE
01F9 =          NXTC    EQU     $
01F9 23                 INX     H                       ;FROM =FROM +1
01FA 221701             SHLD    FROM                    ;*
01FD C3E601             JMP     CHEKLP                  ;CONTINUE CHECKING
                ;
                ; SINGLE SUPPLY 2K PARTS
                ;
                ;       INT2716,MCM2716,TMS2516
                ;---------------------------------------
                ;
                ; CONFIGURE PROMBLASTER U8 SOCKET FOR I2716
                ;
0200 =          I2716C  EQU     $
0200        3E60        MVI     A,01100010B             ;VPP=5V,G=5V,VCC=5v
0202 CD4801             CALL    VCTLOT                  ;*
0205 3EC8               MVI     A,11001000B             ;DISBL DATA, MODE 3
0207 CD3201             CALL    ADHIOT                  ;*
020A AF                 XRA     A                       ;ADDR LO=0, DATA = 0
020B CD2701             CALL    ADLOOT                  ;*
020E CD2401             CALL    PRDTOT                  ;*
0211 C9                 RET
                ;
                ; SETUP A0-A10 SUBROUTINE
                ;
0212 =          I2716S  EQU     $
0212 3A1701             LDA     FROM                    ;ADDRESS SETUP
0215 CD2701             CALL    ADLOOT                  ;*A0-A7
0218 3A1F01             LDA     ADHI                    ;*A8-A10
021B E6F8               ANI     11111000B               ;**
021D 47                 MOV     B,A                     ;**
021E 3A1801             LDA     FROM+1                  ;**
0221 E607               ANI     00000111B               ;**
0223 B0                 ORA     B                       ;**
0224 CD3201             CALL    ADHIOT                  ;**
0227 C9                 RET
                ;
                ; PROGRAM I2716 @ FROM SUBROUTINE
                ;
0228 =          I2716P  EQU     $
0228 CD1202             CALL    I2716S                  ;ADDRESS SETUP
022B 3E80               MVI     A,10000000B             ;ADDR ENBL
022D CD4301             CALL    ORVCTL                  ;*
0230 3E08               MVI     A,00001000B             ;VPP=25V
0232 CD4301             CALL    ORVCTL                  ;*
0235 2A1701             LHLD    FROM                    ;SETUP DATA
0238 7E                 MOV     A,M                     ;*
0239 CD2401             CALL    PRDTOT                  ;*
```

```
023C 3E7F                MVI     A,01111111B     ;ENBL DATA
023E CD3801              CALL    ANADHI          ;*
0241 3E10                MVI     A,00010000B     ;PROGR=5V
0243 CD4301              CALL    ORVCTL          ;*
0246 0632                MVI     B,50            ;WAIT FOR 50 MSEC
0248 =              I2716L EQU   $               ;*
0248 CD5601              CALL    WAITIM          ;*
024B 05                  DCR     B               ;*
024C C24802              JNZ     I2716L          ;*
024F 3EEF                MVI     A,11101111B     ;PROGR=0V
0251 CD4E01              CALL    ANVCTL          ;*ROGR=0V
0254 3EF7                MVI     A,11110111B     ;VPP=5V
0256 CD4E01              CALL    ANVCTL          ;*
0259 3E80                MVI     A,10000000B     ;DISBL DATA
025B CD2D01              CALL    ORADHI          ;*
025E 3E7F                MVI     A,01111111B     ;DISBL ADDR
0260 CD4E01              CALL    ANVCTL          ;*
0263 C9                  RET
                    ;
                    ; READ I2716 @ FROM SUBROUTINE
                    ;
0264 =              I2716Q EQU   $
0264 CD1202              CALL    I2716S          ;ADDR SETUP
0267 3E80                MVI     A,10000000B     ;ENBL ADDR
0269 CD4301              CALL    ORVCTL          ;*
026C 3EDF                MVI     A,11011111B     ;G=0V
026E CD4E01              CALL    ANVCTL          ;*
0271 CD2101              CALL    PRDTIN          ;READ PROM
0274 4F                  MOV     C,A             ;SAVE
0275 3E20                MVI     A,00100000B     ;G=5V
0277 CD4301              CALL    ORVCTL          ;*
027A 3E7F                MVI     A,01111111B     ;DISBL ADDR
027C CD4E01              CALL    ANVCTL          ;*
027F C9                  RET
                    ;
                    ; VERIFY I2716 @ FROM SUBROUTINE
                    ;
0280 =              I2716V EQU   $
0280 CD6402              CALL    I2716Q          ;READ PROM
0283 2A1701              LHLD    FROM            ;PNT2 DATA
0286 7E                  MOV     A,M             ;GET DATA
0287 B9                  CMP     C               ;TEST AGAINST PROM
0288 C9                  RET
                    ;
                    ; READ I2716 @ FROM SUBROUTINE
                    ;
0289 =              I2716R EQU   $
0289 CD6402              CALL    I2716Q          ;READ PROM
028C 2A1701              LHLD    FROM            ;PNT2 TARGET ADDR
028F 71                  MOV     M,C             ;SAVE DATA READ
0290 C9                  RET
                    ;
                    ; CHECK I2716 @ FROM FOR UNBURNED SUBROUTINE
                    ;
0291 =              I2716U EQU   $
```

```
0291 CD6402             CALL    I2716Q          ;READ PROM
0294 3EFF               MVI     A,11111111B
0296 B9                 CMP     C               ;TEST PROM FOR UNBURNED
0297 C9                 RET
                ;
0298                    END
```

47K OHM PULL UP RESISTORS ON ALL Q INPUTS OF U11 & U12. SIP PACKAGES

SEE JU1 MANUAL

EXTENDED DEVICE OPT. SWITCH #

DEVICE ADDR. SWITCH #

AN OPEN SWITCH IS A LOGIC "1"

EXTENDED DEVICE OPTION

CLOCK OPTION

QUALIFIER OPTION

WAIT STATES

PROGRAMMING SOCKET PIN NUMBERS

40 PIN HEADER

ADS	PROMBLASTER II
ACKERMAN DIGITAL SYSTEMS, INC.	
(312) 530-8992	
DATE 3-7-84	REV B.	IEEE 696

ALL RESISTORS 1/4 W. UNLESS MARKED