```
ZZZZZ   OOOOO   BBBB    EEEEE   X   X
    Z   O   O   B   B   E       X   X
   Z    O   O   B   B   E        X X
  Z     O   O   BBBB    EEE       X
 Z      O   O   B   B   E        X X
Z       O   O   B   B   E       X   X
ZZZZZ   OOOOO   BBBB    EEEEE   X   X
```

```
ZZZZZ   M   M    SSS              1      000      000
    Z   MM MM   S   S            11     0   0    0   0
   Z    M M M    S                1     0   0    0   0
  Z     M M M     S               1     0   0    0   0
 Z      M   M      S              1     0   0    0   0
Z       M   M   S   S            1     0   0    0   0
ZZZZZ   M   M    SSS            111     000      000
```

```
 666        4          K   K
6   6      44          K  K
6         4 4          K K
6 66     44444         KK
66  6      4           K K
6   6      4           K  K
 666       4           K   K
```

```
M   M    EEEEE   M   M   OOOOO   RRRR    Y   Y
MM MM    E       MM MM   O   O   R   R    Y Y
M M M    E       M M M   O   O   R   R    Y Y
M M M    EEE     M M M   O   O   RRRR      Y
M   M    E       M   M   O   O   R R       Y
M   M    E       M   M   O   O   R  R      Y
M   M    EEEEE   M   M   OOOOO   R   R     Y
```

ZOBEX
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## WARRANTY

ZOBEX warrants its ZMS 1Ø0 64K memory boards to be free from defects in materials and workmanship for a period of six months from purchase date. ZOBEX will, at its option, repair or replace the defective part or parts to restore the board to proper operating condition. All such repairs and replacements will be made without charge for parts or labor when the board is returned (postage paid) to ZOBEX.

This warranty does not cover boards which have failed, in the judgement of ZOBEX, as a result of alteration, accident, abuse, negligence, improper supply voltages, or misapplication.

This warranty is in lieu of all other warranties, expressed or implied, including warranties of merchantability or fitness for use. In no event will ZOBEX be liable for incidental or consequential damages arising from or in any way connected with the use of this product.

## CHARACTERISTICS and FEATURES

The ZOBEX ZMS 100 64K ram board is a low-cost, high-speed memory for all S-100 computers. It fully meets the new IEEE standard for S-100 devices, and also operates with all pre-standard S-100 computers. Compare our features and pricing with the competition.

FEATURES

Meets new IEEE standard for S-100 slaves

Universally usable with any S-100 8-bit system.

4 MHz operation with NO wait states required.

Totally invisible refreshing.

Full, unlimited DMA operation, in bytes or bursts
- really works with DMA disk controllers -

Low power requirements - less than 8 Watts

Fully compatible with Cromemco, North Star, Delta, Alpha Micro, etc.

De-selectable via Phantom line (bus pin 67)

Software controlled memory mapping for each 16K section

Bank selection via I/O port or IEEE extended address bits

Bank select port switchable to any of 256 I/O ports.

Six months parts and labor warranty.

Our versatile memory mapping feature permits you to select the bank and address for each 16K section of each board. Any section can be addressed in any or all of the 8 banks, giving a total memory space of over 512,000 bytes. This is done through an output port which you can switch-select to be any of the 256 ports in your computer. And you can use the IEEE extended address bits too.

## BOARD SETUP

As delivered, the board is setup to be a conventional 64K memory with bank selection disabled. It is set for 4 MHz operation and IEEE timing. The following configuration changes should be ignored unless you have other requirements.

1. SPEED: Cut the 4M trace located between IC 38 pin 6 and IC 30 pin 10 if you want to operate at a 2 MHz clock rate.

2. 8080 TIMING: Cut the trace between pads M and F, and connect pads D and M if you have an 8080 CPU, or other non-standard timing.

3. I/O PORT: If you intend to use the bank select features, set the dip-switch at IC 31 to the port desired. The top switch is bit 0, and the bottom switch is bit 7. ON means "one", and OFF means "zero". Port 40 (hex) is commonly used. Typically all boards in a system are set to the same port. As delivered, these switches have no effect, since IC 35 is jumpered to ignore them.

4. BANK SWITCHING: There is so much capability in this area with the ZMS 100 that it is difficult to fully explain. Basically every 16K section of memory in your system (up to 32 of them) can be set up to be in any of 8 banks at any address. For a section to be accessed, two things must be true: 1) It must be a part of the currently selected bank, and 2) It must be configured to respond to the 16 bit address curently on the address bus.

The 8 bits of the output port are typically used to individually select one of 8 banks of 64K bytes. Each bit corresponds to a bank, for example sending bit 0 (01 hex) to the port selects bank 0, and sending bit 5 (20 hex) selects bank 5. No more than one bit should normally be sent at one time.

Each of the 16K sections (A,B,C,D) of each memory board may be made a part of any or all of the eight banks, and furthermore may be located at any address which is a multiple of 16K. Each section may also be automatically de-selected by power-up or system reset.

The headers at IC 8 and IC 35 control all of these options. As delivered, the board is setup for "plain vanilla", and all 8 jumpers are connected straight across IC 8, thus enabling all 4 sections on system reset, and addressing Section A = 0000-3FFF, Section B = 4000-7FFF, Section C = 8000-BFFF, and Section D = C000-FFFF.

The header at IC 35 has pins 1-2-3, and 12-13-14 connected. This disables the bank selection from the output port, and activates all 4 sections of the board.

An easy way to configure these two headers is to use a memory mapping chart (found in the appendix). First decide how you want the memory allocated for your application, then write an X in the appropriate blocks in Tables 1 and 2. Be sure to use a separate form for each board in the system - they will not be identical.

Now connect the jumpers from the points given as rows and columns for each X, and the job is done.

## EXAMPLE

Suppose you have two ZMS 100 memory boards you wish to use in a two-bank scheme. Both are addressed at port 40 (hex).

Further, you wish the upper 16K section of memory in each board to be at C000-FFFF in both bank 0 and bank 1. Thus the operating system to be placed in this 16K area "stays put" when you switch banks. The lower three sections of memory are to be distinct.

Let us select section D to be the common section to appear at C000-FFFF.

Table 1 for board 0 will have Xs in all four blocks under the Bank 0 column, and one X in section D under Bank 1. Table 1 for board 1 will have Xs only in sections A-B-C under Bank 1.

Table 2 for board 0 will have one X in each column opposite the desired address, in this case section A = 0000-3FFF, section B = 4000-7FFF, section C = 8000-BFFF, and section D = C000-FFFF. Table 2 for board 1 will be the same except there will not be an X under section D because this memory is to be on board 0 only.

By reading from the tables, the jumpers required for board 0 are:
IC 35 pins 11-12-3-2-7 (in a chain)
IC 8 pins 1-16, 2-15, 3-14, and 4-13.

For board 1 they are:
IC 35 pins 7-13-12-3 (chain)
IC 8 pins 2-15, 3-14, and 4-13.

For board 1 the lower 4 jumpers on header IC 8 may be removed so this board will be disabled on power-up or reset until the software enables it.

Another more complex example is given in the appendices to show some of the additional flexibility of the ZMS 100.

ZOBEX ZMS 100
MEMORY MAPPING CHART

Board #_____, Located in chassis slot #_____

TABLE 1 - IC 35

| | Bank 0 pin 11 | Bank 1 pin 7 | Bank 2 pin 6 | Bank 3 pin 5 | Bank 4 pin 4 | Bank 5 pin 8 | Bank 6 pin 9 | Bank 7 pin 10 |
|---|---|---|---|---|---|---|---|---|
| A pin 13 | | | | | | | | |
| B pin 12 | | | | | | | | |
| C pin 3 | | | | | | | | |
| D pin 2 | | | | | | | | |

TABLE 2 - IC 8 (top half)

| | A pin 13 | B pin 14 | C pin 15 | D pin 16 |
|---|---|---|---|---|
| 0000 - 3FFF pin 4 | | | | |
| 4000 - 7FFF pin 3 | | | | |
| 8000 - BFFF pin 2 | | | | |
| C000 - FFFF pin 1 | | | | |

TABLE 3 - IC 8 (bottom half)

| Section | Jumper |
|---|---|
| A | pins 5 to 12 |
| B | pins 6 to 11 |
| C | pins 7 to 10 |
| D | pins 8 to 9 |

For disabling sections by power-on or reset.

ZOBEX ZMS 100
MEMORY MAPPING CHART

Board #_____, Located in chassis slot #_____

TABLE 1 - IC 35

| | Bank 0 pin 11 | Bank 1 pin 7 | Bank 2 pin 6 | Bank 3 pin 5 | Bank 4 pin 4 | Bank 5 pin 8 | Bank 6 pin 9 | Bank 7 pin 10 |
|---|---|---|---|---|---|---|---|---|
| A pin 13 | | | | | | | | |
| B pin 12 | | | | | | | | |
| C pin 3 | | | | | | | | |
| D pin 2 | | | | | | | | |

TABLE 2 - IC 8 (top half)

| | A pin 13 | B pin 14 | C pin 15 | D pin 16 |
|---|---|---|---|---|
| 0000 - 3FFF pin 4 | | | | |
| 4000 - 7FFF pin 3 | | | | |
| 8000 - BFFF pin 2 | | | | |
| C000 - FFFF pin 1 | | | | |

TABLE 3 - IC 8 (bottom half)

| Section | Jumper |
|---|---|
| A | pins 5 to 12 |
| B | pins 6 to 11 |
| C | pins 7 to 10 |
| D | pins 8 to 9 |

For disabling sections by power-on or reset.

Theory of Operation

BUS SIGNALS:

The ZOBEX ZMS 100 64K memory board uses the following IEEE S-100 bus signals:

| | |
|---|---|
| A0 - A18 | High-true address lines |
| pWR* (77 | Low-true write signal, indicates bus has output data |
| sOUT (45) | High-true, indicates that the current cycle is an output cycle, and that the address bus has the address of an output device. |
| sINP (46) | High-true, indicates that the current cycle is an input cycle, and that the address bus has the address of an input device. |
| pSYNC (76) | High-true, indicates the beginning of a bus cycle. |
| pDBIN (78) | High-true, indicates the data bus is expecting data from the currently addressed slave. |
| POC* (99) | Low-true. Asserted from the CPU to indicate a master reset condition. |
| sM1 (44) | High-true, indicates that the present bus cycle is for instruction read-up (followed by refresh). |
| pSYNC (76) | High-true, indicates the start of a bus cycle. |
| sMEMR (47) | High-true, indicates that the data bus will be used for memory read. |
| RDY (72) | High-true, lets processor run as long as this line is high. |
| pHLDA (26) | High-true, indicates that the data and address buses are in the high-impedance state. Appears in response to a HOLD signal (perhaps from a DMA device). |
| RESET* (75) | Low-true, indicates a total system reset has been commanded, usually from a front-panel switch closure to ground. |
| PHANTOM* | Low-true, indicates that the memory board is to ignore all requests. Usually generated by CPU or ROM boards to allow dual-use addressing for ROM and RAM |
| D0 - D7 | High-true data in/out bus |

## CIRCUIT DETAILS

BANK SELECT:

Refer to page 2 of the logic prints. IC 24 and 25 are comparators which constantly watch for the address bits on the bus to match the switch settings. A high is output from IC 4 pin 12 when the selected port is being sent data.

Refer to page 1. For a 16 K memory section to be accessed, two things must be true: (1) It must be a part of the currently selected bank, and (2) The 16 bits currently on the address bus must contain an address within the limits of the section.

The flip flops at IC 17 and 18 control the BANK selection of each of the four 16K memory sections. These flip flops are set by POC* unless the jumpers across the lower half of IC 8 have been removed. The clock inputs are driven by the PORTX OUT signal when a byte is being sent to the port, and this clocks the inverted data bits from the header at IC 35 into the section flip flops. Thus a one on a given data bit will set the Q output low to enable a section. Which data bit controls which flip flop is a function of how the header at IC 35 is wired.

The AND gate at IC 9 is the final determiner of whether a section will be accessed. The addressing is determined by the jumpers across IC 8 (just to the right of the address decoder at IC 7). The MSEL signal is derived as the OR of all four section enables.

TIMING:

Refer again to page 2. The 18 MHz oscillator at IC 28 feeds IC 29, which is a shift register. This forms a kind of digital delay line, with taps every 55 nanoseconds. Including internal delays, the taps are 0, 55, 111, 166, 222, 277, 333, and 388 nanoseconds. A memory cycle is started by the OR gate at IC 30 when any one of its inputs goes low. Thus a cycle can be started for reading by sMEMR AND pDBIN on pin 9, for writing by pin 13, M1 on pin 12, or PSYNC on pin 10.

The start flip flop at IC 37 then sets, and feeds a high through IC 22 (unless refreshing) to set the CYCLE ON latch at IC 21. This enables the digital delay line, and the RAS signals will be applied at this time to all selected rams. The CAS/RAS multiplexer signal MUX* is supplied by IC 15 pin 3, and will initially be high.

About 40 ns later, the low applied initially to delay line IC 14 pin 1 will arrive at IC 15 pin 2 and will switch the MUX output low, thus enabling the CAS timing. Similarly, the CASX signal will go low at about 80 ns.

The CYCLE ON flip flop will be reset at 222 ns from pin 10 of the shift register, and the cycle will completely terminate by resetting IC 37 at 333 ns from pin 12 of the shift register. There is some jitter in all this timing due to the delay from the beginning of the start pulse and the time of the next pulse from the 18 MHz

oscillator, so the actual time of CYCLE ON can be from 222 to 277 ns.

RAM REFRESH:

Memory refreshing occurs after an M1 cycle when pin 6 of IC 37 goes low (indicating pre-charge time has elapsed). This sets the refresh flip flop at IC 1 pin 5, which starts another digital delay line running at IC 13, controlling the refresh timing. Refresh can also be initiated by the timeout one shot at IC 11, or by the bus master being in a hold or stopped condition, indicated by a high from IC 2 pin 8.

DATA PATHS:

Refer to page 1. The 16 address lines from the S-100 buss are applied to the tri-state latch at IC 33 and 34, and are latched by the leading edge of the CYCLE ON pulse. The ram address multiplexer at IC 26 is controlled by the MUX* and RFSH signals from page 2. Thus either the CAS or RAS addresses are applied to all the ram chips at the appropriate times through the current-limiting resistors.

Data to be written to the rams comes from the data out bus via IC 40, which is always enabled.

Data from the rams to the bus goes through tri-state latch IC 41, which is enabled by the CYCLE ON and EOB* (Enable Output Buffer) signals. EOB* is generated from the pDBIN and MSEL signals at IC 30.

## TROUBLE SHOOTING TIPS

The ZOBEX memory board is supplied only in wired and tested form, and is fully warranted for six months. If you have problems after the warranty period has expired and wish to fix them yourself, the following thoughts should be borne in mind.

You have a substantial investment in expensive chips, so be CAUTIOUS and never remove or install a board in the bus until power has been off for at least ten seconds to let the large filter capacitors discharge.

Remove the memory board.

See that all the solder joints are clean, shiny, and smooth. Dull solder joints are cold solder joints and could cause problems. They should be resoldered. Make sure the solder does not overlap onto adjacent etches or pads.

Inspect the board for evidence of damage. Remove all other cards from the bus. Apply power and check for normal voltages at the regulator outputs. If normal voltages are NOT observed, remove all chips from the board, plug it into the bus and apply power, watching carefully for smoke, smell, or heat. Then check for the proper voltages at the voltage regulator outputs (right-hand leads).

If all is well, replace the chips section by section until you find the one which is shorted. Replace the defective chip(s), re-install the other boards and try again. If you have trouble beyond this point, the usual memory trouble-shooting techniques apply to this board as well as any other.

Memory test programs will be helpful, as will a wide-band oscilloscope. A very effective Z-80 memory test is available from ZS Systems for a nominal charge.

ZOBEX ZMS 100
MEMORY MAPPING CHART

Board #_____, Located in chassis slot #_____

TABLE 1 - IC 35

| | Bank 0 pin 11 | Bank 1 pin 7 | Bank 2 pin 6 | Bank 3 pin 5 | Bank 4 pin 4 | Bank 5 pin 8 | Bank 6 pin 9 | Bank 7 pin 10 |
|---|---|---|---|---|---|---|---|---|
| A pin 13 | | | | | | | | |
| B pin 12 | | | | | | | | |
| C pin 3 | | | | | | | | |
| D pin 2 | | | | | | | | |

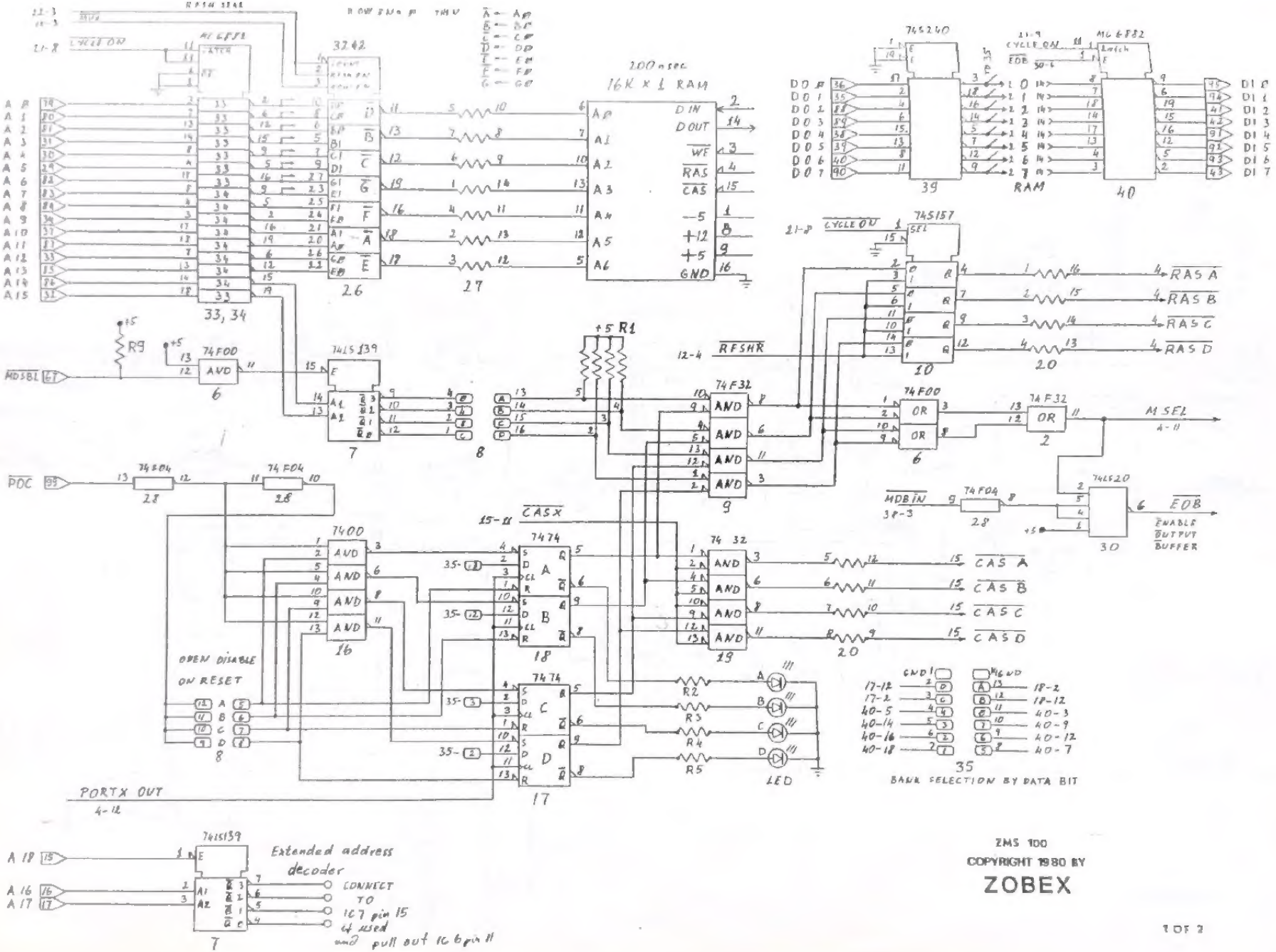
TABLE 2 - IC 8 (top half)

| | A pin 13 | B pin 14 | C pin 15 | D pin 16 |
|---|---|---|---|---|
| 0000 - 3FFF pin 4 | | | | |
| 4000 - 7FFF pin 3 | | | | |
| 8000 - BFFF pin 2 | | | | |
| C000 - FFFF pin 1 | | | | |

TABLE 3 - IC 8 (bottom half)

| Section | Jumper |
|---|---|
| A | pins 5 to 12 |
| B | pins 6 to 11 |
| C | pins 7 to 10 |
| D | pins 8 to 9 |

For disabling sections by power-on or reset.


200 n sec
16K x 1 RAM
74S240
MC6852
CYCLE OUT
EOB
RAM
39
40
74S157
SEL
RFSHR
RAS A
RAS B
RAS C
RAS D
74F00
74F32
MSEL
MDBIN
74S20
EOB
ENABLE OUTPUT BUFFER
POC
74S04
74F04
CASX
7400
7474
CAS A
CAS B
CAS C
CAS D
OPEN DISABLE ON RESET
PORTX OUT
R1
R2
R3
R4
R5
LED
35
BANK SELECTION BY DATA BIT
74S139
Extended address decoder
CONNECT TO IC7 pin 15 if used and pull out IC 6 pin 11
ZMS 100
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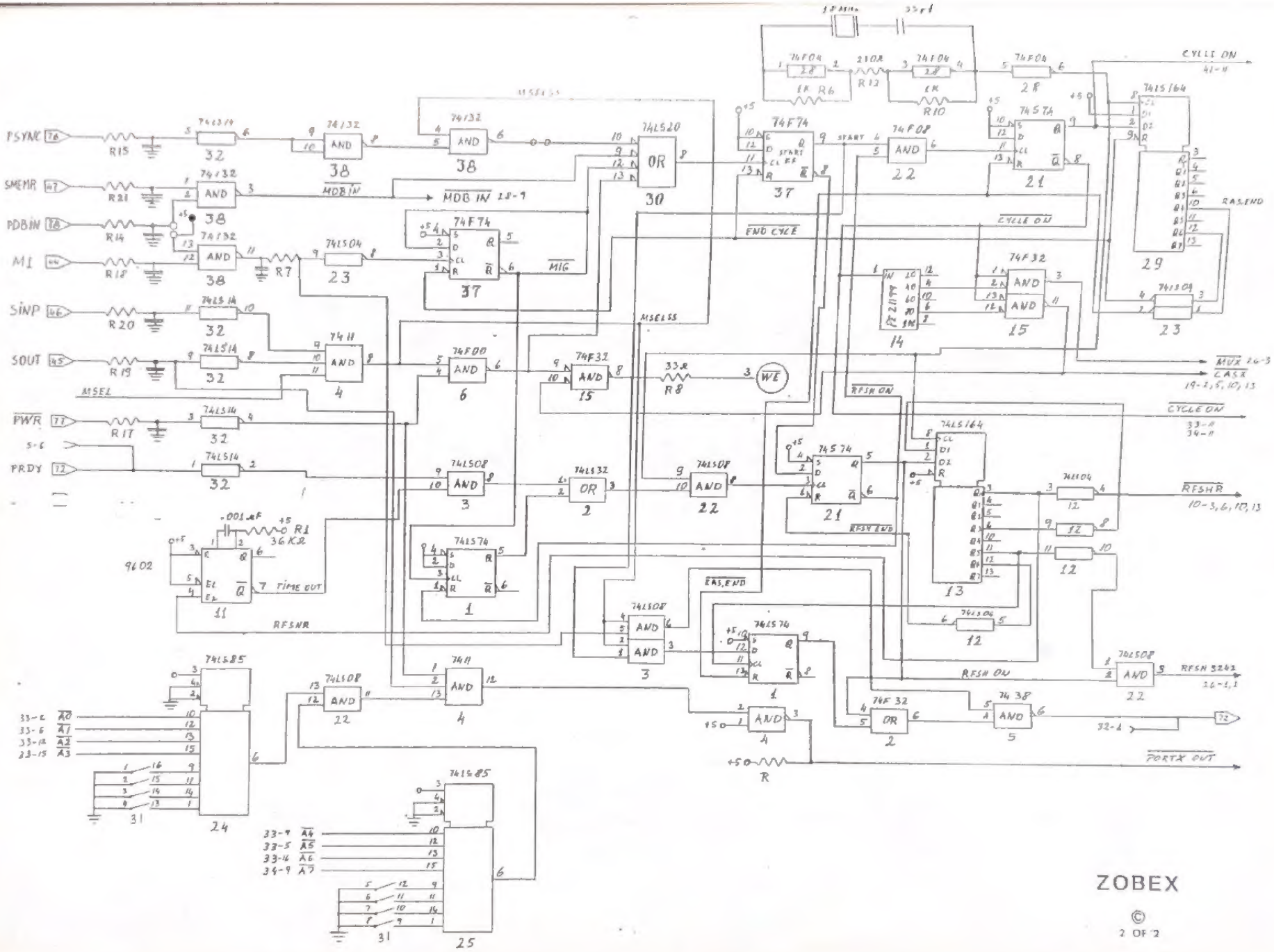
1 OF 2


PSYNC
SMEMR
PDBIN
M1
SINP
SOUT
PWR
PRDY
MSEL
MSELSS
MDB IN
MDB IN 15-7
MIG
END CYCLE
CYCLE ON
START
RFSH ON
RFSH END
EAS,END
RAS,END
RFSHR
TIME OUT
WE
PORTX OUT
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