CPU USERS MANUAL

VECTOR GRAPHIC INC.
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CPU BOARD

TABLE OF CONTENTS

INTRODUCTION

THE VECTOR GRAPHIC INC. CENTRAL PROCESSOR UNIT (CPU) PROVIDES ALL THE CENTRAL PROCESSING AND LOGIC FUNCTIONS FOR YOUR MICROCOMPUTER SYSTEM. THE HEART OF THIS BOARD IS THE 8080A LSI MICROPROCESSOR. COUPLED WITH THE 8080A LSI CHIP ARE VARIOUS PERIPHERAL CIRCUITS TO PERFORM TIMING, CONTROL, BUS INTERFACE, AND POWER SUPPLY REGULATION TO OBTAIN A RELIABLE AND VERSATILE CPU.

ESPECIALLY USEFUL FEATURES OF THE VECTOR GRAPHIC CPU ARE THE 8 LEVEL VECTORED PRIORITY INTERRUPT CIRCUITS AND A REAL TIME CLOCK. PROVISION OF A REAL TIME CLOCK ALLOWS FOR SOPHISTICATED TIMING AND CONTROL FUNCTIONS ONLY FOUND IN ADVANCED INDUSTRIAL MINICOMPUTERS. A PROGRAMMABLE PRIORITY INTERRUPT STRUCTURE ALLOWS THE USER TO ASSIGN DIFFERENT LEVELS OF PRIORITIES OR IMPORTANCE OF THE INTERRUPT INPUTS TO THE MICROCOMPUTER. ASSIGNMENT OF PRIORITY LEVEL IS FULLY PROGRAMMABLE ALLOWING FOR ADAPTIVE OPERATION UNDER PROGRAM CONTROL.

ALL INTERFACES BETWEEN THE CPU BOARD AND THE STANDARD S-100 BUS ARE FULLY BUFFERED FOR ISOLATION AND RELIABLE OPERATION.

A STABLE CLOCK FOR THE 8080A IS PROVIDED BY A CRYSTAL CONTROLLED OSCILLATOR AND CLOCK DRIVER. THIS INSURES OPERATION OF THE 8080A WITHIN THE MANUFACTURERS SPECIFICATIONS FOR TROUBLE FREE OPERATION.

CAREFUL ATTENTION TO GOOD DESIGN PRACTICE PROVIDES USER WITH A CPU GUARANTEED TO OPERATE RELIABLY WITHOUT CONSTANT ADJUSTMENT AND MAINTENANCE.

CPU BOARD PARTS LISTS

QTY.	DESCRIPTION
1	PRINTED CIRCUIT BOARD
1	8080A (A4)
2	8212 (B6, C7)
1	8214 (C1)
1	8224 (A5)
9	8097/74367 (A3, A8, B3, B4, B5, B7, C3, C4, C6)
1	74LS02 (A2)
3	74LS04 (A1, A6, C2)
1	74LS74 (B1)
1	74LS00 (B2)
1	74LS30 (C5)
1	340T-5/7805 REGULATOR
1	79L05 REGULATOR
1	78L12 REGULATOR
2	22 MFD 16V CAPACITORS
1	.001 MFD 1000V CERAMIC DISC CAPACITOR
10	0.1 MFD 50V MONOLITHIC RADICAL CAPACITORS
2	150 PF 1000V CERAMIC DISC CAPACITORS
1	10 PF 600V CERAMIC DISC CAPACITOR
2	4.0 MFD 50V AXIAL ELECTROLYTIC CAPACITORS
2	27 OHM 1 WATT RESISTORS (BANDS OF RED, VIOLET, BLACK)
35	1K 1/4 WATT RESISTORS (BANDS OF BROWN, BLACK, RED)

QTY.	DESCRIPTION
2	47K 1/4 WATT RESISTORS (BANDS OF YELLOW, VIOLET, ORANGE)
9	4.7K 1/4 WATT RESISTORS (BANDS OF YELLOW, VIOLET, RED)
1	15K 1/4 WATT RESISTOR (BANDS OF BROWN, GREEN, ORANGE)
1	100 OHM 1/4 WATT RESISTOR (BANDS OF BROWN, BLACK, BROWN)
1	18 MHZ CRYSTAL
1	1N270 DIODE
1	LM358 OP-AMP AR1
1	HEATSINK
1	40 PIN SOCKET
3	24 PIN SOCKETS
11	16 PIN SOCKETS
7	14 PIN SOCKETS
1	8 PIN SOCKET
2	EJECTORS

FUNCTIONAL DESCRIPTION

THE VECTOR GRAPHIC CPU BOARD IS DESIGNED AROUND THE INTEL 8080A MICROPROCESSOR CHIP. THIS BOARD IS S-100 BUS COMPATIBLE WITH ALL ALTAIR AND IMSAI PRODUCTS, PROVIDING INTERCHANGEABILITY BETWEEN VARIOUS SYSTEMS.

SIMPLICITY OF DESIGN HAS BEEN STRESSED TO ENHANCE RELIABILITY OF OPERATION BY THE USE OF LSI AND MSI INTEGRATED CIRCUITS. THIS GOAL HAS BEEN ACHIEVED WHILE NOT SACRIFICING ANY LOSS IN PERFORMANCE.

INPUT POWER TO THE BOARD IS PLUS AND MINUS 16V AND PLUS 8 VOLTS. TO ACHIEVE THE LEVELS OF +12V AND PLUS AND MINUS 5V, THREE VOLTAGE REGULATORS ARE USED.

AMPLE BYPASS AND FILTERING IS PROVIDED BY ELECTROLYTIC AND CERAMIC CAPACITORS DISTRIBUTED ON THE BOARD.

THE CENTRAL TIMING FUNCTION IS PROVIDED BY AN 8224 CLOCK GENERATOR IC, WITH AN 18 MHZ CRYSTAL USED AS THE PRIMARY FREQUENCY CONTROL ELEMENT FOR THE OSCILLATOR. THE OUTPUTS FROM THIS CHIP ARE ϕ1 AND ϕ2 FOR THE 8080A PLUS A ϕ2 SUITABLE FOR DRIVING TTL CIRCUITS. BUFFERED ϕ1 AND ϕ2 CLOCKS ARE AVAILABLE ON THE S-100 BUS ON PINS 25 (ϕ1) AND 24 (ϕ2).

PROCESSOR TIMING IS DIVIDED INTO TWO BASIC CYCLES. THEY ARE THE MACHINE CYCLE AND INSTRUCTION CYCLE. AN INSTRUCTION CYCLE IS DEFINED AS THE TIME REQUIRED TO FETCH AND EXECUTE AN INSTRUCTION. DURING THE FETCH CYCLE A SELECTED INSTRUCTION IS READ FROM MEMORY AND DEPOSITED IN THE CPU. DURING THE EXECUTION PHASE THE INSTRUCTION IS DECODED AND TRANSLATED INTO SPECIFIC PROCESSING ACTIVITIES. EVERY INSTRUCTION CYCLE CONSISTS OF FROM ONE TO FIVE MACHINE CYCLES. A MACHINE CYCLE IS NEEDED EACH TIME THE PROCESSOR ACCESSES MEMORY OR AN I/O PORT. EACH MACHINE CYCLE CONSISTS OF FROM THREE TO FIVE STATES. A STATE IS DEFINED AS THE INTERVAL BETWEEN TWO ϕ1 CLOCK PULSES.

THE 8224 PROVIDES THE RESET AND READY INPUTS TO THE 8080A. THESE SIGNALS ARE SYNCHRONIZED TO THE ϕ2 CLOCK PULSE AND ARE INITIATED FROM S-100 BUS INPUTS. A RESET MAY BE GENERATED BY THE PRESET (PIN 75) INPUT FROM THE S-100 BUS OR BY AN RC TIME CONSTANT ON THE BOARD WHEN THE SYSTEM IS INITALLY TURNED ON. THE RESET SIGNAL ALSO GENERATES THE POWER ON CLEAR POC (PIN 99) OUTPUT ON THE S-100 BUS.

THE READY OUTPUT FROM THE 8224 INDICATES TO THE 8080A THAT VALID DATA IS AVAILABLE ON THE INPUT DATA LINES. THIS SIGNAL IS GENERATED BY THE PRDY (PIN 72) OR XRDY (PIN 3) INPUTS FROM THE S-100 BUS. FOR EXAMPLE, THE VECTOR GRAPHIC PROM/RAM BOARD GENERATES THE PRDY SIGNAL WHEN DATA IS AVAILABLE FROM THAT BOARD FOR USE BY THE CPU.

DATA I/O LINES ON THE 8080A ARE D0 TO D7. THESE LINES ALLOW FUNCTIONAL DATA COMMUNICATION BETWEEN THE 8080A AND THE REST OF THE COMPUTER SYSTEM. INTERFACE BETWEEN THE 8080A DATA LINES AND THE S-100 BUS IS THROUGH 8097 TRI-STATE DRIVERS. THESE CIRCUITS ALLOW THE 8080A TO OUTPUT DATA TO THE D0 BUS OR INPUT DATA FROM THE DI BUS AT THE CORRECT TIMES. STATUS SIGNALS DESCRIBING THE CURRENT MACHINE CYCLE ARE PROVIDED ON THE 8080A DATA LINES DURING THE FIRST PART OF EACH MACHINE CYCLE. THIS INFORMATION IS STORED IN AN 8212 8 BIT STATUS LATCH WHICH IS GATED ON TO THE S-100 BUS BY 8097 DRIVERS AT THE CORRECT TIME. THE FUNCTION OF EACH STATUS SIGNAL ON THE S-100 BUS IS DEFINED BELOW.

1.	+8V	UNREGULATED INPUT TO +5V REGULATORS
2.	+16V	UNREGULATED INPUT TO +12V REGULATORS
3.	XRDY	ANDED WITH PRDY AND GOES TO 8080 RDY
4.	VIØ	VECTORED INTERRUPT REQUEST Ø
5.	VI1	VECTORED INTERRUPT REQUEST 1
6.	VI2	VECTORED INTERRUPT REQUEST 2
7.	VI3	VECTORED INTERRUPT REQUEST 3
8.	VI4	VECTORED INTERRUPT REQUEST 4
9.	VI5	VECTORED INTERRUPT REQUEST 5
10.	VI6	VECTORED INTERRUPT REQUEST 6
11.	VI7	VECTORED INTERRUPT REQUEST 7
12.	XRDY2	
13.		
14.		
15.		
16.		
17.		
18.	$\overline{\text{STA DSB}}$	STATUS BUFFER DISABLE
19.	$\overline{\text{C/C DSB}}$	COMMAND/CONTROL BUFFER DISABLE
20.	UNPROT	INPUT TO MEMORY PROTECT CIRCUITRY ON MEMORY BD.
21.	SS	INDICATES MACHINE IS IN SINGLE STEP MODE
22.	$\overline{\text{ADD DSB}}$	ADDRESS BUFFER DISABLE
23.	$\overline{\text{DO DSB}}$	DATA OUT (FROM CPU) BUFFER DISABLE
24.	Ø1	PHASE TWO CLOCK TTL LEVELS
25.	Ø2	PHASE ONE CLOCK TTL LEVELS

26.	PHLDA	HOLD ACKNOWLEDGE, BUFFERED 8080 OUTPUT
27.	PWAIT	WAIT ACKNOWLEDGE, BUFFERED 8080 OUTPUT
28.	PINTE	INTERRUPT ENABLE, BUFFERED 8080 OUTPUT
29.	A5	BUFFERED ADDRESS LINE 5 (32)
30.	A4	BUFFERED ADDRESS LINE 4 (16)
31.	A3	BUFFERED ADDRESS LINE 3 (8)
32.	A15	BUFFERED ADDRESS LINE 15 (32768)
33.	A12	BUFFERED ADDRESS LINE 12 (4096)
34.	A9	BUFFERED ADDRESS LINE 1 (2)
35.	DO1	BUFFERED DATA OUT LINE 1
36.	DOØ	BUFFERED DATA OUT LINE Ø
37.	A1Ø	BUFFERED ADDRESS LINE 1Ø (1024)
38.	DO4	BUFFERED DATA OUT LINE 4
39.	DO5	BUFFERED DATA OUT LINE 5
40.	DO6	BUFFERED DATA OUT LINE 6
41.	D12	DATA INPUT LINE 2
42.	D13	DATA INPUT LINE 3
43.	D17	DATA INPUT LINE 7
44.	SMI	LATCHED 8080 M1 STATUS
45.	SOUT	LATCHED 8080 OUT STATUS
46.	SINP	LATCHED 8080 INP STATUS
47.	SMEMR	LATCHED 8080 MEMR STATUS
48.	SHLTA	LATCHED 8080 HLTA STATUS
49.	CLOCK	2 MHZ CLOCK, CRYSTAL CONTROLLED

50. GND LOGIC AND POWER GROUND RETURN

51. +8V UNREGULATED INPUT TO +5V REGULATORS

52. -16V UNREGULATED INPUT TO NEGATIVE REGULATORS

53. $\overline{\text{SSW DSB}}$ SENSE SWITCH DISABLE

54. $\overline{\text{EXT CLR}}$ CLEAR SIGNAL FOR I/O DEVICES

55. CHASSIS GROUND

56. $\overline{\text{STSTB}}$ STROBE SIGNAL (BY 8224 CLOCK CHIP 8800B D/C BOARD)

57. DIGI ENABLE SIGNAL FOR CPU DI DRIVERS 8800B

58. FRDY 8800B FRONT PANEL READY SIGNAL

59.

60.

61.

62.

63.

64.

65.

66.

67. $\overline{\text{PHANTOM}}$

68. MWRT WRITE ENABLE SIGNAL FOR MEMORY

69. $\overline{\text{PS}}$ INDICATES IF ADDRESSED MEMORY IS PROTECTED

70. PROT INPUT TO MEMORY PROTECT CIRCUITRY ON MEMORY BD.

71. RUN INDICATES MACHINE IS IN RUN MODE

72. PRDY ANDED WITH XRDY AND GOES TO 8080 RDY

73. $\overline{\text{PINT}}$ INPUT TO 8080 INTERRUPT REQUEST

74. $\overline{\text{PHOLD}}$ INPUT TO 8080 HOLD REQUEST

75. $\overline{\text{PRESET}}$ CLEAR SIGNAL FOR CPU

76. PSYNC BUFFERED 8080 SYNC SIGNAL

77. $\overline{\text{PWR}}$ BUFFERED 8080 WRITE ENABLE SIGNAL

78. PDBIN BUFFERED 8080 BDIN SIGNAL

79. AØ BUFFERED ADDRESS LINE Ø (1)

80. A1 BUFFERED ADDRESS LINE 1 (2)

81. A2 BUFFERED ADDRESS LINE 2 (4)

82. A6 BUFFERED ADDRESS LINE 6 (64)

83. A7 BUFFERED ADDRESS LINE 7 (128)

84. A8 BUFFERED ADDRESS LINE 8 (256)

85. A13 BUFFERED ADDRESS LINE 13 (8192)

86. A14 BUFFERED ADDRESS LINE 14 (16384)

87. A11 BUFFERED ADDRESS LINE 11 (2048)

88. DO2 BUFFERED DATA OUT LINE 2

89. DO3 BUFFERED DATA OUT LINE 3

90. DO7 BUFFERED DATA OUT LINE 7

91. DI4 DATA INPUT LINE 4

92. DI5 DATA INPUT LINE 5

93. DI6 DATA INPUT LINE 6

94. DI1 DATA INPUT LINE 1

95. DIØ DATA INPUT LINE Ø

96. SINTA LATCHED 8080 INTA STATUS

97. $\overline{\text{SWO}}$ LATCHED 8080 WO STATUS

98. SSTACK LATCHED 8080 STACK STATUS

99. $\overline{\text{POC}}$ LO DURING POWER UP, RESET

100. GND LOGIC AND POWER GROUND RETURN

VECTOR GRAPHIC INC.

STATUS SIGNAL DEFINITIONS

SIGNAL	DEFINITION
SINTA (PIN 96)	ACKNOWLEDGE SIGNAL FOR AN INTERRUPT REQUEST
SWO (PIN 97)	INDICATES THAT THE CURRENT MACHINE CYCLE IS A MEMORY WRITE OR OUTPUT OPERATION
SSTACK (PIN 98)	INDICATES THAT THE ADDRESS BUS HOLDS THE PUSHDOWN STACK ADDRESS FROM THE STACK POINTER
SHLTA (PIN 48)	ACKNOWLEDGE SIGNAL FOR THE HALT INSTRUCTION
SOUT (PIN 45)	INDICATES THAT THE ADDRESS BUS CONTAINS THE ADDRESS OF AN OUTPUT DEVICE
SMI (PIN 44)	INDICATES THAT THE 8080A IS IN THE FETCH CYCLE FOR THE FIRST BYTE OF AN INSTRUCTION
SINP (PIN 46)	INDICATES THAT THE ADDRESS BUS CONTAINS THE ADDRESS OF AN INPUT DEVICE
SMEMR (PIN 47)	INDICATES THAT THE BUS WILL BE USED FOR A MEMORY READ OPERATION

A SOCKET CONNECTOR TO THE 8080A DATA LINES IS ALSO PROVIDED IN THE EVENT IT IS NEEDED TO INTERFACE A CONTROL PANEL TO THE CPU BOARD.

THERE ARE SIXTEEN ADDRESS LINES ON THE 8080A. THIS ALLOWS THE CPU TO ACCESS UP TO 65,536 (64K WHERE K=1024) MEMORY LOCATIONS. THESE ADDRESS LINES ARE CONNECTED TO THE S-100 BUS THROUGH 8097 DRIVERS AND GATED AT APPROPRIATE TIMES.

A POWERFUL PRIORITY VECTORED INTERRUPT STRUCTURE IS PROVIDED ON THE CPU BOARD. THIS IS ACCOMPLISHED USING AN 8214 PRIORITY INTERRUPT CONTROL IC AND AN 8212 LATCH TO GENERATE THE RST INSTRUCTION. THESE CIRCUITS ALLOW THE VECTOR GRAPHIC MICROCOMPUTER TO OPERATE AS A REAL TIME INTERRUPT DRIVEN COMPUTER SYSTEM. FOR A DETAILED DESCRIPTION OF THE THEORY OF INTERRUPTS REFER TO THE INTEL 8080A MICROCOMPUTER SYSTEMS MANUAL.

THERE ARE EIGHT INTERRUPT INPUTS TO THE COMPUTER, VI0 TO VI7, WHICH ARE CONNECTED TO THE 8214 IC. WHEN AN INTERRUPT IS SENSED BY THE 8214, A SYNCHRONIZED INTERRUPT SIGNAL IS SENT TO THE 8080A. THE NUMBER OF THE INTERRUPT IS ENCODED AND SENT TO THE 8212 FOR USE IN GENERATING THE ADDRESS FOR THE INTERRUPT HANDLING SOFTWARE UNIQUE TO THAT INTERRUPT. THE PRIORITY FUNCTON IS PROVIDED WHEN MORE THAN ONE INTERRUPT IS RECEIVED BY THE 8214 BY COMPARING THE NUMBERS OF THE INTERRUPTS WITH A PRIORITY LEVEL STORED IN THE DEVICE. THIS PRIORITY LEVEL IS DETERMINED BY THE USER AND MAY BE CHANGED UNDER SOFTWARE CONTROL. THE INTERRUPT OF HIGHEST PRIORITY IS THE ONE WHICH IS PROCESSED.

OTHER INTERRUPT REQUESTS MAY BE GENERATED AND ENTERED INTO THE CPU BOARD BY THE PINT (PIN 73) INPUT FROM THE S-100 BUS. THE 8080A MAY BE REQUESTED TO ENTER THE HOLD STATE BY THE PHOLD (PIN 74) INPUT FROM THE S-100 BUS. THE HOLD STATE

ALLOWS AN EXTERNAL DEVICE TO GAIN CONTROL OF THE ADDRESS AND DATA LINES. WHEN THE PHOLD SIGNAL IS REMOVED THE 8080A RESUMES NORMAL PROCESSING.

ANOTHER POWERFUL FEATURE OF THE VECTOR GRAPHIC CPU BOARD IS THE PROVISION OF A REAL TIME CLOCK. THIS FEATURE ALLOWS THE USER TO GENERATE A REAL TIME CLOCK OR EXECUTE TIME SEQUENCED OPERATIONS. A STABLE OP-AMP DIFFERENTIATOR SENSES THE 120 HZ RIPPLE ON THE +8V LINE TO GENERATE PRECISE 8.33 MSEC TIME INTERVALS. JUMPER CONNECTIONS ARE PROVIDED FROM THE CLOCK TO THE VECTORED INTERRUPT INPUTS. UNDER SOFTWARE CONTROL, THE USER CAN GENERATE 8.33 MSEC INTERRUPTS TO THE 8080A FOR TIMING OPERATIONS.

THERE ARE NUMEROUS ACKNOWLEDGE AND CONTROL SIGNALS FROM THE 8080A AVAILABLE ON THE S-100 BUS. THESE SIGNALS ARE USEFUL FOR DETERMINING MACHINE STATUS AND CONTROLLING PERIPHERAL OPERATIONS. THEY ARE DEFINED BELOW.

ACKNOWLEDGE AND CONTROL SIGNALS

SIGNAL	DEFINITION
PSYNC (PIN 76)	PROVIDES A SIGNAL TO INDICATE THE BEGINNING OF EACH MACHINE CYCLE
PWR (PIN 77)	USED FOR MEMORY WRITE OR I/O OPERATIONS. DATA IS STABLE WHEN PWR IS LOW
PDBIN (PIN 78)	INDICATES THAT THE 8080A DATA BUS IS IN THE INPUT MODE
PINTE (PIN 28)	INDICATES CONTENTS OF 8080A INTERRUPT ENABLE FLIP-FLOP
PHLDA (PIN 26)	INDICATES THAT THE 8080A IS IN THE HOLD STATE
PWAIT (PIN 27)	INDICATES THAT THE 8080A IS IN THE WAIT STATE

THERE ARE A NUMBER OF SIGNALS WHICH WILL DISABLE VARIOUS PORTIONS OF THE S-100 BUS. WHEN THESE SIGNALS ARE ACTIVE THEY EFFECTIVELY DISCONNECT THAT PORTION OF THE CPU BOARD FROM THE S-100 BUS, THUS ALLOWING EXTERNAL DEVICES TO CONTROL THE S-100 BUS. THIS FEATURE IS USEFUL IN DMA APPLICATIONS AND MULTIPROCESSOR SYSTEMS. THEY ARE DEFINED BELOW.

S-100 BUS DISABLE SIGNALS

SIGNAL	FUNCTION
CC DSBL (PIN 19)	DISABLES THE ACKNOWLEDGE AND CONTROL SIGNALS
ADDR DSBL (PIN 22)	DISABLES THE ADDRESS LINES
DO DSBL (PIN 23)	DISABLES THE OUTPUT DATA LINES
SSW DSBL (PIN 53)	DISABLES THE INPUT DATA LINES
STAT DSBL (PIN 18)	DISABLES THE STATUS LINES

ALL S-100 BUS INTERFACES ARE PROVIDED WITH APPROPRIATE PULL UP RESISTORS FOR

OPTIMUM RESPONSE OF SIGNALS ON THE BUS.

JUMPER INSTALLATION

IF IT IS DESIRED TO USE THE REAL TIME CLOCK FUNCTION ON THE CPU BOARD, A JUMPER MUST BE INSTALLED TO SELECT WHICH INTERRUPT THE CLOCK WILL ACTIVATE. ONLY ONE JUMPER SHOULD BE USED. THIS JUMPER WILL CONNECT THE REAL TIME CLOCK OUTPUT TO THE DESIRED INTERRUPT INPUT. FOR EXAMPLE, IF ONE WISHES TO HAVE THE CLOCK ENTER ON INTERRUPT NUMBER 5 THEN A JUMPER SHOULD BE INSTALLED FROM THE CLOCK TO THE VI5 INTERRUPT.

A PAD IS PROVIDED ON THE PRINTED CIRCUIT BOARD AT THE OUTPUT OF THE REAL TIME CLOCK. THIS POINT IS IDENTIFIED ON THE ASSEMBLY DRAWING AS RTC. SIMPLY SOLDER A WIRE FROM RTC TO THE DESIRED INTERRUPT VI0 TO VI7. PADS ARE PROVIDED FOR EACH INTERRUPT AND ARE LABELED.

CLOCK DEMONSTRATION PROGRAM

A PROGRAM TO DEMONSTRATE THE USE OF INTERRUPTS AND THE REAL TIME CLOCK (RTC) IS LISTED ON THE FOLLOWING PAGES. IN ORDER TO RUN THE PROGRAM, THE RTC INTERRUPT MUST BE JUMPERED ON THE CPU BOARD TO VIO, WHICH CAUSES A "RST 7" TO BE EXECUTED ON INTERRUPT. THIS IS DONE BY SOLDERING A JUMPER BETWEEN THE TWO BOTTOM PADS IN THE COLUMN OF PADS IMMEDIATELY TO THE RIGHT OF C1. A VIDEO DISPLAY IS ASSUMED AT ADDRESS D000.

THE PROGRAM CAN BE LOADED INTO RAM ON THE PROM/RAM BOARD AT CC00 USING THE "P" COMMAND FROM THE MONITOR AND THEN SAVED ON TAPE. EXECUTE THE PROGRAM INITIALLY AT CCB4 (TEST), WHICH HAS A DELAY LOOP TO SIMULATE THE RTC. THIS DOES NOT USE THE INTERRUPTS, BUT WILL DISPLAY AN INCREMENTING TIME ON THE SCREEN TO MAKE SURE THE PROGRAM IS FUNCTIONING.

NOTE: IF YOU HAVE A 3P+S BOARD IN YOUR SYSTEM, CHECK TO MAKE SURE THAT UNUSED CIRCUITRY IS NOT PULLING SOME OF THE INTERRUPT LINES LOW. IT IS NECESSARY TO LEAVE SEVERAL OF THE IC'S OUT IF THEIR INPUTS ARE NOT CONNECTED.

IF THE PROGRAM APPEARS TO BE FUNCTIONING, EXECUTE AT CC00. THE FIRST INSTRUCTIONS WRITE THE "JMP COUNT" INSTRUCTIONS AT LOCATION 0038F IN MEMORY, INITIALIZE THE CURRENT STATUS REGISTER IN THE 8214 PRIORITY ENCODER BY OUTPUTTING 8 TO PORT FD, AND ENABLE THE INTERRUPT FLIP-FLOP IN THE MPU. THIS MUST BE DONE INITIALLY SINCE A POWER UP OR RESET ALSO RESETS THE INTERRUPT FLIP-FLOP, AND IT MUST BE REPEATED AFTER EACH INTERRUPT, WHICH AUTOMATICALLY RESETS THE 8214 AND DISABLES INTERRUPTS. AT THE END OF THIS ROUTINE, EXECUTION RETURNS TO THE MONITOR, OR ANY OTHER PROGRAM THAT INITIALLY CALLS "START".

AN INTERRUPT, WHICH OCCURS EVERY 1/120TH SECOND, CAUSES NORMAL PROGRAM EXECUTION TO BE SUSPENDED, AND THE "COUNT" ROUTINE TO BE EXECUTED. SINCE MANY PROGRAMS HAVE A LIMITED SPACE ALLOCATED FOR THE STACK, THE STACK POINTER IS SAVED AND THE STACK IS REINITIALIZED BELOW THE VIDEO DRIVER STORAGE LOCATIONS AND THEN ALL MPU REGISTERS ARE SAVED. NOTICE THE ORDER IN WHICH THIS IS DONE. THE PSW MUST BE SAVED ON THE OLD STACK BECAUSE DAD SP CHANGES THE CY FLAG.

A CALL TO "TICK" INCREMENTS THE TIME DIGITS STORED AT FACE IN BCD FORMAT AND PROPOGATES A CARRY AS EACH DIGIT OVERFLOWS. THE NUMBER LOADED IN THE "B" REGISTER WHEN "TOCK" IS CALLED DETERMINES THE MODULUS OF EACH REGISTER IN BCD, NOT BINARY. FOR EXAMPLE, THE FIRST CALL TO "TOCK" DIVIDES THE INTERRUPT FREQUENCY BY 12 TO PRODUCE A 10 HZ COUNT RATE. IF THE INCREMENTED REGISTER DOES NOT OVERFLOW, "TOCK" RETURNS TWO LEVELS. THE FIRST DIGIT REGISTER IS EXAMINED, AND IF IT IS ZERO, INDICATING THAT THE TIME HAS CHANGED AND THE DISPLAY MUST BE UPDATED, "DISP" IS CALLED, WHICH WRITES THE DIGITS ON THE UPPER RIGHT HAND CORNER OF THE SCREEN IN THE FOLLOWING FORMAT:

AM - 09:36:25.3

THE TIME IS IN A MODIFIED MILITARY FORMAT; I.E., HALF PAST MIDNIGHT OR NOON = 00:30:00.0

BEFORE RETURNING TO THE PROGRAM INTERRUPTED, THE MPU REGISTERS AND THE STACK POINTER ARE RESTORED, AND INTERRUPTS ARE ENABLED.

THE PROGRAM CAN BE USED WITH OTHER PROGRAMS THAT DO NOT USE THE RST 7 LOCATION OR DEPEND ON CRITICAL TIMING. INCLUDED IN THIS GROUP IS MITS BASIC. THE START ROUTINE WILL OVERWRITE BASIC WITH THE NECESSARY CODE, INCLUDING EI AT LOCATION 0000, WHICH PERMITS RETURNING TO BASIC WITH THE CLOCK RUNNING.

THE PROGRAM CAN BE USED WITHOUT CHANGES WITH THE FOLLOWING VIDEO BOARDS:

VECTOR GRAPHIC FLASH WRITER
VDM-1
POLYMORPHIC VTI
SOLID STATE MUSIC

OPTIONALLY, "PBIAS" CAN BE SET TO 0 FOR ALL OF THE ABOVE EXCEPT VTI IF REVERSE VIDEO IS NOT DESIRED.

THE TIME IS SET USING THE MONITOR "P" COMMAND BY MODIFYING MEMORY LOCATIONS CC16 THROUGH CC1B.

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CC00                    0001 * CLOCK DEMONSTRATION PROGRAM
CC00                    0002 * R. S. HARP 9/4/77
CC00                    0004 PBIAS  EQU   80H
CC00                    0005 *
CC00                    0006 * THIS ROUTINE PUTS THE PROPER CODE AT RST 7
CC00 21 38 00           0010 START  LXI   H,38H          RST 7
CC03 36 C3              0020        MVI   M,0C3H
CC05 21 1C CC           0030        LXI   H,COUNT
CC08 22 39 00           0040        SHLD  39H
CC0B 3E FB              0050        MVI   A,0FBH         ENABLE INTER.
CC0D 32 00 00           0060        STA   0
CC10 3E 08              0070        MVI   A,008H
CC12 D3 FD              0080        OUT   0FDH           SET CUR STAT LATCH
CC14 FB                 0090        EI
CC15 C9                 0100        RET
CC16                    0110 FACE   DS    6              STORAGE FOR TIME
CC1C E5                 0140 COUNT  PUSH  H              MOVE THE STACK
CC1D F5                 0145        PUSH  PSW
CC1E 21 00 00           0150        LXI   H,00
CC21 39                 0160        DAD   SP
CC22 31 00 CF           0170        LXI   SP,0CF00H
CC25 E5                 0180        PUSH  H
CC26 C5                 0190        PUSH  B
CC27 D5                 0200        PUSH  D
CC28 21 16 CC           0210        LXI   H,FACE
CC2B CD 87 CC           0220        CALL  TICK
CC2E 21 16 CC           0230        LXI   H,FACE
CC31 7E                 0240        MOV   A,M
CC32 B6                 0250        ORA   M
CC33 CC 42 CC           0260        CZ    DISP
CC36 3E 08              0270        MVI   A,008H
CC38 D3 FD              0280        OUT   0FDH
CC3A D1                 0290        POP   D
CC3B C1                 0300        POP   B
CC3C E1                 0310        POP   H
CC3D F9                 0320        SPHL
CC3E F1                 0330        POP   PSW
CC3F E1                 0340        POP   H
CC40 FB                 0350        EI
CC41 C9                 0360        RET
CC42                    0365 * FORMAT THE DISPLAY
CC42 11 3F D0           0370 DISP   LXI   D,0D03FH
CC45 23                 0380        INX   H
CC46 CD 70 CC           0390        CALL  WRT2
CC49 23                 0400        INX   H
CC4A 36 AE              0410        MVI   M,'.'+PBIAS
CC4C EB                 0420        XCHG
CC4D 1B                 0430        DCX   D
CC4E CD 70 CC           0440        CALL  WRT2
CC51 36 BA              0450        MVI   M,':'+PBIAS
CC53 EB                 0460        XCHG
CC54 1B                 0470        DCX   D
CC55 CD 70 CC           0480        CALL  WRT2
CC58 36 BA              0490        MVI   M,':'+PBIAS
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CC5A EB                 0500          XCHG
CC5B 1B                 0510          DCX   D
CC5C CD 70 CC           0520          CALL  WRT2
CC5F EB                 0530          XCHG
CC60 46                 0540          MOV   B,M
CC61 EB                 0550          XCHG
CC62 36 AD              0560          MVI   M,'-'+PBIAS
CC64 2B                 0570          DCX   H
CC65 36 CD              0580          MVI   M,'M'+PBIAS
CC67 2B                 0590          DCX   H
CC68 AF                 0600          XRA   A
CC69 B8                 0610          CMP   B
CC6A 36 C1              0620          MVI   M,'A'+PBIAS
CC6C C8                 0630          RZ
CC6D 36 D0              0640          MVI   M,'P'+PBIAS
CC6F C9                 0650          RET
CC70                    0655 * WRITE THE DIGITS ON THE SCREEN
CC70 7E                 0660 WRT2     MOV   A,M
CC71 E6 0F              0670          ANI   00FH
CC73 F6 B0              0680          ORI   30H+PBIAS
CC75 EB                 0690          XCHG
CC76 77                 0700          MOV   M,A
CC77 EB                 0710          XCHG
CC78 1B                 0720          DCX   D
CC79 7E                 0730          MOV   A,M
CC7A 1F                 0740          RAR
CC7B 1F                 0750          RAR
CC7C 1F                 0760          RAR
CC7D 1F                 0770          RAR
CC7E E6 0F              0780          ANI   00FH
CC80 F6 B0              0790          ORI   30H+PBIAS
CC82 EB                 0800          XCHG
CC83 77                 0810          MOV   M,A
CC84 2B                 0820          DCX   H
CC85 13                 0830          INX   D
CC86 C9                 0840          RET
CC87                    0845 * INCREMENT THE TIME
CC87 06 12              0850 TICK     MVI   B,012H
CC89 CD A6 CC           0860          CALL  TOCK
CC8C 06 10              0870          MVI   B,010H
CC8E CD A6 CC           0880          CALL  TOCK
CC91 06 60              0890          MVI   B,060H
CC93 CD A6 CC           0900          CALL  TOCK
CC96 06 60              0910          MVI   B,060H
CC98 CD A6 CC           0920          CALL  TOCK
CC9B 06 12              0930          MVI   B,012H
CC9D CD A6 CC           0940          CALL  TOCK
CCA0 06 02              0950          MVI   B,002H
CCA2 CD A6 CC           0960          CALL  TOCK
CCA5 C9                 0970          RET
CCA6                    0975 * INCREMENT EACH DIGIT
CCA6 7E                 0980 TOCK     MOV   A,M
CCA7 3C                 0990          INR   A
CCA8 27                 1000          DAA
CCA9 B8                 1010          CMP   B
CCAA 77                 1020          MOV   M,A
```

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CCAB C2 B2 CC            1030          JNZ   NCAR
CCAE 36 00               1040          MVI   M,0
CCB0 23                  1050          INX   H
CCB1 C9                  1060          RET
CCB2 F1                  1070 NCAR     POP   PSW
CCB3 C9                  1080          RET
CCB4 CD 1C CC            1090 TEST     CALL  COUNT
CCB7 21 00 FE            1100          LXI   H,0FE00H
CCBA 2C                  1110 DELAY    INR   L
CCBB C2 BA CC            1120          JNZ   DELAY
CCBE 24                  1130          INR   H
CCBF C2 BA CC            1140          JNZ   DELAY
CCC2 C3 B4 CC            1150          JMP   TEST
CCC5                     9000 *

SYMBOL TABLE

COUNT CC1C   DELAY CCBA   DISP  CC42   FACE  CC16   NCAR  CCB2   PBIAS 0080
START CC00   TEST  CCB4   TICK  CC87   TOCK  CCA6   WRT2  CC70

$D CC00 CCC4
CC00 21 38 00 36 C3 21 1C CC 22 39 00 3E FB 32 00 00
CC10 3E 08 D3 FD FB C9 10 01 00 14 00 01 E5 F5 21 00
CC20 00 39 31 00 CF E5 C5 D5 21 16 CC CD 87 CC 21 16
CC30 CC 7E B6 CC 42 CC 3E 08 D3 FD D1 C1 E1 F9 F1 E1
CC40 FB C9 11 3F D0 23 CD 70 CC 23 36 AE EB 1B CD 70
CC50 CC 36 BA EB 1B CD 70 CC 36 BA EB 1B CD 70 CC EB
CC60 46 EB 36 AD 2B 36 CD 2B AF B8 36 C1 C8 36 D0 C9
CC70 7E E6 0F F6 B0 EB 77 EB 1B 7E 1F 1F 1F 1F E6 0F
CC80 F6 B0 EB 77 2B 13 C9 06 12 CD A6 CC 06 10 CD A6
CC90 CC 06 60 CD A6 CC 06 60 CD A6 CC 06 12 CD A6 CC
CCA0 06 02 CD A6 CC C9 7E 3C 27 B8 77 C2 B2 CC 36 00
CCB0 23 C9 F1 C9 CD 1C CC 21 00 FE 2C C2 BA CC 24 C2
CCC0 BA CC C3 B4 CC

$
```

TROUBLE SHOOTING HINTS

THE CPU BOARD IS A SOPHISTICATED MICROPROCESSOR WITH MANY TIME SEQUENCED OPERATIONS. COMPREHENSIVE TROUBLE SHOOTING TECHNIQUES REQUIRE THE USE OF A HIGH SPEED OSCILLOSCOPE AND INTIMATE KNOWLEDGE OF 8080A OPERATION. THE HINTS PROVIDED HERE WILL ALLOW THE USER TO REPAIR A BOARD FOR 90% OF MOST FAILURES, SINCE THEY ARE USUALLY ASSEMBLY ERRORS, SHORTS OR OBVIOUSLY FAILED PARTS.

IF THE CPU BOARD FAILS TO FUNCTION PROPERLY, MAKE THE FOLLOWING CHECKS:

1. CAREFULLY INSPECT FOR SOLDER SHORTS. A MINISCULE AMOUNT OF SOLDER ACROSS TWO PRINTED TRACES IS ALL THAT IS NEEDED FOR A SHORT.

2. CAREFULLY INSPECT FOR A CRACK IN A PC TRACE. THIS TYPE OF FAILURE HAS A LOWER PROBABILITY OF OCCURING.

3. CHECK THE POLARITY OF ALL DIODES AND ELECTROLYTIC CAPACITORS.

4. INSURE THAT ALL IC'S ARE PROPERLY INSTALLED WITH RESPECT TO PIN ORIENTATION. (SEE THE ASSEMBLY DRAWING.) THE MOST COMMON ASSEMBLY ERROR ENCOUNTERED IS IC PINS BENT UNDER THE CHIP. CAREFULLY INSPECT FOR THIS TYPE OF MISTAKE.

5. IF AN EXTENDER BOARD IS BEING USED AND YOU EXPERIENCE SEEMINGLY GHOST-LIKE FAILURES, INSERT THE CPU BOARD DIRECTLY IN THE MOTHERBOARD. TRANSIENT NOISE CAN BE CAUSED BY EXTENDER BOARDS.

STATEMENT OF WARRANTY

ALL COMPONENTS SOLD BY VECTOR GRAPHIC INC. ARE WARRANTEED FOR NINETY (90) DAYS AGAINST DEFECTS IN WORKMANSHIP OR MATERIALS. DEFECTIVE PARTS WILL BE REPLACED AT NO CHARGE WHEN RETURNED POSTPAID TO VECTOR GRAPHIC WITHIN THE WARRANTY PERIOD.

ANY PRODUCT PURCHASED AS A FACTORY ASSEMBLED UNIT IS WARRANTEED FOR 90 DAYS AGAINST DEFECTS IN WORKMANSHIP OR MATERIALS. ALL FACTORY ASSEMBLED UNITS RETURNED POSTPAID TO VECTOR GRAPHIC WITHIN THE WARRANTY PERIOD WILL BE REPAIRED AND RETURNED WITHOUT CHARGE.

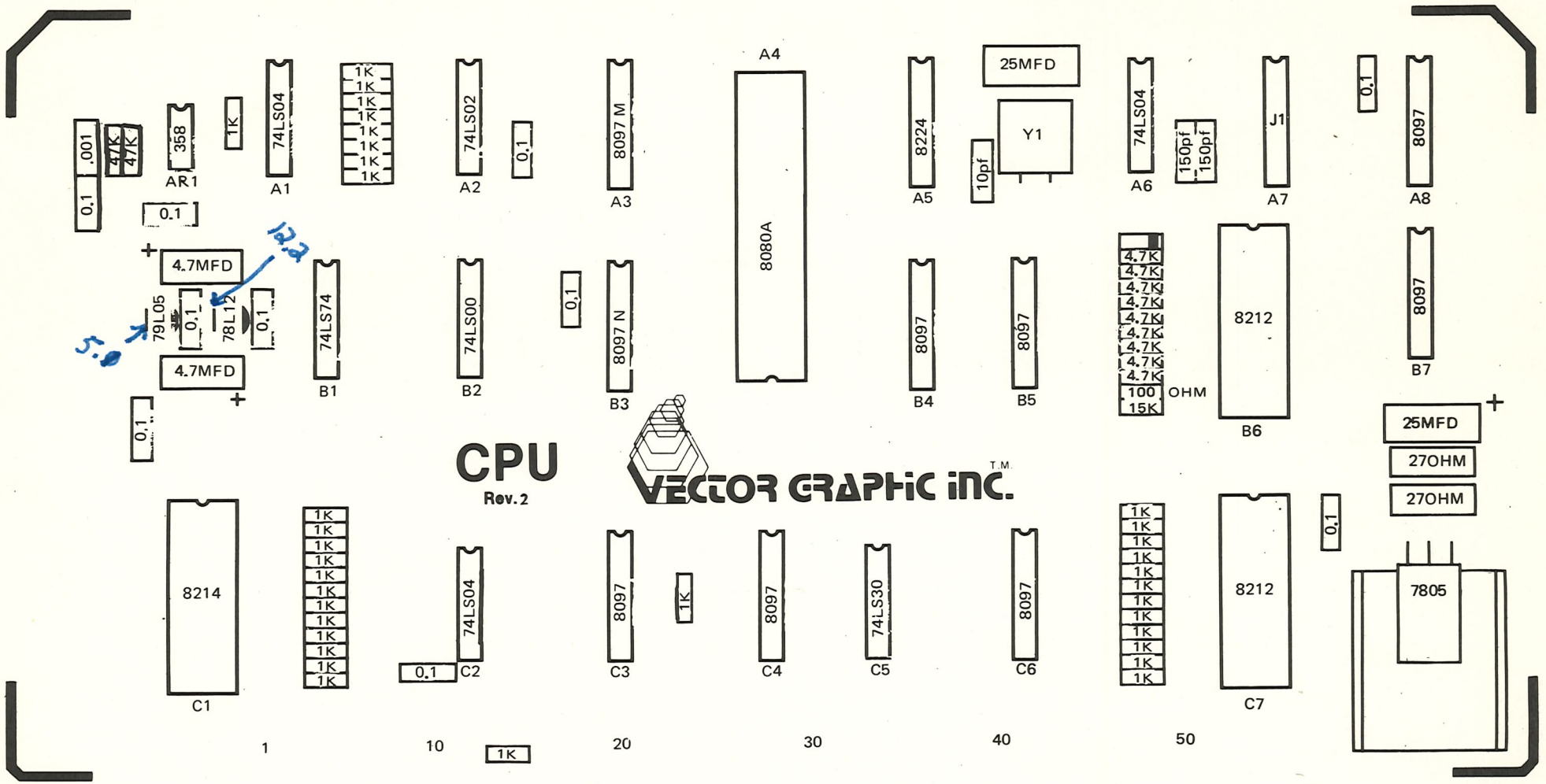
REPAIR AGREEMENT

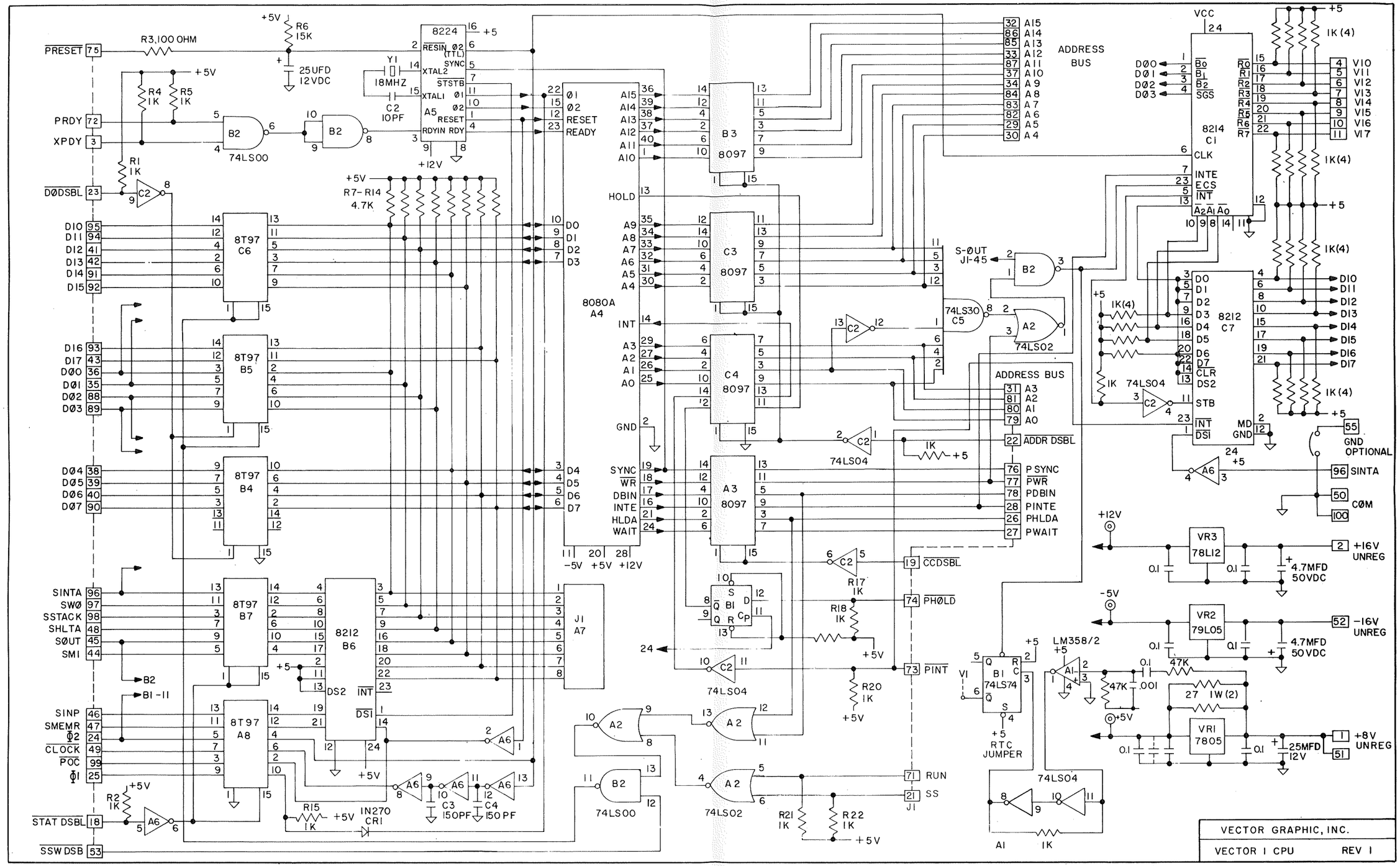
The CPU Board sold hereunder is sold "as is", with all faults and without any warranty, either expressed or implied, including any implied warranty of fitness for intended use or merchantability. However, the above notwithstanding, VECTOR GRAPHIC, INC., will, for a period of ninety (90) days following delivery to customer, repair or replace any CPU Board that is found to contain defects in materials or workmanship, provided:

1. Such defect in material or workmanship existed at the time the CPU Board left the VECTOR GRAPHIC, INC., factory;
2. VECTOR GRAPHIC, INC., is given notice of the precise defect claimed within ten (10) days after its discovery;
3. The CPU Board is promptly returned to VECTOR GRAPHIC, INC., at customer's expense, for examination by VECTOR GRAPHIC, INC., to confirm the alleged defect, and for subsequent repair or replacement if found to be in order.

Repair, replacement or correction of any defects in material or workmanship which are discovered after expiration of the period set forth above will be performed by VECTOR GRAPHIC, INC., at Buyer's expense, provided the CPU Board is returned, also at Buyer's expense, to VECTOR GRAPHIC, INC., for such repair, replacement or correction. In performing any repair, replacement or correction after expiration of the period set forth above, Buyer will be charged in addition to the cost of parts the then-current VECTOR GRAPHIC, INC., repair rate. At the present time the applicable rate is $35.00 for the first hour, and $18.00 per hour for every hour of work required thereafter. Prior to commencing any repair, replacement or correction of defects in material or workmanship discovered after expiration of the period for no-cost-to-Buyer repairs, VECTOR GRAPHIC, INC., will submit to Buyer a written estimate of the expected charges, and VECTOR GRAPHIC, INC., will not commence repair until such time as the written estimate of charges has been returned by Buyer to VECTOR GRAPHIC, INC., signed by duly authorized representative authorizing VECTOR GRAPHIC, INC., to commence with the repair work involved. VECTOR GRAPHIC, INC., shall have no obligation to repair, replace or correct any CPU Board until the written estimate has been returned with approval to proceed, and VECTOR GRAPHIC, INC., may at its option also require prepayment of the estimated repair charges prior to commencing work.

Repair Agreement void if the enclosed card is not returned to VECTOR GRAPHIC, INC. within ten (10) days of end consumer purchase.


CPU
Rev. 2
VECTOR GRAPHIC INC.
T.M.
A1
A2
A3
A4
A5
A6
A7
A8
B1
B2
B3
B4
B5
B6
B7
C1
C2
C3
C4
C5
C6
C7
AR1
8080A
8212
8214
8097
74LS04
74LS02
74LS00
74LS74
74LS30
8224
25MFD
Y1
10pf
150pf
4.7MFD
79L05
78L12
5.0
12
OHM
27OHM
7805
1
10
20
30
40
50


PRESET
R3,100 OHM
+5V
R6 15K
25UFD 12VDC
8224
RESIN
XTAL2
XTALI
RESET
RDYIN
SYNC
STSTB
RDY
Y1 18MHZ
C2 10PF
PRDY
XPDY
R4 1K
R5 1K
B2
74LS00
R1 1K
C2
DØDSBL
+12V
R7-R14 4.7K
8T97 C6
8T97 B5
8T97 B4
8T97 B7
8T97 A8
8212 B6
J1 A7
DI0
DI1
DI2
DI3
DI4
DI5
DI6
DI7
DØ0
DØ1
DØ2
DØ3
DØ4
DØ5
DØ6
DØ7
D0
D1
D2
D3
D4
D5
D6
D7
ØI
Ø2
RESET
READY
-5V +5V +12V
8080A A4
HOLD
INT
GND
SYNC
WR
DBIN
INTE
HLDA
WAIT
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
B3 8097
C3 8097
C4 8097
A3 8097
ADDRESS BUS
S-OUT J1-45
74LS30 C5
74LS02
74LS04
ADDR DSBL
P SYNC
PWR
PDBIN
PINTE
PHLDA
PWAIT
CCDSBL
PHØLD
PINT
RUN
SS
R17 1K
R18 1K
R20 1K
R21 1K
R22 1K
VCC
8214 C1
CLK
INTE
ECS
INT
8212 C7
CLR
DS2
STB
DSI
MD
GND
IK(4)
GND OPTIONAL
SINTA
COM
VR3 78L12
+16V UNREG
4.7MFD 50VDC
VR2 79L05
-16V UNREG
LM358/2
47K
.001
27 IW (2)
VR1 7805
+8V UNREG
25MFD 12V
RTC JUMPER
74LS74
SINTA
SWØ
SSTACK
SHLTA
SØUT
SMI
SINP
SMEMR
CLOCK
POC
STAT DSBL
SSW DSB
R2 1K
R15 1K
CR1 IN270
C3 150PF
C4 150 PF
VECTOR GRAPHIC, INC.
VECTOR I CPU REV I