VECTOR

16K STATIC RAM

User's Manual

REPAIR AGREEMENT

The 16K Static RAM board sold hereunder is sold "as is", with all faults and without any warranty, either expressed or implied, including any implied warranty of fitness for intended use or merchantability. However, the above notwithstanding, VECTOR GRAPHIC, INC., will, for a period of ninety (90) days following delivery to customer, repair or replace any 16K Static RAM board that is found to contain defects in materials or workmanship, provided:

1. Such defect in material or workmanship existed at the time the 16K Static RAM board left the VECTOR GRAPHIC, INC., factory;
2. VECTOR GRAPHIC, INC., is given notice of the precise defect claimed within ten (10) days after its discovery;
3. The 16K Static RAM board is promptly returned to VECTOR GRAPHIC, INC., at customer's expense, for examination by VECTOR GRAPHIC, INC., to confirm the alleged defect, and for subsequent repair or replacement if found to be in order.

Repair, replacement or correction of any defects in material or workmanship which are discovered after expiration of the period set forth above will be performed by VECTOR GRAPHIC, INC., at Buyer's expense, provided the 16K Static RAM board is returned, also at Buyer's expense, to VECTOR GRAPHIC, INC., for such repair, replacement or correction. In performing any repair, replacement or correction after expiration of the period set forth above, Buyer will be charged in addition to the cost of parts the then-current VECTOR GRAPHIC, INC., repair rate. At the present time the applicable rate is $35.00 for the first hour, and $18.00 per hour for every hour of work required thereafter. Prior to commencing any repair, replacement or correction of defects in material or workmanship discovered after expiration of the period for no-cost-to-Buyer repairs, VECTOR GRAPHIC, INC., will submit to Buyer a written estimate of the expected charges, and VECTOR GRAPHIC, INC., will not commence repair until such time as the written estimate of charges has been returned by Buyer to VECTOR GRAPHIC, INC., signed by duly authorized representative authorizing VECTOR GRAPHIC, INC., to commence with the repair work involved. VECTOR GRAPHIC, INC., shall have no obligation to repair, replace or correct any 16K Static RAM board until the written estimate has been returned with approval to proceed, and VECTOR GRAPHIC, INC., may at its option also require prepayment of the estimated repair charges prior to commencing work.

Repair Agreement void if the enclosed card is not returned to VECTOR GRAPHIC, INC. within ten (10) days of end consumer purchase.

16K BOARD

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INTRODUCTION

THE VECTOR GRAPHIC 16K STATIC MEMORY BOARD IS DESIGNED TO BE PLUG-IN COMPATIBLE WITH ALL S-100 BUS COMPUTER SYSTEMS. WE HAVE PROVIDED A HIGH QUALITY PRODUCT BY USING THE FINEST AVAILABLE MEMORY CHIPS AND AEROSPACE QUALITY PRINTED CIRCUIT BOARD. THE MEMORY WILL OPERATE AT A FULL 4 MHZ CLOCK RATE WITHOUT WAIT STATES MAKING IT FULLY COMPATIBLE WITH ALL 8080 AND Z-80 CPU'S. ALL ADDRESS, DATA AND CONTROL LINES ARE FULLY BUFFERED TO REDUCE CAPACITIVE LOADING ON THE BUS. ALL ADDRESS LINES USE SCHMITT TRIGGER BUFFERS FOR BETTER IMMUNITY TO NOISE AND MORE RELIABLE OPERATION. ORGANIZED AS TWO INDEPENDENT 8K BLOCKS, ADDRESS SELECTION IS BY MEANS OF A DIP SWITCH LOCATED ON THE UPPER EDGE OF THE BOARD. WITH THIS FEATURE YOU MAY SEE AND CHANGE MEMORY ADDRESSES WITHOUT REMOVING BOARDS FROM THE COMPUTER. BANK SELECT SWITCHES ARE ALSO LOCATED AT THE TOP EDGE THE BOARD. THESE SWITCHES ALLOW MEMORY BOARDS TO BE ALLOCATED TO 1 OF 8 BANKS OF 65K BYTES EACH, THUS PERMITTING A TOTAL OF 524K BYTES OF CPU ADDRESSABLE MEMORY. ANOTHER FEATURE IS THE OUTPUT DISABLE FEATURE WHICH PERMITS START UP OF THE COMPUTER WITHOUT THE FRONT PANEL SWITCHES. TYPICAL POWER CONSUMPTION OF THE BOARD IS 2.0 AMPS (@ 8V).

THE PURPOSE OF THESE INSTRUCTIONS IS TO HELP YOU PRODUCE THE BEST RESULTS IN THE SHORTEST TIME WITH NO DAMAGE TO THE VARIOUS COMPONENTS.

IF THERE IS ANYTHING THAT YOU DO NOT UNDERSTAND, PLEASE DO NOT HESITATE TO CALL OR WRITE US!

AFTER COMPLETING THE ASSEMBLY, PLEASE FILL OUT AND RETURN THE WARRANTY CARD SO THAT WE CAN ADD YOU TO OUR MAILING LIST FOR FUTURE PRODUCTS.

IMPORTANT PRECAUTIONS

POWER MUST BE OFF WHEN:

INSERTING OR REMOVING BOARDS OR IC CHIPS
CONNECTING OR DISCONNECTING WIRES
SOLDERING

ONLY SOLDER WITH:

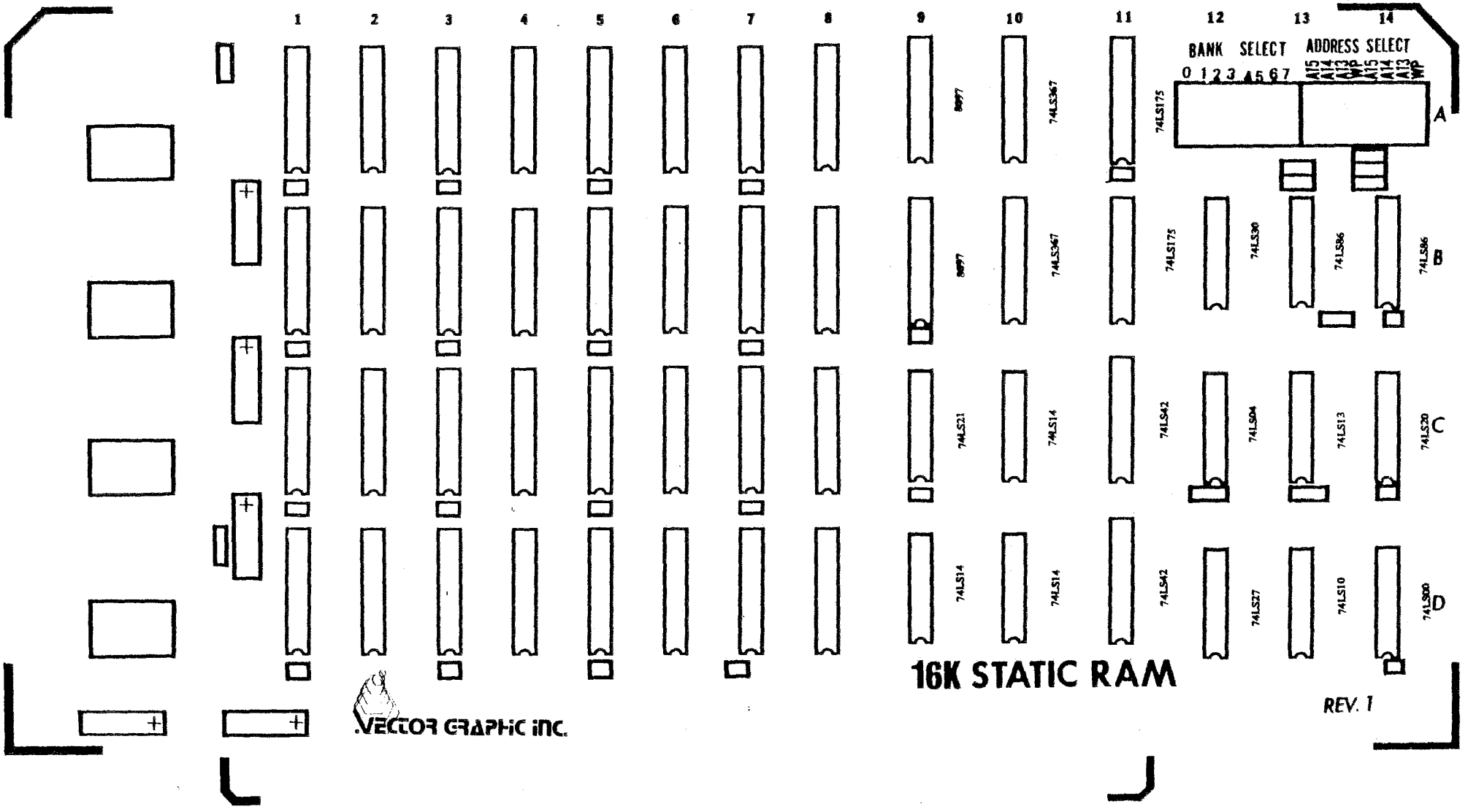
30 WATT MAXIMUM SOLDERING IRON
60/40 ROSIN CORE SOLDER

ALWAYS PROTECT MOS CHIPS FROM STATIC ELECTRICITY.

16K BOARD CONTENTS

QTY.	DESCRIPTION
1	PRINTED CIRCUIT BOARD
4	6106B HEAT SINK
4	7805/340T-5 REGULATOR
2	74367/8097 (A9, B9)
1	74LS00 (D14)
1	74LS04 (C12)
2	74LS367 (A10, B10)
3	74LS14 (C10, D9, D10)
1	74LS13 (C13)
1	74LS21 (C9)
1	74LS27 (D12)
2	74LS42 (C11, D11)
2	74LS86 (B13, B14)
1	74LS30 (B12)
2	74LS175 (A11, B11)
1	74LS10 (D13)
1	74LS20 (C14)
32	2114 (A1-A8, B1-B8, C1-C8, D1-D8)

QTY.	DESCRIPTION
5	22 MFD 16V AXIAL ELECTROLYTIC CAPACITORS
22	0.1 MFD 50V MONOLITHIC RADIAL CAPACITORS
10	4.7K 1/4 WATT CARBON RESISTORS (STRIPES OF YELLOW, VIOLET, RED)
2	8 POSITION DIP SWITCHS
2	EJECTORS
32	18 PIN SOCKETS
8	16 PIN SOCKETS
13	14 PIN SOCKETS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BANK SELECT
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ADDRESS SELECT
A15
A14
A13
WP
A15
A14
A13
WP
74LS175
A
8097
74LS367
74LS175
74LS30
74LS86
74LS86
B
8097
74LS367
74LS21
74LS14
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74LS04
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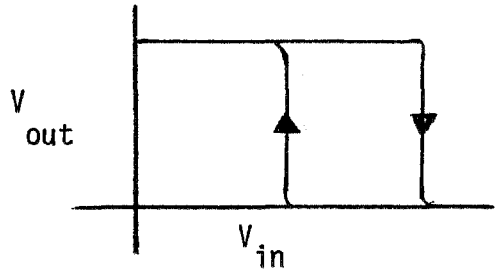
16K STATIC RAM
REV. 1
VECTOR GRAPHIC INC.

THEORY OF OPERATION

THE 16K STATIC MEMORY REPRESENTS AN IMPRESSIVE TECHNOLOGICAL FEAT IN THAT IT CONTAINS WITHIN THE 32 2114 MEMORY CHIPS WELL OVER 750,000 TRANSISTORS. EACH BIT OF INFORMATION IS STORED IN A BISTABLE FLIP-FLOP COMPRISED OF 6 TRANSISTORS. MOST OF THE ADDRESS DECODING TO SELECT AN INDIVIDUAL FLIP-FLOP (CALLED A CELL) IS DONE WITHIN THE CHIP ITSELF. THE CHIPS ARE ORGANIZED AS 1K ADDRESSABLE LOCATIONS OF 4 BITS. THUS TO SELECT AN 8 BIT BYTE, TWO CHIPS MUST BE SELECTED IN PARALLEL. THE TEN LOW ORDER ADDRESS LINES GENERATED BY THE CPU ARE BUFFERED AND INVERTED BY 74LS14 SCHMITT TRIGGERS, AND APPLIED TO THE 32 CHIPS IN PARALLEL. AFTER A MOMENTS CONSIDERATION, YOU SHOULD BE ABLE TO CONVINCE YOURSELF THAT THE ORDER IN WHICH THE ADDRESS LINES ARE CONNECTED TO THE CHIP AS WELL AS THE LOGIC POLARITY IS NOT SIGNIFICANT, SINCE THE SAME CONNECTIONS ARE USED TO READ DATA FROM THE MEMORY AS TO WRITE IT. IT IS IMPORTANT THAT THE ADDRESS LINES GOING TO THE CHIPS BE BUFFERED SINCE THEY REPRESENT A CAPACITIVE LOAD OF ABOUT 150 PF ON EACH ADDRESS LINE, AND THIS MUCH CAPACITANCE WOULD EXCESSIVELY LOAD THE BUS, ANOTHER IMPORTANT CONSIDERATION IS THAT THESE SIGNALS SHOULD BE AS CLEAN AS POSSIBLE WITH NO "GLITCHES" WHICH WOULD CAUSE IMPROPER OPERATION OF THE INTERNAL ADDRESS DECODING IN THE CHIPS. FOR THIS REASON, SCHMITT TRIGGER INVERTERS ARE USED ON ALL ADDRESS INPUTS. THEY HAVE THE CHARACTERISTIC THAT THEIR LOGIC THRESHOLD HAS HYSTERESIS, AS SHOWN BELOW.



THIS FEATURE TENDS TO PREVENT NARROW NOISE SPIKES OR OVERSHOOT AND RINGING FROM HAVING ANY EFFECT.

THE MEMORY IS ORGANIZED AS TWO INDEPENDENT 8K BLOCKS, SO THE 3 MOST SIGNIFICANT BITS ARE DECODED TO SELECT BLOCK A AND B. THE ADDRESS LINES ARE FIRST BUFFERED BY SCHMITT TRIGGERS TO MINIMIZE BUS LOADING AND NOISE AND THEN PROCESSED BY 74LS86 EXCLUSIVE OR GATES. THESE GATES CAN BE THOUGHT OF AS CONTROLLED INVERTERS. IF THE SECOND INPUT IS HI, THE SIGNAL APPLIED TO THE FIRST INPUT WILL APPEAR AT THE OUTPUT INVERTED. IF THE SECOND INPUT IS LO, THE SIGNAL WILL APPEAR AT THE OUTPUT WITHOUT INVERSION. BY OPENING OR CLOSING THE ADDRESS SELECT SWITCHES, THE POLARITY OF THE ADDRESS LINES REQUIRED TO SELECT AN 8K BLOCK CAN BE SELECTED, THEREBY CAUSING THE MEMORY TO RESPOND TO 1 OF 8 POSSIBLE ADDRESSES WITHIN THE 64K ADDRESS RANGE OF THE CPU:

0000	-	1FFF	LO	LO	LO	
2000	-	3FFF	LO	LO	HI	
4000	-	5FFF	LO	HI	LO	HI = UP OR OPEN
6000	-	7FFF	LO	HI	HI	
8000	-	9FFF	HI	LO	LO	LO = DOWN OF CLOSED
A000	-	BFFF	HI	LO	HI	
C000	-	DFFF	HI	HI	LO	
E000	-	FFFF	HI	HI	HI	

THE THREE REMAINING ADDRESS LINES A10, 11, 12 ARE DECODED BY A 74LS42 DECODER TO SELECT ONE PAIR OF MEMORY CHIPS OUT OF 16 FOR EACH BLOCK BY PULLING THE CE INPUT LOW. NOTE THAT SINCE THE INPUTS TO THE 74LS42 ARE INVERTED, THE ORDER OF THE OUTPUTS IS REVERSED. THE 2114 MEMORY CHIPS HAVE COMMON INPUT AND OUTPUT LINES. THE DIRECTION OF SIGNAL FLOW IS CONTROLLED BY THE $\overline{WE}$ SIGNAL. IF THIS SIGNAL IS HI, THE LINES ARE USED TO OUTPUT DATA, IF IT IS LOW, THE DRIVERS WITHIN THE CHIP ARE DISABLED AND THE LINES ARE USED TO INPUT DATA. INTERFACING TO THE S-100 BUS IS ACCOMPLISHED USING 74LS367 TRI STATE DRIVERS ON THE DO LINES WHICH ARE ENABLED BY THE $\overline{WE}$ SIGNAL. DATA OUTPUT FROM MEMORY IS BUFFERED USING 8097 OR 74367 DRIVERS CONNECTED TO THE DI LINES. WHILE DATA READ FROM MEMORY IS AVAILABLE AT THE CHIP OUTPUTS WHENEVER THEIR $\overline{CE}$ LINE IS LO, SEVERAL ADDITIONAL CONDITIONS MUST BE SATISFIED BEFORE THE DATA IS PLACED ON THE DI BUS. GATE C13-8 ANDS SMEMR, PDBIN, $\overline{PHANTOM}$ AND A SIGNAL FROM PIN 66 WHICH WILL BE USED FOR FUTURE APPLICATIONS. SMEMR INDICATES THAT THE CURRENT MACHINE CYCLE IS A MEMORY READ CYCLE (THIS INCLUDES M1, STACK READ, HALT ACKNOWLEDGE CYCLES). THE $\overline{PHANTOM}$ SIGNAL IS USED TO DISABLE THE BUS DRIVERS AFTER A SYSTEM RESET FOR USE WITH THE RESET AND GO PROM RAM BOARD, AND ALLOWS THE PROM RAM BOARD TO OVERLAY RAM FOR THE JUMP ON RESET FEATURE. FOR NORMAL OPERATION THIS SIGNAL IS HI. THE PDBIN SIGNAL CONTROLS THE TIMING OF DATA TO BE PLACED ON THE BUS, AND IS USED BY THE CPU TO INDICATE WHERE AN ADDRESSED BOARD MAY TAKE CONTROL OF THE BUS. THE LEADING EDGE OF THIS SIGNAL IS DELAYED FROM THE START OF THE MACHINE CYCLE TO PREVENT BUS CONFLICTS WHILE INDIVIUAL BOARDS DECODE THE ADDRESS BUS AND THE TRAILING EDGE PRECEEDS ANY CHANGE IN THE ADDRESS FOR THE NEXT MACHINE CYCLE. SCHMITT TRIGGER INPUTS FOR EACH OF THESE SIGNALS ENSURE RELIABLE OPERATION, AND THE OUTPUT OF D14-8 IS GATED WITH A SIGNAL FROM D14-6 WHICH IS HI WHEN EITHER BLOCK IS ADDRESSED TO ENABLE THE DI DRIVERS.

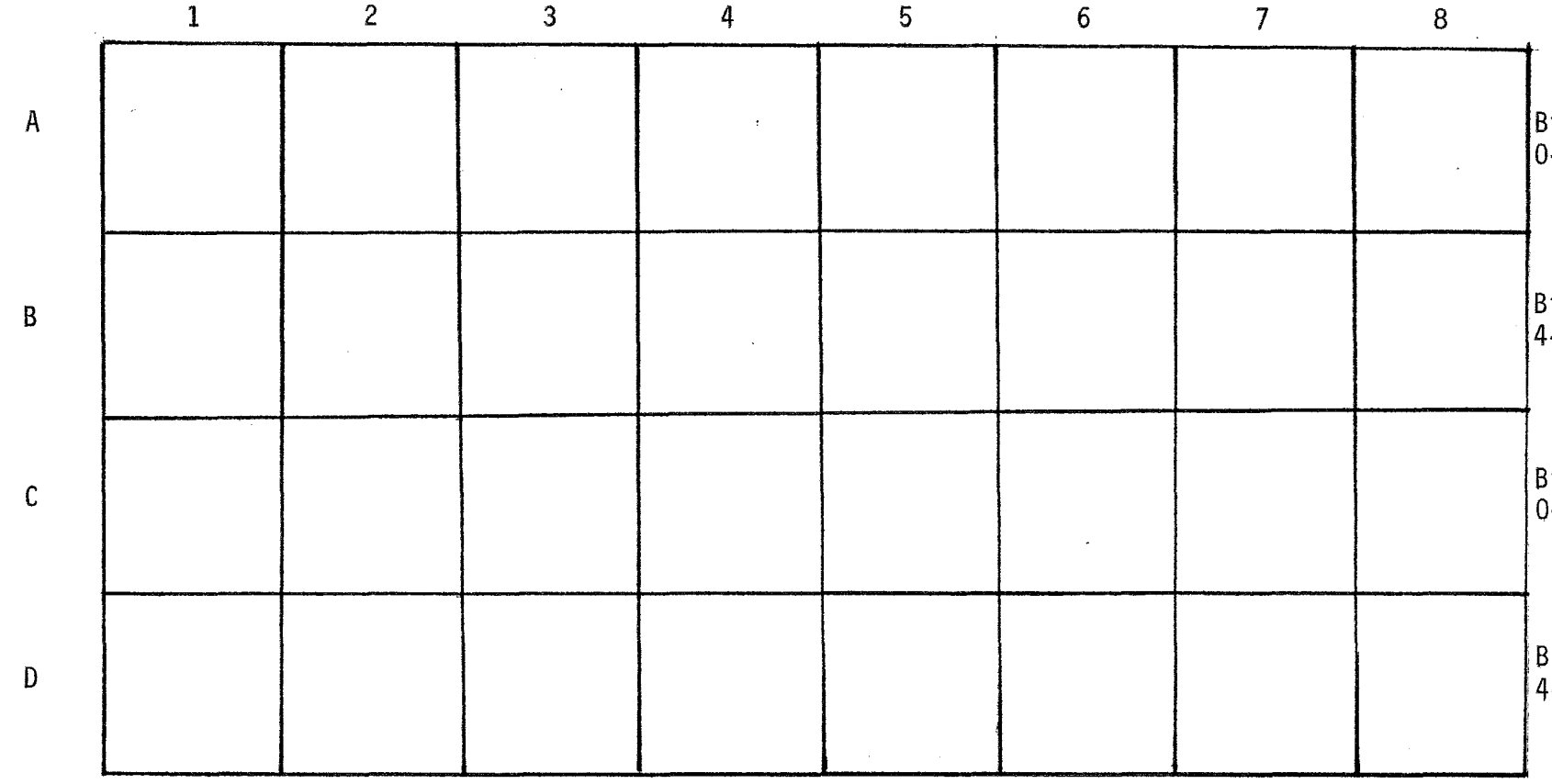
FOR MANY APPLICATIONS, THE 64K ADDRESS SPACE PROVIDED BY THE CPU IS NOT ADEQUATE. AN EXAMPLE IS WHERE LARGE PROGRAMS ARE ASSEMBLED FROM SOURCE FILES. A 12K OBJECT CODE PROGRAM WOULD TYPICALLY REQUIRE ABOUT 200K OF COMMENTED SOURCE CODE. THIS AMOUNT OF MEMORY CAN BE ACCOMODATED BY SWITCHING BANKS WITH AN I/O PORT, AS IMPLEMENTED ON THE 16K RAM. TWO SECTIONS OF C9 DECODE PORT ADDRESS 40 FROM THE LOW ORDER 8 ADDRESS LINES. COMBINING THIS WITH THE PORT STATUS SIGNAL AND $\overline{PWR}$ PROVIDES A STROBE TO A11 AND B11 TO LATCH DATA FROM THE DO BUS. THESE OUTPUTS CAN BE SELECTED BY THE BANK SELECT SWITCH TO ENABLE THE BOARD IN ANY OF 8 BANKS. IF THE SWITCH CORRESPONDING TO BIT 3 IS CLOSED, THE BOARD WILL BE ENABLED BY OUTPUTTING 08 TO PORT 40. AFTER A RESET OR POWER ON CLEAR, BIT 0 IS AUTOMATICALLY ENABLED

IN CONTRAST TO DYNAMIC RAM, A FULLY STATIC RAM SUCH AS THIS IS EXTREMELY SIMPLE. ANY OF THE INPUT SIGNALS MAY BE HELD AT ANY LOGIC STATE FOR ANY LENGTH OF TIME WITHOUT CAUSING LOSS OF DATA. THIS MEANS THAT THERE SHOULD NEVER BE ANY

COMPATIBILITY PROBLEMS FOR THE S100 BUS, AS LONG AS THE ACCESS TIME IS FAST ENOUGH FOR THE PARTICULAR PROCESSOR USED, AND EACH OF THESE BOARDS IS TESTED WITH A VECTOR GRAPHIC Z-80 CPU BOARD AT 4MHZ CLOCK FREQUENCY. THE SIMPLICITY OF THE SUPPORT CIRCUITRY MAKES TROUBLE SHOOTING VERY EASY SHOULD ANY MALFUNCTION OCCUR, MAKING THIS THE MOST DESIREABLE TYPE OF MEMORY IN TERMS OF TROUBLE-FREE OPERATION AND INTERFACING.

16K STATIC RAM

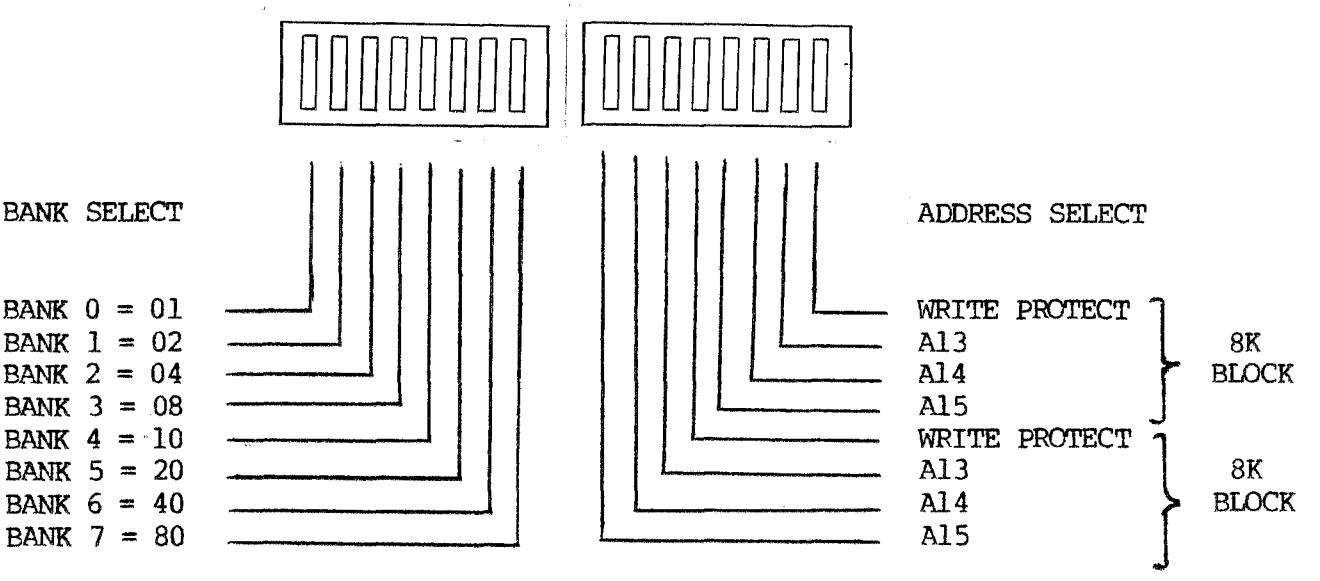
MEMORY CHIP LAYOUT



MEMORY ADDRESSES

USERS GUIDE

AT THE TOP RIGHT HAND CORNER OF THE BOARD ARE TWO SETS OF SWITCHES. THESE CONTROL THE ADDRESSING OF THE BOARD AND THE BANK SELECT FEATURE. THE LAYOUT OF THE SWITCHES IS SHOWN BELOW:



YOU WILL NOTE THAT THE SWITCHES ARE INSTALLED IN DIFFERENT DIRECTIONS. THIS IS TO MAKE THE PHYSICAL SWITCH POSITION CONFORM TO ITS LOGICAL FUNCTION; ALL SWITCHES REPRESENT LOGIC TRUE IF THEY ARE IN THE UP POSITION (THE UPPER EDGE OF THE ROCKER PUSHED IN). EACH BLOCK OF 8K CAN BE ADDRESSED INDEPENDENTLY. IF A SWITCH IS UP, THE ADDRESS LINE IT CORRESPONDS TO MUST BE HI TO SELECT THE BOARD. THUS TO SELECT ADDRESS RANGE 4000-5FFF THE A14 SWITCH WOULD BE UP AND OTHERS DOWN. THE TWO BLOCKS SHOULD NATURALLY BE ADDRESSED AT DIFFERENT LOCATIONS, BUT NO DAMAGE WILL OCCUR IF THEY ARE INADVERTENTLY SET THE SAME. THE WRITE PROTECT SWITCH PREVENTS MEMORY FROM BEING WRITTEN INTO AND COULD BE USED TO PROTECT MEMORY CONTENTS WHILE FIRST TESTING A PROGRAM. THE SWITCH SHOULD BE DOWN FOR NORMAL OPERATION. THIS FEATURE CAN NOT BE USED WITH SELF MODIFYING CODE (MITS BASIC FOR EXAMPLE) WHICH CONTINUOUSLY WRITES OVER ITSELF.

THE BANK SELECT FEATURE IS USED BY SETTING ONE OR MORE OF THE BANK SELECT SWITCHES IN THE UP POSITION. NORMALLY THE LEFTMOST SWITCH WOULD BE IN THE UP POSITION FOR BANK 0 WHICH IS AUTOMATICALLY SELECTED WHEN THE COMPUTER IS FIRST TURNED ON OR RESET (AN EXCEPTION TO THIS IS THE ALTAIR WHICH DOES NOT GENERATE A POWER ON CLEAR SIGNAL WHILE BEING RESET). OPERATION OF THIS FEATURE IS CONTROLLED BY OUTPUTTING AN 8 BIT NUMBER TO PORT 40H. IF THE NUMBER IS 04H, ALL BOARDS WITH THE BANK 2 SWITCH UP WILL BE SELECTED. OBVIOUSLY BOARDS CAN RESIDE IN MORE THAN ONE BANK AND OUTPUTTING A NUMBER TO PORT 40 WITH MORE THAN ONE BIT

HI WILL SELECT MORE THAN ONE BANK. CARE SHOULD BE EXERCISED TO ENSURE THAT ADDRESS CONFLICTS DO NO OCCUR. ONE APPLICATION OF THIS FEATURE IS IN ASSEMBLING PROGRAMS FROM EXTREMELY LARGE FILES. IT CAN ALSO BE USED TO IMPLEMENT A MULTIUSER TIME SHARING SYSTEM. EACH USER WOULD BE ASSIGNED A BANK WHICH COULD CONTAIN THE WRITE PROTECTED OPERATING SYSTEM IN REENTRANT CODE AND THE USERS FILE AREA. SOFTWARE WOULD ENABLE VARIOUS BANKS AS EACH USER ACCESSED THE COMPUTER AND IT WOULD NOT BE POSSIBLE FOR ONE USER TO ACCESS ANOTHER USER'S FILE AREA, EVEN USING THE PEEK AND POKE COMMANDS.

GENERAL TROUBLE SHOOTING GUIDE

BECAUSE OF THE COMPLEXITY OF THE ENTIRE COMPUTER SYSTEM, BOTH HARDWARE AND SOFTWARE, IT IS ESSENTIAL TO ISOLATE ANY PROBLEM TO AN INDIVIDUAL BOARD OR PROGRAM. FORTUNATELY, ALL OF THE COMPUTER LOGIC IS ON EASILY REMOVABLE BOARDS. IT IS EXTREMELY VALUABLE TO HAVE ACCESS TO A TESTED COMPUTER SO THAT THE BOARDS CAN BE INDIVIDUALLY TESTED. ALTHOUGH THERE IS THE POSSIBILITY OF INTERACTION BETWEEN BOARDS DUE TO MARGINAL TIMING OR DEFECTIVE COMPONENTS, THIS IS NOT THE USUAL CASE, AND IT IS BEST TO ASSUME THAT IF A BOARD WORKS IN COMPUTER "A" IT WILL ALSO WORK IN COMPUTER "B".

THE MINIMUM SYSTEM CONSISTS OF THREE BOARDS: THE CPU BOARD, THE PROM/RAM BOARD, AND EITHER A VIDEO OR SERIAL I/O BOARD. MAKE SURE THAT THE MONITOR PROGRAM HAS BEEN PROPERLY PATCHED FOR THE PARTICULAR I/O CONFIGURATION OF YOUR SYSTEM. THERE IS TOTAL CONFUSION IN THE INDUSTRY CONCERNING PORT ASSIGNMENTS, LOGIC CONVENTIONS, AND STRAPPING OPTIONS. SEVERAL TYPES OF PROGRAMMABLE USARTS ARE USED WHICH REQUIRE INITIALIZATION.

IF YOU HAVE CAREFULLY FOLLOWED THE ASSEMBLY INSTRUCTIONS FOR EACH OF THE BOARDS AND THE REGULATORS CHECK OUT, INSTALL ALL CHIPS. LET'S ASSUME YOU ARE USING A VIDEO DISPLAY. AS SOON AS YOU TURN THE COMPUTER ON, YOU SHOULD SEE A DISPLAY OF RANDOM MEMORY GARBAGE ON THE TV SCREEN. THIS WILL BE INDEPENDENT OF ANY FUNCTIONING OF THE COMPUTER OTHER THAN THE CLOCK OSCILLATOR. IF YOU DO NOT GET A PROPER DISPLAY, THE VIDEO INTERFACE MUST BE DEBUGGED FIRST. FEEL THE CHIPS ON THE BOARD. ANY THAT ARE HOT TO THE TOUCH MAY BE IN BACKWARD (PROBABLY DESTROYED IF TTL) OR MAY HAVE THEIR OUTPUTS SHORTED. THERE IS MORE THAN A FACTOR OF TEN DIFFERENCE IN THE POWER DISSIPATION OF TTL CHIPS, BUT THEY SHOULD NOT BE UNCOMFORTABLY HOT TO THE TOUCH.

REMOVE THE BOARD AND INSPECT IT CAREFULLY. ABOUT HALF OF THE PROBLEMS CAN BE FOUND SIMPLY BY VISUAL INSPECTION. LOOK WITH A MAGNIFYING GLASS OR INSPECTION SCOPE AT EACH PIN ON THE BOTTOM FOR UNSOLDERED PINS, MISSING PINS THAT MAY BE BENT UNDER OR BROKEN OFF, SOLDER BRIDGES BETWEEN PINS OR TO ADJACENT TRACES, AND ETCH BRIDGES BETWEEN TRACES (VERY HARD TO SEE). A CAREFUL EXAMINATION WILL TAKE 15 MINUTES, BUT MAY SAVE YOU A LOT OF GRIEF, AND YOU MAY DISCOVER PROBLEMS LIKE UNSOLDERED PINS THAT MAY REVEAL THEMSELVES ONLY LATER AS INTERMITTENT PROBLEMS. EXAMINE THE TOP OF THE BOARD TO BE SURE THE PROPER CHIPS ARE INSTALLED IN THE RIGHT PLACES. SIGHT ALONG THE EDGE OF THE CHIPS TO FIND BENT UNDER PINS. CHIPS ARE SOMETIMES INSERTED WITH A WHOLE ROW OF PINS THAT MISS THE SOCKET HOLES.

IF THE VISUAL INSPECTION FAILS TO GET THE VIDEO DISPLAY WORKING, A COMPONENT MAY BE BAD (USUALLY AN IC). TRY EXCHANGING IDENTICAL COMPONENTS TO SEE IF THE SYMPTOMS CHANGE. AT THIS POINT IT IS WISE TO GO BACK AND CAREFULLY REREAD THE MANUAL TO BE SURE YOU UNDERSTAND THE WAY THE BOARD WORKS AND THAT YOU HAVE SELECTED THE PROPER JUMPER OPTIONS. AFTER THIS, YOU WILL PROBABLY WANT TO TAKE THE UNIT TO A DEALER IF YOU ARE NOT FAMILIAR WITH DIGITAL TROUBLE SHOOTING PROCEDURES, OR GO THROUGH THE CIRCUIT BLOCK BY BLOCK WITH A SCOPE OR LOGIC PROBE IF YOU ARE EXPERIENCED.

AFTER THE VIDEO DISPLAY OR SERIAL I/O IS WORKING, THE RESET SWITCH SHOULD CAUSE

A "*" PROMPT TO BE WRITTEN. IF THIS DOES NOT WORK, FOLLOW THE SAME PROCEDURE ON THE CPU AND PROM/RAM BOARDS. THE CPU BOARD CONSISTS MOSTLY OF 8097 BUS DRIVERS WHICH CAN BE EXCHANGED ONE BY ONE. THE VECTORED INTERRUPT AND REAL TIME CLOCK COMPONENTS, IC A1, ARE NOT NECESSARY IN THE BOARD AT THIS TIME AND SHOULD BE REMOVED. USING A SCOPE, EXAMINE THE OUTPUT PINS OF ALL CHIPS. LOW LOGIC LEVELS ARE NORMALLY LESS THAN 0.2 VOLTS AND HIGH GREATER THAN 3.0 VOLTS. A LEVEL OF 0.4 VOLTS MAY INDICATE SHORTS BETWEEN OUTPUTS WHERE ONE IS TRYING TO PULL HIGH AND THE OTHER LOW. A LEVEL OF 1.2 VOLTS INDICATES AN OPEN CIRCUITED INPUT. NMOS CHIPS HAVE SIMILAR LOGIC LEVELS, WHILE PMOS CHIPS CAN PULL TTL INPUTS TO -0.6V WHERE THE INPUT CLAMP DIODE LIMITS THE VOLTAGE. DO NOT BE SURPRISED AT HOW STRANGE SOME OF THE WAVEFORMS ON THE BUS LOOK, SUCH AS THE DI LINES. THERE ARE PERIODS OF TIME DURING WHICH THE BUS IS NOT BEING ACTIVELY DRIVEN, AND THE VOLTAGE MAY DRIFT DUE TO RECEIVER INPUT CURRENT. ABNORMAL OPERATION IS INDICATED PRINCIPALLY BY ABNORMAL LOGIC LEVELS MAINTAINED CONSTANT FOR AT LEAST ONE CLOCK PERIOD (500 MICROSECONDS).

ONCE YOUR BASIC SYSTEM IS WORKING, CHECK OUT OF MEMORY BOARDS AND OTHER INTERFACES IS RELATIVELY STRAIGHTFORWARD USING THE MEMORY TEST PROGRAM IN THE MONITOR, OR SIMPLE DIAGNOSTIC ROUTINES YOU CAN PROGRAM IN MEMORY ON THE PROM/RAM BOARD. AFTER YOUR SYSTEM IS UP AND RUNNING, IT SHOULD BE QUITE RELIABLE. SINCE MOST MICROCOMPUTER SYSTEMS ARE MEMORY INTENSIVE, THE MEMORY IS THE MOST LIKELY SOURCE OF COMPONENT FAILURE. A SYSTEM WITH 32K OF STATIC MEMORY MAY CONTAIN 75% OF ITS COMPONETS ON THE MEMORY BOARDS. IF A PROBLEM IS EXPERIENCED RUNNING A PROGRAM, FIRST SUSPECT THE MEMORY AND USE THE MONITOR TEST PROGRAM. WE HAVE YET TO EXPERIENCE A PROBLEM WITH OUR 8K MEMORY BOARDS THAT WAS NOT REVEALED BY THE TEST PROGRAM. IF YOU DO MUCH REARRANGING OF YOUR SYSTEM, IT IS A GOOD PRACTICE TO TEST MEMORY FOR A FEW SECONDS WHEN YOU FIRST TURN ON THE COMPUTER TO MAKE SURE THE BOARDS ARE ADDRESSED PROPERLY OR THAT THEY ARE IN THE COMPUTER. THIS MAY SAVE SOME HEAD SCRATCHING WHEN THE PROGRAM YOU HAVE JUST LOADED FAILS TO RESPOND TO YOUR EAGER KEYBOARD TOUCH. IF YOU SUSPECT TEMPERATURE SENSITIVE CHIPS, REMOVE THE COVER OF THE COMPUTER TO INTERRUPT AIR FLOW BETWEEN BOARDS. WE DO NOT RECOMMEND OBSTRUCTING THE AIR FLOW THROUGH THE COMPUTER BY PLACING A SHEET OF PAPER OVER THE LEFT SIDE. A FULL COMPUTER MAY DISSIPATE OVER 300 WATTS AND REACH UNACCEPTABLE TEMPERATURES IF NO AIRFLOW IS PERMITTED.

SPECIFICATIONS

16K FULLY STATIC RAM MODULE (S-100 BUS)

BANK SELECT, 8K BLOCK INDEPENDENT ADDRESSING, WRITE PROTECT, HIGH SPEED, FULLY ASSEMBLED, TESTED, BURNED-IN GUARANTEED 1 YEAR.

SPECIFICATIONS:

CAPACITY:	16,384 BYTES
BUFFERING:	A) SCHMITT TRIGGERS ON ALL ADDRESSES AND CONTROL INPUTS FOR IMPROVED NOISE MARGIN. B) DATA INPUT AND OUTPUT BUFFERED
ACCESS TIME:	COMPATIBLE WITH Z-80 AT 4MHZ - NO WAIT STATES
DMA:	NO RESTRICTIONS
POWER CONSUMPTION:	2.0A AT 8.0 VDC (TYPICAL) REGULATORS CONSERVATIVELY HEAT SUNK.
WRITE PROTECT:	HARDWARE, EACH 8K BLOCK
BANK SELECT:	MAY BE LOCATED IN ANY ONE OR MORE OF EIGHT "BANKS" BY MEANS OF SWITCHES ON THE MODULE. BANKS MAY BE SELECTED BY SOFTWARE.
PHANTOM:	OUTPUT BUFFER DISABLE COMPATIBLE WITH VECTOR GRAPHIC RESET AND GO BOARD, (SOL PHANTOM).
GROUND PLANE:	FEATURES A GRIDDED GROUND PLANE DESIGN FOR REDUCED NOISE.