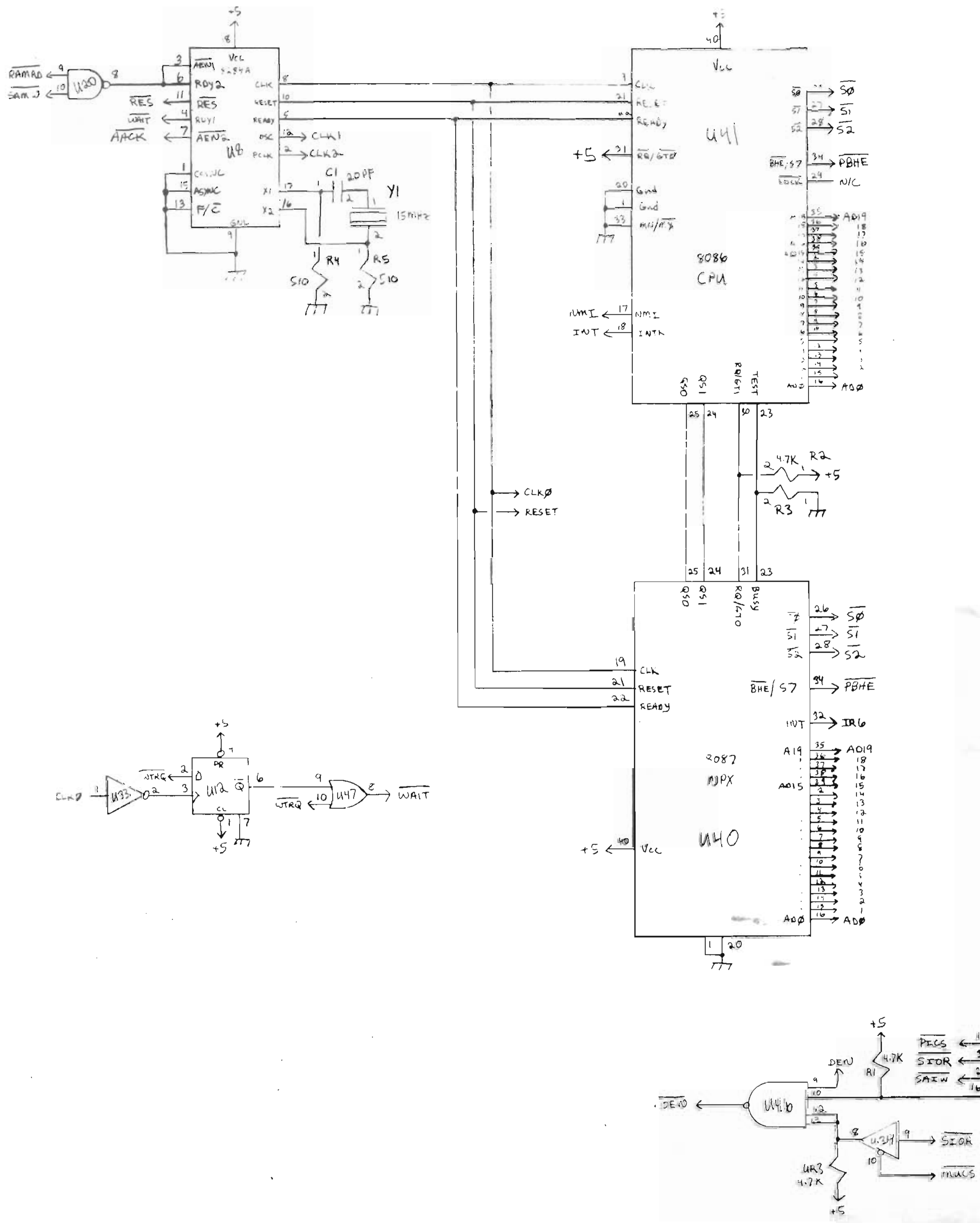
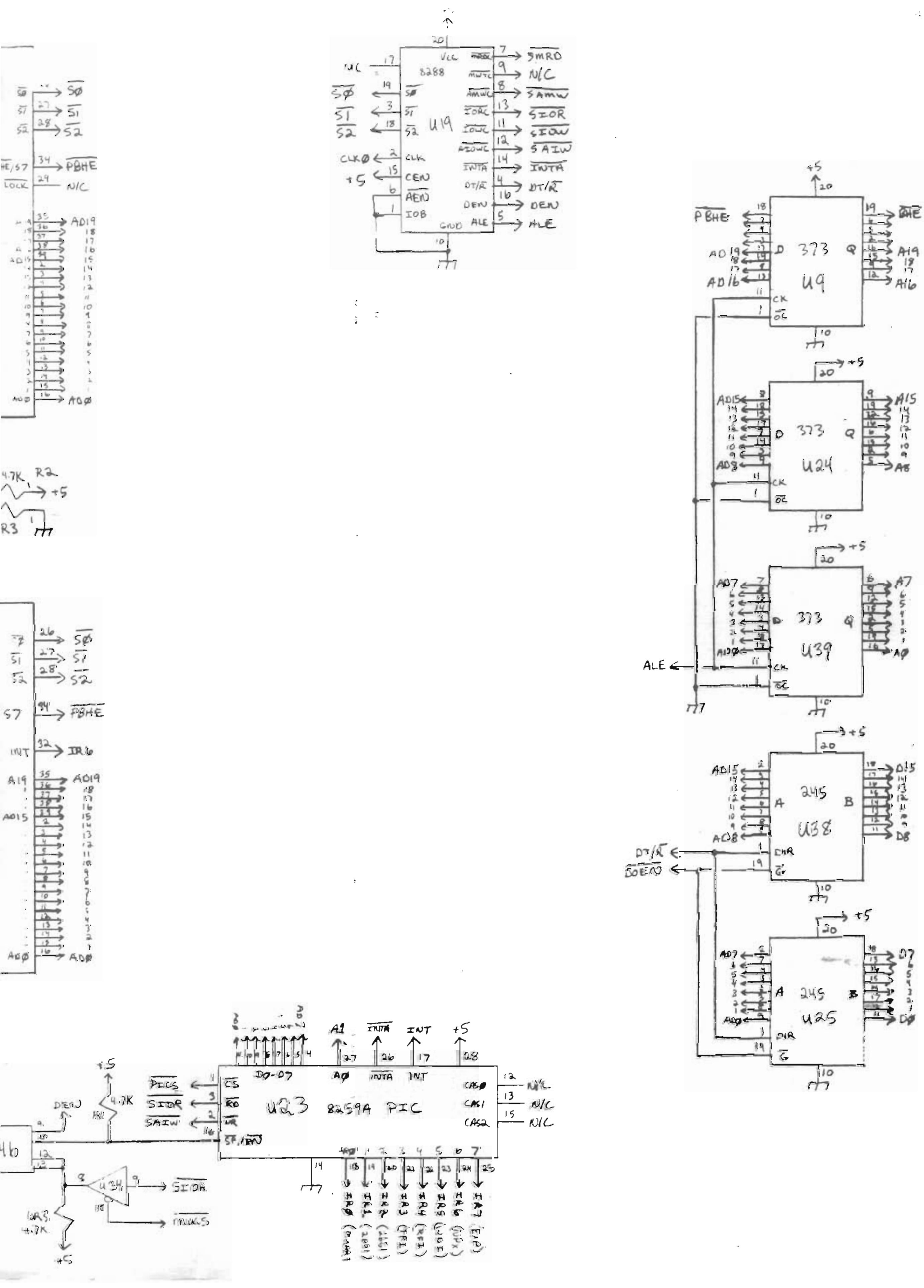
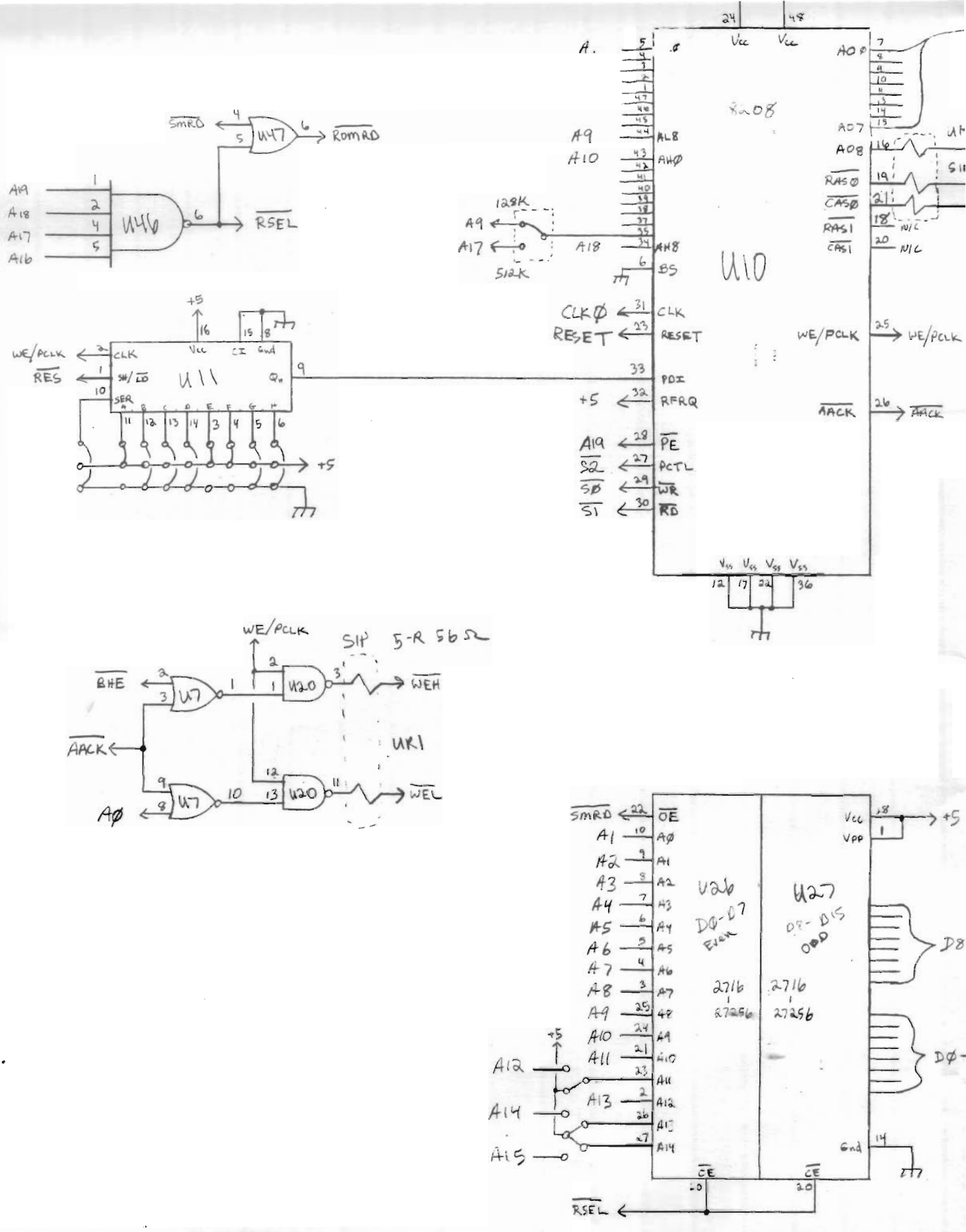
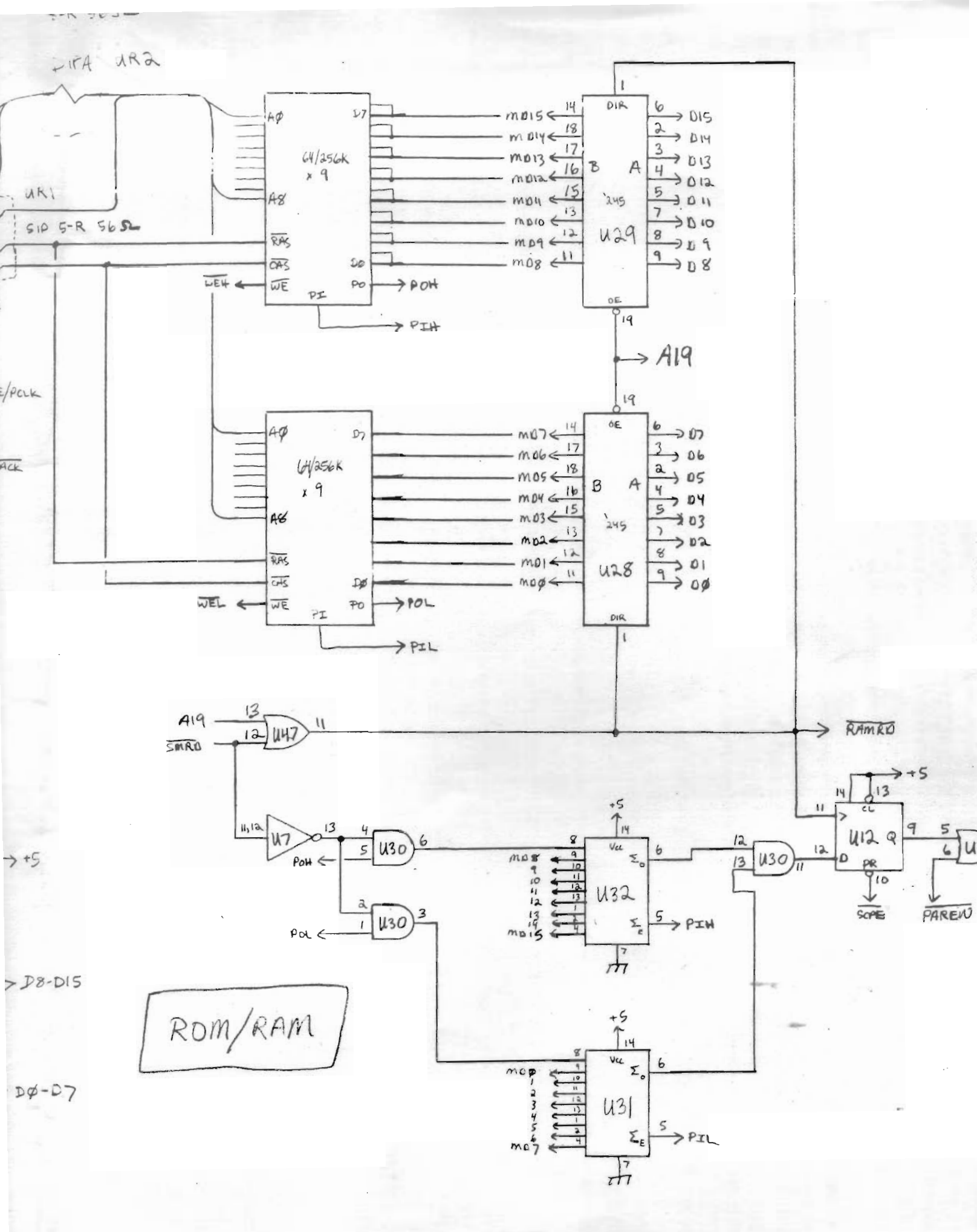
CPU/MPX/PIC



RAMRD
SAMJ
U20
RES
WAIT
AACK
8284A
U8
Vcc
RDY2
AEN2
CSYNC
ASYNC
F/C
GND
CLK
RESET
READY
OSC
PCLK
X1
X2
CLK1
CLK2
C1
20PF
Y1
15MHz
R4
R5
510
U41
8086
CPU
RQ/GT0
Gnd
MN/MX
NMI
INTR
S0
S1
S2
BHE/S7
PBHE
LOCK
N/C
AD19
AD0
QS0
QS1
RQ/GT1
TEST
4.7K
R2
R3
+5
CLK0
RESET
BUSY
RQ/GT0
INT
IR6
A19
AD15
8087
MPX
U40
Vcc
U33
U12
WTRQ
PR
CL
U47
WAIT
U46
DEN
R1
4.7K
PICS
SIOR
SAIW
U34
U83
MMCS


8288
U19
Vcc
S̄MRD
N/C
S̄AMW
S̄IOR
S̄IOW
S̄AIW
ĪNTA
DT/R̄
DEN
ALE
CLKØ
+5
CEN
AEN
IOB
GND
S̄Ø
S̄1
S̄2
PBHE
AD19
AD15
ADØ
4.7K R2
R3
IR6
373
U9
U24
U39
AD16
A19
A16
AD8
A15
A8
AD7
A7
ADØ
AØ
CK
ŌC
245
U38
U25
DIR
G̅
D15
D8
D7
DØ
DT/R̄
SDEN
U23
8259A PIC
DØ-D7
CS
RD
WR
SP/EN
CASØ
CAS1
CAS2
N/C
PICS
SIOR
SAIW
INTA
INT
A1
DIEN
U34
IRØ
IR1
IR2
IR3
IR4
IR5
IR6
IR7


A.
8208
U10
U11
U46
U47
U20
U26
U27
SMRD
ROMRD
RSEL
A19
A18
A17
A16
A10
A9
A8
128K
512K
CLKØ
RESET
WE/PCLK
RES
PDI
RFRQ
AACK
PE
PCTL
WR
RD
S2
SØ
S1
AØ
A1
A2
A3
A4
A5
A6
A7
A11
A12
A13
A14
A15
BHE
WEH
WEL
AACK
SMRD
OE
CE
Vcc
Vpp
Gnd
Vss
+5
D8
DØ
2716
27256
DØ-D7
EVEN
D8-D15
ODD
WE/PCLK
5-R 562

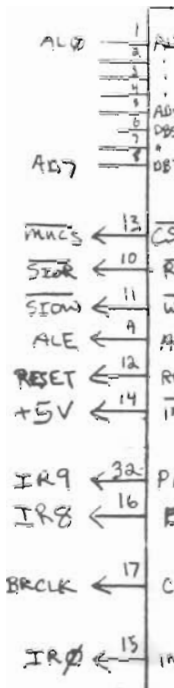

UR1
SIP 5-R 56Ω
64/256K x 9
U29
U28
'245
DIR
OE
A19
WEH
WEL
PIH
PIL
POH
POL
RAMRD
SMRD
U47
U30
U32
U31
U12
SCAS
PARE
+5
ROM/RAM
D8-D15
D0-D7

J4

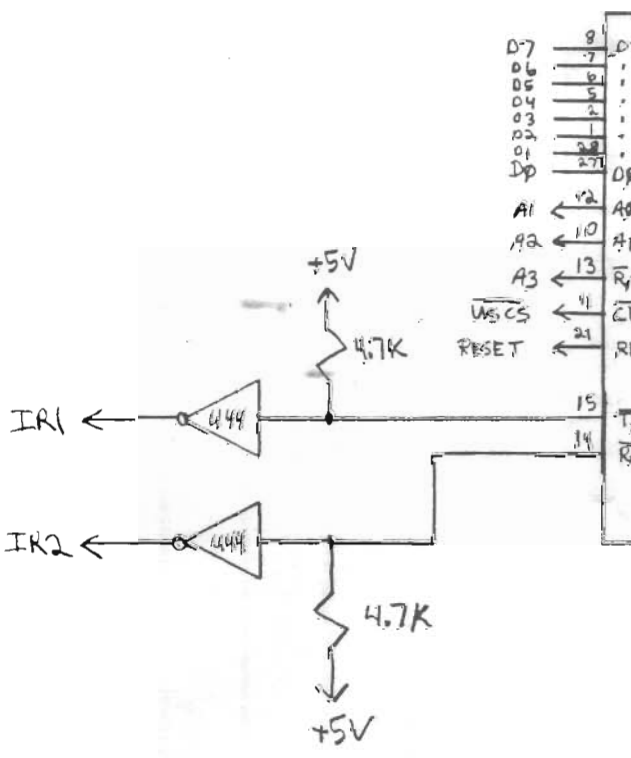
Expansion Bus

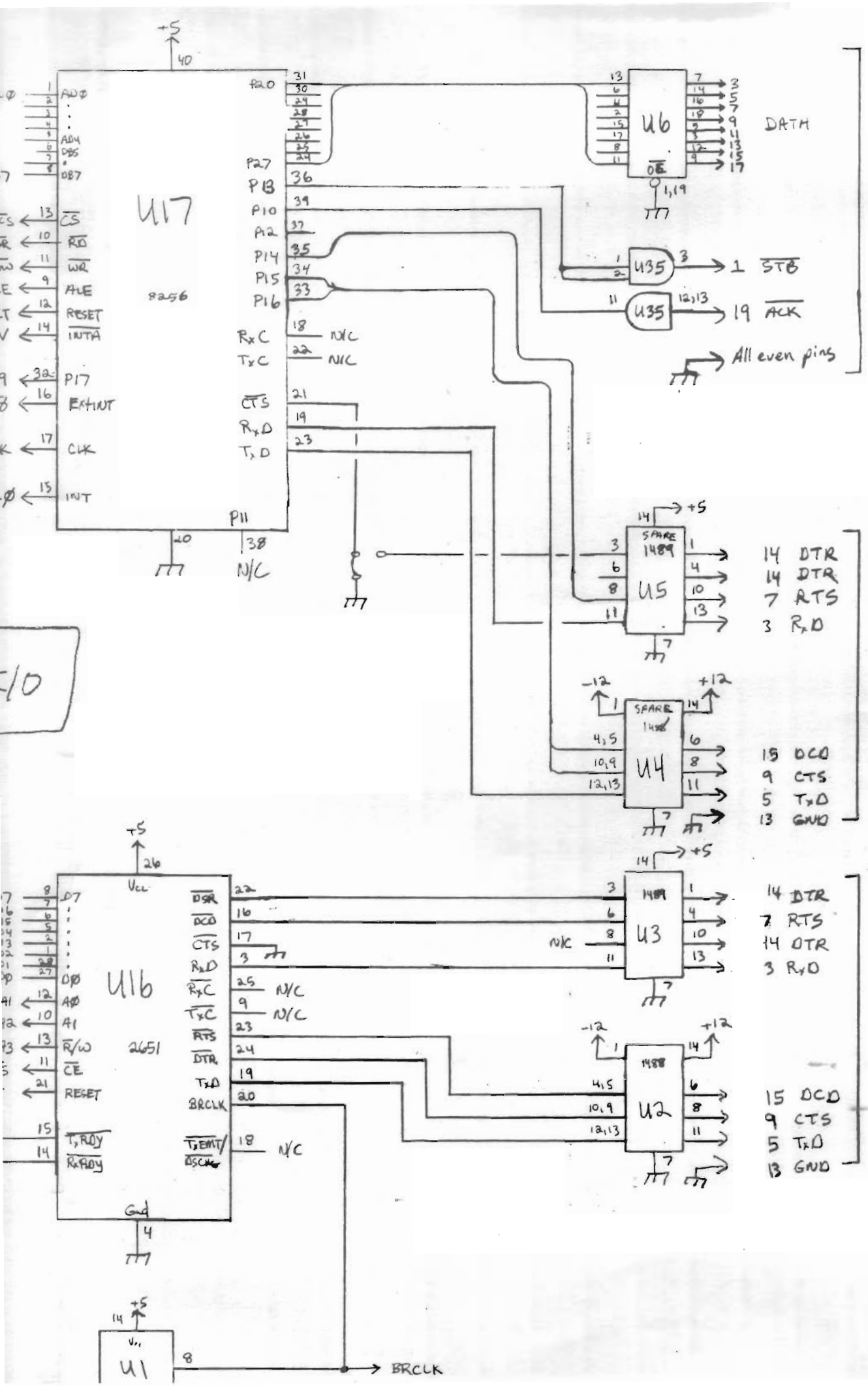
50 pin header

J4, P1	D0
3	D1
5	D2
7	D3
9	D4
11	D5
13	D6
15	D7
17	D8
19	D9
21	D10
23	D11
25	D12
27	D13
29	D14
31	D15
33	CLK2
35	$\overline{SMRD}$
37	$\overline{SAMW}$
39	$\overline{SIOR}$
41	$\overline{SAIW}$
43	IR7
45	IR8
47	IR9
49	CLK0
2	A0
4	A1
6	A2
8	A3
10	A4
12	A5
14	A6
16	A7
18	A8
20	A9
22	A10
24	A11
26	A12
28	A13
30	A14
32	A15
34	A16
36	A17
38	A18
40	A19
42	CLK1
44	$\overline{BHE}$
46	ALE
48	NC
J4, P50	RESET



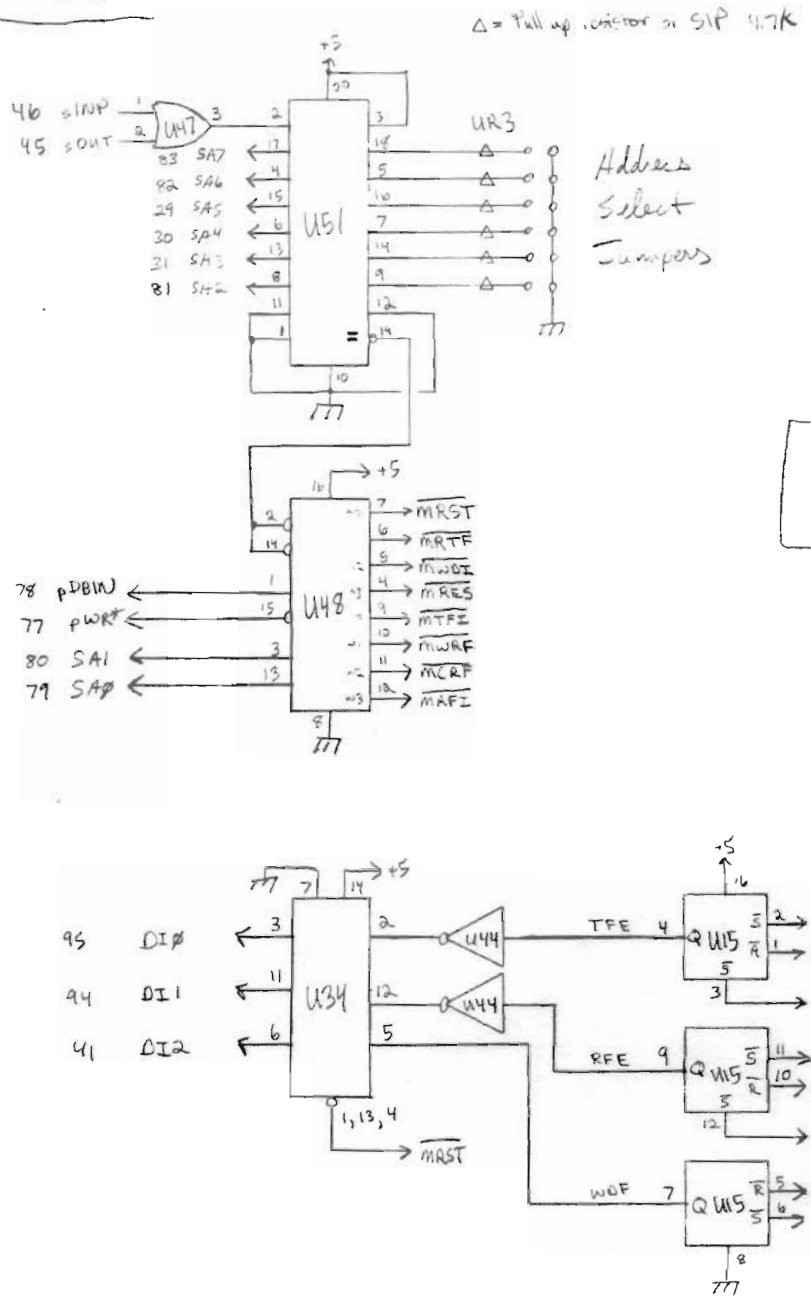
Serial / Parallel I/O



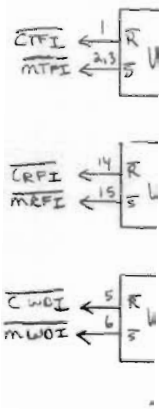

U17
8256
U6
DATA
J3
Centronics Port
20 pin header
U35
1 STB
19 ACK
All even pins
U5
1489
14 DTR
14 DTR
7 RTS
3 RxD
J2 - 16 pin
Serial Po
U4
1488
15 DCD
9 CTS
5 TxD
13 GND
U16
2651
U3
1489
14 DTR
7 RTS
14 DTR
3 RxD
J1 - 16
Serial
U2
1488
15 DCD
9 CTS
5 TxD
13 GND
U1
BRCLK

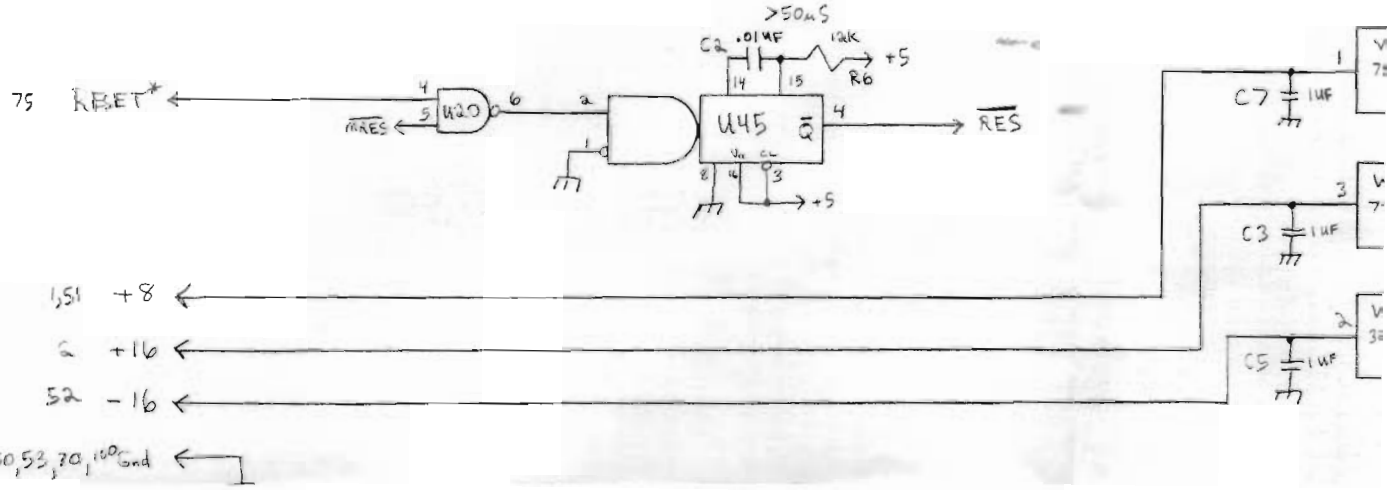
P1

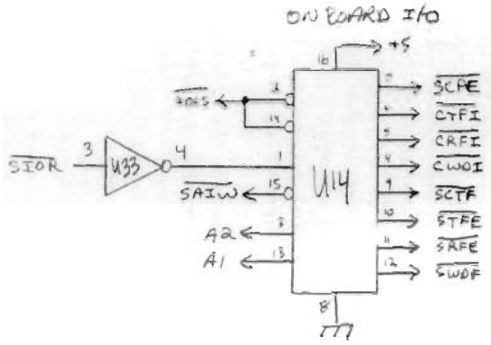
S100 BUS



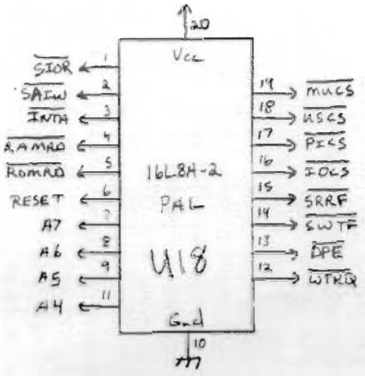
S100 Decode/Control/Status

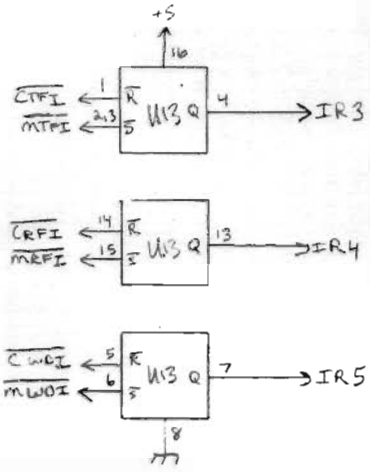


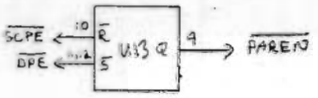


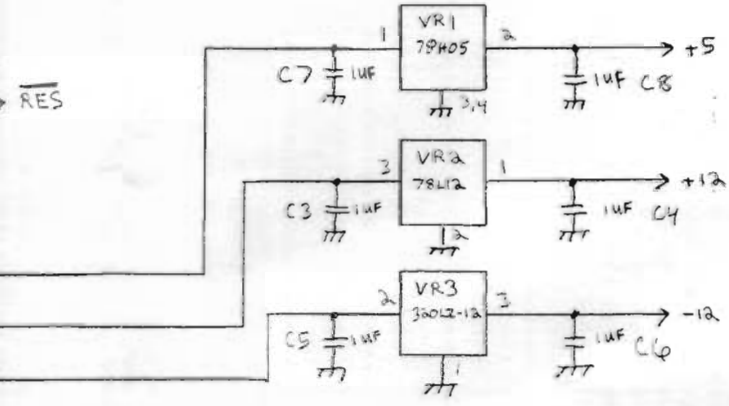


Decode/Control/Status



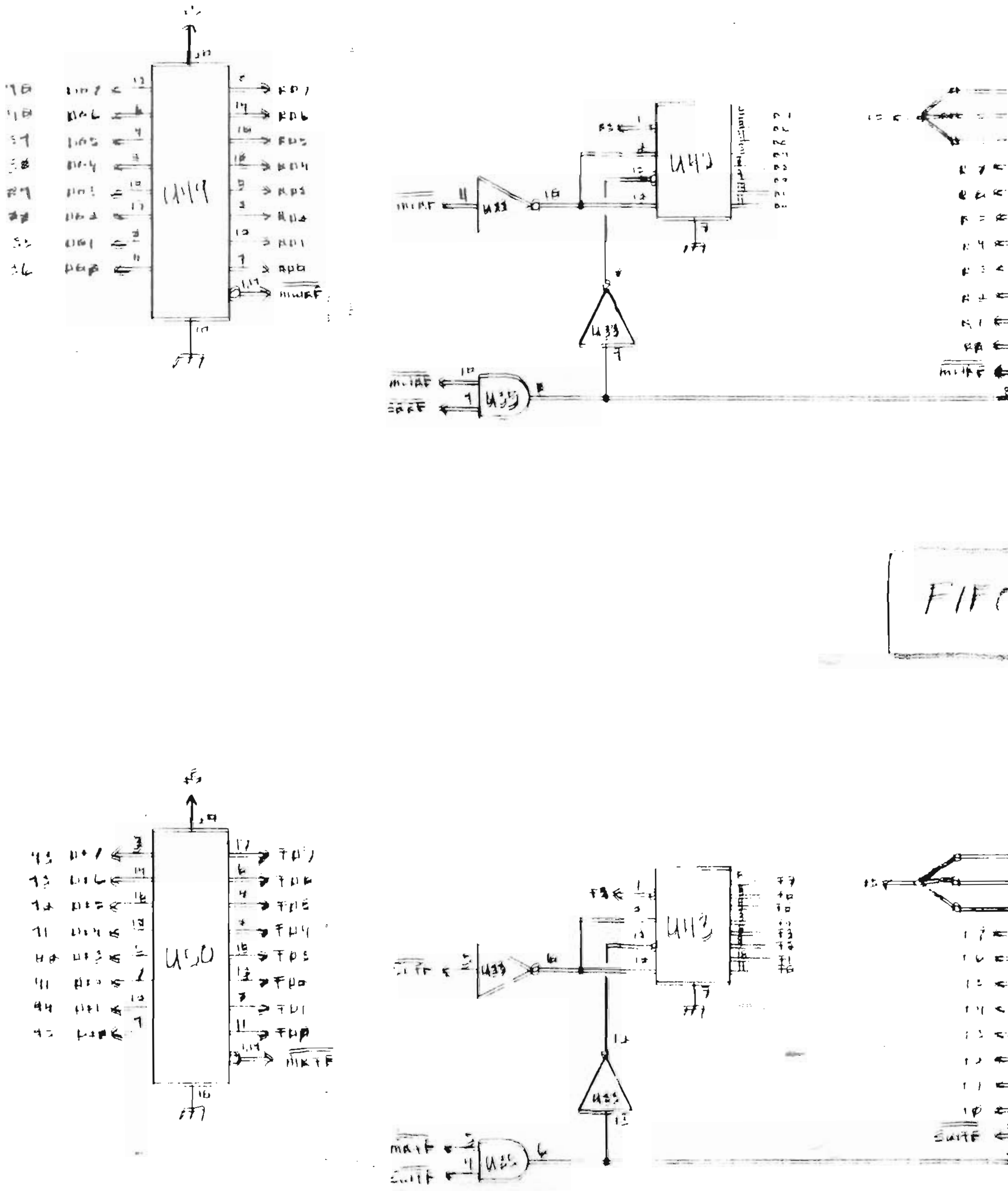


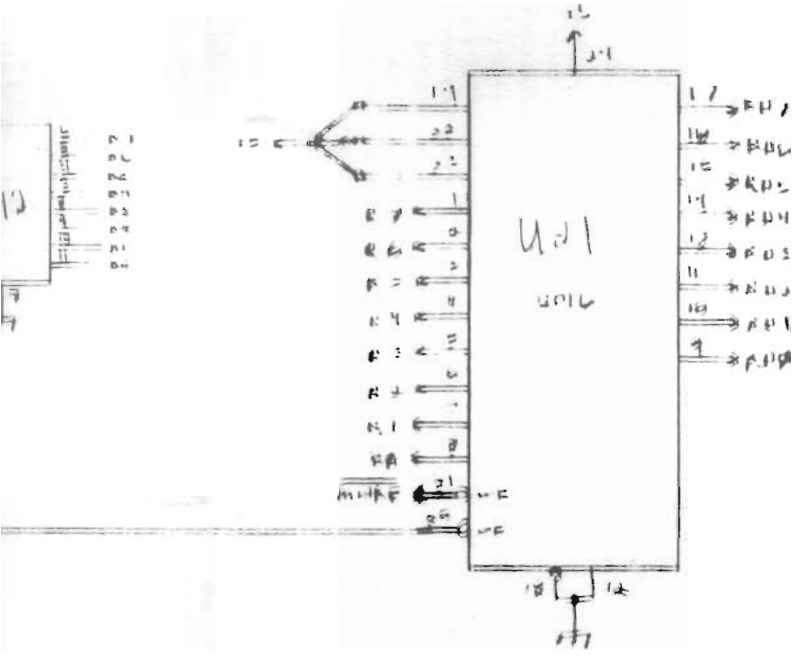


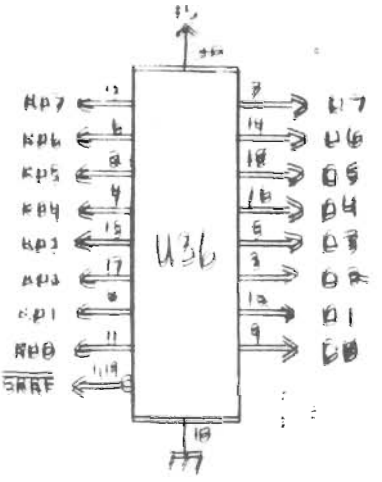


11

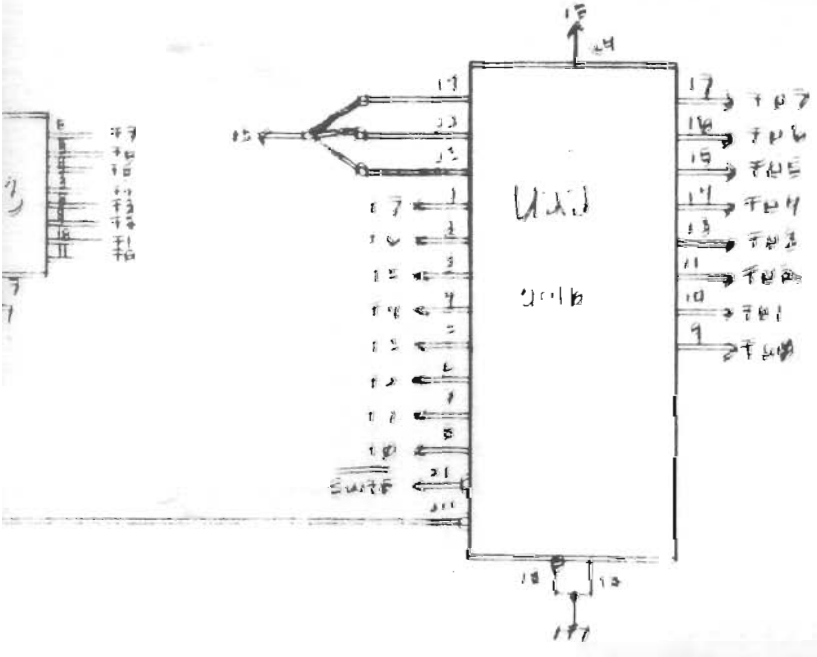
S-100 BUS

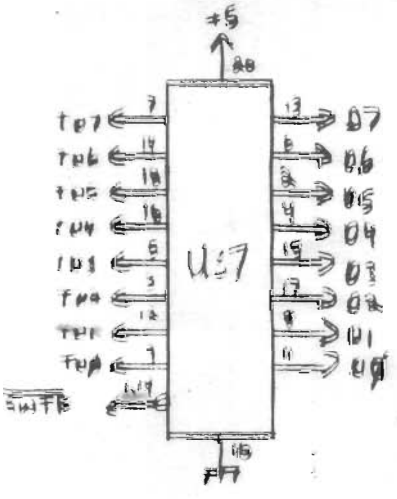


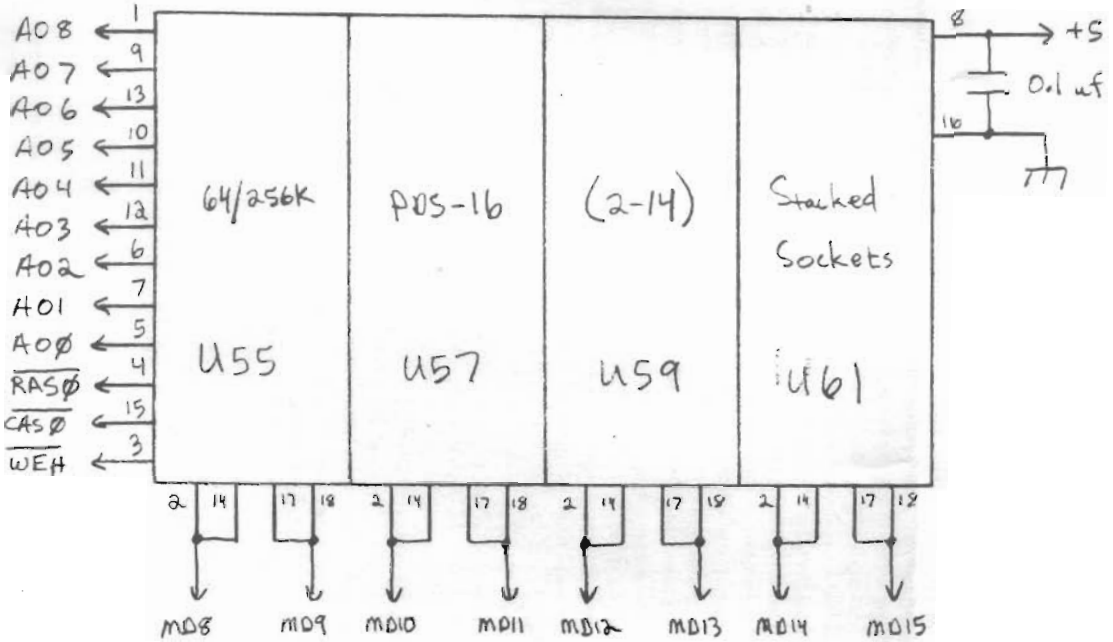




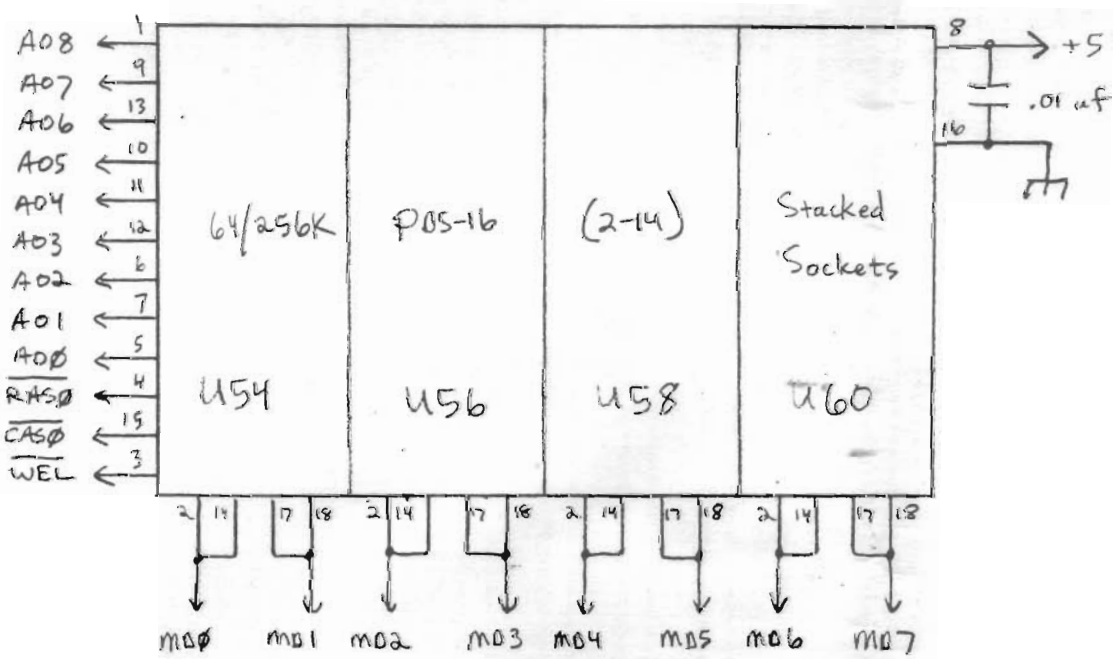
FIFO Circuit

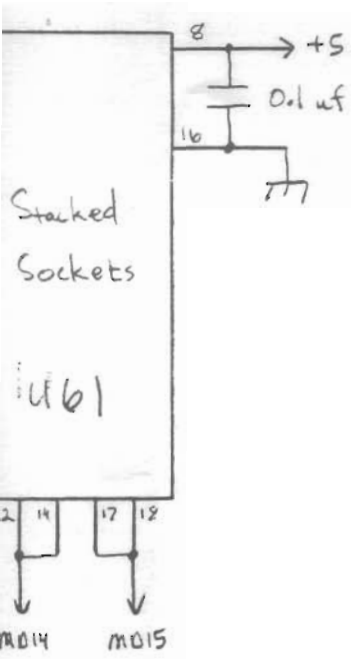


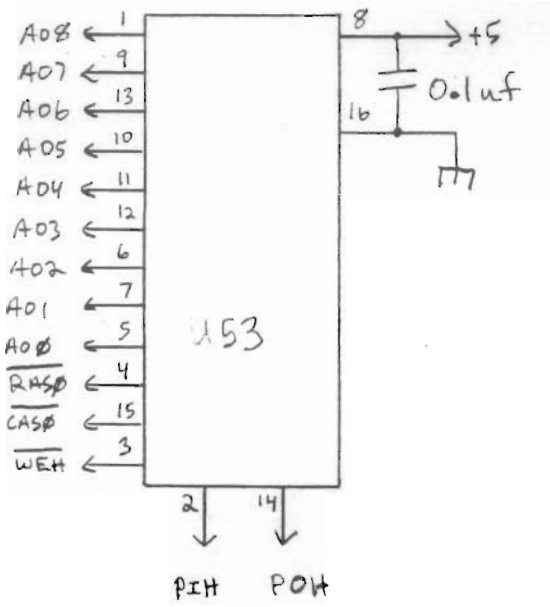



A08
A07
A06
A05
A04
A03
A02
A01
A0Ø
RASØ
CASØ
WEH
64/256K
POS-16
(2-14)
Stacked Sockets
U55
U57
U59
U61
+5
0.1 uf
MD8
MD9
MD10
MD11
MD12
MD13
MD14
MD15

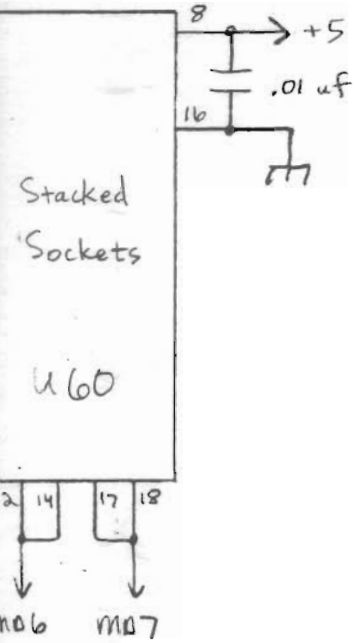
RAM Array

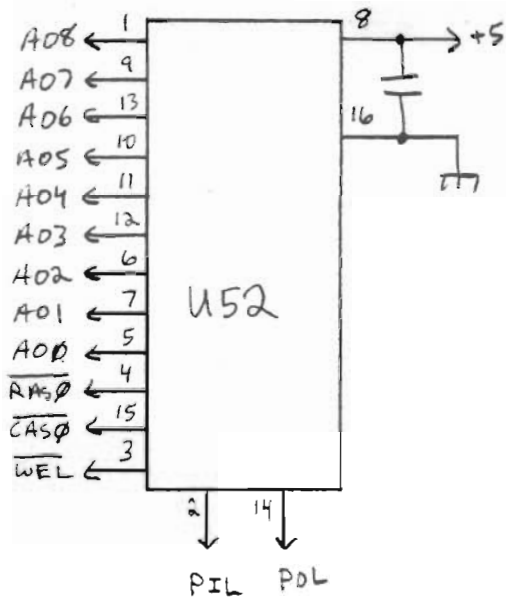

A08
A07
A06
A05
A04
A03
A02
A01
A0Ø
RASØ
CASØ
WEL
64/256K
POS-16
(2-14)
Stacked Sockets
U54
U56
U58
U60
+5
.01 uf
MDØ
MD1
MD2
MD3
MD4
MD5
MD6
MD7

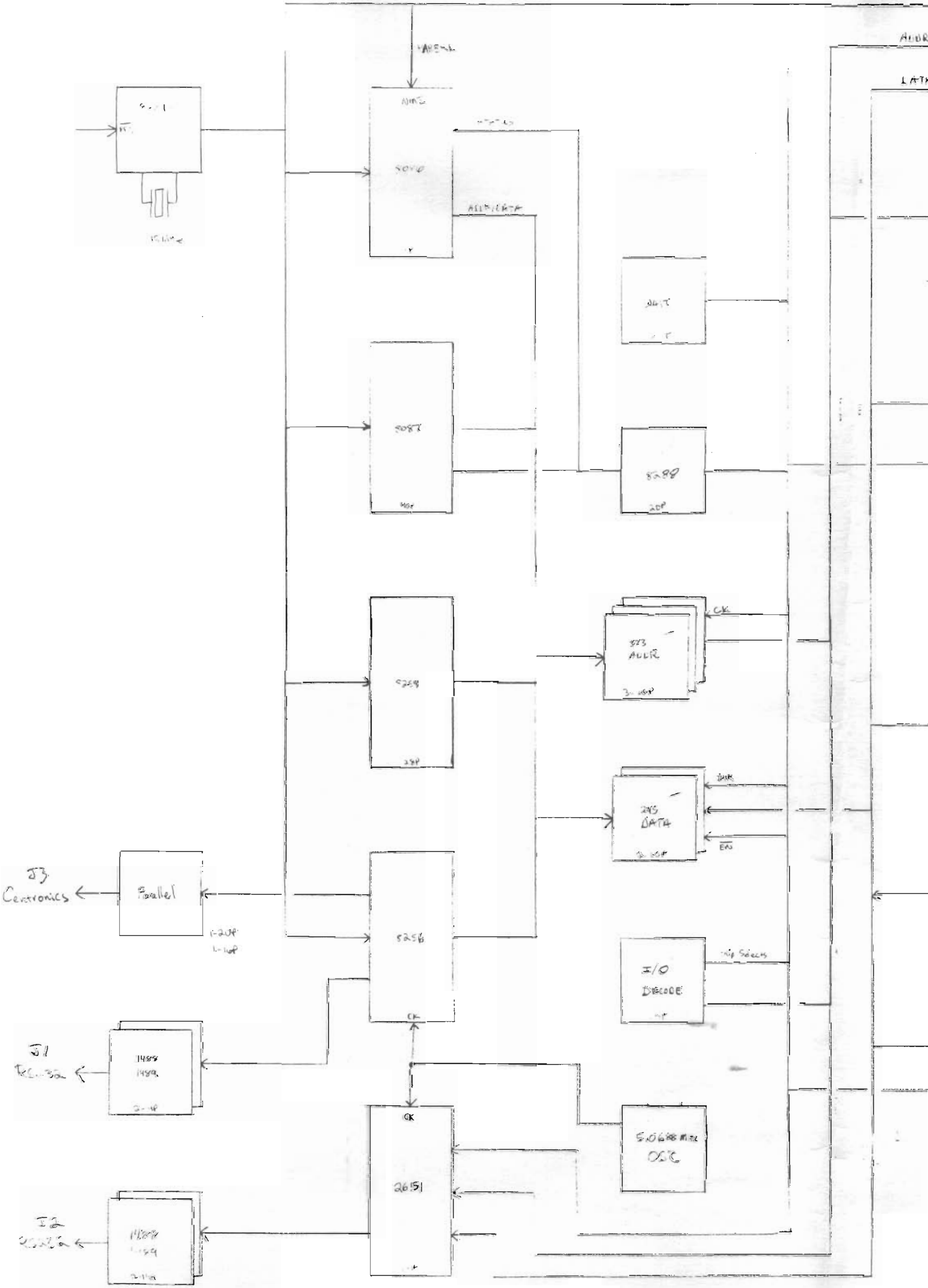

8
+5
0.1 uf
16
Stacked
Sockets
U61
2
14
17
18
MD14
MD15


A08
A07
A06
A05
A04
A03
A02
A01
A0Ø
RASØ
CASØ
WEH
1
9
13
10
11
12
6
7
5
4
15
3
U53
8
+5
0.1 uf
16
2
14
PIH
POH

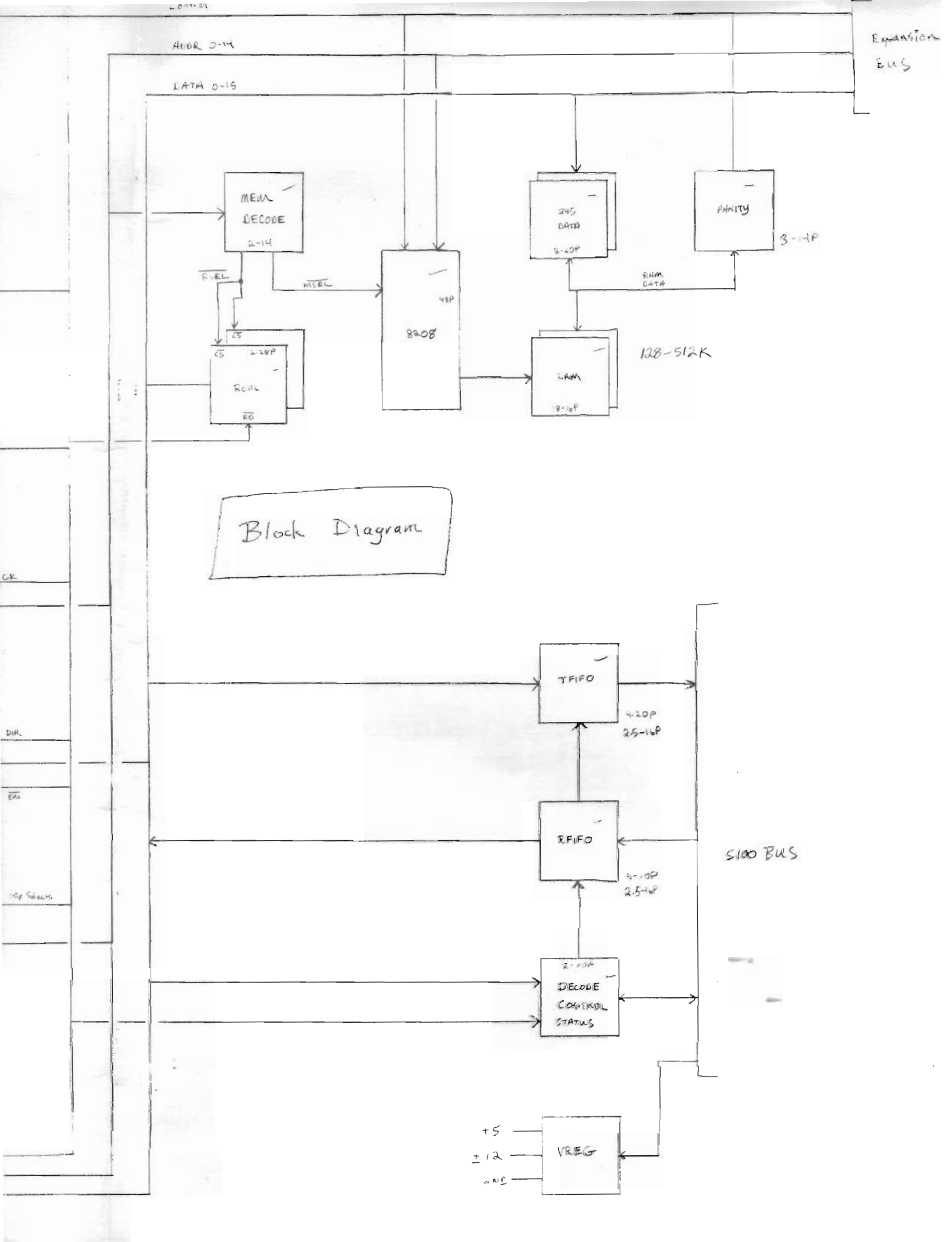
y


8
+5
.01 uf
16
Stacked
Sockets
U60
2
14
17
18
MD6
MD7


A08
A07
A06
A05
A04
A03
A02
A01
A0Ø
RASØ
CASØ
WEL
1
9
13
10
11
12
6
7
5
4
15
3
U52
8
+5
16
2
14
PIL
POL



8288
20P
373
ADDR
CK
245
DATA
DIR
EN
I/O
DECODE
Chip Selects
J3
Centronics
Parallel
1-20P
1-16P
8256
CK
J1
1488
1489
5.0688 MHz
OSC
CK
2651
J2


ADDR 0-19
DATA 0-15
EXPANSION BUS
MEM DECODE
2-14
245 DATA
2-20P
PARITY
3-14P
RSEL
MSEL
48P
8208
RAM DATA
128-512K
2-28P
ROM
RAM
18-16P
Block Diagram
TFIFO
4-20P
2.5-16P
RFIFO
4-20P
2.5-16P
S100 BUS
DECODE CONTROL STATUS
+5
±12
GND
VREG