SBC-I MANUAL

Revision 1

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I. PRODUCT DESCRIPTION

1.1 SYSTEM OVERVIEW

The SBC-I is a slave S-100 board designed for a multiprocessing system and will provide a CPU, I/O, and 128k of memory for each user. A system processor is also needed in order to supervise system level functions. Because each user has a CPU dedicated to his application, his program will execute almost as fast as if he were the only user of the system. Communication with the main system processor occurs via a 1k-byte FIFO on board, with data transfers across the S-100 bus. Since the SBC-I occupies only four I/O ports on the bus there is great potential for system expansion using this system architecture.

The SBC-I board does not have to be used in an S-100 system. The board is designed to be utilized as a stand alone slave processor that will support one user. The communication to the master processor can be achieved on a RS-232 or RS-422 link. This would allow the installation of the SBC-I in a remote dumb terminal with nothing more than power connections required.

1.2 FEATURES

Memory

The 128k byte RAM incorporating memory management provides the space and flexibility required by the increasingly complex software being used in high performance systems. In addition to RAM, one EPROM on board provides an initialization program to set up the LSI IC's on board. After the routines have completed their function the EPROM can be disabled by software. The RAM is composed of 64k-bit RAM IC's to reduce the physical size of the array.

Bank-select controls the access to the EPROM, and a memory management circuit controls access to the RAM. The EPROM, which occupies 000H to 0FFFH, can be disabled after it initializes the SBC-I. A 2716, a 2732, or a 2764 may be used in the EPROM socket. The RAM is partitioned by setting up a bipolar RAM which provides the ability to enable any 4k segment of RAM and address it at any 4k boundary of the CPU address space. Thus a fixed RAM for the operating system can be established, and several programs may be loaded into the remaining RAM which can subsequently be brought into the CPU address space by appropriate operations on the memory management.

Serial Ports

A Z-80A SIO provides two independent serial ports. Both ports are RS-232C compatible and can operate at software-selectable speeds via two channels of a Z-80A CTC. In addition, provision is made to allow a synchronous MODEM to be connected to SIO A. (A synchronous MODEM supplies both the receive and transmit clocks for the serial ports.) The baud-rate clock is supplied by a 2.4576 MHz packaged oscillator.

Parallel Ports

A Z-80A PIO provides a bidirectional parallel port via its "A" port, and control lines from its "B" port. These lines run to connectors providing an interface to parallel devices. Some of the "B" lines are used for on-board functions.

Reset

Both the user and the main system are able to reset the SBC-I. However, the user reset will reset only his SBC-I, while the main system reset will reset all SBC-I's. A monostable provides a 100uSec reset pulse regardless of the length of time the user enables the reset button. This is to prevent the loss of the dynamic RAM data during reset. In addition, a software reset is implemented which will allow the master CPU in the system to reset the SBC-I in the system. This allows the master CPU to "wake up" an SBC-I that doesn't respond to an inquiry. In this manner a user need never have to reset his module in the event of software bugs; the master CPU will keep it running.

SBC-I is a Slave

The SBC-I cannot function as the main processor of the system. It is dedicated to its user. Only the FIFO on-board communicates with the system, which must have a master processor overseeing the system functions.

Communication with the Master CPU

Communication with the Master CPU in the system occurs via a 1k byte FIFO (First-In, First-Out) memory which provides a means for passing messages and blocks of data between the SBC-I and the Bus Master.

S-100 Compatibility

Only those operations required for the FIFO are IEEE-696 (S-100) compatible, because access by any other means (memory or DMA) is not implemented. Thus, the SBC-I appears only as an I/O port-accessed device to the master CPU. For the I/O operations, the SBC-I is completely IEEE-696 (S-100) compatible.

II. SPECIFICATIONS

Central processor:
Z80A, Z80B CPU - 2, 4 or 6 MHz operation.

Memory:
64kbytes RAM, optionally 128kbytes. Uses 200nsec HM4864-3 dynamic RAM at 4 MHz. Memory management circuit allowing 4kbyte segmentation. 128 cycle refresh devices required.

Serial:
Z80A SIO - 2 RS-232C ports, independent operation. Speeds from 110 to 19200 baud.

Parallel:
Z80A PIO - 1 bidirectional port with 4 handshake lines, 4 independent input or output lines. RS-422 adapter available.

EPROM:
2716, 2732, or 2764 device may be used (2716 is standard).

FIFO:
1kbyte 4801 or 2kbyte 2016 may be used (2016 is standard).

S-100 Bus Signals:

A0-A7	sINP	INT*
D00-D07	sOUT	+8V
DI0-DI7	sINTA	+16V
RESET*	pWR*	-16V
POC*	pDBIN	GND

Dimensions:
5.125" x 10.00", excluding edge connector

Workmanship conforms to the requirements of MIL-STD-454.

Forced air cooling is required.

III. INSTALLATION

Upon receipt of SBC-I, check the shipping package for signs of abuse which may indicate possible damage. Check the board physically to look for any parts which may have been damaged during shipping. If any diskettes were shipped with SBC-I, check the diskettes for signs of damage which might be any bending or signs of a sharp object placed against the diskettes. Diskettes are quite fragile and any warping of the surface of the diskette will render it inoperative. Notify Teletek of any discrepancies and call the shipping company if there is shipping damage.

SBC-I is ready for immediate use upon receipt. It requires only that the peripherals which will be used with it be connected to the appropriate connectors along the top of the board. For the particular connections required, see the adjoining section entitled "Peripheral Connections".

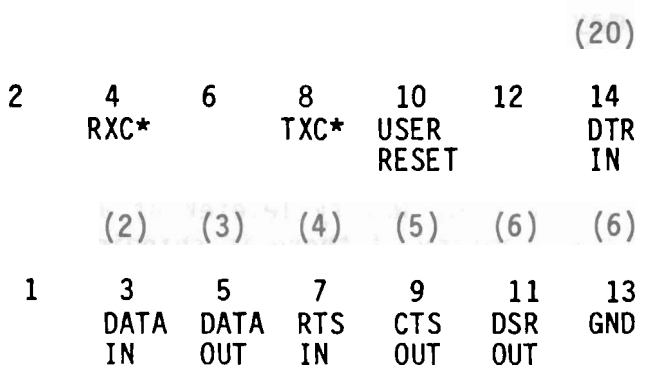
SBC-I need only be plugged into a standard S-100 bus for power and it will be functional, able to utilize the peripherals connected to it with the memory on board. The SBC-I needs to be in a well ventilated area due to the high density of IC's on board. Ideally, the board should be mounted vertically in a stream of air which will be moving across the face of the board. Whatever the mounting position, forced-air cooling is essential. Bring peripheral cables neatly away from the board with enough slack to prevent any tension being applied to the cable, as this may cause the cable to separate from its crimp connection causing intermittent problems.

Some versions of SBC-I do not have on-board RAM. If no RAM is on-board, it must be supplied by installing the 200nsec 64k devices in the columns of empty sockets near the right side of the board. Pin 1 on the IC's should point left. The RAM devices must use the 128 cycle refresh mode in order to be compatible with the SBC-I's refresh circuit. Most 64k RAMs currently on the market meet this requirement - one exception is the Texas Instruments TMS 4164 which requires 256 rows to be strobed during refresh.

Peripheral Connections

Serial Ports

SIO A and SIO-B



EIA pins are shown in parentheses

*-These clock signals are on SIOA only

These are the connections going into channels A and B of the SIO chip. In this configuration, each channel appears as a data communication device, and will connect to a terminal or a printer.

IN and OUT refer to data direction with respect to the SBC-I. Data from an external device is IN to SBC-I, and data to an external device is OUT.

CTS (Clear To Send) and DSR (Data Set Ready) are outputs to the external device and are at a positive voltage levels when the SIO channel is ready to function. RTS (Request To Send) and DTR (Data Terminal Ready) are inputs which must be at a positive voltage level for the SIO channel to function if the Auto Enables option is activated through software.

Either channel can be crimp-connected to a 25-pin RS-232 connector by aligning pin 1 of the cable from the SBC-I connector with pin 1 of the 25-pin RS-232 connector. In this configuration the channel connects directly to a terminal or printer. To connect to a MODEM, the signals must be connected as follows:

SBC-I in #	EIA pin #	Direction	Function
5	2	OUT	Data to MODEM
3	3	IN	Data to SBC-I
11	4	OUT	RTS (Request To Send)
14	5	IN	CTS (Clear To Send)
7	6	IN	DSR (Data Set Ready)
13	7	--	Signal Ground
9	20	OUT	DTR (Data Terminal Ready)

(IN refers to data sent to SBC-I, and OUT refers to data sent to the MODEM.)

Note: If the terminal or printer does not provide RTS and DTR, pins 4, 5, and 20 on the terminal side of the RS-232 male connector must be jumpered together. This ensures that the required handshake signals to the SIO port are provided. If the AUTO ENABLES feature of the SIO is not enabled this is not required. In the standard software provided, AUTO ENABLES is enabled.

EIA Serial Data Transfer Protocol (Control of Data Flow)

Prior to sending or receiving data, the four handshake lines should be active low. However, the SIO will allow control of its receive and transmit functions independently. If the "Auto Enables" function of the SIO channel is enabled (standard), the SIO will not send data until DTR is low (this function is labelled "CTS" on the SIO chip). This is handy for buffered printers which need to stop receiving data until the buffer is printed. By pulling DTR high, the printer will stop the flow of data from the SIO. When it is ready to receive more data, it pulls DTR low. Similarly, if "Auto Enables" is enabled, the SIO will not accept information until RTS is low (this function is labelled "DCD" on the SIO chip). This is primarily used with a communications link where,if signal conditions deteriorate, the data may be garbled.

RS-232-C Voltage Levels

A logic high (a binary ONE), or marking condition, is any voltage less than -3 volts to a minimum of -25 volts. A logic low (a binary ZERO), or spacing condition, is any voltage greater than +3 volts to a maximum of +25 volts. Any level between -3 and +3 volts is undefined. This is called the transition region. The maximum transition time between bit cells is four per cent of the basic clock period. The maximum voltage rate of change (slew rate) is 30 volts/uSec. Thus the maximum RS-232-C transmission speed, based on voltage swings of -12 to +12 volts, is 50,000 baud.

Serial Data Timing

Prior to transmitting data, the signal line is held high (marking). It goes low (spacing) to indicate the start of a character. The bits representing the character are then sent Least Significant Bit first, then a parity bit (if used), and finally 2 stop bits. The stop bits indicate the end of the character and are always logic ONEs. The standard SBC-I is set up for 8 data bits, no parity, and 2 stop bits.

The value of each character bit is held for the entire length of each bit cell. The length in time of each bit cell is the basic clock period, equal to the reciprocal of the baud rate. Thus for 9600 baud, each bit cell is 104 uSec long (.0001041 Sec=1/9600).

Parallel Ports

PIO A

2	4	6	8	10	12	14	16
RESET	+12	+5	GND	B STB	B RDY	A STB	A RDY

1	3	5	7	9	11	13	15
D7	D6	D5	D4	D3	D2	D1	D0

PIO B

2	4	6	8	10
	D1		D2	D3

1	3	5	7	9
	D0		-12	GND

These are the connections into the PIO chip. The PIO chip has two parallel ports, A and B. As configured, PIO A may be used as an input, output, bidirectional or control port with four handshake lines. PIO B is the same except that it does not have bidirectional capabilities or handshake lines.

The signals are:

D0 - D7 — 8 data lines

A STB — Strobe input pulse from a device. Depending on the mode of operation, it means:
1. Output mode: Positive edge of this strobe is issued by the device to acknowledge the receipt of data made available by PIO A.
2. Input mode: The strobe is issued by the device to load data from the device into PIO A.
3. Bidirectional mode: Same as 1, except output data are present only while A STB is low.
4. Control mode: The strobe is inhibited internally.

A RDY — Ready output to a device. Depending on the mode of operation, it means:
1. Output mode: Indicates that the data bus is stable for transfer to the device.
2. Input mode: When active, it indicates that PIO A is ready to accept data from the device.
3. Bidirectional mode: Same as 1.
4. Control mode: Always in a low state.

RESET — The active-low reset line on the SBC-I. This can be used to reset a hard disk connected to PIO A.

B STB — Used when PIO A is in the bidirectional mode; strobes data from the device into PIO A.

B RDY — Used when PIO A is in the bidirectional mode; it goes high to indicate that PIO A is ready for data from the device.

The software supplied by Teletek allows PIO A to be set up as an input port or an output port printer. PIO B is set up in the control mode as follows:

D7 is interrupt request from S-100 bus (an input). Not available for the user.

D6 is the EPROM enable output. Not available for the user.

D5 is attention request from the S-100 bus (input). Not available for the user.

The remaining bits D0-D4 are not used internally and can be utilized by the user. D0-D3 are supplied on the PIO-B connector.

IV. THEORY OF OPERATION

The SBC-I is a stand-alone computer (CPU with ROM, RAM, serial and parallel I/O) which can communicate with the S-100 Bus Master via a FIFO (First-In, First-Out) memory. Because its operation is independent of the S-100 bus, several SBC-I's can be resident in a system providing inexpensive multiple-processor, multiple-user capabilities.

Reset

The SBC-I can be reset in three ways: via an active-low line from the user; when RESET* on the S-100 bus is low; whenever port 03 is read by the master CPU. Any of these reset operations will trigger a monostable which will produce a 100 uSec pulse to reset the on-board logic. Due to this short reset pulse, dynamic memory data will not be lost.

Reset-Jump

After a reset operation, the EPROM/ROM on board will be enabled. This ROM occupies location 0000H to 1FFFH, an 8k-byte block (thus a 2716,2732, or 2764 EPROM may be used). When the ROM is enabled, only the ROM will appear in this memory block: the underlying RAM can be written to, but not read. When the ROM is disabled, all RAM is active.

The initialization program in the ROM must set up the on-board IC's including the memory management bipolar RAM. The program in the ROM can then move itself to another area in RAM and execute that location. It is important to note that the instruction following the disable ROM operation will be fetched from RAM. The ROM is disabled by writing a 0 to bit 6 of PIO B.

Memory Management

The SBC-I contains 128k bytes of RAM which are organized by a bipolar RAM into 32 independent 4k-byte blocks. Because the Z80A CPU can access only 64k bytes at a time, only 16 RAM blocks can be accessed by the CPU at one time. In addition, each block can be write protected.

Two bipolar RAMs, each 16 x 4, provide a high-speed lookup able to control access to the dynamic RAM. The four high-order address lines from the CPU (A-12 - A-15) become the address lines for the bipolar RAMs. The selected bipolar RAM data then provide 4 translated address lines, a row-select signal to choose between the two 64k banks of RAM, and a write-protect signal. The write-protect signal will prevent any alteration of the protected RAM block. The protected block will act like ROM. The row-select signal selects the second bank. Blocks from bank 0 and bank 1 can be mixed in any manner.

The memory management can be used to keep more than one applications program in RAM at one time. Switching the bank of RAM in and out is much faster than a disk access. Alternatively, or in addition, 64k or more of data can be kept in RAM at one time for fast access.

The bipolar RAM is organized as follows:

Bit	Function
5	Write protect, active high
4	Select bank 1, active high
3	Ram A-15
2	Ram A-14
1	Ram A-13
0	RAM A-12

The 16 locations of the bipolar RAM are loaded by using the indirect I/O instructions of the Z-80A CPU. The high-order address lines A-12 and A-15 select which bipolar RAM location is accessed. The data on the data bus are then written into the bipolar RAM. **The C register is always set to access port 1CH.** The following instructions can be used:

(The data are inverted by the bipolar RAMs. Thus to set a bit high, a zero must be written to the RAM.)

OUT (C), r : the B register is loaded to set A-12 through A-15 as desired. The register r contains the desired data.

OUTI, OUTD : the B register is loaded to set A-12 through A-15 as desired (00, 10, 20, etc), and the appropriate data in RAM or ROM are loaded into the bipolar RAMs. Note: don't alter the control of the RAM block in which the memory management data are stored, or erroneous data will be obtained in the next execution of this instruction. Remember that the decremented value of B is placed on the address bus.

Note: the bipolar RAMs must be initialized by the ROM after reset to access the dynamic RAM. Do not use dynamic R. prior to this initialization due to the uncertainty of which RA block will be active or write-protected.

DYNAMIC RAM CONTROL

The dynamic RAMs are accessed whenever the CPU activates its M1 signal, or MREQ and RD or WR are active. Either case will cause a low on the output of U-19 which will clock U-12A and U-12B high. The output of U-12A is gated through U-35 to activate the RAS line of the selected bank of RAM ICs. The address multiplexers, U-32 and U-33, initially send the low order address lines from the CPU to the dynamic RAMs. When RAS goes active low, the RAMs internally latch these low order address lines.

The output of U-12B starts a positive pulse in U-20, a delay line. When the pulse in U-20 reaches the 20% delay point, output 1 goes high which clocks U-28B Q* low, and after being inverted in U-13, resets U-12B. U-28B changes the address multiplexers so that the high-order address lines of the CPU, as modified by the memory management circuit, will be sent to the RAMs.

When the pulse in U-20 reaches the 40% delay point, output 2 goes high which clocks U-28A Q* low. U-28A Q* sets the CAS lin of the RAMs low, which causes the RAMs to latch the high ord CPU address provided by the address multiplexers.

When the pulse in U-20 reaches the 100% point, output 5 goes high. This output is inverted by U-13 and resets U12A, to allow the RAM RAS circuits to pre-charge prior ro the next access.

When the RFSH output of the CPU goes low, the CPU places a refresh address on the lower seven address lines. When MREQ subsequently goes active, a memory cycle is started which is identical to a normal RAM access, except that the address multiplexers do not select the upper address lines and CAS remains inactive.

ROM Options

The SBC-I can support 2716, 2732, and 2764 EPROMs as well as their masked-ROM counterparts. The ROM socket is either 24 or 28 pins and the option jumper below U47 is set according to the device. The following table summarizes the requirements.

ROM	Socket	Jumper
2716	24	E5 to E6
2732	24	E5 to E7
2764	28	E5 to E7

Wait State Options

SBC-I can generate one memory wait-state for the on-board memory cycles. The available options for this wait state are during all ROM accesses, all M1 cycles, or all memory cycles. Usually, only the ROM requires a wait state. For operation at a 6 MHz CPU clock, and with 200nSec RAM, a wait state will be required for all memory cycles. The jumpers for the various wait states are located below U32:

Wait State	Jumper
ROM only	E1 to E4
all M1	E1 to E2
all memory	E1 to E3

CTC

Two channels of a Z-80A CTC provide the clocks for the SIO. Channel 0 provides the clock for SIO-A, and channel 1 provides the clock for SIO-B. The trigger inputs of channels 0 and 1 connect to a 1.2288 MHz source. Thus all standard serial transmission rates will be generated by loading the appropriate integral divisor into the CTC channel. The CTC channel must be set to the Counter mode. The divisor loaded into the CTC channel is calculated as follows:

D=1,228,800/(Baud Rate X R) where D = divisor, Baud Rate = desired serial speed (4800, 9600, etc), and R is the lock divider set in the SIO channel (16, 32, 64).

Example: Desired Baud Rate = 19,200; with SIO divider set to 16

D=1,228,800/(19,200 x 16)
D=4

The output of channel 2 of the CTC connects to the input of channel 3. This allows a large divisor to be implemented t produce a one-second interrupt in channel 3. The trigger input of channel 2 connects to a 9,600 Hz source.

PIO

PIO-A provides parallel communication with an external device. Part of PIO-B provides on-board control functions while the four lines can connect to an external device. Because PIO-B provides the Z-80 mode II vectored interrupt from the S-100 bus, PIO-A cannot be set to the bidirectional mode. The on-board functions of PIO-B are:

PIO-B bit	Function
7	Interrupt request from S-100 bus, active low. This is an input.
6	ROM enable, active high. This is an output.
5	Attention bit from S-100 bus, active low.
4	Not used.

To avoid confusion, only bits 5 and 7 of PIO-B should be enabled for interrupts. PIO-B is set up in the control mode.

SIO

Full handshaking is available on both channels of the SIO. In addition, channel A can connect to a synchronous MODEM that provides the receive and transmit clocks. A user reset line is available at each serial connector. This is an active-low signal that will reset the SBC-I.

If channel A is to connect to a MODEM, the six RS-232 connections DIN, DOUT, RTS, CTS, DSR, and DTR must be swapped to the appropriate lines from the MODEM. In addition, for connection to a synchronous MODEM that supplies the transmit and receive clocks, the connections to TXCA and RXCA must be cut, and jumpers added to U-44 to supply the MODEM clocks.

Connections required for a MODEM are:

EIA	SBC-I
2	5
3	3
4	11
5	14
6	7
20	9

If a synchronous MODEM is employed that supplies transmit and receive clocks for the SIO, the connections from the CTC to pins 13 and 14 of the SIO must be cut,and jumpers installed from pin 13 of the SIO to pin 11 of U44 and pin 14 of the SIO to pin 3 of U-44.

S-100 Bus Addressing

The SBC-I occupies four I/O locations in the S-100 bus I/O space. Address lines A-2 through A-7 of the S-100 bus are decoded to determine the SBC-I address. To set the address, jumpers are placed in the 14-pin address-select pad. This pad is ocated in the lower right part of the board, just below U11. ,he pins select A7 through A2 from left to right. If no jumper is in place, the comparator will respond to a logic-high address line. If the jumper is in place, the comparator will respond to a logic-low address line. Example:

Address desired = C0H

Address-select pad

A-7	Open
A-6	Open
A-5	Jumper
A-4	Jumper
A-3	Jumper
A-2	Jumper

to interrupt acknowledge from the S-100 bus
ring pDBIN active high. If it is desired to
BIN is active, connect E8 to E9. This allows
to be placed on the data bus only when pDBIN
ctive high.

SBC-I Interrupts

SBC-I, the PIO is the highest-priority
the SIO is next, and the CTC is lowest.

Port Assignments

SBC-I

Port	Function
00	SIO-A data
01	SIO-A status and control
02	SIO-B data
03	SIO-B status and control
04	PIO-A data
05	PIO-A control
06	PIO-B data
07	PIO-B control
08	CTC channel 0
09	CTC channel 1
0A	CTC channel 2
0B	CTC channel 3
0C	FIFO data
0D-0F	not used
10H	Clear FIFO address counters
11 - 13H	not used
14H	Clear interrupt request from S-100 bus
15 - 17H	not used
18H	Generate interrupt request to S-100 bus
19 - 1BH	not used
1CH	Memory management control
1D - 1FH	not used

Port Assi

S-100 Bus

rite Operation

Port	Function
00	Generate interrupt request to SBC-I, bit 7 PIOB
01	Write to the FIFO
02	Load interrupt vector register
03	Generate attention request, bit 5 PIOB

Read Operation

00	Clear interrupt request from SBC-I
01	Read data from he FIFO
02	Clear FIFO address counters
03	Reset SBC-I

Note: SBC-I occupies 4 I/O ports on the S-100 bus. Thus he above addressing for multiple SBC-Is will be multiples of 4: 00-03, 04-07, 08-0B, 20-23H, etc.

IN CASE OF TROUBLE

If the SBC-I does not respond the first time it is connected, try the following:

1. It is highly recommended that the entire manual be read carefully, especially the "Peripheral Connections" section.

2. If there is no response at the console, make sure that the handshake lines are functional and the baud rate is correct. Make sure that on-board RAM is working.

3. If the SBC-I was originally shipped without RAM, make sure the memory chips are installed correctly. The RAM devices must use the 128 cycle refresh mode in order to be compatible with the SBC-I's refresh circuit.

SBC-I 1.0 Monitor

The SBC-I monitor has several commands that aid in the debugging of software on the SBC-I. The monitor expects a terminal on SIO B at 9600 baud.

On reset, the memory management circuit is initialized and then the I/O devices. SIO B is set to 9600 baud and SIO A to 1200 baud. PIO A is set up as an output port and PIO B is set up in the bit control mode. Bits 7,5,4,3 and 2 are inputs and bits 6,1 and 0 are outputs.

The monitor code is then moved up to the top 1024 bytes of memory and a jump to the boot routine is executed. To get out of the boot routine the user must type a control X.

Monitor Commands

BT<cr> Boot from the master storage device. The SBC-I waits for an interrupt from the master. When the interrupt is received the SBC-I reads the first 256 bytes in the FIFO and executes them at 0000H. If a Request Acknowledge (on bit 5) is received a 00H is stored in the first byte of the FIFO and the SBC-I generates an interrupt to the master and continues waiting for an interrupt from the master. The first byte returned after an interrupt from the master must be 00H.

CA_#<cr> Change register AF to #.

CB_#<cr> Change reg. BC to #.

CD_#<cr> Change reg. DE to #.

CH_#<cr> Change reg. HL to #.

CS_#<cr> Change reg. SP to #.

CP_#<cr> Change reg. PC to #.

DA_#<cr> Display ASCII - Displays memory in hex and ASCII from #, eight bytes at a time. Hit space bar to see next eight.

E_#<cr> Enter Memory - Write to memory in hex starting at #.

EX_#<cr> Execute - Continue execution setting a breakpoint at #.

F_#1_#2_#3<cr> Fill memory block from #1 to #2 with #3.

H_#1_#2<cr> Perform Hex addition and subtraction of #1 and #2.

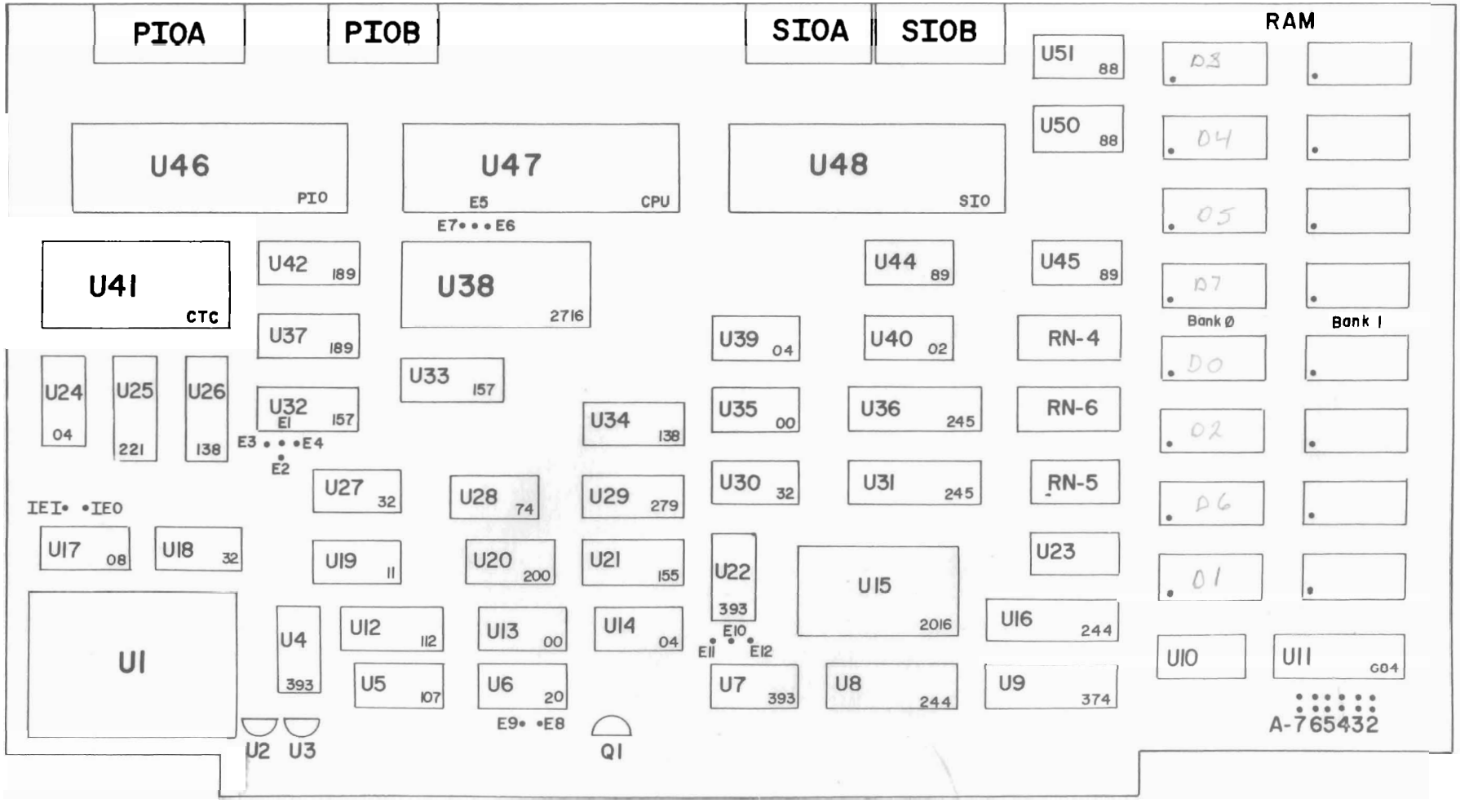
G_#<cr> Go to #. If routine ends with a return, control will be returned to the monitor when routine is done.

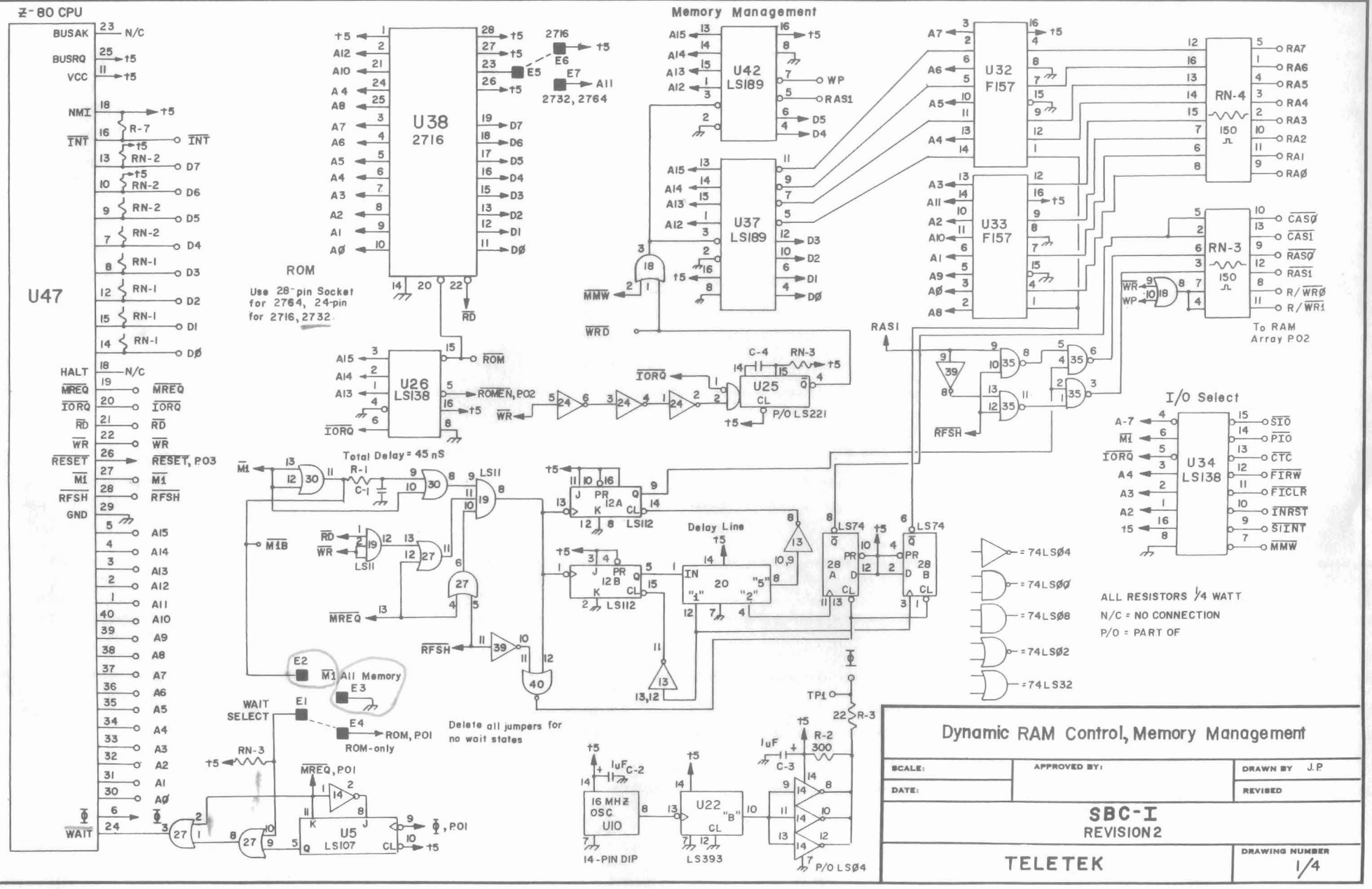
I_#<cr> Input from port #. Hit the space bar to repeat.

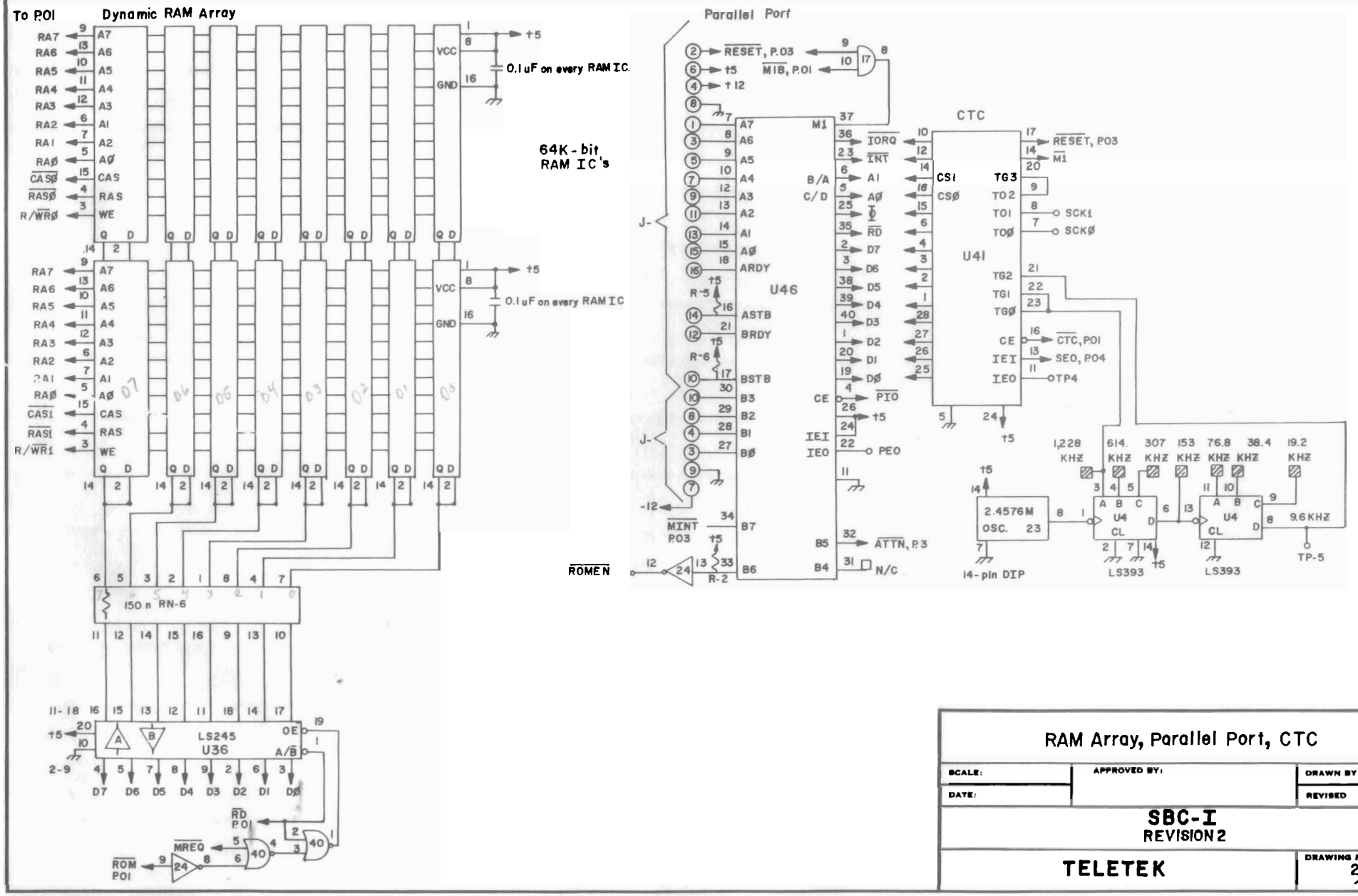
M_#1_#2_#3<cr> Move memory block starting at #1 through #2 to #3.

O_#1_#2<cr> Output to port #1 the byte #2. Hit the space bar to output again. #1 is loaded into register pair BC to allow outputs to the memory management RAM.

TELETEK SBC-I
Board Layout







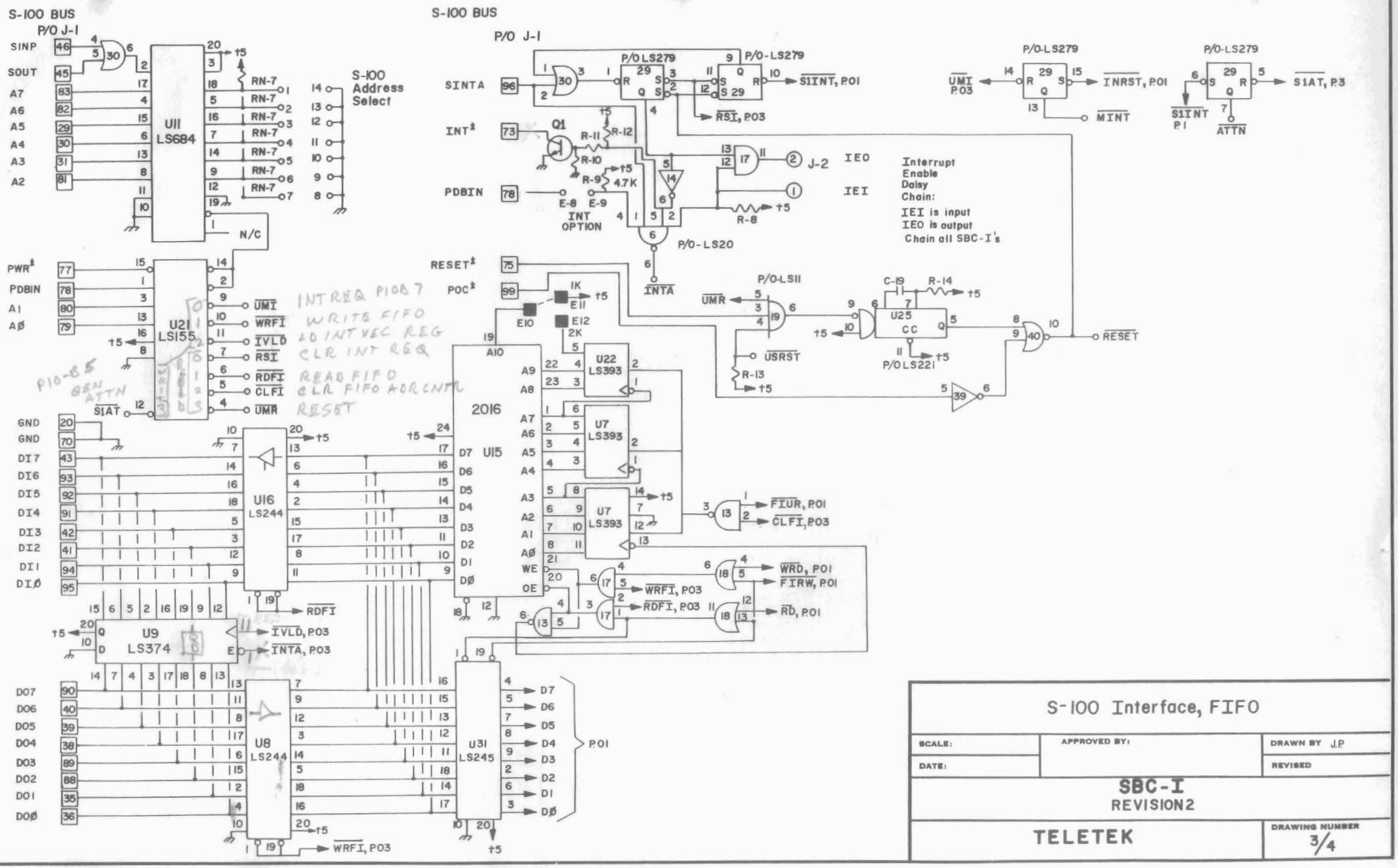
RAM Array, Parallel Port, CTC

SCALE:	APPROVED BY:	DRAWN BY J.P
DATE:		REVISED

SBC-I
REVISION 2

TELETEK

DRAWING NUMBER 2/4



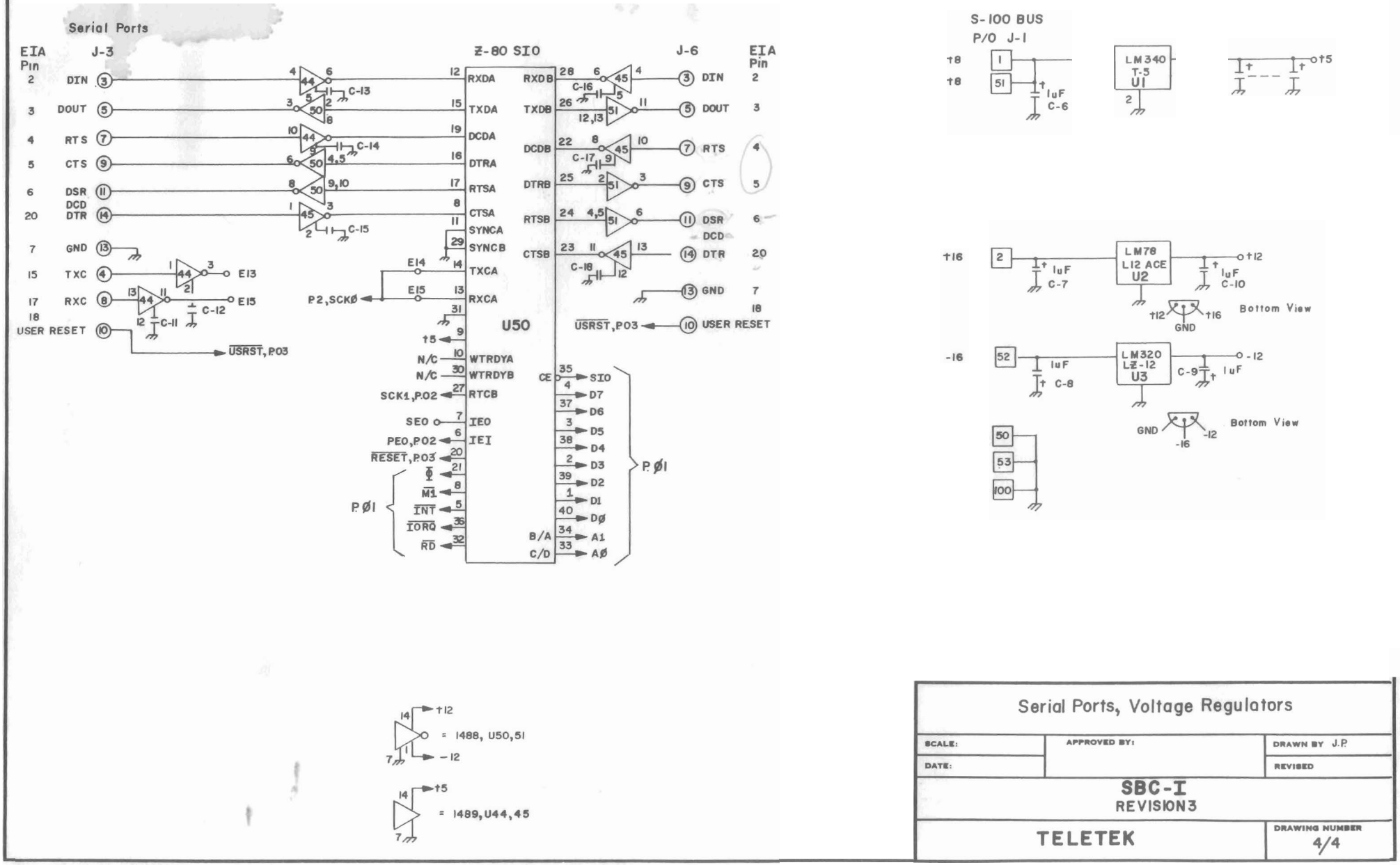
S-100 Interface, FIFO

SCALE:	APPROVED BY:	DRAWN BY J.P
DATE:		REVISED

SBC-I
REVISION 2

TELETEK

DRAWING NUMBER 3/4



Serial Ports, Voltage Regulators		
SCALE:	APPROVED BY:	DRAWN BY J.P.
DATE:		REVISED
SBC-I REVISION 3		
TELETEK		DRAWING NUMBER 4/4

Turbodos & Update

SBCI REVISION 3
DOCUMENTATION

The following changes have been made to the SBCI board to bring it up to a Revision 3 level.

1. Jumper options are now available that allow the user to change the method of communication to the host system from pure interrupt driven to a combination of interrupts and polling. This change will accomodate the TurboDOS operating system.

2. The option to select either a 1K-byte RAM or a 2K-byte RAM for the FIFO has been deleted. The SBCI will now only accept 2K-byte RAM devices.

In order to implement the polling option (when running TurboDOS) the following modifications to the SBCI must be made. All changes are made on the solder side of the SBCI unless otherwise noted.

1. Above pins 13 and 14 of U-16 are three option pads. The center pad is now connected to the right pad (which connects U-9 to D00). Cut this trace between the center and right pads and jumper the center pad to the left pad (which connects U-9 to PIOB D0).

2. Above pin 8 of U-9 there are three option pads. The center pad is now connected to the right pad (which connects U-9 to D01). Cut the trace between the center and right pads, and jumper the center pad to the left pad (which connects U-9 to PIOB D1).

3. Above pin 6 of U-6 there is an option pad. A trace now connects pin 6 to this pad. Cut this trace (this disconnects INTA* from pin 1 of U-9).

4. Between and just to the right of pins 1 and 14 on U-7 there are two option pads. There is currently no connection between these two pads. Jumper these pads together (this connects RSI* to pin 1 of U-9).

5. Remove Q1, located below U-14 (a 2N3904 transistor), in order to disconnect the SBCI from the INT* line on the S-100 bus.