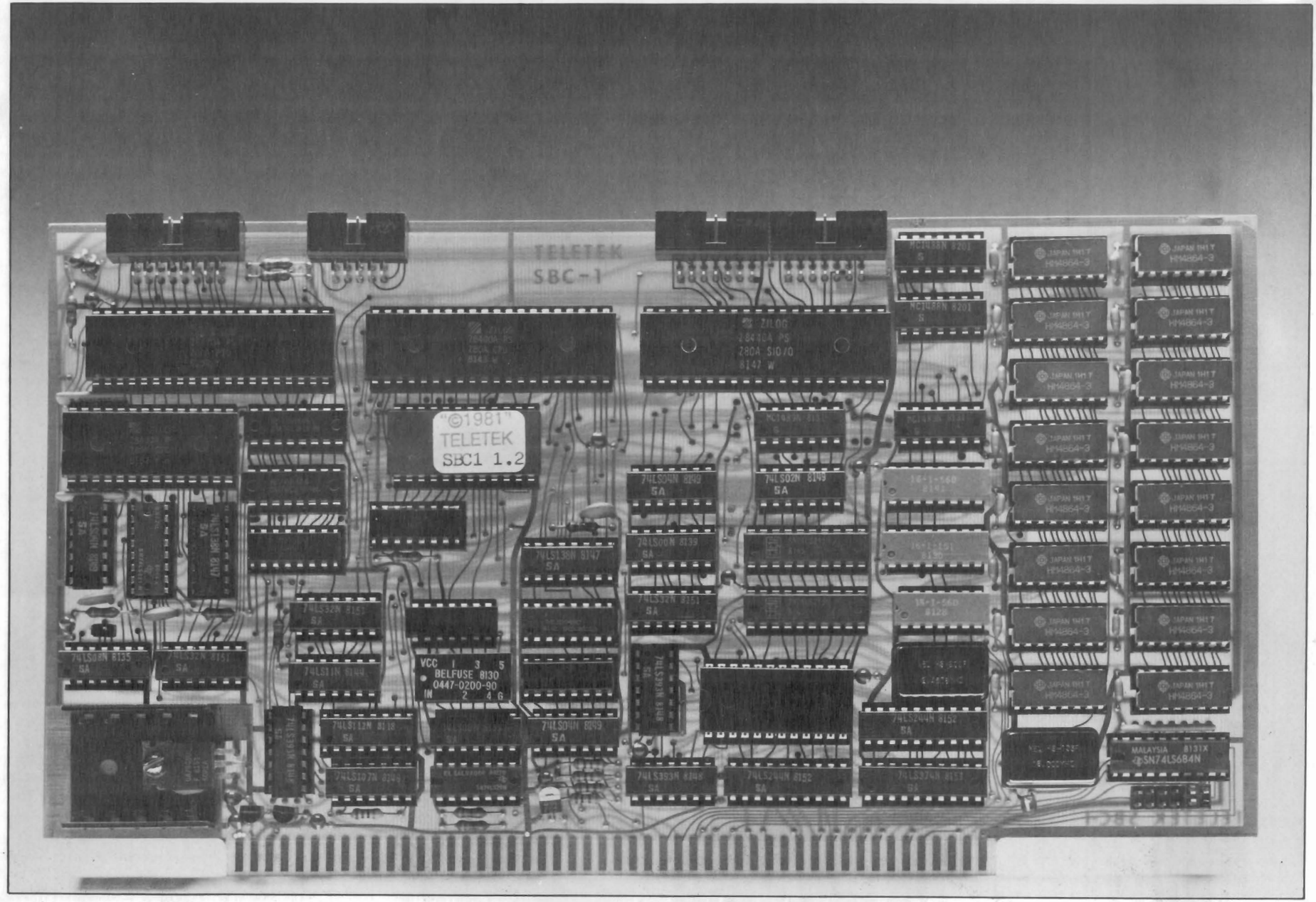
TELETEK



SBC-I

SBC-1 is a single board computer designed to be implemented in a high-performance multiprocessor system. The SBC-I allows the systems integrator to provide each user with his own CPU, 128k of segmented memory, two serial ports, and two parallel ports. Because each user has his own CPU, the addition of other users in the system causes far less speed degradation than in currently available "time-sharing" multi-user systems.

PROCESSOR

The SBC-I uses the high powered Z-80A or Z-80B CPU from Zilog. CPU speed on board the SBC-I is independent of the system clock; therefore, the ability to run a 4MHz SBC-I in a 6MHz S-100 system allows the systems integrator to optimize the efficiency and the cost effectiveness of his system design.

MEMORY

Each SBC-I has 128k of RAM on board which incorporates a memory management circuit that allows virtual memory operation. The circuit partitions the RAM into 4k segments that can be dynamically addressed on any 4k boundary of the CPU address space. This allows ultimate flexibility in the implementation of future operating systems and applications software.

In addition to RAM, there is 2k, 4k, or 8k of EPROM available for initialization routines. After the routines have been completed, the EPROM may be disabled by software.

RAM DRIVE

An option is available that will allow the use of the extra memory provided on SBC-I as a local disk drive. Because this local drive is in reality a bank of semiconductor RAM, it will be many times faster than the system floppy disk drives. This RAM drive is called the "M" drive and it can be used like any other CP/M supported drive unit. Files can be loaded into the M drive using the CP/M PIP command. There is a total of 59k bytes available for file storage.

I/O PORTS

A Zilog SIO provides two independent serial ports with software selectable speeds. A Zilog CTC providing the clock signals to the SIO also has two additional counter/timer outputs available to the user at his option.

Both serial ports provide RS-232C interface capability for easy local interconnection at speeds up to 19,200 baud. The baud-rate clock is supplied by a 2,4576MHz oscillator. In addition, there are provisions allowing a synchronous MODEM to connect to one serial port.

A Zilog PIO provides two parallel ports for use in interfacing parallel devices. One port is bidirectional and the other provides control lines (some of which are used internally).

An adaptor board is available that converts the parallel ports to an RS-422 compatible interface. The RS-422 port provides high speed (up to 154k baud) long distance (4,000 feet) communications ability.

FIFO/S-100 BUS INTERFACE

The bus interface is fully IEEE-696 S-100 compatible. The SBC-I appears as a slave on the S-100 bus and communication to the system is via a 1k byte or 2k byte FIFO interface. Therefore, the SBC-I appears in the system as a set of I/O ports.

There are three levels of reset capability in the system utilizing the SBC-I. The first is the traditional hardware system reset in which all components of the system are reset. The second level of reset ability is when the user resets only his SBC-I leaving other slaves and the bus master undisturbed. The third level of reset is an individual software reset available for each SBC-I on the bus. Therefore, the bus master can reset any one SBC-I without affecting other users.

OPTIONAL USES

The capability of Teletek's SBC-I is not limited to the S-100 bus. With appropriate interfacting SBC-I can be operated as a stand-alone network user node. Communications to other network nodes can be implemented on RS-232, RS-422, or through the FIFO interface.

Specifications subject to change without notice.

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