OPERATIONS
MANUAL

ExpandoRAM

Expandable Random Access Memory Board

SD Systems

LIMITED WARRANTY

This unit is warranted for a period of ninety (90) days from the date of purchase to be free from material or workmanship defects. Should the product fail to perform satisfactorily return it prepaid to SD Systems and it will, at our option, be repaired or replaced free of charge, provided the unit is received during the warranty period. This warranty is invalid if product has been misused or modified. Warranty is limited to replacement of defective parts and and no responsibility is assumed for damage to other equipment.

This warranty is made in lieu of all other warranties expressed or implied.

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TABLES

APPENDICES

SECTION 1

1-0 INTRODUCTION

The EXPANDORAM™ board provides a low cost means for expanding Random Access Memory capability for computers utilizing the S-100 bus structure. The EXPANDORAM™ will interface directly to the following computers: IMSAI, ALTAIR A, ALTAIR B, SOL-8, CROMEMCO, the SBC-100, and Z80 CPU-B card. Poly-88 Computers must have the Poly modifications to put the SM1 and P WAIT Lines (Bus pins 44 and 27 respectively) on the bus.

1-1 GENERAL DESCRIPTION

The EXPANDORAM™ board is a high performance dynamic RAM board using state-of-the-art MOS dynamic memory devices from MOSTEK CORPORATION. The EXPANDORAM™ may be configured to have a memory capacity of 8K, 16K, 24K, or 32K bytes of memory using the MK 4115/4108 (8,192x1 MOS dynamic RAM) or 16K, 32K, 48K, or 64K bytes of memory using the MK 4116 (16,384x1 MOS dynamic RAM) memories. An eight position DIP Switch is provided for positioning memory on any 8K or 16K boundary. Other notable features of the EXPANDORAM™ board include:

(1) Bank selectable write protect.

(2) Phantom output disable or manual switch selectable output disable.

(3) Typical power dissipation of 5 watts.

1-2 PHYSICAL

The EXPANDORAM™ board is implemented on a single 5.25" x 10.0" x 0.65" Printed Circuit board. The board requires three DC voltages at levels of +7V to +10V. +14V to +18V. and -14V to -18V DC. The EXPANDORAM™ board is interfaced to the system by connector J-1.

1-3 SPECIFICATIONS

Table 1-1 lists the overall specifications for the EXPANDORAM™ board.

Table 1-2 lists the pin usages of connector J-1 for the EXPANDORAM™.

TABLE 1-1

SPECIFICATIONS

Memory Capacity	Up to 32,768 bytes (8K RAM) Up to 65,536 bytes (16K RAM)
Memory Access	375 ns max.
Memory Cycle	500 ns min.
Interface Levels	TTL Compatible
Power (2 us memory cycle)	+7V to +10V @ 400 mA (max) +14V to +20V @ 200 mA (max) -14V to -20V @ 30 mA (max)
Physical Dimensions	5.25" x 10.0" x .65"
Operating Temperature	0 degree C to 50 degree C

TABLE 1-2
CONNECTOR J1 PIN OUT
FOR 32K/64K EXPANDORAM™

PIN #	SIGNAL NAME	DIRECTION	DESCRIPTION
1, 51	+8V to 10V		Power
2	+14V to 20V		Power
52	-14V to -20V		Power
24	Ø2	Input	Phase 2 clock
25	Ø1	Input	Phase 1 clock
26	PHOLDA	Input	Hold acknowledge
27	P WAIT	Input	Wait
79, 80, 81, 31, 30, 29, 82, 83	A0-A7	Input	Address bus bits 0-7
84, 34, 37, 87, 33, 85, 86, 32	A8-A15	Input	Address bus bits 8-15
36, 35, 88, 89, 38, 39, 40, 90	D0-0 to D0-7	Input	Data bus in
95, 94, 41, 42, 91, 92, 93 43	D1-0 to D1-7	Output	Data bus out
44	SM1	Input	Machine cycle one
47	SMEMR	Input	Memory read
66	RFSH	Input	Refresh (Z80 CPU card
68	MWRT	Input	Memory write
72	PRDY	Output	Ready
75	RESET	Input	Reset
76	PSYNC	Input	Sync
78	PDBIN	Input	Data bus in
100, 50	GROUND		
48	HALTA	Input	Halt acknowledge

SECTION 2

2-0 FUNCTIONAL DESCRIPTION

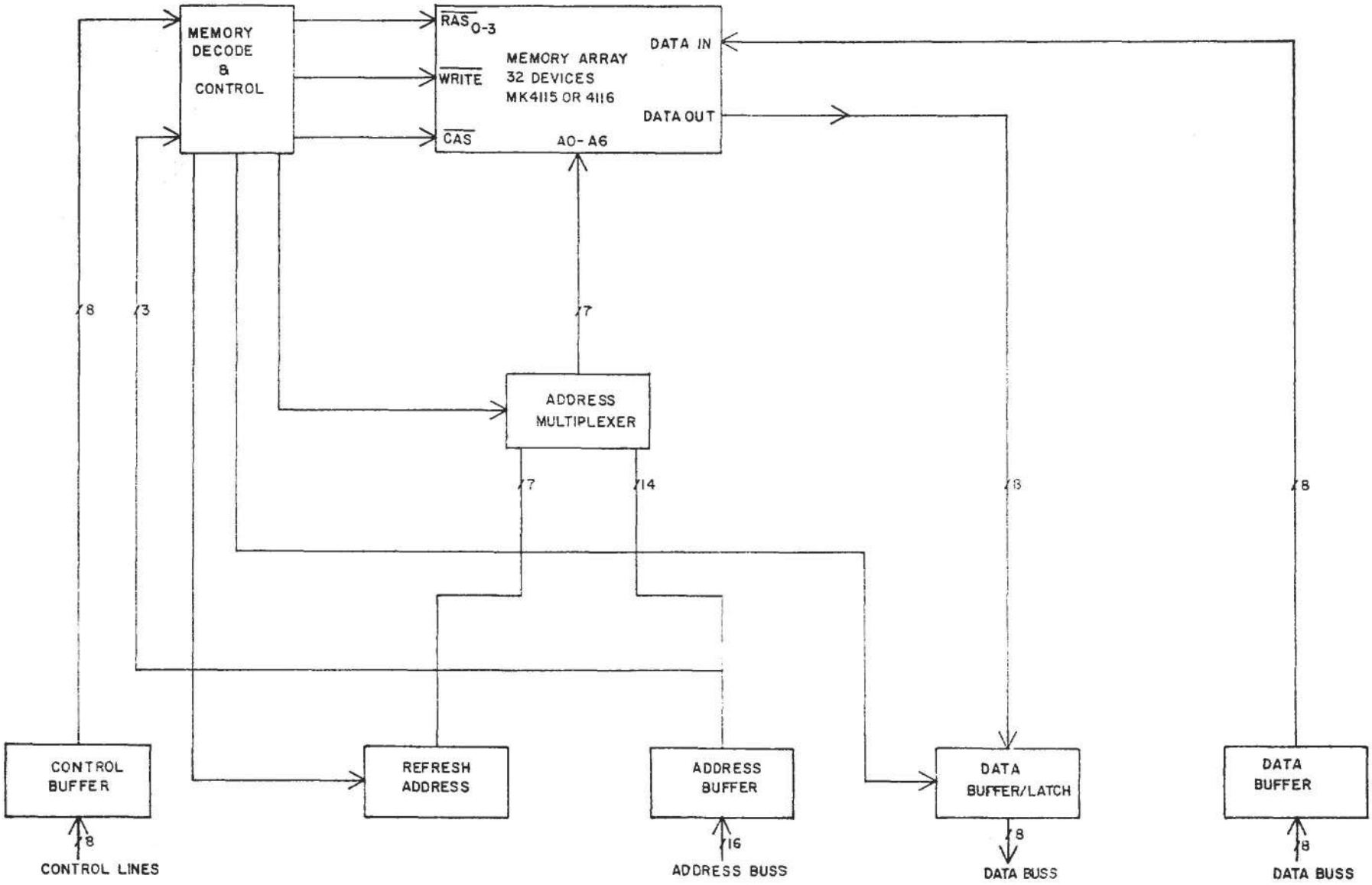
The major functions of the EXPANDORAM™ board are shown in figure 2-1, page 4. The following functions make up the memory interface: memory array, memory decode and control, address multiplexer, and data buffer.

Memory Array - The memory array consists of up to 32 8K or 16K dynamic random access memory elements. Each 8K has an 8,192 x 1 bit capacity, while the 16K has a 16,384 x 1 bit capacity. The 32 8K or 16K RAMS are organized into four banks of eight RAMS each. The eight RAMS each contribute one bit to an addressable location. The total storage capacity of the EXPANDORAM™ is 32,768 or 65,536 bytes, depending on the type of memory device that is used (8K or 16K).

Memory Decode and Control - The memory decode and control section is responsible for generating the timing signals for the memory array, address multiplexer, and data buffer. Timing within the memory decode and control section is generated by a TTL compatible delay line.

Address Multiplexer - The address multiplexer is responsible for taking the address bits from the address bus buffers and multiplexing the proper row and column address into the memory array under control of the memory decode and control section.

Data Buffers - The data buffers, controlled by the memory decode and control section, isolate the memory array from the data bus.



DRAWN JAA	DATE 8/11	SD Systems
CHKD		P.O. Box 28810 • Dallas, Texas 75228 • 214-271-4667
APPD		BLOCK DIAGRAM FOR EXPANDORAM
RLSD		SCALE NONE · SHEET 1 OF 1 · NO 0100005 · REVISION E

SECTION 3

3-0 CONSTRUCTION

The 32K EXPANDORAM™ board kit is intended for those persons who have had some prior experience with kit building and digital electronics. If you do not fall into this category, it is highly recommended that you find an experienced person to help you assemble and check-out the board.

Appendix F shows the parts list for the EXPANDORAM™ board. Double check all parts against the parts list.

3-1 ASSEMBLY PROCEDURE

(1) Install the IC sockets in their proper locations. NOTE: No sockets for DIP switches, U1, U2.

(2) Install the resistors as follows:

- ( ) R1 150 OHM ½W (Brown, Green, Brown)
- ( ) R2 4.1K OHM 1/8W 1% Metal Film
- ( ) R3 6.8 OHM 1/8W 5% (Blue, Grey, Red)
- ( ) R4 33 OHM 1/4W (Orange, Orange, Black)
- ( ) R5, R6 3.3K OHM 1/4W (Orange, Orange, Red)
- ( ) R7 470 OHM 1/2W (Yellow, Violet, Brown)
- ( ) R8 1K OHM 1/4W (Brown, Black, Red)
- ( ) R9 200 OHM 1/4W (Red, Black, Brown)
- ( ) Resistor packs: RP1 3K OHM 6 pin SIP
  RP2-RP5 3K OHM 10 pin SIP

NOTE: Pin 1 of the SIP's is designated by a notch or a dot on one end of the package.

(3) Install Diodes CR1, and CR2 with the banded end as shown on the PC Board.

( ) CR1 1N751

( ) CR2 1N914/1N4148

(4) Install the capacitors as follows:

( ) C1, C10, C13, C18, C19, C22 10 MF Tantalum (Note proper polarity)

( ) C3, C7 100 pf mica

( ) C6, C14 200 pf mica

( ) C2, C4, C5, C8, C9, C11, C12, C15, C16, C17, C20, C21, C23-C70 .1MF Ceramic

NOTE: R10 (1K Ohm) and C71 (100 pf) are present on Rev B or later. However, see options table before installing them (Table 4-3).

(5) Install the two voltage regulators with the heat sink, using the 6-32 hardware supplies. NOTE: There are two types of voltage regulators, a +5V and a +12V. Be sure that the regulators are installed as shown on the PC Board.

( ) VR1 +5V 7805/LM 340-5

( ) VR2 +12V 7812/LM 340-12

(6) Install the wire wrap pins. NOTE: It is not necessary to install the wire wrap pins if the board is to be set up for only one type of microprocessor. The wire wrap pins are for those that will be reconfiguring the board frequently.

( ) E1-E3, E10-E18

( ) E19-E30 Rev B or later only

(7) Install DIP switches.

( ) U1 Observe the proper position of the PC Board (The ON side should be toward the top of the board)

( ) U2

(8) Install Transistor

( ) Q1 2N2222

(9) Double check all solder connections for cold solder joints, unsoldered connections, or shorted connections.

3-2 CHECK OUT PROCEDURE

(1) Install the board in the computer and measure the output of the +5V and +12V regulators, VR1 and VR2,

( ) VR1 = 5 volts

( ) VR2 = 12 volts

(2) Measure the power supply voltages in the memory array. (Any of the memory array IC sockets can be used.)

( ) Pin 1 U29 = -5V

( ) Pin 8 U29 = +12V

( ) Pin 9 U29 = +5V

NOTE: DO NOT PROCEED WITH BOARD CHECK-OUT UNTIL ALL POWER SUPPLY VOLTAGES ARE CORRECT. The TTL logic and MOS memories can be permanently damaged if improper voltages are applied.

(3) Install the IC's in their sockets observing the Pin 1 designation on each socket on the PC Board.

( ) U3 74LS00

( ) U4 74LS93

( ) U5 74LS221

( ) U6 74LS21

( ) U7 74S138

( ) U16 74LS157

( ) U17 74157

( ) U19 74LS14

( ) U20 74LS75

( ) U21 74LS157

( ) U8 74LS00

( ) U9 74LS32

( ) U10 74LS27

( ) U11 74LS93

( ) U12 DELAY LINE

( ) U13 7400

( ) U14 7425

( ) U15 74LS93

( ) U22 74157

( ) U23 74S373

( ) U24 74LS14

( ) U25 74LS14

( ) U26 74LS14

( ) U27 74LS14

( ) U28 74LS244

*( ) U32, U36, U40, U44, U48, U52, U56, U60 (Bank 0)

( ) U31, U35, U39, U43, U47, U51, U55, U58 (Bank 1)

( ) U30, U34, U38, U42, U46, U50, U54, U58 (Bank 2)

( ) U29, U33, U37, U41, U45, U49, U53, U57 (Bank 3)

*NOTE: If less than 32K is being installed on the board then refer to Section IV under ADDRESSING SWITCH to determine in which Bank the memory should be installed.

(4) Double check all IC's for proper orientation and location.

(5) Refer to UTILIZATION SECTION for proper configuration of jumper options, and connect jumper options as required.

(6) Install board into computer and turn on power.

(7) By using front panel or monitor program, deposit data into a memory location that falls within the boundaries of the EXPANDORAM™ board. Now examine the same location in which data was deposited. If the proper data is not read back, power the system down and double check the following:

(1) Check ADDRESSING DIP Switch and WRITE PROTECT DIP switch for the correct settings.

(2) Check jumper options.

(8) Reinstall the board and once again try to write and read data from the EXPANDORAM™ board by the use of a front panel or monitor program. If some of the data bits appear to be stuck, power down the board and examine the memory array for bent pins, or a defective memory device. If the board does not respond in any way to write or read data, then examine the TTL IC's for bent pins or improper insertions into the socket.

(9) If the read/write test is successful, verify that memory on the EXPANDORAM™ can be accessed in every bank of memory that is installed on the board.

(10) If all banks can be written to and read back properly, complete check-out of the board by loading the memory test that is shown in Appendix A. Execute the test and verify that all locations within the memory array are functional.

NOTE: When executing the memory diagnostic, it is recommended that the memory board not be on an extender card. Use of an extender card may introduce external noise into the board.

SECTION 4

4-0 UTILIZATION

This section will explain the various options for the EXPANDORAM™ memory card.

4-1 8K or 16K DEVICE SELECTION JUMPERS

Two types of 8K RAMS can be used with the 32K EXPANDORAM™, whereas one type of 16K RAM is used for the 64K board. Table 4-2 shows the jumpers for the 64K board using the 16K RAMS. 8K RAMS will have a dash number (i.e. 4115-41 or 4108-30). The dash number indicates how the boards should be strapped. Refer to Table 4-1.

4-2 ADDRESSING SWITCH

Figure 4-1 shows the switch positions for address selection of the 32K board populated with 8K RAMS.

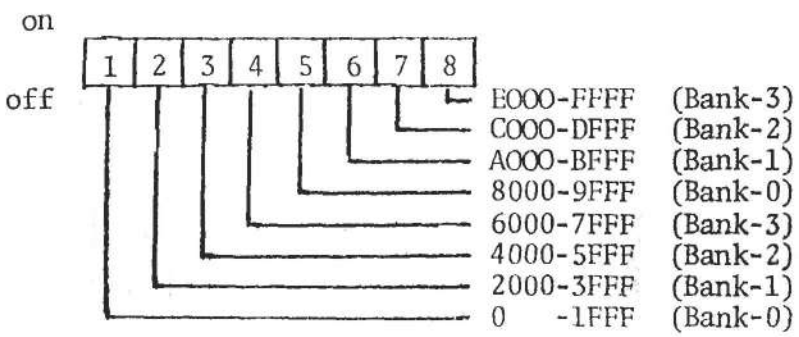


Figure 4-1

TABLE 4-1

JUMPERS FOR MK 4115-40 or -41 SELECTION
or MK 4108-30 or 31

DEVICE	JUMPERS
8K - X0	E16 to E17 Connected
8K - X1	E16 to E17 Open

Where X=4 for 4115 RAMS and X=3 for 4108 RAMS

NOTE: For the 32K RAM board using the 8K, all RAM's for the board must be all -X0 or -X1. The X0's and the X1's CANNOT BE MIXED. Therefore, if additional RAMS are ordered, the same type must be ordered, either -X0's or -X1's.

TABLE 4-2
JUMPERS FOR 16K RAM 64K CONFIGURATION

DEVICE	JUMPERS	
16K RAM	E15 to E16	Connected
	E16 to E17	Open
	E4 to E5	Break etch line
	E6 to E7	Break etch line
	E8 to E9	Break etch line
	E5 to E6	Connected
	E7 to E8	Connected
	E9 to E18	Connected

NOTE: If a 64K Board is to be reconfigured for the 8K RAMS, then the three broken etch lines must be reinstalled, and jumpers connected as shown in Table 4-1.

Figure 4-2 shows the address switch positions for the 64K board populated with 16K RAMS.

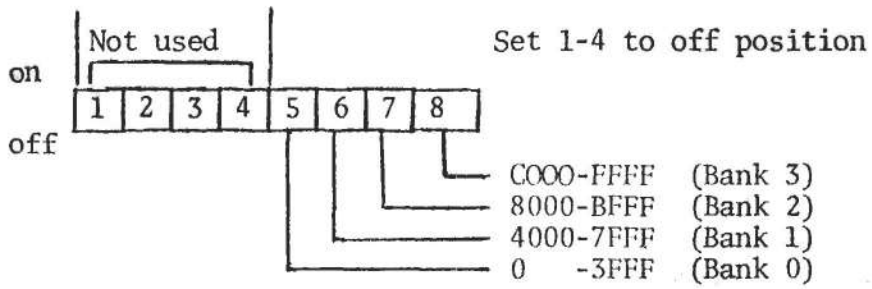


Figure 4-2

4-3 BANK SELECTABLE WRITE PROTECT SWITCH

Figure 4-3 shows the positions for the bank selectable write protect switch.

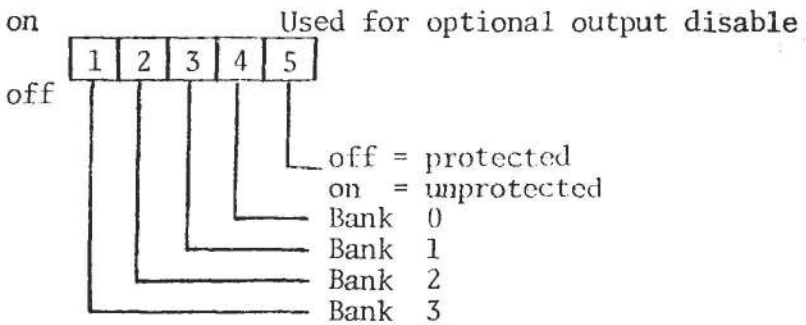


Figure 4-3

4-4 CPU CARD SELECTION

Table 4-3 shows the jumpering for the selection of either an 8080 card, a Z80 CPU card, or IMSAI 8085 CPU card. Expandoram boards are jumpered in the P.C. etch for operation with the SBC-100, Z80 CPU-B and most other Z80 CPU Boards. These P.C. etch jumpers may be cut for use with other CPU's.

Figure 4-4 shows the optional jumpers for connecting the PHANTOM OUTPUT disable control to J1-67 or the manual switch output disable control. (Position 5 of write protect switch.)

TYPE OF OUTPUT DISABLE	JUMPERS
Phantom	E2 to E3 Connected, E1 to E2 Ope
Manual Switch	E1 to E2 Connected, E2 to E3 Ope
None	E1 to E2 to E3 Open

Figure 4-4

NOTE: The PHANTOM OUTPUT disable and the MANUAL switch output disable cannot be enabled at the same time. If the MANUAL switch output disable is selected; Position 5 of the WRITE PROTECT switch will control the function with ON = DISABLE OUTPUT and OFF = ENABLE OUTPUT.

TABLE 4-3

CPU SELECTION

CPU	JUMPER	NOTES	ETCH JUMPERING ON REV E
Z80	E11-E12		x
SBC-100	E20-E21		x
	E22-E23		x
	E26-GND		
	E31-E32*		
	R10	Insert a wire across R10 holes	
8080	E10-E11	Must cut E11-E12	
	E20-E21		x
	E22-E23		x
	E25-E26	Must cut E26-GND	
	R10	Insert a wire across R10 holes	
IMSAI	E10-E11	Cut E11-E12	
8085	E13-E14		
MPU-B	E19-E20	Cut E20-E21	
	E22-E24	Cut E22-E23	
	E26-E27	Cut E26-GND	
	E28-E29		
	R10	Add R10 (1K OHM)	
	C71	Add C71 (100 pf)	

* (E31-E32) prevents depositing in front panel systems and is only necessary when operating with a wait state based disk controller (i.e. versafloppy). If this is not wanted, cut E31-E32 and connect E32-E33.

Figure 4-5 shows the jumper options for enabling/disabling DMA.

	DMA	JUMPERS
FOR 8080 and Z80 CPU CARDS ONLY!	Disabled	E13 to E14 Connected
	Enabled	E13 to E14 Open

Figure 4-5

NOTE: DMA to and from the EXPANDORAM™ is limited to 1 ms or less due to the refreshing requirement of the dynamic memories. It is important to note that the board will not execute refresh cycles during a DMA, if the DMA is enabled. If DMA is disabled, then when a DMA cycle is acknowledged, the board will execute its automatic refresh cycle to retain memory during DMA cycles to and from other memory boards.

A DMA read cycle will be triggered when the following logical equation is true:

$$\text{DMA READ} = \text{MEMR} \cdot \text{SYNC} \cdot \overline{\emptyset 2}$$

A DMA write cycle will be triggered with the following condition:

$$\text{DMA WRITE} = \text{MEMW}$$

APPENDIX A

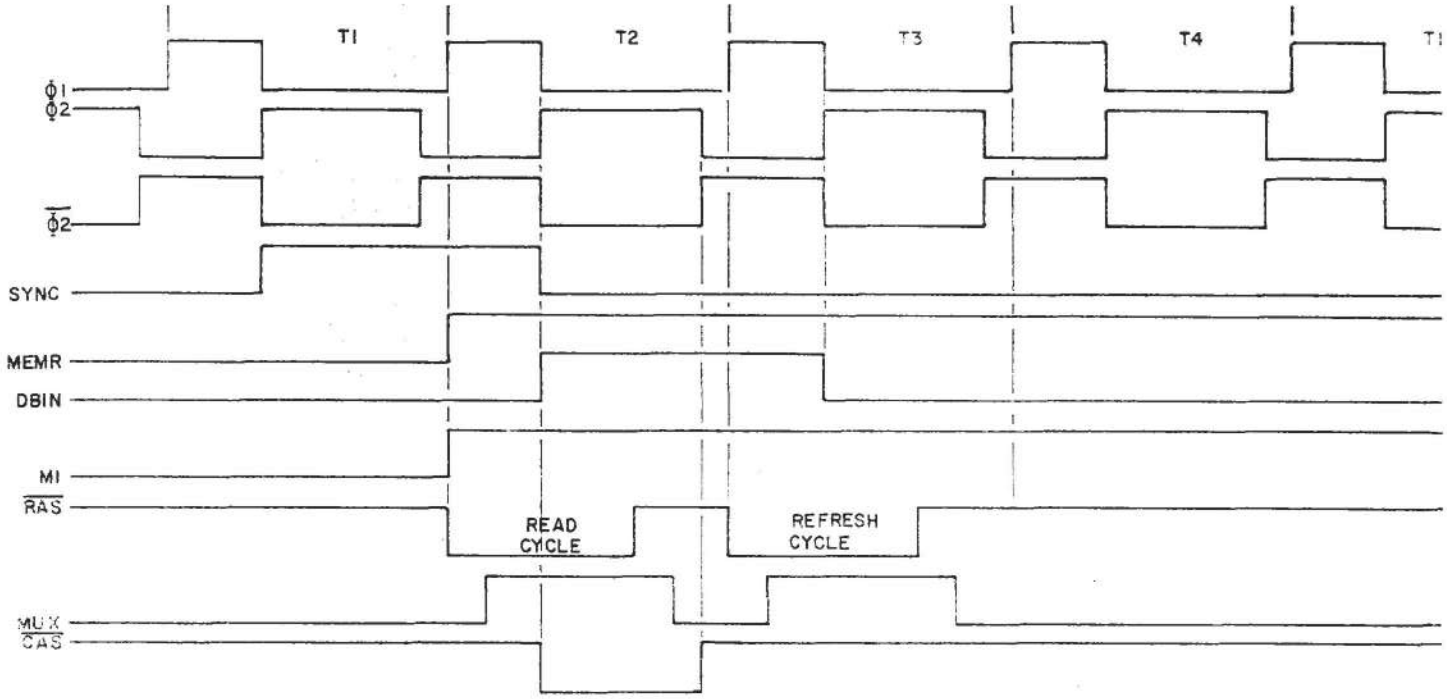
MEMORY DIAGNOSTIC SOFTWARE LISTING

```
ADDR  OBJECT     ST # SOURCE STATEMENT

                 0001 ;TRANSLATED FROM DEC 1976 INTERFACE MAGAZINE
                 0002 ;
                 0003 ;THIS IS A MODIFIED ADDRESS STORAGE TEST WITH
                 0004 ;AN INCREMENTING PATTERN
                 0005 ;
                 0006 ;256 PASSES MUST BE EXECUTED BEFORE THE MEMORY
                 0007 ;IS COMPLETELY TESTED
                 0008 ;
                 0009 ;IF AN ERROR OCCURS,THE PATTERN WILL BE STORED
                 0010 ;AT LOCATION '002C'H AND THE ADDRESS OF THE
                 0011 ;ERROR LOCATION WILL BE STORED AT '002D'H
                 0012 ;AND '002E'H.
                 0013 ;
                 0014 ;THE CONTENTS OF LOCATIONS '000C'H AND '001D'H
                 0015 ;SHOULD BE SELECTED ACCORDING TO THE FOLLOWING
                 0016 ;MEMORY SIZE TESTED
                 0017 ;
                 0018 ;TOP OF MEMORY TO
                 0019 ;BE TESTED                              VALUE OF EPAGE
                 0020 ;
                 0021 ;      4K                                    '10'H
                 0022 ;      8K                                    '20'H
                 0023 ;     16K                                    '40'H
                 0024 ;     32K                                    '80'H
                 0025 ;     48K                                    'C0'H
                 0026 ;     64K                                    'FF'H
                 0027 ;
                 0028 ;THE PROGRAM IS SET UP TO START TESTING AT
                 0029 ;LOCATION '002F'H. THE STARTING ADDRESS FOR THE
                 0030 ;TEST CAN BE MODIFIED BY CHANGING LOCATIONS
                 0031 ;'0003'H-'0004'H AND '0011'H '0012'H.
                 0032 ;
                 0033 ;TEST TIME FOR A 16K BY 8 MEMORY IS APPROX.  4 MIN.
                 0034 ;
                 0035          PSECT    ABS
>0000            0036          ORG      0000H
0000  0600        0037          LD       B,0        ;CLEAR B PATRN MODIFIER
                 0038 ;LOAD UP MEMORY
0002  212F00      0039 LOOP:    LD       HL,START   ;GET STARTING ADDR
0005  7D          0040 FILL:    LD       A,L        ;LOW BYTE TO ACCM
0006  AC          0041          XOR      H          ;XOR WITH HIGH BYTE
0007  A8          0042          XOR      B          ;XOR WITH PATTERN
0008  77          0043          LD       (HL),A     ;STORE IN ADDR
0009  23          0044          INC      HL         ;INCREMENT ADDR
000A  7C          0045          LD       A,H        ;LOAD HIGH BYTE OF ADDR
000B  FE10        0046          CP       EPAGE      ;COMPARE WITH STOP ADDR
000D  C20500      0047          JP       NZ,FILL    ;NOT DONE,GO BACK
                 0048 ;READ AND CHECK TEST DATA
0010  212F00      0049          LD       HL,START;GET START ADDR
0013  7D          0050 TEST:    LD       A,L        ;LOAD LOW BYTE
0014  AC          0051          XOR      H          ;XOR WITH HIGH BYTE
0015  A8          0052          XOR      B          ;XOR WITH MODIFIER
0016  BE          0053          CP       (HL)       ;COMPARE WITH MEMORY LOC
0017  C22500      0054          JP       NZ,EXIT    ;ERROR EXIT
001A  23          0055          INC      HL         ;UPDATE MEMORY ADDR
001B  7C          0056          LD       A,H        ;LOAD HIGH BYTE
001C  FE10        0057          CP       EPAGE      ;COMPARE WITH STOP ADDR
001E  C21300      0058          JP       NZ,TEST    ;LOOP BACK
```

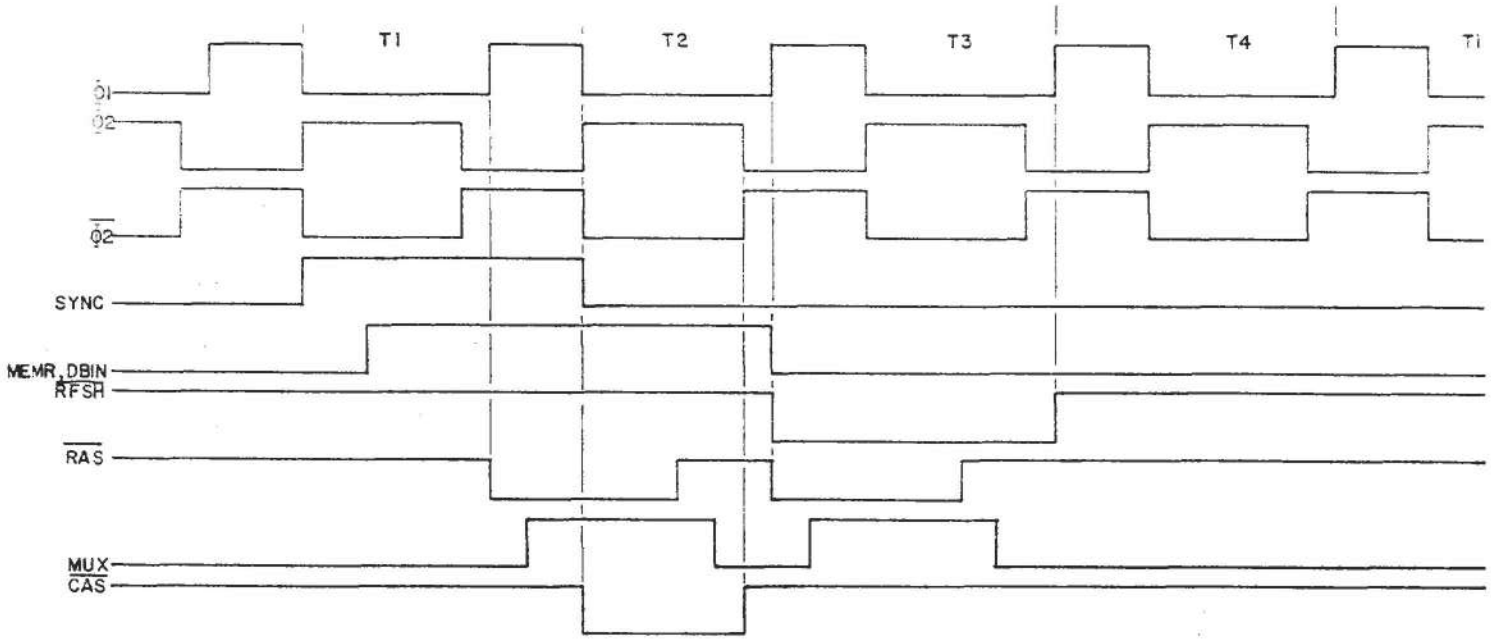
```
ADDR   OBJECT    ST # SOURCE STATEMENT

0021   04        0059          INC     B           ;UPDATE MODIFIER
0022   C30200    0060          JP      LOOP        ;RST WITH NEW MODIFIER
                 0061 ;ERROR EXIT
0025   222D00    0062 EXIT:    LD      (BYTE),HL   ;SAVE ERROR ADDRESS
0028   327C00    0063          LD      (PATRN),A   ;SAVE BAD PATTERN
002B   76        0064          HALT                ;FLAG OPERATOR
>002C            0065 PATRN:   DEFS    1
>002D            0066 BYTE:    DEFS    2
002F   2F00      0067 START:   DEFW    $
0031   3100      0068          DEFW    $           ;PLACE FOR FIRST ADDR
>0010            0069 FPAGE:   EQU     10H         ;SET UP FOR 4K TEST
                 0070          END

ERRORS=0000
```

APPENDIX B

EXPANDORAM TIMING DIAGRAM

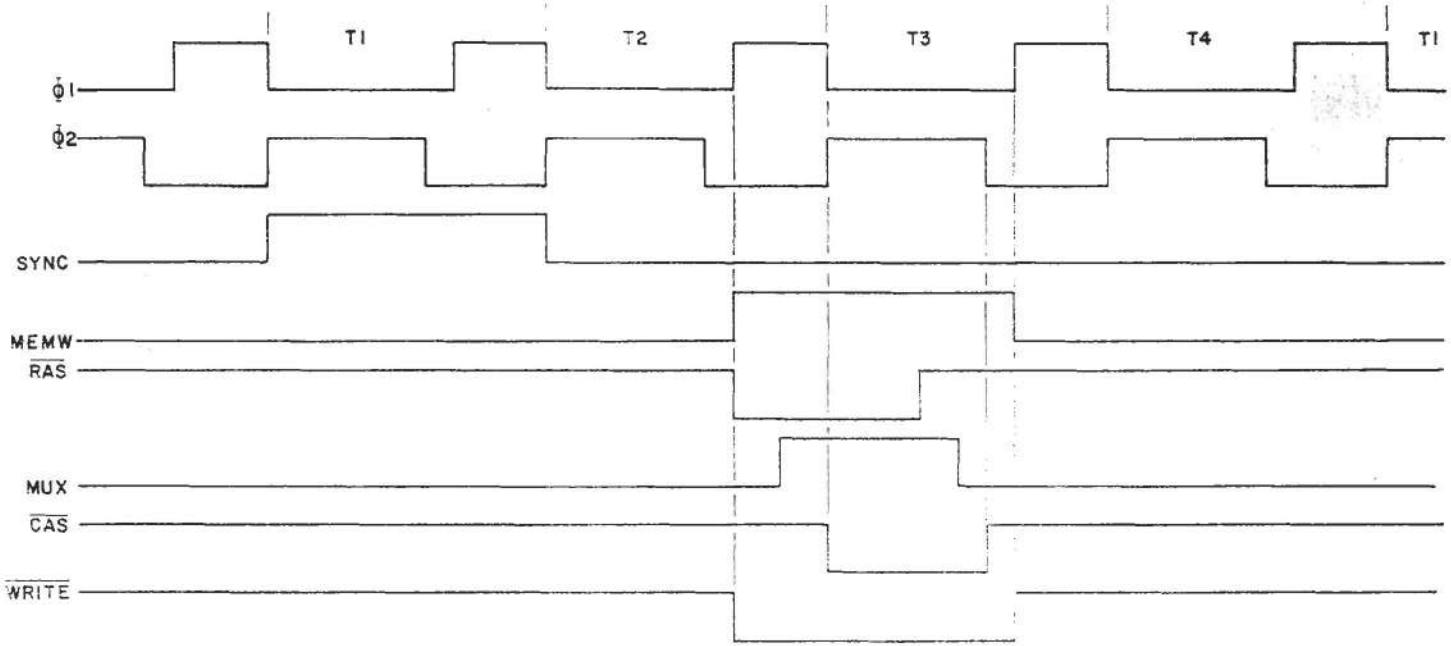


OP CODE FETCH CYCLE (8080 CPU)

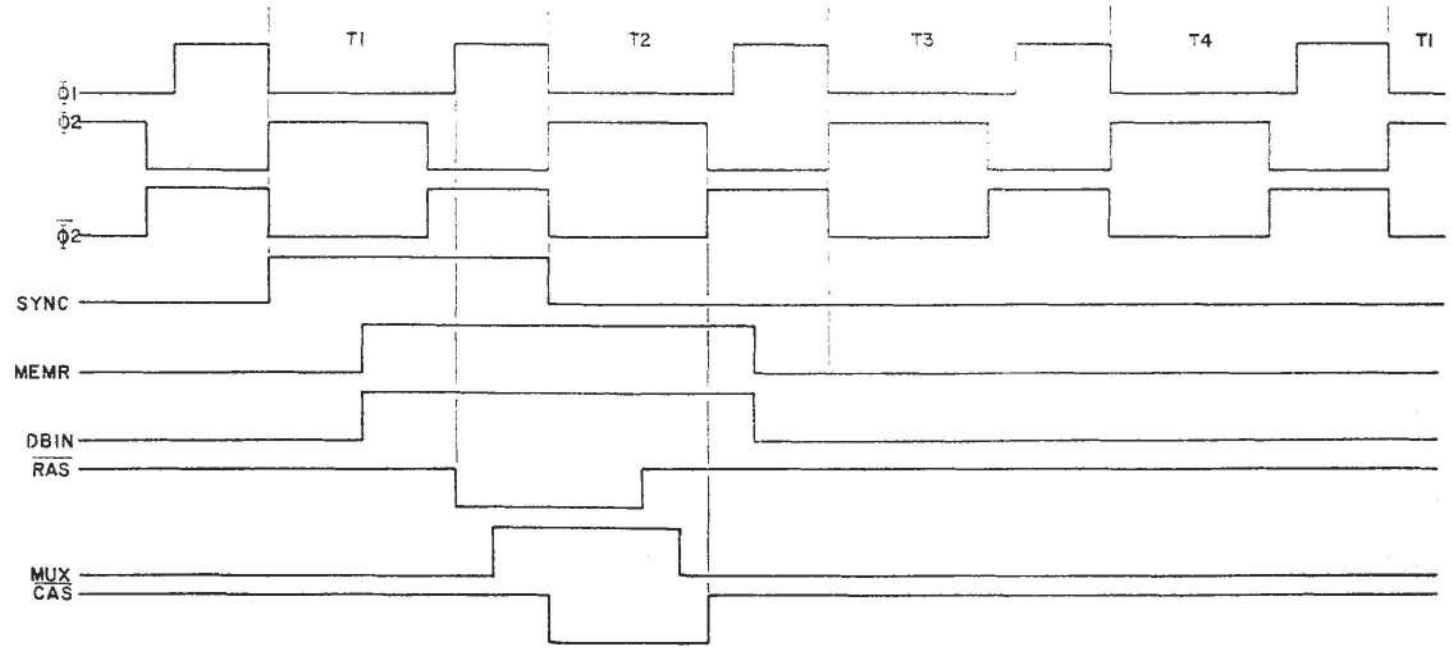


OP CODE FETCH CYCLE (Z80 CPU)

DRAWN JAA	DATE 8/11	SD Systems
CHK'D		P.O. Box 28810 • Dallas, Texas 75228 • 214-271-2561
APP'D		TIMING DIAGRAM FOR EXPANDORAM
RLSD		SCALE NONE · SHEET 1 OF 2 · NO 0100004 · REVISION E



MEMORY WRITE CYCLE (Z80&8080 CPU'S)

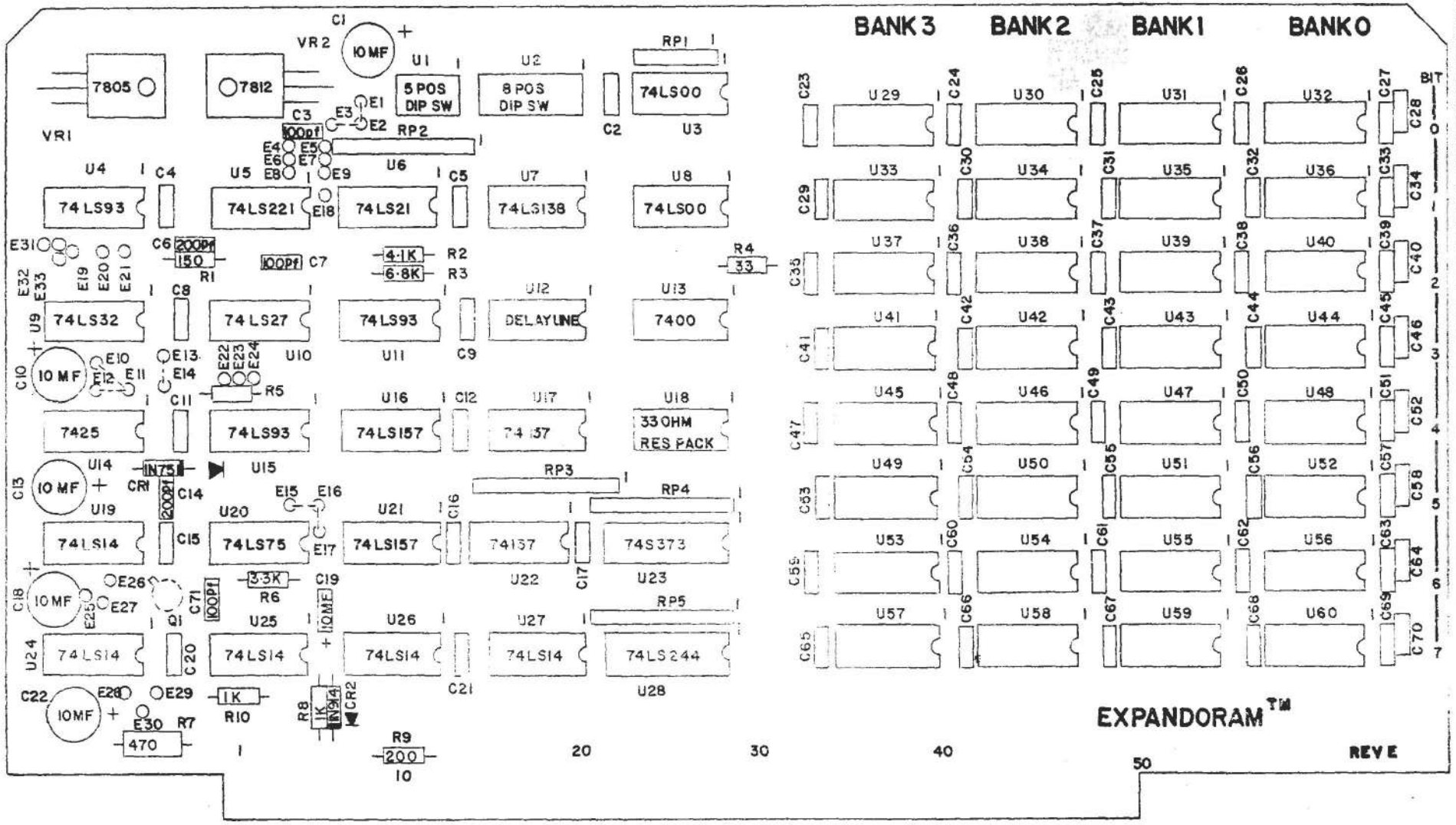


MEMORY READ CYCLE (Z80& 8080 CPU'S)

DRAWN JAA	DATE 8/11	SD Systems P.O. Box 28810 • Dallas, Texas 75228 • 214-271-4867
CHKD		
APPD		TIMING DIAGRAM FOR EXPANDORAM
RLSD		SCALE NONE · SHEET 2 OF 2 · NO. 0100004 · REVISION E

APPENDIX C

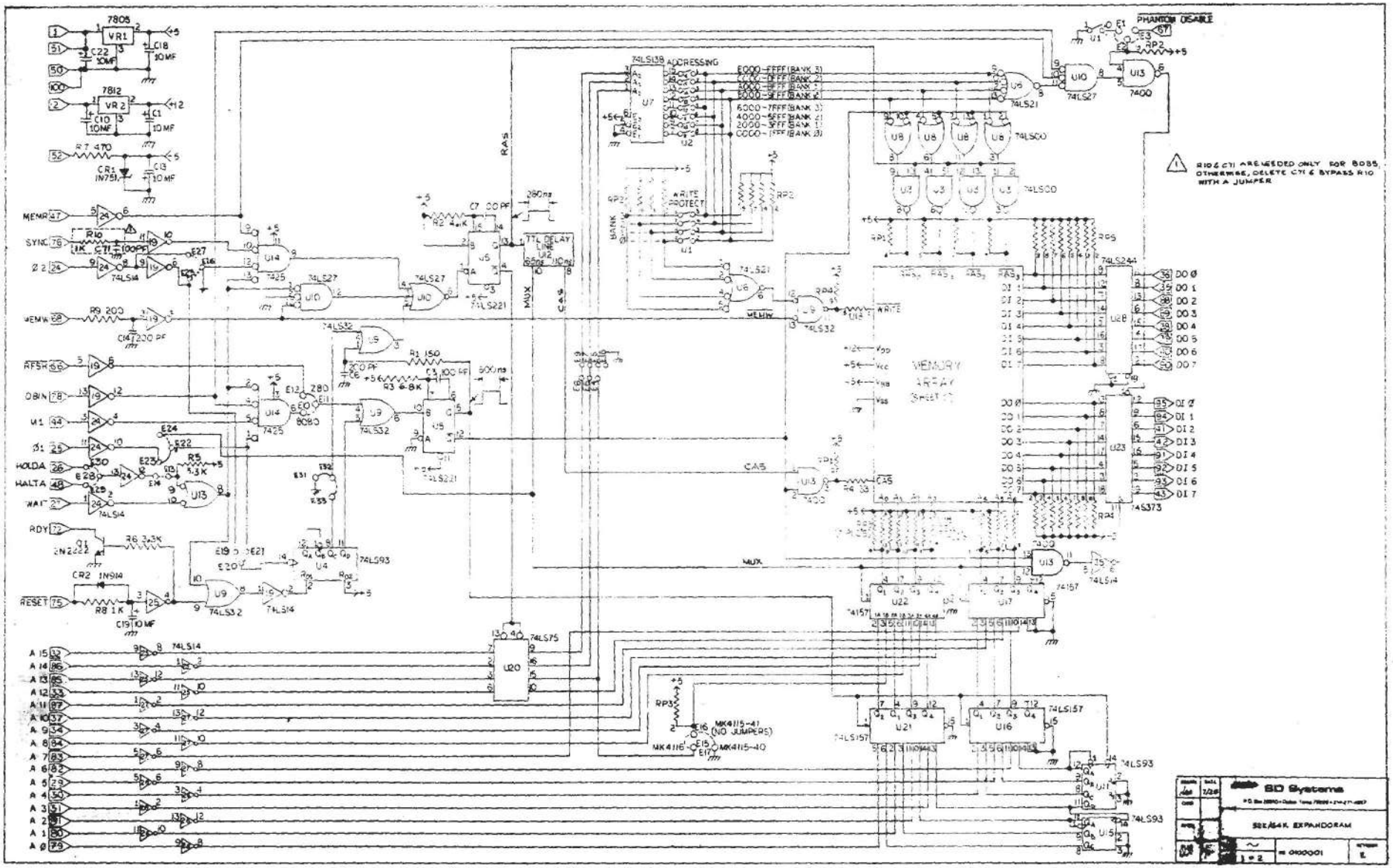
EXPANDORAM PARTS PLACEMENT DRAWING

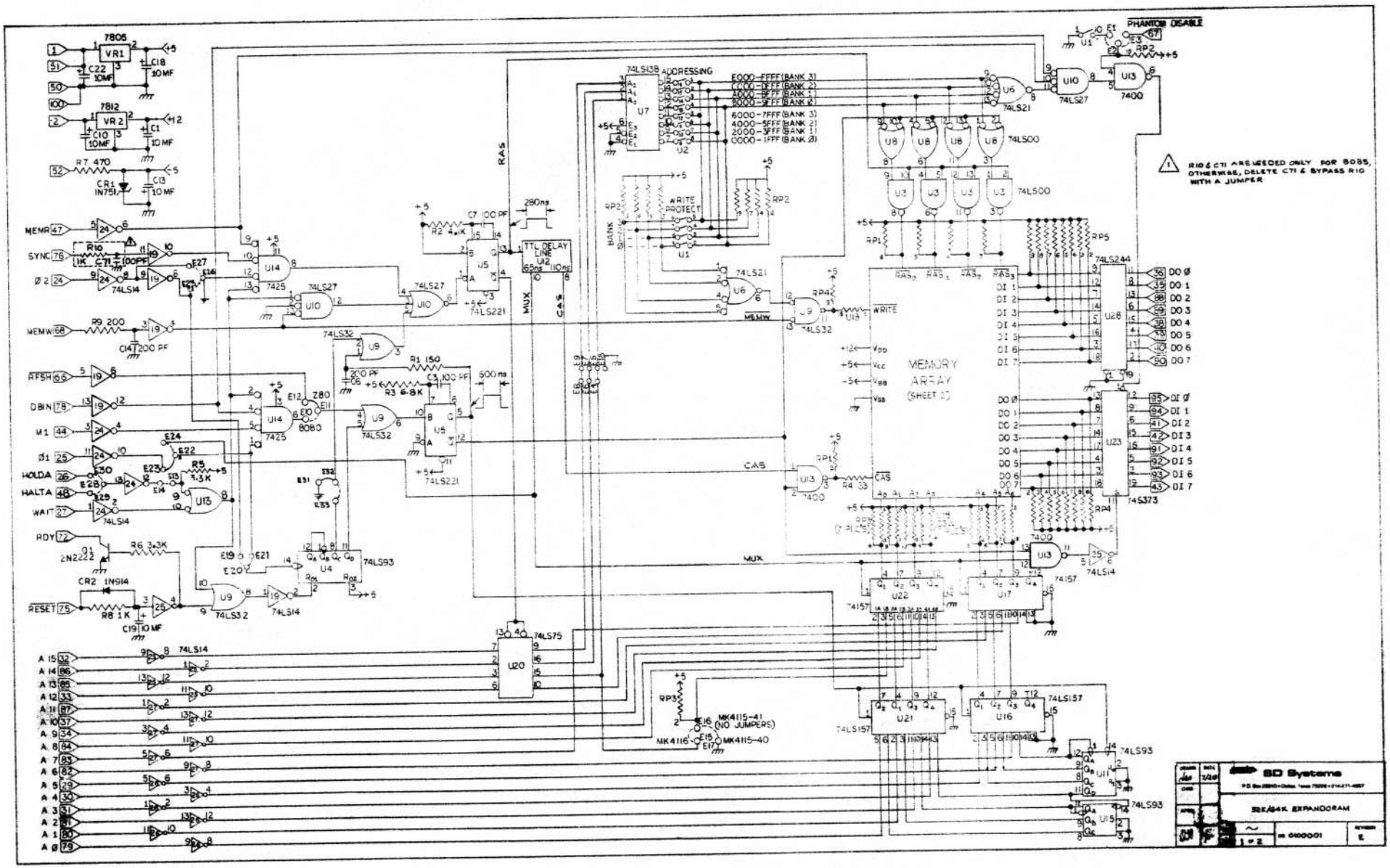


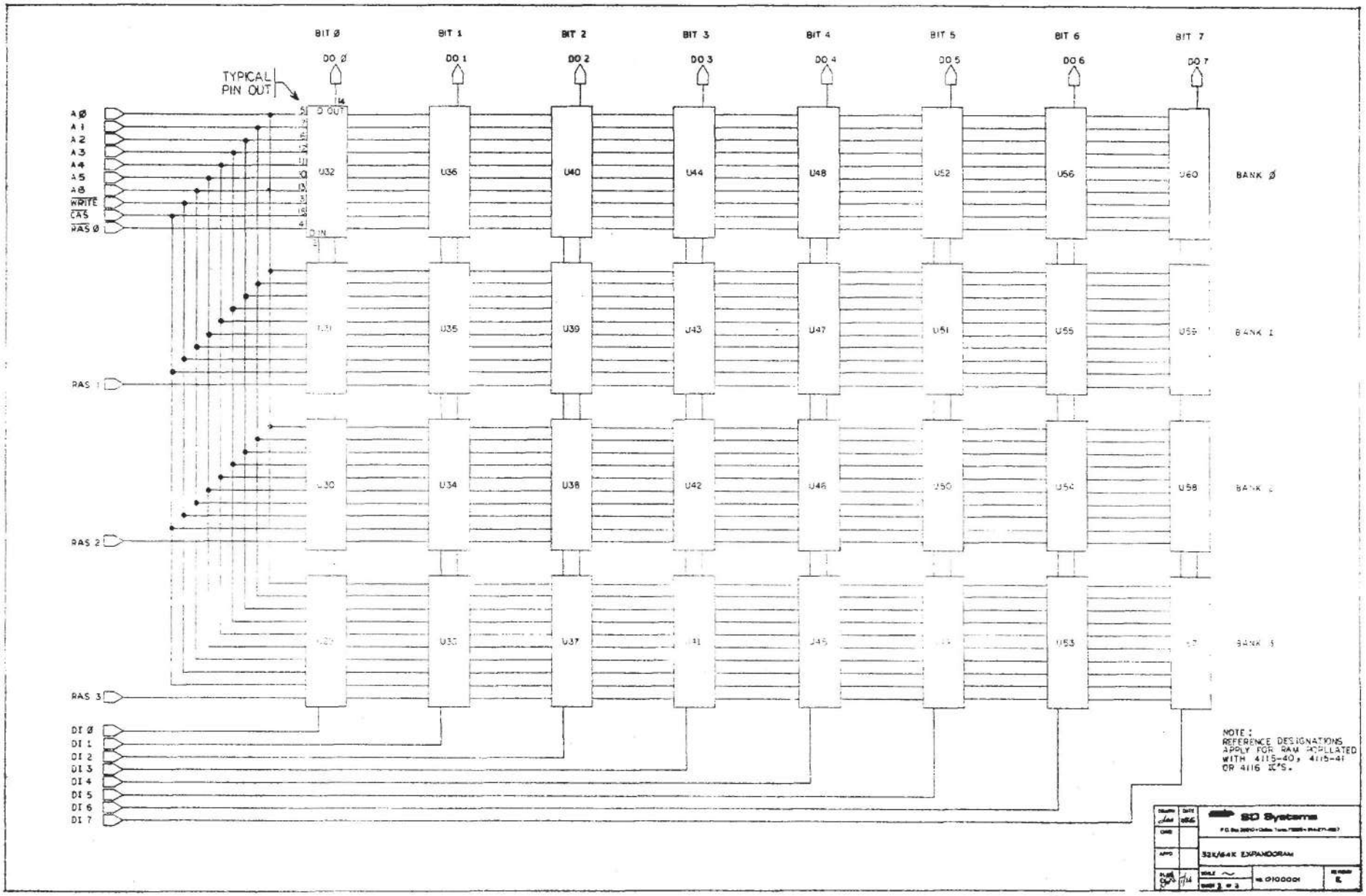
DRAWN JAA	DATE 8/10	SD Systems	
CHKD		P.O. Box 29810 • Dallas, Texas 75229 • 214-271-4667	
APPD		PARTS PLACEMENT DRAWING	
RLSD		SCALE NONE	NO. 0100003
		SHEET 1 OF 1	REVISION E

APPENDIX D

EXPANDORAM SCHEMATIC


7805
7812
VR1
VR2
C22 10MF
C18 10MF
C10 10MF
C1 10MF
C13 10MF
R7 470
CR1 IN751
MEMR
SYNC
Ø2
MEMW
RFSH
OBIN
M1
Ø1
HOLDA
HALTA
WAIT
RDY
Q1 2N2222
R6 3.3K
CR2 IN914
RESET
R8 1K
C19 10MF
R10 1K
C71 100PF
R9 200
C14 200 PF
R1 150
C3 100 PF
R3 6.8K
R5 4.3K
R2 4.7K
C7 .001 MF
280ns
TTL DELAY LINE U2
RAS
MUX
CAS
74LS138 ADDRESSING
E000-EFFF (BANK 3)
C000-DFFF (BANK 2)
A000-BFFF (BANK 1)
8000-9FFF (BANK 0)
6000-7FFF (BANK 3)
4000-5FFF (BANK 2)
2000-3FFF (BANK 1)
0000-1FFF (BANK 0)
WRITE PROTECT
BANK
PHANTOM DISABLE
RP2
RP1
RP3
R104 C71 ARE NEEDED ONLY FOR 8085, OTHERWISE, DELETE C71 & BYPASS R10 WITH A JUMPER
MEMORY ARRAY SHEET 2
WRITE
CAS
MUX
MK4115-41 (NO JUMPERS)
MK4116
MK4115-40
DO Ø
DO 1
DO 2
DO 3
DO 4
DO 5
DO 6
DO 7
DI Ø
DI 1
DI 2
DI 3
DI 4
DI 5
DI 6
DI 7
A 15
A 14
A 13
A 12
A 11
A 10
A 9
A 8
A 7
A 6
A 5
A 4
A 3
A 2
A 1
A Ø
SD Systems
32K/64K EXPANDORAM


7805
VR1
C22 10MF
C18 10MF
7812
VR2
C10 10MF
C1 10MF
R7 470
CR1 IN751
C13 10MF
PHANTOM DISABLE
RP2
74LS138
ADDRESSING
E000-FFFF (BANK 3)
C000-DFFF (BANK 2)
A000-BFFF (BANK 1)
8000-9FFF (BANK 0)
6000-7FFF (BANK 3)
4000-5FFF (BANK 2)
2000-3FFF (BANK 1)
0000-1FFF (BANK 0)
74LS27
74LS21
74LS00
74LS244
74LS373
74LS32
74LS14
74LS93
74LS157
74LS75
7400
7425
8080
RAS
MUX
CAS
WRITE
MEMW
WRITE PROTECT
BANK SELECT
TTL DELAY LINE
MEMORY ARRAY
(SHEET 2)
MEMR
SYNC
Ø2
MEMW
AFSH
DBIN
M1
Ø1
HOLDA
HALTA
WAIT
RDY
RESET
2N2222
CR2 1N914
R10 1K
R9 200
R1 150
R2 4.4K
R3 6.8K
R4 33
R5 1.3K
R6 3.3K
R8 1K
C7 100 PF
C3 100 PF
C6 200 PF
C14 200 PF
C19 10 MF
280ns
500ns
MK4115-41 (NO JUMPERS)
MK4116
MK4115-40
A 15
A 14
A 13
A 12
A 11
A 10
A 9
A 8
A 7
A 6
A 5
A 4
A 3
A 2
A 1
A Ø
DO Ø
DO 1
DO 2
DO 3
DO 4
DO 5
DO 6
DO 7
DI Ø
DI 1
DI 2
DI 3
DI 4
DI 5
DI 6
DI 7
R10 & CT1 ARE NEEDED ONLY FOR 8085, OTHERWISE, DELETE CT1 & BYPASS R10 WITH A JUMPER
SD Systems
32K/64K EXPANDORAM
1 of 2


BIT Ø
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
DO Ø
DO 1
DO 2
DO 3
DO 4
DO 5
DO 6
DO 7
TYPICAL PIN OUT
D OUT
D IN
U32
U36
U40
U44
U48
U52
U56
U60
BANK Ø
U31
U35
U39
U43
U47
U51
U55
U59
BANK 1
U30
U34
U38
U42
U46
U50
U54
U58
BANK 2
U33
U37
U41
U45
U53
BANK 3
A Ø
A 1
A 2
A 3
A 4
A 5
A 8
WRITE
CAS
RAS Ø
RAS 1
RAS 2
RAS 3
DI Ø
DI 1
DI 2
DI 3
DI 4
DI 5
DI 6
DI 7
NOTE:
REFERENCE DESIGNATIONS APPLY FOR RAM POPULATED WITH 4115-40, 4115-41 OR 4116 IC'S.
SD Systems
32K/64K EXPANDORAM

APPENDIX E

EXPANDORAM PARTS LIST

SD Systems

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BILL OF MATERIALS

Title:	PL No.	Rev.
EXPANDORAM, 32K	0100000	E
Date Released:	**Approved:**	**Sheet 1 Of 3**

Item no	Qty	SD-P/N	Description	Unit Cost	Extension
1	6	7030009	10MF,25Volt Min. Tant, C1,C10,C13,C18,C19,C22		
2	2	7030004	100PF 5% Dipped MICA, C3, C7		
3	2	7030005	200PF,5% Dipped MICA C6, C14		
4	60	7030007	.1 MFD, C2,C4,C5,C8,C9,C11,C12,C15,C16,C17,C20,		
			C21, C23-C70		
5	1	7040003	1N751 5V Zener, CR1		
6	1	7040001	1N914 or 1N4148 Silicon Signal, CR2		
7	2	7010160	74LS00, Quad 2 Input NAND Gate, U3, U8		
8	3	7010205	74LS93 4 Bit Binary Counter, U4, U11, U15		
9	1	7010259	74LS221,, Dual Monostable Multiv., U5		
10	1	7010175	74LS21, Dual 4 Input NAND Gate, U6		
11	1	7010219	74LS138, 3 to 8 Line Decoder, U7		
12	1	7010181	74LS32, Quad 2 Input OR Gate, U9		
13	1	7010178	74LS27, Triple 3 Input NOR Gate, U10		
14	1	7010001	7400, Quad 2 Input NAND Gate, U13		
15	1	7010022	7425, Dual 4 Input NOR Gate, U14		
16	2	7010228	74LS157, Quad 2 to 1 Line Selector, U16, U21		
17	2	7010093	74157, Quad 2 to 1 Line Selector, U17, U22		
18	5	7010172	74LS14, Hex Schmitt Trig., U19,U24,U25,U26,U27		
19	1	7010196	74LS75, Quad 4-Bit Latch, U20		
20	1	7010339	74S373, Octal D Latch, U23		
21	1	7010264	74LS244, Octal Buffer, U28		
22	16	7010325	MK 4215 16K X 1 Memory, U29-U60		
23	1	7160001	7805, 5 Volt Regulator VR1		

SD Systems

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BILL OF MATERIALS

Title:	PL No.	Rev.
EXPANDORAM, 32K	0100000	E
Date Released:	**Approved:**	**Sheet** 2 **Of** 3

Item no	Qty	SD-P/N	Description	Unit Cost	Extension
24	1	7160003	7812, 12 Volt Regulator, VR2		
25	1	7020053	150 Ohm ¼W Carbon, R1		
26	1	7020169	4.1K Ohm 1%, 1/8W Metal R2 Film		
27	1	7020170	6.8K Ohm 1%, 1/8W Metal Film R3		
28	1	7020037	33 Ohm ¼W Carbon, R4		
29	2	7020085	3.3K Ohm ¼W Carbon R5, R6		
30	1	7020065	470 Ohm ¼W Carbon R7		
31	1	7020073	1K Ohm ¼W Carbon R8		
32	1	7020056	200 Ohm ¼W Carbon R9		
33	1	7010344	3.3K Ohm 6 Pin SIP, RP1		
34	4	7010345	3.3K Ohm 10 Pin SIP, RP2-RP5		
35	1	7010346	33 Ohm 16 Pin DIP, U18		
36	1	7040005	2N2222 NPN Silicon, Q1		
37	1	7050001	5 Pos. DIP Switch, U1		
38	1	7050002	8 Pos. DIP Switch, U2		
39	1	7010343	TTL Delay Line, DM355, U12		
40	1	7130003	Heat Sink 6106-13		
41	2	7130006	6-32 X 3/8 Screw PPH		
42	2	7130007	6-32 Nut		
43	16	7060002	14 Pin DIP Socket,		
44	40	7060003	16 Pin DIP Socket		
45	2	7060005	20 Pin DIP Socket		
46	9	7170001	Wire Wrap Pins		
47	1	0100002	P. C. Board		

SD Systems

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BILL OF MATERIALS

Title:	PL No.	Rev.
EXPANDORAM, 32K	0100000	E
Date Released:	**Approved:**	**Sheet** 3 **Of** 3

Item No	Qty	SD-P/N	Description	Unit Cost	Extension
48	1	7020073	Resistor, 1K, ¼W, 5% R10 (Optional)		
49	1	7030004	Capacitor, 100PF, 5% Dipped MICA, C71 (Optional)		