

ATTACHMENT

Procedure to upgrade Rev D ExpandoRAM II boards to 256Kbyte capacity.

To use the ExpandoRAM II board with the 64K-bit IC's in an SD-OS environment, the following modifications to the board must be made:

1. Cut the etch between E17 and E16.
2. Cut the etch between E1 and E2.
3. Cut the etch between E4 and E5.
4. Cut the etch between E6 and E8.
5. Install a jumper between E17 and E18.
6. Install a jumper between E2 and E3.
7. Install a jumper between E6 and E7.
8. Remove all of the filter capacitors connected to pin 9 of the RAM chips (quantity 8, C57 thru C64). Unsoldering is recommended.
9. Install the new PROM (EX64-48) at location U8.

To use a COSMOS system with 48K byte partitions and with more than 4 users on the RAM II with 64K chips, the following additional mods must be made:

1. Cut the etch connected to pin 32 of the S-100 bus connector.
2. Cut the etch connected from pin 11 of U24 to pin 13 of U18.
3. Remove jumper installed in step 5 above.
4. Install a 74LS32 IC close to or under location U18.
5. Hook pin 14 of the 74SL32 to pin 14 of U18.
6. Hook pin 7 of the 74LS32 to pin 7 of U18.
7. Hook pin 1 of the 74LS32 to pin 1 of U18.
8. Hook pin 13 of the 74LS32 to pin 13 of U18.
9. Hook pin 2 of the 74LS32 to pin 12 of the 74LS32.

ATTACHMENT - (Continued)

10. Hook pin 32 of the S100 bus to pin 13 of the 74LS32.
11. Hook pin 2 of the 74LS32 to pin 7 of U13.
12. Hook pin 3 of the 74LS32 to pin 4 of U24.
13. Hook pin 11 of the 74LS32 to pin 11 of U24.

DESCRIPTION

The 82S130 and 82S131 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S130 and 82S131 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S130 and 82S131 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0° to +75°C) specify N82S130/131, F or N, and for the military temperature range (-55° C to +125° C) specify S82S130/131, F.

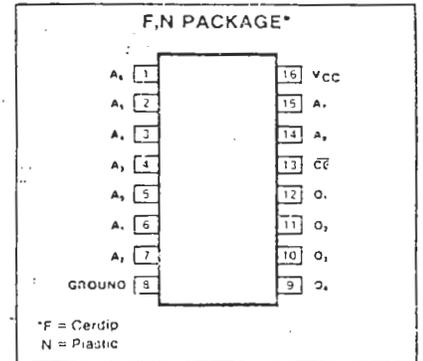
FEATURES

- Address access time:
N82S130/131: 50ns max
S82S130/131: 70ns max
- Power dissipation: 0.3mW/bit typ
- Input loading:
N82S130/131: -100µA max
S82S130/131: -150µA max
- On-chip address decoding
- Output options:
82S130: Open collector
82S131: Tri-state
- No separate fusing pins
- Unprogrammed outputs are low level
- Fully TTL compatible

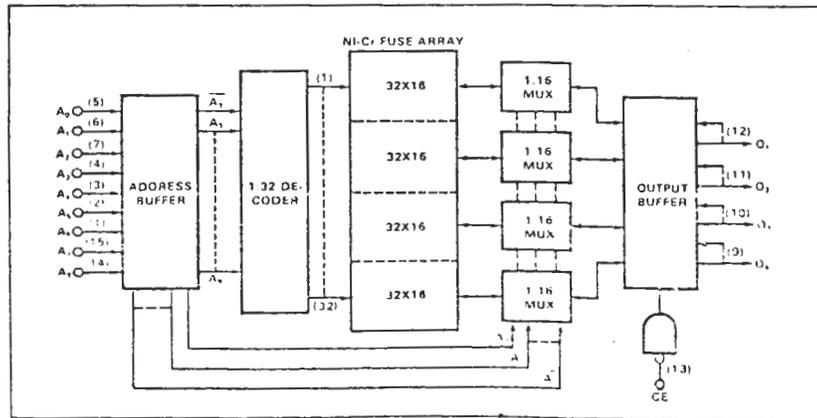
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	Vdc
V _{IN} Input voltage	+5.5	Vdc
V _{OH} Output voltage		Vdc
V _{OH} High (82S130)	+5.5	
V _O Off-state (82S131)	+5.5	
T _A Operating Temperature range		°C
T _A Operating N82S130/131	0 to +75	
T _A Operating S82S130/131	-55 to -125	
T _{STG} Storage	-65 to -150	

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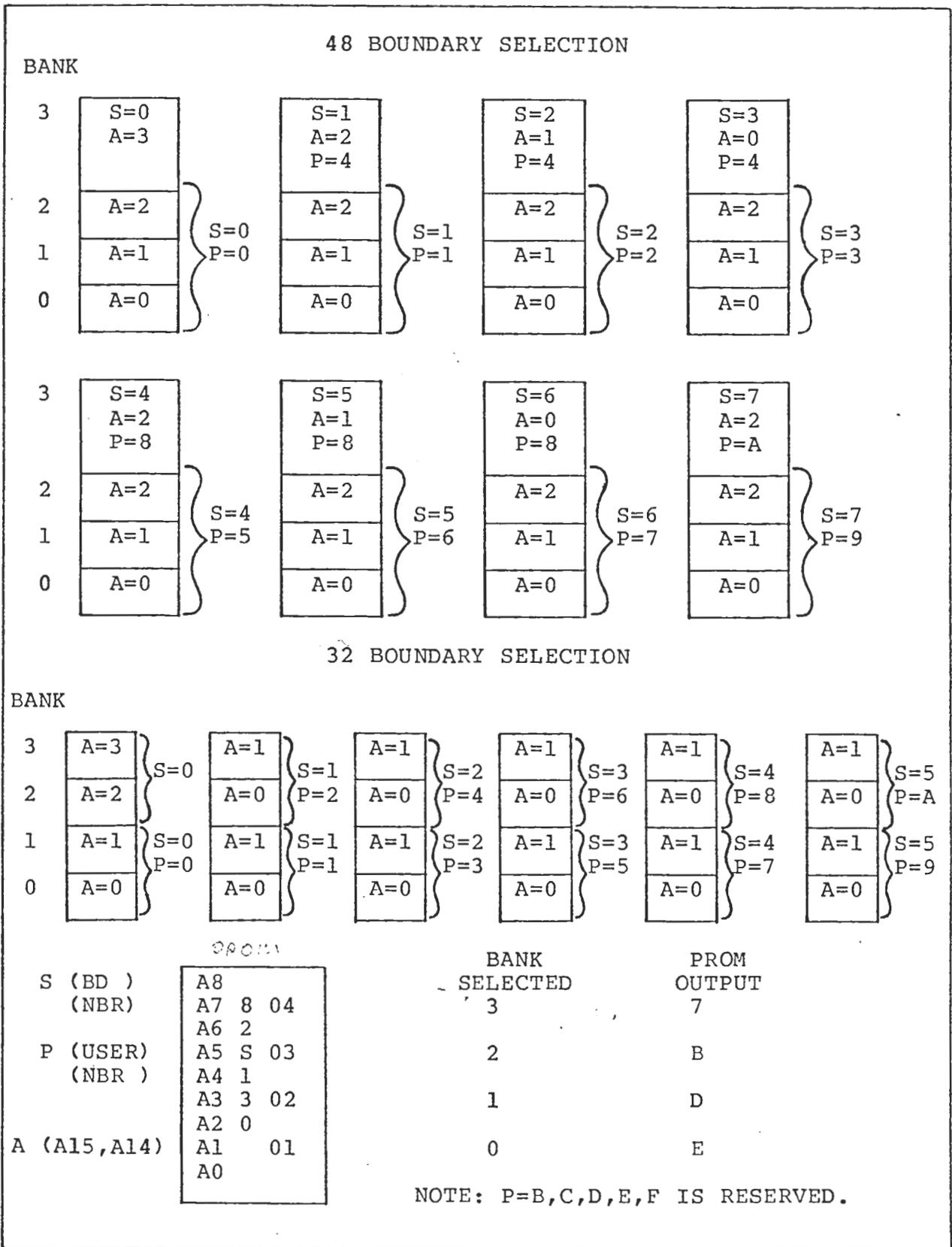


Figure 2-4. PROM Program and Page Mapping.

INTEL PROMs FROM HAMILTON/AVNET

48K BOUNDARIES

STANDARD MEMORY TRUTH TABLE

LSB (ADDRESS) = PIN _____

LSB (OUTPUT) = PIN _____

corresponds to column B0, row 1 to column B1, etc. In using this form specify a program, simply punch the appropriate row and column for each logical "1" in the rotated truth table. (Keep in mind that column 1 on the card corresponds to word 0 on the form, column 2 to word 1, etc.)

For purposes of standardization, the definitions of Logical "1's" and "0's" are as follows:

"1" = H = P (Relatively more positive voltage.)
 "0" = L = N (Relatively less positive voltage.)

If further information is needed, contact your nearest Hamilton/Avnet location, or TWX 910-340-7080.

INSTRUCTIONS

The "Standard Memory Truth Table" is designed to accommodate word sizes ranging from 1 to 8 bits per word. Any number of words can be specified simply by using additional forms and providing the proper information in the Memory Organization. (For additional protection from errors the proper word number should be written in the margin to the left of the printed word number for each added page.)

The layout of each section provides a convenient means for converting the truth table to a punched card format. By rotating form 90° CCW, each section will correspond to the first 64 columns of an 80 column card, where row 0

WORD NO.	SECTION A DATA				4 B3	3 B2	2 B1	1 B0	CARD PUNCH
	S	P	A	DATA					
0	0	0	0	7	0	1	1	1	1
1	0	0	0	7	0	1	1	1	2
2	0	0	0	7	1	0	1	1	3
3	0	0	0	7	1	0	1	1	4
4	0	0	0	7	1	0	1	1	5
5	0	0	0	7	1	0	1	1	6
6	0	0	0	7	1	0	1	1	7
7	0	0	0	7	1	0	1	1	8
8	0	0	0	7	1	0	1	1	9
9	0	0	0	7	1	0	1	1	10
10	0	0	0	7	1	0	1	1	11
11	0	0	0	7	1	0	1	1	12
12	0	0	0	7	1	0	1	1	13
13	0	0	0	7	1	0	1	1	14
14	0	0	0	7	1	0	1	1	15
15	0	0	0	7	1	0	1	1	16
16	0	0	0	7	1	0	1	1	17
17	0	0	0	7	1	0	1	1	18
18	0	0	0	7	1	0	1	1	19
19	0	0	0	7	1	0	1	1	20
20	0	0	0	7	1	0	1	1	21
21	0	0	0	7	1	0	1	1	22
22	0	0	0	7	1	0	1	1	23
23	0	0	0	7	1	0	1	1	24
24	0	0	0	7	1	0	1	1	25
25	0	0	0	7	1	0	1	1	26
26	0	0	0	7	1	0	1	1	27
27	0	0	0	7	1	0	1	1	28
28	0	0	0	7	1	0	1	1	29
29	0	0	0	7	1	0	1	1	30
30	0	0	0	7	1	0	1	1	31
31	0	0	0	7	1	0	1	1	32
32	0	0	0	7	1	0	1	1	33
33	0	0	0	7	1	0	1	1	34
34	0	0	0	7	1	0	1	1	35
35	0	0	0	7	1	0	1	1	36
36	0	0	0	7	1	0	1	1	37
37	0	0	0	7	1	0	1	1	38
38	0	0	0	7	1	0	1	1	39
39	0	0	0	7	1	0	1	1	40
40	0	0	0	7	1	0	1	1	41
41	0	0	0	7	1	0	1	1	42
42	0	0	0	7	1	0	1	1	43
43	0	0	0	7	1	0	1	1	44
44	0	0	0	7	1	0	1	1	45
45	0	0	0	7	1	0	1	1	46
46	0	0	0	7	1	0	1	1	47
47	0	0	0	7	1	0	1	1	48
48	0	0	0	7	1	0	1	1	49
49	0	0	0	7	1	0	1	1	50
50	0	0	0	7	1	0	1	1	51
51	0	0	0	7	1	0	1	1	52
52	0	0	0	7	1	0	1	1	53
53	0	0	0	7	1	0	1	1	54
54	0	0	0	7	1	0	1	1	55
55	0	0	0	7	1	0	1	1	56
56	0	0	0	7	1	0	1	1	57
57	0	0	0	7	1	0	1	1	58
58	0	0	0	7	1	0	1	1	59
59	0	0	0	7	1	0	1	1	60
60	0	0	0	7	1	0	1	1	61
61	0	0	0	7	1	0	1	1	62
62	0	0	0	7	1	0	1	1	63
63	0	0	0	7	1	0	1	1	64

WORD NO.	SECTION B DATA				4 B3	3 B2	2 B1	1 B0	CARD PUNCH
	S	P	A	DATA					
64	1	0	0	F					1
65	1	0	0	F					2
66	1	0	0	F					3
67	1	0	0	F					4
68	1	0	0	F					5
69	1	0	0	F					6
70	1	0	0	F					7
71	1	0	0	F					8
72	1	0	0	F					9
73	1	0	0	F					10
74	1	0	0	F					11
75	1	0	0	F					12
76	1	0	0	F					13
77	1	0	0	F					14
78	1	0	0	F					15
79	1	0	0	F					16
80	1	0	0	F					17
81	1	0	0	F					18
82	1	0	0	F					19
83	1	0	0	F					20
84	1	0	0	F					21
85	1	0	0	F					22
86	1	0	0	F					23
87	1	0	0	F					24
88	1	0	0	F					25
89	1	0	0	F					26
90	1	0	0	F					27
91	1	0	0	F					28
92	1	0	0	F					29
93	1	0	0	F					30
94	1	0	0	F					31
95	1	0	0	F					32
96	1	0	0	F					33
97	1	0	0	F					34
98	1	0	0	F					35
99	1	0	0	F					36
100	1	0	0	F					37
101	1	0	0	F					38
102	1	0	0	F					39
103	1	0	0	F					40
104	1	0	0	F					41
105	1	0	0	F					42
106	1	0	0	F					43
107	1	0	0	F					44
108	1	0	0	F					45
109	1	0	0	F					46
110	1	0	0	F					47
111	1	0	0	F					48
112	1	0	0	F					49
113	1	0	0	F					50
114	1	0	0	F					51
115	1	0	0	F					52
116	1	0	0	F					53
117	1	0	0	F					54
118	1	0	0	F					55
119	1	0	0	F					56
120	1	0	0	F					57
121	1	0	0	F					58
122	1	0	0	F					59
123	1	0	0	F					60
124	1	0	0	F					61
125	1	0	0	F					62
126	1	0	0	F					63
127	1	0	0	F					64

LSB (ADDRESS) = PIN _____

LSB (OUTPUT) = PIN _____

STANDARD MEMORY TRUTH TABLE

<p>CUSTOMER NAME _____</p> <p>CUSTOMER PART NO. _____</p> <p>MEMORY ORGANIZATION: _____</p> <p>WORDS _____ AND _____ THRU _____</p> <p>BUYER'S NAME _____</p> <p>PROGRAMMERS NAME _____</p> <p>PURCHASE ORDER NO. _____</p> <p>MANUFACTURER'S PART NO. _____</p> <p>SPECIAL MARKING (IF ANY) _____</p>	<p>PHONE _____</p> <p>REV. _____</p> <p>BITS/WORD _____</p> <p>SPECIFIED ON THIS PAGE _____</p>
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WORD NO.	SECTION A DATA				CARD PUNCH
	S	P	A	DATA	
128	0	0	0	F	1
129	0	0	1	F	1
130	0	0	2	F	1
131	0	0	3	F	1
132	0	0	4	F	1
133	0	0	5	F	1
134	0	0	6	F	1
135	0	0	7	F	1
136	0	1	0	F	1
137	0	1	1	F	1
138	0	1	2	F	1
139	0	1	3	F	1
140	0	1	4	F	1
141	0	1	5	F	1
142	0	1	6	F	1
143	0	1	7	F	1
144	0	2	0	F	1
145	0	2	1	F	1
146	0	2	2	B	1
147	0	2	3	B	1
148	0	2	4	D	1
149	0	2	5	D	1
150	0	2	6	E	1
151	0	2	7	E	1
152	0	3	0	F	1
153	0	3	1	F	1
154	0	3	2	F	1
155	0	3	3	F	1
156	0	3	4	F	1
157	0	3	5	F	1
158	0	3	6	F	1
159	0	3	7	F	1
160	0	4	0	F	1
161	0	4	1	F	1
162	0	4	2	F	1
163	0	4	3	F	1
164	0	4	4	F	1
165	0	4	5	F	1
166	0	4	6	F	1
167	0	4	7	F	1
168	0	5	0	F	1
169	0	5	1	F	1
170	0	5	2	F	1
171	0	5	3	F	1
172	0	5	4	F	1
173	0	5	5	F	1
174	0	5	6	F	1
175	0	5	7	F	1
176	0	6	0	F	1
177	0	6	1	F	1
178	0	6	2	F	1
179	0	6	3	F	1
180	0	6	4	F	1
181	0	6	5	F	1
182	0	6	6	F	1
183	0	6	7	F	1
184	0	7	0	F	1
185	0	7	1	F	1
186	0	7	2	F	1
187	0	7	3	F	1
188	0	7	4	F	1
189	0	7	5	F	1
190	0	7	6	F	1
191	0	7	7	F	1

WORD NO.	SECTION B DATA				CARD PUNCH
	S	P	A	DATA	
192	0	0	0	F	1
193	0	0	1	F	1
194	0	0	2	F	1
195	0	0	3	F	1
196	0	0	4	F	1
197	0	0	5	F	1
198	0	0	6	F	1
199	0	0	7	F	1
200	0	1	0	F	1
201	0	1	1	F	1
202	0	1	2	F	1
203	0	1	3	F	1
204	0	1	4	F	1
205	0	1	5	F	1
206	0	1	6	F	1
207	0	1	7	F	1
208	0	2	0	F	1
209	0	2	1	F	1
210	0	2	2	F	1
211	0	2	3	F	1
212	0	2	4	F	1
213	0	2	5	F	1
214	0	2	6	F	1
215	0	2	7	F	1
216	0	3	0	F	1
217	0	3	1	F	1
218	0	3	2	F	1
219	0	3	3	F	1
220	0	3	4	F	1
221	0	3	5	F	1
222	0	3	6	F	1
223	0	3	7	F	1
224	0	4	0	F	1
225	0	4	1	F	1
226	0	4	2	F	1
227	0	4	3	F	1
228	0	4	4	F	1
229	0	4	5	F	1
230	0	4	6	F	1
231	0	4	7	F	1
232	0	5	0	F	1
233	0	5	1	F	1
234	0	5	2	F	1
235	0	5	3	F	1
236	0	5	4	F	1
237	0	5	5	F	1
238	0	5	6	F	1
239	0	5	7	F	1
240	0	6	0	F	1
241	0	6	1	F	1
242	0	6	2	F	1
243	0	6	3	F	1
244	0	6	4	F	1
245	0	6	5	F	1
246	0	6	6	F	1
247	0	6	7	F	1
248	0	7	0	F	1
249	0	7	1	F	1
250	0	7	2	F	1
251	0	7	3	F	1
252	0	7	4	F	1
253	0	7	5	F	1
254	0	7	6	F	1
255	0	7	7	F	1

INTEL PROMS FROM HAMILTON/AVNET

LSB (ADDRESS) = PIN _____

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STANDARD MEMORY TRUTH TABLE

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The layout of each section provides a convenient means for converting the truth table to a punched card format. By rotating form 90° CCW, each section will correspond to the first 64 columns of an 80 column card, where row 0

corresponds to column B0, row 1 to column B1, etc. In using this format specify a program, simply punch the appropriate row and column for each logical "1" in the related truth table. (Keep in mind that column 1 on the card corresponds to word 0 on the form, column 2 to word 1, etc.)

For purposes of standardization, the definitions of Logical "1's" and "0's" are as follows:
 "1" = H = P = (Relatively more positive voltage.)
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If further information is needed, contact your nearest Hamilton/Avnet location, or TWX 910-340-7080.

WORD NO.	SECTION A DATA				SECTION B DATA				CARD PUNCH
	S	P	A	DATA	4 B3	3 B2	2 B1	1 B0	
256	4	0	0	F	1	1	1	1	1
257	4	0	1	F					
258	4	0	2	F					
259	4	0	3	F					
260	4	0	4	F					
261	4	0	5	F					
262	4	0	6	F					
263	4	0	7	F					
264	4	1	0	F					
265	4	1	1	F					
266	4	1	2	F					
267	4	1	3	F					
268	4	1	4	F					
269	4	1	5	F					
270	4	1	6	F					
271	4	1	7	F					
272	4	2	0	F					
273	4	2	1	F					
274	4	2	2	F					
275	4	2	3	F					
276	4	2	4	F					
277	4	2	5	F					
278	4	2	6	F					
279	4	2	7	F					
280	4	3	0	F					
281	4	3	1	F					
282	4	3	2	F					
283	4	3	3	F					
284	4	3	4	F					
285	4	3	5	F					
286	4	3	6	F					
287	4	3	7	F					
288	4	4	0	F					
289	4	4	1	F					
290	4	4	2	F					
291	4	4	3	F					
292	4	4	4	F					
293	4	4	5	F					
294	4	4	6	F					
295	4	4	7	F					
296	4	5	0	F					
297	4	5	1	F	1	1	1	1	
298	4	5	2	F	1	0	1	1	
299	4	5	3	F	1	0	1	1	
300	4	5	4	F	1	1	0	1	
301	4	5	5	F	1	1	0	1	
302	4	5	6	F	1	1	1	0	
303	4	5	7	F	1	1	1	0	
304	4	6	0	F	1	1	1	1	
305	4	6	1	F					
306	4	6	2	F					
307	4	6	3	F					
308	4	6	4	F					
309	4	6	5	F					
310	4	6	6	F					
311	4	6	7	F					
312	4	7	0	F					
313	4	7	1	F					
314	4	7	2	F					
315	4	7	3	F					
316	4	7	4	F					
317	4	7	5	F					
318	4	7	6	F					
319	4	7	7	F	1	1	1	1	

WORD NO.	SECTION B DATA				SECTION A DATA				CARD PUNCH
	S	P	A	DATA	4 B3	3 B2	2 B1	1 B0	
320	5	0	0	F					
321	5	0	1	F					
322	5	0	2	F					
323	5	0	3	F					
324	5	0	4	F					
325	5	0	5	F					
326	5	0	6	F					
327	5	0	7	F					
328	5	1	0	F					
329	5	1	1	F					
330	5	1	2	F					
331	5	1	3	F					
332	5	1	4	F					
333	5	1	5	F					
334	5	1	6	F					
335	5	1	7	F					
336	5	2	0	F					
337	5	2	1	F					
338	5	2	2	F					
339	5	2	3	F					
340	5	2	4	F					
341	5	2	5	F					
342	5	2	6	F					
343	5	2	7	F					
344	5	3	0	F					
345	5	3	1	F					
346	5	3	2	F					
347	5	3	3	F					
348	5	3	4	F					
349	5	3	5	F					
350	5	3	6	F					
351	5	3	7	F					
352	5	4	0	F					
353	5	4	1	F					
354	5	4	2	F					
355	5	4	3	F					
356	5	4	4	F					
357	5	4	5	F					
358	5	4	6	F					
359	5	4	7	F					
360	5	5	0	F					
361	5	5	1	F					
362	5	5	2	F					
363	5	5	3	F					
364	5	5	4	F					
365	5	5	5	F					
366	5	5	6	F					
367	5	5	7	F					
368	5	6	0	F					
369	5	6	1	F	1	1	1	1	
370	5	6	2	F	1	0	1	1	
371	5	6	3	F	1	0	1	1	
372	5	6	4	F	1	1	0	1	
373	5	6	5	F	1	1	0	1	
374	5	6	6	F	1	1	1	0	
375	5	6	7	F	1	1	1	0	
376	5	7	0	F	1	1	1	1	
377	5	7	1	F					
378	5	7	2	F					
379	5	7	3	F					
380	5	7	4	F					
381	5	7	5	F					
382	5	7	6	F					
383	5	7	7	F	1	1	1	1	

64 KRAMS

POWER (TYP)

CURRENT (MAX)

	OPER	STANDBY	Memory	Rfslcy	STROBE
* TI 4164	125mw (typ)	17.5mw (typ)	37mA	32mA	5mA
		64KSYS	296mA	256mA	40mA
		256KSYS	1184mA	1024mA	160mA
105TEK					
4564	300mw	22mw	54mA	45mA	4mA
		64KSYS	432mA	360mA	32mA
		256KSYS	1728mA	1440mA	128mA
105TEK					
4164	330mw	22mw	60mA		4
		64KSYS	480mA		32mA
		256KSYS	1920mA		128mA
* schi					
4864	330mw	20mw	60mA	4.5mA	3.5mA
		64KSYS	480mA	36mA	28mA
		256KSYS	1920mA	144mA	112mA
Artima					
umc4164	250mw		45mA	35mA	4mA
		64KSYS	360mA	280mA	32mA
		256KSYS	1440mA	1120mA	128mA

* MCM6665 L20

* IEC 4164D

OKI

284 MW/CHIP @ 5V
 PERROTT ASSOC
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