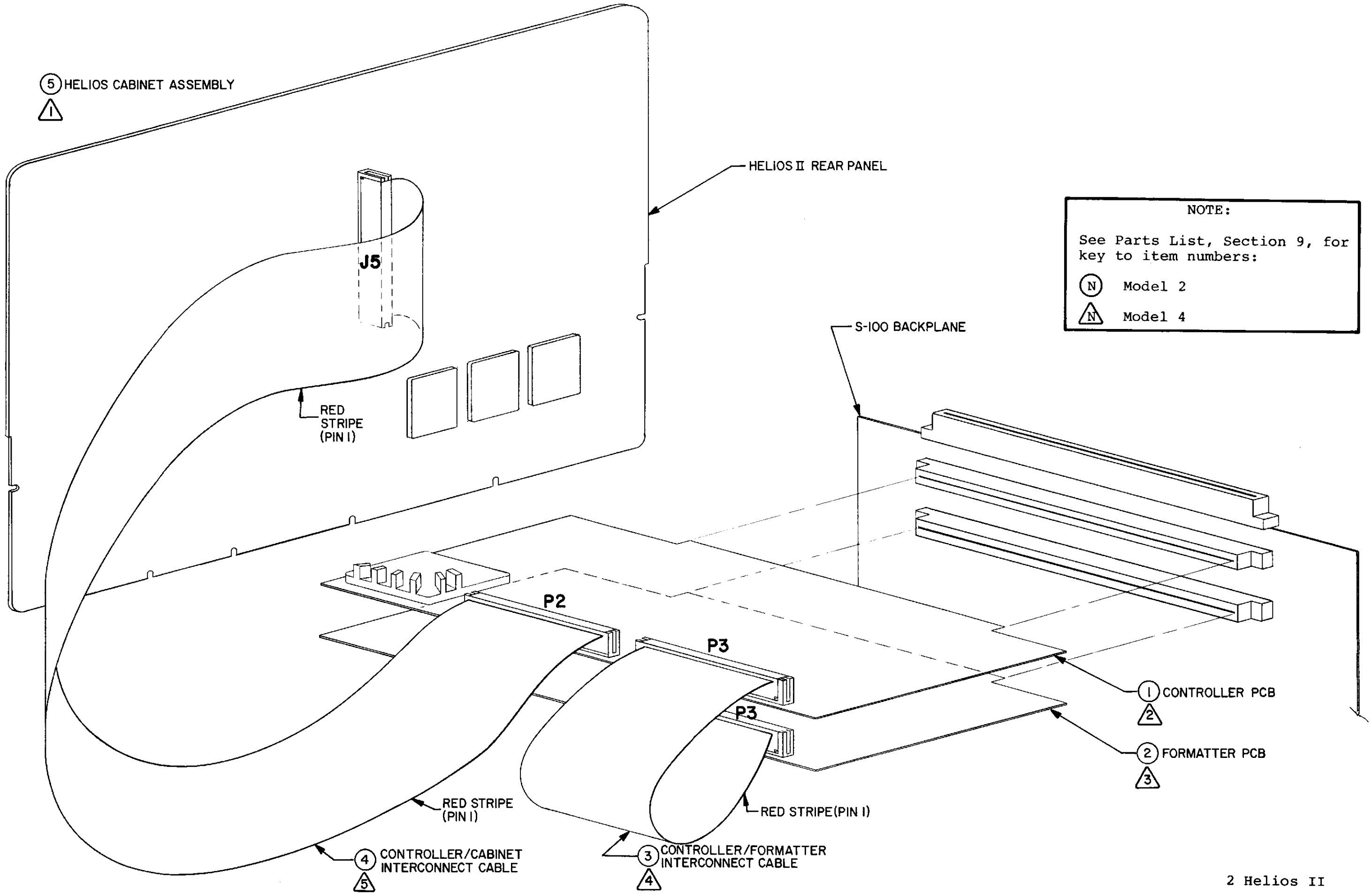



NOTE:

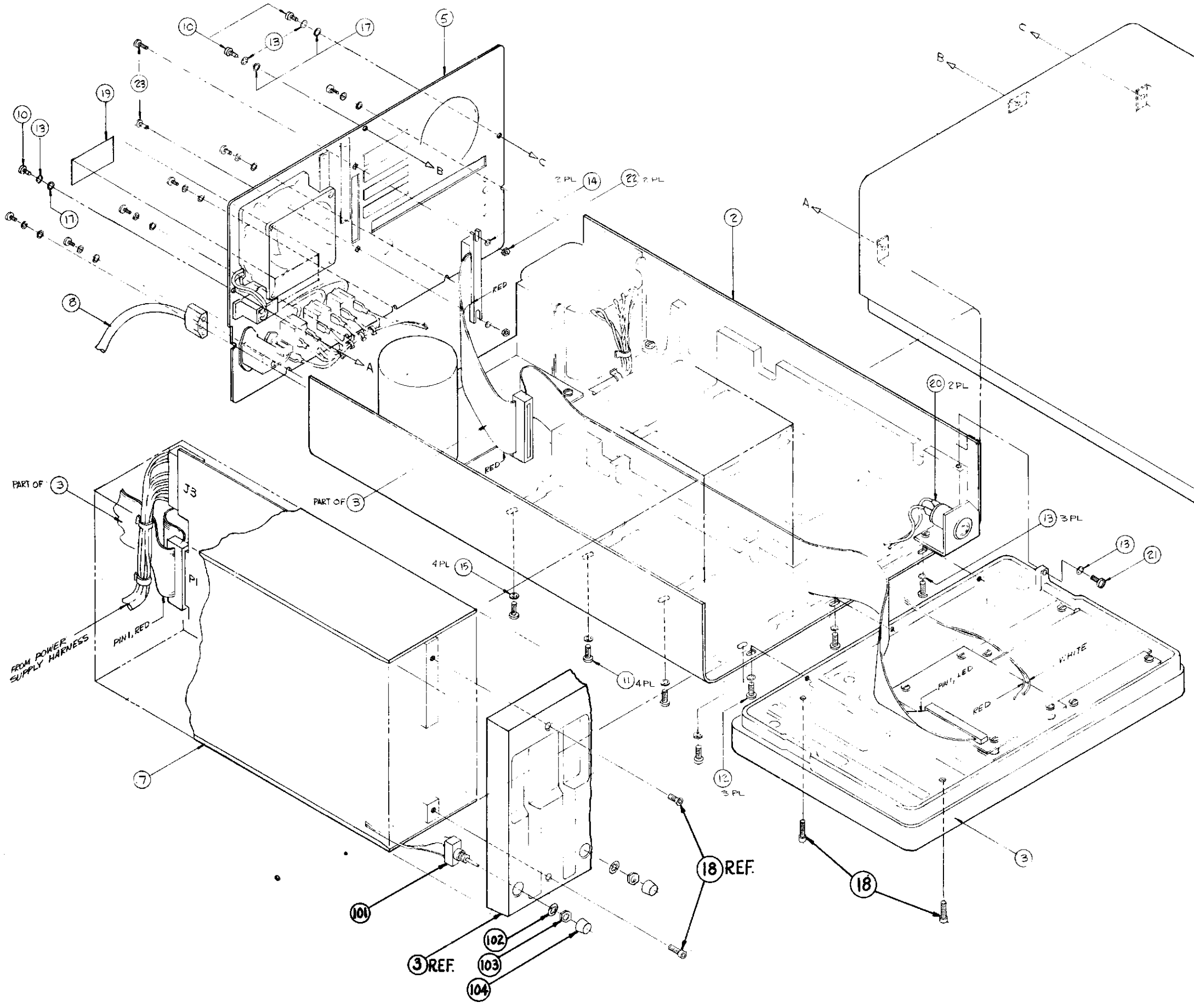
See Parts List, Section 9, for key to item numbers:

(N) Model 2

△N Model 4

2 Helios II

Fig. 8-1 System Assembly, Interconnect Diagram (I-2-78)



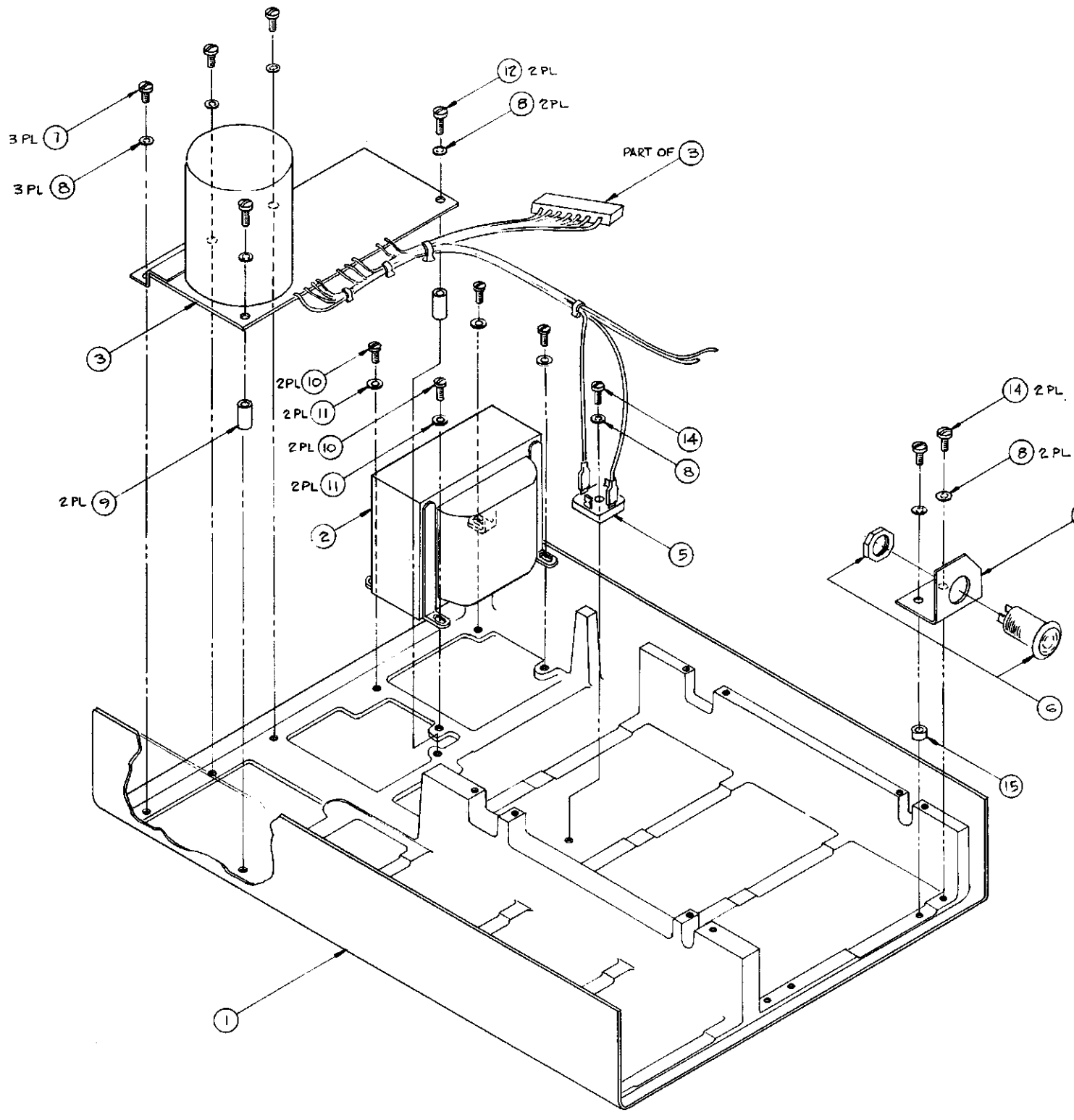

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL FLAT WASHERS ARE ITEM 16
   ALL LOCK WASHERS ARE ITEM 14
   ALL SCREWS ARE ITEM 9

**See Parts List, Section 9, for key to encircled item numbers**



Fig. 8-2 Cabinet Assembly, Model 2, Exploded (300000+I-2-78)

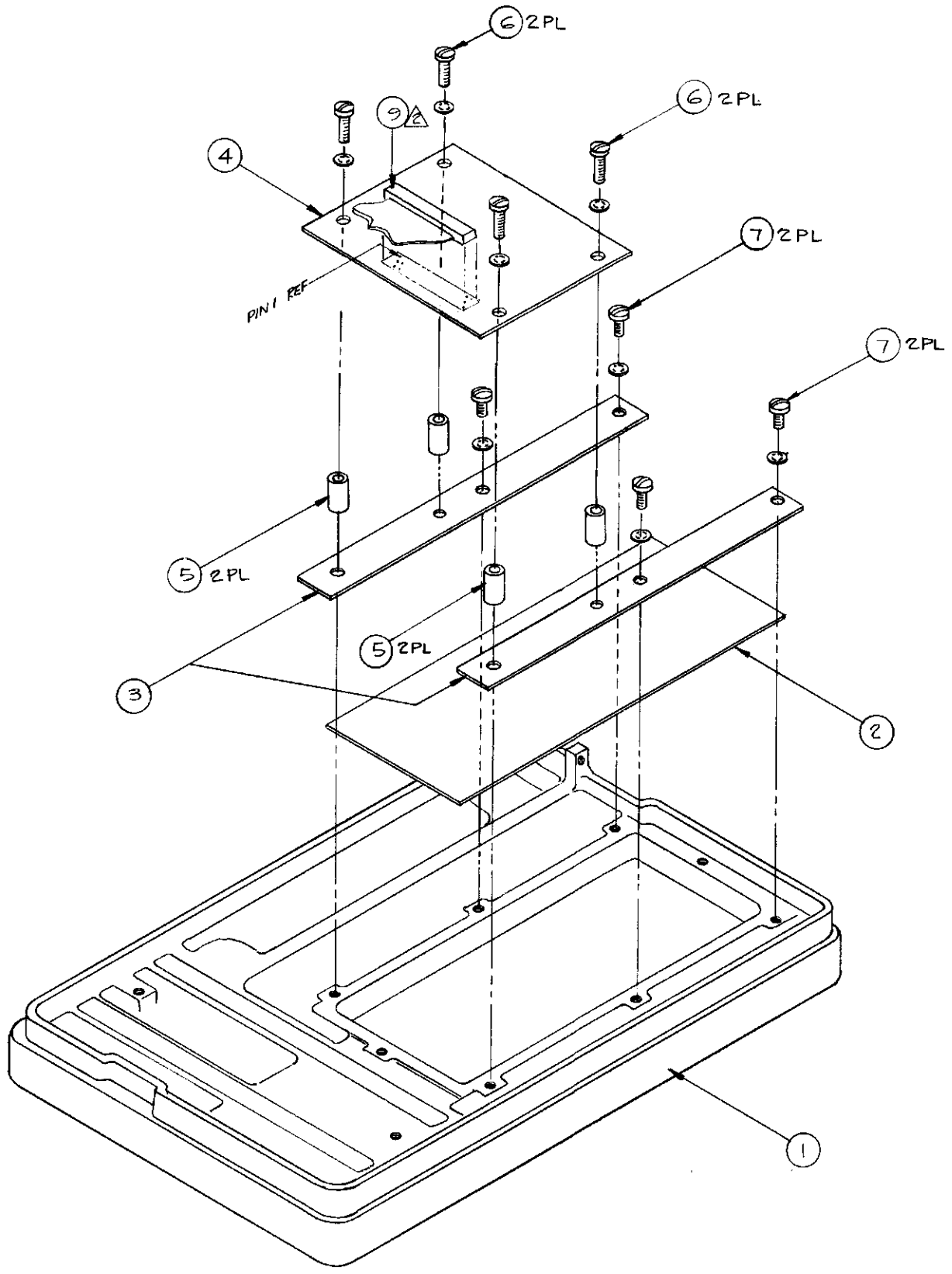



See Parts List, Section 9, for key to encircled item numbers

2 Helios II

302004 D

Fig. 8-3 Base Assembly, Model 2, Exploded




NOTES:

1. UNLESS OTHERWISE SPECIFIED: ALL LOCKWASHERS ARE ITEM 8.

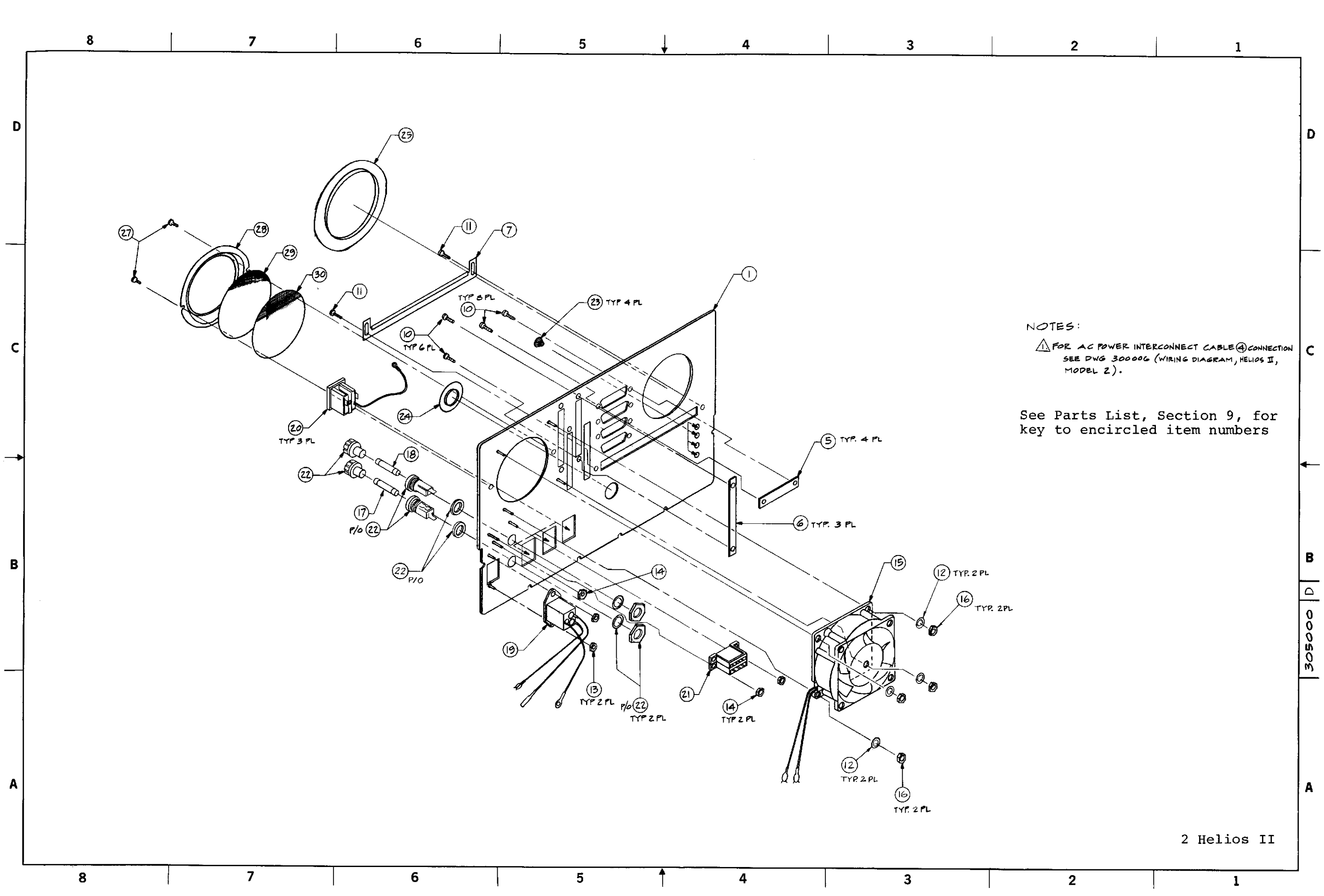
△2 SOLDER ITEM 9 TO ITEM 4 AS SHOWN BEFORE ITEM 4 IS MOUNTED TO ITEM 1.

See Parts List, Section 9, for key to encircled item numbers

306000

2 Helios II

Fig. 8-4 Bezel Assembly, Model 2, Exploded (306000E)




NOTES:

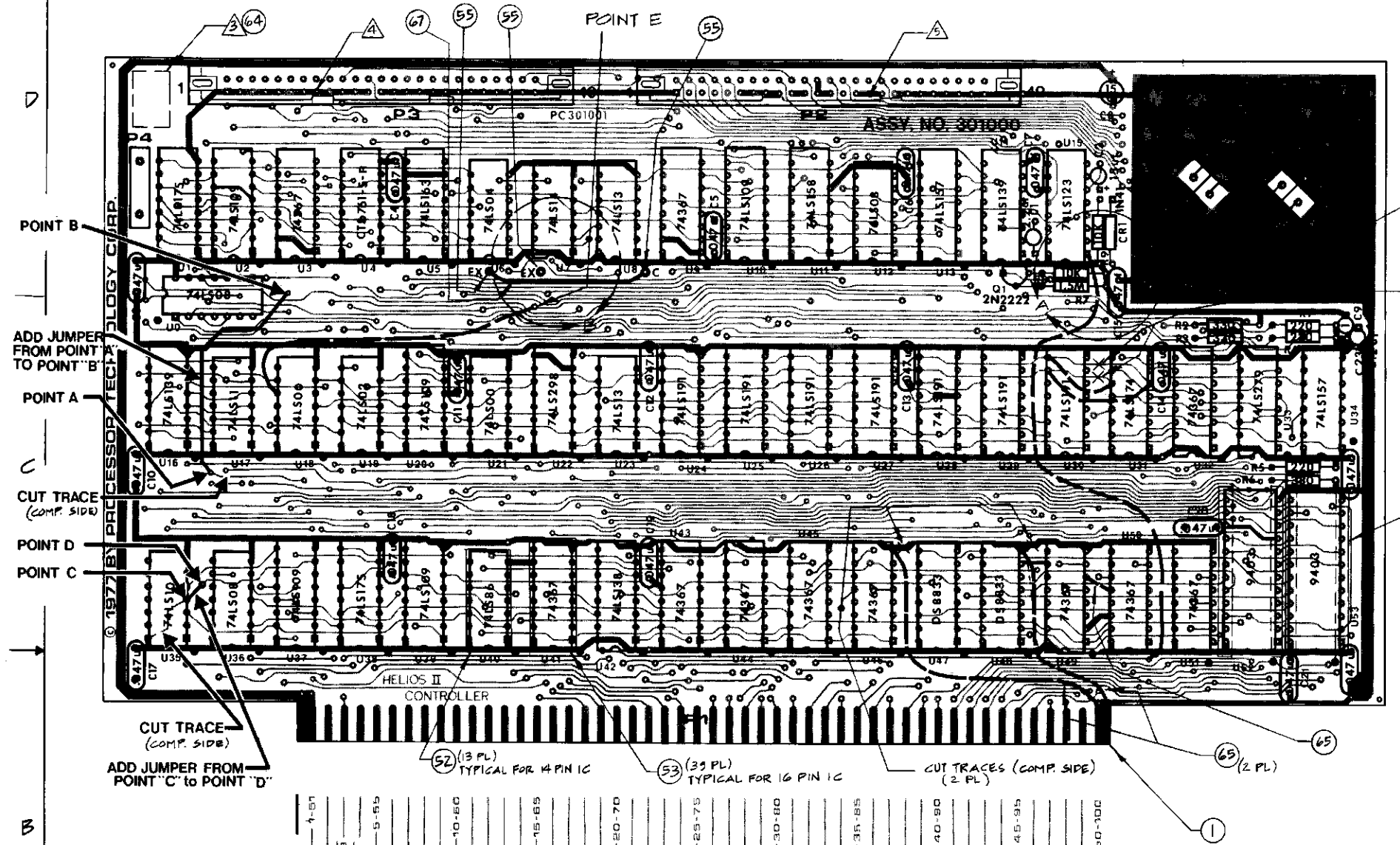
⚠1 FOR AC POWER INTERCONNECT CABLE ④ CONNECTION SEE DWG 300006 (WIRING DIAGRAM, HELIOS II, MODEL 2).

See Parts List, Section 9, for key to encircled item numbers

2 Helios II

300503 D

Fig. 8-5 Rear Panel Assembly, Model 2, Exploded



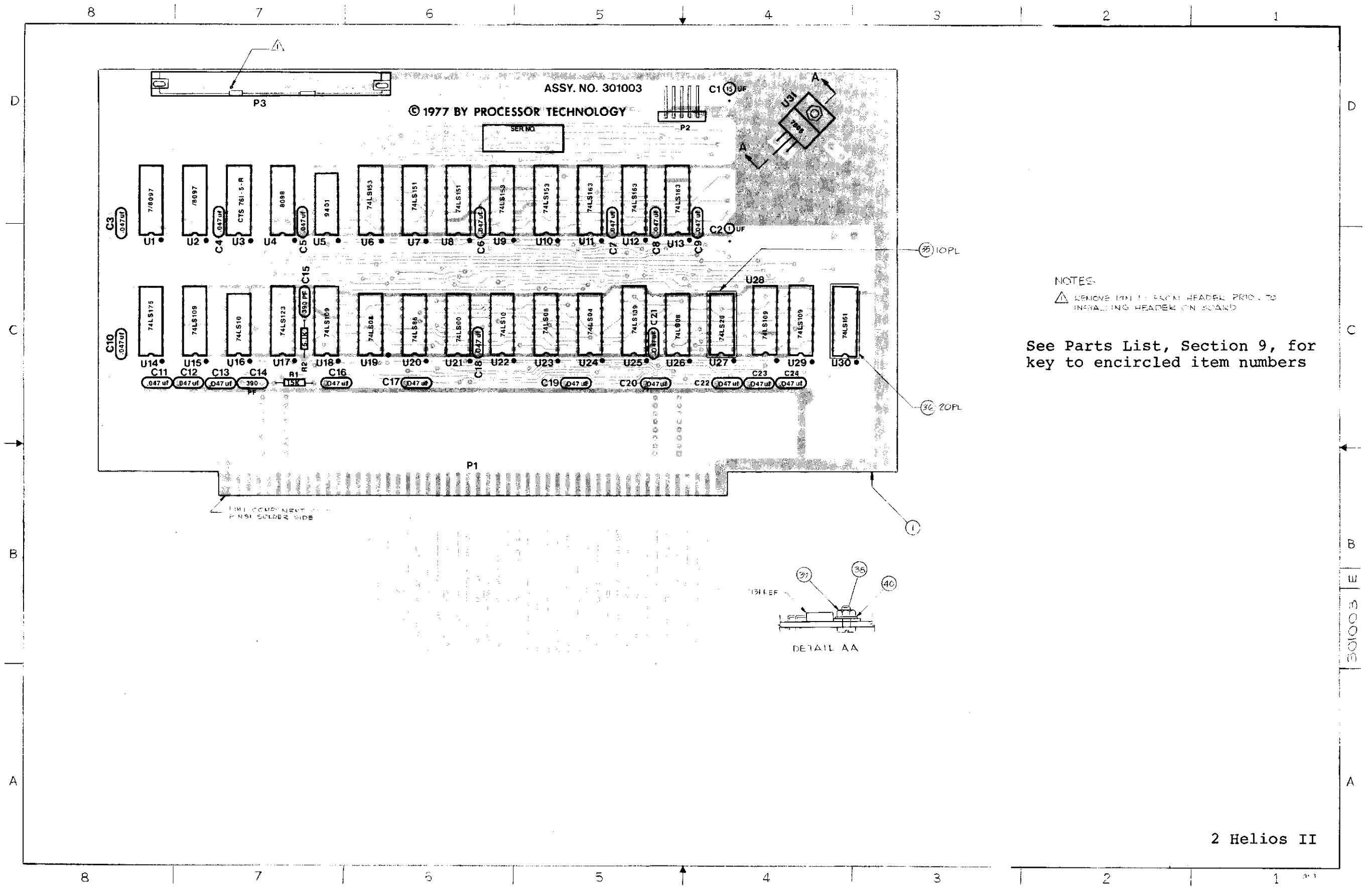

NOTES:

1. ALL HEAVY-THICK DASHED LINES ARE JUMPERS ON THE SOLDER SIDE (FARSIDE) OF THE PCB. ALL HEAVY-THICK SOLID LINES ARE JUMPERS ON THE COMPONENT SIDE (NEARSIDE) OF THE PCB.
2. (NOT USED)
3. MARK LABEL, ITEM (64), WITH REV LETTER AND PLACE IN APPROXIMATE AREA SHOWN.
4. REMOVE PIN 15 FROM HEADER PRIOR TO INSTALLING HEADER ON BOARD.
5. REMOVE PIN 31 FROM HEADER PRIOR TO INSTALLING HEADER ON BOARD.
6. UNLESS OTHERWISE SPECIFIED ALL JUMPER WIRES ARE 24 AWG, ITEM (67)

See Parts List, Section 9, for key to encircled item numbers



Fig. 8-6 Controller PCB Assembly (C/G)



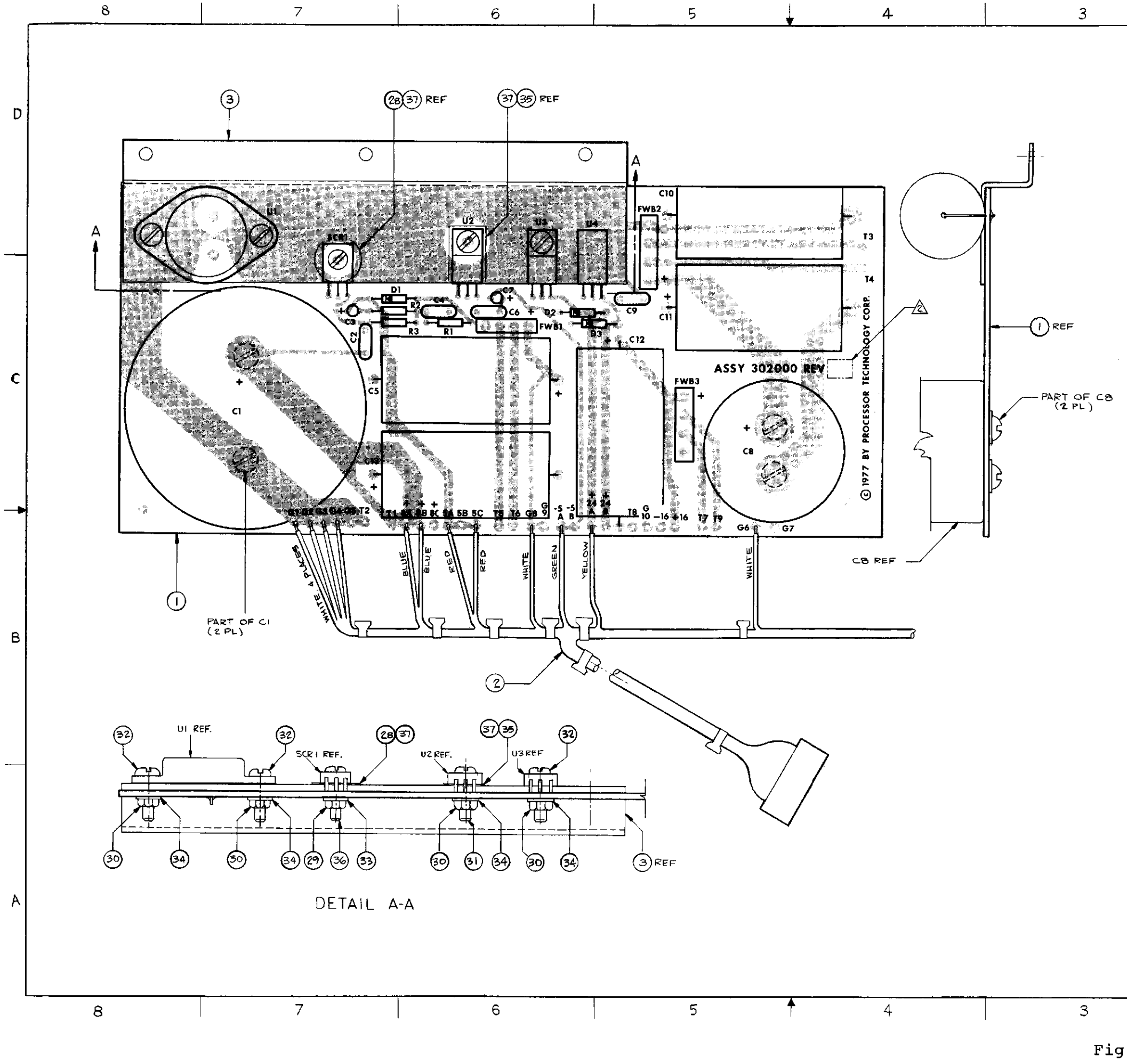

NOTES:

⚠ REMOVE PIN 1 FROM HEADER PRIOR TO INSTALLING HEADER ON BOARD

See Parts List, Section 9, for key to encircled item numbers



Fig. 8-7 Formatter PCB Assembly (C/E)



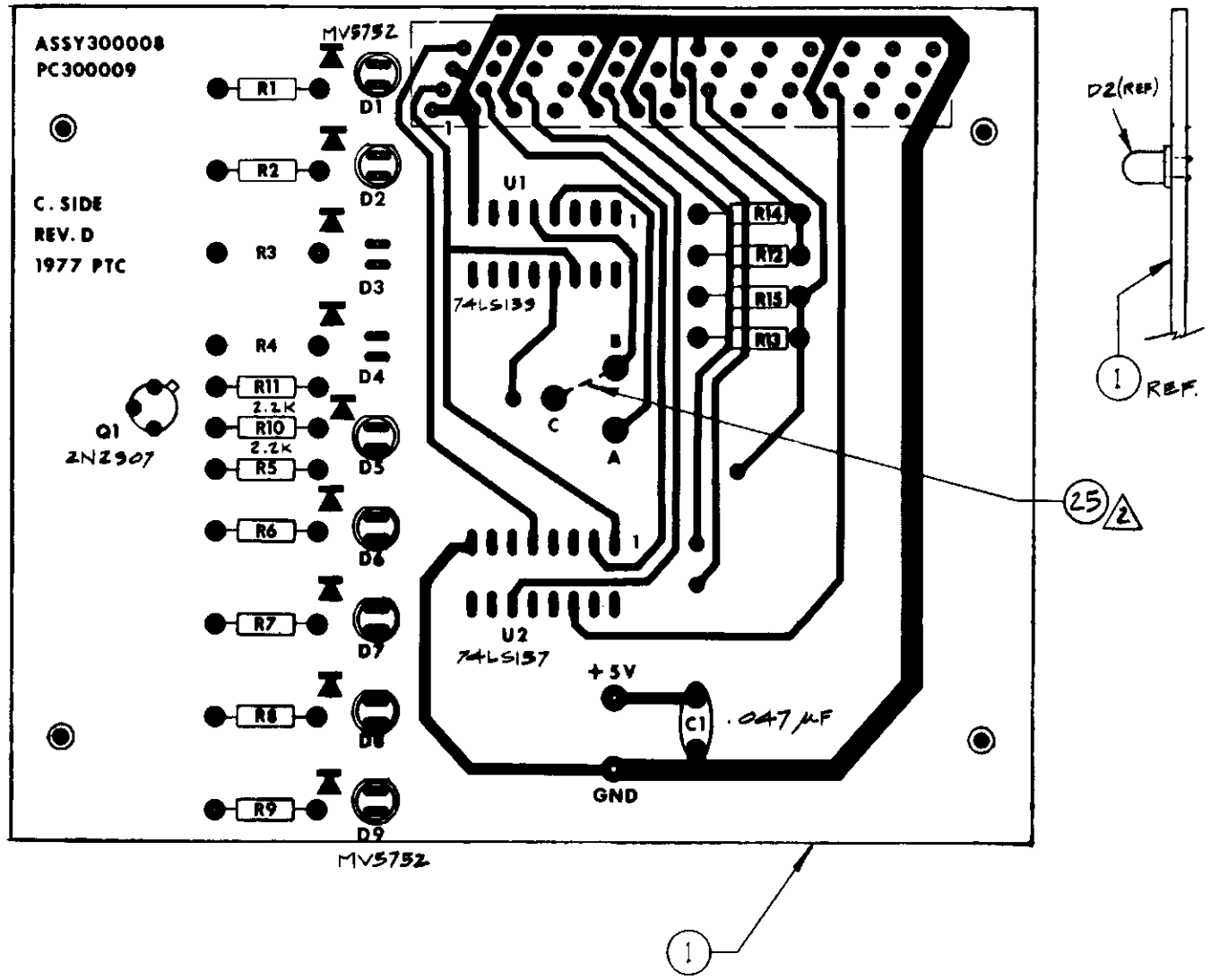

NOTES:

1. THERMAL COMPOUND, ITEM 37, IS TO BE PLACED BETWEEN HEATSINK AND ALL COMPONENTS WHICH ARE MOUNTED TO THE HEATSINK.
2. MARK REV LETTER "D" WITH INDELIBLE INK IN APPROXIMATE AREA SHOWN.

See Parts List, Section 9, for key to encircled item numbers

2 Helios II

Fig. 8-8 Regulator PCB Assembly, Model 2 (C/D)




NOTES:
UNLESS OTHERWISE SPECIFIED:
1. RESISTOR VALUES ARE 220 OHMS.
2. SOLDER A #24 SOLID BUS WIRE JUMPER BETWEEN B & C ON THE FARSIDE (SOLDER SIDE) OF PCB.

See Parts List, Section 9, for key to encircled item numbers



Fig. 8-9 Indicator Panel PCB Assembly (300008 D/F)

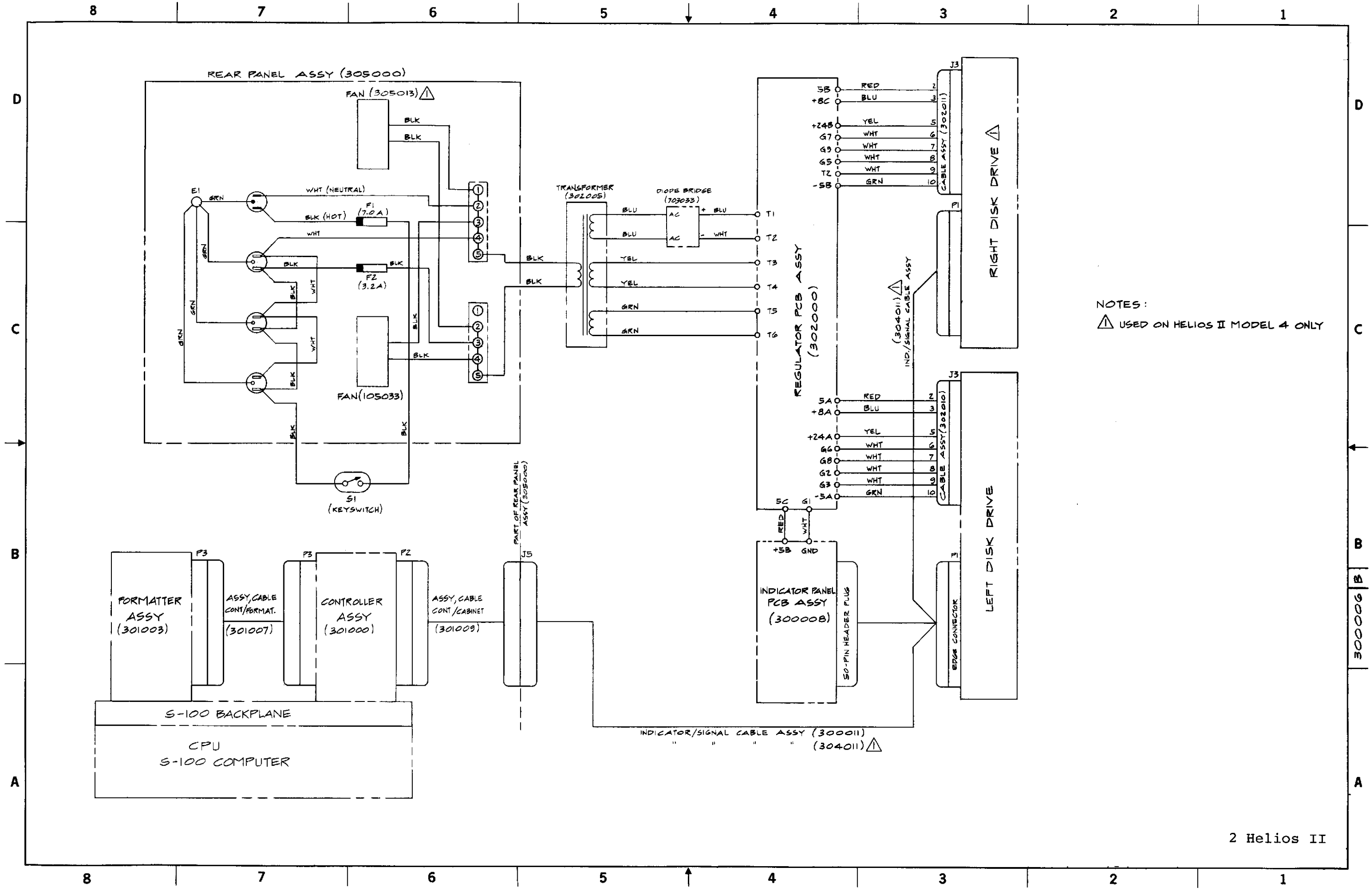
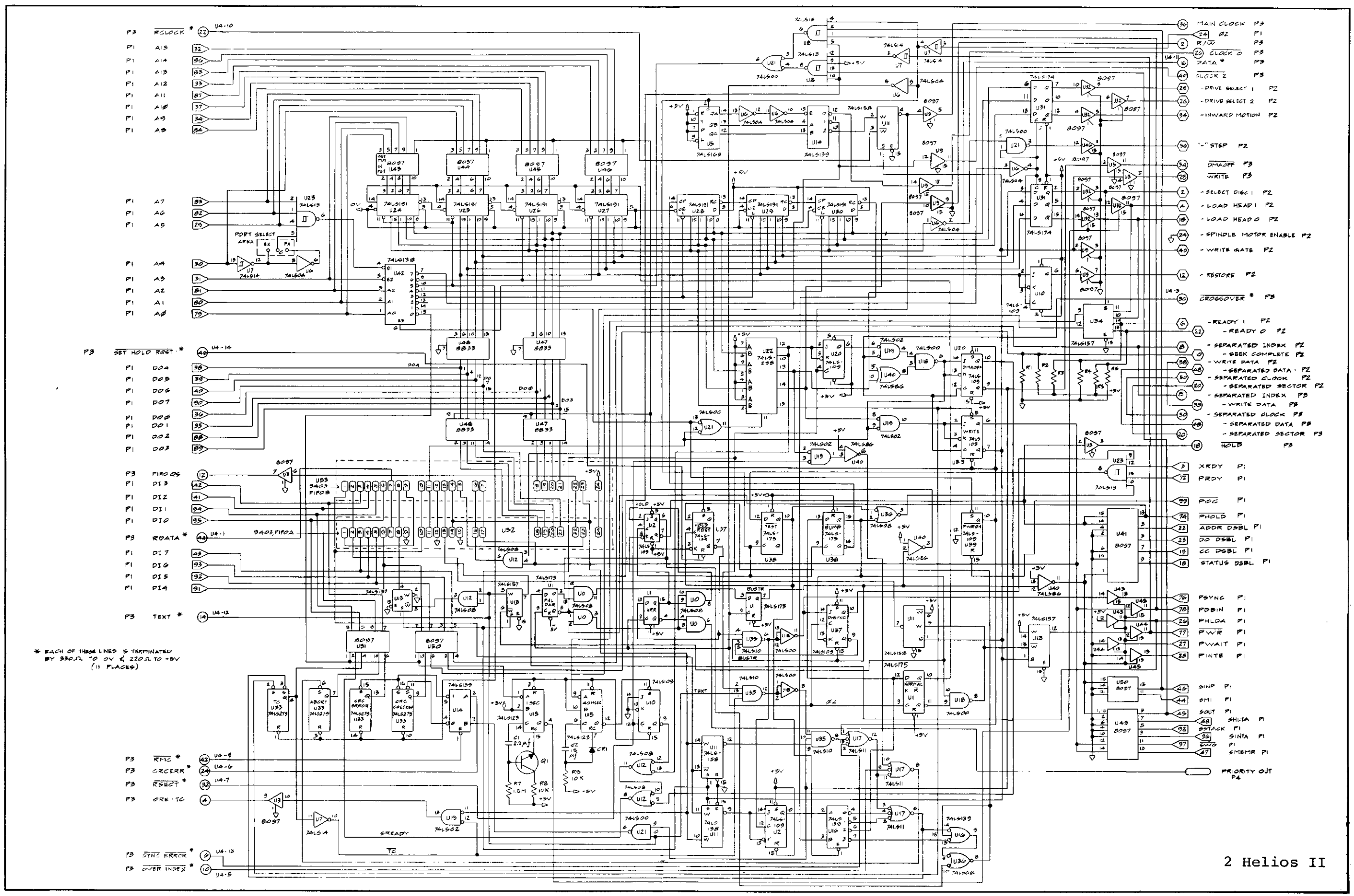


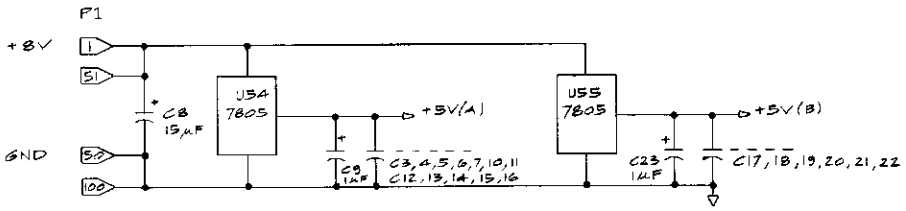

Fig. 8-10 System Wiring Diagram

| N TABLE | |
|---|---|
| USED | DELETED |
| | |
| | |
| | |
| | |
| -J3 | |




2 Helios II

Fig. 8-11 Controller PCB, Schematic (301002E)




POWER SUPPLY

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   - A ALL CAPACITOR VALUES ARE .047 AND UNITS IN μF.
   - B ALL RESISTOR VALUES ARE IN OHM, ¼W, 5%

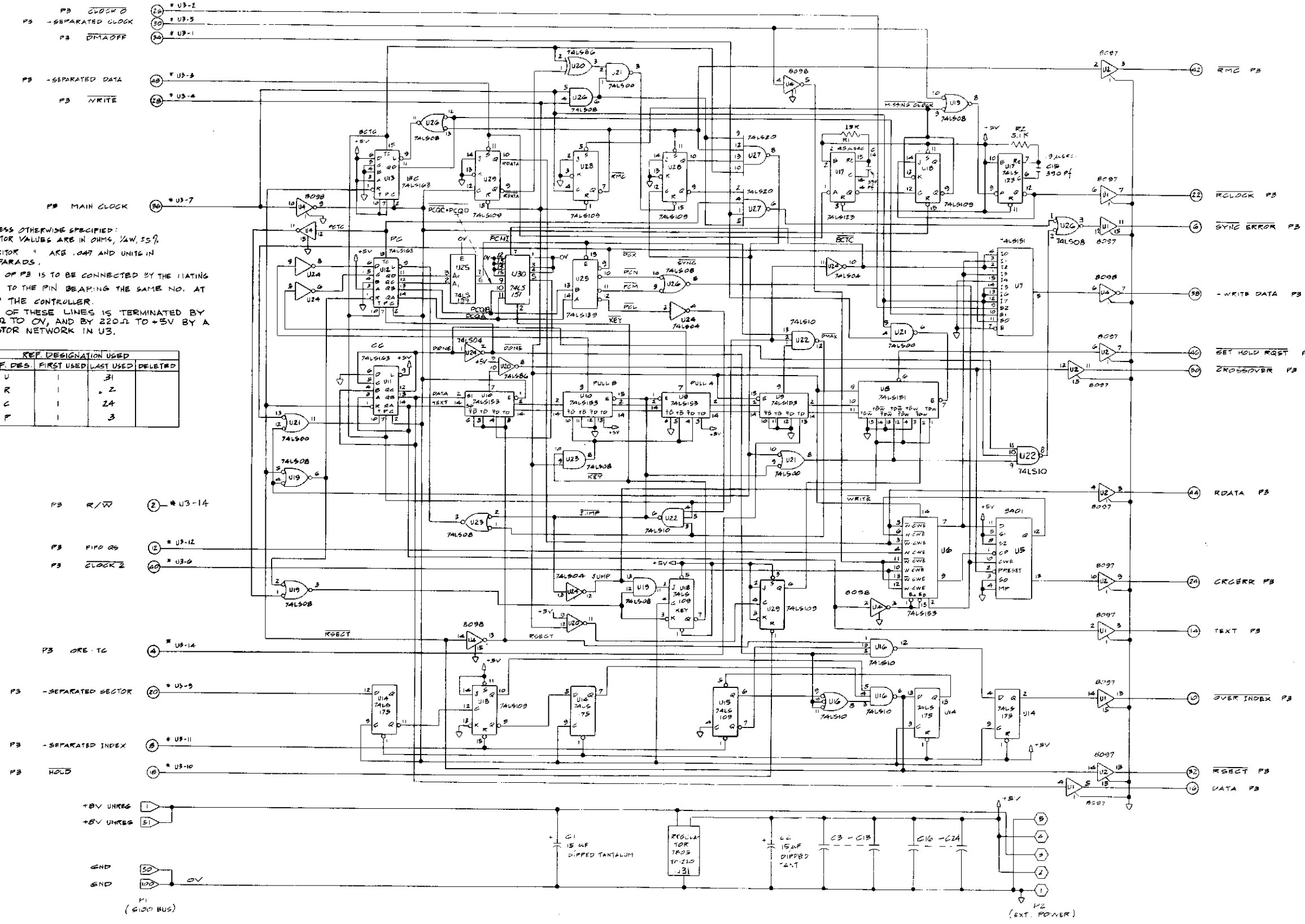
REF. DESIGNATION TABLE

| FIRST USED | LAST USED | NOT USED | DELETED |
|---|---|---|---|
| U1 | U55 | | |
| R1 | R9 | | |
| P1 | P4 | | |
| C1 | C23 | | |
| CR1 | | | |
| J4 | | J1-J3 | |

NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTOR VALUES ARE IN OHMS, ¼W, ±5%
2. " CAPACITOR " ARE .047 AND UNITS IN MICROFARADS.
3. EACH PIN OF P3 IS TO BE CONNECTED BY THE MATING CABLE TO THE PIN BEARING THE SAME NO. AT P3 OF THE CONTROLLER.
4. * EACH OF THESE LINES IS TERMINATED BY 330Ω TO 0V, AND BY 220Ω TO +5V BY A RESISTOR NETWORK IN U3.

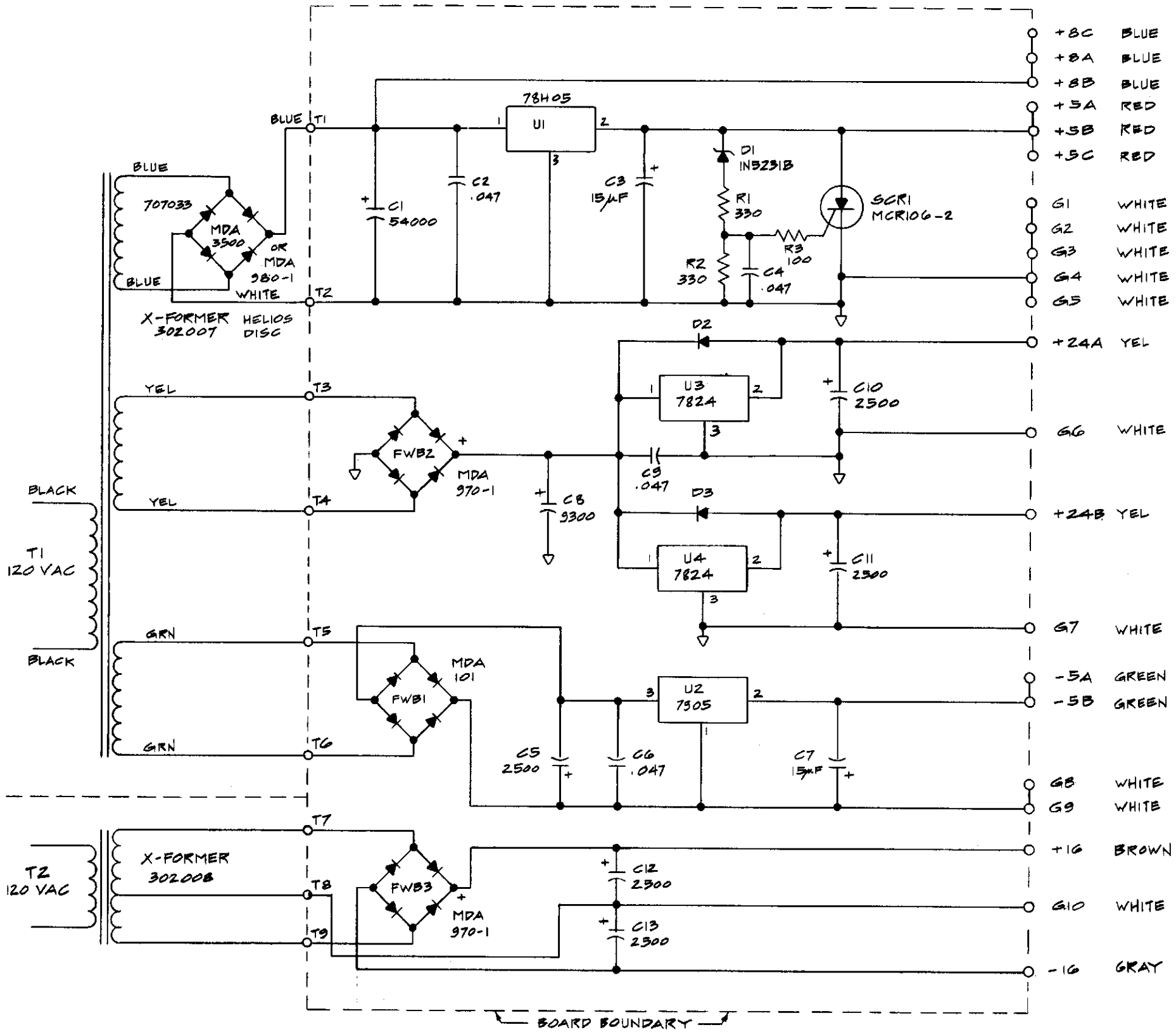
REF. DESIGNATION USED

| REF. DES. | FIRST USED | LAST USED | DELETED |
|---|---|---|---|
| U | 1 | 31 | |
| R | 1 | 2 | |
| C | 1 | 24 | |
| P | 1 | 3 | |




2 Helios II

Fig. 8-12 Formatter PCB, Schematic (301005D)

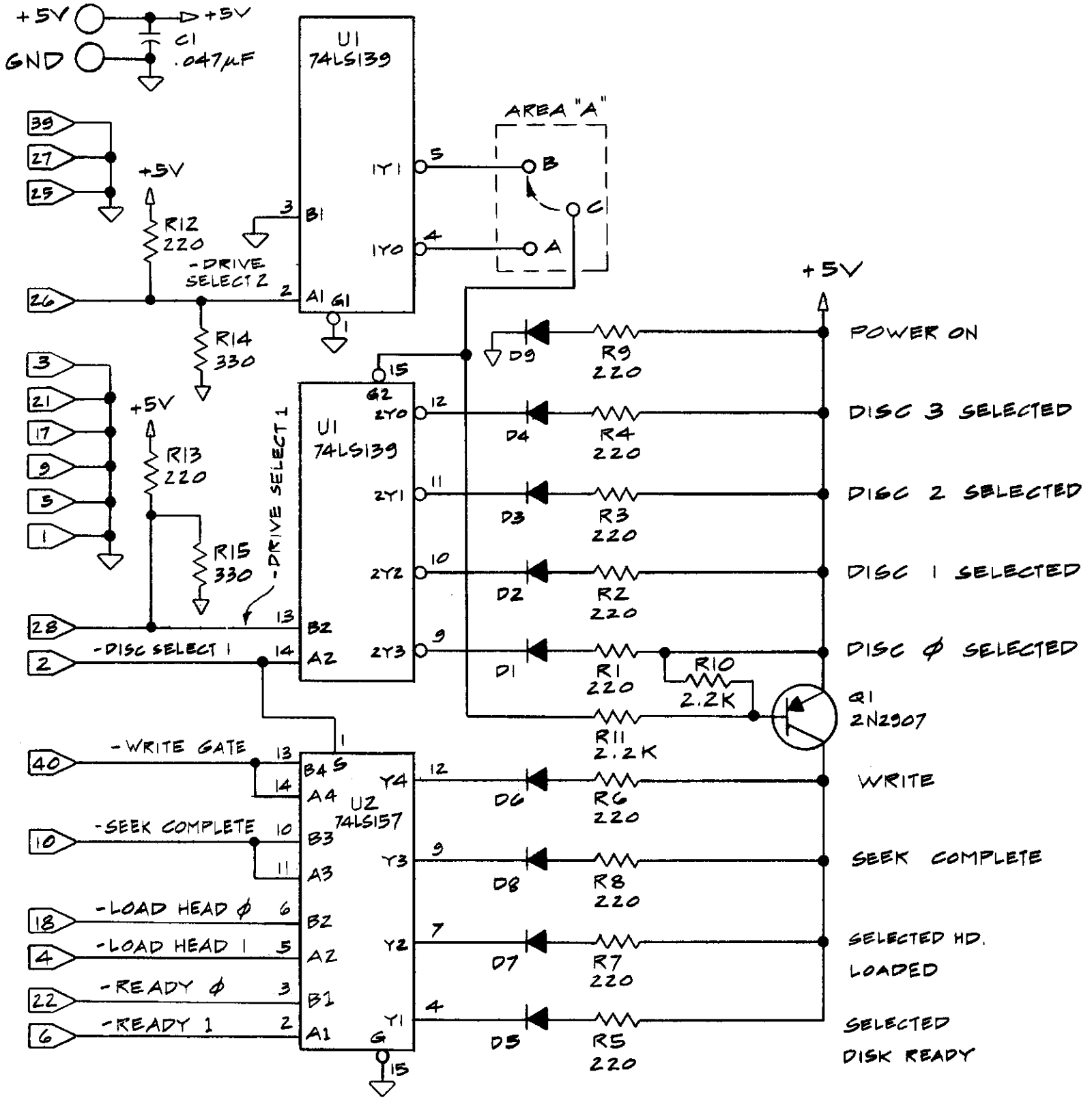



NOTES:

1. UNLESS OTHERWISE SPECIFIED
   A. ALL RESISTOR VALUES ARE GIVEN IN OHMS (Ω)
   B. ALL CAPACITOR VALUES ARE GIVEN IN MICROFARADS (µF)



Fig. 8-13 Regulator PCB, Schematic (302002A)




NOTES:

A. UNLESS OTHERWISE SPECIFIED
   1. ALL DIODES ARE LED, MV5752, RED
   2. ALL RESISTOR VALUES IN OHMS, ¼W, 5%
   3. ALL CAPACITOR VALUES IN MICROFARADS

B. I.C. PWR & GND PIN CONNECTION

| REF DES. | IC NO. | PIN NO +5V | PIN. NO. GND |
|---|---|---|---|
| U1 | 74LS139 | 16 | 8 |
| U2 | 74LS157 | 16 | 8 |
| | | | |

C. COMPONENT REF. DESIGNATION

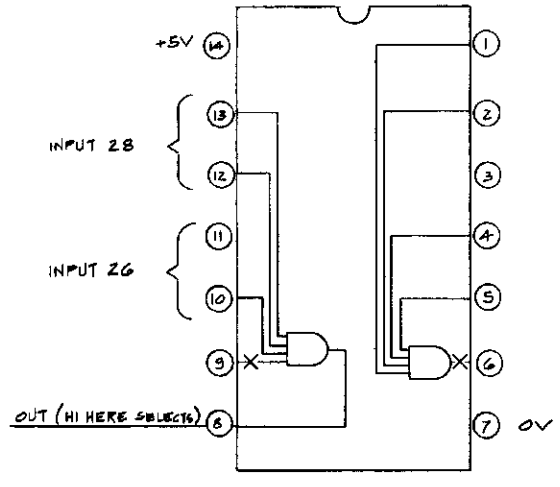
| LAST USED | DELETED |
|---|---|
| U2 | |
| Q1 | |
| D9 | D3 & D4 ON SINGLE DRIVE (-01 & -02) ONLY |
| R15 | R3 & R4 " " " " " |
| C1 | |

D. JUMPER B TO C FOR SINGLE OR #1 HELIOS CABINET
   JUMPER A TO C FOR 2ND HELIOS CABINET

2 Helios II

Fig. 8-14 Indicator Panel PCB, Schematic (300007E)

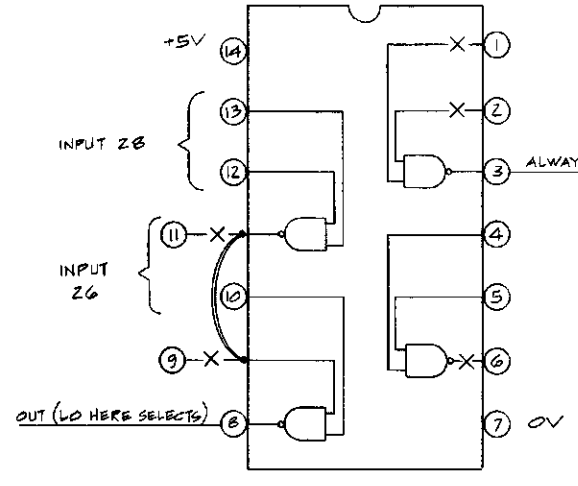
A DUAL FLOPPY DISC DRIVE CONTAINING THIS SELECTOR IN U11 WILL RESPOND AS UNITS 0 & 1




TO MAKE THIS DEVICE
1. GET A 74LS21
2. CUT OFF PINS 6, 9
3. REMOVE PREVIOUS NOMENCLATURE
4. MARK WITH PT PART NUMBER AND "0-1"

| INPUT Z8 | INPUT Z6 | OUT |
|---|---|---|
| LO | LO | LO |
| LO | HI | LO |
| HI | LO | LO |
| HI | HI | [HI] |

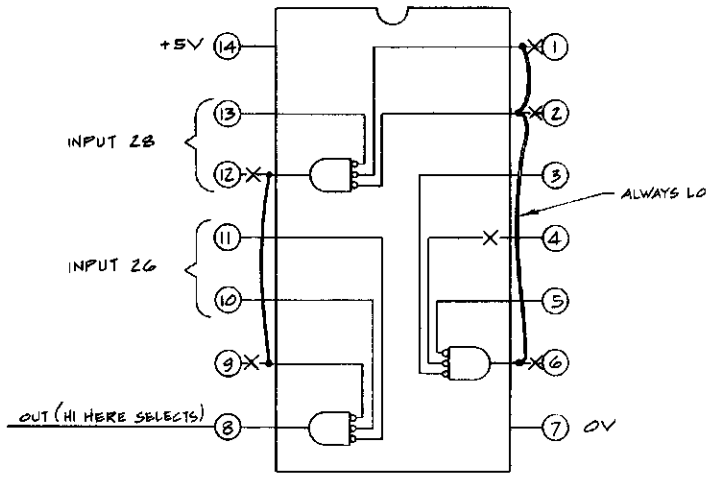
A DUAL FLOPPY DISC DRIVE CONTAINING THIS SELECTOR IN U11 WILL RESPOND AS UNITS 2 & 3




TO MAKE THIS DEVICE
1. GET A 74LS37
2. CUT OFF PINS 1, 2, 6
3. BEND UP PINS 9, 11 & CONNECT THEM TOGETHER
4. REMOVE PREVIOUS NOMENCLATURE
5. MARK WITH PT PART NUMBER AND "2-3"

| INPUT Z8 | INPUT Z6 | OUT |
|---|---|---|
| LO | LO | HI |
| LO | HI | [LO] |
| HI | LO | HI |
| HI | HI | HI |

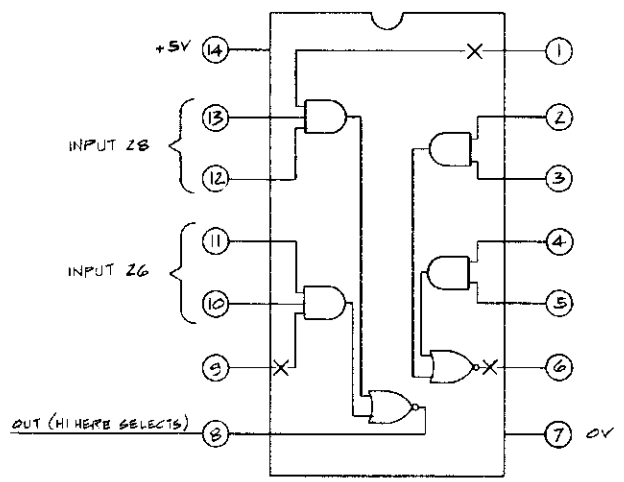
A DUAL FLOPPY DISC DRIVE CONTAINING THIS SELECTOR IN U11 WILL RESPOND AS UNITS 4 & 5




TO MAKE THIS DEVICE
1. GET A 74LS27
2. CUT OFF PIN 4
3. BEND UP PINS 1, 2, 6 & CONNECT THEM TOGETHER
4. BEND UP PINS 9, 12 & CONNECT THEM TOGETHER
5. REMOVE PREVIOUS NOMENCLATURE
6. MARK WITH PT PART NUMBER AND "4-5"

| INPUT Z8 | INPUT Z6 | OUT |
|---|---|---|
| LO | LO | LO |
| LO | HI | LO |
| HI | LO | [HI] |
| HI | HI | LO |

A DUAL FLOPPY DISC DRIVE CONTAINING THIS SELECTOR IN U11 WILL RESPOND AS UNITS 6 & 7




TO MAKE THIS DEVICE
1. GET A 74LS51
2. CUT OFF PINS 1, 6, 9
3. REMOVE PREVIOUS NOMENCLATURE
4. MARK WITH PT PART NUMBER AND "6-7"

| INPUT Z8 | INPUT Z6 | OUT |
|---|---|---|
| LO | LO | [HI] |
| LO | HI | LO |
| HI | LO | LO |
| HI | HI | LO |



Fig. 8-15 Selector DIPSs, Schematic Assemblies, (30015-18B)

-to-Pin Assignments,
or Panel
300011, Model 2)
pins are ground.

| CON-TROLLER P2 | DRIVE P1 | INDI-CATOR PANEL |
|---|---|---|
| X | X | X |
| X | X | X |
| X | X | X |
| X | X | — |
| X | X | X |
| X | X | — |
| X | X | X |
| X | X | — |
| X | X | X |
| | | |
| X | X | — |
| X | X | X |
| X | X | X |
| X | X | — |
| X | X | — |
| X | X | — |
| X | X | — |
| X | X | X |
| X | X | — |
| X | X | — |

.

odd numbered pins are
ct cable to controller

l are unidirectional.
: are listed on this

Section 3, Unpack-

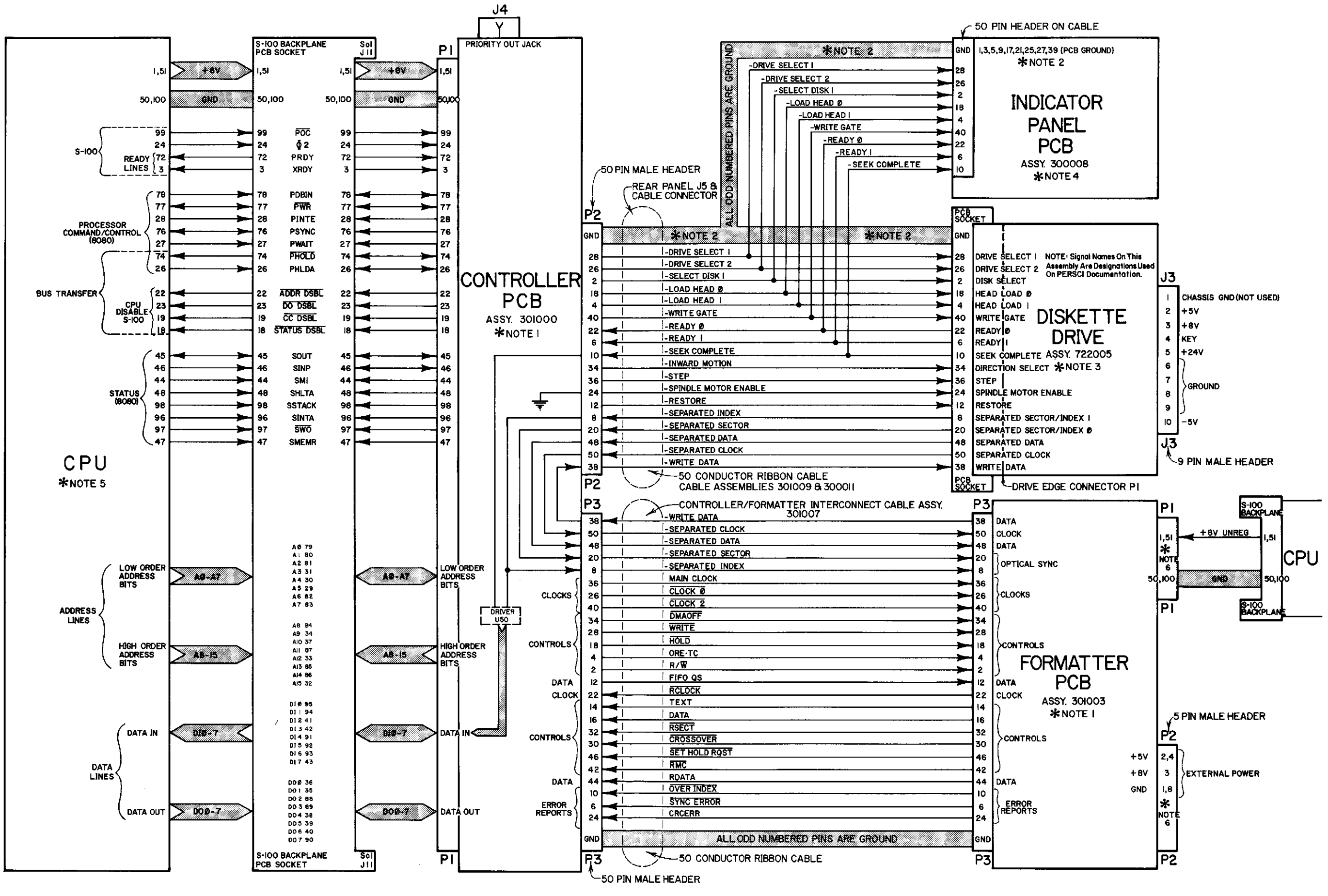



Fig. 8-16 Pin-to-Pin Signal Flow Diagram (I-2-78)

Table 8-1 Numerical Pin-to-Pin Assignments, Controller P3/Formatter P3 (Cable Assy. 301007, Model 2 and 4)
Note: All odd numbered pins are ground.

| PIN # | SIGNAL NAME |
|---|---|
| 2 | R/$\overline{W}$ |
| 4 | ORE·TC |
| 6 | $\overline{\text{SYNC ERROR}}$ |
| 8 | -SEPARATED INDEX |
| 10 | $\overline{\text{OVER INDEX}}$ |
| 12 | FIFO QS |
| 14 | TEXT |
| 16 | DATA |
| 18 | $\overline{\text{HOLD}}$ |
| 20 | -SEPARATED SECTOR |
| 22 | $\overline{\text{RCLOCK}}$ |
| 24 | CRCERR |
| 26 | $\overline{\text{CLOCK Ø}}$ |
| 28 | $\overline{\text{WRITE}}$ |
| 30 | $\overline{\text{CROSSOVER}}$ |
| 32 | $\overline{\text{RSECT}}$ |
| 34 | $\overline{\text{DMAOFF}}$ |
| 36 | MAIN CLOCK |
| 38 | -WRITE DATA |
| 40 | $\overline{\text{CLOCK 2}}$ |
| 42 | $\overline{\text{RMC}}$ |
| 44 | RDATA |
| 46 | $\overline{\text{SET HOLD RQST}}$ |
| 48 | -SEPARATED DATA |
| 50 | -SEPARATED CLOCK |

Table 8-2 Numerical Pin-to-Pin Assignments, Controller/Drive/Indicator Panel
(Cable Assys. 301009 and 300011, Model 2)
Note: All odd numbered pins are ground.

| PIN # | SIGNAL | CONTROLLER P2 | DRIVE P1 | INDICATOR PANEL |
|---|---|---|---|---|
| 2 | -DISK SELECT 1 | X | X | X |
| 4 | -LOAD HEAD 1 | X | X | X |
| 6 | -READY 1 | X | X | X |
| 8 | -SEPARATED INDEX | X | X | — |
| 10 | -SEEK COMPLETE | X | X | X |
| 12 | -RESTORE | X | X | — |
| 18 | -LOAD HEAD Ø | X | X | X |
| 20 | -SEPARATED SECTOR | X | X | — |
| 22 | -READY Ø | X | X | X |
| 24 | -SPINDLE MOTOR ENABLE | X | X | — |
| 26 | -DRIVE SELECT 2 | X | X | X |
| 28 | -DRIVE SELECT 1 | X | X | X |
| 34 | -INWARD MOTION | X | X | — |
| 36 | -STEP | X | X | — |
| 38 | -WRITE DATA | X | X | — |
| 40 | -WRITE GATE | X | X | X |
| 48 | -SEPARATED DATA | X | X | — |
| 50 | -SEPARATED CLOCK | X | X | — |

*NOTES

1. See Table 8-1, 8-2 and 7-7 for numerical pin-to-pin assignments.
2. Among the controller, formatter, drive, and indicator panel, all odd numbered pins are ground. Some indicator panel pins are grounded by the interconnect cable to controller ground.
3. For system wiring see Fig. 8-10, System Wiring Diagram.
4. Signals among the controller, formatter, drive and indicator panel are unidirectional.
5. Only those signal/pins on the CPU which are used by the controller are listed on this drawing.
6. P1 and P2 on the formatter are alternative DC power sources. (See Section 3, Unpacking and Assembly Tips.)

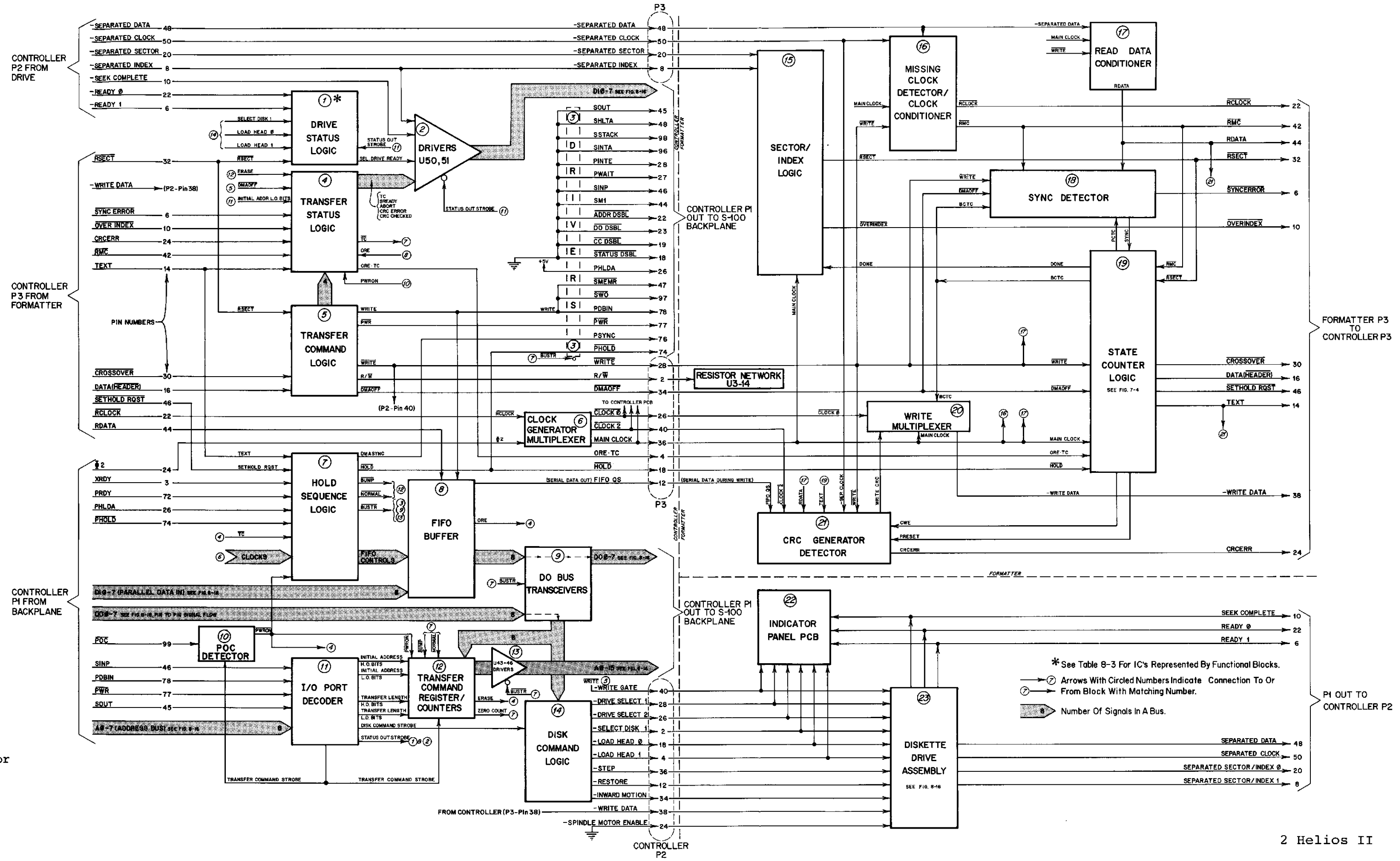



Fig. 8-17 System Block Diagram (I-3-78)

## Table 8-3 Key to System Functional Block Diagram

(The encircled key numbers refer to matching numbers on Fig. 8-17, System Block Diagram.)

### CONTROLLER PCB

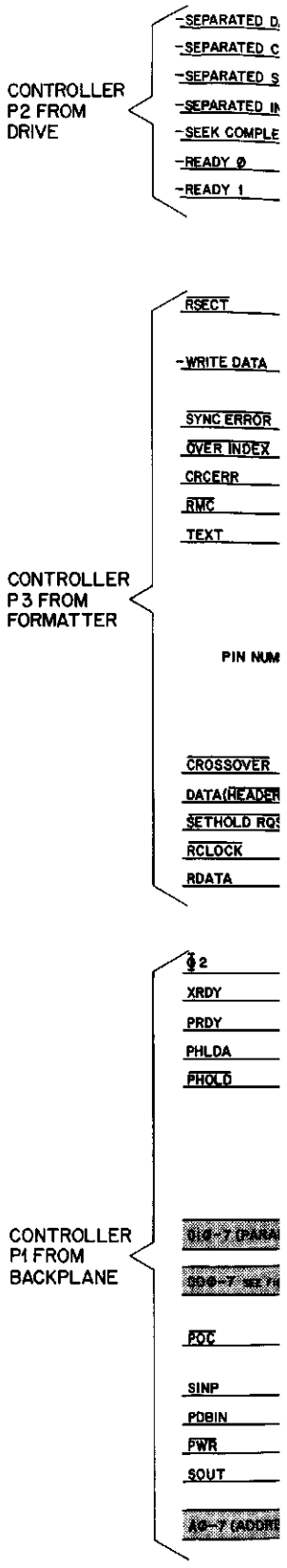
(Refer to Fig. 8-11, Controller PCB Schematic.)

| KEY # | NAME OF FUNCTIONAL BLOCK | ICs REPRESENTED |
|---|---|---|
| (1) | Drive Status Logic | U10-9,U12-8,11,U15,U34 |
| (2) | S-100 Tri-state Bus Drivers | U50,U51 |
| (3) | S-100 Tri-state Bus Drivers | U41,U43,U44,U45,U49,U50 |
| (4) | Transfer Status Logic | U14,U19,U21,U33 |
| (5) | Transfer Command Logic | U13,U18-6,U19-1,4,10,U20, U21-11,U39-3,U40-8 |
| (6) | Clock Generator/Multiplexer | U5,U6,U7,U11,U14 |
| (7) | Hold Sequence Logic | UØ,U1,U2,U3,U11,U12,U13,U16, U17,U18,U23,U35,U36,U37, U38,U40; Abort Logic: U35-8,12,U17-8, 12,U18-3 |
| (8) | FIFO Buffer | U52,U53 |
| (9) | DO Bus Transceivers | U47,U48 |
| (10) | PWR ON Detector/Clear Generator | U39 |
| (11) | I/O Port Decoder | U6,U7,U8,U21,U23,U42 |
| (12) | Transfer Command Register/Counters | U22,U24 through U30 |
| (13) | S-100 Tri-state Address Bus Drivers | U41,U43 through U46,U49,U50 |
| (14) | Disk Command Logic | U10-6,U21-3,U31 |

### FORMATTER PCB

(Refer to Fig. 8-12, Formatter PCB Schematic.)

| KEY # | NAME OF FUNCTIONAL BLOCK | ICs REPRESENTED |
|---|---|---|
| (15) | Sector/Index Logic | U14,U15,U16 |
| (16) | Clock Detector/Conditioner | U17,U18,U19,U28 |
| (17) | Read Data Conditioner | U29 |
| (18) | Sync Detector | U20,U21,U22,U26,U27,U28 |
| (19) | State Counter Logic | (Refer to Fig. 7-4.) |
| (20) | Write Multiplexer | U7 |
| (21) | CRC Generator/Detector | U4,U5,U6 |
| (22) | Indicator Panel PCB | (Refer to Fig. 8-14, Indicator Panel PCB, Schematic.) |
| (23) | Diskette Drive Assembly | (Refer to schematics in the Helios II Service Manual.) |



See Parts List, Section 9, for key to encircled item numbers

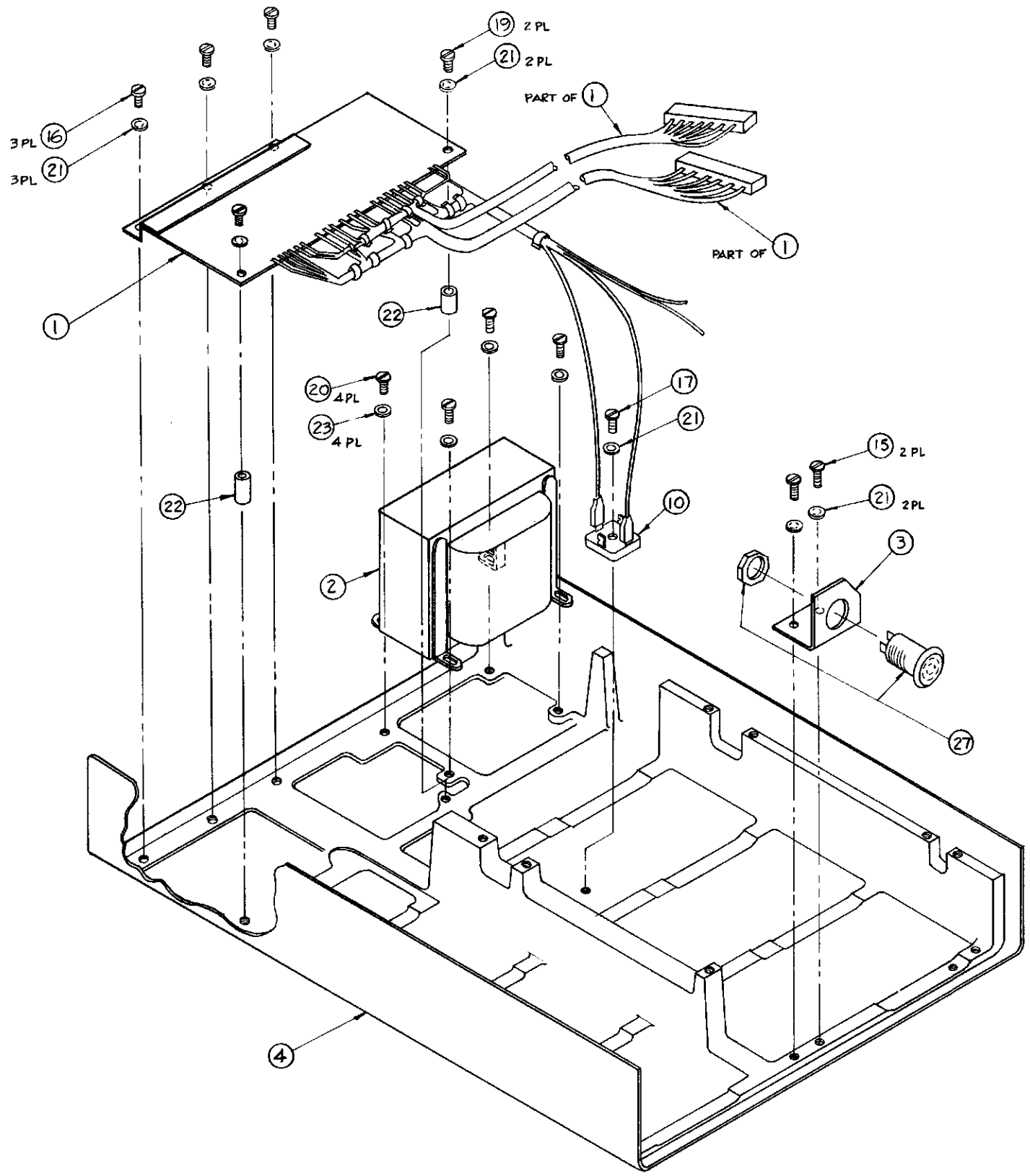
NOTES:

1 UNLESS OTHERWISE SPECIFIED:
ALL FLAT WASHERS ARE ITEM (25)
ALL LOCK WASHERS ARE ITEM (19)
ALL SCREWS ARE ITEM (14)

⚠4 INSTALL DRIVE SELECTORS DURING PRODUCTION TEST.

2 Helios II

Fig. 8-18 Cabinet Assembly, Model 4, Exploded

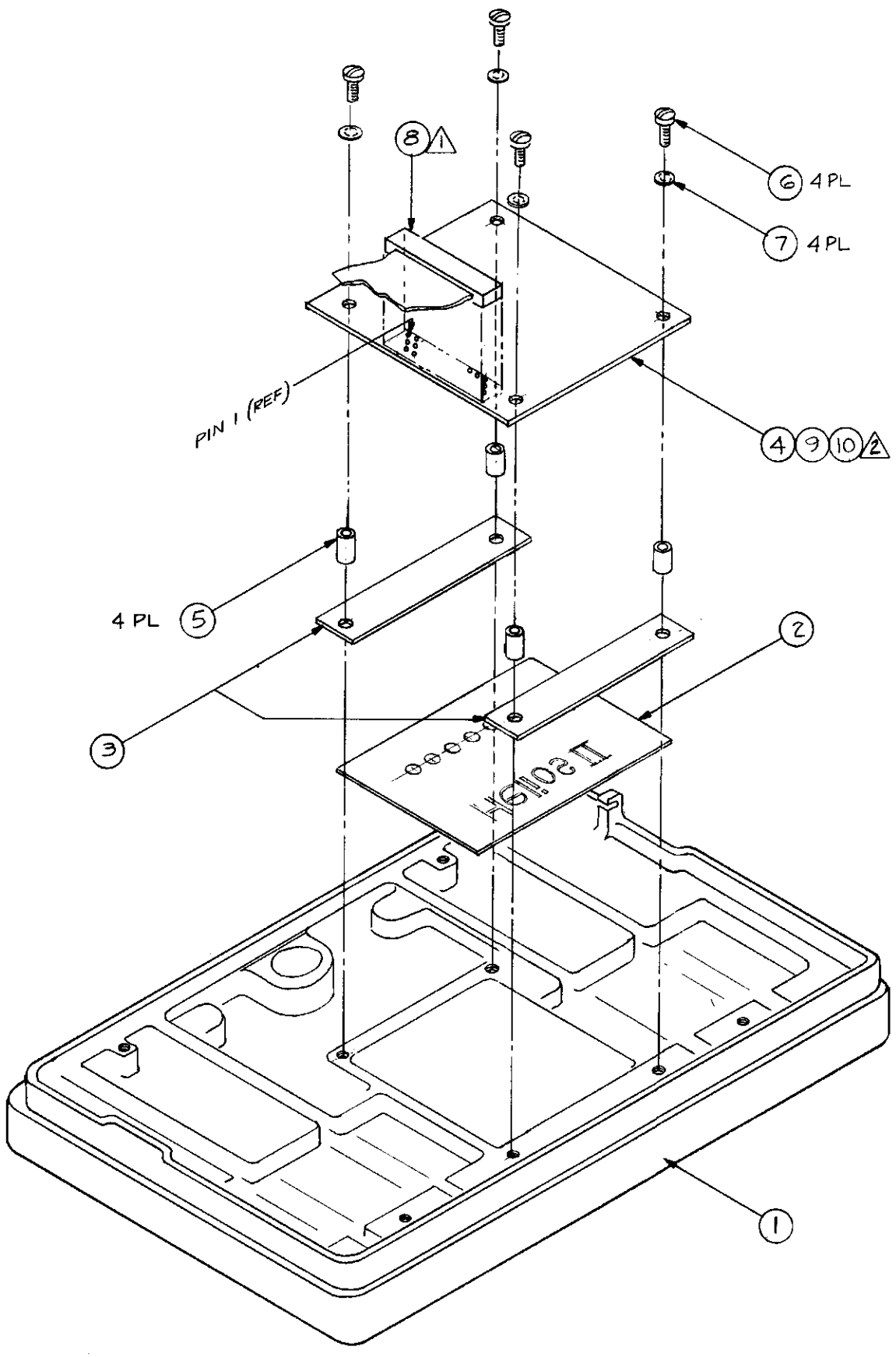



See Parts List, Section 9, for key to encircled item numbers

2 Helios II

304020 A

Fig. 8-19 Base Assembly, Model 4, Exploded




NOTES:

⚠1 SOLDER ITEM 8 TO ITEM 4 BEFORE ITEM 4 IS MOUNTED TO ITEM 1.

⚠2 MOUNT AND SOLDER D3, D4, R3, R4 (ITEMS 9 AND 10) ON P.C. BOARD (ITEM 4) BEFORE MOUNTING ITEM 4 TO ITEM 1.

See Parts List, Section 9, for key to encircled item numbers

2 Helios II

304010 A B

Fig. 8-20 Bezel Assembly, Model 4, Exploded

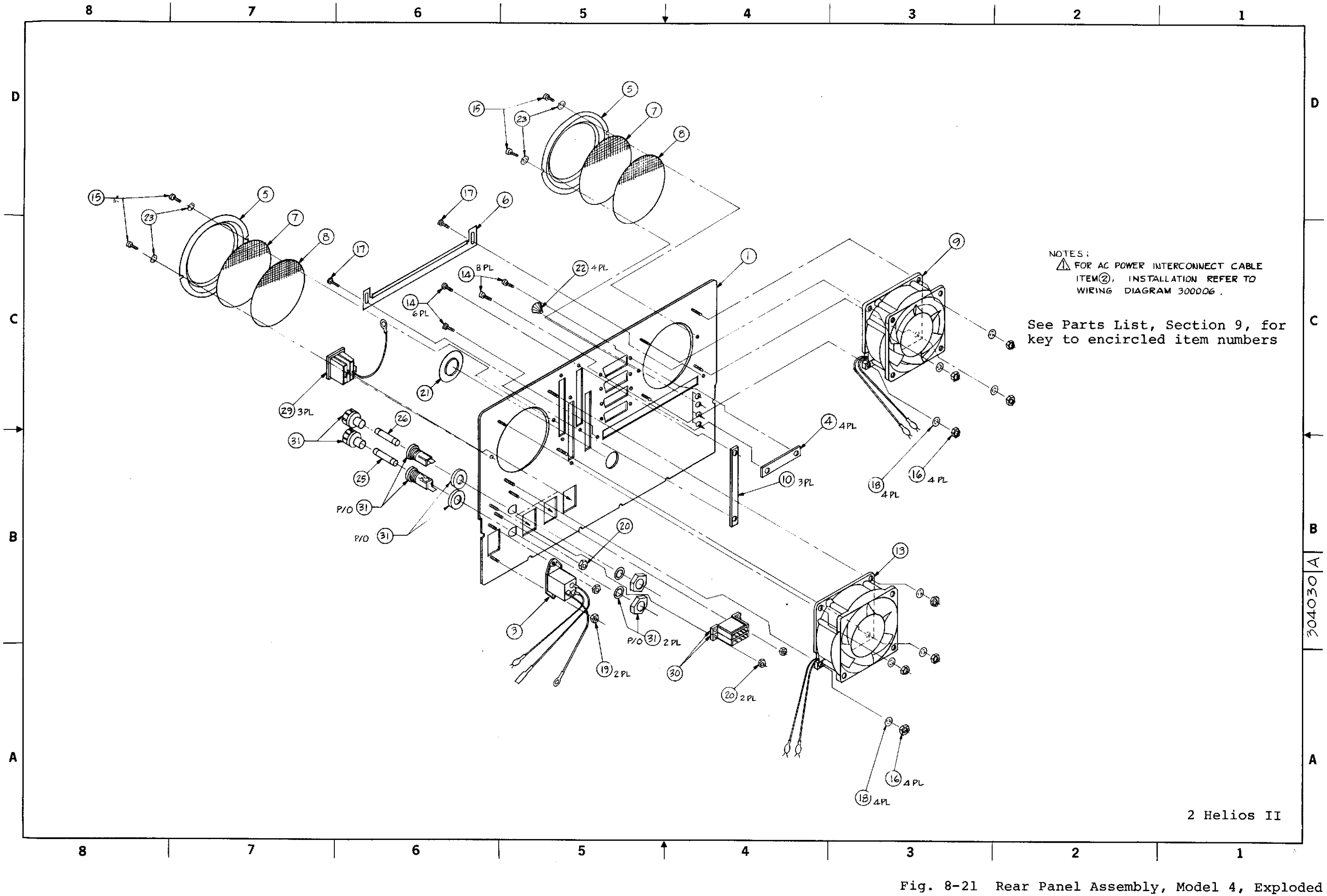
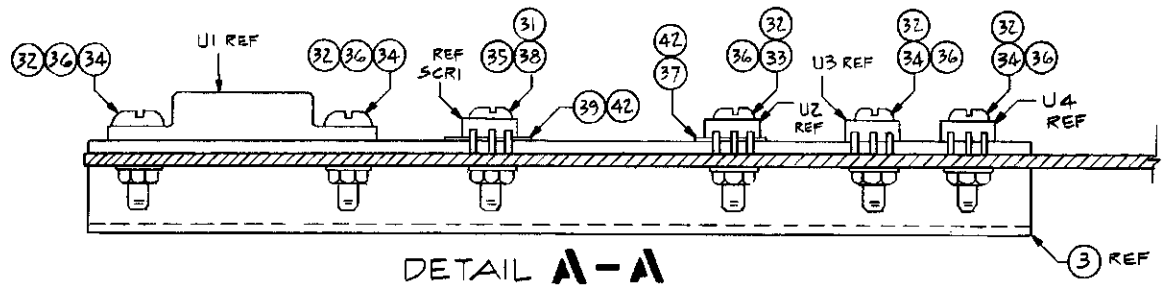
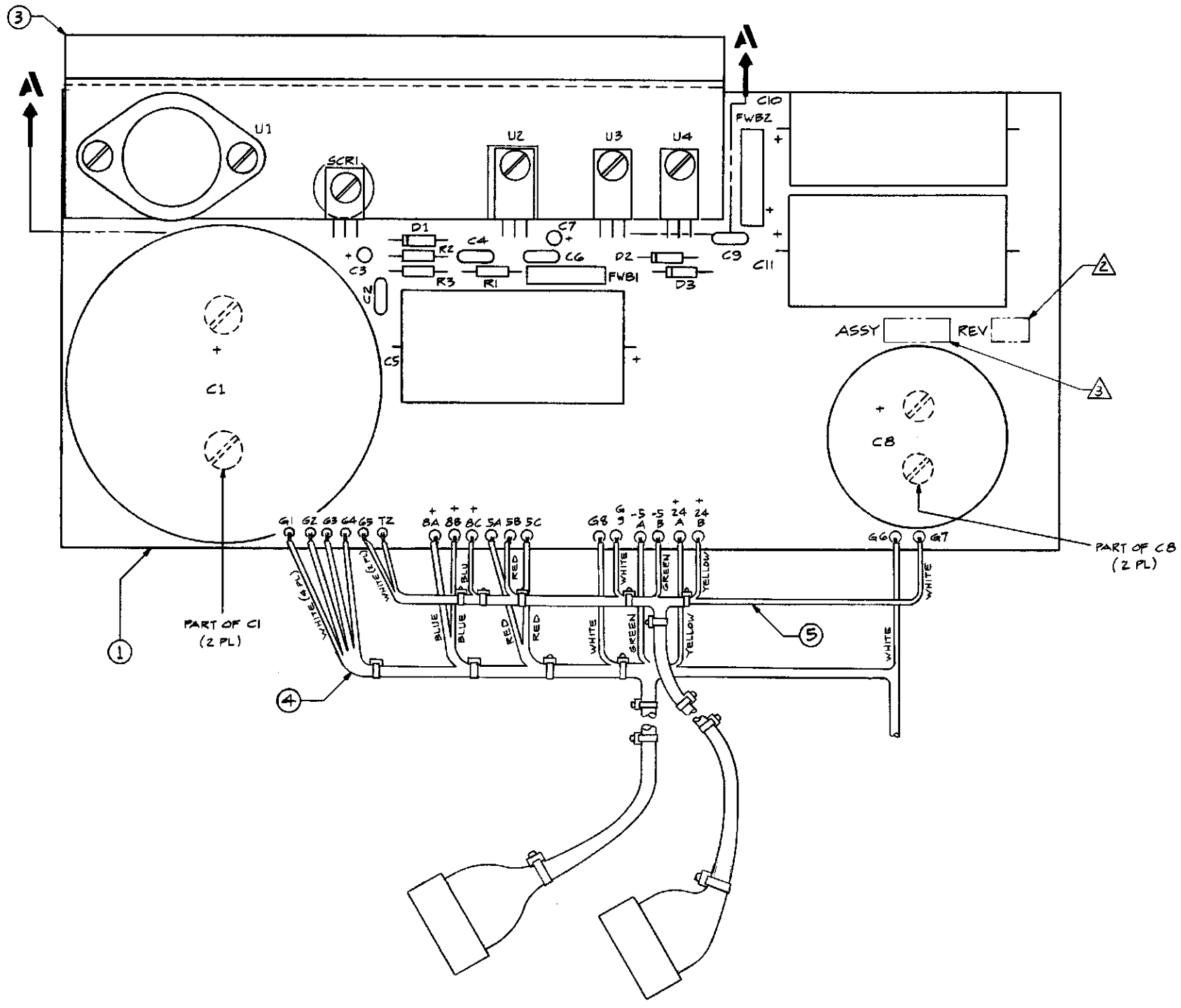



Fig. 8-21 Rear Panel Assembly, Model 4, Exploded




DETAIL A-A




NOTES:

1. THERMAL COMPOUND, ITEM 37, IS TO BE PLACED BETWEEN HEATSINK AND ALL COMPONENTS WHICH ARE MOUNTED TO THE HEATSINK.
2. MARK REV LETTER WITH INDELLIBLE INK IN APPROXIMATE AREA SHOWN.
3. MARK ASSY NO. "304025" IN APPROXIMATE AREA SHOWN.

See Parts List, Section 9, for key to encircled item numbers

2 Helios II

304025

Fig. 8-22 Regulator PCB Assembly, Model 4