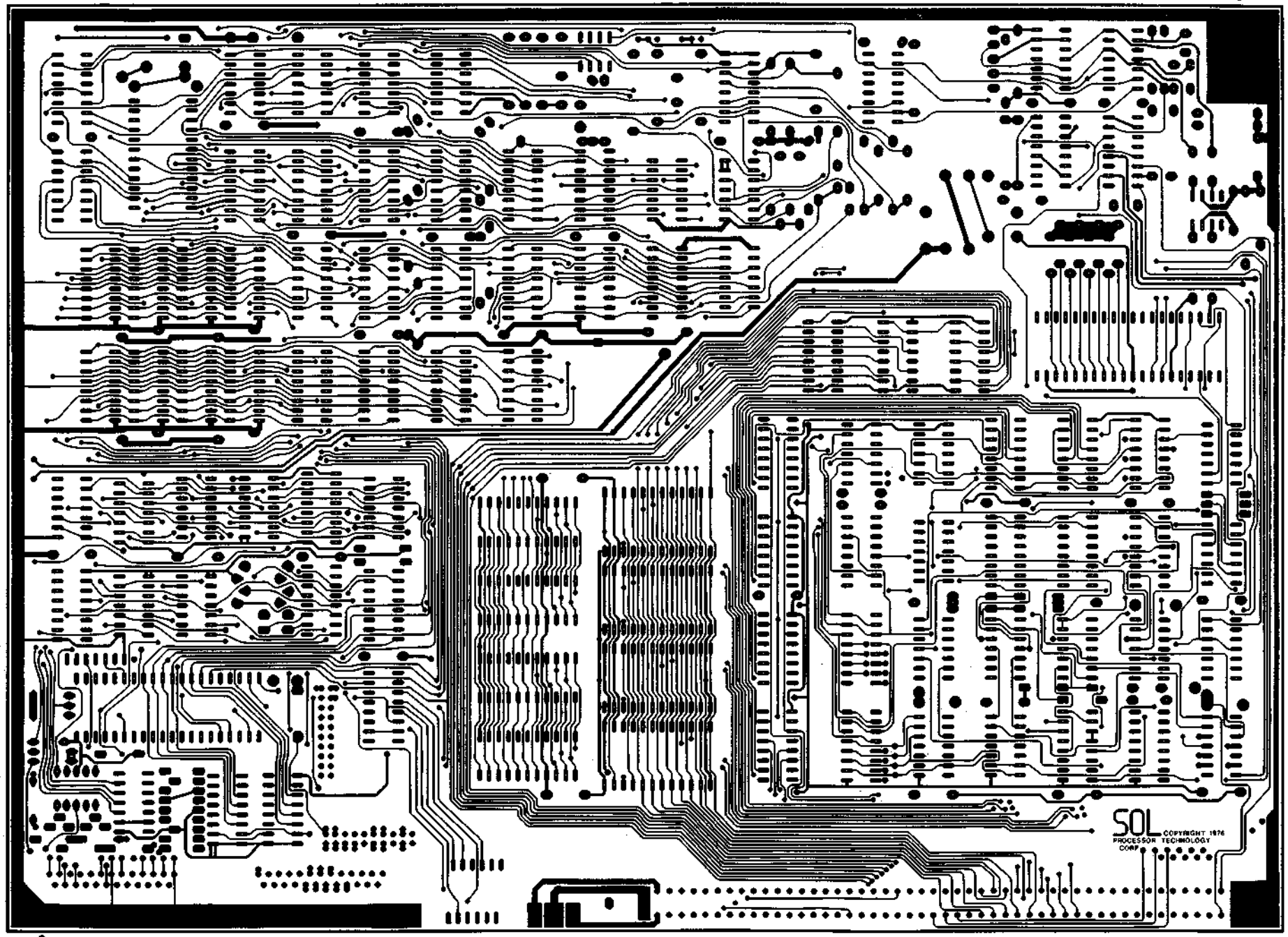
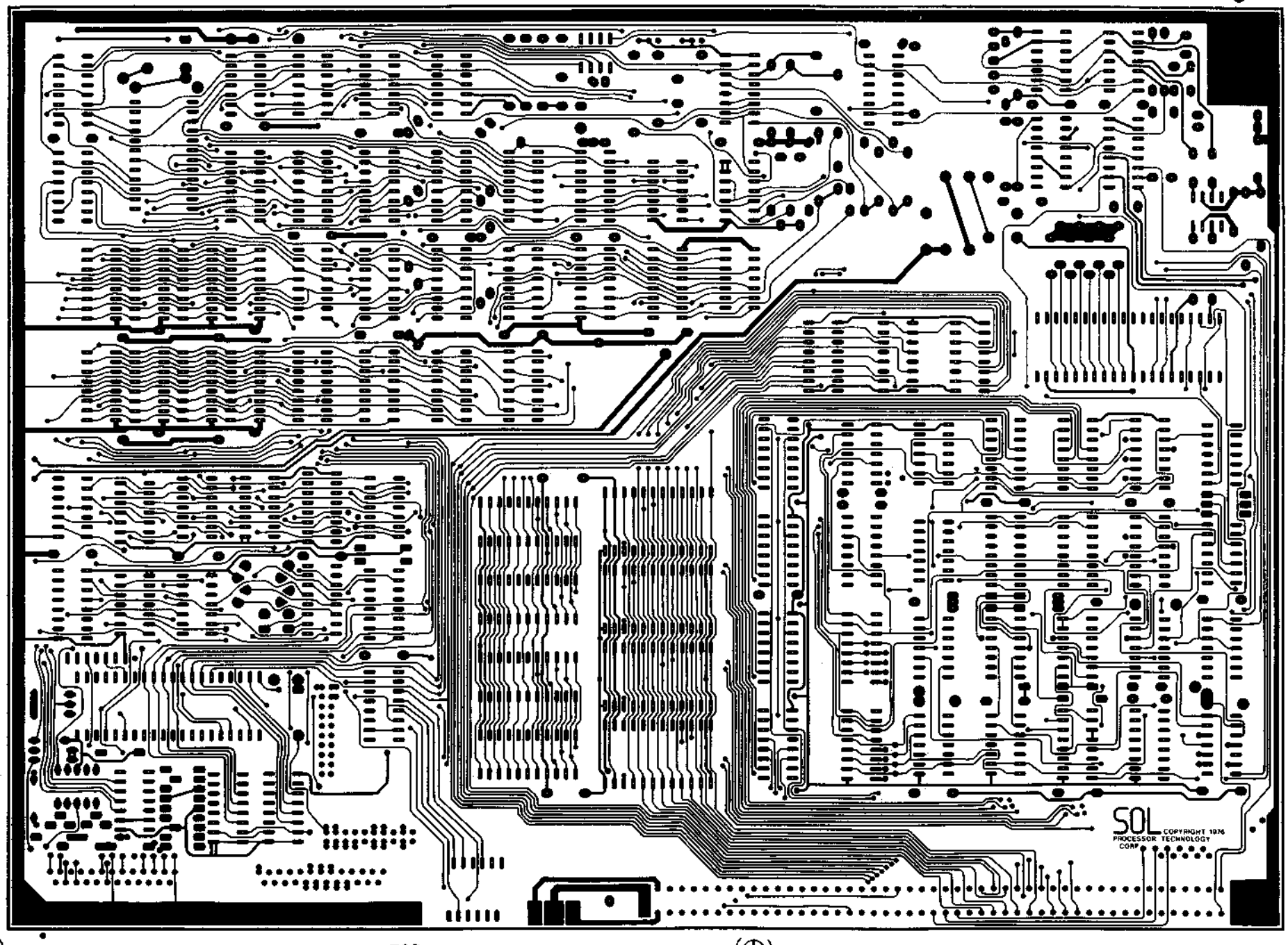
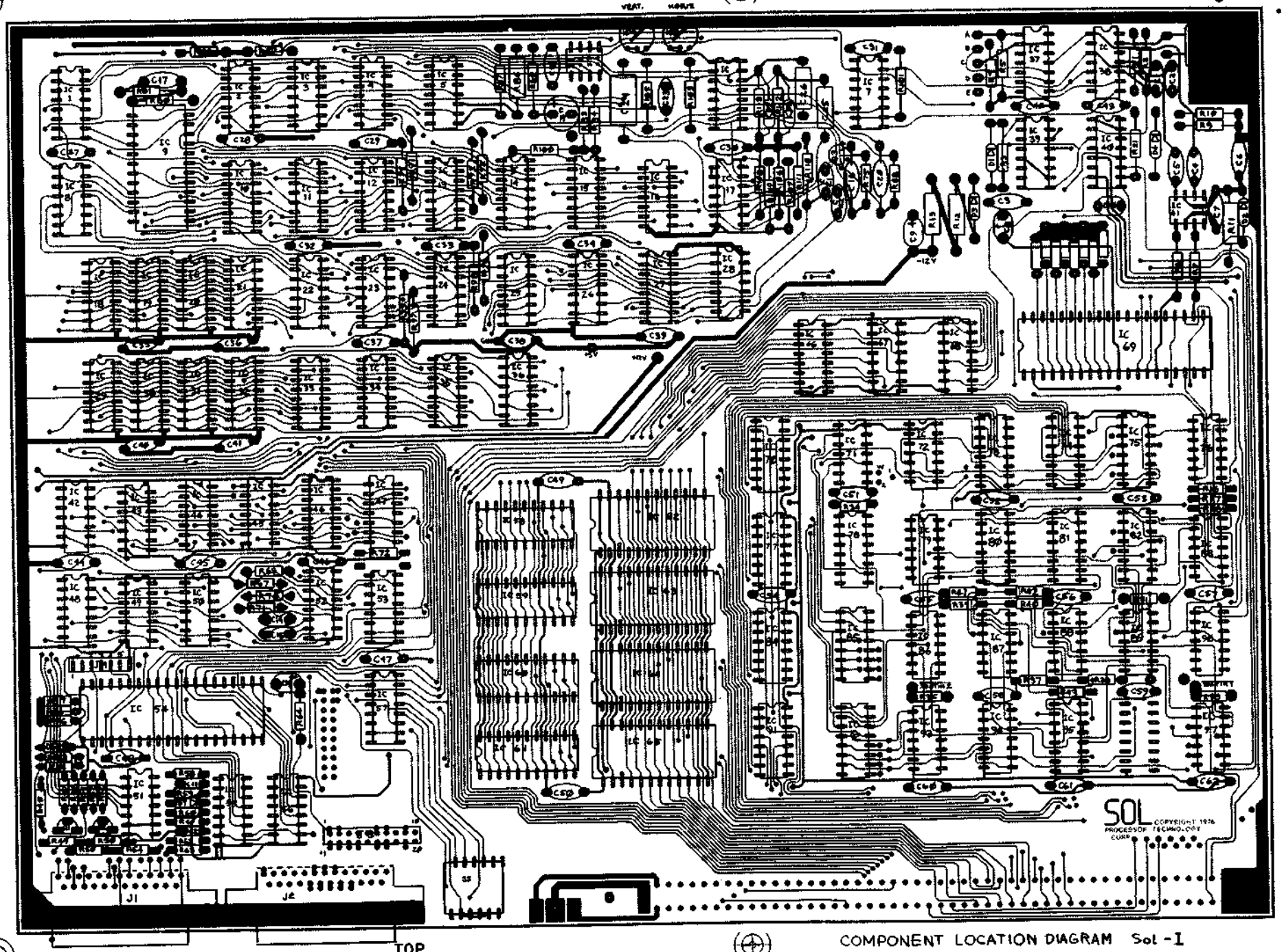


TOP

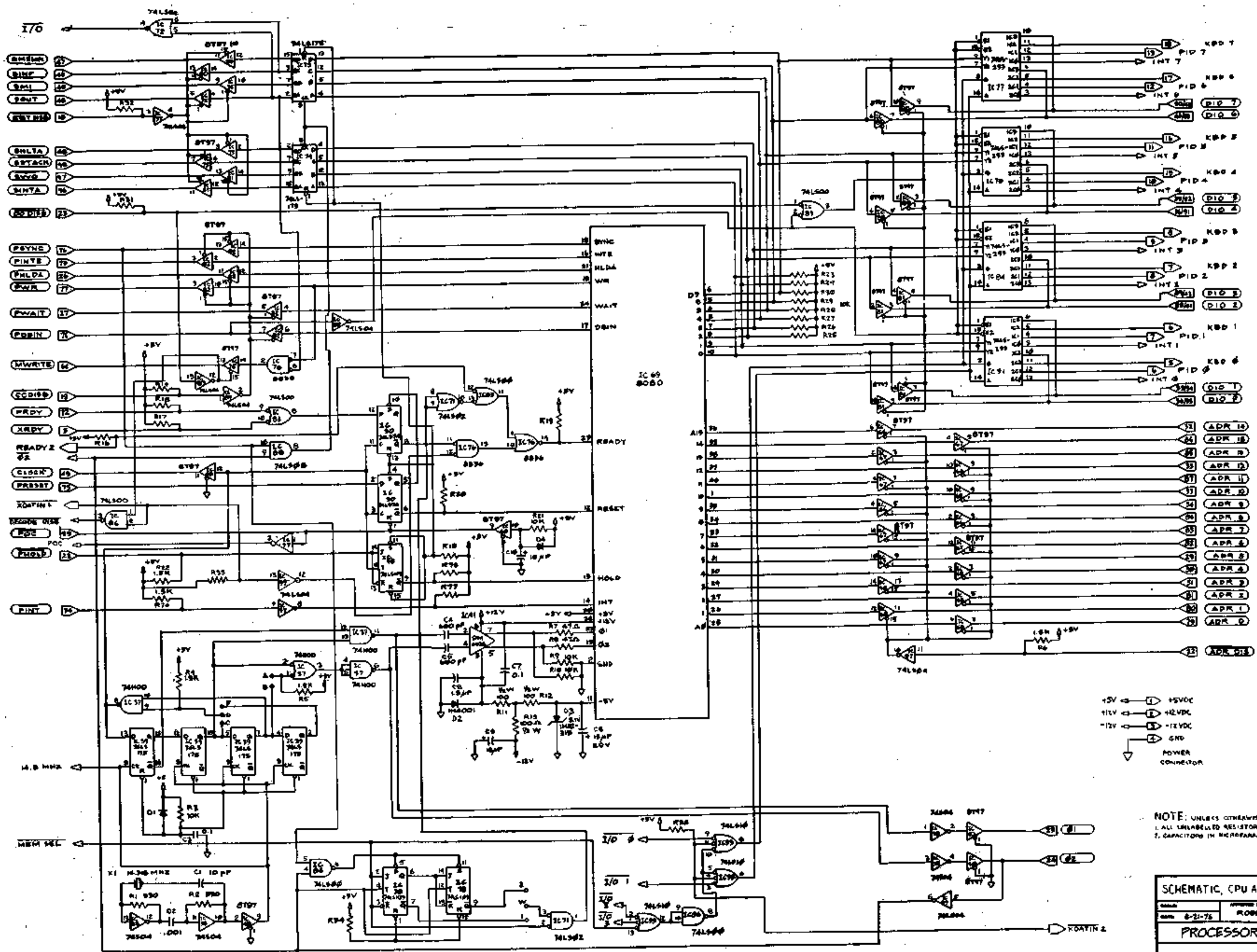


TOP

9.50"
13.25"
BOTTOM

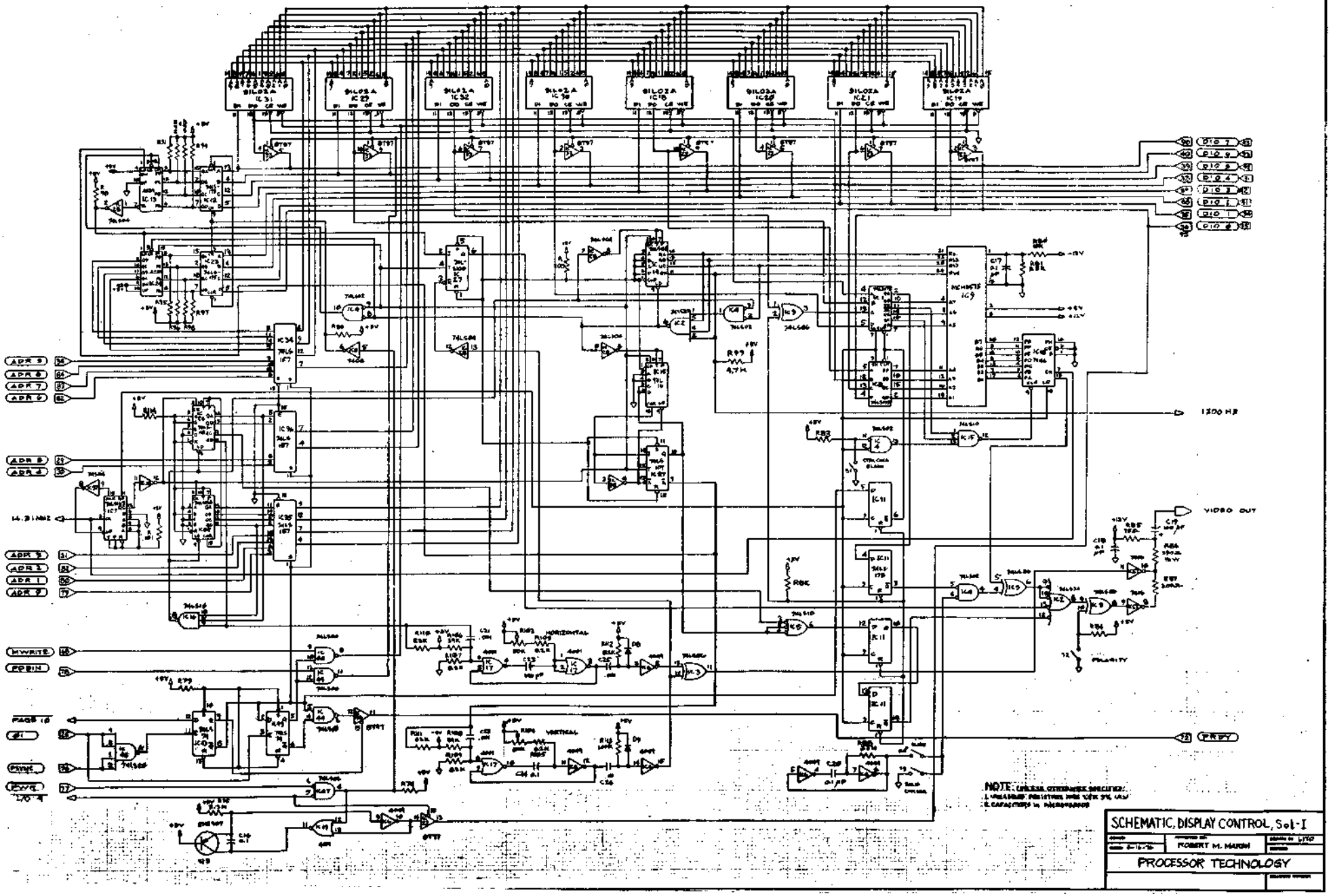


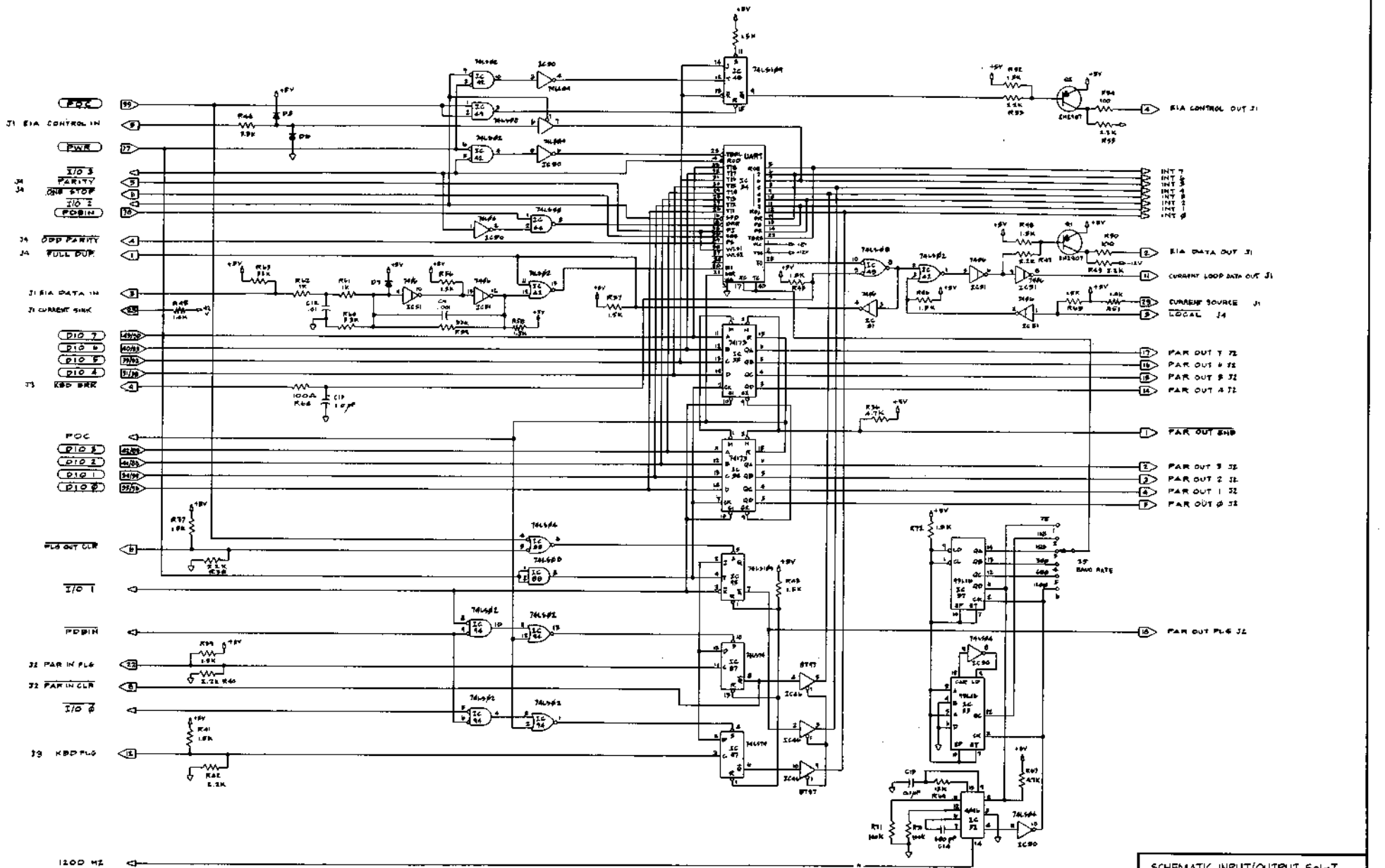
COMPONENT LOCATION DIAGRAM Sol-1



NOTE: UNLESS OTHERWISE SPECIFIED:
1. ALL UNLABELLED RESISTORS 4.7 K 1/4W 5%
2. CAPACITORS IN MICROFARADS

SCHEMATIC, CPU AND BUS, Sol-I		
	ROBERT M. MARSH	
8-21-76		
PROCESSOR TECHNOLOGY		

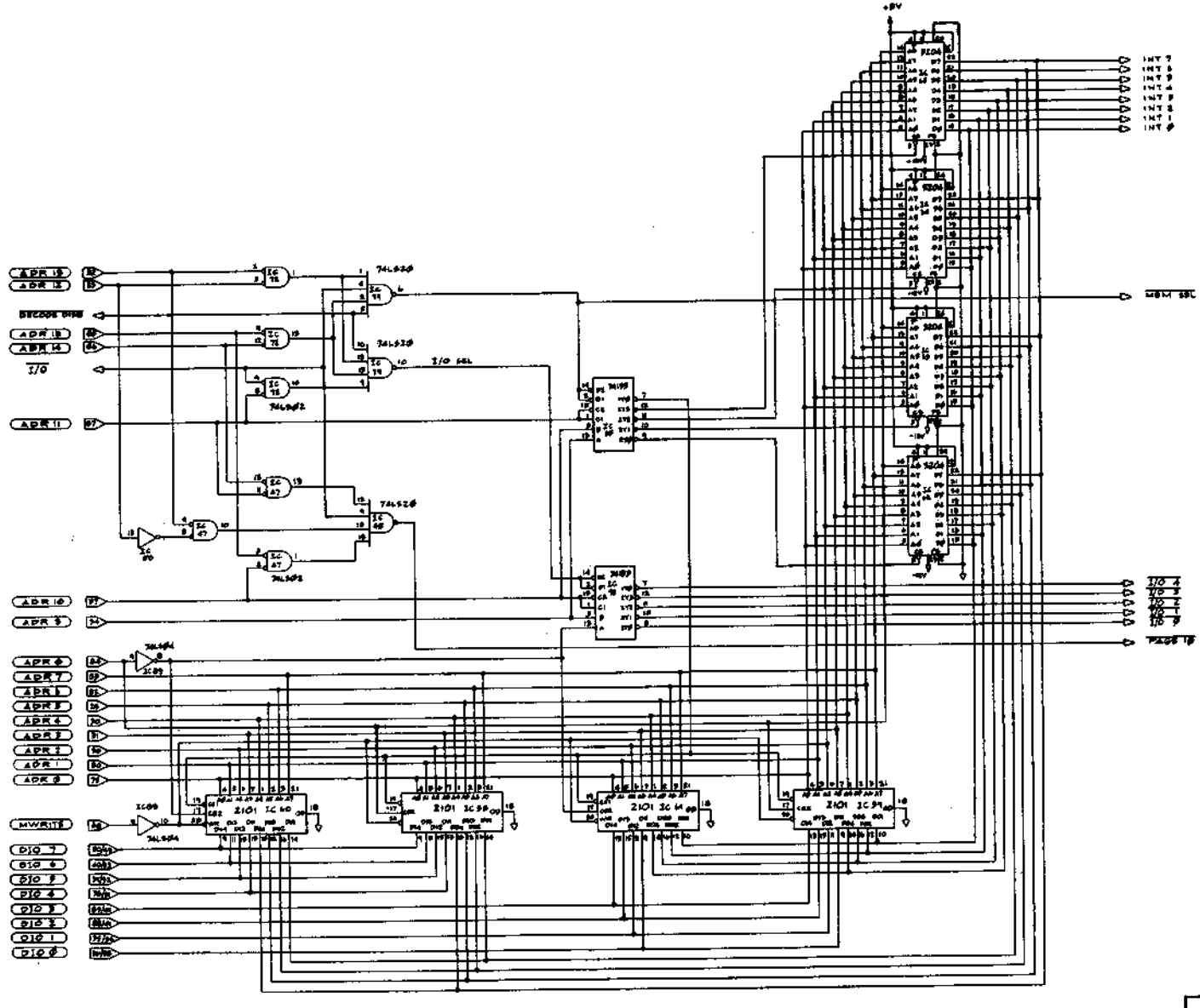

SCHEMATIC, DISPLAY CONTROL, Sol-I
ROBERT M. MARSH
PROCESSOR TECHNOLOGY
1300 HZ
VIDEO OUT
14.31 MHZ
HORIZONTAL
VERTICAL



SCHEMATIC, INPUT/OUTPUT, SOL-I

DATE 9-24-76	APPROVED BY: ROBERT M. MARSH	DRAWN BY LITO

PROCESSOR TECHNOLOGY



SCHEMATIC, MEMORY, Sol -I

DRAWN 6-22-76	APPROVED BY ROBERT M MARSH	RELEASED BY ENG

PROCESSOR TECHNOLOGY