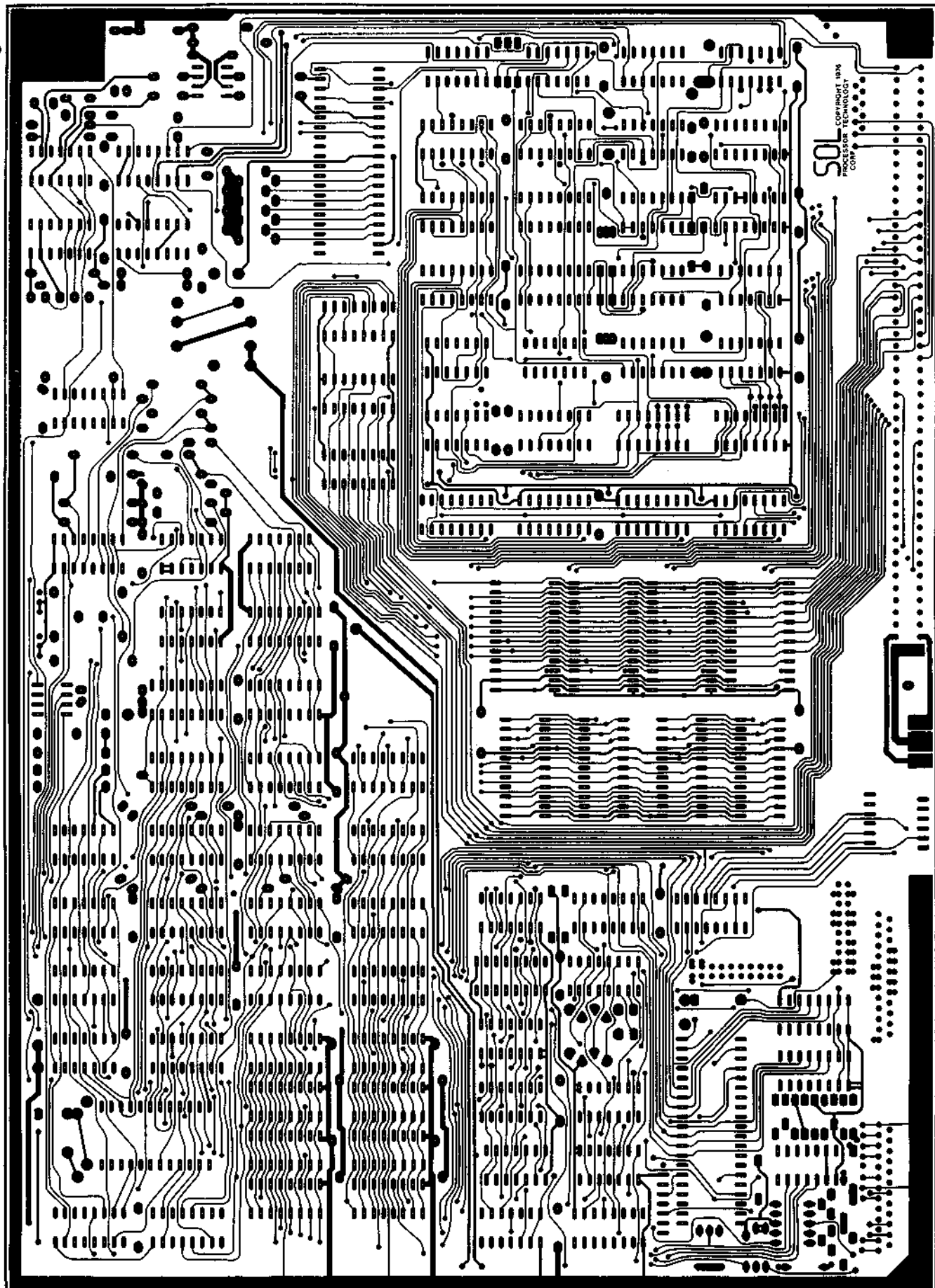


501
COPYRIGHT 1974
PERMISSION TECHNOLOGY
COMPANY

CC 2256

SOL
CORPORATION
PROCESSOR TECHNOLOGY

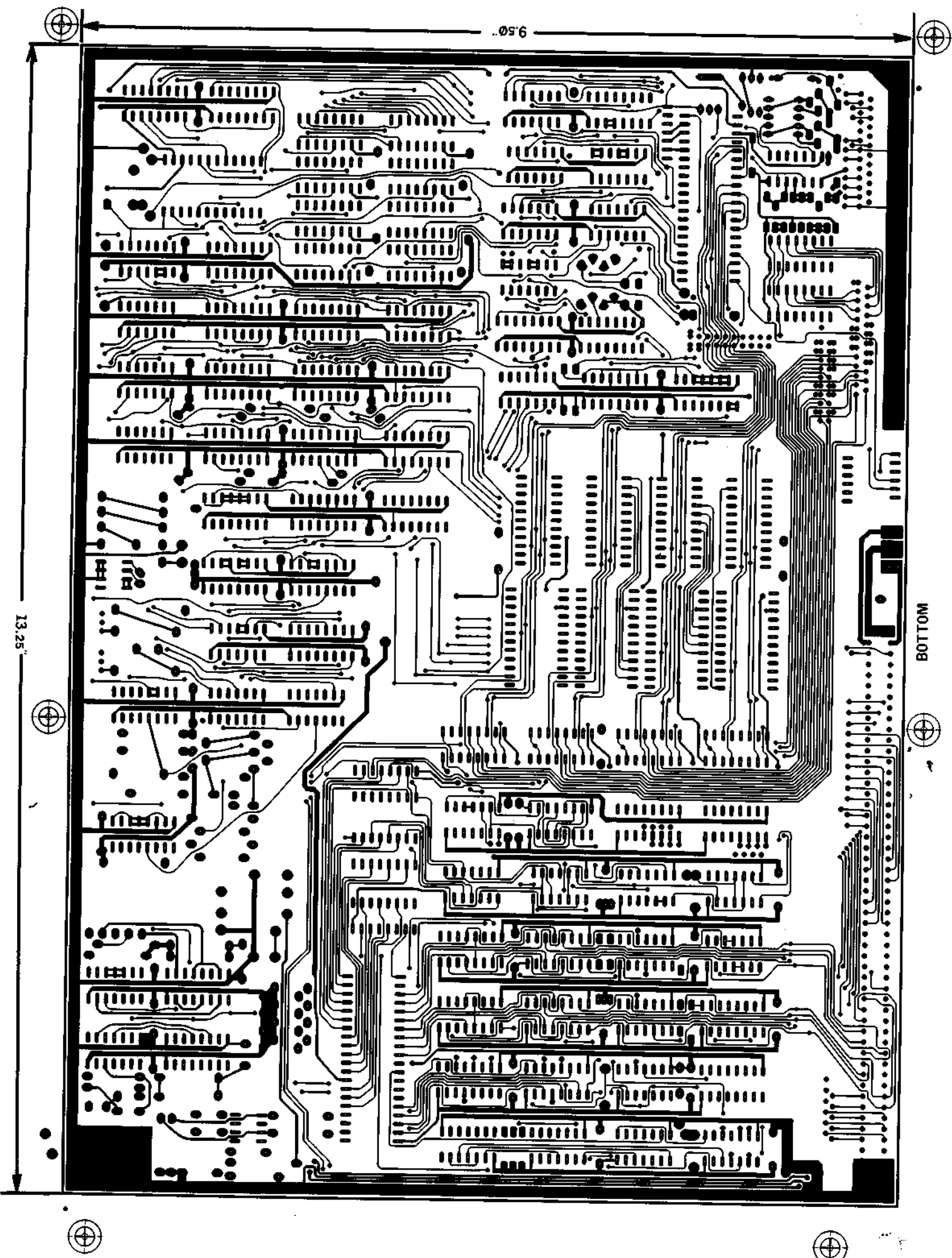
TOP

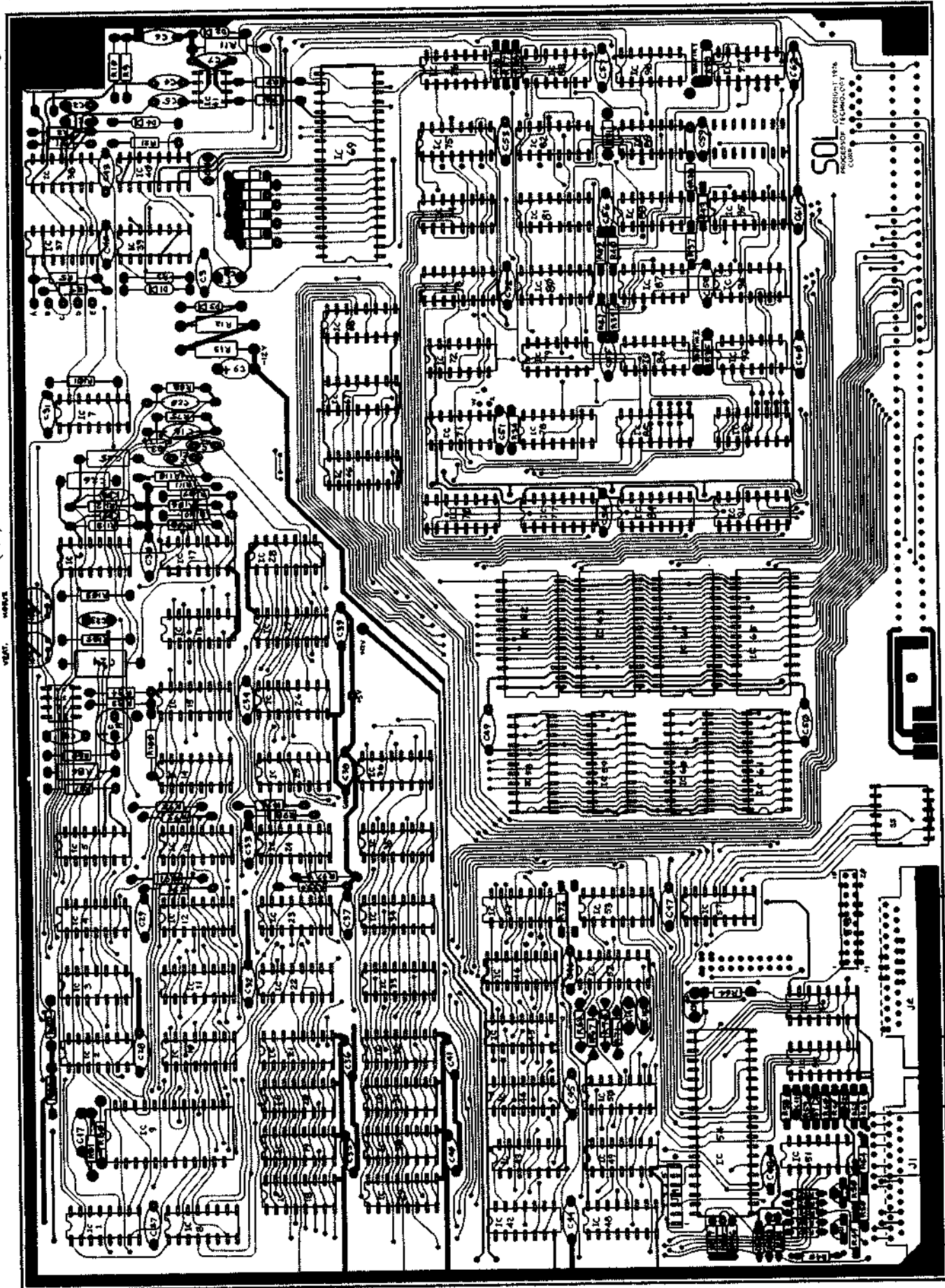


056

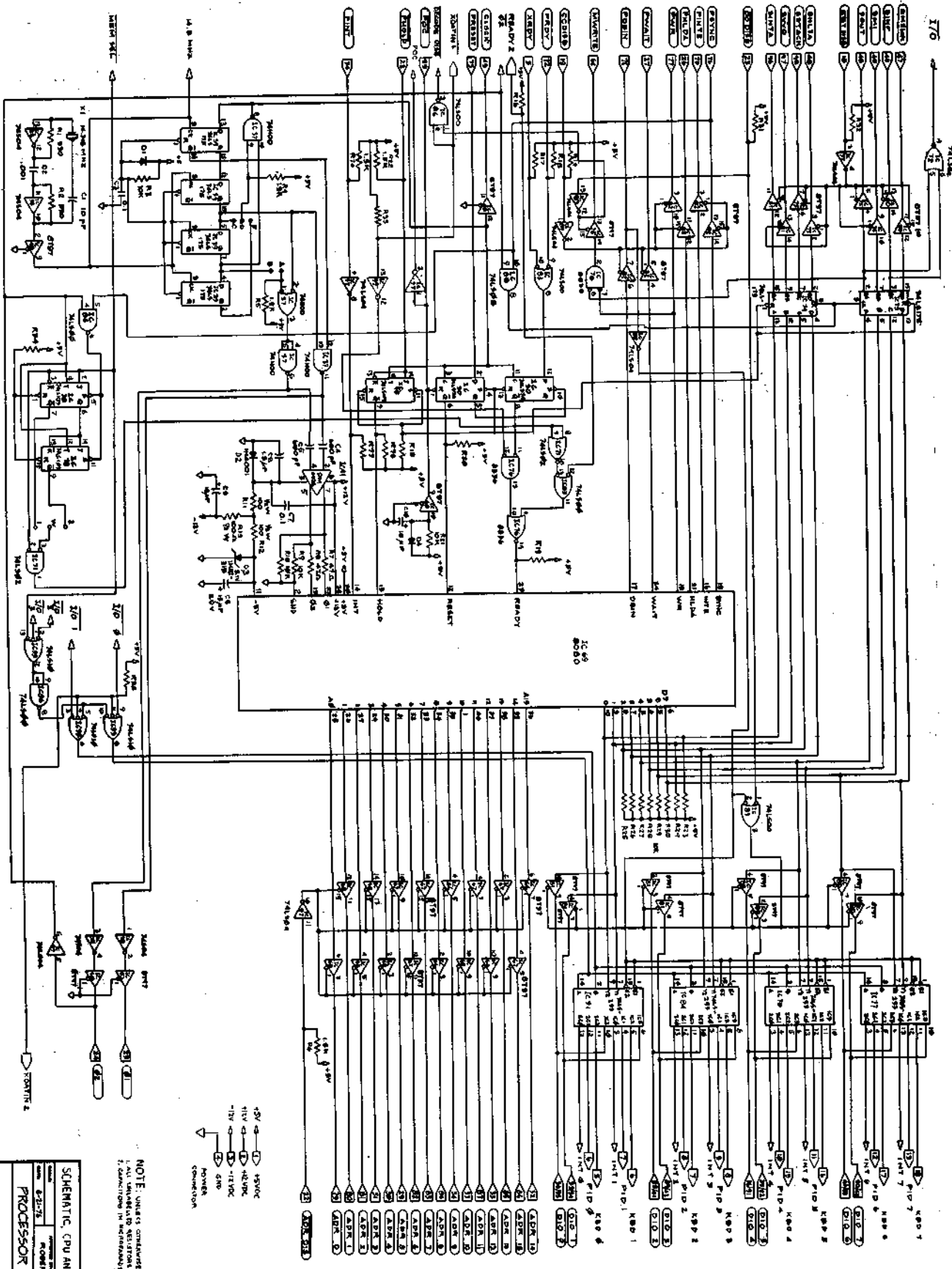
13.25

BOTTOM





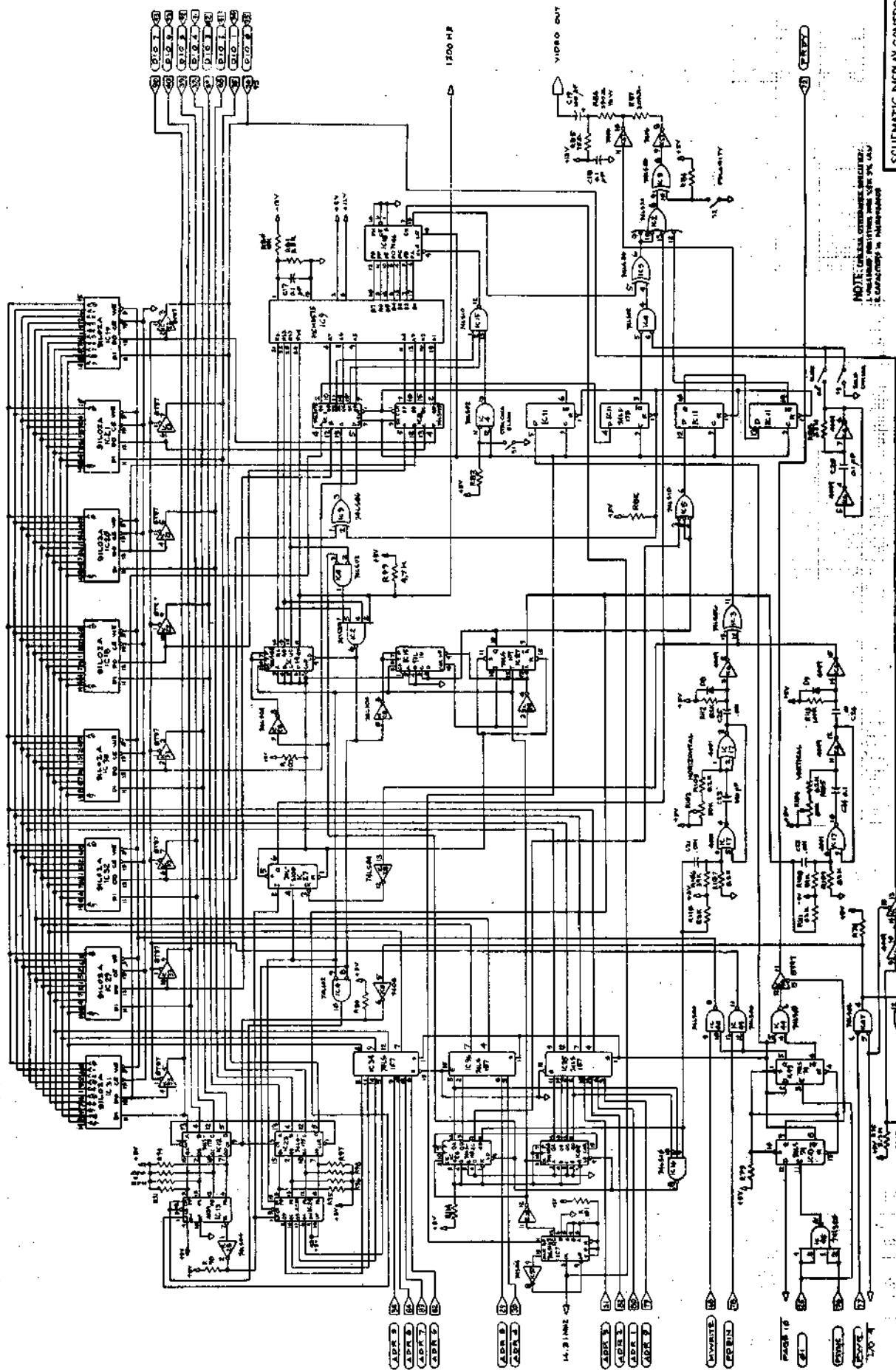
COMPONENT LOCATION DIAGRAM Sol - I



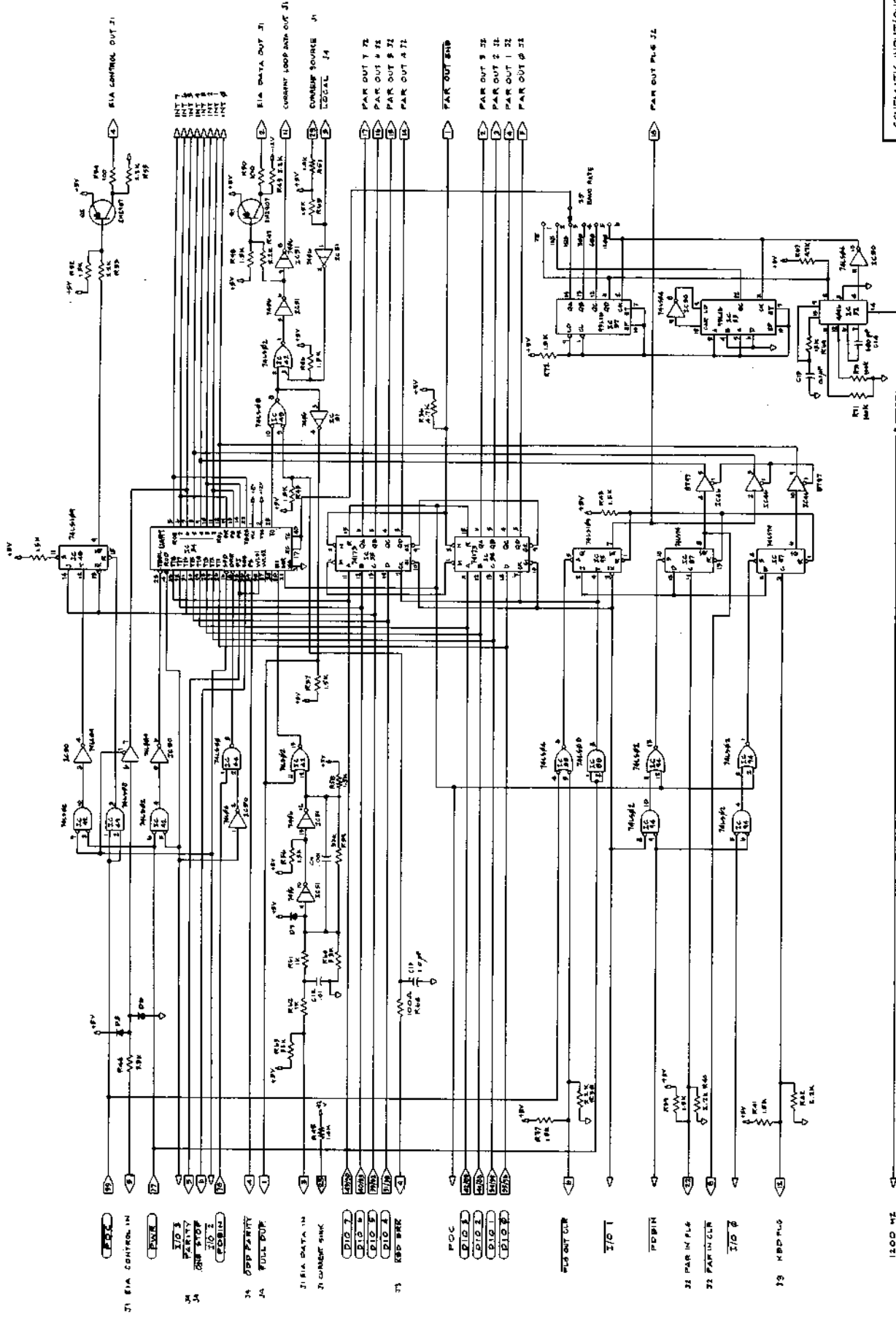
NOTE: UNLESS OTHERWISE SPECIFIED,
 1. ALL UNDIMENSIONED MEASUREMENTS ARE IN MILLIMETERS.
 2. CONNECTIONS IN RED ARE FOR THE BOARD.

+5V → 5VREG
 +12V → 12VREG
 -12V → -12VREG
 → GND
 ▲ POWER CONNECTION

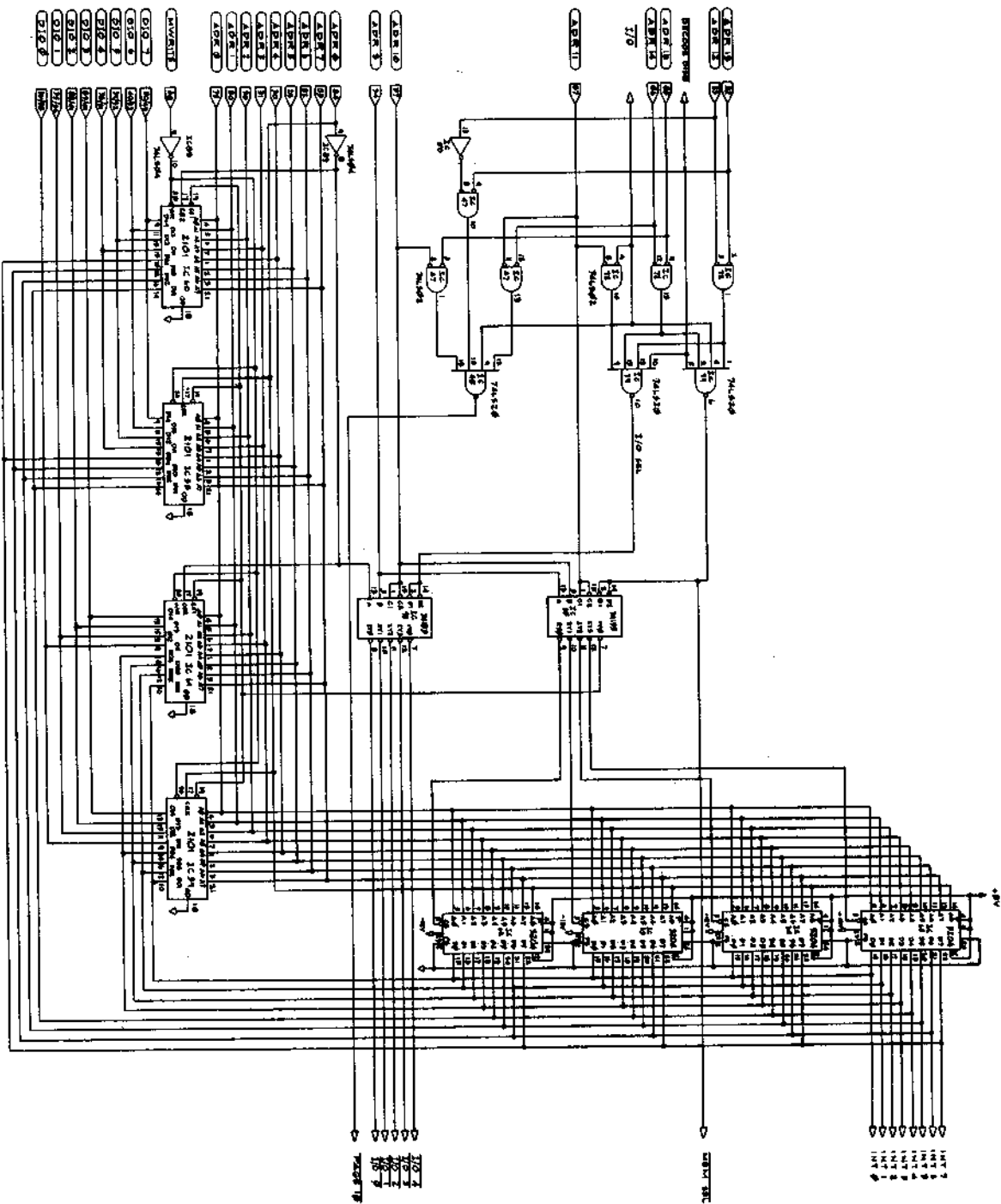
SCHEMATIC: CPU AND BUS, Sol-1
 DATE: 8-21-78
 ROBERT W. FRANK
 LITTON
 PROCESSOR TECHNOLOGY



NOTE: CHECK ALL CONNECTIONS CAREFULLY.
 1. VERIFY ALL CONNECTIONS WITH DATA SHEET.
 2. CONFIRM ALL CONNECTIONS.



SCHEMATIC INPUT/OUTPUT, 501-1
 ROBERT H. MARSH
 PROCESSOR TECHNOLOGY



SCHEMATIC MEMORY, 501-I
 MODEL 5-327-76
 ROBERT N. MARSH
 PROCESSOR TECHNOLOGY
 1976