3P+S INPUT/OUTPUT MODULE

ASSEMBLY and OPERATING INSTRUCTIONS

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PROCESSOR TECHNOLOGY CORPORATION

SECTION I

INTRODUCTION and GENERAL INFORMATION

3P+S INPUT/OUTPUT MODULE

1.1 INTRODUCTION

This manual supplies the information needed to assemble, test and use the 3P+S Input/Output Module. We suggest that you first scan the entire manual before starting assembly. Then make sure you have all the parts and components specified in the "Parts List" (see Page II-2). When assembling the module, follow the instructions in the order given.

Should you encounter any problem during assembly, call on us for help if necessary. If your completed module does not work properly, recheck your assembly step by step. Most problems stem from backward installed components and/or installing the wrong component. Once you are satisfied that the module is correctly assembled, feel free to ask for our help.

1.2 GENERAL INFORMATION

1.2.1 3P+S Description

The 3P+S Input/Output Module is designed to meet all the I/O needs of most 8800 system users. For example, one teletype and two TV typewriters with keyboards can operate simultaneously with the 8800 through only one 3P+S. Similarly, one RS-232-C modem, a teletype, and one TV typewriter plus another parallel data device can all be interfaced with one 3P+S at the same time.

One parallel port is available to set up control conditions for both parallel and serial ports, as well as to set the serial I/O baud rate under program control. The baud rate can be set from 35 to 9600 Baud. Another parallel port allows polling the input data available flags and external device ready flags. This port also permits checking the serial I/O error flags. Full handshaking with both input and output peripherals can be implemented.

Module addressing is jumper selectable to any one of 64 address segments within the 8800 range of 256 I/O addresses. Additional flexibility allows either the UART (Universal Asynchronous Receiver Transmitter) and control port or the two parallel ports to occupy the lower two relative addresses.

Interfacing to the 8800 vectored interrupt bus is provided as a jumper selectable option. Any of the UART error flags or handshaking signals can be used to generate interrupts. A Vectored Interrupt Module, however, is required for this purpose.

1.2.2 Receiving Inspection

When your module arrives, examine the shipping container for signs of possible damage to the contents during transit. Then inspect the contents for damage. (We suggest you save the shipping materials for use in returning the module to Processor Technology

should it become necessary to do so.) If your 3P+S kit is damaged, please write us at once describing the condition so that we can take appropriate action.

If there is no apparent damage, check that your kit has the correct number of component containers and materials. There should be three trays of integrated circuits, six bags of components and hardware, 4-feet of flat cable and a PC (printed circuit) board. Let us know of any shortages so that we can supply the needed materials.

1.2.3 Warranty Information

In brief, the parts supplied with the module, as well as the assembled module, are warranted against defects in materials and workmanship for a period of 6 months after the date of purchase. Refer to Appendix I for the complete "Statement of Warranty".

1.2.4 Replacement Parts

Order replacement parts by component nomenclature (e.g., SN74175) and/or a complete description (e.g., 6.8 ohm, ½ watt, 5% resistor).

1.2.5 Factory Service

In addition to in-warranty service, Processor Technology also provides factory repair service on out-of-warranty products. Before returning the module to Processor Technology, first obtain authorization to do so. After the return is authorized, proceed as follows:

1. Write a letter describing the problem.

2. Pack the module with the letter in a container suitable to the method of shipment.

3. Ship prepaid to Processor Technology, 2465 Fourth Street, Berkeley, CA 94710.

Your module will be repaired as soon as possible after receipt and return shipped to you prepaid.

SECTION II

ASSEMBLY
and
TEST

3P+S INPUT/OUTPUT MODULE

2.1 ASSEMBLY

CAUTION

THIS DEVICE USES A MOS INTEGRATED CIRCUIT WHICH CAN BE DAMAGED BY STATIC ELECTRICITY DISCHARGES. AVOID UNNECESSARY HANDLING OF THIS I.C. AND WEAR COTTON CLOTHING, RATHER THAN SYNTHETICS, WHEN HANDLING IT.

2.1.1 Parts and Components

Check all parts and components against the "Parts List" (Table 2-1). If you have difficulty in identifying any parts by sight, refer to Figure 2-1.

2.1.2 Orientation

The heat sink area will be located in the lower left-hand corner of the board when the 100-pin edge connector is on the lower edge of the card. J1 is the 44-pin edge connector at the upper left; J2 is the 44-pin edge connector at the upper right.

2.1.3 Integrated Circuit Installation

NOTE

To facilitate IC replacement, we recommend that you install DIP sockets in all IC locations on the PC board. (Except for the UART socket, IC sockets are not included in your kit.) If you elect to install sockets, make the installations before performing any of the subsequent assembly steps.

Refer to the component location diagram in Section V and the instructions on installation of DIP devices in Appendix III. Install the following I.C.'s in the indicated locations. Pay careful attention to the proper orientation.

I.C. NO.	TYPE	ORIENTATION
IC 1	74177	Pin 1 lower left
IC 2	74177	" " " "
IC 3	74177	" " " "
IC 4	74177	" " " "
IC 5	MC1488	" " " "
IC 6	74175	" " upper left
IC 7	93L16	" " lower left
IC 8	93L16	" " " "
IC 9	93L16	" " " "

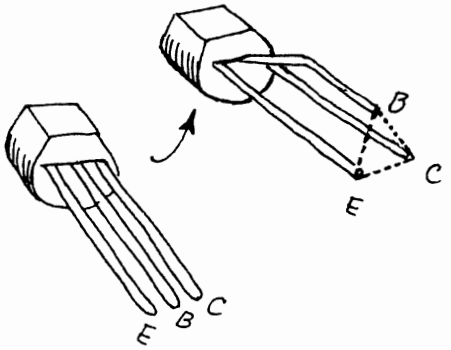
Table 2-1. Parts List: 3P+S I/O Module

INTEGRATED CIRCUITS

Tray #1		Tray #2		Tray #3	
1	DM 7400 or 74LS00	1	DM74155 or 74LS155	1	1488PC
2	DM 7406	1	DM74175 or 74LS175	1	1489APC
2	N74LS08	1	DM74109 or DM8124N or 74LS109	1	DM8131
4	DM74177	3	93L16PC or 74LS163	1	DM8836 or 8T380
		4	AM25LS153PC	1	DM8837 or 8T37
				2	DM8097 or 74367 or 8T97

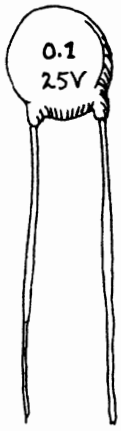
OTHER COMPONENTS and MATERIALS

Bag #1:	Capacitors	3	1 mfd dipped tantalum electrolytic
		3	15 mfd dipped tantalum electrolytic
		19	0.1 mfd disc ceramic capacitor
Bag #2:	Resistors	1	6.8 ohms ½ watt 5%
		3	330 ohms ¼ watt 5%
		2	4.02k ohms ¼ watt 1%
		2	100 ohms ¼ watt 5%
		5	1.0k ohms ¼ watt 5%
		8	2.2k ohms ¼ watt 5%
		1	1N4148 DIODE
Bag #3:	Hardware	1	78L12ACZ
		1	LM340T-5.0 or 7805UC
		2	2N2222 transistors
		3	2N2907 transistors
		3	6-32 screw nut, lock washer sets
			solder
			bare jumper wire
			spaghetti
Bag #4:	Sockets	6	Augat pins in carriers
		1	40 DIP
Bag #5:	UART	1	AMI S1883 UART or TMS6011NC
Bag #6:	Heatsink	1	
	Flat cable	4	feet
	PC Board	1	
	Manual	1	

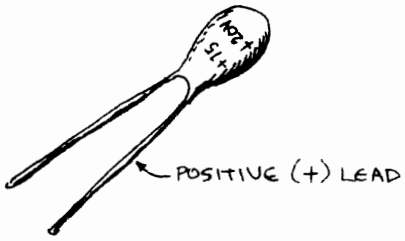


transistor - TO-92 package (plastic)

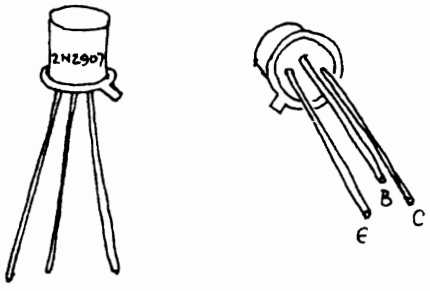
transistor - TO-18 package (metal can)

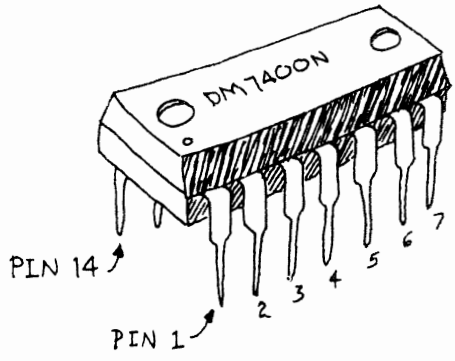


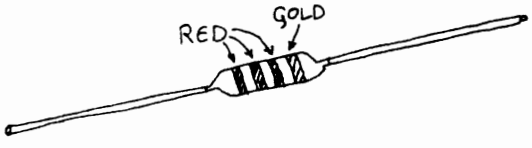
ceramic disc capacitor



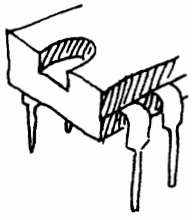
dipped tantalum electrolytic capacitor

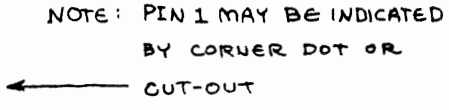






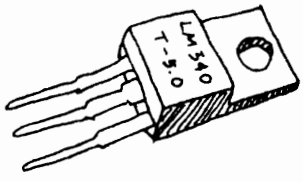
carbon film resistor 5% (gold) or 10% (silver)





dual-inline-package (DIP) integrated circuit
8,14,16,24 or 40 pins (14 pin shown)

metal film 1% precision resistor



regulator IC or power transistor (TO-220)

Figure 2-1. Identification of components.

I.C. NO.	TYPE	ORIENTATION
IC 10	MC1489	Pin 1 lower left
IC 11	74LS153	" " upper left
IC 12	74LS153	" " " "
IC 13	74LS153	" " " "
IC 14	74LS153	" " lower left
IC 15	74109	" " upper left
IC 16	not installed this step	
IC 17	not installed this step	
IC 18	LM741C	" " " "
IC 19	Install only if your computer has a vectored interrupt capability. (Specific installation instructions will be the subject of a technical bulletin as soon as information on the vectored interrupt module becomes available.)	
IC 20	74155	Pin 1 lower left
IC 21	7400	" " " "
IC 22	DM8836	" " upper left
IC 23	DM8837	" " lower right
IC 24	DM8131	" " " "
IC 25	40-pin socket	no orientation
IC 26	74LS08	Pin 1 lower left
IC 27	74LS08	" " " "
IC 28	DM8097	" " upper left
IC 29	DM8097	" " lower left
IC 30	7406	" " " "

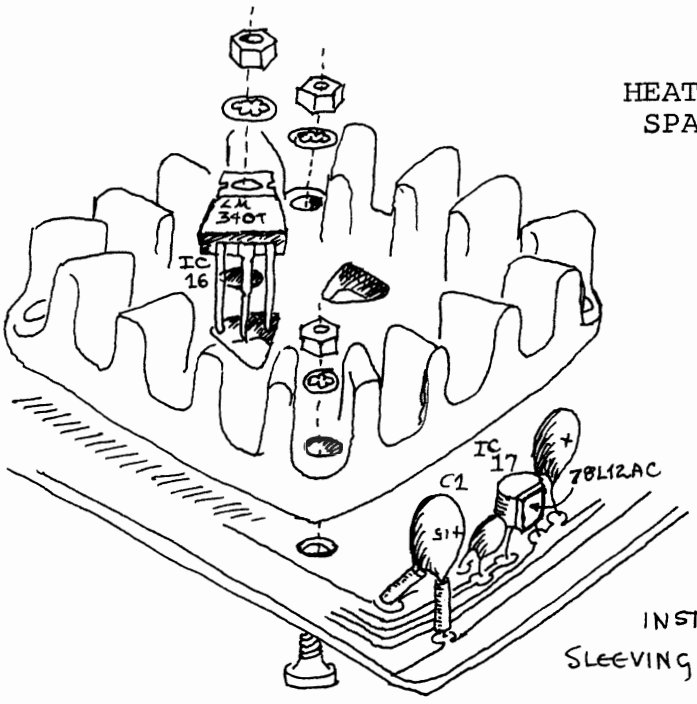
Check for proper position and orientation. Then solder all IC's. (See Appendix III.) Avoid creating "solder bridges" between adjacent pins of IC's and between pins and traces which run between pins.

2.1.4 Heat Sink Installation

Refer to Figure 2-2 and component location diagram (Section V). Position the large, black heat sink (flat side to the board) over the square foil area on the lower left corner. Orient the sink so that the triangle of holes is under one of the triangular cut-outs in the sink. Using 6-32 screws, nuts, and lockwashers, attach the heat sink to the board, inserting the screws from the back side of the board.

2.1.5 Electrolytic Capacitor Installation

Refer to component location diagram in Section V. Install dipped, upright tantalum electrolytic capacitors in the following locations. Take care to observe the proper values and orientations.



HEATSINK, REGULATOR, and SPAGHETTI INSTALLATION

Figure 2-2

CAPACITOR	VALUE	ORIENTATION
C1 .(See Figure 2-2)	.15 uf	"+" lead down
C2	.15 uf	"+" lead lower left
C3	1.0 uf	"+" lead top
C4	1.0 uf	"+" lead down
C5	1.0 uf	"+" lead down
C6	.15 uf	"+" lead left

Check the capacitors for proper value and orientation, and solder.

2.1.6 Disc Capacitor Installation

Refer to the component location diagram in Section V. Install 0.1 uf disc ceramic capacitors in locations C7 through C25. Take care to mount the capacitor leads in the proper holes. After mounting each capacitor, bend the leads outward underneath the board, solder and trim.

2.1.7 Resistor Installation

Refer to the component location diagram in Section V. Install the following resistors in the indicated locations.

LOCATION	VALUE	COLOR CODE
R1	4020 ohms	4021F
R2	4020 ohms	4021F
R3	100 ohms	brown-black-brown
R4	6.8 ohms	blue-grey-gold
R5	2.2 kohms	red-red-red
R6	2.2 kohms	red-red-red
R7	1.0 kohms	brown-black-red
R8	1.0 kohms	brown-black-red
R9	1.0 kohms	brown-black-red
R10	not installed this step	
R11	2.2 kohms	red-red-red
R12	330 ohms	orange-orange-brown
R13	330 ohms	orange-orange-brown
R14	100 ohms	brown-black-brown
R15	1.0 kohms	brown-black-red
R16	2.2 kohms	red-red-red
R17	2.2 kohms	red-red-red
R18	330 ohms	orange-orange-brown
R19	2.2 kohms	red-red-red
R20	2.2 kohms	red-red-red
R21	1.0 kohms	brown-black-red

Take particular care to install R5, R8, R12, R13, R19 and R20 in the proper holes.

After checking the location and value of all resistors, solder and trim.

2.1.8 Diode and Transistor Installation

Refer to the component location diagram in Section V and the diagram on transistor lead identification (Figure 2-1).

Install diode CR1 in the location indicated by the diode symbol on the component location diagram. The end of the diode with the band marked on it is installed toward the left. Solder and trim the leads.

Install 2N2907 transistors Q1, Q2, Q3 in the locations indicated. The emitter lead is oriented to the left and the base lead is oriented downwards. Push straight down on the transistors until they are stopped by their leads. Install jumper between Q2 emitter and R1 as shown in Figure 2-3. Solder and trim all leads.

Install 2N2222 transistors Q4 and Q5 (See Figure 2-4.) in the locations indicated. The emitter lead of Q4 is oriented to the lower right; the emitter lead of Q5 is oriented toward the top. Push straight down on the transistors until they are stopped by their leads. Solder and trim the leads.

REAR OF BOARD, LOWER RIGHT-HAND CORNER:

(100-pin Edge Connector positioned at bottom)

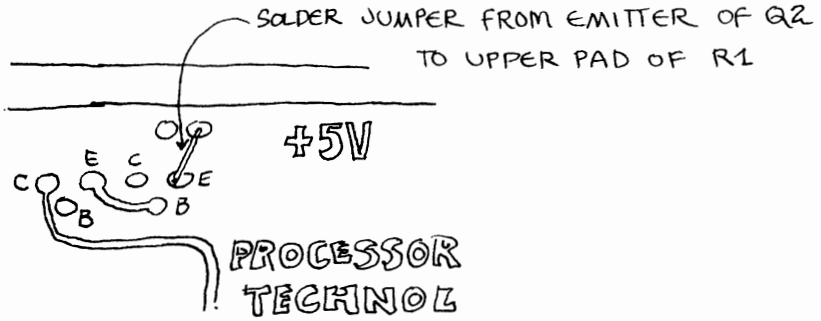
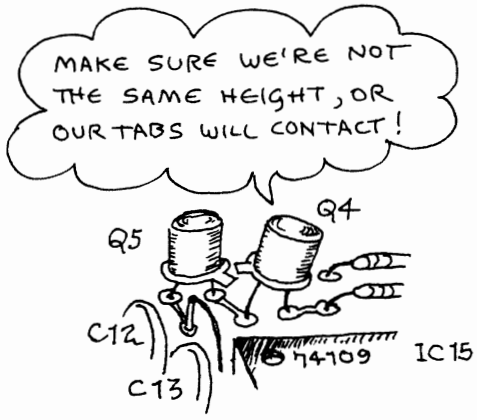


Figure 2-3



TRANSISTOR INSTALLATION, Q4 and Q5 PRECAUTIONS

Figure 2-4

2.1.9 R10 Installation

Before installing R10, refer to Paragraph 3.1.3 in Section III. Connect upper lead of R10 as shown in the component location diagram in Section V. If bit Ø is to be the input for Q3, the peripheral control driver, connect the lower lead of R10 to the lefthand terminal in Area F. Connect the lower lead of R10 to the righthand terminal in Area F if bit 1 is selected as the input to Q3.

2.1.10 Regulator Installation

Refer to Figure 2-2 and the component location diagram (Section V). Position regulator IC 16 (LM340T) as shown and observe how the leads must be bent to fit the holes. Note that the center lead (3) must be bent downwards at a point approximately 0.2 inches further from the body than the other leads. Bend the leads so that no

contact is made with the heat sink when the regulator is flat against the heat sink and its mounting hole is aligned with the hole in the heat sink. Fasten the regulator to the heat sink using a 6-32 screw, lockwasher and nut. Insert the screw from the back side of the board. Solder and trim the leads.

Install regulator IC 17 (78L12AC) as shown, with the flat face oriented downwards. Bend the center lead back to fit into the hole indicated. Push straight downwards until the IC is stopped by its leads. Solder and trim the leads.

2.1.11 Jumper Installation

There is only one permanent wire jumper on this device. It is located in the center of the board and is oriented vertically. Install a piece of insulated wire as shown in the component location diagram and solder. Trim the ends.

2.1.12 UART Installation

Refer to the component location diagram and the cautionary note at the beginning of this Section. The UART (IC 25, S1883) is a MOS device. Set the board on a flat surface and carefully position the UART on its socket, with pin 1 oriented toward the upper right. Gently insert all of the pins of the UART into the entries of the socket and check to be sure that no pin is obstructed. Press downward on the UART chip with an even, firm pressure until it seats. Excessive pressure may indicate a blocked pin, which can bend or break. Inspect the UART chip after installation for any possible bent pins.

2.1.13 Ribbon Cable Jumper Installation

This jumper connects the inputs to IC 19 and the VI bus terminals in Area G.

NOTE

Install this jumper only if your computer has a vectored interrupt capability.

Refer to component location diagram in Section V. On the back (solder) side of the board, install a piece of ribbon cable (approximately 8" long) between the VI bus (Ø thru 7) in Area G and V INT terminals (Ø thru 7). (The V INT terminals are to the immediate right--as viewed from component side of board--of IC 19.) To ensure correct terminal-to-terminal interconnection, make a 90° fold in the cable below the VI bus in Area G. This technique is clearly illustrated in Figure 2-5.

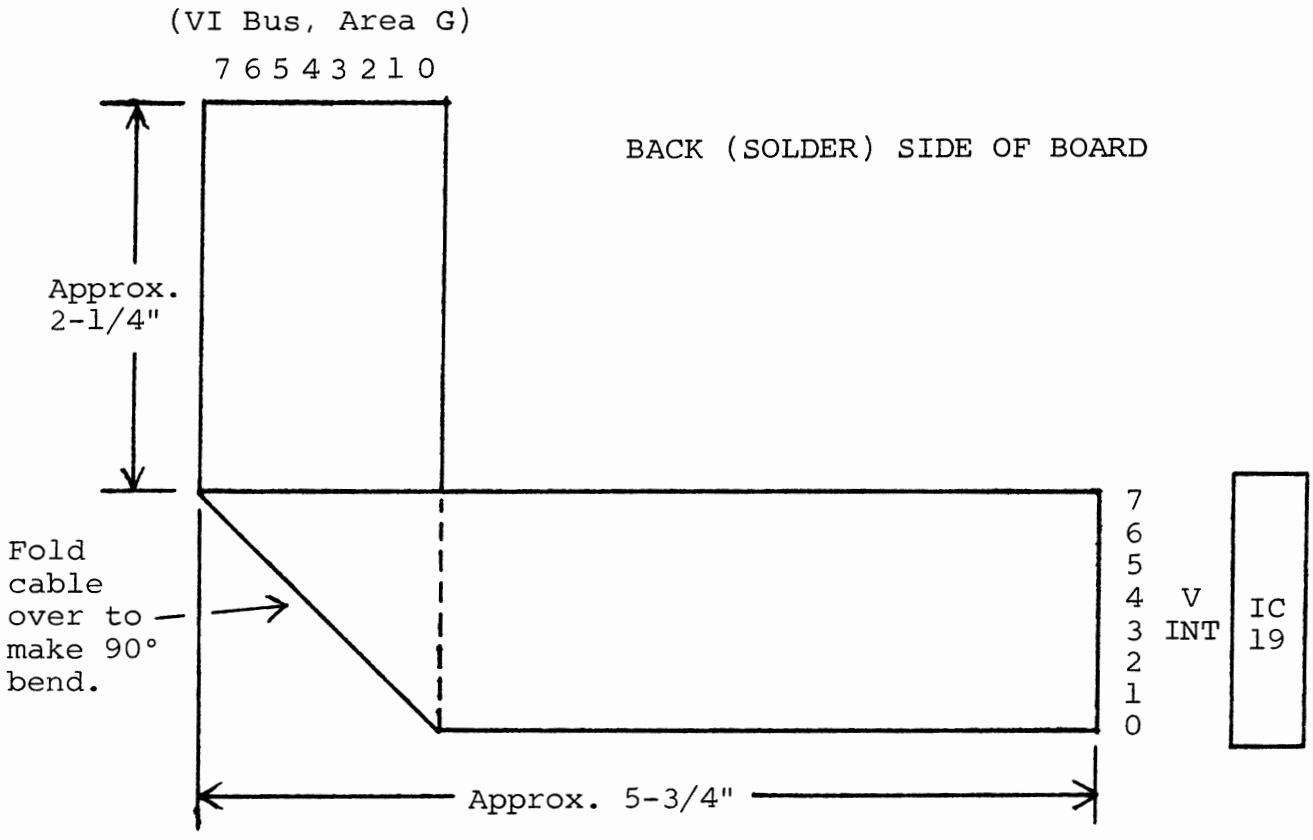

(VI Bus, Area G)
7 6 5 4 3 2 1 0
BACK (SOLDER) SIDE OF BOARD
Approx.
2-1/4"
Fold
cable
over to
make 90°
bend.
7
6
5
4
3
2
1
0
V
INT
IC
19
Approx. 5-3/4"

Figure 2-5

2.2 TEST

The test procedure for the 3P+S Input/Output Module checks the various input/output ports.

2.2.1 Output Ports A and B, Test No. 1

Install 3P+S in computer. Execute Test No. 1 program given in Appendix V.

2.2.2 Input Ports, Test No. 2

With 3P+S installed in computer, execute Test No. 2 program given in Appendix V.

2.2.3 Serial Input/Output, Test No. 3

With 3P+S installed in computer, execute Test No. 3 program given in Appendix V.

SECTION III

OPTION SELECTION

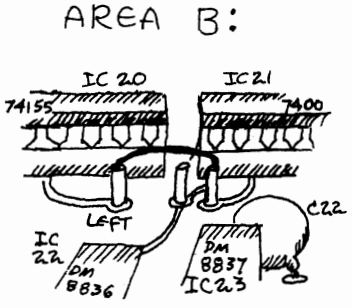
3P+S INPUT/OUTPUT MODULE

3.1 OPTION SELECTION

3.1.1 Address Selection

The 3P+S will respond to addresses up to 256 in 64 groups of four. Within each group of four, the order of response of the four I/O channels may be changed by jumper selection in Area B (See Figure 3-1.) as shown by the following table:

ADDRESS BITS AØ	ADDRESS BITS A1	CHANNEL SELECTED (left jumpered to center)	CHANNEL SELECTED (left jumpered to right)
Ø	Ø	A	C
1	Ø	B	D
Ø	1	C	A
1	1	D	B



Area B jumpers determine whether the UART--control port pair, i.e. ports C and D, will be the upper or the lower two addresses on the card.

Figure 3-1

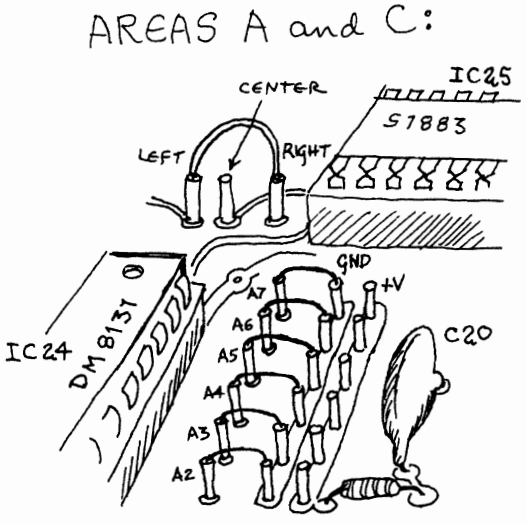
The group of addresses is selected by six jumpers in Area A (See Figure 3-2.) as follows:

ADDRESS RANGE Decimal	ADDRESS RANGE Octal	ADDRESS BITS A7	A6	A5	A4	A3	A2
0 - 3	0 - 3	G	G	G	G	G	G
4 - 7	4 - 7	G	G	G	G	G	V
8 - 11	10 - 13	G	G	G	G	V	G
12 - 15	14 - 17	G	G	G	G	V	V
16 - 19	20 - 23	G	G	G	V	G	G
20 - 23	24 - 27	G	G	G	V	G	V
24 - 27	30 - 33	G	G	G	V	V	G
28 - 31	34 - 37	G	G	G	V	V	V
32 - 35	40 - 43	G	G	V	G	G	G
36 - 39	44 - 47	G	G	V	G	G	V

ADDRESS RANGE		ADDRESS BITS					
Decimal	Octal	A7	A6	A5	A4	A3	A2
40 - 43	50 - 53	G	G	V	G	V	G
44 - 47	54 - 57	G	G	V	G	V	V
48 - 51	60 - 63	G	G	V	V	G	G
52 - 55	64 - 67	G	G	V	V	G	V
56 - 59	70 - 73	G	G	V	V	V	G
60 - 63	74 - 77	G	G	V	V	V	V
64 - 67	100 - 103	G	V	G	G	G	G
68 - 71	104 - 107	G	V	G	G	G	V
72 - 75	110 - 113	G	V	G	G	V	G
76 - 79	114 - 117	G	V	G	G	V	V
80 - 83	120 - 123	G	V	G	V	G	G
84 - 87	124 - 127	G	V	G	V	G	V
88 - 91	130 - 133	G	V	G	V	V	G
92 - 95	134 - 137	G	V	G	V	V	V
96 - 99	140 - 143	G	V	V	G	G	G
100 - 103	144 - 147	G	V	V	G	G	V
104 - 107	150 - 153	G	V	V	G	V	G
108 - 111	154 - 157	G	V	V	G	V	V
112 - 115	160 - 163	G	V	V	V	G	G
116 - 119	164 - 167	G	V	V	V	G	V
120 - 123	170 - 173	G	V	V	V	V	G
124 - 127	174 - 177	G	V	V	V	V	V
128 - 131	200 - 203	V	G	G	G	G	G
132 - 135	204 - 207	V	G	G	G	G	V
136 - 139	210 - 213	V	G	G	G	V	G
140 - 143	214 - 217	V	G	G	G	V	V
144 - 147	220 - 223	V	G	G	V	G	G
148 - 151	224 - 227	V	G	G	V	G	V
152 - 155	230 - 233	V	G	G	V	V	G
156 - 159	234 - 237	V	G	G	V	V	V
160 - 163	240 - 243	V	G	V	G	G	G
164 - 167	244 - 247	V	G	V	G	G	V
168 - 171	250 - 253	V	G	V	G	V	G
172 - 175	254 - 257	V	G	V	G	V	V
176 - 179	260 - 263	V	G	V	V	G	G
180 - 183	264 - 267	V	G	V	V	G	V
184 - 187	270 - 273	V	G	V	V	V	G
188 - 191	274 - 277	V	G	V	V	V	V
192 - 195	300 - 303	V	V	G	G	G	G
196 - 199	304 - 307	V	V	G	G	G	V
200 - 203	310 - 313	V	V	G	G	V	G
204 - 207	314 - 317	V	V	G	G	V	V
208 - 211	320 - 323	V	V	G	V	G	G
212 - 215	324 - 327	V	V	G	V	G	V
216 - 219	330 - 333	V	V	G	V	V	G
220 - 223	334 - 337	V	V	G	V	V	V
224 - 227	340 - 343	V	V	V	G	G	G
228 - 231	344 - 347	V	V	V	G	G	V

ADDRESS RANGE		ADDRESS BITS					
Decimal	Octal	A7	A6	A5	A4	A3	A2
232 - 235	350 - 353	V	V	V	G	V	G
236 - 239	354 - 357	V	V	V	G	V	V
240 - 243	360 - 363	V	V	V	V	G	G
244 - 247	364 - 367	V	V	V	V	G	V
248 - 251	370 - 373	V	V	V	V	V	G
252 - 255	374 - 377	reserved for front panel switches					

Area C jumpers connect the UART control strobe input to either the Control Output Port strobe (for software control of the UART serial port conditions; e.g. word length selection, parity selection and number of bits per data word), or to +5V (for hardwired selection of a single UART operating mode).



Area A jumpers select which one of the possible 64 address segments the 3P+S module will occupy.

Figure 3-2

Six DIP-type carriers of solder - in receptacles - are provided. These may be installed where frequent changes of jumpers may be necessary. They will accept and hold 24 gauge wire (solid) in a pressure fit. It is suggested that these receptacles be installed in all of the holes in Area A.

To select the desired address, connect jumper wires from the holes or receptacles in the lefthand column of Area A to the proper V (righthand) or G (center) holes or receptacles. Solder if no receptacles are used.

3.1.2 Channel C Input

Channel C is intended for use as the "status" or "control" channel for the other channels. In the "input" direction data enters that channel through terminals CØ through C7 in Area G. (See component location diagram in Section V.) Data may be jumpered to these terminals in any combination from the following sources: (Control bit selection, however, is normally dictated by the program. That is, the source-terminal relationship cannot always be random.)

UART Flags

PE (parity error)
FE (framing error)
OE (overrun error)
RDA (receiver data available)
TBE (transmitter buffer empty)

Channel Flags

FA (latch set by XDAA; external data available Channel A)
FB (latch set by XDAB; external data available Channel B)
XA (input from external latch XDRA;
external data received Channel A)
XB (input from external latch XDRB;
external data received Channel B)

EIA Inputs A, B, C, D

When an EIA device such as a modem is used, serial data will enter on one EIA channel and status data, such as carrier detect, will be received on other EIA channels. The 3P+S has provision for receiving up to four EIA channels which should not be confused with the data channels A through D used in the 3P+S.

The sources listed above may be used to set up the "status word", each bit of which is an independent indicator of the status of various channels and sections in the 3P+S. Where interrupt is not used, this word is continuously tested by the computer to detect any changes such as a new word received. With interrupt, examination of the status word by the computer is carried out only after notification of the CPU by the interrupt system.

3.1.3 Channel C Output

Data output on Channel C goes to two places: bits 4 through 7 are brought to terminals in Area H (See Figure 3-3.) from which they may be jumpered to status inputs of the UART. Bits Ø through 3 are strobed into latch IC 6 and are made available at terminals in Area E, see Figure 3-4, (baud rate), Area F (peripheral control driver), and Area J (EIA outputs). The destinations of the various bits are as follows:

Area H jumpers connect the UART condition inputs to Control Output port C, bits 4 through 7. Normal 110 Baud TTY operation (with the ASR33) requires that none of these jumpers be connected (if the Control Strobe input is jumpered to +5V) or that all five condition inputs be initialized via a software routine (to a high state) if the UART serial I/O is to be software controlled for more than one Baud rate and/or set of operating conditions.

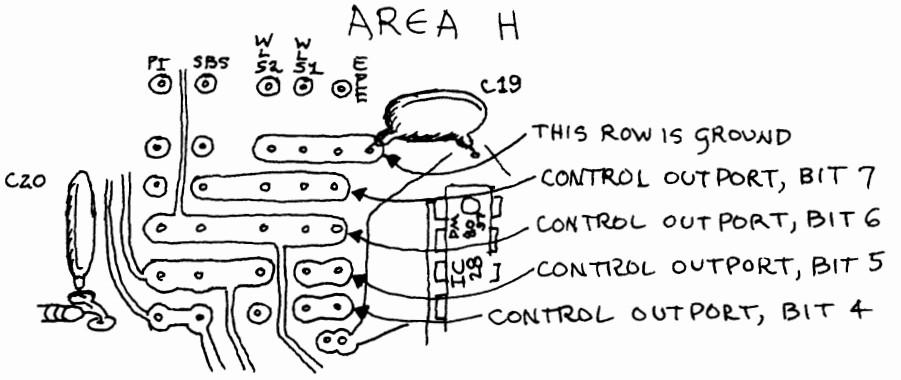


Figure 3-3

Area E jumpers select the Baud rate for the serial I/O (i.e. the UART, port D).

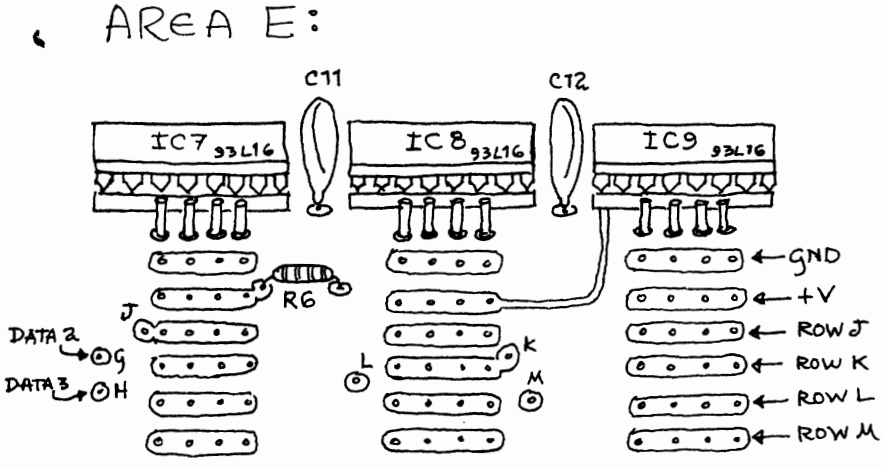


Figure 3-4

Bit Ø: row 2 of Area J, lefthand terminal of Area F
Bit 1: row 4 of Area J, righthand terminal of Area F
Bit 2: terminal G of Area E
Bit 3: terminal H of Area E, row 3 of Area J
Bit 4: bottom row, Area H
Bit 5: 5th row, Area H
Bit 6: 4th row, Area H
Bit 7: 3rd row, Area H

The status inputs to the UART are brought out to the top row of terminals in Area H and consist of the following: (all high active)

Lefthand : Parity Inhibit (PI). Inhibits transmission of the parity bit (after data bits) and disables parity error detection circuitry in the receiver.

2nd from Left: Stop Bit Select (SBS). Selects one stop bit if inactive (low). Selects two stop bits if active (unless five bit word length is selected, in which case 1.5 stop bits are selected).

4th from Left: Word Length Select 1 (WLS1).
3rd from Left: Word Length Select 2 (WLS2). Select the number bits per character:

WLS1	WLS2	Bits Per Character
H	H	8
L	H	7
H	L	6
L	L	5

(Note that these word lengths do not include the parity bit if it is enabled.)

Righthand: Even Parity Enable (EPE). If parity is not inhibited, selects polarity of parity bit. "High" selects even parity (even number of bits per character).

NOTE

If you enable the parity bit, you should generally reduce the word length by one bit to keep the total number of bits in the word the same as the selected word length.

These status inputs may be tied "low" by being connected to the second row from the top in Area H (ground), and may be held "high" by being left unconnected. (Standard Teletype setup has all status inputs "high".)

Loading of new information into the status registers of the UART is performed by CRL, Control Register Load, pin 34 of the UART, which is brought out to the righthand terminal of Area C. If this is jumpered to the lefthand terminal it will go active whenever information is output to Channel C.

If the status information is "hard wired" (not variable by the computer), CRL should be jumpered to the center terminal of Area C (See Figure 3-2), where it will be held "high".

It is obvious that if CRL is connected to the Channel C strobe, then each time new data is sent out on the low-order bits of Channel C the same "old data" must be present on the high - order bits of that word. Otherwise new status information will be written into the Control Registers of the UART each time.

The Peripheral Control Driver provides a means for driving high-current loads such as lamps and relays. Bit Ø or bit 1 are selected as an input to this driver by the connection of R10 (2.2 kohm, red-red-red) as shown in the component location diagram. The lower lead is connected either to the righthand terminal (bit 1) or the lefthand terminal (bit Ø) in Area F.

Four EIA-level outputs are available for the output of data selected in Area J. When an EIA device (such as a modem) is connected, serial data is ordinarily transmitted by one output. The others may be used for the transmission of steady-state status or control signals such as "request to send".

In Area J the topmost row of terminals are the four EIA outputs.
The next row down is data bit Ø.
The third row from the top is data bit 3.
The fourth row from the top is data bit 1.
The fifth and bottom row is serial data from the UART.

(Note that bit 2 is not available for use at Area J.)

The Programmable Baud Rate Generator (IC 7, IC 8, IC 9) may be connected to yield almost any baud rate imaginable. It consists of a variable-modulo counter that divides the 2.0 Mhz clock, Ø2. The modulus of the counter is varied by changing the preset value which is loaded into the counter at each "overflow". This value consists of a twelve-bit binary number which is grouped into three words of four bits each.

Baud Rate	Modulus	Preset	Binary (LSB)		(MSB)
35	3571	514	0100	0000	0100
45.55	2744	1341	1011	1100	1010
50	2500	1585	1000	1100	0110

Baud Rate	Modulus	Preset	Binary (LSB)		(MSB)
56.85	2198	1886	0111	1010	1110
61.12	2045	2040	0001	1111	1110
66.67	1874	2210	0100	0101	0001
74.23	1684	2401	1000	0110	1001
75	1667	2418	0100	1110	1001
110	1136	2949	1010	0001	1101
134.46	929	3155	1100	1010	0011
150	833	3252	0010	1101	0011
300	417	3668	0010	1010	0111
600	208	3877	1010	0100	1111
1200	104	3981	1011	0001	1111
2400	52	4033	1000	0011	1111
3600	35	4050	0100	1011	1111
4800	26	4059	1101	1011	1111
9600	13	4072	0001	0111	1111

(Note that the output of the divider is sixteen times the desired baud rate. This is a requirement of the UART.)

If the baud rate does not have to be changed by the computer, the binary number corresponding to the desired baud rate may be set up at the inputs to the counters. "1" is set up by connecting an input to +V (third row from the top), and "Ø" is set up by connection to Ground (second row from top). The order of the inputs is the same from left to right as the binary bits in the preceding baud rate table.

If the baud rate is to be selectable between any two rates by the computer, the following procedure should be used:

1. Select the two baud rates and write the binary numbers one under the other so that the columns line up.

2. For those columns having "Ø" in both numbers, jumper the corresponding inputs to Ground (second row from top).

3. For those columns having "1" in both numbers, jumper the corresponding inputs to +V (third row from top).

4. For those columns having a "1" in the top row and a "Ø" in the bottom row, jumper the corresponding inputs to an unused row in Area E, for example, the fourth row from the top.

5. For those columns having a "Ø" in the top number and a "1" in the bottom number, jumper the corresponding inputs to another unused row in Area E, for example, the fifth from the top.

6. Jumper terminal "G" in Area E to terminal "J". Jumper terminal "H" to terminal "K".

7. Software may be written so that in the word sent out on Channel C the following relationship applies between bits 2 and 3 and the two desired baud rates (top and bottom numbers):

Bit 2	Bit 3	Baud Rate
Ø	1	bottom number
1	Ø	top number

NOTE

Only two baud rates may be selected with this technique. Using some additional parts, it is possible to expand the number of baud rates. Those who wish to do this should contact the factory for an engineering bulletin describing these techniques.

3.1.4 Channel D Input

Channel D handles data to and from the UART. In the input direction, data may be taken in from any of the four EIA channels or the current loop receiver. The data is jumpered to the "R IN" terminal in Area G.

If an EIA input is used, jumper from the desired "A", "B", "C", or "D" terminal in Area G to the R IN terminal.

If the current loop receiver is used, jumper the terminal to the right of the collector lead of transistor Q5 to the terminal just to the right of Q4.

3.1.5 Channel D Output

Any of the four EIA transmitters may be driven by serial data from the UART. The desired terminal on the top row of Area J may be jumpered to the bottom row of Area J. The latter carries the serial output of the UART.

If the current loop transmitter is not used, the center terminal in Area D should be jumpered to the righthand terminal in Area D. (See Figure 3-5.) This will ensure that the current loop output is "floating".

If the current loop transmitter is used, the center terminal in Area D should be jumpered to the lefthand terminal in that area.

Area D jumpers enable or disable the TTY current loop output.

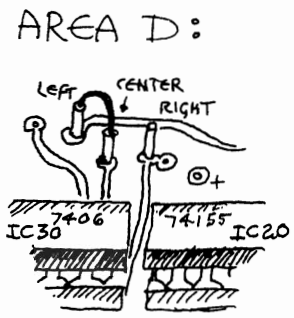


Figure 3-5

The current receiver of the external device should be connected between pins 15 and S of J1. Pin 15 is the more positive of the two.

3.1.6 Channel A and B Flags

Two flip-flops (IC 15) are provided to latch external signals denoting available data. The inputs to these flip-flops, XDAA and XDAB, are active low. 2.2 kohm pullup resistors are provided (R19, R20) in case the external device has no pullup. They should be returned to the +5 volt source on the board, not an external power supply. This is done by jumpering pins 4 and/or D of J2 to pins W and/or 19 of J1.

When either latch is set a high-active acknowledge signal AKA or AKB is presented at J2 pin 13 or P. The flag remains set until an input is carried out from that channel.

Data must be held stable at the Channel A or B inputs from the time the flag is set until the time it is cleared. <u>This requires an external data latch</u>. AKA or AKB may be used as a high-active clock for such a latch.

SECTION IV

PERIPHERAL INTERFACING

3P+S INPUT/OUTPUT MODULE

4.1 PERIPHERAL INTERFACING

4.1.1 Input/Output Interfacing

All input/output interfacing between the 3P+S and peripheral is done with J1 (3P+S outputs) and J2 (inputs to 3P+S). Pin connections for J1 and J2 are defined in Figure 4-1.

4.1.2 EIA RS-232-C

EIA Standard RS-232-C, "Interface Between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange," ensures equipment compatability and interchangeability between different manufacturers by defining the electrical and mechanical interface between a modem and data terminal. Specifically, RS-232-C sets the voltage levels that can be present at the interface. It also establishes the handshaking routine and timing.

The RS-232-C standard signal levels are as follows:

DATA	BINARY	CONTROL	VOLTAGE LEVEL
Mark	1	Off	-3 to -25v
Space	0	On	+3 to +25v

A load between 3000 and 7000 ohms must be presented to these signals. With this loading, the voltage levels will be between ± 5 and ± 15 volts, the minimum and maximum voltages set by RS-232-C.

A standard 25-pin "dataphone" interface connector is used. EIA RS-232-C pin number assignments are as follows:

PIN NO.	CIRCUIT	SIGNAL NAME	DESCRIPTION
1	AA	Protective Ground	Chassis
2	BA	Transmitted Data	Data flow from terminal to modem
3	BB	Received Data	Data flow from modem to terminal
4	CA	Request to Send	Control signal from terminal asking for permission to send data
5	CB	Clear to Send	Control signal sent to terminal indicating transmission can begin.
6	CC	Data Set Ready	Control signal sent to terminal indicating data equipment is operational

PIN NO.	CIRCUIT	SIGNAL NAME	DESCRIPTION
7	AB	Signal Ground (Common Return)	Ground line for all signals
8	CF	Received Line Signal Detector	Control signal sent to terminal indicating transmission path for received data is established
9-25		Additional signals, primarily used in high-speed synchronous data transmission.	

The preceding pin assignment-signal relationships reflect a terminal-modem connection. The 3P+S may either replace a terminal (when connected to a modem) or communicate with a terminal. In these two cases, the signals clearly have different functions with respect to the 3P+S and processor.

To configure the 3P+S for an RS-232-C interface, proceed as follows:

1. Connect UART transmitter output to EIA 4 OUT driver by placing a jumper between 4 and Row 5 in Area J.

2. Connect Channel C bit Ø (request to send) to EIA 3 OUT driver by placing a jumper between 3 and Row 2 in Area J.

3. Connect EIA 1 IN (received data) to UART receiver input by placing a jumper between 1 and R IN in Area G.

4. Connect EIA 2 IN (carrier detect) to DIØ (Data In Bus) by placing a jumper between 2 and CØ in Area G.

5. Make the following input-output connections between the 3P+S and EIA connector.

3P+S CONNECTOR/PIN	EIA CONNECTOR PIN
J2-K	3
J2-L	8
J1-11	7
J1-R	2
J1-P	4

All connections and jumpers required for an RS-232-C interface are shown in Figure 4-2.

4.1.3 Teletype, Models ASR33 or KSR33

The Teletype (TTY) is probably the most common data terminal around. It is a current loop device, originally intended to send and receive data over a single loop of wire. A normally closed

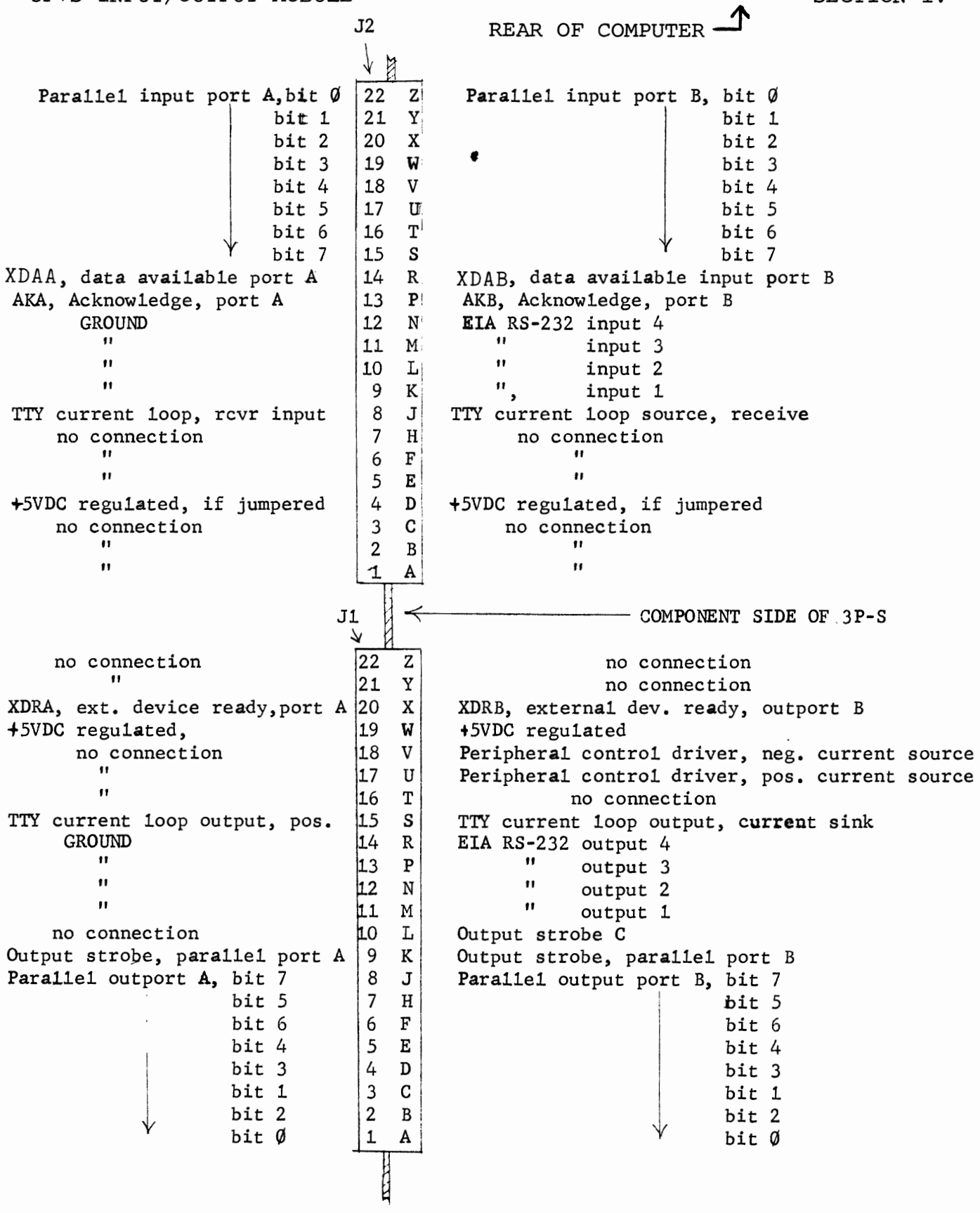


Figure 4-1. J1 and J2 Pin Connections.

sending switch maintains current flow when the TTY is sending. Current flow represents a "1". With this switch open, no current flows to denote a "0". When a character is sent from the TTY, the sending switch opens and closes in a sequence specific to that character.

On the receiving side of the TTY is a selector magnet, an electromagnet normally held in the energized state by the current flow. When the magnet is de-energized (no current flow), it places the printing mechanism into operation.

To configure the 3P+S for the simplest ASR33 or KSR33 Teletype interface, proceed as follows:

1. Assign address Ø to the 3P+S by placing jumpers between A2 through A7 and the ground bus in Area A.

2. Place a jumper between left (L) and right (R) in Area B.

3. Hard wire enable the control inputs to the UART by placing a jumper between center (C) and right (R) in Area C.

4. Enable the teletype current loop connection by placing a jumper between left (L) and center (C) in Area D.

5. Program the Baud Rate Generator (IC 7 through 9) for 110 baud as follows:

   Jumper pins 3 and 5 of IC 7, pin 6 of IC 8, and pins 3, 4, 6 of IC 9 to the +V bus (the row immediately below the GND bus) in Area E.

   Jumper pins 4 and 6 of IC 7, pins 3, 4, 5 of IC 8, and pin 5 of IC 9 to the GND bus (top row) in Area E.

6. Connect RDA (receiver data available) and TBE (transmitter buffer empty) to two of the CØ through C7 control bits in Area G. (Note that control bit selection normally depends on the program. It cannot always be random.)

7. Connect the current loop input to the UART RCV IN input by placing a jumper between the terminal to the immediate right of transistor Q4 and the terminal to the immediate right of Q5. (Q4 and Q5 are located to the left of Area G.)

8. UNPLUG THE TELETYPE and remove the cover. Locate the barrier strip to which the TTY power cord is connected. This is a black barrier strip on the back at the lower left (as viewed from the rear of the TTY). It is behind a panel of square white plastic connectors to which many

wires connect. The barrier strip may be hidden by a grey fiber insulating strip. There are nine screw terminals on the barrier strip, numbered 1 to 9 from left to right. Make connections between this strip and the 3P+S as follows:

3P+S CONNECTOR/PIN	TTY BARRIER STRIP PIN
J1-15	7
J1-S	6
J2-8	4
J2-J	3

All connections and jumpers required for an ASR33 or KSR33 Teletype interface are shown in Figure 4-3.

4.1.4 Teleprinter, Model 15

Instructions for interfacing the Model 15 Teleprinter are based on the following assumptions:

- Only the minimal printer-keyboard mechanism is used. (In many cases additional teleprinter circuitry may be present to perform some of the functions of the circuitry to be subsequently described.)
- The selector magnet coil will be driven without the use of the power supply in the teleprinter.

To configure the 3P+S for a Model 15 Teleprinter interface, proceed as follows:

1. Connect the jumpers in Areas A, B, C, D, E, and G as described in Steps 1 through 6 of the ASR33/KSR33 Teletype instructions.
2. Connect the current loop input to the UART RCV IN input as described in Step 7 of the ASR33/KSR33 Teletype instructions.
3. Make the following input/output connections between the 3P+S and Model 15.

   Disconnect brown wire from the keyboard terminal block (second terminal from front of block) located on the right side (as viewed from the front) of the Model 15. (See Figure 4-4.) Connect the wire to J2-J on the 3P+S.

   Disconnect yellow wire (fourth terminal from front of block) from keyboard terminal block. (See Figure 4-4.) Connect wire to J2-8 on the 3P+S.

Connect J1-S and 15 to reed relay circuit shown in Figure 4-5.

Connect one contact of reed relay (See Figure 4-5) to the output of the 12-volt unregulated supply shown in Figure 4-6.

The Model 15 selector magnet coil is connected to a terminal block located on the left side rear (as viewed from the front) of the teleprinter. Both coil leads are yellow and connected to the outside terminals on the block. (See Figure 4-4.) The coil is not sensitive to polarity.

Connect power supply ground to one of the magnet coil terminals on the block. Connect the other relay contact to the other magnet coil terminal.

CAUTION

ONLY USE THE REED RELAY TECHNIQUE TO DRIVE THE SELECTOR MAGNET COIL. SIMPLE SOLID-STATE CIRCUITRY AND "DAMPER DIODE" TECHNIQUES WILL NOT WORK.

All connections and jumpers required for a Model 15 Teleprinter interface are shown in Figure 4-7.

4.1.5 Teleprinter, Model 28

The interface instructions for the Model 28 Teleprinter are based on the same assumptions outlined for the Model 15.

To configure the 3P+S for a Model 28 Teleprinter, proceed as follows:

1. Perform Steps 1 and 2 of Model 15 instructions.

2. Make the following input/output connections between the 3P+S and Model 28:

   Connect pins Ø and 2 on the Model 28 keyboard (refer to Figure 4-8) connection plug (upper left side as viewed from front) to J2-J and 8 respectively on the 3P+S.

   Connect J1-S and 15 to the selector magnet coils as described in Step 3 of the Model 15 instructions.

All connections and jumpers required for a Model 28 Teleprinter interface are shown in Figure 4-9. (See NOTE and CAUTION on Page IV-12.)

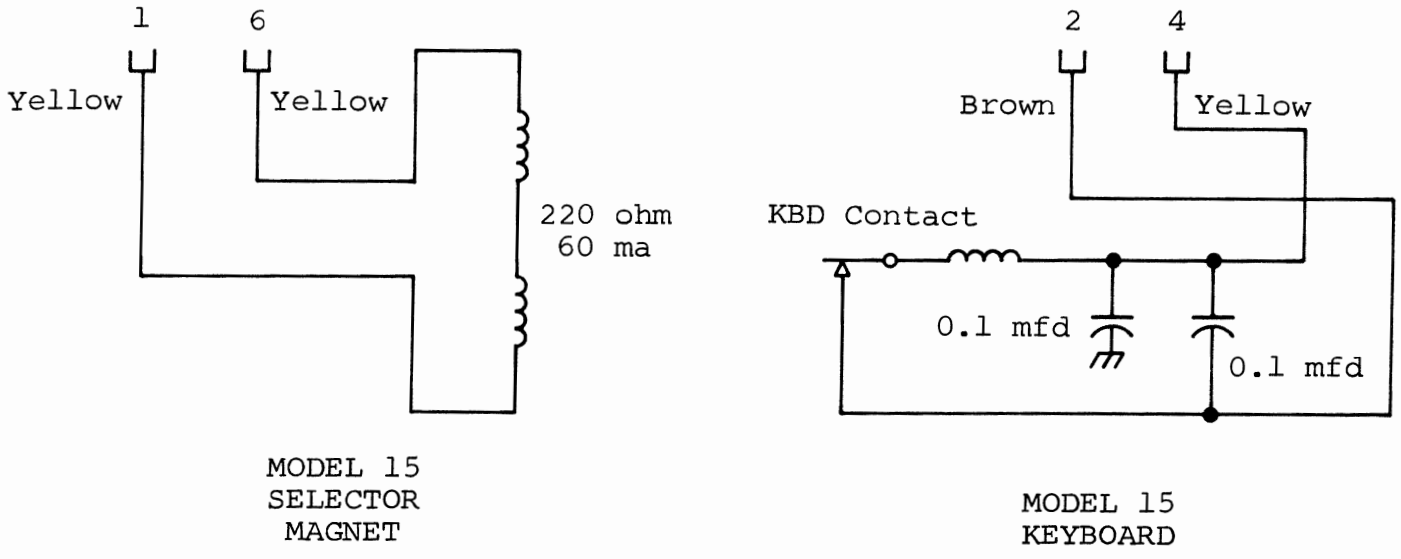


Figure 4-4. Model 15 magnet and keyboard connections.

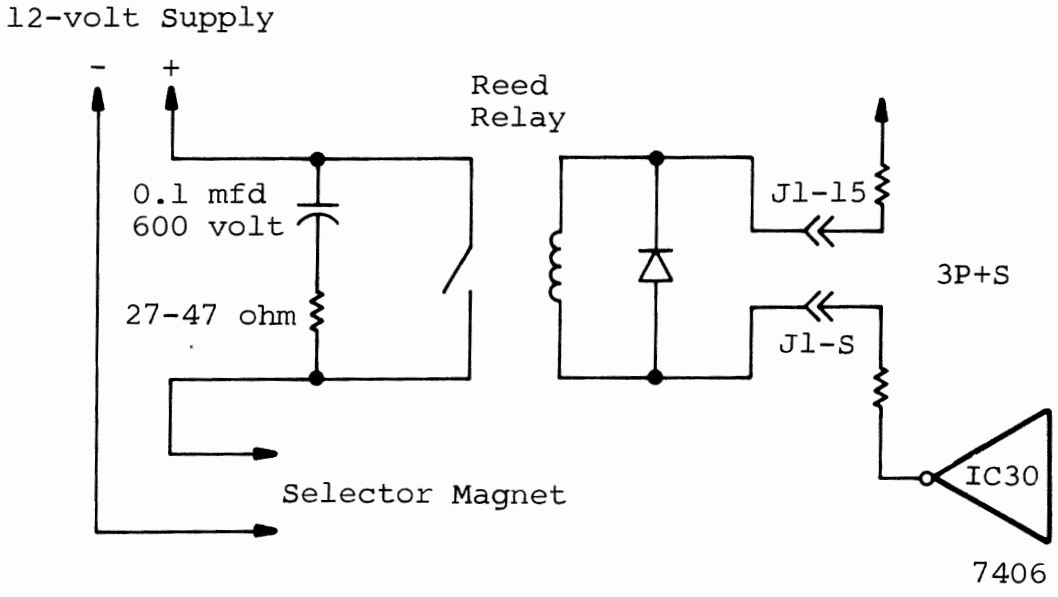


Figure 4-5. Reed relay circuit.

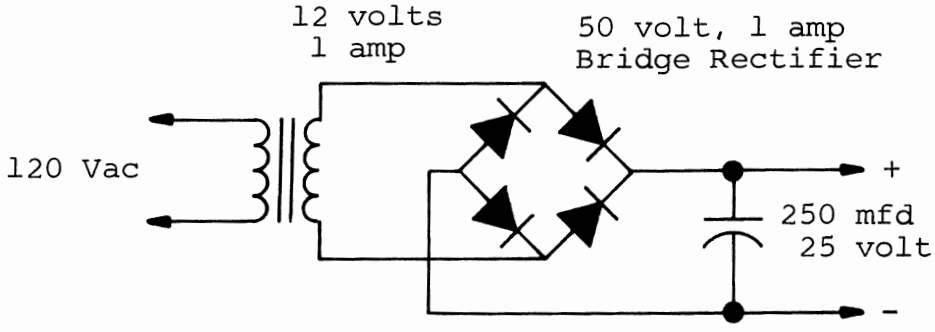


Figure 4-6. 12-volt unregulated power supply circuit.

NOTE

The selector magnet in the Model 28 has two coils. (See Figure 4-8.) These can be parallel connected for 12 volt operation or series connected for 24 volt operation. Since the magnetic fields can add or subtract, take care when connecting the two coils. The coils are connected to a terminal block located on the righthand side (as viewed from the front). For parallel operation, connect pin 1 to pin 0 and pin 3 to pin 4 on this block. For series operation, connect pin 0 to pin 1 and external circuitry to pins 3 and 4. In both cases, polarity is not critical once the connections are made.

CAUTION

ONLY USE THE REED RELAY TECHNIQUE TO DRIVE THE SELECTOR MAGNET COIL. SIMPLE SOLID-STATE CIRCUITRY AND "DAMPER DIODE" TECHNIQUES WILL NOT WORK.

4.1.6 CT1024 TV Typewriter II

The 3P+S can directly interface to the parallel inputs of the TV Typewriter II as well as the keyboard. The TV Typewriter (TVT), however, must be slightly modified to make the signal on pin 6 of IC 9 in the TVT available to the 3P+S.

Make this modification by connecting a wire between pin 6 of IC 9 and pin R of J2 on the 3P+S. This assumes Channel B in the 3P+S is used. (If J9, normally the keyboard input plug on the TVT, is used to connect the TVT and 3P+S, connect pin 6 of IC 9 to pin 9 of J9. Then connect pin 9 of J9 to J2-R on the 3P+S.) Once modified, pin 6 of IC 9 drives the XDAB input to IC 15 in the 3P+S.

Also, connect the jumper at IC 32 in the TVT from pin 1 to pin 3 of IC 32. This causes data to be strobed on the trailing edge of the strobe pulse.

After modifying the TVT, proceed as follows to configure the 3P+S for a TVT II interface:

1. Place a jumper between left (L) and right (R) in Area B.

2. Place a jumper between XB and C1 in Area G.

3. Place a jumper between FB and C5 in Area G.

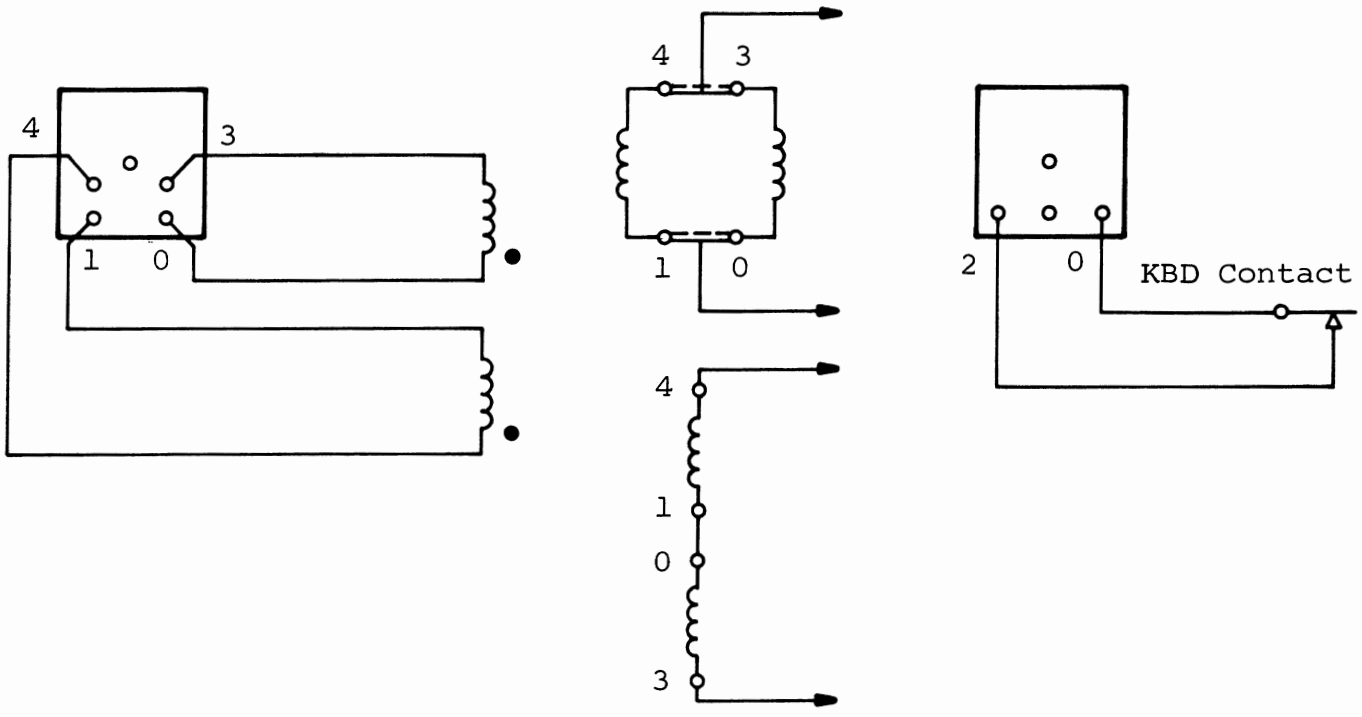


Figure 4-8. Model 28 magnet and keyboard connections.

4. Make the following connections between the 3P+S and TVT II. (Assumes Channel B in 3P+S is used.)

3P+S CONNECTOR/PIN	TVT II CONNECTOR/PIN
J1-A	J9-1
J1-C	J9-4
J1-B	J9-5
J1-D	J9-7
J1-E	J9-8
J1-H	J9-12
J1-F	J9-11
J1-K	J9-10 (strobe)
J1-11	J9-3 (ground)

All connections and jumpers required for a TVT II interface are shown in Figure 4-10.

You may be faced with two problems with this interface. One concerns the strobe pulse and keyboard data stability; the other concerns software.

XDAB is used as a flag for keyboard input to the 3P+S. The signal must be negative-going and 1 to 10 microseconds in duration. To ensure a proper XDAB signal, use of the strobe latch circuit in Figure 4-11 is recommended. If the data from the keyboard is not stable for several microseconds after XDAB, a data latch (see Figure 4-11) must also be used.

The second problem arises when serial software (e.g., 8K basic or SW1F) is used since the TVT II is a parallel device. To solve the problem, you have two alternatives: change the software or modify the hardware.

With the latter alternative, the address ports must be changed. This change is accomplished by switching the THRL input to the UART from pin 7 of IC 20 to pin 5 of IC 20, the STROBE B output from pin 5 of IC 20 to pin 7 of IC 20, the DRR input to the UART from pin 9 of IC 20 to pin 11 of IC 20, and the S input (pin 11) of IC 15 from pin 11 of IC 20 to pin 9 of IC 20.

A demonstration program to write characters onto the TVT II follows:

ADDRESS	OCTAL DATA	MNEMONIC
0	076	MVI A
1	377	
2	323	OUT
3	000	
4	076	MVI A
5	300	
6	041	LX
7	377	
10	020	
11	323	OUT
12	001	
13	055	DCR L
14	302	JNZ
15	013	
16	000	

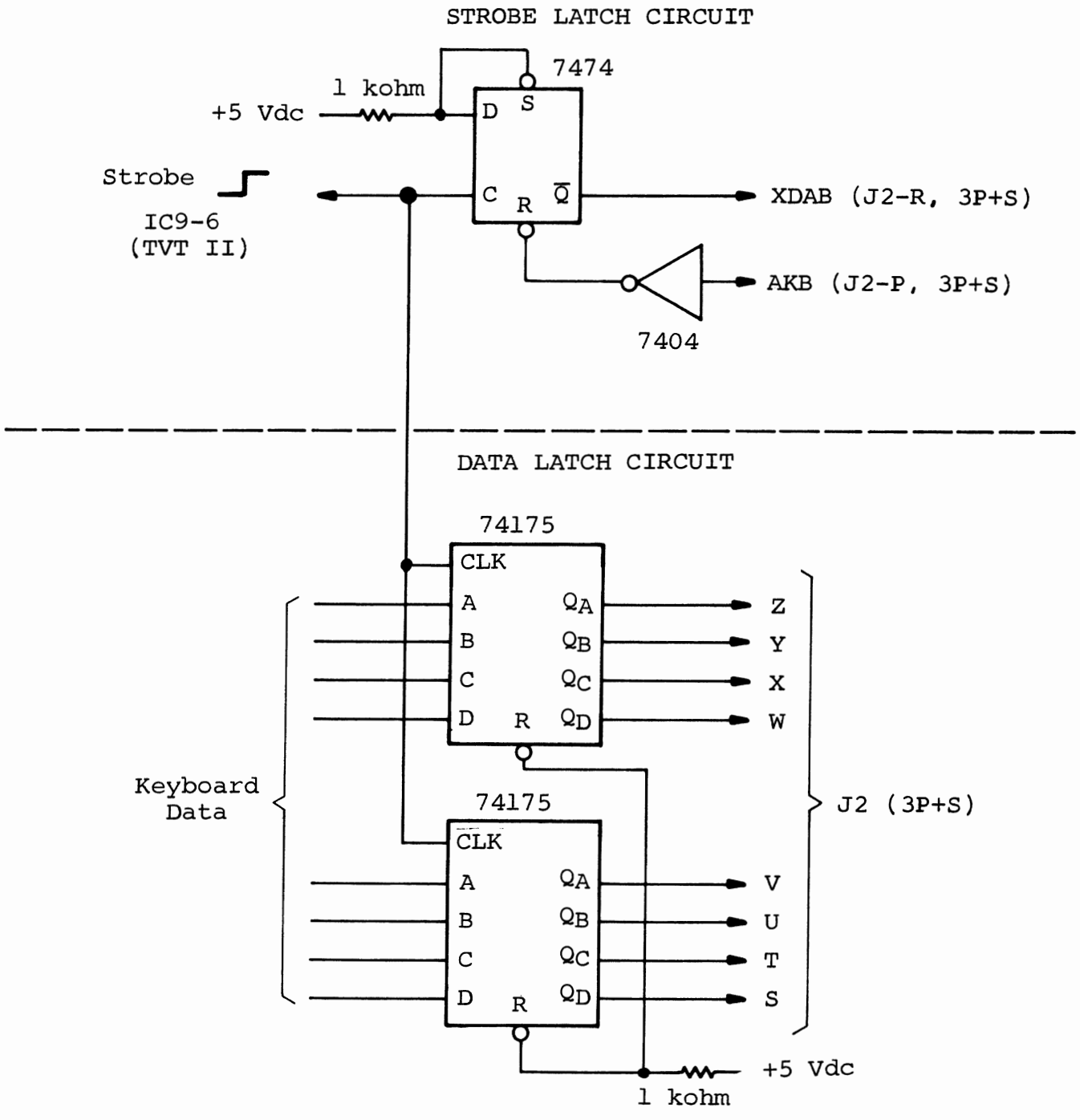


Figure 4-11. External strobe and data latch circuits.

SECTION V

DRAWINGS

3P+S INPUT/OUTPUT MODULE

PROCESSOR TECHNOLOGY CORPORATION

APPENDICES

3P+S INPUT/OUTPUT MODULE

STATEMENT of WARRANTY

PROCESSOR TECHNOLOGY COMPANY, in recognition of its responsibility to provide quality components and adequate instruction for their proper assembly, warrants its products as follows:

All components sold by Processor Technology Company are purchased through normal factory distribution and any part which fails because of defects in workmanship or material will be replaced at no charge for a period of 6 months following the date of purchase. The defective part must be returned postpaid to Processor Technology Company within the warranty period.

Any malfunctioning module, purchased as a kit and returned to Processor Technology within the warranty period, which in the judgement of P.T. Co. has been assembled with care and not subjected to electrical or mechanical abuse, will be restored to proper operating condition and returned, regardless of cause of malfunction, with a minimal charge to cover postage and handling.

Any modules purchased as a kit and returned to P.T. Co. which in the judgement of P.T. Co. are not covered by the above conditions will be repaired and returned at a cost commensurate with the work required. In no case will this charge exceed $20.00 without prior notification and approval of the owner.

Any modules, purchased as assembled units are guaranteed to meet specifications in effect at the time of manufacture for a period of at least 6 months following purchase. These modules are additionally guaranteed against defects in materials or workmanship for the same 6 month period. All warranted factory assembled units returned to P.T. Co. postpaid will be repaired and returned without charge.

This warranty is made in lieu of all other warranties expressed or implied and is limited in any case to the repair or replacement of the module involved.

JUMP

C3	JMP	Adr
C2	JNZ	
CA	JZ	
D2	JNC	
DA	JC	
E2	JPO	
EA	JPE	
F2	JP	
FA	JM	
E9	PCHL	

CALL

CD	CALL	Adr
C4	CNZ	
CC	CZ	
D4	CNC	
DC	CC	
E4	CPO	
EC	CPE	
F4	CP	
FC	CM	

RETURN

C9	RET
C0	RNZ
C8	RZ
D0	RNC
D8	RC
E0	RPO
E8	RPE
F0	RP
F8	RM

RESTART

C7	RST	0
CF	RST	1
D7	RST	2
DF	RST	3
E7	RST	4
EF	RST	5
F7	RST	6
FF	RST	7

ROTATE†

07	RLC
0F	RRC
17	RAL
1F	RAR

CONTROL

00	NOP
76	HLT
F3	DI
FB	EI

MOVE (cont)

58	MOV	E,B
59	MOV	E,C
5A	MOV	E,D
5B	MOV	E,E
5C	MOV	E,H
5D	MOV	E,L
5E	MOV	E,M
5F	MOV	E,A
60	MOV	H,B
61	MOV	H,C
62	MOV	H,D
63	MOV	H,E
64	MOV	H,H
65	MOV	H,L
66	MOV	H,M
67	MOV	H,A
68	MOV	L,B
69	MOV	L,C
6A	MOV	L,D
6B	MOV	L,E
6C	MOV	L,H
6D	MOV	L,L
6E	MOV	L,M
6F	MOV	L,A
70	MOV	M,B
71	MOV	M,C
72	MOV	M,D
73	MOV	M,E
74	MOV	M,H
75	MOV	M,L
77	MOV	M,A

ACCUMULATOR*

80	ADD	B
81	ADD	C
82	ADD	D
83	ADD	E
84	ADD	H
85	ADD	L
86	ADD	M
87	ADD	A
88	ADC	B
89	ADC	C
8A	ADC	D
8B	ADC	E
8C	ADC	H
8D	ADC	L
8E	ADC	M
8F	ADC	A
90	SUB	B
91	SUB	C
92	SUB	D
93	SUB	E
94	SUB	H
95	SUB	L
96	SUB	M
97	SUB	A
98	SBB	B
99	SBB	C
9A	SBB	D
9B	SBB	E
9C	SBB	H
9D	SBB	L
9E	SBB	M
9F	SBB	A
A0	ANA	B
A1	ANA	C
A2	ANA	D
A3	ANA	E
A4	ANA	H
A5	ANA	L
A6	ANA	M
A7	ANA	A
A8	XRA	B
A9	XRA	C
AA	XRA	D
AB	XRA	E
AC	XRA	H
AD	XRA	L
AE	XRA	M
AF	XRA	A
B0	ORA	B
B1	ORA	C
B2	ORA	D
B3	ORA	E
B4	ORA	H
B5	ORA	L
B6	ORA	M
B7	ORA	A
B8	CMP	B
B9	CMP	C
BA	CMP	D
BB	CMP	E
BC	CMP	H
BD	CMP	L
BE	CMP	M
BF	CMP	A

CONSTANT DEFINITION

0BDH, 1AH	Hex
105D, 105	Decimal
72O, 72Q	Octal
11011B, 00110B	Binary
'TEST', 'A', 'B'	ASCII

OPERATORS

+ −

MOVE IMMEDIATE

06	MVI	B, D8
0E	MVI	C, D8
16	MVI	D, D8
1E	MVI	E, D8
26	MVI	H, D8
2E	MVI	L, D8
36	MVI	M, D8
3E	MVI	A, D8

Acc IMMEDIATE*

C6	ADI	D8
CE	ACI	D8
D6	SUI	D8
DE	SBI	D8
E6	ANI	D8
EE	XRI	D8
F6	ORI	D8
FE	CPI	D8

LOAD IMMEDIATE

01	LXI	B, D16
11	LXI	D, D16
21	LXI	H, D16
31	LXI	SP, D16

STACK OPS

C5	PUSH	B
D5	PUSH	D
E5	PUSH	H
F5	PUSH	PSW
C1	POP	B
D1	POP	D
E1	POP	H
F1	POP	PSW*
E3	XTHL	
F9	SPHL	

DOUBLE ADD†

09	DAD	B
19	DAD	D
29	DAD	H
39	DAD	SP

SPECIALS

EB	XCHG	
27	DAA*	
2F	CMA	
37	STC†	
3F	CMC†	

INPUT/OUTPUT

D3	OUT	D8
DB	IN	D8

MOVE

40	MOV	B,B
41	MOV	B,C
42	MOV	B,D
43	MOV	B,E
44	MOV	B,H
45	MOV	B,L
46	MOV	B,M
47	MOV	B,A
48	MOV	C,B
49	MOV	C,C
4A	MOV	C,D
4B	MOV	C,E
4C	MOV	C,H
4D	MOV	C,L
4E	MOV	C,M
4F	MOV	C,A
50	MOV	D,B
51	MOV	D,C
52	MOV	D,D
53	MOV	D,E
54	MOV	D,H
55	MOV	D,L
56	MOV	D,M
57	MOV	D,A

INCREMENT**

04	INR	B
0C	INR	C
14	INR	D
1C	INR	E
24	INR	H
2C	INR	L
34	INR	M
3C	INR	A
03	INX	B
13	INX	D
23	INX	H
33	INX	SP

DECREMENT**

05	DCR	B
0D	DCR	C
15	DCR	D
1D	DCR	E
25	DCR	H
2D	DCR	L
35	DCR	M
3D	DCR	A
0B	DCX	B
1B	DCX	D
2B	DCX	H
3B	DCX	SP

LOAD/STORE

0A	LDAX	B
1A	LDAX	D
2A	LHLD	Adr
3A	LDA	Adr
02	STAX	B
12	STAX	D
22	SHLD	Adr
32	STA	Adr

PSEUDO INSTRUCTION

ORG	Adr	
END		
EQU	D16	
DS	D16	
DB	D8	[,]
DW	D16	[,]

STANDARD SETS

A	SET	7
B	SET	0
C	SET	1
D	SET	2
E	SET	3
H	SET	4
L	SET	5
M	SET	6
SP	SET	6
PSW	SET	6

D8 = constant, or logical/arithmetic expression that evaluates to an 8 bit data quantity.

D16 = constant, or logical/arithmetic expression that evaluates to a 16 bit data quantity.

Adr = 16 bit address

* = all Flags (C,Z,S,P) affected

† = only CARRY affected

** = all Flags except CARRY affected; (exception: INX & DCX affect no Flags)

LOADING DIP (DUAL IN-LINE PACKAGE) DEVICES

Most DIP devices have their leads spread so that they can not be dropped straight into the board. They must be "walked in" using the following procedure:

(1) Orient the device properly. Pin 1 is indicated by a small embossed dot on the top surface of the device at one corner. Pins are numbered counterclockwise from pin 1.

(2) Insert the pins on one side of the device into their holes on the printed circuit card. Do not press the pins all the way in, but stop when they are just starting to emerge from the opposite side of the card.

(3) Exert a sideways pressure on the pins at the other side of the device by pressing against them where they are still wide below the bend. Bring this row of pins into alignment with its holes in the printed circuit card and insert them an equal distance, until they begin to emerge.

(4) Press the device straight down until it seats on the points where the pins widen.

(5) Turn the card over and select two pins at opposite corners of the device. Using a fingernail or a pair of long-nose pliers, push these pins outwards until they are bent at a 45 degree angle to the surface of the card. This will secure the device until it is soldered.

SOLDERING TIPS

(1) Use a low-wattage iron — 25 watts is good. Larger irons run the risk of burning the printed-circuit board. Don't try to use a soldering gun, they are too hot.

(2) Use a small pointed tip and keep it clean. Keep a damp piece of sponge by the iron and wipe the tip on it after each use.

(3) Use 60-40 rosin-core solder ONLY. DO NOT use acid-core solder or externally applied fluxes. Use the smallest diameter solder you can get.

NOTE: DO NOT press the top of the iron on the pad or trace. This will cause the trace to "lift" off of the board which will result in permanent damage.

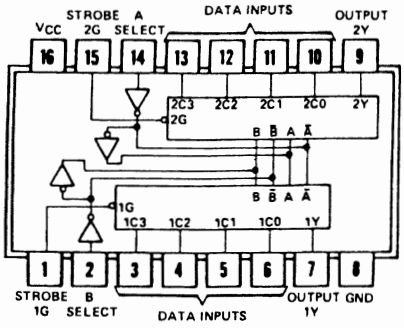
(4) In soldering, wipe the tip, apply a light coating of new solder to it, and apply the tip to both parts of the joint, that is, both the component lead and the printed-circuit pad. Apply the solder against the lead and pad being heated, but not directly to the tip of the iron. Thus, when the solder melts the rest of the joint will be hot enough for the solder to "take," (i.e., form a capillary film).

(5) Apply solder for a second or two, then remove the solder and keep the iron tip on the joint. The rosin will bubble out. Allow about three or four bubbles, but don't keep the tip applied for more than ten seconds.

(6) Solder should follow the contours of the original joint. A blob or lump may well be a solder bridge, where enough solder has been built upon one conductor to overflow and "take" on the adjacent conductor. Due to capillary action, these solder bridges look very neat, but they are a constant source of trouble when boards of a high trace density are being soldered. Inspect each integrated circuit and component after soldering for bridges.

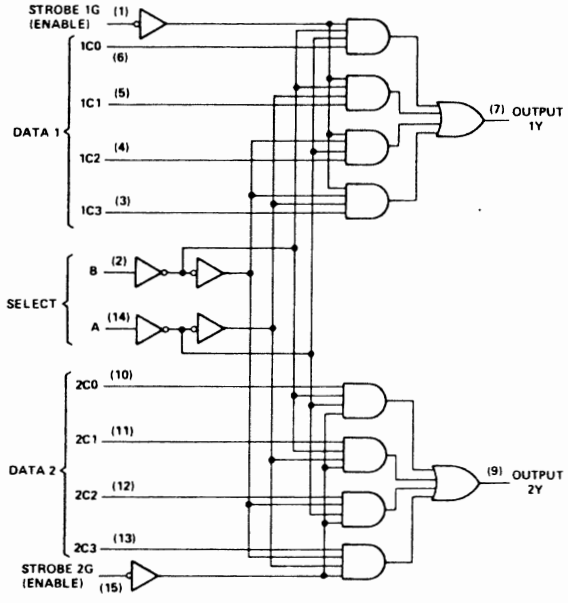
(7) To remove solder bridges, it is best to use a vacuum "solder puller" if one is available. If not, the bridge can be reheated with the iron and the excess solder "pulled" with the tip along the printed circuit traces until the lump of solder becomes thin enough to break the bridge. Braid-type solder remover, which causes the solder to "wick up" away from the joint when applied to melted solder, may also be used.

AM25LS153PC

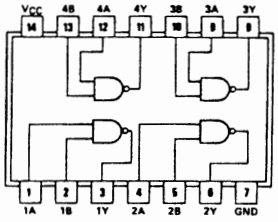


SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

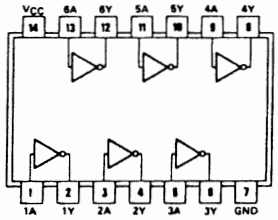


DM7400



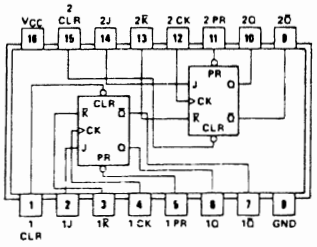
positive logic:
$Y = \overline{AB}$

DM7406



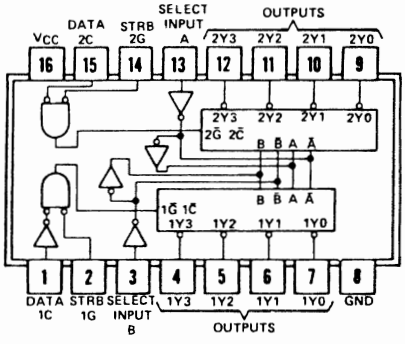
positive logic:
$Y = \overline{A}$

DM74109 or DM8124N



INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\bar{K}$	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\bar{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\bar{Q}_0$

DM74155

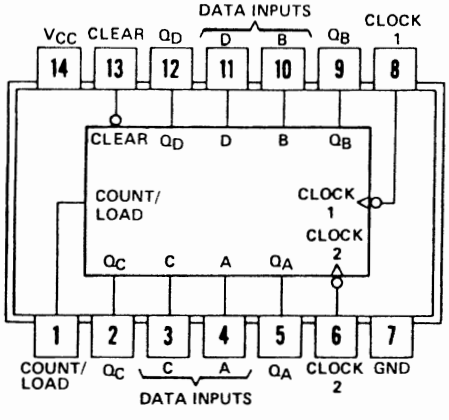


2-LINE-TO-4-LINE DECODER
OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

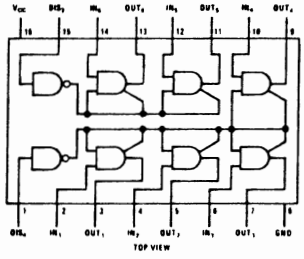
INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

DM74177



asynchronous input: Low input to clear sets Q_A, Q_B, Q_C, and Q_D low.

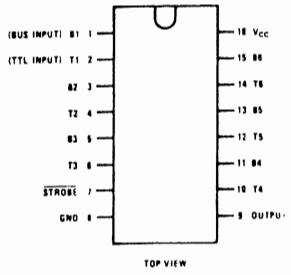
DM8097

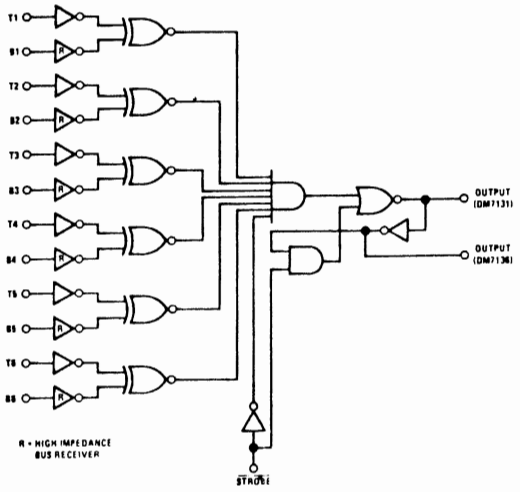


DISABLE DIS_4	INPUT DIS_2	INPUT	OUTPUT
0	0	0	0
0	0	1	1
X	1	X	H-Z*
1	X	X	H-Z**

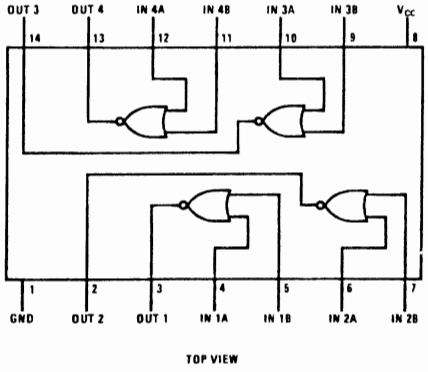
*Output 5-6 only
**Output 1-4 only
X = Irrelevant

DM8131

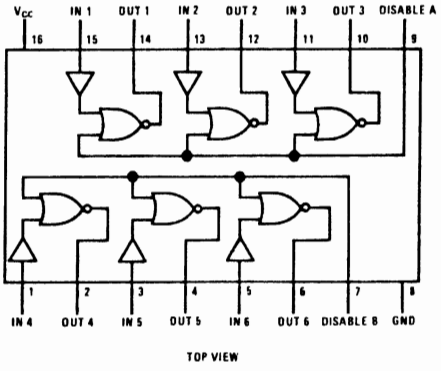




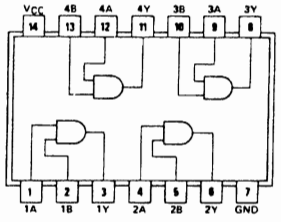
DM8836



DM8837

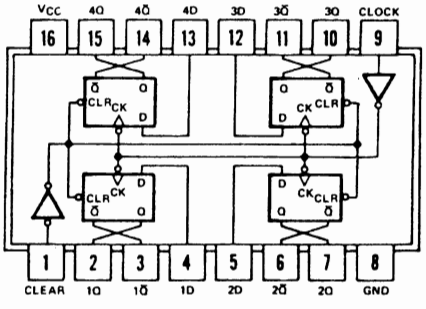


N74LS08

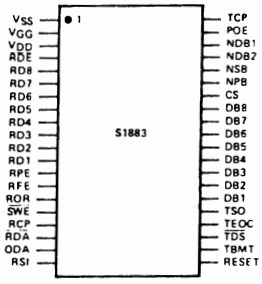


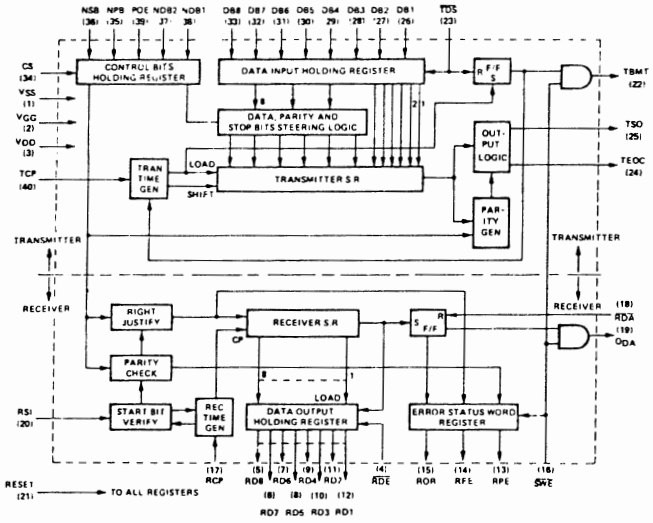
positive logic:
Y = AB

SN74175

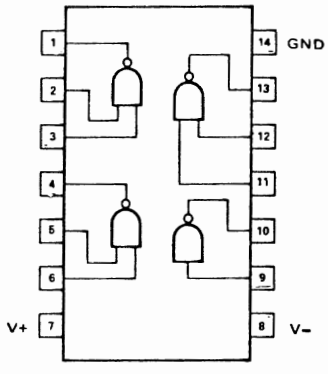


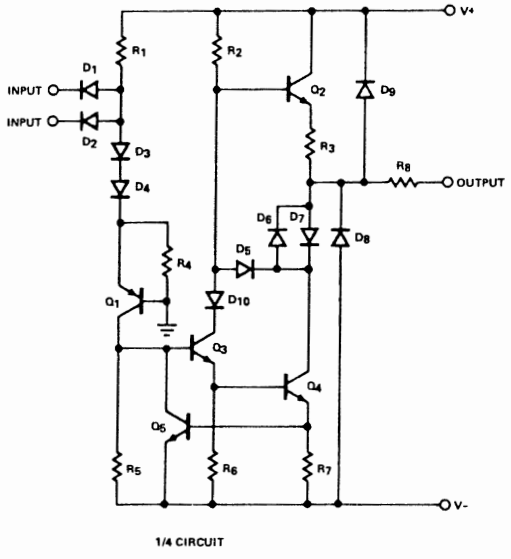
S1883





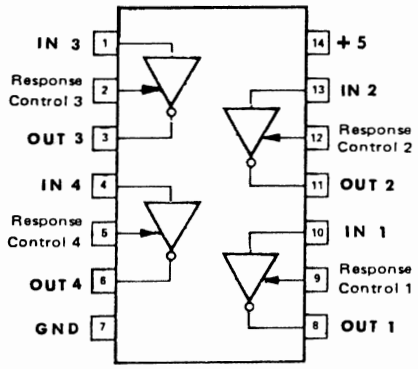
1488PC

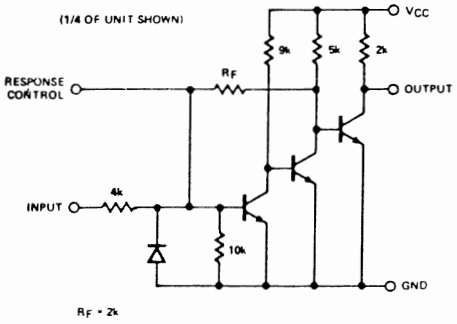




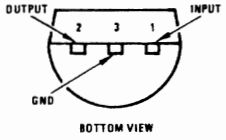
1/4 CIRCUIT

1489APC

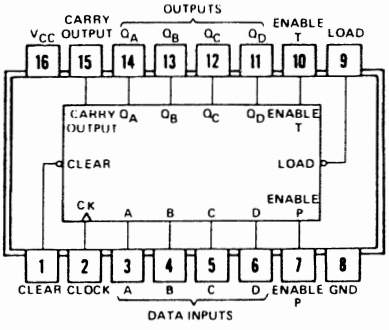




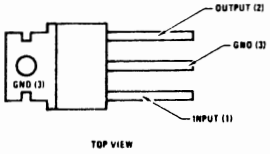
78L12ACZ

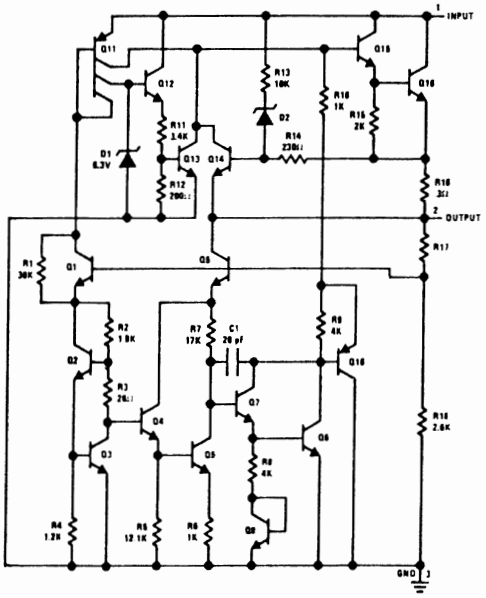


93L16PC

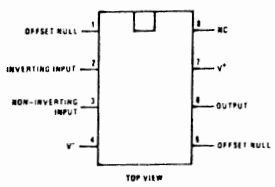


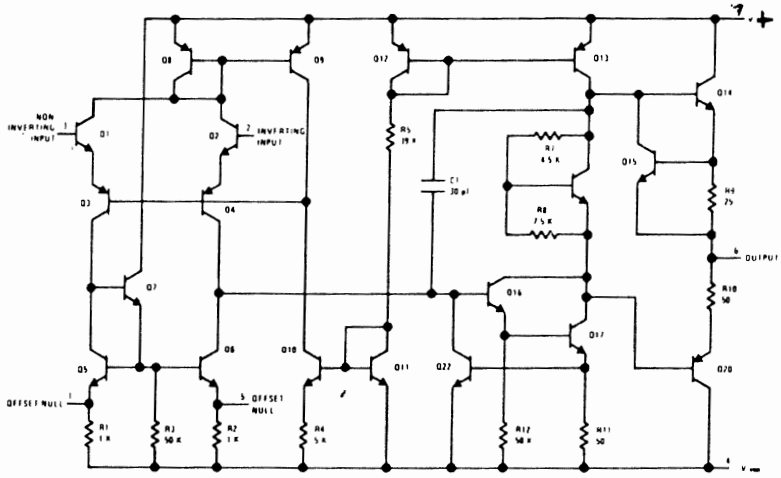
LM340T-5.0





LM741CN


OFFSET NULL
INVERTING INPUT
NON-INVERTING INPUT
V-
NC
V+
OUTPUT
OFFSET NULL
TOP VIEW


NON INVERTING INPUT
INVERTING INPUT
OFFSET NULL
OFFSET NULL
OUTPUT

V.1 PARALLEL INPUT/OUTPUT, TESTS 1 AND 2

```
                        0000 *  3P+S PARALLEL PORT TEST PROGRAMS
                        0005 *  PROCESSOR TECHNOLOGY CORP.
                        0010 *  2465 FOURTH STREET
                        0015 *  BERKELEY, CALIF 94710
                        0020 *  (415) 549-0857
                        0025 *
                        0030 *
                        0035 * THESE PROGRAMS ASSEMBLED USING THE ALS-8 RESIDENT
                        0040 * FIRMWARE EXECUTIVE, EDITOR AND ASSEMBLER.




                        0005 * TEST NO. 1
                        0010 *  THIS TEST CHECKS OUTPUT PORTS A AND B. THE SENSE
                        0015 *  SWITCHES ARE OUTPUT TO PORTS A AND B. IF FOR EXAMPLE
                        0020 *  SENSE SWITCH 0 (ADDR. 8) IS UP, THE OUTPUT FROM
                        0025 *  BIT 0, I.E. PIN 1 FOR PORT A OR PIN A FOR PORT B,
                        0030 *  SHOULD BE HIGH (APPROX. FROM 2.5 TO 5.0 VOLTS DC.
                        0035 *  IF THE SENSE SWITCH IS DOWN THE OUTPUT SHOULD BE
                        0040 *  FROM 0 TO 0.5 VOLTS DC. PLEASE NOTE THAT ON OUTPUT
                        0045 *  PORT CONNECTOR J1 THE PIN NUMBERS DO NOT FOLLOW
                        0050 *  THE OUTPUT BIT NUMBERS IN NUMERICAL ORDER.
                        0055 *
0000 DB FF              0060 LOOP IN 0FFH
0002 D3 06              0065  OUT PRTA
0004 D3 07              0070  OUT PRTB
0006 C3 00 00           0075  JMP LOOP
0009                    0080 PRTA EQU 6 *ASSUME AREA A IS SET TO RECOGNIZE
0009                    0085 PRTB EQU 7 *CARD ADDRESS 34HEX




                        0000 *   TEST NO. 2
                        0002 *  THIS TEST CHECKS THE INPUT PORTS. EACH INPORT
                        0005 *  PIN SHOULD BE GROUNDED. THE CORRESPONDING OUTPUT BIT
                        0010 *  WILL GO FROM HIGH (APPROX. 2.5 TO 5.0 VDC) TO LOW
                        0015 *  (APPROX. 0 TO .5 VDC) FOR BOTH PORTS A AND B.
                        0020 *  FOR THESE TESTS THE 3P+S SHOULD BE SET UP WITH
                        0025 *  THE PARALLEL PORTS AS THE HIGHER TWO ADDRESSES
                        0030 *  AND THE SERIAL AND CONTROL PORTS AS THE LOWER TWO
                        0035 *  ADDRESSES. I.E. SET  THE JUMPER IN AREA B FROM L@
                        0040 *  LEFT TO RIGHT.
0000                    0045 *
0000                    0050 *
0000                    0055 *
0000 DB 06              0060 LOP IN PRTA
0002 D3 06              0065  OUT PRTA
0004 C3 00 00           0070  JMP LOP
0007 DB 07              0075 LOOP IN PRTB
0009 D3 07              0080  OUT PRTB
000B C3 07 00           0085  JMP LOOP
000E                    0090 PRTA EQU 6
000E                    0095 PRTB EQU 7
000E                    0100 *START PROGRAM AT ADDRESS 0000 TO TEST
000E                    0105 *PORT A, START AT ADDRESS 0007
000E                    0110 *TO TEST  INPUT PORT B.
```

V.2 SERIAL INPUT/OUTPUT, TEST 3

The Serial Input/Output Test consists of two tests, Test 1 and Test 2 (not to be confused with Parallel Port Tests 1 and 2). In addition to testing the 3P+S, these tests-which are coded-provide an opportunity to become familiar with handling input and output to your machine.

Service routines are coded to reside in restart locations on page Ø so that they can be left there. Restart routines 1, 2, 3, 4 and 5 are, in general, standard types of I/O service routines that provide the ability to input a character and echo it to the output device. Carriage return and line feed routines are also included. At the conclusion of the test, a patch is provided to disable the delay routine used during the test.

V.2.1 Test Preparation (Prior to Installing 3P+S)

Step 1. In Area G, jumper TBE (transmitter buffer empty) and RDA (receiver data available) flags to D7 and D6 respectively. (Refer to Paragraph 3.1.2 in Section III.)

Step 2. In Area E, select Baud rate (refer to Paragraph 3.1.3 in Section III) required by the peripheral device you are using. Baud rate is the number of bits serialized per second, and will probably be some fixed rate: for example, 110 for a Teletype, 134.5 for a Selectric and 45.5 for a Model 15 Teletype. In setting the Baud rate, you are establishing a speed match between the computer and I/O device.

Step 3. In Area G, jumper OE (overrun error), FE (framing error) and PE (parity error) status flags to any available data bits. (Refer to Paragraph 3.1.2 in Section III.) Being able to monitor these flags can be useful if you have a keyboard of unknown ancestry or quality.

> OE indicates the UART received the character, but before you could unload it with IN1, another character started to write into the UART buffer.
>
> FE indicates the UART did not see an expected stop bit at the end of the serial data. A consistent FE indication means, in all probability, that the Baud rate is not properly jumpered. Cold solder joints could well be the problem. Cold solder joints can be detected by measuring the voltages on pins 3, 4, 5 and 6 of IC 7, 8 and 9. (Ø = Ø volts, 1 = 3.2 to 5 volts) A 2 volt reading indicates a probable cold solder joint.
>
> PE indicates the UART detected a parity error in the data.

Step 4. In Area H, select word length and number of stop bits required by the device you are using. (Refer to Paragraph 3.1.3 in Section III.)

Step 5. Configure the 3P+S to interface the peripheral you are using. (Refer to Section IV.)

Step 6. Carefully check your jumpers to confirm they are all made correctly.

Step 7. Install 3P+S.

V.2.2 Serial Test 1

Step 1. Enter the program given in Paragraph V.2.5 through the front panel switches in the same way you would enter a bootstrap program. Be sure that what you enter is correct, for it is easy to make an error when switching data in through the front panel.

Step 2. Put all front panel switches down and raise the EXAMINE switch. You should be looking at address 0000H which contains 31H. If not, again raise EXAMINE switch and make sure all address switches are down.

Step 3. Single step to location 08H. This takes a long time for much initialization takes place, a restart 3 is executed to load register A with the pattern 0DH and perform a restart 2. Restart 2 moves register A to register B and does a restart 1 which inputs status.

Step 4. When you reach 08H, single step once. The INPUT light should come on. You should also see data bit D7 (TBE), but not D6 (RDA). Nor should you see the bits associated with OE, FE and PE. If you do, the Baud rate is incorrect, the peripheral device is fast or slow, or the word length is incorrect.

Step 5. Assuming the correct indications in Step 4, single step to location 13H. Then single step three times. If you have an ASCII device, it should have performed a carriage return. If you have output by the time you reach 15H, you're well on the way to verifying correct assembly of your 3P+S.

Step 6. Continue single stepping to see if you get a line feed by the next time you get to 15H. If you do, press the RUN switch. Your device should output this character string:

0123456789:;<=>?"@ABCDEFGHIJKLMNOPQ

(30H) ——————————————————→ (51HEX)

NOTE

If you are outputting to a Baudot or Selectric, the character string will be either slightly or greatly different, depending on the code your device should get.

If there is no output to the device, check the following:

1. Is there any detectable action at the device? Some action, even if wrong, can indicate a possible place to look for trouble.

2. Make sure you have a signal ground from your device to J1 or J2. If you are connected through 25-pin connectors to the back of the computer, pin 7 is signal ground.

   EIA signals leave the 3P+S through pin M of J1 to pin 3 of the 25-pin connector. They come in on pin 2 of the 25-pin connector to pin K of J2 on the 3P+S.

   If you are using current loop, make sure you have a loop and current in the loop. (Pin assignments for the 25-pin connectors are not standardized for current loop operation.

3. Raise Switch 8 to introduce a delay loop in the program. This puts a delay between each character. If your device now outputs the character stream, you probably selected the wrong number of stop bits. A stop bit is a steady "make" ("1" bit) that marks the end of a character and restores the serial transmission signal to a "make" (looped) condition.

4. If you are using EIA, double check the jumpers you installed on the 3P+S. Consult schematic to determine bits that may be failing or functions that are inoperative. Change the wiring on J1 and J2 (J2-K to J2-L and J1-M to J1-N) to use one of the other EIA circuits. If there is now output to the device, you may have a bad IC.

5. If you are using current loop, doublecheck the jumpers you installed.

Step 7. Once you obtain the character stream without the delay loop, proceed to Serial Test 2.

V.2.3 Serial Test 2

Step 1. Lower Switch 8 if you used the delay in Serial Test 1 and raise Switch 15.

Step 2. This step inputs the status of Port Ø and checks the RDA flag. Single step until you get to location 20H. While looking at the INP (input) light, single step once. When INP lights, data bit D6 (RDA) should be off.

Step 3. Strike a key on your device. D6 should light. If not, status is not being received correctly. If you did not get FE or D6, the serial transmission was either not received or the connections are not correct.

Should you be unable to get D6 to light, check the Baud rate. If an FE indication persists, look for a bad integrated circuit in IC 7, IC 8, IC 9 or IC 21. Try switching identical IC types to locate the problem.

If D6 lights when the key is depressed, go on to the next step.

Step 4. Single step to location 28H. Single step once, and when INP lights, the data from the UART is displayed in DØ through D7. (It is echoed back from your I/O device.)

Data bit D7 may or may not indicate a parity bit. Some keyboard devices automatically generate parity, some do not. If you receive a parity bit from your device, you may have to add parity to any data you send to it.

The remainder of the program performs the functions to echo the input back to your I/O device.

If you have data problems after obtaining status, try these character sets:

U and * ? and @ RUBOUT and (CONTROL-SHIFT-P)

These bit patterns are alternate 1's and Ø's, and will thus help in locating a timing problem.

If you have no data problems after this step, your 3P+S is operating correctly.

V.2.4 Post Test Procedures (Optional)

Raise Switch 14 and strike a key. This causes 56H to be executed. If you have an instruction at this location it will be executed; if you have a halt; there will be a halt.

Should you wish to preserve the test for use when you want to input and output, or do a carriage return-line feed, change byte--

2A from 77 to D7 (RST2) CHANGE

2B from F7 to C9 (RET) CHANGE

2C through 2F to 00 (NOP)

V.2.5 Serial Input/Output Test Program

```
0000                    0001 *
0000                    0002 *
0000                    0003 *
0000                    0004 *              <<<  SERIAL I/O TEST  >>>
0000                    0005 *
0000                    0006 *  PROCESSOR TECHNOLOGY CORP.
0000                    0007 *  6200 HOLLIS STREET
0000                    0008 *  EMERYVILLE, CALIF.  94608
0000                    0009 *  (415) 652-8080
0000                    0010 *
0000                    0011 *
0000                    0012 IBUF   EQU    $+3    SET SPECIAL BUFFER NEAR HERE
0000 C3 6B 00           0013        JMP    INIT
0003                    0014        ORG    8
0008                    0015 *
0008                    0016 *  -RST 1-  LOOP UNTIL TBE IS OK
0008 DB 00              0017 TBET   IN     STATUS
000A E6 80              0018        ANI    TBE    TBE "AND"WITH THE BIT MASK
000C C0                 0019        RNZ    .      LEAVE WHEN BIT GOES TRUF
000D C3 08 00           0020        JMP    TBET
0010                    0021 *
0010                    0022 *
0010                    0023 *  -RST 2-  OUTPUT CHR IN REG "A"
0010 47                 0024 COUT   MOV    B,A    HOLD CHAR IN REG B
0011 CF                 0025        RST    1      GO FIND TBE
0012 78                 0026        MOV    A,B    GET OUTPUT CHAR
0013 D3 01              0027        OUT    PORT1  PUT IT OUT
0015 C9                 0028        RET
0016 00                 0029        NOP
0017 00                 0030        NOP
0018                    0031 *
0018                    0032 *  -RST 3-  CARRIAGE RETURN/LINE FEED
0018 3E 0D              0033 CRLF   MVI    A,0DH  SET UP C/R.
001A D7                 0034        RST    2      OUTPUT IT
001B 3E 0A              0035        MVI    A,10   NOW THE LINE FEED
001D D7                 0036        RST    2      IT ALSO
001E C9                 0037        RET
001F 00                 0038        NOP
0020                    0039 *  -RST 4-  HAS CHAR BEEN INPUT?
0020 DB 00              0040 CKIN   IN     STATUS  GET STATUS
0022 E6 40              0041        ANI    RDA    RDA "AND" WITH RDA MASK BIT
0024 C0                 0042        RNZ    .      LEAVE WHEN BIT COMES TRUE
0025 C3 20 00           0043        JMP    CKIN   LOOP UNTIL IT DOES
0028                    0044 *
0028                    0045 *  -RST 5-  GET CHAR FROM INPUT PORT
0028 DB 01              0046 CGET   IN     PORT1  GET CHAR FROM DATA PORT
002A 77                 0047        MOV    M,A    COPY TO LOCATION 0003
002B F7                 0048        RST    6      CHECK IF DELAY IS WANED
002C 7E                 0049        MOV    A,M    RETRIEVE CHAR
002D D7                 0050        RST    2      ECHO THE CHR
```

```
002E C9                 0051          RET
002F 00                 0052          NOP
0030                    0053 *
0030                    0054 *   -RST 6-  FIND IF DELAY FROM SENSE SWITCHES
0030 DB FF              0055          IN    SNSW    INPUT THE SWITCHES
0032 0F                 0056          RRC   .       PUT BIT DO IN CARRY
0033 DC 5A 00           0057          CC    DELAY   DO DELAY IF CARRY
0036 C9                 0058          RET
0037                    0059 *
0037                    0060 *    TESTS BEGIN HERE
0037                    0061 *
0037 DF                 0062 TEST1    RST   3       DO CR,LF
0038 7A                 0063 T1C1     MOV   A,D     GET TEST CHR
0039 D7                 0064          RST   2       OUTPUT IT
003A DB FF              0065          IN    SNSW    INPUT FROM SENSE W SWITCHES
003C 07                 0066          RLC   .       PUT D7 IN CARRY
003D DA 49 00           0067          JC    TEST2   IF BIT 7 IS UP THEN EXIT TEXT1
0040 F7                 0068          RST   6       CHECK IF DELAY IS WANTED
0041 14                 0069          INR   D       FORM NEXT TEST CHAR
0042 0C                 0070          INR   C       BUMP CHAR COUNTER
0043 CA 71 00           0071          JZ    CRST    RESET CHARACTER STRING
0046 C3 38 00           0072          JMP   T1C1    LOOP FOR TEST1
0049                    0073 *
0049                    0074 *
0049 E7                 0075 TEST2    RST   4       CHECK IF CHR HAS BEEN INPUT
004A EF                 0076          RST   5       GO INPUT IT
004B DB FF              0077          IN    SNSW    INPUT THE SWITCHES
004D 07                 0078          RLC   .       PUT D6....
004E 07                 0079          RLC   .       ....IN THE CARRY
004F DA 55 00           0080          JC    ENDT    IF 6 THEN END OF TESTS
0052 C3 49 00           0081          JMP   TEST2   KEEP ON TRUCKIN
0055                    0082 *
0055 76                 0083 ENDT     HLT   .       STOP HERE ON END OF TEST
0056                    0084          DS    4       ROOM FOR OTHER "ENDS"
005A                    0085 *
005A                    0086 *    DELAY LOOP
005A                    0087 *
005A CF                 0088 DELAY    RST   1       WAIT FOR TBE
005B E5                 0089          PUSH  H       DO ALL KNIDS OF..
005C AF                 0090          XRA   A       .....STALL TACTICS
005D 6F                 0091          MOV   L,A     CLEAR L
005E 67                 0092          MOV   H,A     CLEAR H
005F EB                 0093 STALL    XCHG  .       SWAP REGISTERS
0060 EB                 0094          XCHG  .       BACK AGAIN
0061 2C                 0095          INR   L       COUNT UP IN REG L
0062 C2 5F 00           0096          JNZ   STALL   LOOP
0065 24                 0097          INR   H       COUNT UP IN REG H
0066 C2 5F 00           0098          JNZ   STALL   MORE LOOP
0069 E1                 0099          POP   H       RETRIEVE THE REAL H&L
006A C9                 0100          RET   .       AND QUIT STALLING
006B                    0101 *
006B                    0102 *   -- INITIALIZATION -START PROGRAM HERE
006B                    0103 *
006B 31 FF 00           0104 INIT     LXI   SP,255  SET UP STACK
006E 21 03 00           0105          LXI   H,IBUF  SET MEMORY REFERENCE
0071 16 30              0106 CRST     MVI   D,30H   SET FIRST CHR
0073 0E D5              0107          MVI   C,0D5H  PRINT FROM 0 TO Z
0075 C3 37 00           0108          JMP   TEST1   GO TO FIRST TEST
```

```
0078                    0109 *
0078                    0110 *     EQUATES
0078                    0111 *
0078                    0112 STATUS EQU   0       BIT FOR STATUS INPUT PORT
0078                    0113 PORT1  EQU   1       DATA INPUT PORT
0078                    0114 TBE    EQU   80H     TBE BIT MASK
0078                    0115 RDA    EQU   40H     RDA BIT MASK
0078                    0116 SNSW   EQU   0FFH    SENSE SWITCH PORT

CGET    0028
CKIN    0020    0043
COUT    0010
CRLF    0018
CRST    0071    0071
DELAY   005A    0057
ENDT    0055    0080
IBUF    0003    0105
INIT    006B    0013
PORT1   0001    0027 0046
RDA     0040    0041
SNSW    00FF    0055 0065 0077
STALL   005F    0096 0098
STATU   0000    0017 0040
T1C1    0038    0072
TBE     0080    0018
TBET    0007    0020
TEST1   0037    0108
TEST2   0049    0067 0081
```