EXPLORER 85

LEVEL B ASSEMBLY MANUAL

SPECIFICATIONS

The Level B expansion kit provides the signals plus buffers/drivers to support up to 6 S100 bus boards. Level B also includes the following:

a) address decoding for on board 4K RAM expansion selectable in 4K blocks
b) address decoding for on board 8K EPROM expansion selectable in 8K blocks
c) address and data bus drivers for on board expansion
d) Wait state generator (jumper selectable) to allow the use of slower memories
e) two separate 5V regulators to insure maximum stability and a noise free bus

PARTS LIST

Please check your kit against the following list of parts:

Description	Quantity
IC Socket 14 pin	10
IC Socket 16 pin	7
IC Socket 24 pin	1
IC 74LS244	4
IC 8216	4
IC 74LS20	1
IC 74LS138	3
IC 74LS30	1
IC 8212	1
IC 74LS04	3
IC 74LS74	2
IC 74LS10	2
IC 74LS00	1
5 Volt Regulators LM340T or (7805)	2
Heatsink	2
Screw 6-32 x 3/8"	2
Nut 6-32	2
Capacitor 10uf electrolytic	2
Capacitor .01 disc	25
Capacitor 150pf disc	1
Resistor 100 ohm (brown, black, brown)	1
Resistor 4.7K (yellow, violet, red)	29
Assembly Manual	1

ASSEMBLY INSTRUCTIONS

( ) 1. Install 14 Pin IC sockets at locations U202,204,210,211,212,215,216, 218,220, and 221. (Solder)

( ) 2. Install 16 Pin IC sockets at locations U200,201,203,205,206,207, and 217. (Solder)

( ) 3. Install 24 Pin IC socket at location U208. Note no sockets are supplied or recommended for U9,13,14 or 19.

( ) 4. Remove Jumper S-11 installed in Level A system.

( ) 5. Using a safety razor blade or sharp knife, cut the foil pattern jumper on the bottom side of the board between pins 3 and 4, 6 and 7, 9 and 10, and 12 and 13 on both IC U206 and U207.

( ) 6. Install the 5 Volt regulators LM 340T or (7805) at locations Q200 and Q201. Install the heat sinks between the regulator and the PC board and secure with 6-32 screws and nuts as shown. (Solder)

Before proceeding apply power and check output voltage of Q200 and Q201. The reading should be 5V$\pm$ 5%

( ) 7. Install the 10 uF capacitors at locations C200 and C203. Note polarity. (Solder)

( ) 8. Install the 100Ω resistor (brown, black, brown) at location R228. (Solder)

( ) 9. Install the 150 pf Disc capacitor at location C229. (Solder)

( ) 10. Install resistor 4.7K (yellow, violet, red) at locations R200-227, 229. (Solder)

( ) 11. Install capacitors .01 Disc at locations C201,204-225,227 and 228. Note C203 and 226 are not assigned. (Solder)

( ) 12. Install IC 74LS244 in locations IC U209,213,214 and 219. Note no sockets are supplied or recommended. (Solder)

( ) 13. Install IC 8216 in locations U200,201,206,207.

( ) 14. Install IC 74LS20 in location U202

( ) 15. Install IC 74LS138 in locations U203,205,217.

( ) 16. Install IC 74LS30 in location U204.

( ) 17. Install IC 8212 in location U208.

( ) 18. Install IC 74LS04 in location U210,212,216.

( ) 19. Install IC 74LS74 in location U211,220.

( ) 20. Install IC 74LS10 in locations U215,221.

( ) 21. Install IC 74LS00 in location 218.

( ) 22. Placing a jumper in S-1 will add 1 wait-state to each machine cycle and may be required if you are using slow memory. Do not install S-1 at this time.

( ) 23. No jumpers or switches are required at locations SW200, 201. These are only required for Levels D & E.

( ) 24. Install optional S100 Bus connectors in locations J3 and J4.

( ) 25. Power supply connections to the S100 bus boards are located at the front left side of the Mother Board. If your S100 boards require only +8VDC, you may connect the +8V S100 power input to the +8V system input located on the rear of the Mother Board.

WARRANTY: All components of this kit are warranteed for six months from the date of shipment. Defective components will be replaced free of charge if returned within six months with $1.00 each to cover testing and return postage. Return parts in a suitable package and ship insured to Netronics Research & Development Limited, Route 202, New Milford, Connecticut 06776, attention: Service Department, with a letter explaining the defect. Any parts received damaged due to poor packaging will be returned. (i.e., DO NOT ship IC's in envelopes via the mail).

IN CASE OF DIFFICULTY: After having carefully checked your work and you still have difficulty getting your Explorer to work, the Factory Service Department will repair, fully test, and return your system for a flat fee (see below). This covers all parts, except parts destroyed by your negligence, (i.e., IC installed backwards, broken, etc.), and return postage. Package the unit (less cabinet) carefully and return insured with a letter describing the difficulty.

If your system includes other level components, please see the instruction book for fees which apply to the further expanded systems. If any components are added which are not part of a Netronics kit you will be advised of the service charge prior to any work being done. If you have added any "Levels" to your system (using your own parts) it would be advisable to purchase the appropriate assembly manual, which will contain any factory modifications or updates, prior to returning your unit.

SCHEDULE OF IN WARRANTY FACTORY TROUBLESHOOTING PRICES*

	FLAT FEE
Level A	$12.50
Hex Keypad/Display	7.00
Level A + B	16.50
Level A + B + D and/or E	20.00
Power Supply	6.50
ASCII Keyboard	7.00
Video Display Board	9.50

* Covers cost of all parts except those destroyed by the customer. These prices are not valid for levels added using parts not obtained from Netronics. If you have parts not supplied by Netronics send your unit and request a quotation.

← INTO CPU
→ INTO S100

EXPLORER-85 S100 BUS SIGNAL DEFINITIONS

PIN NUMBER		SYMBOL	NAME	FUNCTION
1		+8V		Unregulated +8 volts on bus to power S100 cards
2		+16V		Unregulated +16 volts on bus to power S100 cards
3	←	$\overline{\text{XRDY}}$	External Ready	A low on this line causes the processor to enter a WAIT state
4		N/C	Vectored Interrupt Line 0	These may be connected to RST 5.5, RST 6.5, RST 7.5 or the TRAP input for custom applications
5		N/C	Vectored Interrupt Line 1	
6		N/C	Vectored Interrupt Line 2	
7		N/C	Vectored Interrupt Line 3	
8		N/C	Vectored Interrupt Line 4	
9		N/C	Vectored Interrupt Line 5	
10		N/C	Vectored Interrupt Line 6	
11		N/C	Vectored Interrupt Line 7	
12		N/C		Not used by Explorer 85
13		N/C		Not used by Explorer 85
14		N/C		Not used by Explorer 85
15		N/C		Not used by Explorer 85
16		N/C		Not used by Explorer 85
17		N/C		Not used by Explorer 85
18	←	$\overline{\text{STAT DSB}}$	Status Disable	Tri-states the 8 status line buffers
19	←	$\overline{\text{CCDSB}}$	Command Control Disable	Tri-states the 6 command control line buffers
20		N/C UNPROT		Not used by Explorer 85
21		N/C 99		Not used by Explorer 85
22	←	$\overline{\text{ADDRDSBL}}$	Address Disable	Tri-states the 16 address line buffers

EXPLORER-85 S100 BUS SIGNAL DEFINITIONS

PIN NUMBER	SYMBOL	NAME	FUNCTION
23	$\overline{\text{DODSBL}}$	Data Out Disable	Tri-states the 8 data out lines
24	Ø2	Phase 2 Clock	
25	Ø1	Phase 1 Clock	
26	PHLDA	Processor Hold Acknowledge	Control output signal which appears when the processor is in the HOLD state
27	PWAIT	Processor Wait	Control output signal which appears when the processor is in a WAIT state
28			Not used by Explorer 85
29	A5	Address Line 5	
30	A4	Address Line 4	
31	A3	Address Line 3	
32	A15	Address Line 15	
33	A12	Address Line 12	
34	A9	Address Line 9	
35	DO 1	Data Out Line 1	
36	DO Ø	Data Out Line Ø	
37	A10	Address Line 10	
38	DO 4	Data Out Line 4	
39	DO 5	Data Out Line 5	
40	DO 6	Data Out Line 6	
41	D1 2	Data In Line 2	
42	DI 3	Data In Line 3	
43	DI 7	Data In Line 7	
44	SM1	Machine Cycle 1	Status output signal which indicates that the processor is in the fetch cycle for the first byte of an instruction

EXPLORER-85 S100 BUS SIGNAL DEFINITIONS

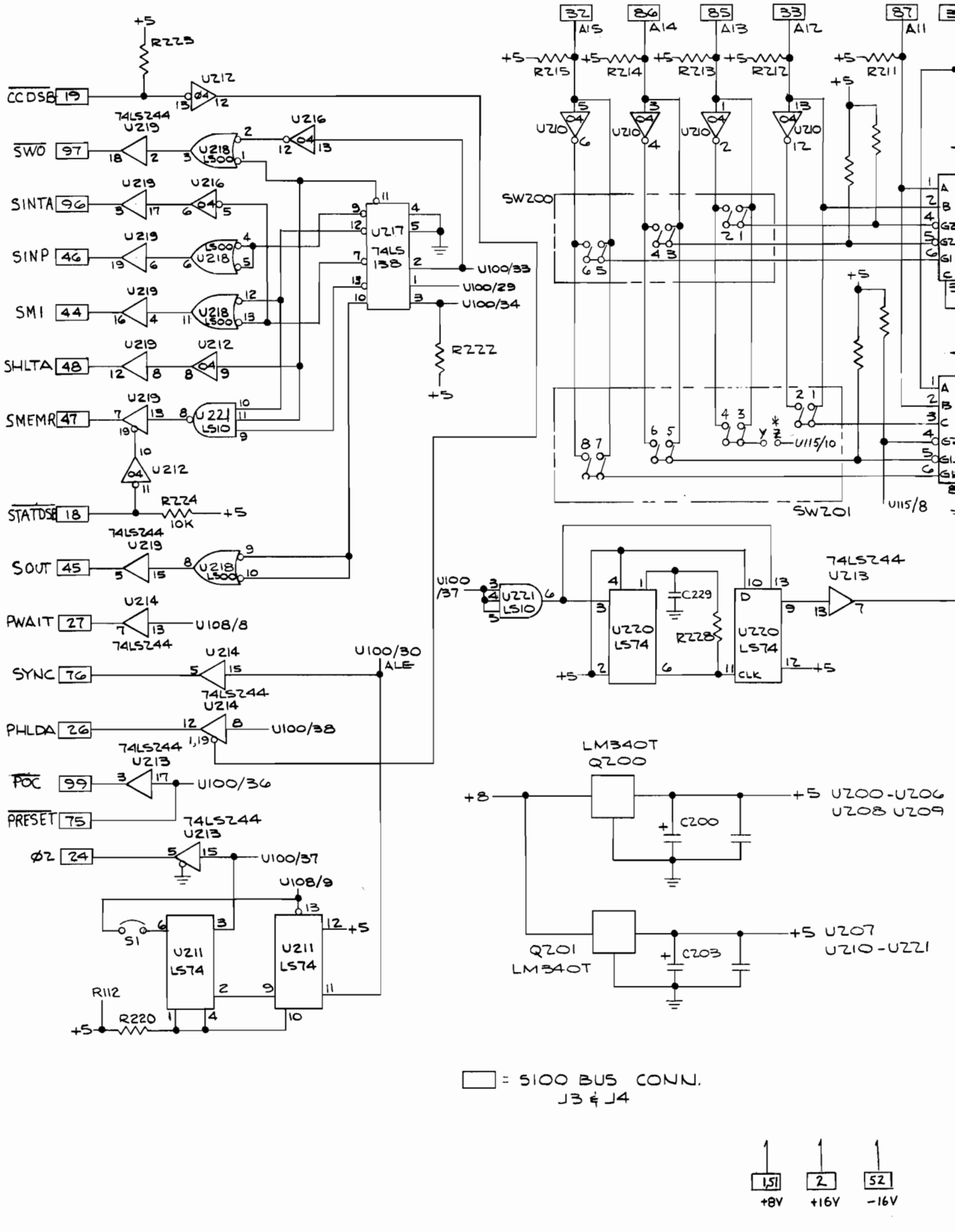
PIN NUMBER	SYMBOL	NAME	FUNCTION
→ 45	SOUT	Status Output	Status output signal which indicates that the address bus contains the address of an output device and the data bus will contain the output data if PWR is active
→ 46	SINP	Status Input	Status output signal which indicates that the address bus contains the address of an input device and that the data bus contains the input data if PDBIN is active
→ 47	SMEMR	Status Memory Read	Status output signal which indicates that the data bus will be used for memory read data
→ 48	SHLTA	Status Halt Acknowledge	Status output signal which acknowledges a HALT instruction
49			Not used in Explorer 85
50	GRD	S100 Bus Ground	
51	+8V		Unregulated +8V on bus to power S100 cards
52	-16V		Unregulated -16V to power S100 cards
53			Not used by Explorer 85
54			Not used by Explorer 85
55	AC	AC Input	Used for 50/60 Hz timer applications
56,57			Not used by Explorer 85
← 58	FRDY	Front Panel Ready	When low MWRITE is disabled
59-67			Not used by Explorer 85
→ 68	MWRITE	Memory Write	Indicates that the current data on the Data Out bus is to be written into the memory location currently on the address bus

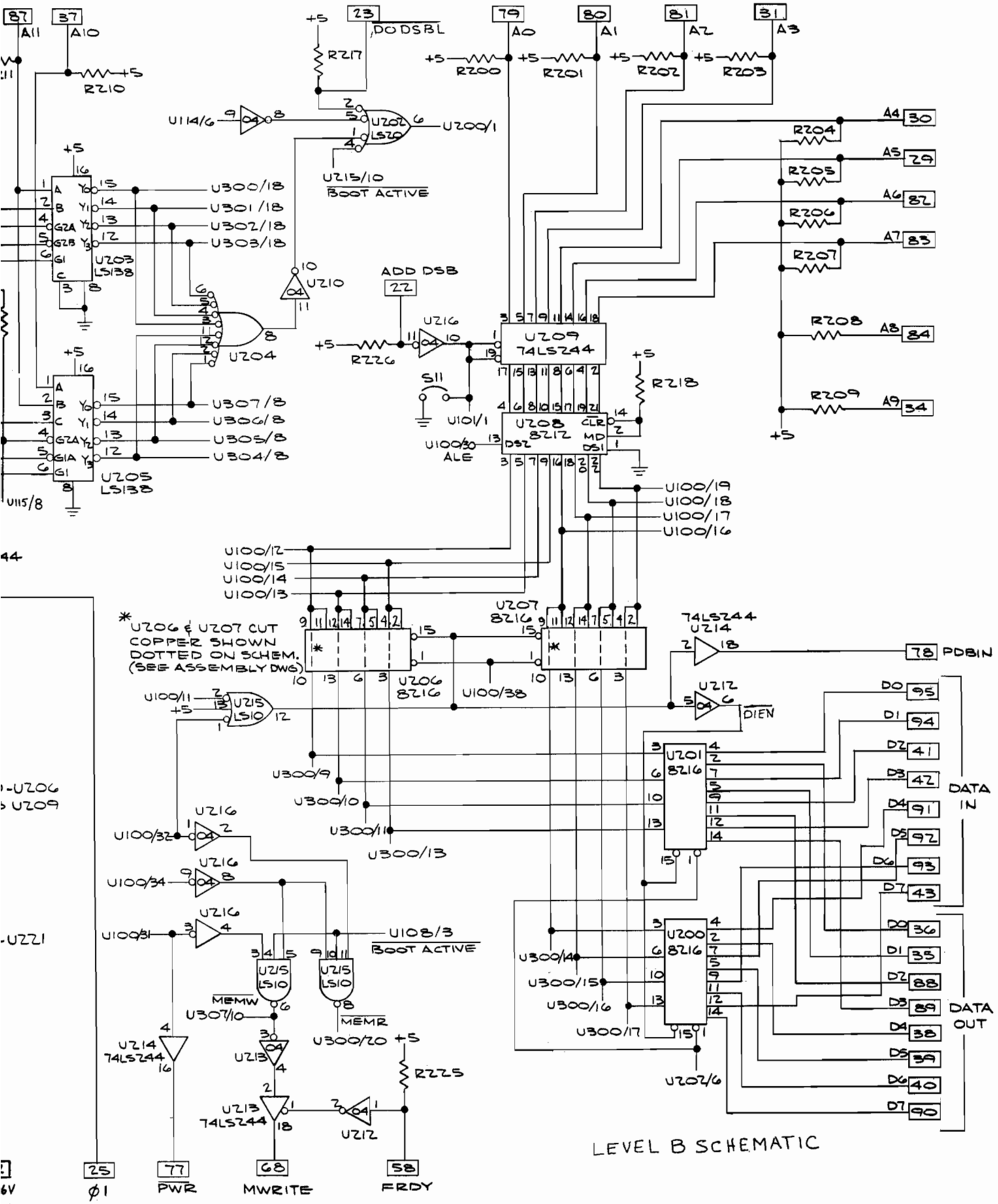
EXPLORER-85 S100 BUS SIGNAL DEFINITIONS

PIN NUMBER	SYMBOL	NAME	FUNCTION
69-71			Not used by Explorer 85
← 72	PRDY	Processor Ready	Command control input that controls the RUN state of the processor
← 73	$\overline{\text{PINT}}$	Interrupt Request	The processor will recognize an interrupt request on this line at the end of the current instruction or while halted
← 74	$\overline{\text{PHOLD}}$	Processor Hold	Processor command input signal which requests the processor to enter the HOLD state
← 75	$\overline{\text{PRESET}}$	Reset	Processor command input which resets the processor
→ 76	PSYNC	Sync Signal	Processor control output to indicate the beginning of each machine cycle
→ 77	$\overline{\text{PWR}}$	Processor Write	Processor control output used for memory write or I/O output control
→ 78	PDBIN	Data Bus In	Processor control output signal indicating to external circuits that the data bus is in the input mode
→ 79	AØ	Address Line Ø	
→ 80	A1	Address Line 1	
→ 81	A2	Address Line 2	
→ 82	A6	Address Line 6	
→ 83	A7	Address Line 7	
→ 84	A8	Address Line 8	
→ 85	A13	Address Line 13	
→ 86	A14	Address Line 14	
→ 87	A11	Address Line 11	

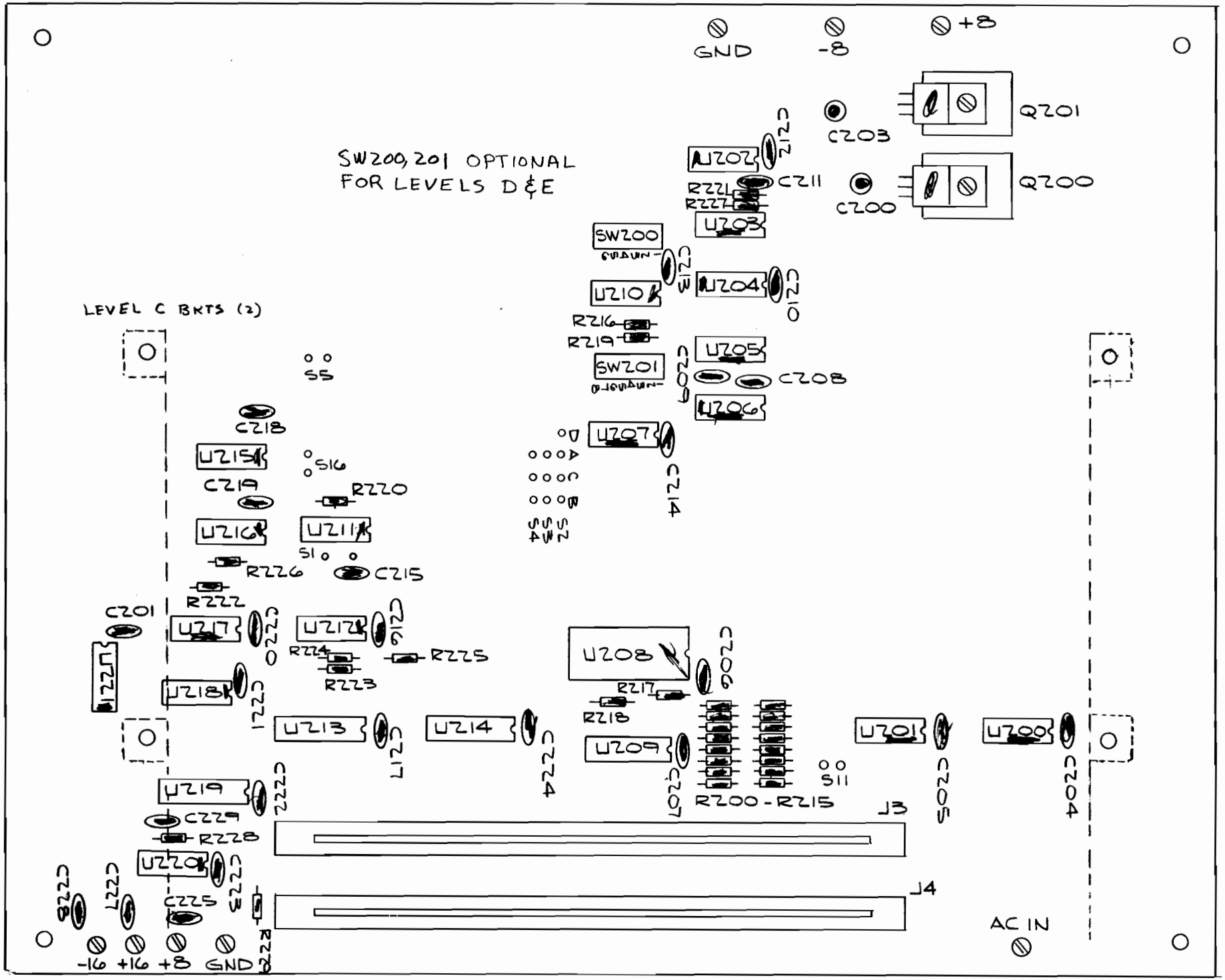
EXPLORER-85 S100 BUS SIGNAL DEFINITIONS

PIN NUMBER	SYMBOL	NAME	FUNCTION
→ 88	DO 2	Data Out Line 2	
→ 89	DO 3	Data Out Line 3	
→ 90	DO 7	Data Out Line 7	
← 91	DI 4	Data In Line 4	
← 92	DI 5	Data In Line 5	
← 93	DI 6	Data In Line 6	
← 94	DI 1	Data In Line 1	
← 95	DI Ø	Data In Line Ø	
← 96 →	SINTA	Interrupt Acknowledge	Status output to acknowledge signal to interrupt request
→ 97	$\overline{\text{SWO}}$	Status Write Output	Status output signal indicates that the operation in the current machine cycle will be a memory write or I/O function
98			Not used by Explorer 85
→ 99	$\overline{\text{POC}}$	Power On Clear	
100	GRD	Ground	


+5
RZ23
CCDSB 19
U212
74LS244
U219
SWO 97
U218 LS00
U216
SINTA 96
SINP 46
SM1 44
SHLTA 48
SMEMR 47
U221 LS10
STATDSB 18
RZ24 10K
SOUT 45
PWAIT 27
U108/8
SYNC 76
U100/30 ALE
PHLDA 26
U100/38
POC 99
U100/36
PRESET 75
Ø2 24
U100/37
U108/9
S1
U211 LS74
R112
R220
U217 74LS 138
U100/33
U100/29
U100/34
RZ22
32 A15
86 A14
85 A13
33 A12
87 A11
RZ15
RZ14
RZ13
RZ12
RZ11
SW200
SW201
U115/10
U115/8
U100 /37
U221 LS10
U220 LS74
C229
RZ28
74LS244 U213
LM340T Q200
C200
+8
+5 U200-U206 U208 U209
Q201 LM340T
C203
+5 U207 U210-U221
= S100 BUS CONN. J3 & J4
1,51 +8V
2 +16V
52 -16V



LEVEL B SCHEMATIC



LEVEL B ASSEMBLY [ ]G