The NABU 1100 System:
A Technical Guide

NOTICE

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Because of our policy of constantly searching for ways to improve our products, all specifications are subject to change without notice.

DIRECTORY

INTRODUCTION

The following technical manual for the Nabu 1100 System is designed to familiarize you with the components, internal hardware, and capabilities of your new system.

Basically, the manual contains documentation from the manufacturers of the system's components; such as Nabu, Volker-Craig, NEC, etc. It has been written for the knowledgeable user, with additional information included for those at an engineering level.

The computer itself, the keyboard/terminal, and the optional printer are the components of your system. The computer is manufactured by Nabu, and comes housed in a specially designed moveable cabinet, with two drawers. The lower drawer can be used for storage of diskettes etc., while the upper drawer contains the hardware associated with the computer. The system features 64K user memory capacity, and uses the Z-80A microprocessing unit developed by Zilog. Total storage capacity of the system is 2 Megabytes, with the use of floppy diskettes. As well, the system provides interfaces for printer and controls.

The keyboard/terminal is manufactured by Volker-Craig, and is microprocessor based; providing a full set of standard functions as well as a variety of options. The non-glare screen can display up to 24 lines x 80 characters (a total of 1920 character positions). The keyboard is detachable and features a full set of punctuation and special symbols, a variety of control keys, and a numeric keypad.

Printer options for the Nabu 1100 System include a NEC Spinwriter 5510/20, a NEC 3510/20, or a Centronics printer. Although these three options are available, the most common option is the NEC Spinwriter 5510/20, which is a letter-quality printer with a printing speed of up to 660 words a minute. The Spinwriter features an interchangeable, rotating thimble which contains up to 128 fully formatted characters, and has a color printing option.

Now that the system has been introduced and briefly described; the manufacturer's documentation on the system components will follow. This information should help you to understand, operate and maintain your system, in order to obtain the best possible performance from it!

SYSTEM MAINTENANCE

Maintenance of your new computer system should be one of your most important consideration, since proper maintenance can help avoid computer downtime and costly repairs.

General maintenance of the system involves periodic checks of the hardware. This preventive maintenance inspection should be done every six months by a qualified service Technician.

Regular cleaning should be done by the operator at least once a month as follows:

- vacuum under the system cabinet
- vacuum paper dust out of printer
- clean cabinet, printer, and screen with any spray cleaner and a soft cloth. *

* NOTE: Spray the cleaner only on the cloth, NOT ON THE EQUIPMENT.

The system cabinet has been installed with rollers, for maneuverability when cleaning etc. However, if the system is to be moved a long distance (to another office building for example), we recommend you repack it in its original cartons, to avoid damage.

The Computer

Manufactured by Nabu Corporation

DIRECTORY

INTRODUCTION

Congratulations on the purchase of your new Nabu 1100 Computer; you have invested in a sophisticated and reliable microprocessing unit. This system uses the powerful Zilog Z-80A microprocessor chip, and is equipped with 2 double-sided, double-density floppy Disk Drives. It features 64K user memory capacity; 62K of which is designated as R/W memory, and 2K as R/O memory. Total storage capacity for the system, using floppy diskettes, is 2 Megabytes (1 Megabyte per Drive).

The system is equipped with two RS-232C Serial I/0 ports with programmable Baud Rate. These I/0 ports facilitate the use of both a console and a printer; or any two peripherals you may require. As well, a parallel output port is provided for the use of the optional Centronics dot matrix printer. Another feature of the system is the programmable timer, which can be used to implement a real time clock for the system.

The computer hardware is located in the upper drawer of the specially designed cabinet. Directly against the right side of the drawer as you open it are the Disk Drives, manufactured by Shugart. They feature low heat dissipation, improved access time, capacity for single or double density recording on standard diskettes, and write protection and programmable door lock for improved data security. The Shugart Disk Drive manual has been included for further information.

To the left of the Disk Drives is the card cage containing the printed circuit boards, which plug into a standard S-100 Bus. There have been some modifications to certain pin functions, and these are indicated in the S-100 Bus table included in the manual. Attached to the boards are the interconnecting cables used to interface between the various components of the system. The four printed circuit boards (CPU, Memory, Input/Output, and Floppy Controller) are described in detail in the manual, and complete circuit diagrams for each board have been included.

TABLE 1: IEEE S-100 BUS UTILIZATION

PIN #	SIGNAL NAME	IMPLEMENTATION
1	+8 Volts	Power supply
2	+16 Volts	Power supply
3	XRDY (S)	Not implemented
4	VIO*(S)	Not implemented
5	VI1*(S)	Not implemented
6	VI2*(S)	Not implemented
7	VI3*(S)	Not implemented
8	VI4*(S)	Not implemented
9	VI5*(S)	Not implemented
10	VI6*(S)	Not implemented
11	VI7*(S)	Not implemented
12	NMI*(S)	Implemented but not used
13	PWRFAIL*(B)	Not implemented
14	DMA3*(M)	Not implemented
15	A18 (M)	Not implemented
16	A16 (M)	Not implemented
17	A17 (M)	Not implemented
18	SDSB*(M)	Disables the 8 status signals
19	CDSB*(M)	Disables the 5 control output signals
20	GDN (B)	Ground (not implemented)
21	NDEF	Not to be defined
22	ADSB*(M)	Disables the 16 address signals
23	DODSB*(M)	Disables the 8 data output signals
24	ø (B)	Master timing signal
25	pSTVAL*(M)	Status valid strobe
26	pHLDA (M)	Hold control signal
†† 27	PWAIT	Indicates processor is in wait state
28	RFU	Reserved for future use
29	A5 (M)	Address bit 5
30	A4 (M)	Address bit 4
31	A3 (M)	Address bit 3
32	A15 (M)	Address bit 15
33	A12 (M)	Address bit 12
34	A9 (M)	Address bit 9
35	DO1 (M)	Data out bit 1
36	DO0 (M)	Data out bit 0
37	A10 (M)	Address bit 10
38	DO4 (M)	Data out bit 4
39	DO5 (M)	Data out bit 5
40	DO6 (M)	Data out bit 6
41	DI2 (S)	Data in bit 2
42	DI3 (S)	Data in bit 3
43	DI7 (S)	Data in bit 7
44	sM1 (M)	Op-code fetch status signal
45	sOUT (M)	Transfer status signal
46	sINP (M)	Transfer status signal
47	sMEMR (M)	Memory read status signal
48	sHLTA (M)	HLT acknowledge
49	CLOCK(B)	2 MHz (0.5%) 40-60% duty cycle
50	GND (B)	Ground

51	+8 Volts (B)	Power supply
52	-16 Volts (B)	Power supply
53	GND (B)	Ground (not implemented)
54	SLAVE CLR*(B)	Reset bus slaves
55	DMA0*(M)	Not implemented
56	DMA1*(M)	Not implemented
57	DMA2*(M)	Not implemented
58	sXTRQ*(M)	Not implemented
59	A19 (M)	Not implemented
60	SIXTN*(S)	Not implemented
61	A20 (M)	Not implemented
62	A21 (M)	Not implemented
63	A22 (M)	Not implemented
64	A23 (M)	Not implemented
†65	MREQ	Memory request
†66	MRFSH	Memory refresh
67	PHANTOM*(M/S)	Enables phantom slaves
68	MWRT (B)	Memory write
69	RFU	Reserved for future use
70	GND (B)	Ground (not implemented)
71	RFU	Reserved for future use
72	RDY (S)	Ready input
73	INT*(S)	Primary interrupt request
74	HOLD*(M)	HOLD control signal
75	RESET*(B)	Resets bus master devices
76	pSYNC (M)	Control signal identifying BSl
77	pWR*(M)	Data bus control signal
78	pDBIN (M)	Data in control signal
79	A0 (M)	Address bit 0
80	A1 (M)	Address bit 1
81	A2 (M)	Address bit 2
82	A6 (M)	Address bit 6
83	A7 (M)	Address bit 7
84	A8 (M)	Address bit 8
85	A13 (M)	Address bit 13
86	A14 (M)	Address bit 14
87	A11 (M)	Address bit 11
88	DO2 (M)	Data out bit 2
89	DO3 (M)	Data out bit 3
90	DO7 (M)	Data out bit 7
91	DI4 (S)	Data in bit 4
92	DI5 (S)	Data in bit 5
93	DI6 (S)	Data in bit 6
94	DI1 (S)	Data in bit 1
95	DI0 (S)	Data in bit 0
96	sINTA (M)	Interrupt status signal
97	sWO*(M)	Data out status signal
††98	FREQ	Status signal for 4 MHz clock
99	POC*(B)	Power-on clear signal
100	GND (B)	Ground

† These signals are not defined in the standard but are used in the system for the Z-80A microprocessor memory control signal.

†† These signals are non-standard

TABLE 2: BOARD POSITIONS IN CARD CAGE

1. Empty
2. FLOPPY DISK CONTROLLER BOARD
3. INPUT/OUTPUT BOARD
4. Empty
5. CPU BOARD
6. Empty
7. MEMORY BOARD
8. Empty

NOTE: Positions indicated are numbered from left to right as viewed from the front of the cabinet.

POWER SUPPLY

The S3 power supply (from Sunny International) is an open-frame module located behind the two drives in the top drawer of the Nabu system. It provides unregulated +8, +16, and -16 volts for the S-100 bus and regulated +5, -5 and +24 volts for the disk drives. It consists of four major components: transformer, rectifiers, filter capacitors, and regulators.

The transformer primary has two 110V windings. They are connected in parallel for use with a 110V supply, and in series for use with a 220V supply.

SPECIFICATIONS:

INPUT: 110 Volts AC, 60 Hz, single phase

OUTPUT: Unregulated: +8 Volts @ 14A, +16 Volts @ 3A, -16 Volts @ 3A

Regulated: +5 Volts @ 4A, -5 Volts @ 1A, +24 Volts @ 4A

1.0 CPU BOARD

GENERAL INFORMATION

The Nabu ACP-1101 CPU Board is designed to bring the full power of the Zilog Z-80A microprocessor to the S-100 bus. The CPU board has provision for up to three 2716 type EPROM's (for a total of 6K bytes), and two 2114 type static RAM's (for a total of 1K bytes). The base address of this memory block can be set using on-board jumpers. The board also performs an automatic jump to a user selected memory address on system start-up or reset. The clock frequency of the main processor is also selectable between 2 and 4 MHz. When the 4 MHz clock frequency is used, the board automatically inserts one wait state when the on-board EPROM or RAM is accessed.

When used in the Nabu 1100 computer system, the board operates at a 4 MHz clock rate, with one 2716 EPROM and two 2114 RAM's addressed from F800H to FFFFH.

SPECIFIC FEATURES

Clock Frequency Selection

The Nabu ACP-1101 may be clocked either at 4 MHz or 2 MHz. The operating frequency is selectable with Jumper 8 (JP-8). (Please refer to the board layout for the location of all jumpers). Connecting this jumper sets the operating clock frequency to 2 MHz. The standard CPU card is shipped with the jumper disconnected and runs reliably at 4 MHz.

Pin 98, labelled as FREQ, on the S-100 bus, is used by the Nabu system as an indicator line for the operating frequency. For 4 MHz operation the line will be high; for 2 MHz it is low.

Automatic Power-On Jump

When system power is turned on, or a reset signal is received, the CPU jumps to one of two hundred and fifty-six possible memory locations. The jump address is selected by the eight address jumpers JP-9 to JP-16. Only the eight most significant address bits (A15 - A8) are used to decode the jump address. The eight least significant address bits (A7 - A0) are taken as logic 0 as shown on the next page.

Power-On Jump Address: X X 0 0

A7 - A0, always at logic 0

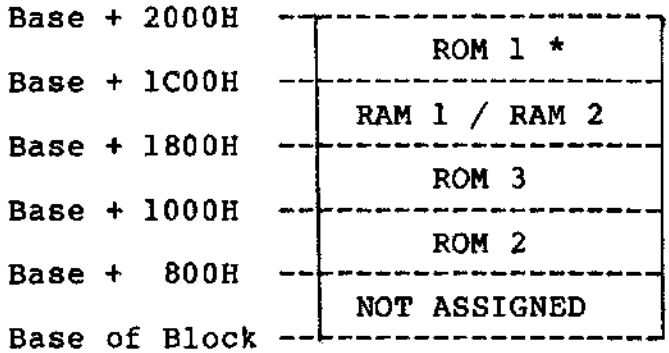
A15 - A8, selected by user

The standard Nabu CPU board has the power-on jump address set at FC00H (jumpers JP-15 and JP-16 installed).

On-Board Memory Selection

The Nabu CPU board offers a maximum of six kilo-bytes of on-board memory, which consists of three 2K x 8 (2716 type) EPROM's and two 1K x 4 (2114 type) static RAM's. IC sockets are provided on the board for the memory chips.

The memory address for the on-board EPROM's and RAM's are grouped as a block. Within the block, the individual memory chips are allocated as follows:



*Only the upper 1K of ROM 1 is used.

The RAM is configured as 1024 x 4 bits (2114 type). RAM 1 stores data bits D0, D7, D6, and D5; and RAM 2 stores data bits D4, D3, D2, and D1.

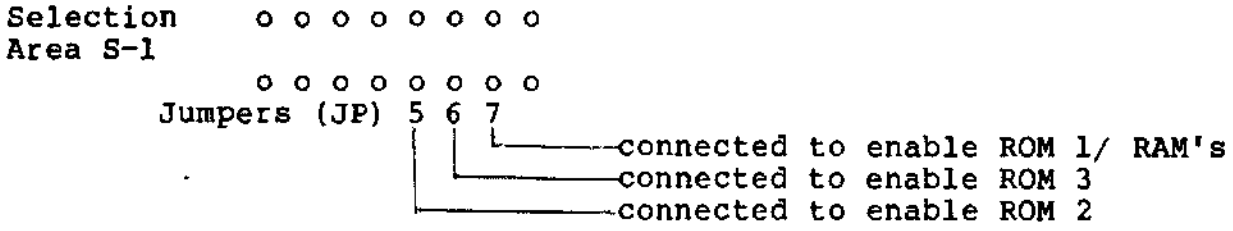
The base address of the block is set by jumpers JP-1 through JP-3. The three most-significant address bits are used to set the address of the block. Table 1 (on the following page), lists the possible base addressses of the block corresponding to each jumper connection.

JUMPERS (JP)			STARTING ADDRESS (IN HEX) OF:			
1	2	3	ROM 2	ROM 3	RAM 1/RAM 2	ROM 1
0	0	0	0800	1000	1800	1C00
0	0	1	2800	3000	3800	3C00
0	1	0	4800	5000	5800	5C00
0	1	1	6800	7000	7800	7C00
1	0	0	8800	9000	9800	9C00
1	0	1	A800	B000	B800	BC00
1	1	0	C800	D000	D800	DC00
1	1	1	E800	F000	F800	FC00

'1' represents 'Jumper is connected'
'0' represents 'Jumper is disconnected'

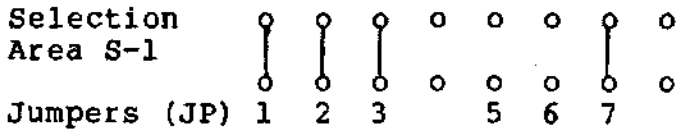
TABLE 1: Jumper Connection And Starting Address of Memory

The enabling of these memory chips is done by connecting jumpers JP-5, JP-6, and JP-7 in the selection area S-1. JP-5 enables ROM 2, JP-6 enables ROM 3, and JP-7 enables ROM 1 and RAM 1/ RAM 2, as seen in the figure below. (Note that ROM 1 and RAM 1/ RAM 2 are enabled together, and so both must be used together).

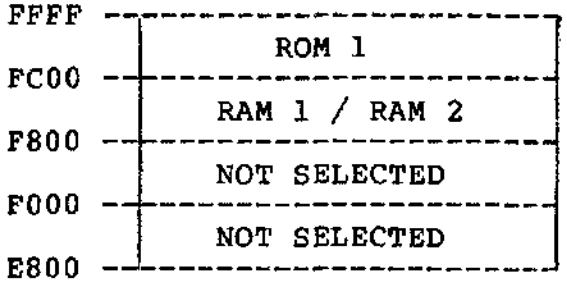


In addition, enabling on-board RAM's and EPROM's renders any external devices or memory at the selected address-block inaccessible to a read instruction. However, a write operation will write into all devices located there.

The standard Nabu ACP-1101 is shipped with the following memory setting:



The memory map corresponding to the standard setting would be:



When both the 4 MHz operating frequency, and the on-board EPROM's and RAM's are chosen, (as in the standard Nabu ACP-1101 setting), one wait-cycle is automatically inserted by the CPU logic circuitry.

Refresh Enable

Dynamic RAM's periodically require a refresh to maintain the data stored within the memory cell. The Nabu CPU board brings the memory-refresh signal from the Zilog Z-80A microprocessor to the S-100 bus. Pin 66 on the S-100 bus is designated by Nabu as the memory-refresh signal, RFSH. The memory request signal from the Z-80A processor is also brought out to the S-100 bus. Pin 65 (named as MREQ), is used to indicate a valid memory address on the address bus.

NABU ACP-1101 CPU BOARD
PARTS LIST

Integrated Circuits

U1-U4	2114	1024 x 4-bit NMOS static RAM
U5	74LS136	Quadruple 2-input NOR with open-collector outputs
U6	74LS42	4-line-to-10-line decoder
U7	74LS20	Dual 4-input NAND
U8, U9, U28, U30-U34	74LS241	Octal buffer/line-driver with 3-state outputs
U10	74LS175	Quadruple D-type flip-flop
U11	74LS123	Dual retriggerable monostable multivibrator with clear
U12, U17, U20, U23, U24	74LS74	Dual D-type rising-edge-triggered flip-flop with preset and clear
U13	74LS132	Quadruple 2-input NAND with Schmitt-triggered inputs
U14, U21	74LS04	Hex inverter
U15	74LS08	Quadruple 2-input AND
U16	74LS32	Quadruple 2-input OR
U18	Z-80A-CPU	Central processing unit (4 MHz)
U19	74LS157	Quadruple 2-line-to-1-line multiplexer
U22, U25, U35	74LS02	Quadruple 2-input NOR
U26	74LS367	Hex non-inverting bus-driver
U27	74LS14	Hex inverter with Schmitt-triggered inputs
U29, U36	74LS368	Hex inverting bus-driver
U37, U38	7805	5 V positive voltage regulator
ROM1-ROM3	2716	2716 EPROM with bootstrap program

Transistors:

Q1	2N4124	NPN silicon transistor
Q2	2N4126	PNP silicon transistor

Diodes:

D1, D2	1N914A	Silicon switching diode

Capacitors:

C1-C10, C13-C15, C19-C24, C25, C26, C30, C31	0.1 µF
C11, C18	33 pF disc
C12	22 µF, 16 V tantalum electrolytic
C16, C27-C29	10 µF, 16 V tantalum electrolytic
C17	10 nF

Resistors:

R1, R2	10 k Ω
R3, R5-R7, R11	1 k Ω
R4	100 Ω
R8	220 Ω
R9	22 Ω
R10	100 k Ω
RN1-RN3	9-resistor pack of 1 kΩ resistors with common pin #1

Crystal:

XTAL	8.000 MHz parallel-resonant

Quantity	Description
16	14 pin socket
7	16 pin socket
4	18 pin socket
8	20 pin socket
3	24 pin socket
1	40 pin socket
1	Delta 680-0.5-220 Heatsink
6	#6-32 x 3/8" machine screw
6	#6-32 nuts
1	p.c. board

Z8400
Z80® CPU Central Processing Unit

Zilog

Product Specification

March 1981

Features

- The instruction set contains 158 instructions. The 78 instructions of the 8080A are included as a subset; 8080A software compatibility is maintained.
- Six MHz, 4 MHz and 2.5 MHz clocks for the Z80B, Z80A, and Z80 CPU result in rapid instruction execution with consequent high data throughput.
- The extensive instruction set includes string, bit, byte, and word operations. Block searches and block transfers together with indexed and relative addressing result in the most powerful data handling capabilities in the microcomputer industry.
- The Z80 microprocessors and associated family of peripheral controllers are linked by a vectored interrupt system. This system may be daisy-chained to allow implementation of a priority interrupt scheme. Little, if any, additional logic is required for daisy-chaining.
- Duplicate sets of both general-purpose and flag registers are provided, easing the design and operation of system software through single-context switching, background-foreground programming, and single-level interrupt processing. In addition, two 16-bit index registers facilitate program processing of tables and arrays.
- There are three modes of high speed interrupt processing: 8080 compatible, non-Z80 peripheral device, and Z80 Family peripheral with or without daisy chain.
- On-chip dynamic memory refresh counter.

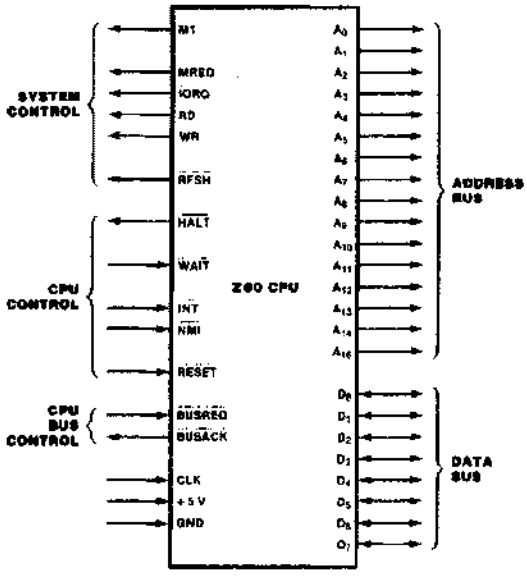


Figure 1. Pin Functions

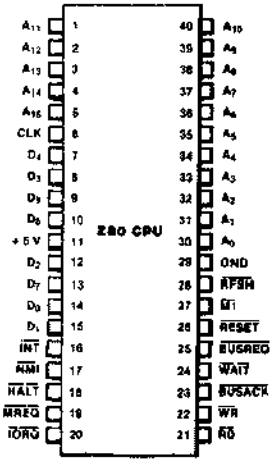


Figure 2. Pin Assignments

General Description

The Z80, Z80A, and Z80B CPUs are third-generation single-chip microprocessors with exceptional computational power. They offer higher system throughput and more efficient memory utilization than comparable second- and third-generation microprocessors. The internal registers contain 208 bits of read/write memory that are accessible to the programmer. These registers include two sets of six general-purpose registers which may be used individually as either 8-bit registers or as 16-bit register pairs. In addition, there are two sets of accumulator and flag registers. A group of "Exchange" instructions makes either set of main or alternate registers accessible to the programmer. The alternate set allows operation in foreground-background mode or it may be reserved for very fast interrupt response.

The Z80 also contains a Stack Pointer, Program Counter, two index registers, a Refresh register (counter), and an Interrupt register. The CPU is easy to incorporate into a system since it requires only a single +5 V power source, all output signals are fully decoded and timed to control standard memory or peripheral circuits, and is supported by an extensive family of peripheral controllers. The internal block diagram (Figure 3) shows the primary functions of the Z80 processors. Subsequent text provides more detail on the Z80 I/O controller family, registers, instruction set, interrupts and daisy chaining, and CPU timing.

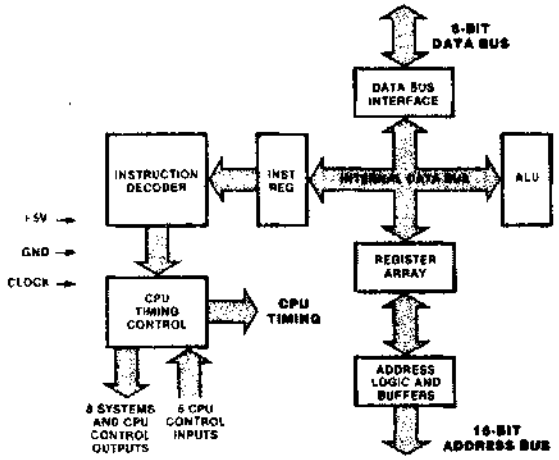


Figure 3. Z80 CPU Block Diagram

Z80 Microprocessor Family

The Zilog Z80 microprocessor is the central element of a comprehensive microprocessor product family. This family works together in most applications with minimum requirements for additional logic, facilitating the design of efficient and cost-effective microcomputer-based systems.

Zilog has designed five components to provide extensive support for the Z80 microprocessor. These are:

- The PIO (Parallel Input/Output) operates in both data-byte I/O transfer mode (with handshaking) and in bit mode (without handshaking). The PIO may be configured to interface with standard parallel peripheral devices such as printers, tape punches, and keyboards.
- The CTC (Counter/Timer Circuit) features four programmable 8-bit counter/timers, each of which has an 8-bit prescaler. Each of the four channels may be configured to operate in either counter or timer mode.
- The DMA (Direct Memory Access) controller provides dual port data transfer operations and the ability to terminate data transfer as a result of a pattern match.
- The SIO (Serial Input/Output) controller offers two channels. It is capable of operating in a variety of programmable modes for both synchronous and asynchronous communication, including Bi-Synch and SDLC.
- The DART (Dual Asynchronous Receiver/Transmitter) device provides low cost asynchronous serial communication. It has two channels and a full modem control interface.

Z80 CPU Registers

Figure 4 shows three groups of registers within the Z80 CPU. The first group consists of duplicate sets of 8-bit registers: a principal set and an alternate set (designated by ' [prime], e.g., A'). Both sets consist of the Accumulator Register, the Flag Register, and six general-purpose registers. Transfer of data between these duplicate sets of registers is accomplished by use of "Exchange" instructions. The result is faster response to interrupts and easy, efficient implementation of such versatile programming techniques as background-foreground data processing. The second set of registers consists of six registers with assigned functions. These are the I (Interrupt Register), the R (Refresh Register), the IX and IY (Index Registers), the SP (Stack Pointer), and the PC (Program Counter). The third group consists of two interrupt status flip-flops, plus an additional pair of flip-flops which assists in identifying the interrupt mode at any particular time. Table 1 provides further information on these registers.

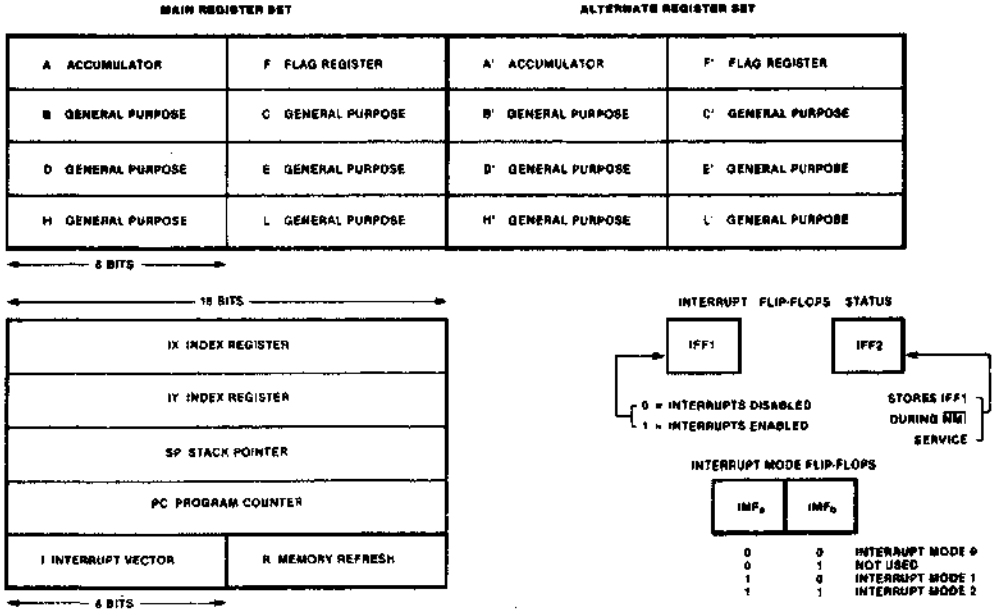


Figure 4. CPU Registers

Z80 CPU Registers (Continued)

Register		Size (Bits)	Remarks
A, A'	Accumulator	8	Stores an operand or the results of an operation.
F, F'	Flags	8	See Instruction Set.
B, B'	General Purpose	8	Can be used separately or as a 16-bit register with C.
C, C'	General Purpose	8	See B, above.
D D'	General Purpose	8	Can be used separately or as a 16-bit register with E.
E, E'	General Purpose	8	See D, above.
H, H'	General Purpose	8	Can be used separately or as a 16-bit register with L.
L, L'	General Purpose	8	See H above.
			Note: The (B,C), (D,E), and (H,L) sets are combined as follows: B — High byte C — Low byte D — High byte E — Low byte H — High byte L — Low byte
I	Interrupt Register	8	Stores upper eight bits of memory address for vectored interrupt processing.
R	Refresh Register	8	Provides user-transparent dynamic memory refresh. Automatically incremented and placed on the address bus during each instruction fetch cycle.
IX	Index Register	16	Used for indexed addressing.
IY	Index Register	16	Same as IX, above.
SP	Stack Pointer	16	Stores addresses or data temporarily. See Push or Pop in instruction set.
PC	Program Counter	16	Holds address of next instruction.
IFF_1-IFF_2	Interrupt Enable	Flip Flops	Set or reset to indicate interrupt status (see Figure 4).
IMFa-IMFb	Interrupt Mode	Flip-Flops	Reflect Interrupt mode (see Figure 4).

Table 1. Z80 CPU Registers

Interrupts: General Operation

The CPU accepts two interrupt input signals: $\overline{NMI}$ and $\overline{INT}$. The $\overline{NMI}$ is a non-maskable interrupt and has the highest priority. $\overline{INT}$ is a lower priority interrupt since it requires that interrupts be enabled in software in order to operate. Either $\overline{NMI}$ or $\overline{INT}$ can be connected to multiple peripheral devices in a wired-OR configuration.

The Z80 has a single response mode for interrupt service for the non-maskable interrupt. The maskable interrupt, $\overline{INT}$, has three programmable response modes available. These are:

- Mode 0 — compatible with the 8080 microprocessor.
- Mode 1 — Peripheral Interrupt service, for use with non-8080/Z80 systems.
- Mode 2 — a vectored interrupt scheme, usually daisy-chained, for use with Z80 Family and compatible peripheral devices.

The CPU services interrupts by sampling the $\overline{NMI}$ and $\overline{INT}$ signals at the rising edge of the last clock of an instruction. Further interrupt service processing depends upon the type of interrupt that was detected. Details on interrupt responses are shown in the CPU Timing Section.

Interrupts: General Operation (Continued)

Non-Maskable Interrupt ($\overline{NMI}$). The non-maskable interrupt cannot be disabled by program control and therefore will be accepted at at all times by the CPU. $\overline{NMI}$ is usually reserved for servicing only the highest priority type interrupts, such as that for orderly shutdown after power failure has been detected. After recognition of the $\overline{NMI}$ signal (providing $\overline{BUSREQ}$ is not active), the CPU jumps to restart location 0066H. Normally, software starting at this address contains the interrupt service routine.

Maskable Interrupt ($\overline{INT}$). Regardless of the interrupt mode set by the user, the Z80 response to a maskable interrupt input follows a common timing cycle. After the interrupt has been detected by the CPU (provided that interrupts are enabled and $\overline{BUSREQ}$ is not active) a special interrupt processing cycle begins. This is a special fetch ($\overline{M1}$) cycle in which $\overline{IORQ}$ becomes active rather than $\overline{MREQ}$, as in a normal $\overline{M1}$ cycle. In addition, this special $\overline{M1}$ cycle is automatically extended by two $\overline{WAIT}$ states, to allow for the time required to acknowledge the interrupt request and to place the interrupt vector on the bus.

Mode 0 Interrupt Operation. This mode is compatible with the 8080 microprocessor interrupt service procedures. The interrupting device places an instruction on the data bus, which is then acted on six times by the CPU. This is normally a Restart Instruction, which will initiate an unconditional jump to the selected one of eight restart locations in page zero of memory.

Mode 1 Interrupt Operation. Mode 1 operation is very similar to that for the $\overline{NMI}$. The principal difference is that the Mode 1 interrupt has a vector address of 0038H only.

Mode 2 Interrupt Operation. This interrupt mode has been designed to utilize most effectively the capabilities of the Z80 microprocessor and its associated peripheral family. The interrupting peripheral device selects the starting address of the interrupt service routine. It does this by placing an 8-bit address vector on the data bus during the interrupt acknowledge cycle. The high-order byte of the interrupt service routine address is supplied by the I (Interrupt) register. This flexibility in selecting the interrupt service routine address allows the peripheral device to use several different types of service routines. These routines may be located at any available location in memory. Since the interrupting device supplies the low-order byte of the 2-byte vector, bit 0 (A_0) must be a zero.

Interrupt Priority (Daisy Chaining and Nested Interrupts). The interrupt priority of each peripheral device is determined by its physical location within a daisy-chain configuration. Each device in the chain has an interrupt enable input line (IEI) and an interrupt enable output line (IEO), which is fed to the next lower priority device. The first device in the daisy chain has its IEI input hardwared to a High level. The first device has highest priority, while each succeeding device has a corresponding lower priority. This arrangement permits the CPU to select the highest priority interrupt from several simultaneously interrupting peripherals.

The interrupting device disables its IEO line to the next lower priority peripheral until it has been serviced. After servicing, its IEO line is raised, allowing lower priority peripherals to demand interrupt servicing.

The Z80 CPU will nest (queue) any pending interrupts or interrupts received while a selected peripheral is being serviced.

Interrupt Enable/Disable Operation. Two flip-flops, IFF_1 and IFF_2, referred to in the register description are used to signal the CPU interrupt status. Operation of the two flip-flops is described in Table 2. For more details, refer to the *Z80 CPU Technical Manual* and *Z80 Assembly Language Manual.*

Action	IFF_1	IFF_2	Comments
CPU Reset	0	0	Maskable interrupt $\overline{INT}$ disabled
DI instruction execution	0	0	Maskable interrupt $\overline{INT}$ disabled
EI instruction execution	1	1	Maskable interrupt $\overline{INT}$ enabled
LD A,I instruction execution	*	*	IFF_2 → Parity flag
LD A,R instruction execution	*	*	IFF_2 → Parity flag
Accept $\overline{NMI}$	0	IFF_1	IFF_1 → IFF_2 (Maskable interrupt $\overline{INT}$ disabled)
RETN instruction execution	IFF_2	*	IFF_2 → IFF_1 at completion of an $\overline{NMI}$ service routine.

Table 2. State of Flip-Flops

Instruction Set

The Z80 microprocessor has one of the most powerful and versatile instruction sets available in any 8-bit microprocessor. It includes such unique operations as a block move for fast, efficient data transfers within memory or between memory and I/O. It also allows operations on any bit in any location in memory.

The following is a summary of the Z80 instruction set and shows the assembly language mnemonic, the operation, the flag status, and gives comments on each instruction. The *Z80 CPU Technical Manual* (03-0029-01) and *Assembly Language Programming Manual* (03-0002-01) contain significantly more details for programming use.

The instructions are divided into the following categories:

- 8-bit loads
- 16-bit loads
- Exchanges, block transfers, and searches
- 8-bit arithmetic and logic operations
- General-purpose arithmetic and CPU control
- 16-bit arithmetic operations
- Rotates and shifts
- Bit set, reset, and test operations
- Jumps
- Calls, returns, and restarts
- Input and output operations

A variety of addressing modes are implemented to permit efficient and fast data transfer between various registers, memory locations, and input/output devices. These addressing modes include:

- Immediate
- Immediate extended
- Modified page zero
- Relative
- Extended
- Indexed
- Register
- Register indirect
- Implied
- Bit

8-Bit Load Group

Mnemonic	Symbolic Operation	Flags S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD r, r'	r ← r'	•	•	X	•	X	•	•	•	01 r r'		1	1	4	r, r' Reg.
LD r, n	r ← n	•	•	X	•	X	•	•	•	00 r 110		2	2	7	000 B
										← n →					001 C
LD r, (HL)	r ← (HL)	•	•	X	•	X	•	•	•	01 r 110		1	2	7	010 D
LD r, (IX + d)	r ← (IX + d)	•	•	X	•	X	•	•	•	11 011 101	DD	3	5	19	011 E
										01 r 101					100 H
										← d →					101 L
LD r, (IY + d)	r ← (IY + d)	•	•	X	•	X	•	•	•	11 111 101	FD	3	5	19	111 A
										01 r 110					
										← d →					
LD (HL), r	(HL) ← r	•	•	X	•	X	•	•	•	01 110 r		1	2	7	
LD (IX + d), r	(IX + d) ← r	•	•	X	•	X	•	•	•	11 011 101	DD	3	5	19	
										01 110 r					
										← d →					
LD (IY + d), r	(IY + d) ← r	•	•	X	•	X	•	•	•	11 111 101	FD	3	5	19	
										01 110 r					
										← d →					
LD (HL), n	(HL) ← n	•	•	X	•	X	•	•	•	00 110 110	36	2	3	10	
										← n →					
LD (IX + d), n	(IX + d) ← n	•	•	X	•	X	•	•	•	11 011 101	DD	4	5	19	
										00 110 110	36				
										← d →					
										← n →					
LD (IY + d), n	(IY + d) ← n	•	•	X	•	X	•	•	•	11 111 101	FD	4	5	19	
										00 110 110	36				
										← d →					
										← n →					
LD A, (BC)	A ← (BC)	•	•	X	•	X	•	•	•	00 001 010	0A	1	2	7	
LD A, (DE)	A ← (DE)	•	•	X	•	X	•	•	•	00 011 010	1A	1	2	7	
LD A, (nn)	A ← (nn)	•	•	X	•	X	•	•	•	00 111 010	3A	3	4	13	
										← p →					
										← n →					
LD (BC), A	(BC) ← A	•	•	X	•	X	•	•	•	00 000 010	02	1	2	7	
LD (DE), A	(DE) ← A	•	•	X	•	X	•	•	•	00 010 010	12	1	2	7	
LD (nn), A	(nn) ← A	•	•	X	•	X	•	•	•	00 110 010	32	3	4	13	
										← n →					
										← p →					
LD A, I	A ← I	↕	↕	X	0	X	IFF	0	•	11 101 101	ED	2	2	9	
										01 010 111	57				
LD A, R	A ← R	↕	↕	X	0	X	IFF	0	•	11 101 101	ED	2	2	9	
										01 011 111	5F				
LD I, A	I ← A	•	•	X	•	X	•	•	•	11 101 101	ED	2	2	9	
										01 000 111	47				
LD R, A	R ← A	•	•	X	•	X	•	•	•	11 101 101	ED	2	2	9	
										01 001 111	4F				

NOTES: r, r' means any of the registers A, B, C, D, E, H, L.
IFF the contents of the interrupt enable flip-flop (IFF) is copied into the P/V flag.
For an explanation of flag notation and symbols for mnemonic tables, see Symbolic Notation section following tables.

16-Bit Load Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LD dd, nn	dd ← nn	•	•	X	•	X	•	•	•	00 dd0 001 ← n → ← n →	3	3	10	dd: 00 BC, 01 DE, 10 HL, 11 SP
LD IX, nn	IX ← nn	•	•	X	•	X	•	•	•	11 011 101 DD 00 100 001 21 ← n → ← n →	4	4	14	
LD IY, nn	IY ← nn	•	•	X	•	X	•	•	•	11 111 101 FD 00 100 001 21 ← n → ← n →	4	4	14	
LD HL, (nn)	H ← (nn + 1) L ← (nn)	•	•	X	•	X	•	•	•	00 101 010 2A ← n → ← n →	3	5	16	
LD dd, (nn)	dd_H ← (nn + 1) dd_L ← (nn)	•	•	X	•	X	•	•	•	11 101 101 ED 01 ddl 011 ← n → ← n →	4	6	20	
LD IX, (nn)	IX_H ← (nn + 1) IX_L ← (nn)	•	•	X	•	X	•	•	•	11 011 101 DD 00 101 010 2A ← n → ← n →	4	6	20	
LD IY, (nn)	IY_H ← (nn + 1) IY_L ← (nn)	•	•	X	•	X	•	•	•	11 111 101 FD 00 101 010 2A ← n → ← n →	4	6	20	
LD (nn), HL	(nn + 1) ← H (nn) ← L	•	•	X	•	X	•	•	•	00 100 010 22 ← n → ← n →	3	5	16	
LD (nn), dd	(nn + 1) ← dd_H (nn) ← dd_L	•	•	X	•	X	•	•	•	11 101 101 ED 01 dd0 011 ← n → ← n →	4	6	20	
LD (nn), IX	(nn + 1) ← IX_H (nn) ← IX_L	•	•	X	•	X	•	•	•	11 011 101 DD 00 100 010 22 ← n → ← n →	4	6	20	
LD (nn), IY	(nn + 1) ← IY_H (nn) ← IY_L	•	•	X	•	X	•	•	•	11 111 101 FD 00 100 010 22 ← n → ← n →	4	6	20	
LD SP, HL	SP ← HL	•	•	X	•	X	•	•	•	11 111 001 F9	1	1	6	
LD SP, IX	SP ← IX	•	•	X	•	X	•	•	•	11 011 101 DD 11 111 001 F9	2	2	10	
LD SP, IY	SP ← IY	•	•	X	•	X	•	•	•	11 111 101 FD 11 111 001 F9	2	2	10	
PUSH qq	(SP - 2) ← qq_L (SP - 1) ← qq_H SP ← SP - 2	•	•	X	•	X	•	•	•	11 qq0 101	1	3	11	qq: 00 BC, 01 DE, 10 HL, 11 AF
PUSH IX	(SP - 2) ← IX_L (SP - 1) ← IX_H SP ← SP - 2	•	•	X	•	X	•	•	•	11 011 101 DD 11 100 101 E5	2	4	15	
PUSH IY	(SP - 2) ← IY_L (SP - 1) ← IY_H SP ← SP - 2	•	•	X	•	X	•	•	•	11 111 101 FD 11 100 101 E5	2	4	15	
POP qq	qq_H ← (SP + 1) qq_L ← (SP) SP ← SP + 2	•	•	X	•	X	•	•	•	11 qq0 001	1	3	10	
POP IX	IX_H ← (SP + 1) IX_L ← (SP) SP ← SP + 2	•	•	X	•	X	•	•	•	11 011 101 DD 11 100 001 E1	2	4	14	
POP IY	IY_H ← (SP + 1) IY_L ← (SP) SP ← SP + 2	•	•	X	•	X	•	•	•	11 111 101 FD 11 100 001 E1	2	4	14	

NOTES: dd is any of the register pairs BC, DE, HL, SP.
qq is any of the register pairs AF, BC, DE, HL.
$(PAIR)_H$, $(PAIR)_L$ refer to high order and low order eight bits of the register pair respectively.
e.g., BC_L = C, AF_H = A.

Exchange, Block Transfer, Block Search Groups

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
EX DE, HL	DE ↔ HL	•	•	X	•	X	•	•	•	11 101 011 EB	1	1	4	
EX AF, AF'	AF ↔ AF'	•	•	X	•	X	•	•	•	00 001 000 08	1	1	4	
EXX	BC ↔ BC' DE ↔ DE' HL ↔ HL'	•	•	X	•	X	•	•	•	11 011 001 D9	1	1	4	Register bank and auxiliary register bank exchange
EX (SP), HL	H ↔ (SP + 1) L ↔ (SP)	•	•	X	•	X	•	•	•	11 100 011 E3	1	5	19	
EX (SP), IX	IX_H ↔ (SP + 1) IX_L ↔ (SP)	•	•	X	•	X	•	•	•	11 011 101 DD 11 100 011 E3	2	6	23	
EX (SP), IY	IY_H ↔ (SP + 1) IY_L ↔ (SP)	•	•	X	•	X	•	•	•	11 111 101 FD 11 100 011 E3	2	6	23	
LDI	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC - 1	•	•	X	①	X	0	0	•	11 101 101 ED 10 100 000 A0	2	4	16	Load (HL) into (DE), increment the pointers and decrement the byte counter (BC)
LDIR	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC - 1 Repeat until BC = 0	•	•	X	0	X	0	0	•	11 101 101 ED 10 110 000 B0	2 2	5 4	21 16	If BC ≠ 0 If BC = 0

NOTE: ① P/V flag is 0 if the result of BC - 1 = 0, otherwise P/V = 1.

Exchange, Block Transfer, Block Search Groups (Continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
LDD	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1	•	•	X 0 X	①	0	•	11 101 101 ED 10 101 000 A8	2	4	16	
LDDR	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1 Repeat until BC = 0	•	•	X 0 X	0	0	•	11 101 101 ED 10 111 000 B8	2 2	5 4	21 16	If BC ≠ 0 If BC = 0
CPI	A − (HL) HL ← HL + 1 BC ← BC − 1	↕	② ↕	X ↕ X	① ↕	1	•	11 101 101 ED 10 100 001 A1	2	4	16	
CPIR	A − (HL) HL ← HL + 1 BC ← BC − 1 Repeat until A = (HL) or BC = 0	↕	② ↕	X ↕ X	① ↕	1	•	11 101 101 ED 10 110 001 B1	2 2	5 4	21 16	If BC ≠ 0 and A ≠ (HL) If BC = 0 or A = (HL)
CPD	A − (HL) HL ← HL − 1 BC ← BC − 1	↕	② ↕	X ↕ X	① ↕	1	•	11 101 101 ED 10 101 001 A9	2	4	16	
CPDR	A − (HL) HL ← HL − 1 BC ← BC − 1 Repeat until A = (HL) or BC = 0	↕	② ↕	X ↕ X	① ↕	1	•	11 101 101 ED 10 111 001 B9	2 2	5 4	21 16	If BC ≠ 0 and A ≠ (HL) If BC = 0 or A = (HL)

NOTES: ① P/V flag is 0 if the result of BC − 1 = 0, otherwise P/V = 1
② Z flag is 1 if A = (HL), otherwise Z = 0

8-Bit Arithmetic and Logical Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
ADD A, r	A ← A + r	↕	↕	X ↕ X	V	0	↕	10 000 r	1	1	4	r Reg. 000 B 001 C 010 D 011 E 100 H 101 L 111 A
ADD A, n	A ← A + n	↕	↕	X ↕ X	V	0	↕	11 000 110 ← n →	2	2	7	
ADD A, (HL)	A ← A + (HL)	↕	↕	X ↕ X	V	0	↕	10 000 110	1	2	7	
ADD A, (IX + d)	A ← A + (IX + d)	↕	↕	X ↕ X	V	0	↕	11 011 101 DD 10 000 110 ← d →	3	5	19	
ADD A, (IY + d)	A ← A + (IY + d)	↕	↕	X ↕ X	V	0	↕	11 111 101 FD 10 000 110 ← d →	3	5	19	
ADC A, s	A ← A + s + CY	↕	↕	X ↕ X	V	0	↕	001				s is any of r, n, (HL), (IX + d), (IY + d) as shown for ADD instruction. The indicated bits replace the 000 in the ADD set above.
SUB s	A ← A − s	↕	↕	X ↕ X	V	1	↕	010				
SBC A, s	A ← A − s − CY	↕	↕	X ↕ X	V	1	↕	011				
AND s	A ← A ∧ s	↕	↕	X 1 X	P	0	0	100				
OR s	A ← A ∨ s	↕	↕	X 0 X	P	0	0	110				
XOR s	A ← A ⊕ s	↕	↕	X 0 X	P	0	0	101				
CP s	A − s	↕	↕	X ↕ X	V	1	↕	111				
INC r	r ← r + 1	↕	↕	X ↕ X	V	0	•	00 r 100	1	1	4	
INC (HL)	(HL) ← (HL) + 1	↕	↕	X ↕ X	V	0	•	00 110 100	1	3	11	
INC (IX + d)	(IX + d) ← (IX + d) + 1	↕	↕	X ↕ X	V	0	•	11 011 101 DD 00 110 100 ← d →	3	6	23	
INC (IY + d)	(IY + d) ← (IY + d) + 1	↕	↕	X ↕ X	V	0	•	11 111 101 FD 00 110 100 ← d →	3	6	23	
DEC m	m ← m − 1	↕	↕	X ↕ X	V	1	•	101				m is any of r, (HL), (IX + d), (IY + d) as shown for INC. DEC same format and states as INC. Replace 100 with 101 in opcode

General-Purpose Arithmetic and CPU Control Groups

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
DAA	Converts acc. content into packed BCD following add or subtract with packed BCD operands.	↕	↕	X	↕	X	P	•	↕	00 100 111	27	1	1	4	Decimal adjust accumulator.
CPL	$A \leftarrow \bar{A}$	•	•	X	1	X	•	1	•	00 101 111	2F	1	1	4	Complement accumulator (one's complement).
NEG	$A \leftarrow 0 - A$	↕	↕	X	↕	X	V	1	↕	11 101 101 01 000 100	ED 44	2	2	8	Negate acc. (two's complement)
CCF	$CY \leftarrow \overline{CY}$	•	•	X	X	X	•	0	↕	00 111 111	3F	1	1	4	Complement carry flag.
SCF	$CY \leftarrow 1$	•	•	X	0	X	•	0	1	00 110 111	37	1	1	4	Set carry flag.
NOP	No operation	•	•	X	•	X	•	•	•	00 000 000	00	1	1	4	
HALT	CPU halted	•	•	X	•	X	•	•	•	01 110 110	76	1	1	4	
DI *	IFF ← 0	•	•	X	•	X	•	•	•	11 110 011	F3	1	1	4	
EI *	IFF ← 1	•	•	X	•	X	•	•	•	11 111 011	FB	1	1	4	
IM 0	Set interrupt mode 0	•	•	X	•	X	•	•	•	11 101 101 01 000 110	ED 46	2	2	8	
IM 1	Set interrupt mode 1	•	•	X	•	X	•	•	•	11 101 101 01 010 110	ED 56	2	2	8	
IM 2	Set interrupt mode 2	•	•	X	•	X	•	•	•	11 101 101 01 011 110	ED 5E	2	2	8	

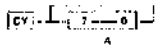
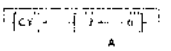
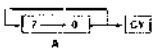
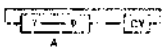
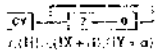
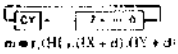
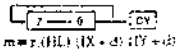
NOTES: IFF indicates the interrupt enable flip-flop
CY indicates the carry flip-flop
* indicates interrupts are not sampled at the end of EI or DI

16-Bit Arithmetic Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
ADD HL, ss	$HL \leftarrow HL + ss$	•	•	X	X	X	•	0	1	00 ss1 001		1	3	11	ss Reg. 00 BC 01 DE 10 HL 11 SP
ADC HL, ss	$HL \leftarrow HL + ss + CY$	↕	↕	X	X	X	V	0	1	11 101 101 01 ss1 010	ED 4A	2	4	15	
SBC HL, ss	$HL \leftarrow HL - ss - CY$	↕	↕	X	X	X	V	1	1	11 101 101 01 ss0 010	ED 42	2	4	15	
ADD IX, pp	$IX \leftarrow IX + pp$	•	•	X	X	X	•	0	1	11 011 101 00 pp1 001	DD 09	2	4	15	pp Reg. 00 BC 01 DE 10 IX 11 SP
ADD IY, rr	$IY \leftarrow IY + rr$	•	•	X	X	X	•	0	1	11 111 101 00 rr1 001	FD 09	2	4	15	rr Reg. 00 BC 01 DE 10 IY 11 SP
INC ss	$ss \leftarrow ss + 1$	•	•	X	•	X	•	•	•	00 ss0 011		1	1	6	
INC IX	$IX \leftarrow IX + 1$	•	•	X	•	X	•	•	•	11 011 101 00 100 011	DD 23	2	2	10	
INC IY	$IY \leftarrow IY + 1$	•	•	X	•	X	•	•	•	11 111 101 00 100 011	FD 23	2	2	10	
DEC ss	$ss \leftarrow ss - 1$	•	•	X	•	X	•	•	•	00 ss1 011		1	1	6	
DEC IX	$IX \leftarrow IX - 1$	•	•	X	•	X	•	•	•	11 011 101 00 101 011	DD 2B	2	2	10	
DEC IY	$IY \leftarrow IY - 1$	•	•	X	•	X	•	•	•	11 111 101 00 101 011	FD 2B	2	2	10	

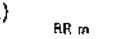
NOTES: ss is any of the register pairs BC, DE, HL, SP
pp is any of the register pairs BC, DE, IX, SP
rr is any of the register pairs BC, DE, IY, SP

Rotate and Shift Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
RLCA		•	•	X	0	X	•	0	↕	00 000 111	07	1	1	4	Rotate left circular accumulator
RLA		•	•	X	0	X	•	0	↕	00 010 111	17	1	1	4	Rotate left accumulator.
RRCA		•	•	X	0	X	•	0	↕	00 001 111	0F	1	1	4	Rotate right circular accumulator.
RRA		•	•	X	0	X	•	0	↕	00 011 111	1F	1	1	4	Rotate right accumulator.
RLC r		↕	↕	X	0	X	P	0	↕	11 001 011 00 000 r	CB	2	2	8	Rotate left circular register r.
RLC (HL)		↕	↕	X	0	X	P	0	↕	11 001 011 00 000 110	CB 06	2	4	15	r Reg. 000 B 001 C 010 D 011 E 100 H 101 L 111 A
RLC (IX + d)		↕	↕	X	0	X	P	0	↕	11 011 101 11 001 011 — d — 00 000 110	DD CB 06	4	6	23	
RLC (IY + d)		↕	↕	X	0	X	P	0	↕	11 111 101 11 001 011 — d — 00 000 110	FD CB 06	4	6	23	
RL m		↕	↕	X	0	X	P	0	↕	010					Instruction format and states are as shown for RLC's. To form new opcode replace 000 of RLC's with shown code.
RRC m		↕	↕	X	0	X	P	0	↕	001					

m = r, (HL), (IX + d), (IY + d)

Rotate and Shift Group (Continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
RR m	 m ≡ r, (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	CB 00 011 r		2	2	8	
SLA m	m ≡ r, (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	CB 00 100 r		2	2	8	
SRA m	m ≡ r, (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	CB 00 101 r		2	2	8	
SRL m	m ≡ r, (HL), (IX + d), (IY + d)	↕	↕	X	0	X	P	0	↕	CB 00 111 r		2	2	8	
RLD		↕	↕	X	0	X	P	0	•	ED 01 101 111	ED 6F	2	5	18	Rotate digit left and right between the accumulator and location (HL). The contents of the upper half of the accumulator is unaffected.
RRD		↕	↕	X	0	X	P	0	•	ED 01 100 111	ED 67	2	5	18	The contents of the upper half of the accumulator is unaffected.

Bit Set, Reset and Test Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
BIT b, r	Z ← $\overline{r_b}$	X	↕	X	↕	X	X	0	•	CB 01 b r		2	2	8	r: 000 B, 001 C, 010 D, 011 E, 100 H, 101 L, 111 A. b: 000 0, 001 1, 010 2, 011 3, 100 4, 101 5, 110 6, 111 7
BIT b, (HL)	Z ← $\overline{(HL)_b}$	X	↕	X	↕	X	X	0	•	CB 01 b 110		2	3	12	
BIT b, (IX + d)	Z ← $\overline{(IX+d)_b}$	X	↕	X	↕	X	X	0	•	DD CB d 01 b 110		4	5	20	
BIT b, (IY + d)	Z ← $\overline{(IY+d)_b}$	X	↕	X	↕	X	X	0	•	FD CB d 01 b 110		4	5	20	
SET b, r	r_b ← 1	•	•	X	•	X	•	•	•	CB 11 b r		2	2	8	
SET b, (HL)	$(HL)_b$ ← 1	•	•	X	•	X	•	•	•	CB 11 b 110		2	4	15	
SET b, (IX + d)	$(IX+d)_b$ ← 1	•	•	X	•	X	•	•	•	DD CB d 11 b 110		4	6	23	
SET b, (IY + d)	$(IY+d)_b$ ← 1	•	•	X	•	X	•	•	•	FD CB d 11 b 110		4	6	23	
RES b, m	m_b ← 0 m ≡ r, (HL), (IX + d), (IY + d)	•	•	X	•	X	•	•	•	CB 10 b r / 10 b 110 / DD CB d 10 b 110 / FD CB d 10 b 110					To form new opcode replace 11 of SET b, s with 10. Flags and time states for SET instruction.

NOTE: The instruction mnemonic is followed by one, two or three operands.

Jump Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210	Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
JP nn	PC ← nn	•	•	X	•	X	•	•	•	C3 — n — — n —		3	3	10	
JP cc, nn	If condition cc is true PC ← nn, otherwise continue	•	•	X	•	X	•	•	•	11 cc 010 — n — — n —		3	3	10	cc: 000 NZ non-zero, 001 Z zero, 010 NC non-carry, 011 C carry, 100 PO parity odd, 101 PE parity even, 110 P sign positive, 111 M sign negative
JR e	PC ← PC + e	•	•	X	•	X	•	•	•	00 011 000 — e − 2 —	18	2	3	12	
JR C, e	If C = 0, continue. If C = 1, PC ← PC + e	•	•	X	•	X	•	•	•	00 111 000 — e − 2 —	38	2	2	7	If condition not met
												2	3	12	If condition is met.
JR NC, e	If C = 1, continue. If C = 0, PC ← PC + e	•	•	X	•	X	•	•	•	00 110 000 — e − 2 —	30	2	2	7	If condition not met
												2	3	12	If condition is met.
JP Z, e	If Z = 0 continue. If Z = 1, PC ← PC + e	•	•	X	•	X	•	•	•	00 101 000 — e − 2 —	28	2	2	7	If condition not met.
												2	3	12	If condition is met.
JR NZ, e	If Z = 1, continue. If Z = 0, PC ← PC + e	•	•	X	•	X	•	•	•	00 100 000 — e − 2 —	20	2	2	7	If condition not met
												2	3	12	If condition is met.
JP (HL)	PC ← HL	•	•	X	•	X	•	•	•	E9		1	1	4	
JP (IX)	PC ← IX	•	•	X	•	X	•	•	•	DD E9		2	2	8	

Jump Group (Continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode	No. of Bytes	No. of M Cycles	No. of T States	Comments
JP (IY)	PC ← IY	•	•	X	•	X	•	•	•	11 111 101 FD 11 101 001 E9	2	2	8	
DJNZ, e	B ← B − 1 If B = 0, continue If B ≠ 0, PC ← PC + e	•	•	X	•	X	•	•	•	00 010 000 10 — e − 2 →	2	2	8	If B = 0.
									2	3	13	If B ≠ 0

NOTES: e represents the extension in the relative addressing mode.
e is a signed two's complement number in the range < − 126, 129 >.
e − 2 in the opcode provides an effective address of pc + e as PC is incremented by 2 prior to the addition of e

Call and Return Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode	No. of Bytes	No. of M Cycles	No. of T States	Comments
CALL nn	(SP − 1) ← PC_H (SP − 2) ← PC_L PC ← nn	•	•	X	•	X	•	•	•	11 001 101 CD — n → — n →	3	5	17	
CALL cc, nn	If condition cc is false continue, otherwise same as CALL nn	•	•	X	•	X	•	•	•	11 cc 100 — n → — n →	3	3	10	If cc is false.
									3	5	17	If cc is true.
RET	PC_L ← (SP) PC_H ← (SP + 1)	•	•	X	•	X	•	•	•	11 001 001 C9	1	3	10	
RET cc	If condition cc is false continue, otherwise same as RET	•	•	X	•	X	•	•	•	11 cc 000	1	1	5	If cc is false.
									1	3	11	If cc is true.
RETI	Return from interrupt	•	•	X	•	X	•	•	•	11 101 101 ED 01 001 101 4D	2	4	14	
RETN[1]	Return from non-maskable interrupt	•	•	X	•	X	•	•	•	11 101 101 ED 01 000 101 45	2	4	14	
RST p	(SP − 1) ← PC_H (SP − 2) ← PC_L PC_H ← 0 PC_L ← p	•	•	X	•	X	•	•	•	11 t 111	1	3	11	

cc: 000 NZ non-zero; 001 Z zero; 010 NC non-carry; 011 C carry; 100 PO parity odd; 101 PE parity even; 110 P sign positive; 111 M sign negative

t: 000 00H; 001 08H; 010 10H; 011 18H; 100 20H; 101 28H; 110 30H; 111 38H

NOTE: *RETN loads IFF_2 → IFF_1

Input and Output Group

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode	No. of Bytes	No. of M Cycles	No. of T States	Comments
IN A, (n)	A ← (n)	•	•	X	•	X	•	•	•	11 011 011 DB — n →	2	3	11	n to A_0 ~ A_7 Acc. to A_8 ~ A_{15}
IN r, (C)	r ← (C) if r = 110 only the flags will be affected	↕	↕ ①	X	P	0	•	11 101 101 ED 01 r 000	2	3	12	C to A_0 ~ A_7 B to A_8 ~ A_{15}
INI	(HL) ← (C) B ← B − 1 HL ← HL + 1	X	↕ ①	X	X	X	X	•	•	11 101 101 ED 10 100 010 A2	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
INIR	(HL) ← (C) B ← B − 1 HL ← HL + 1 Repeat until B = 0	X	↕ ①	X	X	X	X	•	•	11 101 101 ED 10 110 010 B2	2	5 (If B ≠ 0)	21	C to A_0 ~ A_7 B to A_8 ~ A_{15}
									2	4 (If B = 0)	16	
IND	(HL) ← (C) B ← B − 1 HL ← HL − 1	X	↕ ①	X	X	X	X	•	•	11 101 101 ED 10 101 010 AA	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
INDR	(HL) ← (C) B ← B − 1 HL ← HL − 1 Repeat until B = 0	X	↕ ①	X	X	X	X	•	•	11 101 101 ED 10 111 010 BA	2	5 (If B ≠ 0)	21	C to A_0 ~ A_7 B to A_8 ~ A_{15}
									2	4 (If B = 0)	16	
OUT (n), A	(n) ← A	•	•	X	•	X	•	•	•	11 010 011 D3 ← n —	2	3	11	n to A_0 ~ A_7 Acc. to A_8 ~ A_{15}
OUT (C), r	(C) ← r	•	• ①	X	•	X	•	•	•	11 101 101 ED 01 r 001	2	3	12	C to A_0 ~ A_7 B to A_8 ~ A_{15}
OUTI	(C) ← (HL) B ← B − 1 HL ← HL + 1	X	↕ ①	X	X	X	X	•	•	11 101 101 ED 10 100 011 A3	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}
OTIR	(C) ← (HL) B ← B − 1 HL ← HL + 1 Repeat until B = 0	X	↕ ①	X	X	X	X	•	•	11 101 101 ED 10 110 011 B3	2	5 (If B ≠ 0)	21	C to A_0 ~ A_7 B to A_8 ~ A_{15}
									2	4 (If B = 0)	16	
OUTD	(C) ← (HL) B ← B − 1 HL ← HL − 1	X	↕ ①	X	X	X	X	•	•	11 101 101 ED 10 101 011 AB	2	4	16	C to A_0 ~ A_7 B to A_8 ~ A_{15}

NOTE: ① If the result of B − 1 is zero the Z flag is set, otherwise it is reset

Input and Output Group (Continued)

Mnemonic	Symbolic Operation	S	Z	H	P/V	N	C	Opcode 76 543 210 Hex	No. of Bytes	No. of M Cycles	No. of T States	Comments
OTDR	(C) ← (HL) B ← B - 1 HL ← HL - 1 Repeat until B = 0	X	1	X	X	X	1	• 11 101 101 BD 10 111 011	2	5 (If B ≠ 0); 4 (If B = 0)	21 16	C to A_0 - A_7 B to A_8 - A_{15}

Summary of Flag Operation

Instruction	D_7 S	Z		H		P/V	N	D_0 C	Comments
ADD A, s; ADC A, s	↕	↕	X	↕	X	V	0	↕	8-bit add or add with carry.
SUB s; SBC A, s; CP s; NEG	↕	↕	X	↕	X	V	1	↕	8-bit subtract, subtract with carry, compare and negate accumulator.
AND s	↕	↕	X	1	X	P	0	0	Logical operations.
OR s; XOR s	↕	↕	X	0	X	P	0	0	
INC s	↕	↕	X	↕	X	V	0	•	8-bit increment.
DEC s	↕	↕	X	↕	X	V	1	•	8-bit decrement.
ADD DD, ss	•	•	X	X	X	•	0	↕	16-bit add.
ADC HL, ss	↕	↕	X	X	X	V	0	↕	16-bit add with carry.
SBC HL, ss	↕	↕	X	X	X	V	1	↕	16-bit subtract with carry.
RLA, RLCA, RRA, RRCA	•	•	X	0	X	•	0	↕	Rotate accumulator.
RL m, RLC m; RR m; RRC m; SLA m; SRA m, SRL m	↕	↕	X	0	X	P	0	↕	Rotate and shift locations.
RLD, RRD	↕	↕	X	0	X	P	0	•	Rotate digit left and right.
DAA	↕	↕	X	↕	X	P	•	↕	Decimal adjust accumulator.
CPL	•	•	X	1	X	•	1	•	Complement accumulator.
SCF	•	•	X	0	X	•	0	1	Set carry.
CCF	•	•	X	X	X	•	0	↕	Complement carry.
IN r,(C)	↕	↕	X	0	X	P	0	•	Input register indirect.
INI, IND, OUTI, OUTD	X	↕	X	X	X	X	1	•	Block input and output. Z = 0 if B ≠ 0 otherwise Z = 1.
INIR; INDR, OTIR, OTDR	X	1	X	X	X	X	1	•	
LDI, LDD	X	X	X	0	X	↕	0	•	Block transfer instructions. P/V = 1 if BC ≠ 0, otherwise P/V = 0.
LDIR; LDDR	X	X	X	0	X	0	0	•	
CPI; CPIR; CPD; CPDR	X	↕	X	X	X	↕	1	•	Block search instructions. Z = 1 if A = (HL), otherwise Z = 0. P/V = 1 if BC ≠ 0, otherwise P/V = 0.
LD A, I; LD A, R	↕	↕	X	0	X	IFF	0	•	The content of the interrupt enable flip-flop (IFF) is copied into the P/V flag.
BIT b, s	X	↕	X	1	X	X	0	•	The state of bit b of location s is copied into the Z flag.

Symbolic Notation

Symbol	Operation
S	Sign flag. S = 1 if the MSB of the result is 1.
Z	Zero flag. Z = 1 if the result of the operation is 0.
P/V	Parity or overflow flag. Parity (P) and overflow (V) share the same flag. Logical operations affect this flag with the parity of the result while arithmetic operations affect this flag with the overflow of the result. If P/V holds parity, P/V = 1 if the result of the operation is even, P/V = 0 if result is odd. If P/V holds overflow, P/V = 1 if the result of the operation produced an overflow.
H	Half-carry flag. H = 1 if the add or subtract operation produced a carry into or borrow from bit 4 of the accumulator.
N	Add/Subtract flag. N = 1 if the previous operation was a subtract.
H & N	H and N flags are used in conjunction with the decimal adjust instruction (DAA) to properly correct the result into packed BCD format following addition or subtraction using operands with packed BCD format.
C	Carry/Link flag. C = 1 if the operation produced a carry from the MSB of the operand or result.

Symbol	Operation
↕	The flag is affected according to the result of the operation.
•	The flag is unchanged by the operation.
0	The flag is reset by the operation.
1	The flag is set by the operation.
X	The flag is a "don't care."
V	P/V flag affected according to the overflow result of the operation.
P	P/V flag affected according to the parity result of the operation.
r	Any one of the CPU registers A, B, C, D, E, H, L.
s	Any 8-bit location for all the addressing modes allowed for the particular instruction.
ss	Any 16-bit location for all the addressing modes allowed for that instruction.
ii	Any one of the two index registers IX or IY.
R	Refresh counter.
n	8-bit value in range < 0, 255 >.
nn	16-bit value in range < 0, 65535 >.

Pin Descriptions

A_0–A_{15}. *Address Bus* (output, active High, 3-state). A_0–A_{15} form a 16-bit address bus. The Address Bus provides the address for memory data bus exchanges (up to 64K bytes) and for I/O device exchanges.

$\overline{\text{BUSACK}}$. *Bus Acknowledge* (output, active Low). Bus Acknowledge indicates to the requesting device that the CPU address bus, data bus, and control signals $\overline{\text{MREQ}}$, $\overline{\text{IORQ}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ have entered their high-impedance states. The external circuitry can now control these lines.

$\overline{\text{BUSREQ}}$. *Bus Request* (input, active Low). Bus Request has a higher priority than $\overline{\text{NMI}}$ and is always recognized at the end of the current machine cycle. $\overline{\text{BUSREQ}}$ forces the CPU address bus, data bus, and control signals $\overline{\text{MREQ}}$, $\overline{\text{IORQ}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ to go to a high-impedance state so that other devices can control these lines. $\overline{\text{BUSREQ}}$ is normally wire-ORed and requires an external pullup for these applications. Extended $\overline{\text{BUSREQ}}$ periods due to extensive DMA operations can prevent the CPU from properly refreshing dynamic RAMs.

D_0–D_7. *Data Bus* (input/output, active High, 3-state). D_0–D_7 constitute an 8-bit bidirectional data bus, used for data exchanges with memory and I/O.

$\overline{\text{HALT}}$. *Halt State* (output, active Low). $\overline{\text{HALT}}$ indicates that the CPU has executed a Halt instruction and is awaiting either a non-maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOPs to maintain memory refresh.

$\overline{\text{INT}}$. *Interrupt Request* (input, active Low). Interrupt Request is generated by I/O devices. The CPU honors a request at the end of the current instruction if the internal software-controlled interrupt enable flip-flop (IFF) is enabled. $\overline{\text{INT}}$ is normally wire-ORed and requires an external pullup for these applications.

$\overline{\text{IORQ}}$. *Input/Output Request* (output, active Low, 3-state). $\overline{\text{IORQ}}$ indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. $\overline{\text{IORQ}}$ is also generated concurrently with $\overline{\text{M1}}$ during an interrupt acknowledge cycle to indicate that an interrupt response vector can be placed on the data bus.

$\overline{\text{M1}}$. *Machine Cycle One* (output, active Low). $\overline{\text{M1}}$, together with $\overline{\text{MREQ}}$, indicates that the current machine cycle is the opcode fetch cycle of an instruction execution. $\overline{\text{M1}}$, together with $\overline{\text{IORQ}}$, indicates an interrupt acknowledge cycle.

$\overline{\text{MREQ}}$. *Memory Request* (output, active Low, 3-state). $\overline{\text{MREQ}}$ indicates that the address bus holds a valid address for a memory read or memory write operation.

$\overline{\text{NMI}}$. *Non-Maskable Interrupt* (input, active Low). $\overline{\text{NMI}}$ has a higher priority than $\overline{\text{INT}}$. $\overline{\text{NMI}}$ is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop, and automatically forces the CPU to restart at location 0066H.

$\overline{\text{RD}}$. *Memory Read* (output, active Low, 3-state). $\overline{\text{RD}}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

$\overline{\text{RESET}}$. *Reset* (input, active Low). $\overline{\text{RESET}}$ initializes the CPU as follows: it resets the interrupt enable flip-flop, clears the PC and Registers I and R, and sets the interrupt status to Mode 0. During reset time, the address and data bus go to a high-impedance state, and all control output signals go to the inactive state. Note that $\overline{\text{RESET}}$ must be active for a minimum of three full clock cycles before the reset operation is complete.

$\overline{\text{RFSH}}$. *Refresh* (output, active Low). $\overline{\text{RFSH}}$, together with $\overline{\text{MREQ}}$, indicates that the lower seven bits of the system's address bus can be used as a refresh address to the system's dynamic memories.

$\overline{\text{WAIT}}$. *Wait* (input, active Low). $\overline{\text{WAIT}}$ indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter a Wait state as long as this signal is active. Extended $\overline{\text{WAIT}}$ periods can prevent the CPU from refreshing dynamic memory properly.

$\overline{\text{WR}}$. *Memory Write* (output, active Low, 3-state). $\overline{\text{WR}}$ indicates that the CPU data bus holds valid data to be stored at the addressed memory or I/O location.

CPU Timing

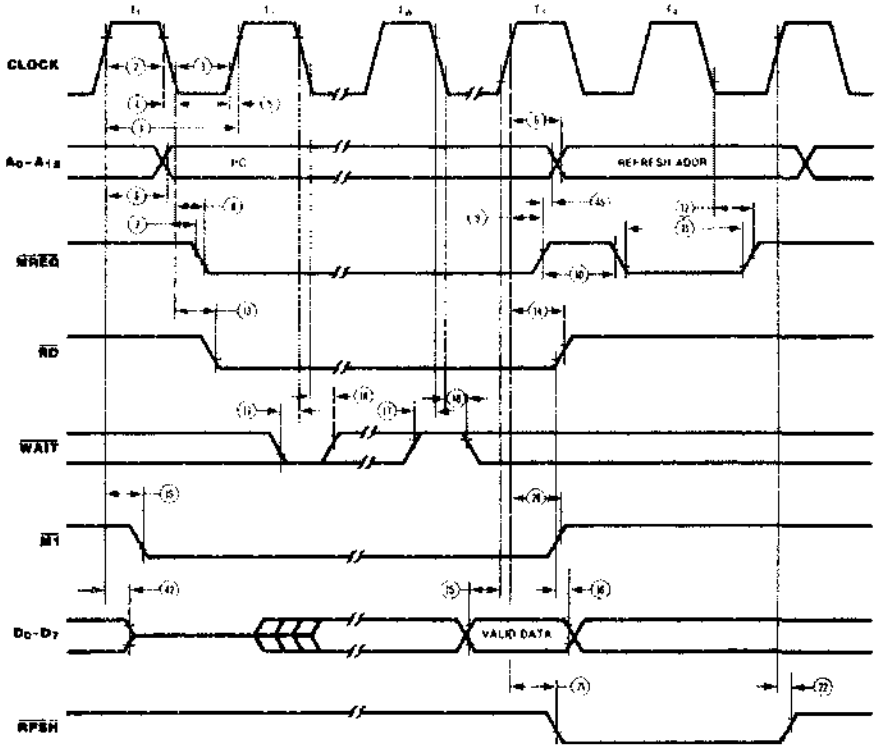
The Z80 CPU executes instructions by proceeding through a specific sequence of operations:

- Memory read or write
- I/O device read or write
- Interrupt acknowledge

The basic clock period is referred to as a T time or cycle, and three or more T cycles make up a machine cycle (M1, M2 or M3 for instance). Machine cycles can be extended either by the CPU automatically inserting one or more Wait states or by the insertion of one or more Wait states by the user.

Instruction Opcode Fetch. The CPU places the contents of the Program Counter (PC) on the address bus at the start of the cycle (Figure 5). Approximately one half clock cycle later, $\overline{MREQ}$ goes active. The falling edge of $\overline{MREQ}$ can be used directly as a Chip Enable to dynamic memories. When active, $\overline{RD}$ indicates that the memory data can be enabled onto the CPU data bus.

The CPU samples the $\overline{WAIT}$ input with the rising edge of clock state T3. During clock states T3 and T4 of an M1 cycle dynamic RAM refresh can occur while the CPU starts decoding and executing the instruction. When the Refresh Control signal becomes active, refreshing of dynamic memory can take place



NOTE: T_W = Wait cycle added when necessary for slow ancillary devices

Figure 5. Instruction Opcode Fetch

CPU Timing (Continued)

Memory Read or Write Cycles. Figure 6 shows the timing of memory read or write cycles other than an opcode fetch ($\overline{M1}$) cycle. The $\overline{MREQ}$ and $\overline{RD}$ signals function exactly as in the fetch cycle. In a memory write cycle, $\overline{MREQ}$ also becomes active when the address bus is stable, so that it can be used directly as a Chip Enable for dynamic memories. The $\overline{WR}$ line is active when the data bus is stable, so that it can be used directly as an R/$\overline{W}$ pulse to most semiconductor memories.

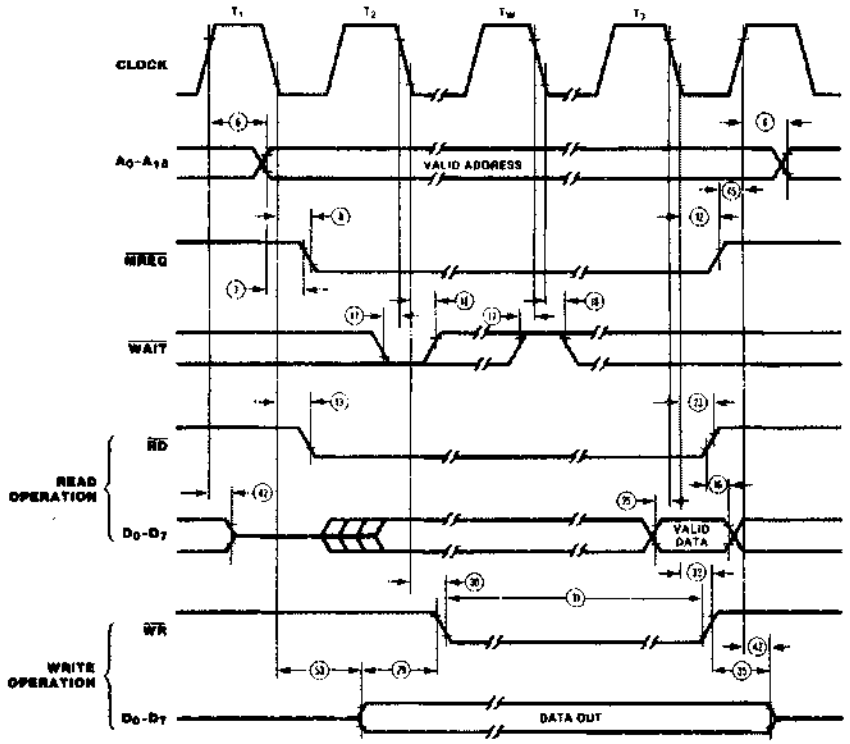
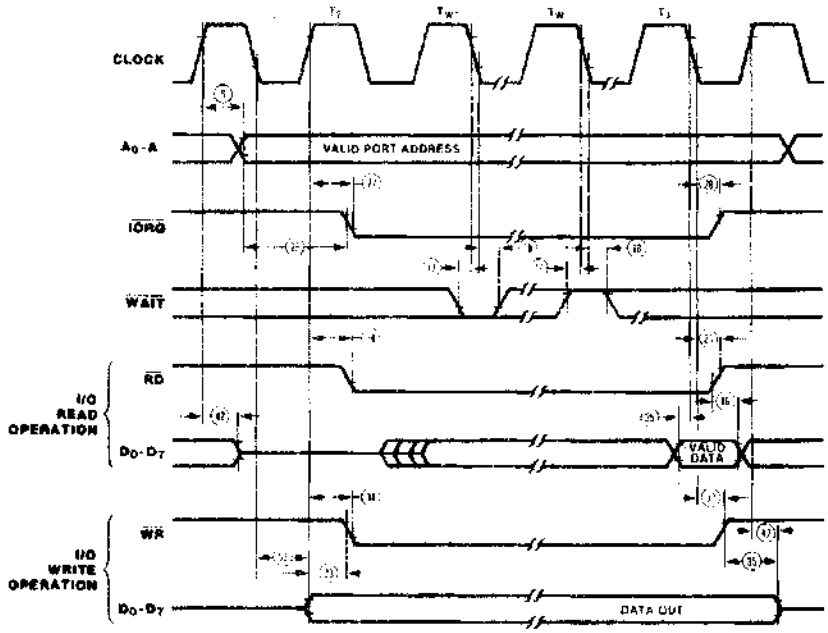


Figure 6. Memory Read or Write Cycles

CPU Timing (Continued)

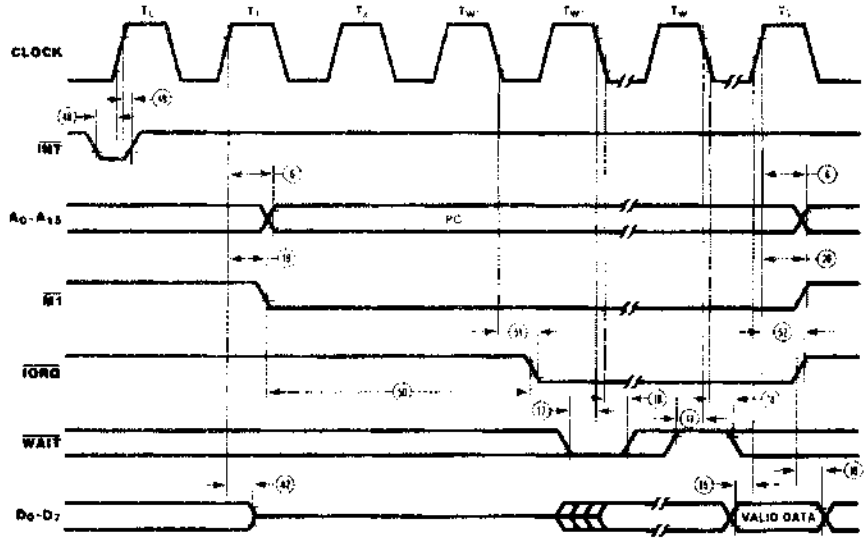
Input or Output Cycles. Figure 7 shows the timing for an I/O read or I/O write operation. During I/O operations, the CPU automatically inserts a single Wait state (T_W). This extra Wait state allows sufficient time for an I/O port to decode the address and the port address lines.



NOTE: T_{W^*} = One Wait cycle automatically inserted by CPU

Figure 7. Input or Output Cycles

Interrupt Request/Acknowledge Cycle. The CPU samples the interrupt signal with the rising edge of the last clock cycle at the end of any instruction (Figure 8). When an interrupt is accepted, a special $\overline{M1}$ cycle is generated. During this $\overline{M1}$ cycle, $\overline{IORQ}$ becomes active (instead of $\overline{MREQ}$) to indicate that the interrupting device can place an 8-bit vector on the data bus. The CPU automatically adds two Wait states to this cycle.

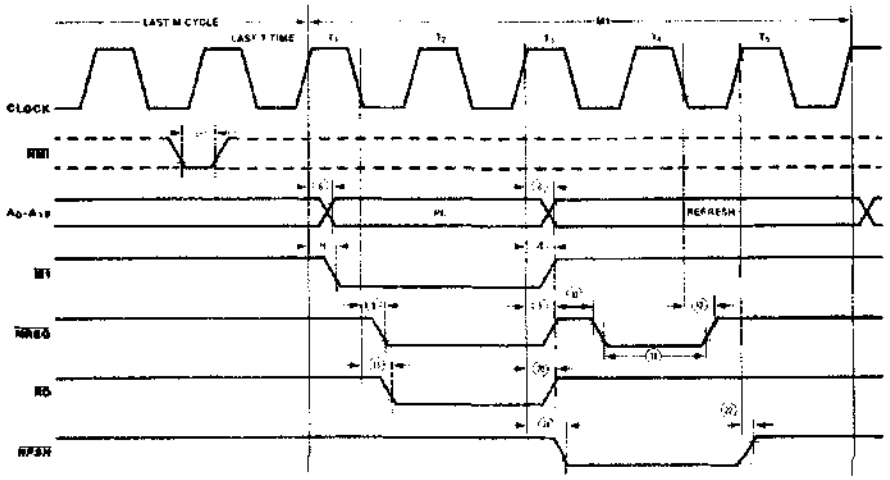


NOTE: 1) T_L = Last state of previous instruction. 2) Two Wait cycles automatically inserted by CPU(*).

Figure 8. Interrupt Request/Acknowledge Cycle

CPU Timing (Continued)

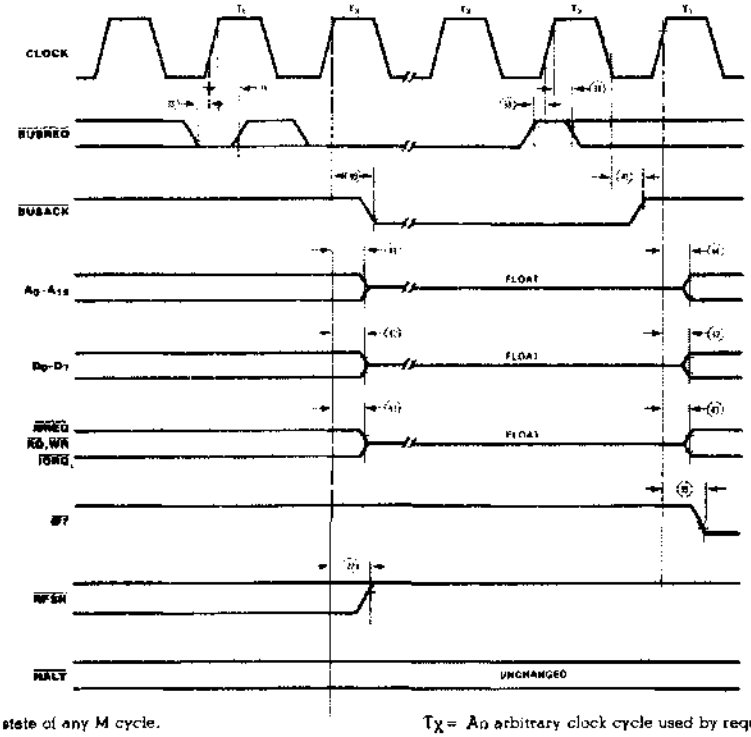
Non-Maskable Interrupt Request Cycle. $\overline{NMI}$ is sampled at the same time as the maskable interrupt input $\overline{INT}$ but has higher priority and cannot be disabled under software control. The subsequent timing is similar to that of a normal memory read operation except that data put on the bus by the memory is ignored. The CPU instead executes a restart (RST) operation and jumps to the $\overline{NMI}$ service routine located at address 0066H (Figure 9).



*Although $\overline{NMI}$ is an asynchronous input, to guarantee its being recognized on the following machine cycle, $\overline{NMI}$'s falling edge must occur no later than the rising edge of the clock cycle preceding T_{LAST}.

Figure 9. Non-Maskable Interrupt Request Operation

Bus Request/Acknowledge Cycle. The CPU samples $\overline{BUSREQ}$ with the rising edge of the last clock period of any machine cycle (Figure 10). If $\overline{BUSREQ}$ is active, the CPU sets its address, data, and $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$ lines to a high-impedance state with the rising edge of the next clock pulse. At that time, any external device can take control of these lines, usually to transfer data between memory and I/O devices.

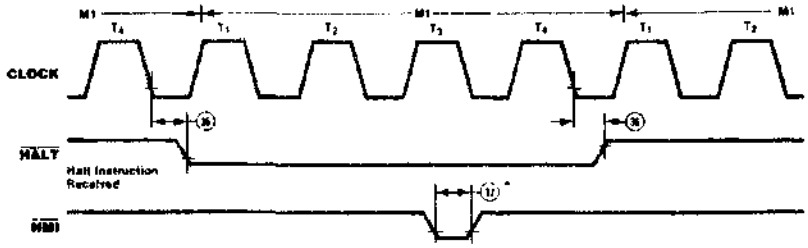


NOTE: T_L = Last state of any M cycle. T_X = An arbitrary clock cycle used by requesting device.

Figure 10. Bus Request/Acknowledge Cycle

CPU Timing (Continued)

Halt Acknowledge Cycle. When the CPU receives a $\overline{HALT}$ instruction, it executes NOP states until either an $\overline{INT}$ or $\overline{NMI}$ input is received. When in the Halt state, the $\overline{HALT}$ output is active and remains so until an interrupt is processed (Figure 11).



NOTE: INT will also force a Halt exit.

*See note, Figure 9.

Figure 11. Halt Acknowledge Cycle

Reset Cycle. $\overline{RESET}$ must be active for at least three clock cycles for the CPU to properly accept it. As long as $\overline{RESET}$ remains active, the address and data buses float, and the control outputs are inactive. Once $\overline{RESET}$ goes inactive, two internal T cycles are consumed before the CPU resumes normal processing operation. $\overline{RESET}$ clears the PC register, so the first opcode fetch will be to location 0000 (Figure 12).

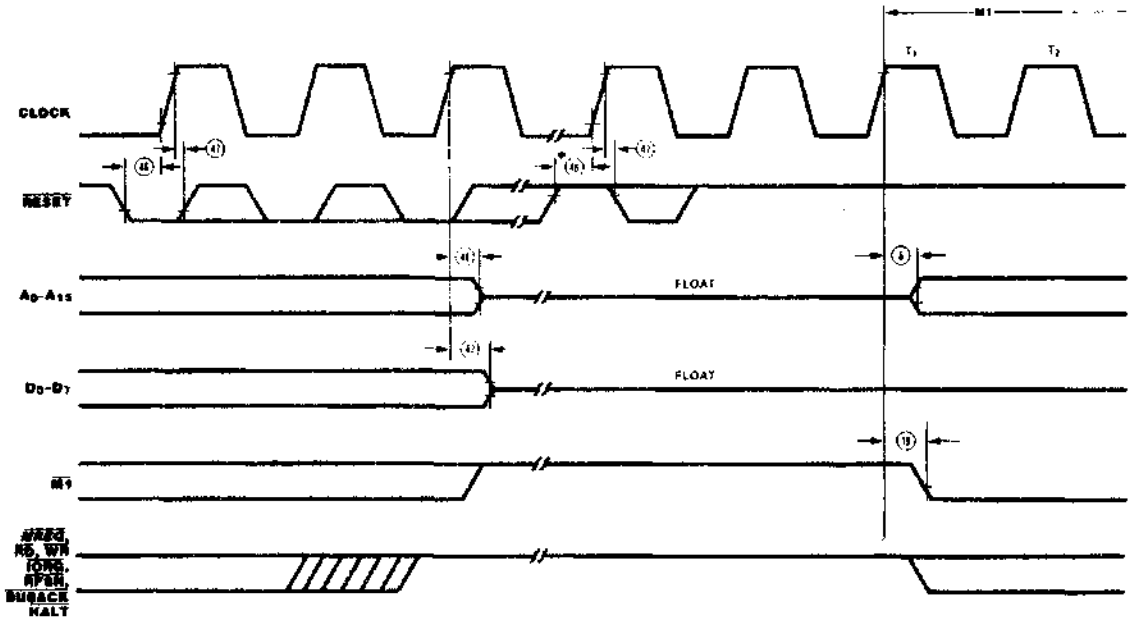


Figure 12. Reset Cycle

AC Characteristics

Number	Symbol	Parameter	Z80 CPU Min (ns)	Z80 CPU Max (ns)	Z80A CPU Min (ns)	Z80A CPU Max (ns)	Z80B CPU Min (ns)	Z80B CPU Max (ns)
1	TcC	Clock Cycle Time	400*		250*		165*	
2	TwCh	Clock Pulse Width (High)	180*		110*		65*	
3	TwCl	Clock Pulse Width (Low)	180	2000	110	2000	65	2000
4	TfC	Clock Fall Time	—	30	—	30	—	20
5	TrC	Clock Rise Time	—	30	—	30	—	20
6	TdCr(A)	Clock ↑ to Address Valid Delay	—	145	—	110	—	90
7	TdA(MREQf)	Address Valid to $\overline{MREQ}$ ↓ Delay	125*	—	65*	—	35*	—
8	TdCf(MREQf)	Clock ↓ to $\overline{MREQ}$ ↓ Delay	—	100	—	85	—	70
9	TdCr(MREQr)	Clock ↑ to $\overline{MREQ}$ ↑ Delay	—	100	—	85	—	70
10	TwMREQh	$\overline{MREQ}$ Pulse Width (High)	170*		110*		65*	
11	TwMREQl	$\overline{MREQ}$ Pulse Width (Low)	360*	—	220*	—	135*	—
12	TdCf(MREQr)	Clock ↓ to $\overline{MREQ}$ ↑ Delay	—	100	—	85	—	70
13	TdCf(RDf)	Clock ↓ to $\overline{RD}$ ↓ Delay	—	130	—	95	—	80
14	TdCr(RDr)	Clock ↑ to $\overline{RD}$ ↑ Delay	—	100	—	85	—	70
15	TsD(Cr)	Data Setup Time to Clock ↑	50		35		30	
16	ThD(RDr)	Data Hold Time to $\overline{RD}$ ↑	—	0	—	0	—	0
17	TsWAIT(Cf)	$\overline{WAIT}$ Setup Time to Clock ↓	70	—	70	—	60	—
18	ThWAIT(Cf)	$\overline{WAIT}$ Hold Time after Clock ↓	—	0	—	0	—	0
19	TdCr(M1f)	Clock ↑ to $\overline{M1}$ ↓ Delay	—	130	—	100	—	80
20	TdCr(M1r)	Clock ↑ to $\overline{M1}$ ↑ Delay	—	130	—	100	—	80
21	TdCr(RFSHf)	Clock ↑ to $\overline{RFSH}$ ↓ Delay	—	180	—	130	—	110
22	TdCr(RFSHr)	Clock ↑ to $\overline{RFSH}$ ↑ Delay	—	150	—	120	—	100
23	TdCf(RDr)	Clock ↓ to $\overline{RD}$ ↑ Delay	—	110	—	85	—	70
24	TdCr(RDf)	Clock ↑ to $\overline{RD}$ ↓ Delay	—	100	—	85	—	70
25	TsD(Cf)	Data Setup to Clock ↓ during M_2, M_3, M_4 or M_5 Cycles	60		50		40	
26	TdA(IORQf)	Address Stable prior to $\overline{IORQ}$ ↓	320*	—	180*	—	110*	—
27	TdCr(IORQf)	Clock ↑ to $\overline{IORQ}$ ↓ Delay	—	90	—	75	—	65
28	TdCf(IORQr)	Clock ↓ to $\overline{IORQ}$ ↑ Delay	—	110	—	85	—	70
29	TdD(WRf)	Data Stable prior to $\overline{WR}$ ↓	190*	—	80*	—	25*	—
30	TdCf(WRf)	Clock ↓ to $\overline{WR}$ ↓ Delay	—	90	—	80	—	70
31	TwWR	$\overline{WR}$ Pulse Width	360*	—	220*	—	135*	—
32	TdCf(WRr)	Clock ↓ to $\overline{WR}$ ↑ Delay	—	100	—	80	—	70
33	TdD(WRf)	Data Stable prior to $\overline{WR}$ ↓	20*	—	-10*	—	-55*	—
34	TdCr(WRf)	Clock ↑ to $\overline{WR}$ ↓ Delay	—	80	—	65	—	60
35	TdWRr(D)	Data Stable from $\overline{WR}$ ↑	120*		60*		30*	
36	TdCf(HALT)	Clock ↓ to $\overline{HALT}$ ↑ or ↓	—	300	—	300	—	260
37	TwNMI	$\overline{NMI}$ Pulse Width	80	—	80	—	70	—
38	TsBUSREQ(Cr)	$\overline{BUSREQ}$ Setup Time to Clock ↑	80	—	50	—	50	—

*For clock periods other than the minimums shown in the table, calculate parameters using the expressions in the table on the following page.

AC Characteristics (Continued)

Number	Symbol	Parameter	Z80 CPU Min (ns)	Z80 CPU Max (ns)	Z80A CPU Min (ns)	Z80A CPU Max (ns)	Z80B CPU Min (ns)	Z80B CPU Max (ns)
39	ThBUSREQ(Cr)	BUSREQ Hold Time after Clock ↑	0	--	0	--	0	-
40	TdCr(BUSACKf)	Clock ↑ to BUSACK ↓ Delay		120		100		90
41	TdCf(BUSACKr)	Clock ↓ to BUSACK ↑ Delay		110		100	-	90
42	TdCr(Dz)	Clock ↑ to Data Float Delay	--	90	--	90	--	80
43	TdCr(CTz)	Clock ↑ to Control Outputs Float Delay (MREQ, IORQ, RD, and WR)		110	--	80	--	70
44	TdCr(Az)	Clock ↑ to Address Float Delay	-	110	--	90	-	80
45	TdCTr(A)	Address Stable after MREQ ↑, IORQ ↑, RD ↑, and WR ↑	160*		80*		35*	
46	TsRESET(Cr)	RESET to Clock ↑ Setup Time	90	--	60	--	60	-
47	ThRESET(Cr)	RESET to Clock ↑ Hold Time	--	0	--	0	--	0
48	TsINTf(Cr)	INT to Clock ↑ Setup Time	80	--	80	--	70	-
49	ThINTr(Cr)	INT to Clock ↑ Hold Time	-	0	--	0	--	0
50	TdM1f(IORQf)	M1 ↓ to IORQ ↓ Delay	920*		565*		365*	
51	TdCf(IORQf)	Clock ↓ to IORQ ↓ Delay	-	110	--	85	--	70
52	TdCf(IORQr)	Clock ↓ to IORQ ↑ Delay	--	100		85	--	70
53	TdCf(D)	Clock ↓ to Data Valid Delay	-	230	--	150	--	130

*For clock periods other than the minimum shown, calculate parameters as for the following equations. Calculated values above assumed Tr = TfC = 20 ns.

Footnotes to AC Characteristics

Number	Symbol	Z80	Z80A	Z80B
1	TcC	TwCh + TwCl + TrC + TfC	TwCh + TwCl + TrC + TfC	TwCh + TwCl + TrC + TfC
2	TwCh	Although static by design, TwCh of greater than 200 μs is not guaranteed	Although static by design, TwCh of greater than 200 μs is not guaranteed	Although static by design, TwCh of greater than 200 μs is not guaranteed
7	TdA(MREQf)	TwCh + TfC - 75	TwCh + TfC - 65	TwCh + TfC - 50
10	TwMREQh	TwCh + TfC - 30	TwCh + TfC - 20	TwCh + TfC - 20
11	TwMREQl	TcC - 40	TcC - 30	TcC - 30
26	TdA(IORQf)	TcC - 80	TcC - 70	TcC - 55
29	TdD(WRf)	TcC - 210	TcC - 170	TcC - 140
31	TwWR	TcC - 40	TcC - 30	TcC - 30
33	TdD(WRf)	TwCl + TrC - 190	TwCl + TrC - 140	TwCl + TrC - 140
35	TdWRr(D)	TwCl + TrC - 80	TwCl + TrC - 70	TwCl + TrC - 55
45	TdCTr(A)	TwCl + TrC - 40	TwCl + TrC - 50	TwCl + TrC - 50
50	TdM1f(IORQf)	2TcC + TwCh + TfC - 80	2TcC + TwCh + TfC - 65	2TcC + TwCh + TfC - 50

AC Test Conditions:
V_{IH} = 2.0 V
V_{IL} = 0.8 V
V_{IHC} = V_{CC} -0.6 V
V_{ILC} = 0.45 V
V_{OH} = 2.0 V
V_{OL} = 0.8 V
FLOAT = ±0.5 V

Absolute Maximum Ratings

Storage Temperature . . . . −65°C to +150°C
Temperature under Bias . . . . . Specified operating range
Voltages on all inputs and outputs with respect to ground . −0.3 V to +7 V
Power Dissipation . . . . . 1.5 W

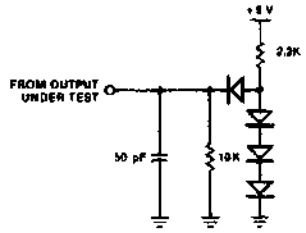
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0 V). Positive current flows into the referenced pin. Available operating temperature ranges are:

- 0°C to +70°C, $+4.75\ V \le V_{CC} \le +5.25\ V$
- −40°C to +85°C, $+4.75\ V \le V_{CC} \le +5.25\ V$
- −55°C to +125°C, $+4.5\ V \le V_{CC} \le +5.5\ V$

All ac parameters assume a load capacitance of 50 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for address and control lines.



DC Characteristics

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	−0.3	0.45	V	
V_{IHC}	Clock Input High Voltage	V_{CC} −.6	V_{CC} +.3	V	
V_{IL}	Input Low Voltage	−0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 1.8 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −250 μA
I_{CC}	Power Supply Current				
	Z80		150[1]	mA	
	Z80A		200[2]	mA	
	Z80B		200	mA	
I_{LI}	Input Leakage Current		10	μA	V_{IN} = 0 to V_{CC}
I_{LEAK}	3-State Output Leakage Current in Float	−10	10[3]	μA	V_{OUT} = 0.4 to V_{CC}

1. For military grade parts, I_{CC} is 200 mA.
2. Typical rate for Z80A is 90 mA.
3. A_{15}-A_0, D_7-D_0, $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$.

Capacitance

Symbol	Parameter	Min	Max	Unit	Note
C_{CLOCK}	Clock Capacitance		35	pF	Unmeasured pins returned to ground
C_{IN}	Input Capacitance		5	pF	
C_{OUT}	Output Capacitance		10	pF	

T_A = 25°C, f = 1 MHz

Ordering Information

Product Number	Package/ Temp	Speed	Description	Product Number	Package/ Temp	Speed	Description
Z8400	CE	2.5 MHz	Z80 CPU (40-pin)	Z8400A	DE	4.0 MHz	Z80A CPU (40-pin)
Z8400	CM	2.5 MHz	Same as above	Z8400A	DS	4.0 MHz	Same as above
Z8400	CMB	2.5 MHz	Same as above	Z8400A	PE	4.0 MHz	Same as above
Z8400	CS	2.5 MHz	Same as above	Z8400A	PS	4.0 MHz	Same as above
Z8400	DE	2.5 MHz	Same as above	Z8400B	CE	6.0 MHz	Z80B CPU (40-pin)
Z8400	DS	2.5 MHz	Same as above	Z8400B	CM	6.0 MHz	Same as above
Z8400	PE	2.5 MHz	Same as above	Z8400B	CMB	6.0 MHz	Same as above
Z8400	PS	2.5 MHz	Same as above	Z8400B	CS	6.0 MHz	Same as above
Z8400A	CE	4.0 MHz	Z80A CPU (40-pin)	Z8400B	DE	6.0 MHz	Same as above
Z8400A	CM	4.0 MHz	Same as above	Z8400B	DS	6.0 MHz	Same as above
Z8400A	CMB	4.0 MHz	Same as above	Z8400B	PE	6.0 MHz	Same as above
Z8400A	CS	4.0 MHz	Same as above	Z8400B	PS	6.0 MHz	Same as above

NOTES: C = Ceramic, D = Cerdip, P = Plastic, E = -40°C to +85°C, M = -55°C to +125°C, MB = -55°C to +125°C with MIL-STD-883 Class B processing, S = 0°C to +70°C

2.0 64K DYNAMIC MEMORY BOARD

GENERAL INFORMATION

The Nabu Memory Board ADM-1000, uses industry standard 4116 dynamic random-access memories (RAM's); which provide low cost and low power consumption. Reliability of the board is enhanced by the low support-IC count, and the use of a precision delay line for critical timing.

Address lines and data lines are fully buffered by line drivers/receivers with hysteresis at the inputs to improve noise immunity. The memory board offers a full 64K bytes of read/write memory; however only 62K bytes are available to the user in the Nabu 1100 System, since 2K bytes are allocated to the disk bootstrap program in ROM. A signal called PHANTOM from the S-100 bus, can be utilized to allow user ROM to overlay the RAM.

In the Nabu 1100 System, the access time of the memory chips is 150 nanoseconds (ns), permitting operation at 4 MHz, with no wait states added. The use of slower memory chips is not recommended. Memory refresh is done automatically by the Z-80A CPU after each instruction fetch. This mode of refresh is totally transparent to the programmer and does not slow down the CPU operation.

SPECIFIC FEATURES

Memory Organization

The 4116 RAM chip has a 16K x 1 organization, with eight chips connected in parallel to form a 16K byte memory bank. Four memory banks are implemented on the memory board.

The jumper options on the left side of the board are used for selecting memory banks. Each bank can be enabled or disabled, by installing or removing each corresponding jumper. In this way, up to 64K bytes of memory space can be obtained.

The jumpers are numbered as follows:

Jumper	Bank #	RAM IC's Needed	Address Space
JP-1:	1	RAM 1 - RAM 8,	0000H - 3FFFH
JP-2:	2	RAM 9 - RAM 16,	4000H - 7FFFH
JP-3:	3	RAM 17 - RAM 24,	8000H - BFFFH
JP-4:	4	RAM 25 - RAM 32,	C000H - FFFFH

Each bank is enabled by installing the appropriate jumper.

Memory Refresh

As mentioned, the memory refresh is done automatically by the Z-80A CPU through the S-100 bus. The CPU contains a 7-bit memory refresh counter, which is incremented automatically after each instruction fetch. The data in the counter is sent out on the lower portion of the address bus along with two refresh control signals, $\overline{RFSH}$ (pin 66) and $\overline{MREQ}$ (pin 65); while the CPU is decoding and executing the fetched instruction. This refresh operation must be performed at least every two milliseconds in order to retain data.

An interrupt request/acknowledge cycle in the system does not affect the memory refresh operation, since only two wait states are added to this cycle for identifying the interrupting

I/O device. However, a bus request/acknowledge cycle used in Direct Memory Access (DMA), for instance, can cause a memory refresh problem if very long DMA cycles are used. Therefore, the DMA controller must perform the necessary refresh function.

A user supplied S-100 bus compatible board which uses wait states can also be used in the Nabu 1100 System, providing the wait states added do not exceed the 2 ms limit. However, caution should be used in adding boards with wait states, unless the number and frequency of wait states is strictly controlled.

Data Buffers and PHANTOM

All data-in and data-out lines of the memory chips are buffered by U9 and U14. The data-in lines are always enabled and the data-out lines are controlled by U5, whose four inputs are conditioned by PDBIN, SMEMR, $\overline{\text{MREQ}}$, $\overline{\text{PHANTOM}}$, and by two high address bits (A15 and A14). Reading of the RAM contents is not allowed when U5 is disabled; however writing into the RAM is still permissible.

$\overline{\text{PHANTOM}}$ is normally pulled high through a resistor. This line is primarily used for system bootstrapping by overlaying the RAM with ROM (not used in the Nabu 1100 System). This is done by pulling $\overline{\text{PHANTOM}}$ low at system start-up, copying the ROM contents into the RAM which occupies the same address, and executing the bootstrap program from the RAM after pulling $\overline{\text{PHANTOM}}$ high. In this way, a full 64K bytes of read/write memory is obtained.

NABU ADM-1000 64K DYNAMIC MEMORY BOARD
PARTS LIST

Integrated Circuits:

U1	74LS75	Quadruple latch
U2	74LS42	4-line-to-10-line decoder
U3, U4	74LS00	Quadruple 2-input NAND
U5	74LS20	Dual 4-input NAND
U6	74LS132	Quadruple 2-input NAND with Schmitt-triggered inputs
U7, U8	74S157	Quadruple 2-line-to-1-line Schottky multiplexer
U9, U14	74LS241	Octal buffer/line-driver with 3-state outputs
U10-U13	74LS14	Hex inverter with Schmitt-triggered inputs
U15	STTLDM-355	TTL-compatible logic-delay module
U16	7805	5 V positive voltage regulator
U17	7812	12 V positive voltage regulator
RAM1-RAM32	4116	16384-bit dynamic RAM (150 ns)

Diodes:

D1	1N4733A	5.1 V, 1.0 W, 5 % zener diode

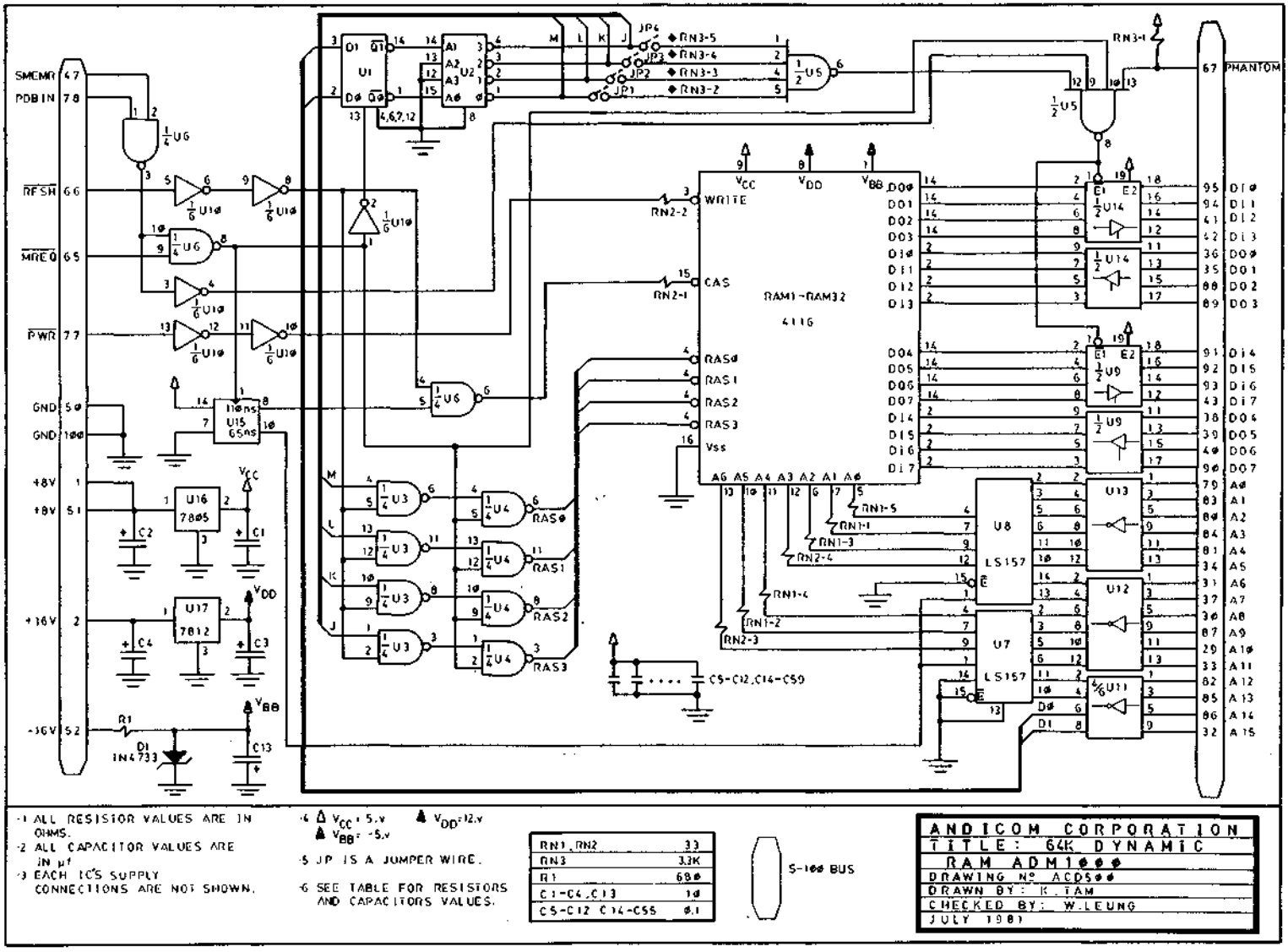
Capacitors:

C1-C4, C13	10 µF, 25 V tantalum electrolytic
C5-C12, C14-C59	0.1 µF

Resistors:

R1	680Ω, 0.5 W, 10%
RN1,RN2	5-resistor pack of 33Ω resistors
RN3	5-resistor pack of 3.3 kΩ resistors with common pin #1

Quantity	Description
36	16 pin IC socket
9	14 pin IC socket
2	20 pin IC socket
2	6-32 x 3/8" machine screw
2	#6-32 nuts
2	Delta 291-0.36-AB-H
1	p.c. board



-1 ALL RESISTOR VALUES ARE IN OHMS.
-2 ALL CAPACITOR VALUES ARE IN μf
-3 EACH IC'S SUPPLY CONNECTIONS ARE NOT SHOWN.

-4 △ V_{CC} = 5.v ▲ V_{DD}=12.v ▲ V_{BB}= -5.v

-5 JP IS A JUMPER WIRE.

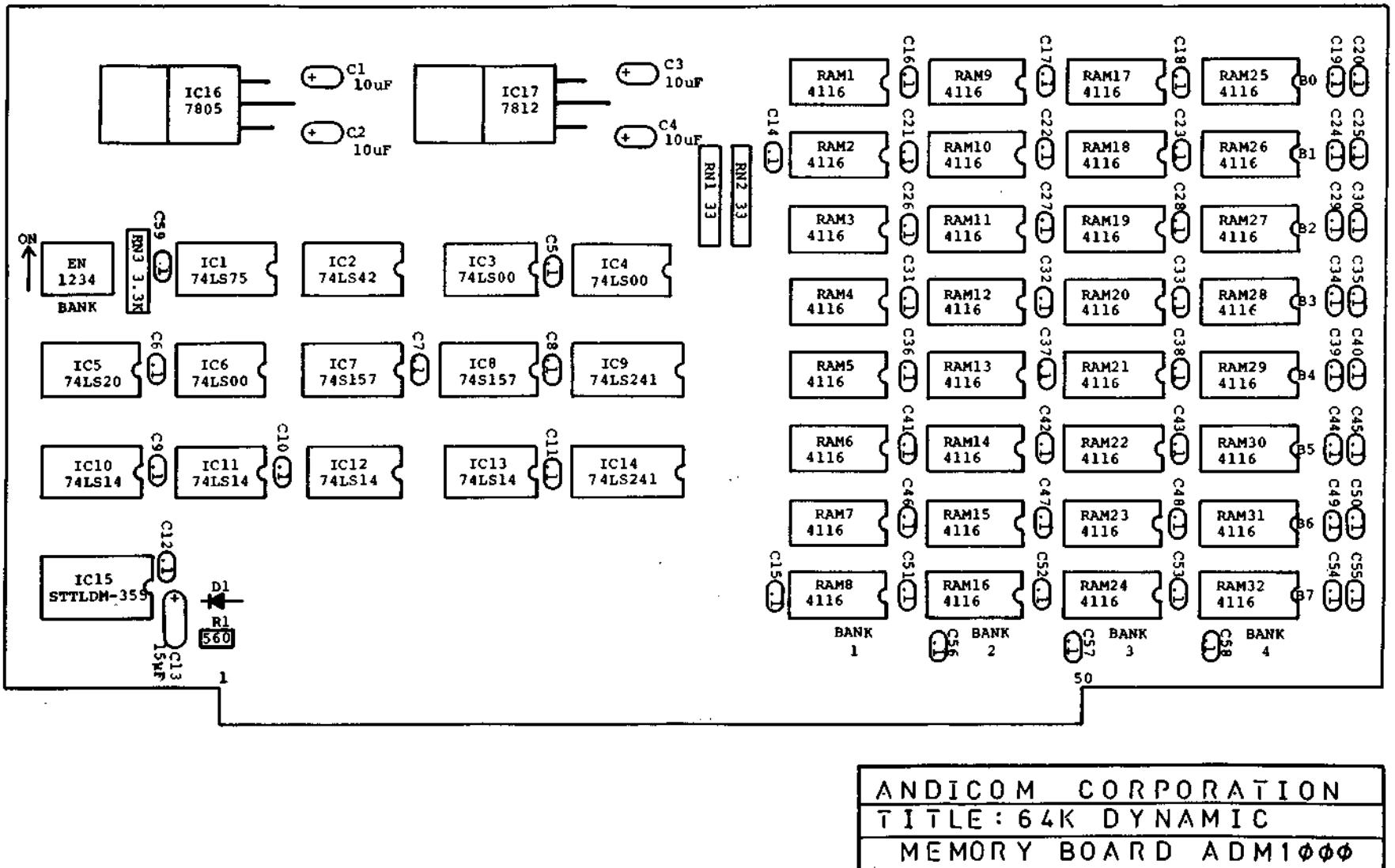
-6 SEE TABLE FOR RESISTORS AND CAPACITORS VALUES.

RN1, RN2	33
RN3	3.3K
R1	68Ø
C1-C4, C13	1Ø
C5-C12 C14-C55	Ø.1

S-100 BUS

ANDICOM CORPORATION
TITLE: 64K DYNAMIC RAM ADM100
DRAWING NO ACD500
DRAWN BY: K.TAM
CHECKED BY: W.LEUNG
JULY 1981

FIGURE 4: SCHEMATIC DIAGRAM OF DYNAMIC MEMORY BOARD



ANDICOM CORPORATION
TITLE: 64K DYNAMIC
MEMORY BOARD ADM1ΦΦΦ

FIGURE 5: DYNAMIC MEMORY BOARD LAYOUT

NEC Microcomputers, Inc.

NEC

μPD416
μPD416-1
μPD416-2
μPD416-3
μPD416-5

16384 x 1 BIT DYNAMIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The NEC μPD416 is a 16384 words by 1 bit Dynamic MOS RAM. It is designed for memory applications where very low cost and large bit storage are important design objectives.

The μPD416 is fabricated using a double-poly-layer N channel silicon gate process which affords high storage cell density and high performance. The use of dynamic circuitry throughout, including the sense amplifiers, assures minimal power dissipation.

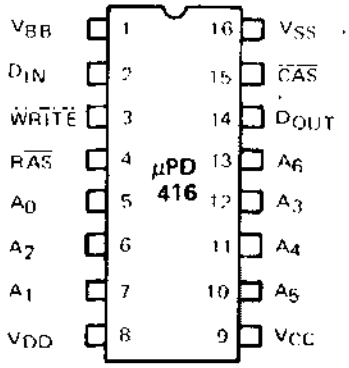
Multiplexed address inputs permit the μPD416 to be packaged in the standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is available in either ceramic or plastic. Noncritical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

FEATURES

- 16384 Words x 1 Bit Organization
- High Memory Density – 16 Pin Ceramic and Plastic Packages
- Multiplexed Address Inputs
- Standard Power Supplies +12V, -5V, +5V
- Low Power Dissipation; 462 mW Active (MAX), 40 mW Standby (MAX)
- Output Data Controlled by $\overline{CAS}$ and Unlatched at End of Cycle
- Read-Modify-Write, $\overline{RAS}$-only Refresh, and Page Mode Capability
- All Inputs TTL Compatible, and Low Capacitance
- 128 Refresh Cycles
- 5 Performance Ranges:

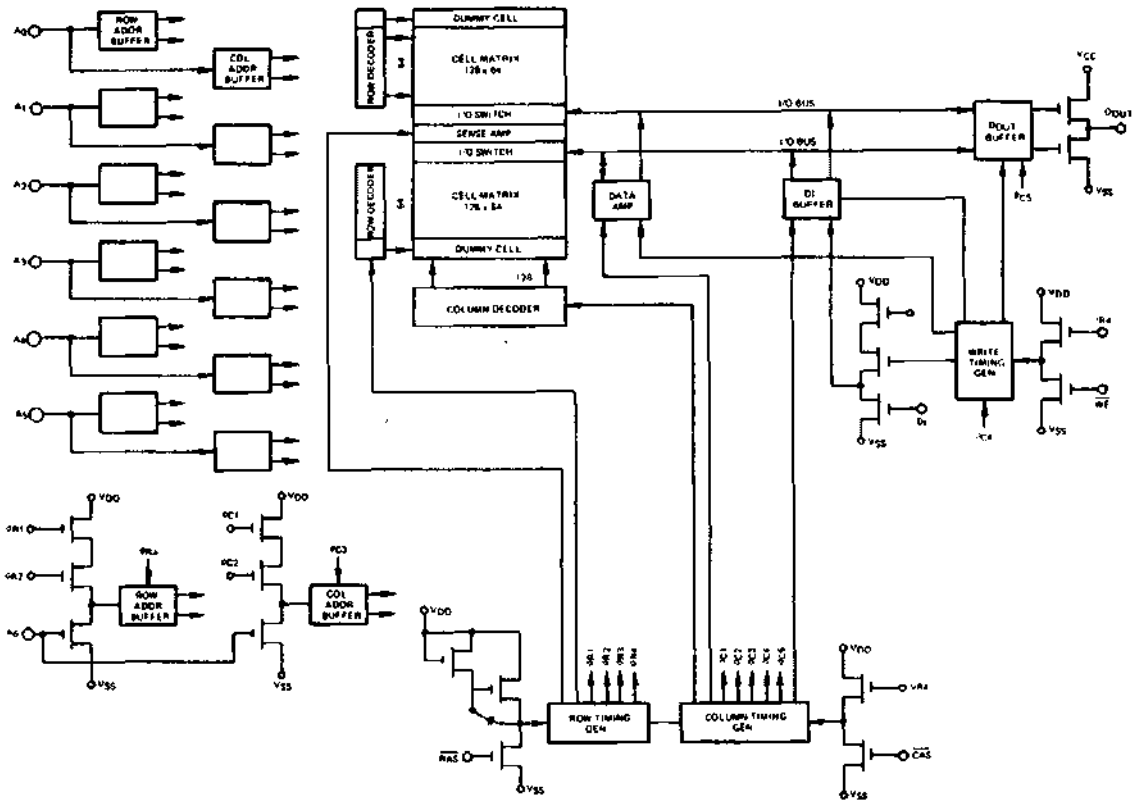
	ACCESS TIME	R/W CYCLE	RMW CYCLE
μPD416	300 ns	510 ns	575 ns
μPD416-1	250 ns	410 ns	465 ns
μPD416-2	200 ns	375 ns	375 ns
μPD416-3	150 ns	375 ns	375 ns
μPD416-5	120 ns	320 ns	320 ns

PIN CONFIGURATION



A_0-A_6	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write
V_{BB}	Power (-5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-55°C to +150°C
All Output Voltages ①	-0.5 to +20 Volts
All Input Voltages ①	-0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC}, V_{SS} ①	-0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC} ②	-1.0 to +15 Volts
Short Circuit Output Current	50 mA
Power Dissipation	1 Watt

Notes: ① Relative to V_{BB}
② Relative to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{BB} = -5V ± 10%, V_{CC} = +5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance (A_0-A_6), D_{IN}	C_{I1}		4	5	pF	
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}		8	10	pF	
Output Capacitance (D_{OUT})	C_O		5	7	pF	

AC CHARACTERISTICS

T_a = 0°C to +70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS										UNIT	TEST CONDITIONS
		μPD416		μPD416-1		μPD416-2		μPD416-3		μPD416-6			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	510		410		375		320		320		ns	③
Read-write cycle time	t_{RWC}	575		465		375		375		320		ns	③
Page mode cycle time	t_{PC}	330		275		225		170		160		ns	
Access time from $\overline{RAS}$	t_{RAC}		300		250		200		150		120	ns	④ ⑥
Access time from $\overline{CAS}$	t_{CAC}		200		165		135		100		80	ns	⑤ ⑥
Output buffer turn-off delay	t_{OFF}	0	80	0	60	0	50	0	40	0	35	ns	⑦
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	35	3	35	ns	②
$\overline{RAS}$ precharge time	t_{RP}	200		150		120		100		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	300	10,000	250	10,000	200	32,000	150	32,000	120	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	200		165		135		100		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	200	10,000	165	10,000	135	10,000	100	10,000	80	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	40	100	35	85	25	65	20	50	15	40	ns	⑧
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	-20		-20		-20		-20		0		ns	
Row address set-up time	t_{ASR}	0		0		0		0		0		ns	
Row address hold time	t_{RAH}	40		35		25		20		15		ns	
Column address set-up time	t_{ASC}	-10		-10		-10		-10		-10		ns	
Column address hold time	t_{CAH}	90		75		65		45		40		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	190		160		120		95		80		ns	
Read command set-up time	t_{RCS}	0		0		0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		0		0		ns	
Write command hold time	t_{WCH}	90		75		55		45		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	190		160		120		95		80		ns	
Write command pulse width	t_{WP}	90		75		55		45		40		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	120		85		70		50		50		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	120		85		70		50		50		ns	
Data-in set-up time	t_{DS}	0		0		0		0		0		ns	⑨
Data-in hold time	t_{DH}	90		75		55		45		40		ns	⑨
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	190		160		120		95		80		ns	
CAS precharge time (for page mode cycle only)	t_{CP}	120		100		80		60		60		ns	
Refresh period	t_{REF}		2		2		2		2		2	ms	
$\overline{WRITE}$ command set-up time	t_{WCS}	-20		-20		-20		-20		0		ns	⑩
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	140		125		95		70		60		ns	⑩
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	240		200		160		120		120		ns	⑩

Notes:

① AC measurements assume t_T = 5 ns.

② V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}

③ The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_a ≤ 70°C) is assured.

④ Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.

⑤ Assumes that $t_{RCD} > t_{RCD}$ (max).

⑥ Measured with a load equivalent to 2 TTL loads and 100 pF.

⑦ t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

⑧ Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}

⑨ These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

⑩ t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) $\geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

DC CHARACTERISTICS

T_a = 0°C to +70°C (1), V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Supply Voltage	V_{DD}	10.8	12.0	13.2	V	(2)
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	(2) (3)
Supply Voltage	V_{SS}	0	0	0	V	(2)
Supply Voltage	V_{BB}	− 4.5	−5.0	−5.5	V	(2)
Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7		7.0	V	(2)
Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	V_{IH}	2.4		7.0	V	(2)
Input Low (Logic 0) Voltage, all inputs	V_{IL}	− 1.0		0.8	V	(2)
Operating V_{DD} Current	I_{DD1}			35	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} Min. (4)
Standby V_{DD} Current	I_{DD2}			1.5	mA	$\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance
Refresh V_{DD} Current — All Speeds except μPD416-5	I_{DD3}			25	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = 375 ns (4)
Refresh V_{DD} Current — μPD416-5	I_{DD3}			27	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = 375 ns (4)
Page Mode V_{DD} Current	I_{DD4}			27	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = 225 ns (4)
Operating V_{CC} Current	I_{CC1}				μA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = 375 ns (5)
Standby V_{CC} Current	I_{CC2}	-10		10	μA	$\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance
Refresh V_{CC} Current	I_{CC3}	-10		10	μA	$\overline{RAS}$ cycling, $\overline{CAS}$ - V_{IHC}, t_{RC} = 375 ns
Page Mode V_{CC} Current	I_{CC4}				μA	$\overline{RAS}$ · V_{IL}, $\overline{CAS}$ cycling, t_{PC} 225 ns (5)
Operating V_{BB} Current	I_{BB1}			200	μA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} 375 ns
Standby V_{BB} Current	I_{BB2}			100	μA	$\overline{RAS}$ · V_{IHC}, D_{OUT} High Impedance
Refresh V_{BB} Current	I_{BB3}			200	μA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}, t_{RC} = 375 ns
Page Mode V_{BB} Current	I_{BB4}			200	μA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = 225 ns
Input Leakage (any input)	$I_{I(L)}$	-10		10	μA	V_{BB} = -5V, 0V ≤ V_{IN} ≤ +7V, all other pins not under test = 0V
Output Leakage	$I_{O(L)}$	-10		10	μA	D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V
Output High Voltage (Logic 1)	V_{OH}	2.4			V	I_{OUT} = -5 mA (3)
Output Low Voltage (Logic 0)	V_{OL}			0.4	V	I_{OUT} = 4.2 mA

Notes: (1) T_a is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and high power dissipation is permissible, however, provided AC operating parameters are met. See Figure 1 for derating curve.

(2) All voltages referenced to V_{SS}.

(3) Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

(4) I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. See Figures 2, 3 and 4 for I_{DD} limits at other cycle rates.

(5) I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.

DERATING CURVES

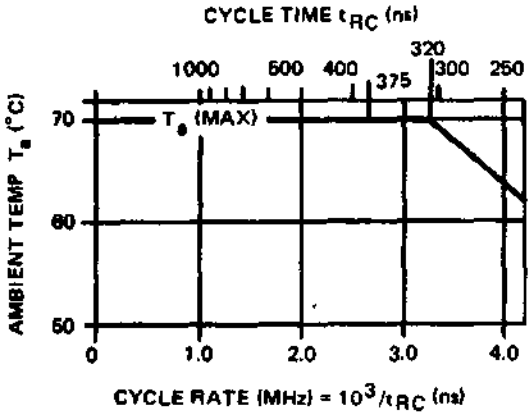


FIGURE 1

Maximum ambient temperature versus cycle rate for extended frequency operation. T_a (max) for operation at cycling rates greater than 2.66 MHz (t_{CYC} < 375 ns) is determined by T_a (max) [°C] = 70 – 9.0 x (cycle rate [MHz] –2.66). For μPD416-5, it is T_a (max) [°C] = 70 – 9.0 (cycle rate [MHz] – 3.125).

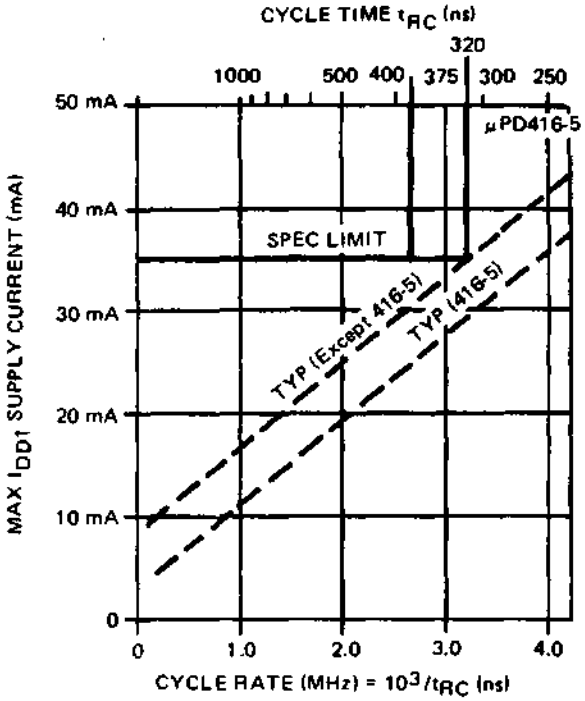


FIGURE 2

Maximum I_{DD1} versus cycle rate for device operation at extended frequencies.

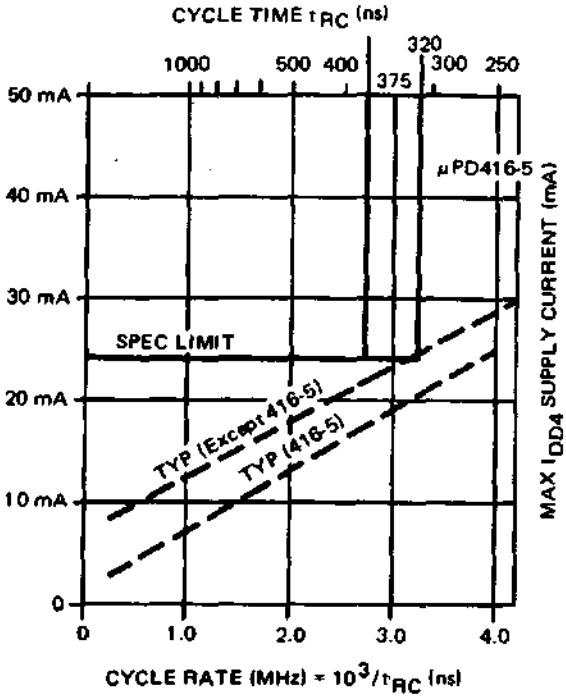


FIGURE 3

Maximum I_{DD3} versus cycle rate for device operation at extended frequencies.

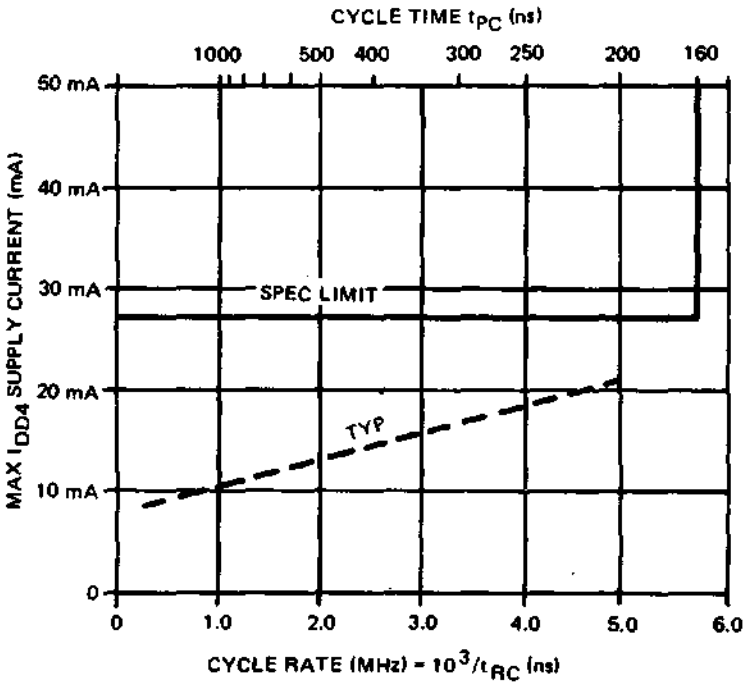
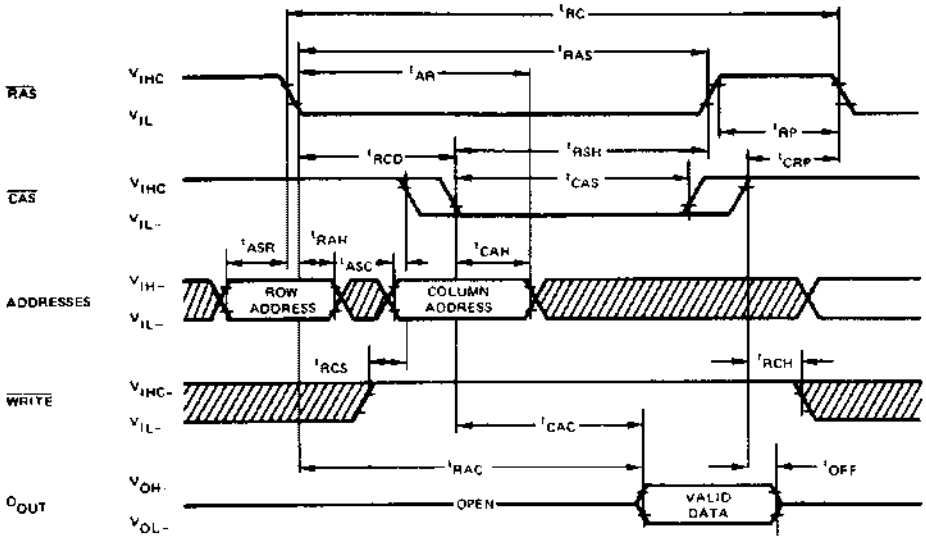


FIGURE 4

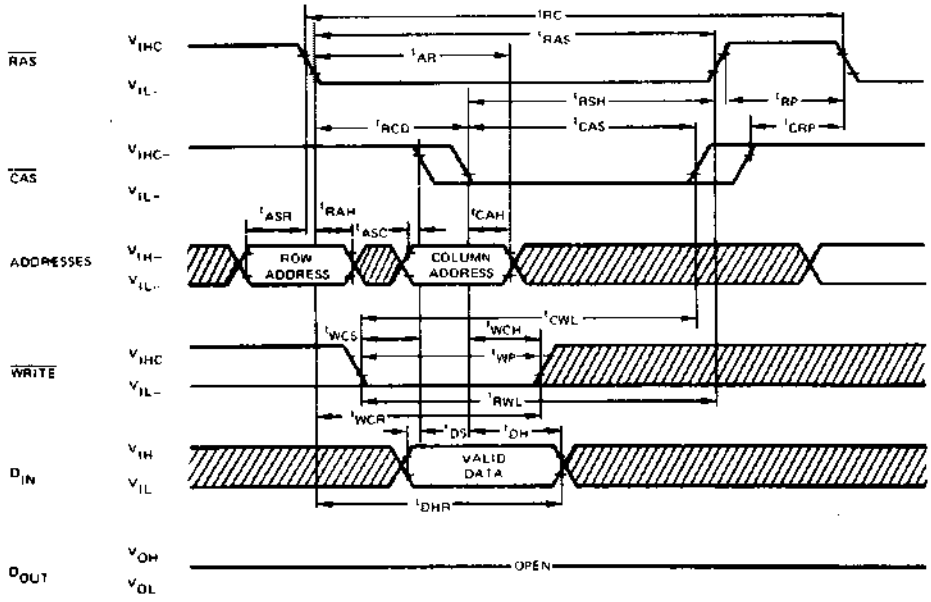
Maximum I_{DD4} versus cycle rate for device operation in page mode.

TIMING WAVEFORMS

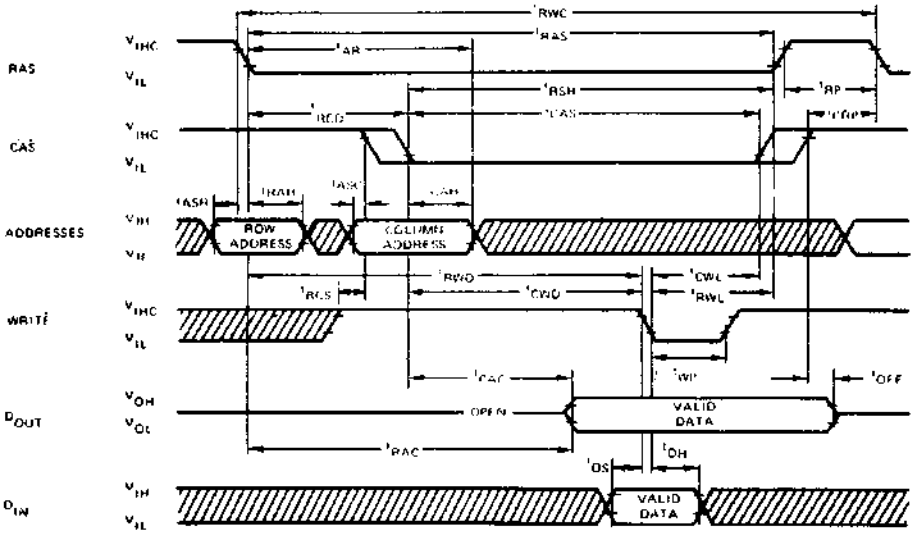
READ CYCLE



WRITE CYCLE

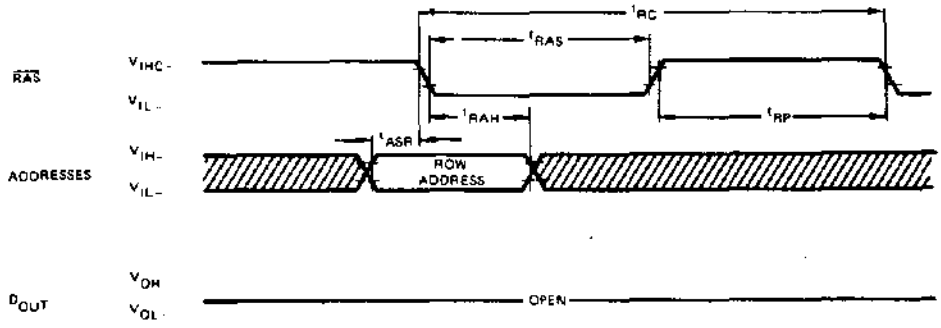


READ-WRITE/READ-MODIFY–WRITE CYCLE



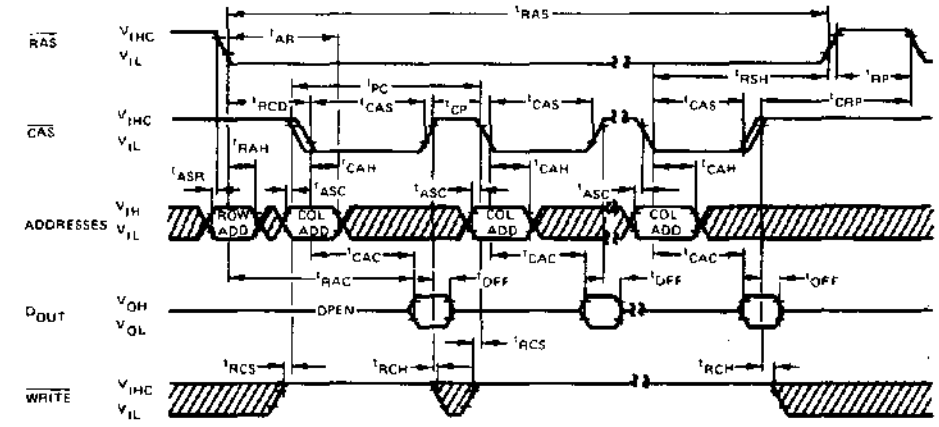
TIMING WAVEFORMS (CONT.)

"RAS-ONLY" REFRESH CYCLE

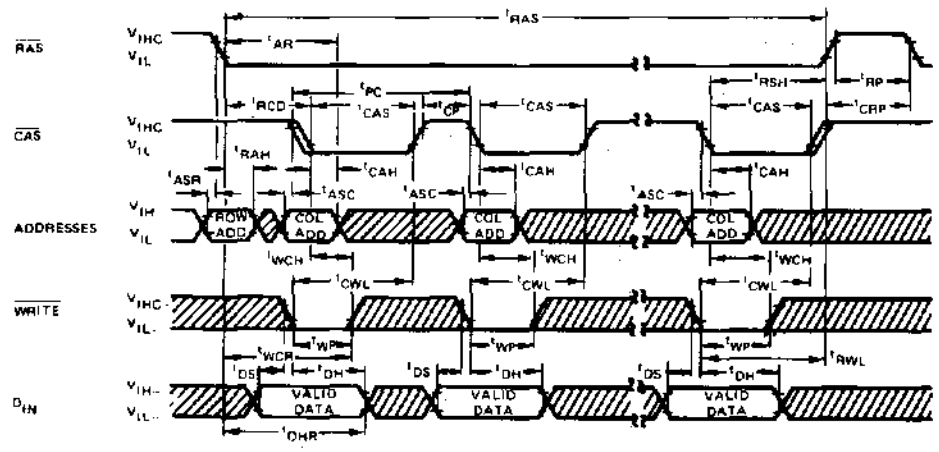


Note: CAS = V_{IHC}, WRITE = Don't Care

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



ADDRESSING

The 14 address bits required to decode 1 of 16,384 bit locations are multiplexed onto the 7 address pins and then latched on the chip with the use of the Row Address Strobe ($\overline{RAS}$), and the Column Address Strobe ($\overline{CAS}$). The 7 bit row address is first applied and $\overline{RAS}$ is then brought low. After the $\overline{RAS}$ hold time has elapsed, the 7 bit column address is applied and $\overline{CAS}$ is brought low. Since the column address is not needed internally until a time of t_{CRD} MAX after the row address, this multiplexing operation imposes no penalty on access time as long as $\overline{CAS}$ is applied no later than t_{CRD} MAX. If this time is exceeded, access time will be defined from $\overline{CAS}$ instead of $\overline{RAS}$.

DATA I/O

For a write operation, the input data is latched on the chip by the negative going edge of $\overline{WRITE}$ or $\overline{CAS}$, whichever occurs later. If $\overline{WRITE}$ is active before $\overline{CAS}$, this is an "early WRITE" cycle and data out will remain in the high impedance state throughout the cycle. For a READ, WRITE, OR READ-MODIFY-WRITE cycle, the data output will contain the data in the selected cell after the access time. Data out will assume the high impedance state anytime that $\overline{CAS}$ goes high.

PAGE MODE

The page mode feature allows the μPD416 to be read or written at multiple column addresses for the same row address. This is accomplished by maintaining a low on $\overline{RAS}$ and strobing the new column addresses with $\overline{CAS}$. This eliminates the setup and hold times for the row address resulting in faster operation.

REFRESH

Refresh of the memory matrix is accomplished by performing a memory cycle at each of the 128 row addresses every 2 milliseconds or less. Because data out is not latched, "$\overline{RAS}$ only" cycles can be used for simple refreshing operation.

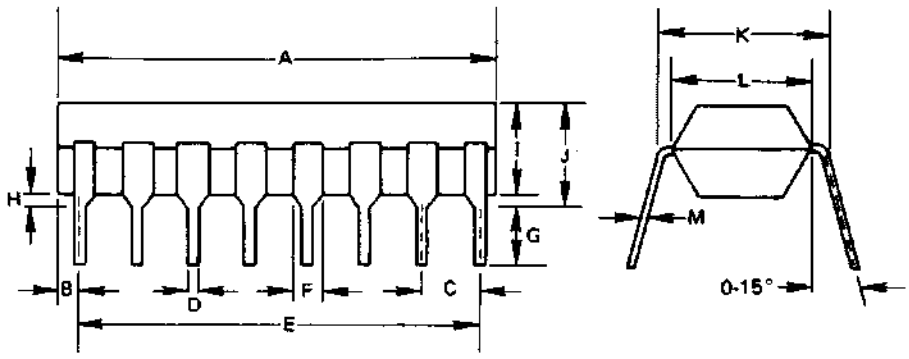
CHIP SELECTION

Either $\overline{RAS}$ and/or $\overline{CAS}$ can be decoded for chip select function. Unselected chip outputs will remain in the high impedance state.

POWER SEQUENCING

In order to assure long term reliability, V_{BB} should be applied first during power up and removed last during power down.

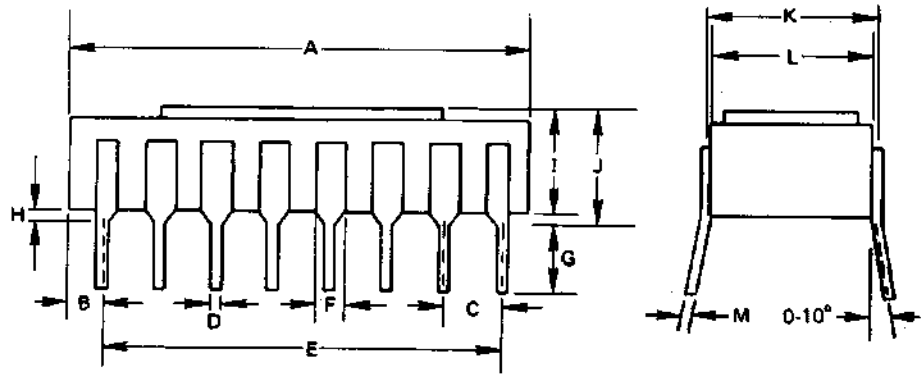
PACKAGE OUTLINE μPD416C



(Plastic)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

μPD416D



(Ceramic)

ITEM	MILLIMETERS	INCHES
A	20.5 MAX.	0.81 MAX.
B	1.36	0.05
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	3.5 MIN.	0.14 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.20 MAX.
K	7.6	0.30
L	7.3	0.29
M	0.27	0.01

3.0 INPUT-OUTPUT BOARD

GENERAL INFORMATION

The Nabu input/output board AIO-1100 provides two serial input/output ports, one parallel output port, and six programmable 16 bit timers. The board is S-100 bus compatible and all data lines are buffered with line drivers to increase current drive capability.

The serial ports are implemented by two 8251 programmable communication interfaces (PCI's), and each has separate software programmable baud rate selection. Line drivers and receivers are provided for EIA RS-232C standard signals. The parallel output port is a simple 8-bit, D-type latch; which can be easily programmed to interface with any parallel printer.

The six programmable counters are implemented by two 8253 programmable interval timers (PIT's). Two of the six counters are configured as baud rate generators for the two serial ports, while the remaining four counters may be used as desired by the user (eg. rate generators, real time clocks, etc.).

In the Nabu 1100 System, input and output functions are done by polling through software interrogation loops. However, the I/O board is also capable of operating in an interrupt driven system. The board provides a selectable interrupt vector which allows the programmer to locate the interrupt service routine anywhere in memory.

SPECIFIC FEATURES

Serial Ports

Full duplex RS-232C serial data communication with two external devices is permitted via the two programmable communication interfaces. The PCI features parity, overrun and framing error detection. As well, there is a choice of 1, 1 1/2, or 2 stop bits with false start bit detection, and modem control signals $\overline{DSR}$, $\overline{DTR}$, $\overline{CTS}$, and $\overline{RTS}$. The baud rates of the serial ports are software selectable and are available in a range from 110 to 9600.

In the Nabu 1100 System, connector J2 is assigned as the main console device. The associated PCI (U6) is programmed for the asynchronous transmit/receive mode, with one stop-bit, no parity, eight data bits, a 16x transmitter clock, and a baud rate of 9600.

Connector J1 is assigned as the list device in the system, which is normally a NEC Spinwriter. The associated PCI (U3) is programmed the same way as U6; the only exception being the baud rate is 1200. By connecting the reverse channel signal from the NEC printer to $\overline{CTS}$ of U3, no communication protocol is needed. However, if an 8251A is used in U3, a problem of repeating characters will occur whenever the reverse channel becomes active. This problem can be overcome by making use of $\overline{DSR}$ on U3 and performing a slight modification in the operating system (which will not be discussed here).

The port addresses are assigned as follows:

Device	Connector	PCI	Port Address	
Console	J2	U6	Status register	82H
			Data register	83H
List	J1	U3	Status register	80H
			Data register	81H

The two 26-pin header strips (J1 and J2) are connected through two ribbon cables to the RS-232C connectors located on the back of the system. The connector associated with J1 is located above that associated with J2.

The pins are assigned as follows:

J1 or J2 Pin Number	Pin Name	Data Direction
2	RXD	Input
3	TXD	Output
4	$\overline{CTS}$	Input
5	$\overline{RTS}$	Output
6	$\overline{DTR}$	Output
7	GND	-
20	$\overline{DSR}$	Input

The pin numbers of the rear panel DB connector are the same as those for J1 or J2.

Jumpers JP-1 through JP-4 (on pins 6, 5, 4, and 20 respectively on connector J2) are normally not installed, since none of these modem control signals are used by the main console. However, in order for data transmission, the resistor R1 must be present to make $\overline{CTS}$ active.

Jumpers JP-5 through JP-8 (on pins 6, 5, 4 and 20 respectively on connector J1) are factory installed for interfacing to the NEC Spinwriter.

Parallel Ports

One parallel output port is available from J3 to the user, and is normally used to interface to a parallel printer, if needed. It is assigned the address 8DH in the Nabu 1100 System. The interface cable to a Centronics parallel printer would be wired as follows:

Signals	J3 Pin Number		Centronics Printer Pin #
D0	1	---------->	2
D1	2	---------->	3
D2	3	---------->	4
D3	4	---------->	5
D4	5	---------->	6
D5	6	---------->	7
D6	7	---------->	8
DATA STROBE	8	---------->	1
BUSY	9	<----------	11
GND	22	<---------->	16

A parallel input port is available as an option. It uses connector J4 and is assigned the same address as the parallel output port.

Programmable Timers

Six programmable 16-bit counters are available from the two PIT's (U18 and U20). Two 16-bit counters from U18 are used as baud rate generators for the two serial ports. They are software programmable, and the baud rate can be selected to suit each user's requirements.

The four remaining counters are not used in the Nabu 1100 System. They are available to the user (through wirewrapping) for implementing a real time clock, which will be discussed in the next section.

The address assignments for the timer are as follows:

8253 PIT	Counter	Address	Function
U20	0	84H	Available to the user
	1	85H	
	2	86H	
	Control register	87H	
U18	0	88H	
	1	89H	Clock for List PCI
	2	8AH	Clock for console PCI
	Control register	8BH	

For the timers used as baud rate generators, the following table relates the programmed count to the generated baud rate:

Baud Rate	Programmed Count
110	1136H
300	0417H
600	0208H
1200	0104H
2400	0052H
4800	0026H
9600	0013H

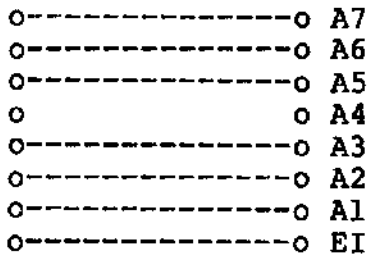
NOTE: The PIT must be programmed for mode 3 operation with binary coded decimal (BCD) counter format for these values.

Jumper Connections

Four jumpers located near the middle of the board are used for setting the board address. They are set to 80H for the Nabu 1100 System, by installing a jumper at A7.

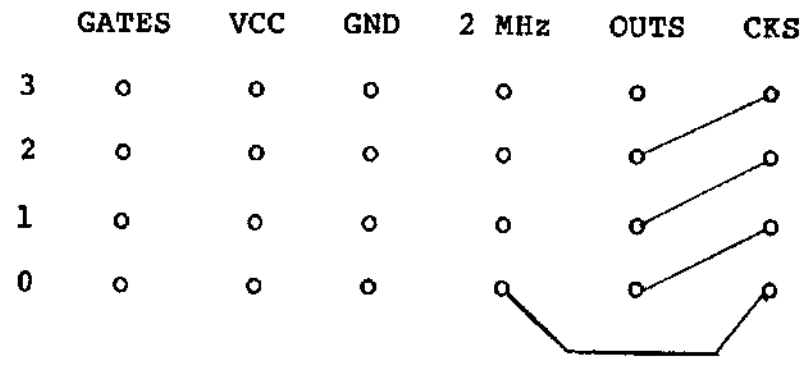
NOTE: With jumper means logic one.

The eight jumpers located in the lower right hand corner of the board are used to establish an interrupt capability on the I/O board. The top seven jumper spaces are used to set the interrupt vector, while the bottom space enables the interrupt. Interrupts are not used in the input/output scheme for the Nabu 1100 system. However, the board is preset to enable interrupts with the interrupt vector set to 10H for future expansion to a multi-user system. Thus, the standard board is shipped with interrupt jumpers installed, as shown:

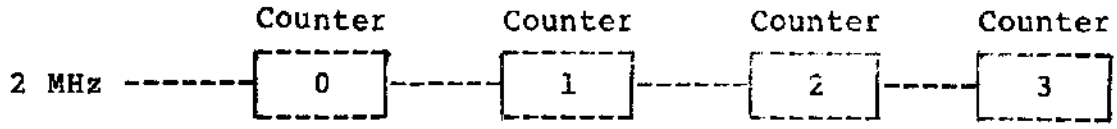


NOTES: 1) Interrupt vector setting: without jumper means logic one.
2) A0 is always logic zero.
3) EI setting: with jumper means enable.

The 24-pin wirewrap pad (located above the board base address setting jumpers), is used for interconnection of the timers. A connection for a real time clock implementation is shown below:



The equivalent block diagram is:



Counters #0 and 1 can be programmed to be a frequency divider so that the output of Counter #1 is a 1 Hz clock (1 second period). Counters #2 and 3 are used to accumulate the count. The counter contents can then be read by the CPU to determine the time.

By connecting the timer's output to the Interrupt Request pin of the CPU, the timer can be programmed to interrupt the CPU at a preset time. Detailed instructions on the configuration of the 8253 PIT are provided in the manufacturer's data sheets.

NABU AIO-1100 INPUT/OUTPUT BOARD
PARTS LIST

Integrated Circuits:

U1, U4	1488	RS232 hex driver
U2, U5	1489	RS232 hex receiver
U3	8251	Intel programmable communication interface
U6	8251A	Intel programmable communication interface (improved version)
U7, U12	74LS244	Octal buffer/line-driver with 3-state outputs
U8, U9	74LS38	Quadruple 2-input positive-NAND buffer with open-collector outputs
U10, U11	74LS273	Octal D-type flip-flop
U13-U16, U29	74LS00	Quadruple 2-input NAND
U17, U26	74LS04	Hex inverter
U18, U20	8253	Intel programmable interval timer
U19, U27-U28, U31-U33	74LS367	Hex bus driver
U21, U25	74LS32	Quadruple 2-input OR
U22	74LS136	Quad exclusive-OR with open-collector outputs
U23	74LS139	Dual 2-to-4-line decoder/demultiplexer
U24	74LS10	Triple 3-input NAND
U30	74LS74	Dual D-type positive-edge-triggered flip-flop with preset and clear
U34	7812	12 V positive voltage regulator
U35	7912	12 V negative voltage regulator
U36, U37	7805	5 V positive voltage regulator

Capacitors:

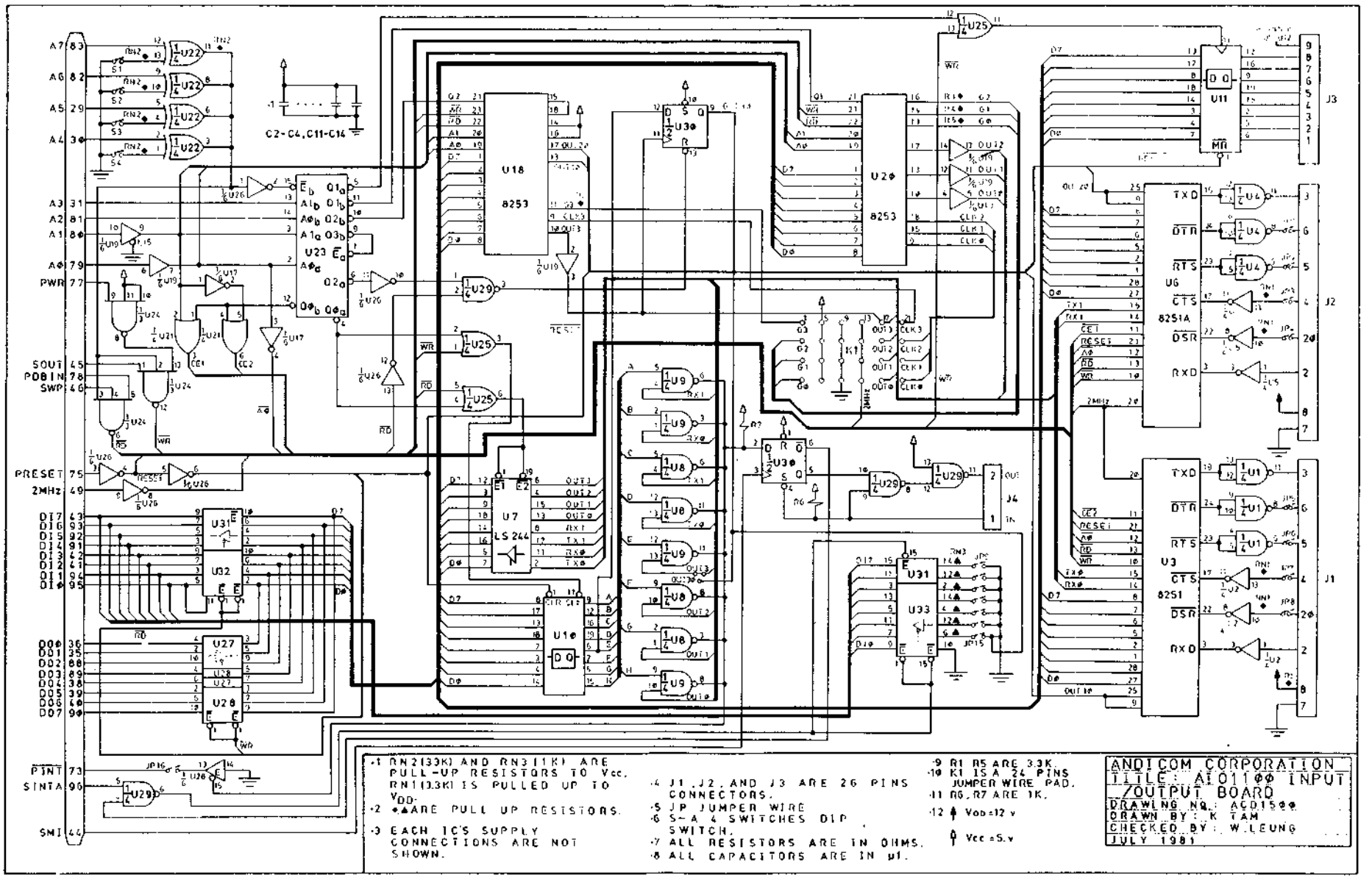
C1, C5-C10	10 µF 35 V tantalum electrolytic
C2-C4, C11-C14	0.1 µF

Resistors:

R1-R5	3.3 kΩ
R6, R7	1 kΩ
RN1, RN2	3.3 kΩ
RN3	1 kΩ

Quantity	Description
14	14 pin IC socket
7	16 pin IC socket
4	20 pin IC socket
4	28 pin IC socket

Quantity	Description
1	delta 1-630-0.50 dual TO-220 heatsink
1	4 position dip switch
3	26 pin right angle pin connector
4	2 pin straight pin connector
6	#6-32 x 3/8" machine screw
6	#6-32 nuts
1	p.c. board



·1 RN2(33K) AND RN3(1K) ARE PULL-UP RESISTORS TO Vcc. RN1(3.3K) IS PULLED UP TO V_{DD}.
·2 ◆▲ARE PULL UP RESISTORS.
·3 EACH IC'S SUPPLY CONNECTIONS ARE NOT SHOWN.
·4 J1, J2, AND J3 ARE 26 PINS CONNECTORS.
·5 JP JUMPER WIRE
·6 S-A 4 SWITCHES DIP SWITCH.
·7 ALL RESISTORS ARE IN OHMS.
·8 ALL CAPACITORS ARE IN µf.
·9 R1 R5 ARE 3.3K.
·10 K1 IS A 24 PINS JUMPER WIRE PAD.
·11 R6, R7 ARE 1K.
·12 Vod=12 v
Vcc=5.v

ANDICOM CORPORATION
TITLE : AI011ØØ INPUT /OUTPUT BOARD
DRAWING NO. : ACD15ØØ
DRAWN BY : K TAM
CHECKED BY : W.LEUNG
JULY 1981

FIGURE 6: SCHEMATIC DIAGRAM OF INPUT/OUTPUT BOARD

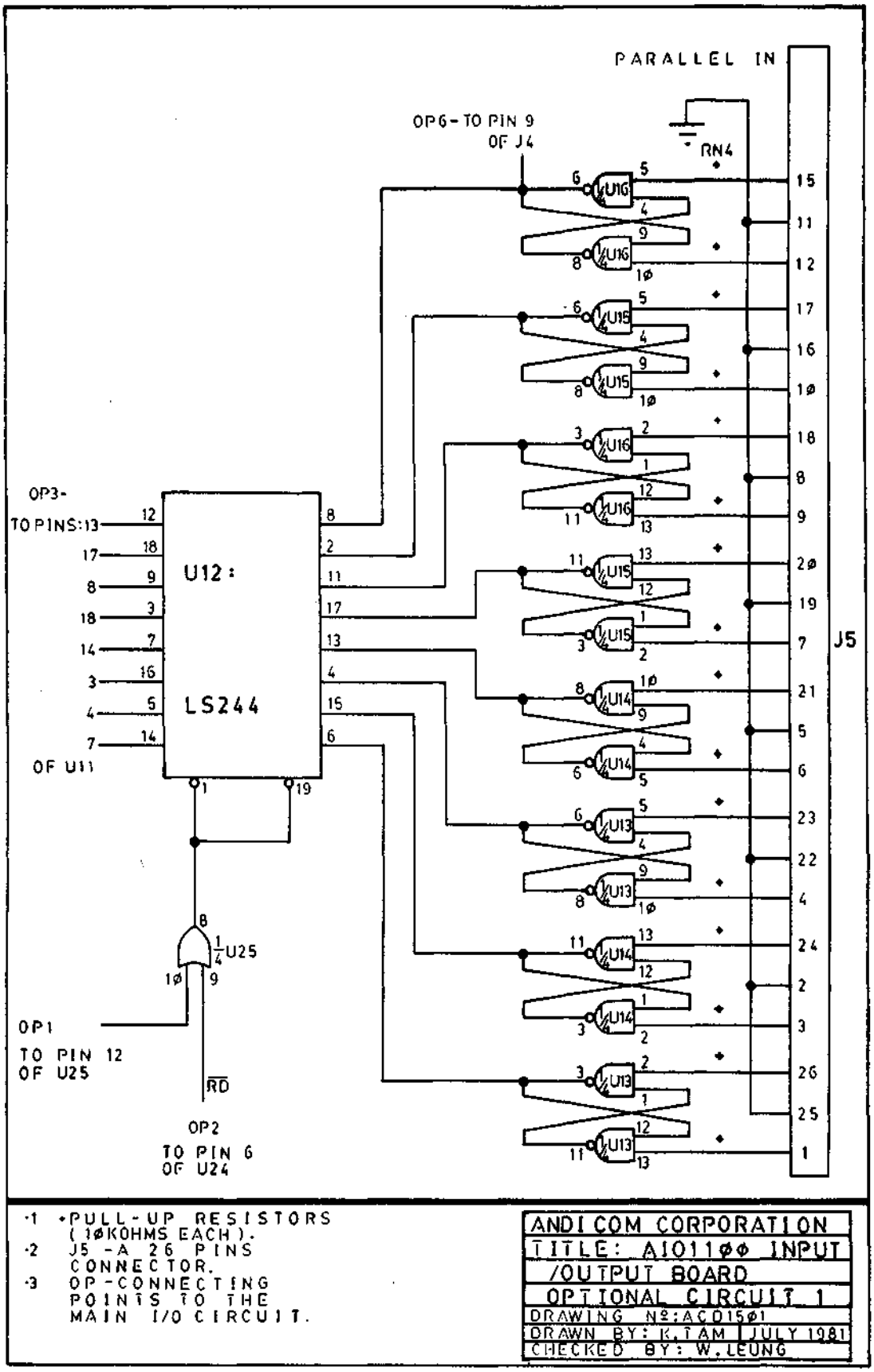


FIGURE 7: INPUT/OUTPUT BOARD OPTIONAL CIRCUIT #1

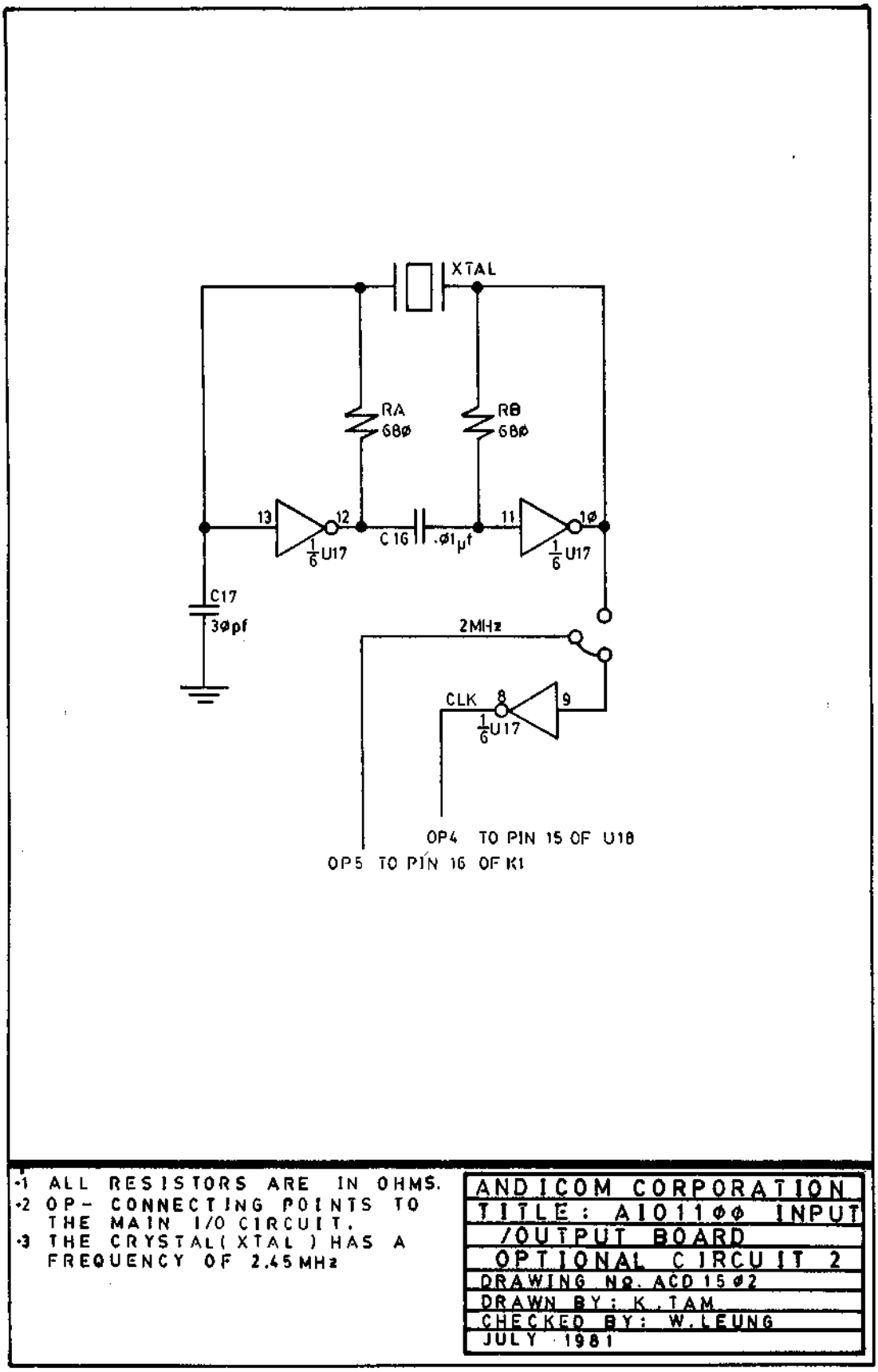


FIGURE 8: INPUT/OUTPUT BOARD OPTIONAL CIRCUIT #2

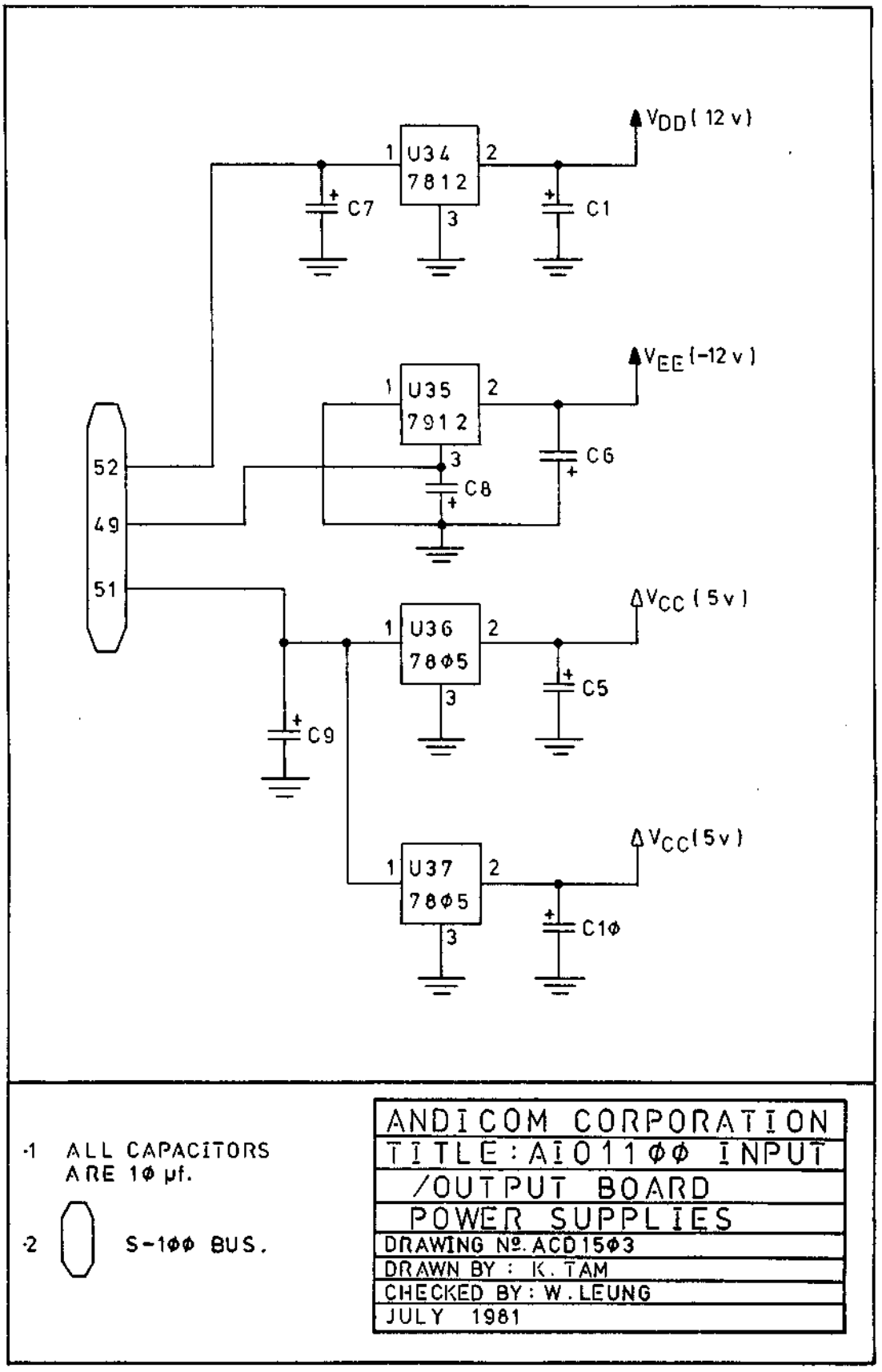
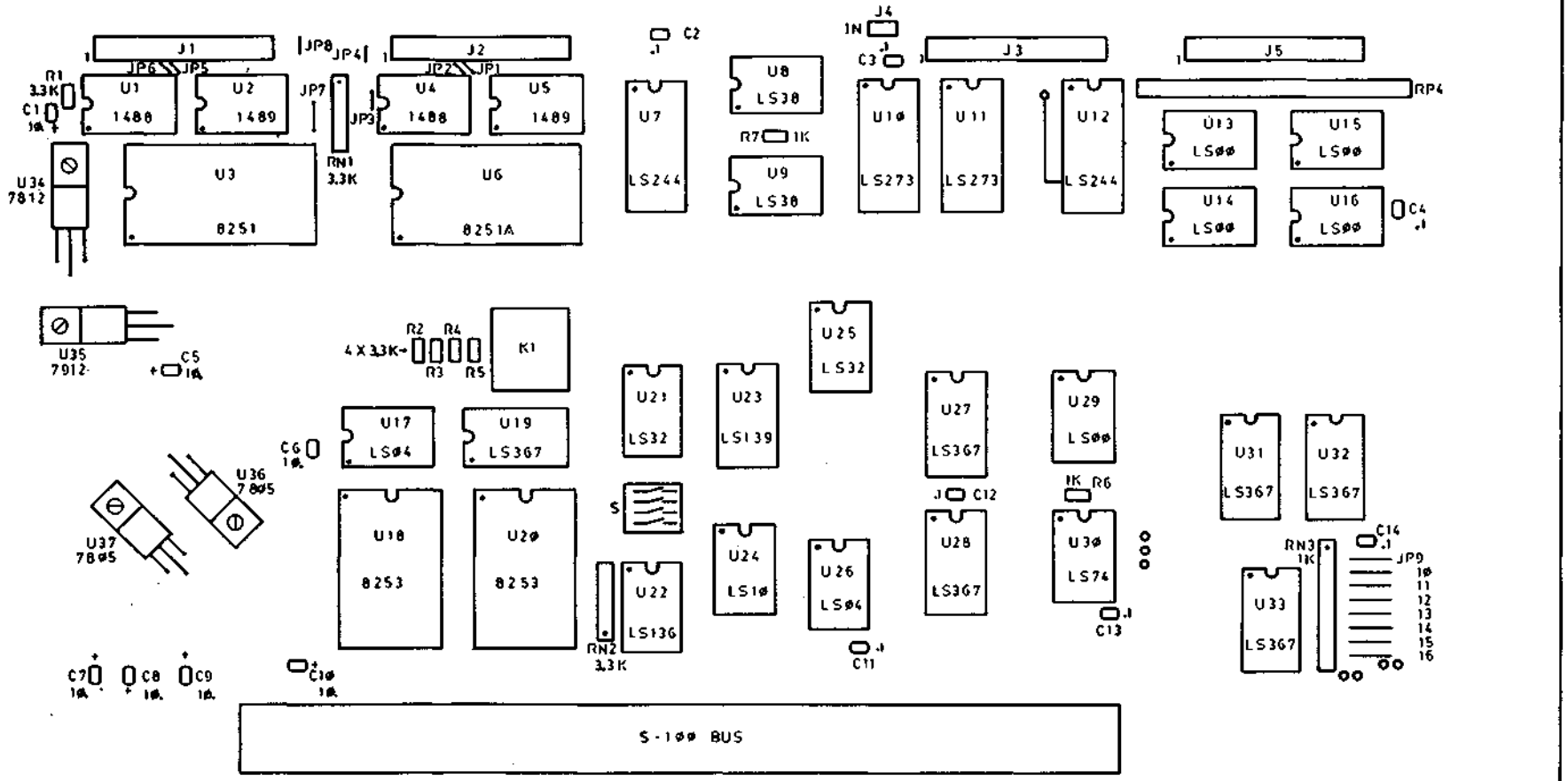


FIGURE 9: INPUT/OUTPUT BOARD POWER SUPPLY



NOTE: ALL RESISTOR VALUES ARE IN OHMS.
ALL CAPACITOR VALUES ARE IN MICROFARADS.

ANDICOM CORPORATION
TITLE: AIO1100 INPUT/OUTPUT BOARD COMPONENTS LAYOUT
DRAWING N°:ACD1504
DRAWN BY: K. TAM
CHECKED BY: W. LEUNG
JULY 1981

8251A/S2657
PROGRAMMABLE COMMUNICATION INTERFACE

- **Synchronous and Asynchronous Operation**
- **Synchronous 5-8 Bit Characters; Internal or External Character Synchronization; Automatic Sync Insertion**
- **Asynchronous 5-8 Bit Characters; Clock Rate—1, 16 or 64 Times Baud Rate; Break Character Generation; 1, 1½, or 2 Stop Bits; False Start Bit Detection; Automatic Break Detect and Handling**
- **Synchronous Baud Rate — DC to 64K Baud**
- **Asynchronous Baud Rate — DC to 19.2K Baud**
- **Full Duplex, Double Buffered, Transmitter and Receiver**
- **Error Detection — Parity, Overrun and Framing**
- **Fully Compatible with 8080/8085 CPU**
- **28-Pin DIP Package**
- **All Inputs and Outputs are TTL Compatible**
- **Single +5V Supply**
- **Single TTL Clock**

The Intel® 8251A is the enhanced version of the industry standard, Intel® 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART), designed for data communications with Intel's new high performance family of microprocessors such as the 8085. The 8251A is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPTY. The chip is constructed using N-channel silicon gate technology.

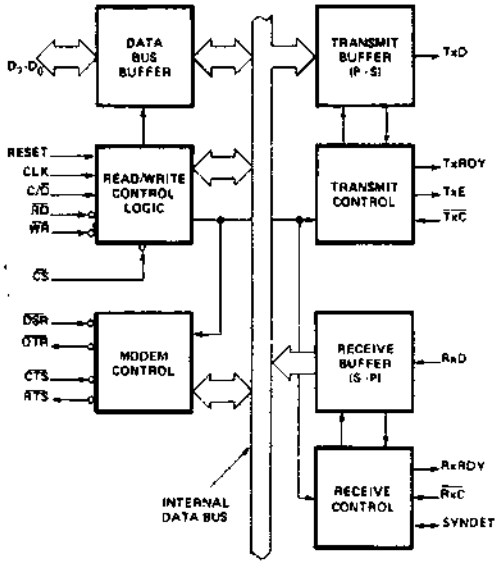


Figure 1. Block Diagram

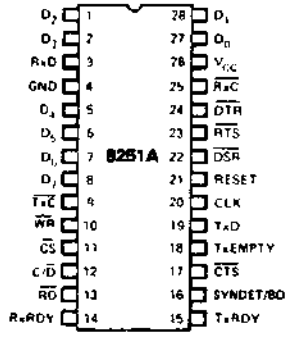


Figure 2. Pin Configuration

FEATURES AND ENHANCEMENTS

8251A is an advanced design of the industry standard USART, the Intel® 8251. The 8251A operates with an extended range of Intel microprocessors that includes the new 8085 CPU and maintains compatibility with the 8251. Familiarization time is minimal because of compatibility and involves only knowing the additional features and enhancements, and reviewing the AC and DC specifications of the 8251A.

The 8251A incorporates all the key features of the 8251 and has the following additional features and enhancements:

- 8251A has double-buffered data paths with separate I/O registers for control, status, Data In, and Data Out, which considerably simplifies control programming and minimizes CPU overhead.
- In asynchronous operations, the Receiver detects and handles "break" automatically, relieving the CPU of this task.
- A refined Rx initialization prevents the Receiver from starting when in "break" state, preventing unwanted interrupts from a disconnected USART.
- At the conclusion of a transmission, TxD line will always return to the marking state unless SBRK is programmed.
- Tx Enable logic enhancement prevents a Tx Disable command from halting transmission until all data previously written has been transmitted. The logic also prevents the transmitter from turning off in the middle of a word.
- When External Sync Detect is programmed, Internal Sync Detect is disabled, and an External Sync Detect status is provided via a flip-flop which clears itself upon a status read.
- Possibility of false sync detect is minimized by ensuring that if double character sync is programmed, the characters be contiguously detected and also by clearing the Rx register to all ones whenever Enter Hunt command is issued in Sync mode.
- As long as the 8251A is not selected, the $\overline{RD}$ and $\overline{WR}$ do not affect the internal operation of the device.
- The 8251A Status can be read at any time but the status update will be inhibited during status read.
- The 8251A is free from extraneous glitches and has enhanced AC and DC characteristics, providing higher speed and better operating margins.
- Synchronous Baud rate from DC to 64K.
- Fully compatible with Intel's new industry standard, the MCS-85.

AFN-01573B

FUNCTIONAL DESCRIPTION

General

The 8251A is a Universal Synchronous/Asynchronous Receiver/Transmitter designed specifically for the 80/85 Microcomputer Systems. Like other I/O devices in a Microcomputer System, its functional configuration is programmed by the system's software for maximum flexibility. The 8251A can support virtually any serial data technique currently in use (including IBM "bi-sync").

In a communication environment an interface device must convert parallel format system data into serial format for transmission and convert incoming serial format data into parallel system data for reception. The interface device must also delete or insert bits or characters that are functionally unique to the communication technique. In essence, the interface should appear "transparent" to the CPU, a simple input or output of byte-oriented system data.

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the 8251A to the system Data Bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions of the CPU. Control words, Command words and Status information are also transferred through the Data Bus Buffer. The command status and data in, and data out are separate 8-bit registers to provide double buffering.

This functional block accepts inputs from the system Control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register that store the various control formats for the device functional definition.

RESET (Reset)

A "high" on this input forces the 8251A into an "Idle" mode. The device will remain at "Idle" until a new set of control words is written into the 8251A to program its functional definition. Minimum RESET pulse width is 6 t_{CY} (clock must be running).

CLK (Clock)

The CLK input is used to generate internal device timing and is normally connected to the Phase 2 (TTL) output of the 8224 Clock Generator. No external inputs or outputs are referenced to CLK but the frequency of CLK must be greater than 30 times the Receiver or Transmitter data bit rates.

$\overline{WR}$ (Write)

A "low" on this input informs the 8251A that the CPU is writing data or control words to the 8251A.

$\overline{RD}$ (Read)

A "low" on this input informs the 8251A that the CPU is reading data or status information from the 8251A.

C/$\overline{D}$ (Control/Data)

This input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the 8251A that the word on the Data Bus is either a data character, control word or status information.
1 = CONTROL/STATUS 0 = DATA

$\overline{CS}$ (Chip Select)

A "low" on this input selects the 8251A. No reading or writing will occur unless the device is selected. When $\overline{CS}$ is high, the Data Bus in the float state and $\overline{RD}$ and $\overline{WR}$ will have no effect on the chip.

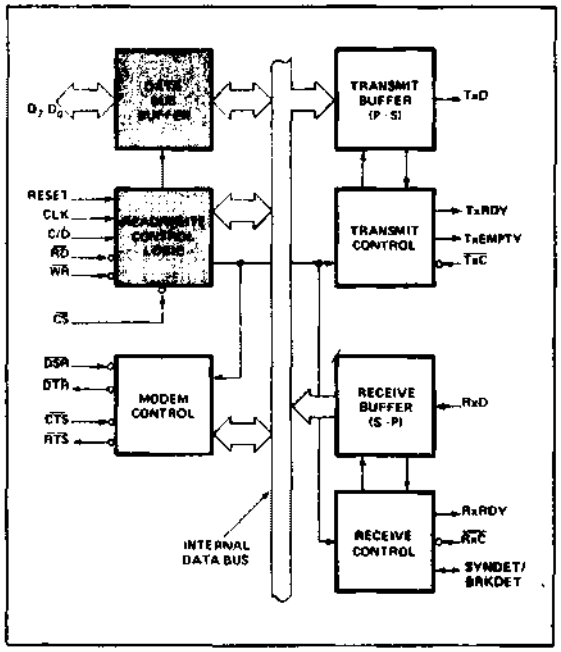


Figure 3. 8251A Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	8251A DATA → DATA BUS
0	1	0	0	DATA BUS → 8251A DATA
1	0	1	0	STATUS → DATA BUS
1	1	0	0	DATA BUS → CONTROL
X	1	1	0	DATA BUS → 3-STATE
X	X	X	1	DATA BUS → 3-STATE

Modem Control

The 8251A has a set of control inputs and outputs that can be used to simplify the interface to almost any Modem. The Modem control signals are general purpose in nature and can be used for functions other than Modem control, if necessary.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input signal is a general purpose, 1-bit inverting input port. Its condition can be tested by the CPU using a Status Read operation. The $\overline{DSR}$ input is normally used to test Modem conditions such as Data Set Ready.

$\overline{DTR}$ (Data Terminal Ready)

The $\overline{DTR}$ output signal is a general purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{DTR}$ output signal is normally used for Modem control such as Data Terminal Ready or Rate Select.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output signal is a general purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{RTS}$ output signal is normally used for Modem control such as Request to Send.

$\overline{CTS}$ (Clear to Send)

A "low" on this input enables the 8251A to transmit serial data if the Tx Enable bit in the Command byte is set to a "one." If either a Tx Enable off or $\overline{CTS}$ off condition occurs while the Tx is in operation, the Tx will transmit all the data in the USART, written prior to Tx Disable command before shutting down. On the 8251A/S2657 if $\overline{CTS}$ off or Tx Enable off condition occurs before the last character written appears in the serial bit stream, that character will be transmitted again upon $\overline{CTS}$ on or Tx Enable on condition.

Transmitter Buffer

The Transmitter Buffer accepts parallel data from the Data Bus Buffer, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin on the falling edge of $\overline{TxC}$. The transmitter will begin transmission upon being enabled if $\overline{CTS}$ = 0. The TxD line will be held in the marking state immediately upon a master Reset or when Tx Enable/$\overline{CTS}$ off or TxEMPTY.

Transmitter Control

The transmitter Control manages all activities associated with the transmission of serial data. It accepts and issues signals both externally and internally to accomplish this function.

TxRDY (Transmitter Ready)

This output signals the CPU that the transmitter is ready to accept a data character. The TxRDY output pin can be used as an interrupt to the system, since it is masked by Tx Disabled, or, for Polled operation, the CPU can check TxRDY using a Status Read operation. TxRDY is automatically reset by the leading edge of $\overline{WR}$ when a data character is loaded from the CPU.

Note that when using the Polled operation, the TxRDY status bit is *not* masked by Tx Enabled, but will only indicate the Empty/Full Status of the Tx Data Input Register.

TxE (Transmitter Empty)

When the 8251A has no characters to transmit, the TxEMPTY output will go "high". It resets automatically upon receiving a character from the CPU if the transmitter is enabled. TxEMPTY can be used to indicate the end of a transmission mode, so that the CPU "knows" when to "turn the line around" in the half-duplexed operational mode.

In SYNChronous mode, a "high" on this output indicates that a character has not been loaded and the SYNC character or characters are about to be or are being transmitted automatically as "fillers". TxEMPTY does not go low when the SYNC characters are being shifted out.

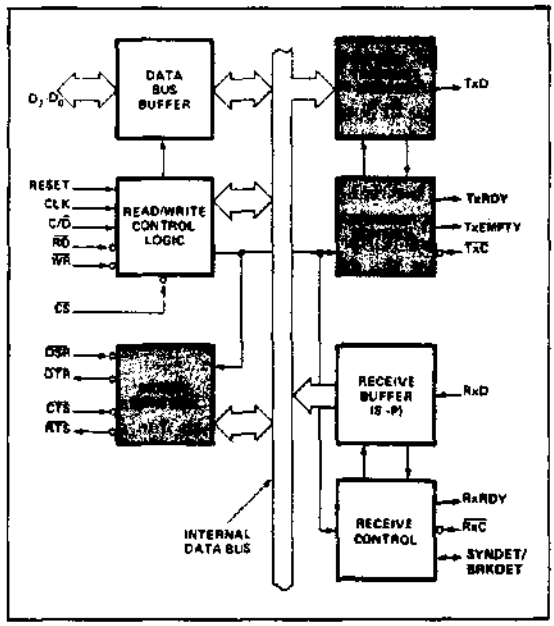


Figure 4. 8251A Block Diagram Showing Modem and Transmitter Buffer and Control Functions

$\overline{TxC}$ (Transmitter Clock)

The Transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous transmission mode, the Baud Rate (1x) is equal to the $\overline{TxC}$ frequency. In Asynchronous transmission mode the baud rate is a fraction of the actual $\overline{TxC}$ frequency. A portion of the mode instruction selects this factor; it can be 1, 1/16 or 1/64 the $\overline{TxC}$.

For Example:

If Baud Rate equals 110 Baud,
$\overline{TxC}$ equals 110 Hz (1x)
$\overline{TxC}$ equals 1.76 kHz (16x)
$\overline{TxC}$ equals 7.04 kHz (64x).

The falling edge of $\overline{TxC}$ shifts the serial data out of the 8251A.

Receiver Buffer

The Receiver accepts serial data, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU. Serial data is input to RxD pin, and is clocked in on the rising edge of $\overline{RxC}$.

Receiver Control

This functional block manages all receiver-related activities which consist of the following features:

The RxD initialization circuit prevents the 8251A from mistaking an unused input line for an active low data line in the "break condition". Before starting to receive serial characters on the RxD line, a valid "1" must first be detected after a chip master Reset. Once this has been determined, a search for a valid low (Start bit) is enabled. This feature is only active in the asynchronous mode, and is only done once for each master Reset.

The False Start bit detection circuit prevents false starts due to a transient noise spike by first detecting the falling edge and then strobing the nominal center of the Start bit (RxD = low).

The Parity Toggle F/F and Parity Error F/F circuits are used for parity error detection and set the corresponding status bit.

The Framing Error Flag F/F is set if the Stop bit is absent at the end of the data byte (asynchronous mode), and also sets the corresponding status bit.

RxRDY (Receiver Ready)

This output indicates that the 8251A contains a character that is ready to be input to the CPU. Rx RDY can be connected to the interrupt structure of the CPU or, for Polled operation, the CPU can check the condition of RxRDY using a Status Read operation.

Rx Enable off both masks and holds RxRDY in the Reset Condition. For Asynchronous mode, to set RxRDY, the Receiver must be Enabled to sense a Start Bit and a complete character must be assembled and transferred to the Data Output Register. For Synchronous mode, to set RxRDY, the Receiver must be enabled and a character must finish assembly and be transferred to the Data Output Register.

Failure to read the received character from the Rx Data Output Register prior to the assembly of the next Rx Data character will set overrun condition error and the previous character will be written over and lost. If the Rx Data is being read by the CPU when the internal transfer is occurring, overrun error will be set and the old character will be lost.

$\overline{RxC}$ (Receiver Clock)

The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the Baud Rate (1x) is equal to the actual frequency of $\overline{RxC}$. In Asynchronous Mode, the Baud Rate is a fraction of the actual $\overline{RxC}$ frequency. A portion of the mode instruction selects this factor; 1, 1/16 or 1/64 the $\overline{RxC}$.

For Example:

Baud Rate equals 300 Baud, if
$\overline{RxC}$ equals 300 Hz (1x)
$\overline{RxC}$ equals 4800 Hz (16x)
$\overline{RxC}$ equals 19.2 kHz (64x).

Baud Rate equals 2400 Baud, if
$\overline{RxC}$ equals 2400 Hz (1x)
$\overline{RxC}$ equals 38.4 kHz (16x)
$\overline{RxC}$ equals 153.6 kHz (64x).

Data is sampled into the 8251A on the rising edge of $\overline{RxC}$.

NOTE: In most communications systems, the 8251A will be handling both the transmission and reception operations of a single link. Consequently, the Receive and Transmit Baud Rates will be the same. Both $\overline{TxC}$ and $\overline{RxC}$ will require identical frequencies for this operation and can be tied together and connected to a single frequency source (Baud Rate Generator) to simplify the interface.

SYNDET (SYNC Detect)/BRKDET (Break Detect)

This pin is used in SYNChronous Mode for SYNDET and may be used as either input or output, programmable through the Control Word. It is reset to output mode low upon RESET. When used as an output (internal Sync mode), the SYNDET pin will go "high" to indicate that the 8251A has located the SYNC character in the Receive mode. If the 8251A is programmed to use double Sync characters (bi-sync), then SYNDET will go "high" in the middle of the last bit of the second Sync character. SYNDET is automatically reset upon a Status Read operation.

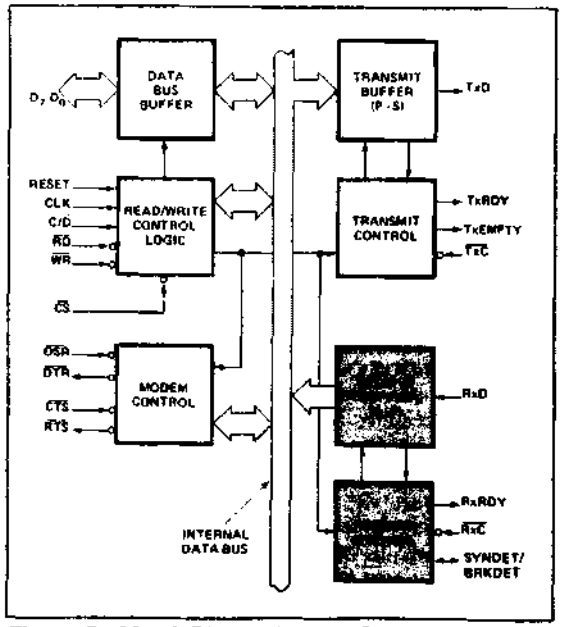


Figure 5. 8251A Block Diagram Showing Receiver Buffer and Control Functions

When used as an input (external SYNC detect mode), a positive going signal will cause the 8251A to start assembling data characters on the rising edge of the next $\overline{RxC}$. Once in SYNC, the "high" input signal can be removed. When External SYNC Detect is programmed, the Internal SYNC Detect is disabled.

BREAK DETECT (Async Mode Only)

This output will go high whenever the receiver remains low through two consecutive stop bit sequences (including the start bits, data bits, and parity bits). Break Detect may also be read as a Status bit. It is reset only upon a master chip Reset or Rx Data returning to a "one" state.

NOTE: On the 8251A/S2657, if the RxData returns to a "one" state during the last bit of the next character after the break, break detect will latch-up, and the device must be cleared by a Chip Reset.

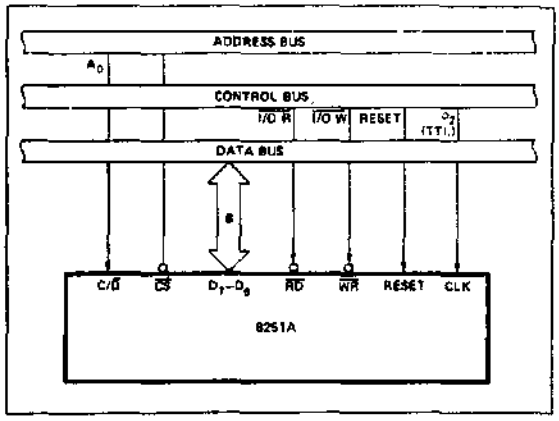


Figure 6. 8251A Interface to 8080 Standard System Bus

DETAILED OPERATION DESCRIPTION

General

The complete functional definition of the 8251A is programmed by the system's software. A set of control words must be sent out by the CPU to initialize the 8251A to support the desired communications format. These control words will program the: BAUD RATE, CHARACTER LENGTH, NUMBER OF STOP BITS, SYNCHRONOUS or ASYNCHRONOUS OPERATION, EVEN/ODD/OFF PARITY, etc. In the Synchronous Mode, options are also provided to select either internal or external character synchronization.

Once programmed, the 8251A is ready to perform its communication functions. The TxRDY output is raised "high" to signal the CPU that the 8251A is ready to receive a data character from the CPU. This output (TxRDY) is reset automatically when the CPU writes a character into the 8251A. On the other hand, the 8251A receives serial data from the MODEM or I/O device. Upon receiving an entire character, the RxRDY output is raised "high" to signal the CPU that the 8251A has a complete character ready for the CPU to fetch. RxRDY is reset automatically upon the CPU data read operation.

The 8251A cannot begin transmission until the Tx Enable (Transmitter Enable) bit is set in the Command Instruction and it has received a Clear To Send ($\overline{CTS}$) input. The TxD output will be held in the marking state upon Reset.

Programming the 8251A

Prior to starting data transmission or reception, the 8251A must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the 8251A and must immediately follow a Reset operation (internal or external).

The control words are split into two formats:

1. Mode Instruction
2. Command Instruction

Mode Instruction

This format defines the general operational characteristics of the 8251A. It must follow a Reset operation (internal or external). Once the Mode Instruction has been written into the 8251A by the CPU, SYNC characters or Command Instructions may be inserted.

Command Instruction

This format defines a status word that is used to control the actual operation of the 8251A.

Both the Mode and Command Instructions must conform to a specified sequence for proper device operation. The Mode Instruction must be inserted immediately following a Reset operation, prior to using the 8251A for data communication.

All control words written into the 8251A after the Mode Instruction will load the Command Instruction. Command Instructions can be written into the 8251A at any time in the data block during the operation of the 8251A. To return to the Mode Instruction format, the master Reset bit in the Command Instruction word can be set to initiate an internal Reset operation which automatically places the 8251A back into the Mode Instruction format. Command Instructions must follow the Mode Instructions or Sync characters.

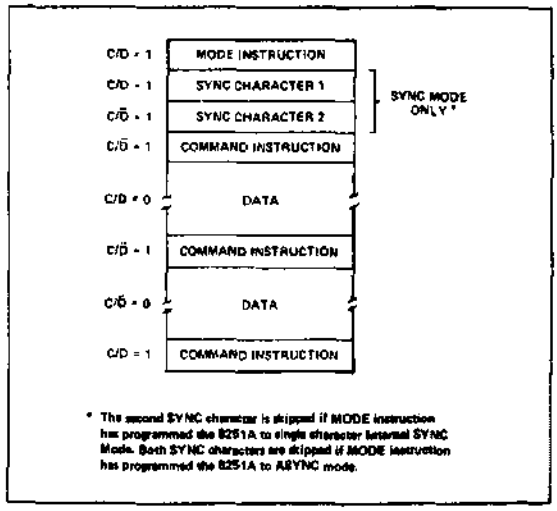


Figure 7. Typical Data Block

Mode Instruction Definition

The 8251A can be used for either Asynchronous or Synchronous data communication. To understand how the Mode Instruction defines the functional operation of the 8251A, the designer can best view the device as two separate components sharing the same package, one Asynchronous the other Synchronous. The format definition can be changed only after a master chip Reset. For explanation purposes the two formats will be isolated.

NOTE: When parity is enabled it is not considered as one of the data bits for the purpose of programming the word length. The actual parity bit received on the Rx Data line cannot be read on the Data Bus. In the case of a programmed character length of less than 8 bits, the least significant Data Bus bits will hold the data; unused bits are "don't care" when writing data to the 8251A, and will be "zeros" when reading the data from the 8251A.

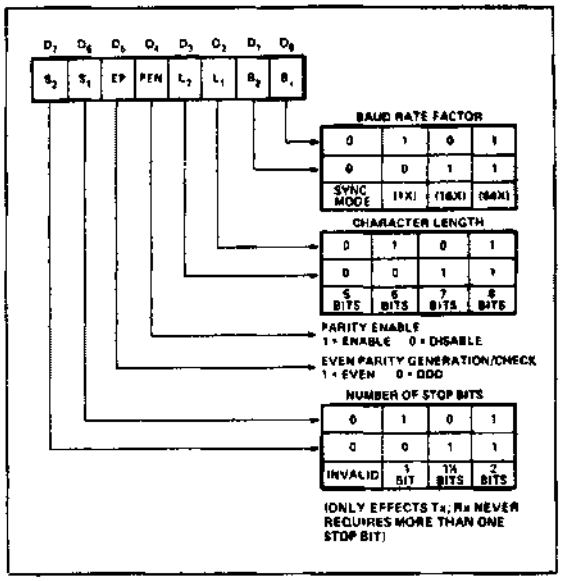


Figure 8. Mode Instruction Format, Asynchronous Mode

Asynchronous Mode (Transmission)

Whenever a data character is sent by the CPU the 8251A automatically adds a Start bit (low level) followed by the data bits (least significant bit first), and the programmed number of Stop bits to each character. Also, an even or odd Parity bit is inserted prior to the Stop bit(s), as defined by the Mode Instruction. The character is then transmitted as a serial data stream on the TxD output. The serial data is shifted out on the falling edge of $\overline{TxC}$ at a rate equal to 1, 1/16, or 1/64 that of the $\overline{TxC}$, as defined by the Mode Instruction. BREAK characters can be continuously sent to the TxD if commanded to do so.

When no data characters have been loaded into the 8251A the TxD output remains "high" (marking) unless a Break (continuously low) has been programmed.

Asynchronous Mode (Receive)

The RxD line is normally high. A falling edge on this line triggers the beginning of a START bit. The validity of this START bit is checked by again strobing this bit at its nominal center (16X or 64X mode only). If a low is detected again, it is a valid START bit, and the bit counter will start counting. The bit counter thus locates the center of the data bits, the parity bit (if it exists) and the stop bits. If parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RxD pin with the rising edge of $\overline{RxC}$. If a low level is detected as the STOP bit, the Framing Error flag will be set. The STOP bit signals the end of a character. Note that the *receiver* requires only *one* stop bit, regardless of the number of stop bits programmed. This character is then loaded into the parallel I/O buffer of the 8251A. The RxRDY pin is raised to signal the CPU that a character is ready to be fetched. If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the OVERRUN Error flag is raised (thus the previous character is lost). All of the error flags can be reset by an Error Reset Instruction. The occurrence of any of these errors will not affect the operation of the 8251A.

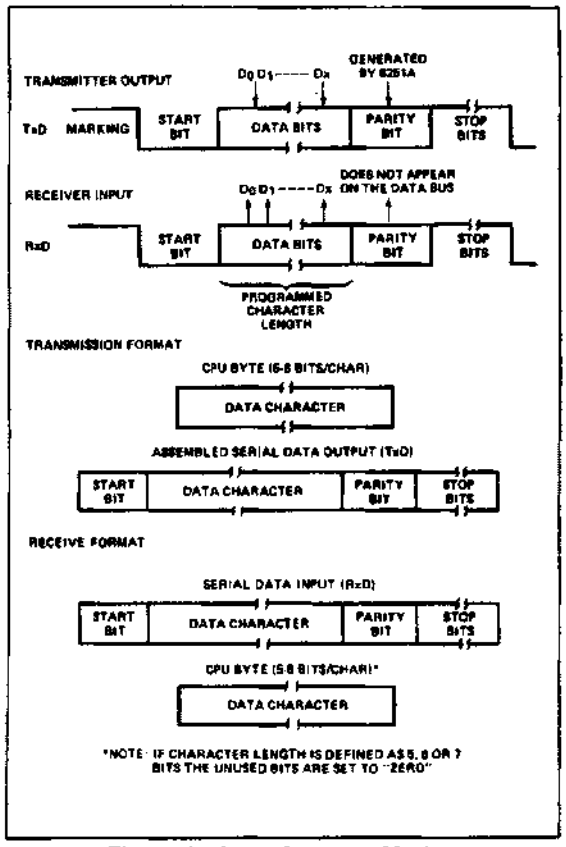
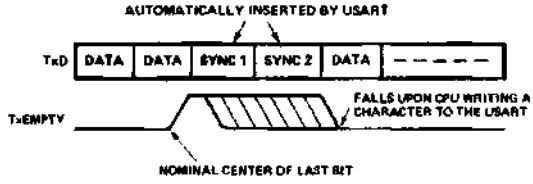


Figure 9. Asynchronous Mode

Synchronous Mode (Transmission)

The TxD output is continuously high until the CPU sends its first character to the 8251A which usually is a SYNC character. When the $\overline{CTS}$ line goes low, the first character is serially transmitted out. All characters are shifted out on the falling edge of $\overline{TxC}$. Data is shifted out at the same rate as the $\overline{TxC}$.

Once transmission has started, the data stream at the TxD output must continue at the $\overline{TxC}$ rate. If the CPU does not provide the 8251A with a data character before the 8251A Transmitter Buffers become empty, the SYNC characters (or character if in single SYNC character mode) will be automatically inserted in the TxD data stream. In this case, the TxEMPTY pin is raised high to signal that the 8251A is empty and SYNC characters are being sent out. TxEMPTY does not go low when the SYNC is being shifted out (see figure below). The TxEMPTY pin is internally reset by a data character being written into the 8251A.



Synchronous Mode (Receive)

In this mode, character synchronization can be internally or externally achieved. If the SYNC mode has been programmed, ENTER HUNT command should be included in the first command instruction word written. Data on the RxD pin is then sampled in on the rising edge of $\overline{RxC}$. The content of the Rx buffer is compared at every bit boundary with the first SYNC character until a match occurs. If the 8251A has been programmed for two SYNC characters, the subsequent received character is also compared; when both SYNC characters have been detected, the USART ends the HUNT mode and is in character synchronization. The SYNDET pin is then set high, and is reset automatically by a STATUS READ. If parity is programmed, SYNDET will not be set until the middle of the parity bit instead of the middle of the last data bit.

In the external SYNC mode, synchronization is achieved by applying a high level on the SYNDET pin, thus forcing the 8251A out of the HUNT mode. The high level can be removed after one $\overline{RxC}$ cycle. An ENTER HUNT command has no effect in the asynchronous mode of operation.

Parity error and overrun error are both checked in the same way as in the Asynchronous Rx mode. Parity is checked when not in Hunt, regardless of whether the Receiver is enabled or not.

The CPU can command the receiver to enter the HUNT mode if synchronization is lost. This will also set all the used character bits in the buffer to a "one", thus preventing a possible false SYNDET caused by data that happens to be in the Rx Buffer at ENTER HUNT time. Note that the SYNDET F/F is reset at each Status Read, regardless of whether internal or external SYNC has been programmed. This does not cause the 8251A to return to the HUNT mode. When in SYNC mode, but not in HUNT, Sync Detection is still functional, but only occurs at the "known" word boundaries. Thus, if one Status Read indicates SYNDET and a second Status Read also indicates SYNDET, then the programmed SYNDET characters have been received since the previous Status Read. (If double character sync has been programmed, then both sync characters have been contiguously received to gate a SYNDET indication.) When external SYNDET mode is selected, internal Sync Detect is disabled, and the SYNDET F/F may be set at any bit boundary.

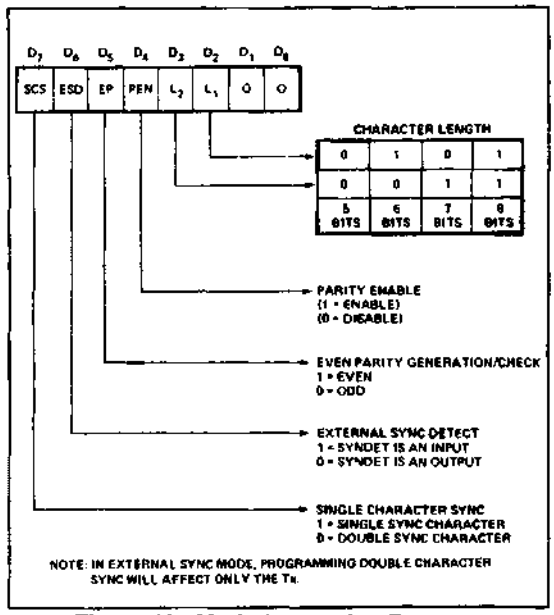


Figure 10. Mode Instruction Format, Synchronous Mode

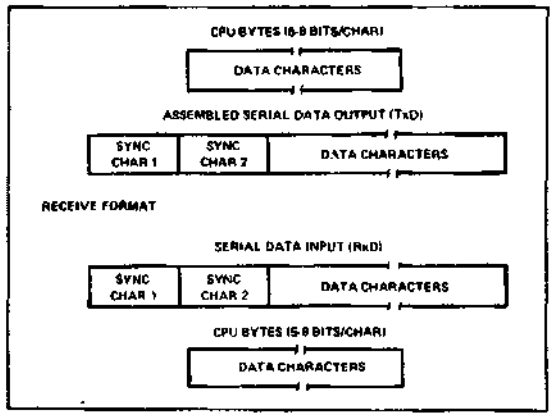
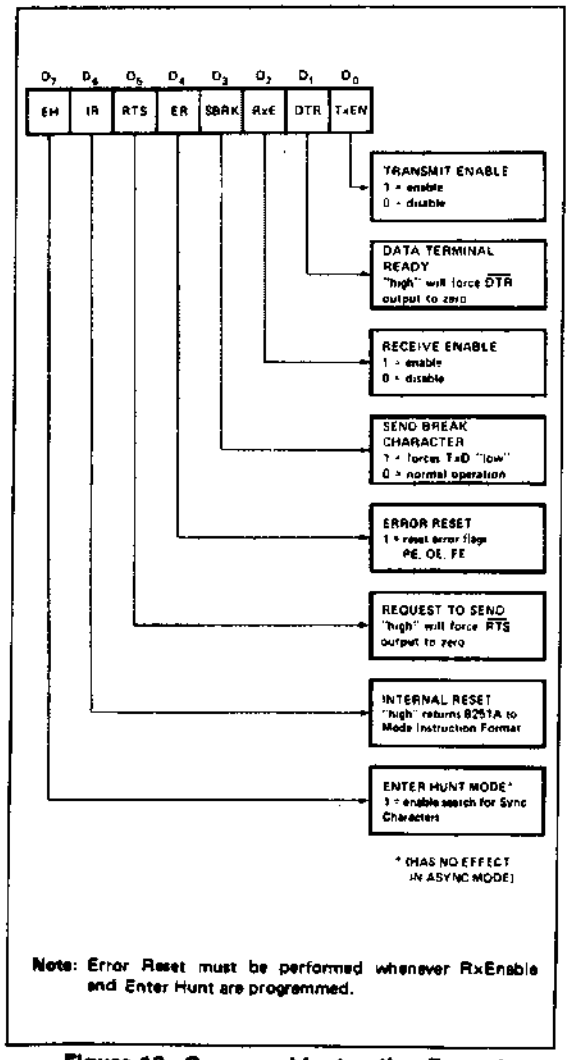


Figure 11. Data Format, Synchronous Mode

COMMAND INSTRUCTION DEFINITION

Once the functional definition of the 8251A has been programmed by the Mode Instruction and the Sync Characters are loaded (if in Sync Mode) then the device is ready to be used for data communication. The Command Instruction controls the actual operation of the selected format. Functions such as: Enable Transmit/Receive, Error Reset and Modem Controls are provided by the Command Instruction.

Once the Mode Instruction has been written into the 8251A and Sync characters inserted, if necessary, then all further "control writes" ($C/\overline{D}$ = 1) will load a Command Instruction. A Reset Operation (internal or external) will return the 8251A to the Mode Instruction format.



Note: Error Reset must be performed whenever RxEnable and Enter Hunt are programmed.

Figure 12. Command Instruction Format

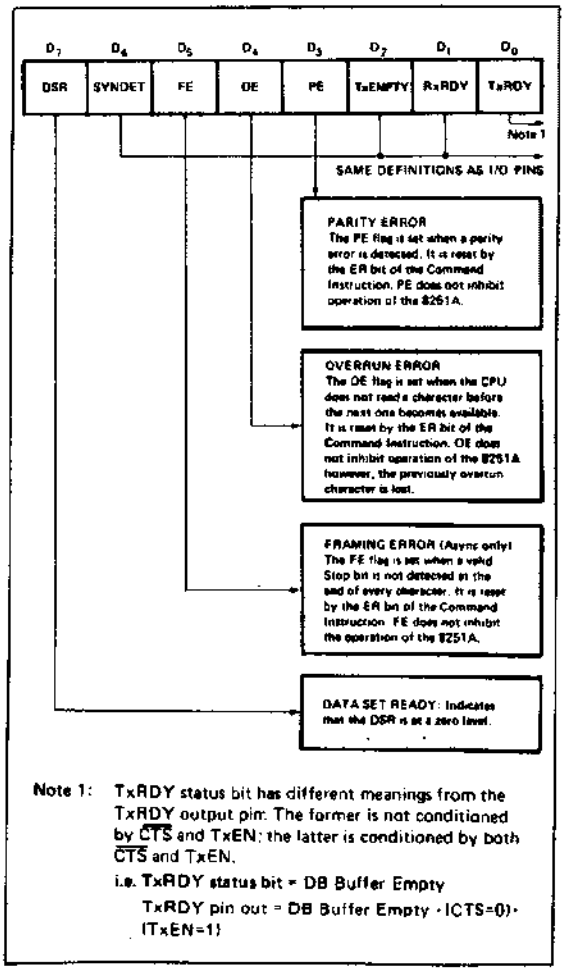
STATUS READ DEFINITION

In data communication systems it is often necessary to examine the "status" of the active device to ascertain if errors have occurred or other conditions that require the processor's attention. The 8251A has facilities that allow the programmer to "read" the status of the device at any time during the functional operation. (The status update is inhibited during status read).

A normal "read" command is issued by the CPU with $C/\overline{D}$ = 1 to accomplish this function.

Some of the bits in the Status Read Format have identical meanings to external output pins so that the 8251A can be used in a completely Polled environment or in an interrupt driven environment. TxRDY is an exception.

Note that status update can have a maximum delay of 28 clock periods from the actual event affecting the status.



Note 1: TxRDY status bit has different meanings from the TxRDY output pin: The former is not conditioned by $\overline{CTS}$ and TxEN; the latter is conditioned by both $\overline{CTS}$ and TxEN.

i.e. TxRDY status bit = DB Buffer Empty

TxRDY pin out = DB Buffer Empty · (CTS=0) · (TxEN=1)

Figure 13. Status Read Format

APPLICATIONS OF THE 8251A

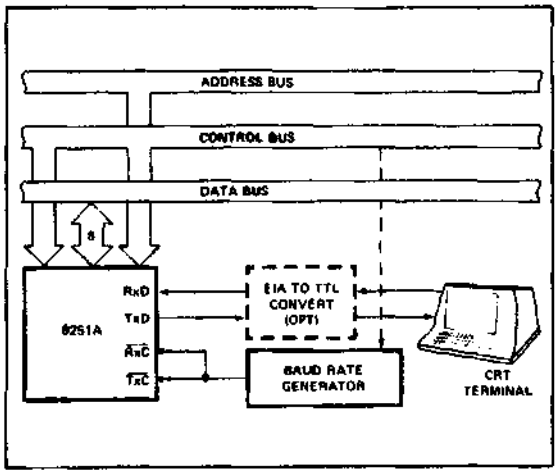


Figure 14. Asynchronous Serial Interface to CRT Terminal, DC—9600 Baud

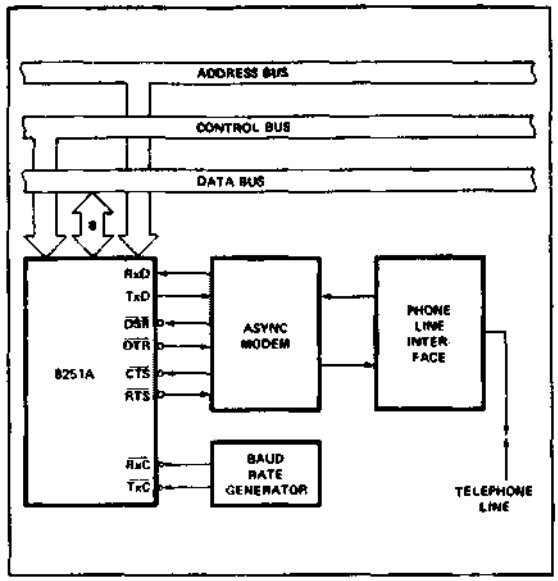


Figure 16. Asynchronous Interface to Telephone Lines

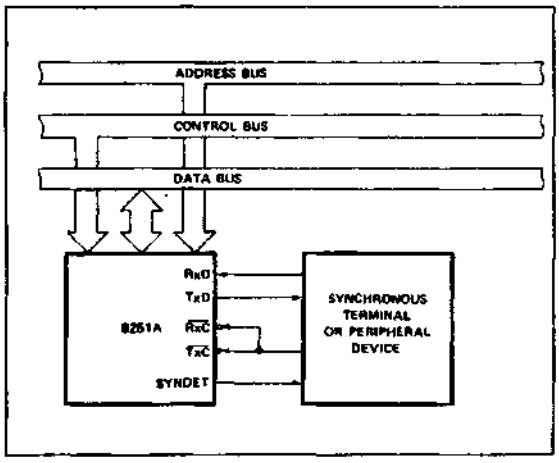


Figure 15. Synchronous Interface to Terminal or Peripheral Device

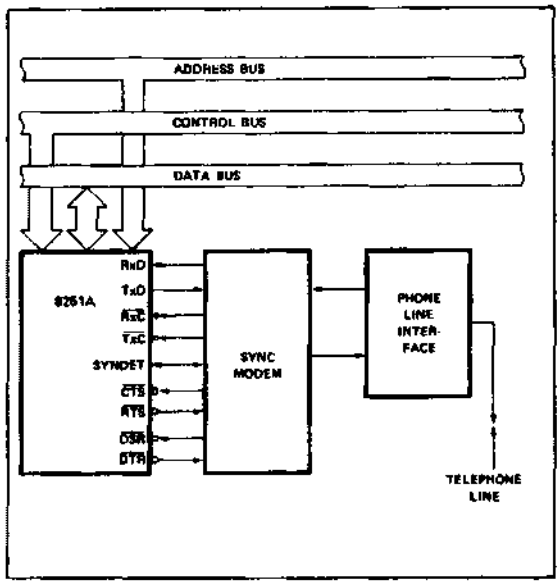


Figure 17. Synchronous Interface to Telephone Lines

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . . −0.5V to +7V
Power Dissipation . . . . . 1 Watt

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%, GND = 0V)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.2	V_{CC}	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} TO 0.45V
I_{IL}	Input Leakage		±10	μA	V_{IN} = V_{CC} TO 0.45V
I_{CC}	Power Supply Current		100	mA	All Outputs = High

CAPACITANCE (T_A = 25°C, V_{CC} = GND = 0V)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance		10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to GND

A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%, GND = 0V)

Bus Parameters (Note 1)

READ CYCLE

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AR}	Address Stable Before $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	50		ns	Note 2
t_{RA}	Address Hold Time for $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	50		ns	Note 2
t_{RR}	$\overline{READ}$ Pulse Width	250		ns	
t_{RD}	Data Delay from $\overline{READ}$		250	ns	3, C_L = 150 pF
t_{DF}	$\overline{READ}$ to Data Floating	10	100	ns	

A.C. CHARACTERISTICS (Continued)

WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AW}	Address Stable Before $\overline{WR}$	50		ns	
t_{WA}	Address Hold Time for $\overline{WR}$	50		ns	
t_{WW}	$\overline{WR}$ Pulse Width	250		ns	
t_{DW}	Data Set Up Time for $\overline{WR}$	150		ns	
t_{WD}	Data Hold Time for $\overline{WR}$	50		ns	
t_{RV}	Recovery Time Between WRITES	6		t_{CY}	Note 4

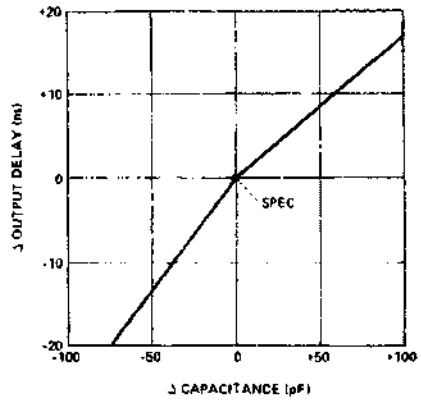
OTHER TIMINGS

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{CY}	Clock Period	320	1350	ns	Notes 5, 6
t_{ϕ}	Clock High Pulse Width	140	t_{CY-90}	ns	
$t_{\overline{\phi}}$	Clock Low Pulse Width	90		ns	
t_R, t_F	Clock Rise and Fall Time		20	ns	
t_{DTx}	TxD Delay from Falling Edge of $\overline{TxC}$		1	µs	
f_{Tx}	Transmitter Input Clock Frequency				
	1x Baud Rate	DC	64	kHz	
	16x Baud Rate	DC	310	kHz	
	64x Baud Rate	DC	615	kHz	
t_{TPW}	Transmitter Input Clock Pulse Width				
	1x Baud Rate	12		t_{CY}	
	16x and 64x Baud Rate	1		t_{CY}	
t_{TPD}	Transmitter Input Clock Pulse Delay				
	1x Baud Rate	15		t_{CY}	
	16x and 64x Baud Rate	3		t_{CY}	
f_{Rx}	Receiver Input Clock Frequency				
	1x Baud Rate	DC	64	kHz	
	16x Baud Rate	DC	310	kHz	
	64x Baud Rate	DC	615	kHz	
t_{RPW}	Receiver Input Clock Pulse Width				
	1x Baud Rate	12		t_{CY}	
	16x and 64x Baud Rate	1		t_{CY}	
t_{RPD}	Receiver Input Clock Pulse Delay				
	1x Baud Rate	15		t_{CY}	
	16x and 64x Baud Rate	3		t_{CY}	
t_{TxRDY}	TxRDY Pin Delay from Center of last Bit		8	t_{CY}	Note 7
$t_{TxRDY\ CLEAR}$	TxRDY ↓ from Leading Edge of $\overline{WR}$		6	t_{CY}	Note 7
t_{RxRDY}	RxRDY Pin Delay from Center of last Bit		24	t_{CY}	Note 7
$t_{RxRDY\ CLEAR}$	RxRDY ↓ from Leading Edge of $\overline{RD}$		6	t_{CY}	Note 7
t_{IS}	Internal SYNDET Delay from Rising Edge of $\overline{RxC}$		24	t_{CY}	Note 7
t_{ES}	External SYNDET Set-Up Time Before Falling Edge of $\overline{RxC}$	16		t_{CY}	Note 7
$t_{TxEMPTY}$	TxEMPTY Delay from Center of Last Bit	20		t_{CY}	Note 7
t_{WC}	Control Delay from Rising Edge of WRITE (TxEn, $\overline{DTR}$, $\overline{RTS}$)	8		t_{CY}	Note 7
t_{CR}	Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)	20		t_{CY}	Note 7

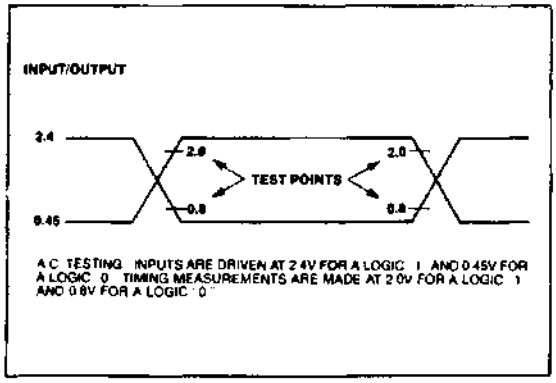
A.C. CHARACTERISTICS (Continued)

NOTES:
1. AC timings measured V_{OH} = 2.0, V_{OL} = 0.8, and with load circuit of Figure 1.
2. Chip Select (CS) and Command/Data (C/D) are considered as Addresses.
3. Assumes that Address is valid before $\overline{RD}\downarrow$.
4. This recovery time is for Mode Initialization only. Write Data is allowed only when TxRDY = 1. Recovery Time between Writes for Asynchronous Mode is 8 t_{CY} and for Synchronous Mode is 16 t_{CY}.
5. The TxC and RxC frequencies have the following limitations with respect to CLK: For 1x Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(30\ t_{CY})$; For 16x and 64x Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(4.5\ t_{CY})$.
6. Reset Pulse Width = 6 t_{CY} minimum; System Clock must be running during Reset.
7. Status update can have a maximum delay of 28 clock periods from the event affecting the status.

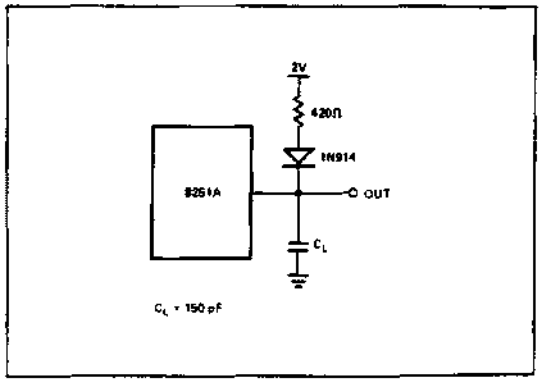
TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE (pF)



A.C. TESTING INPUT, OUTPUT WAVEFORM

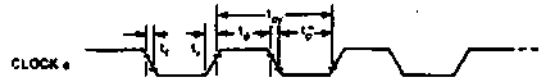


A.C. TESTING LOAD CIRCUIT

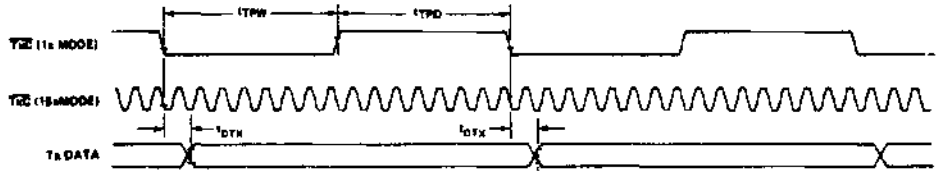


WAVEFORMS

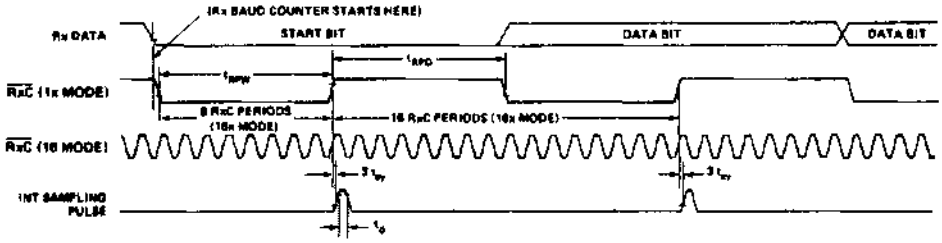
SYSTEM CLOCK INPUT



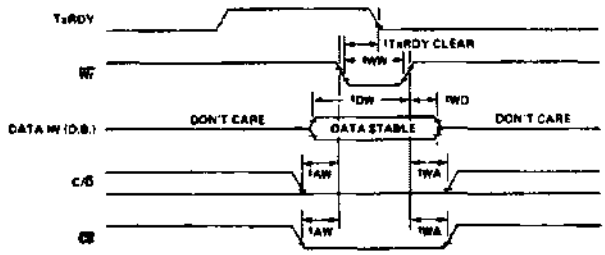
TRANSMITTER CLOCK AND DATA



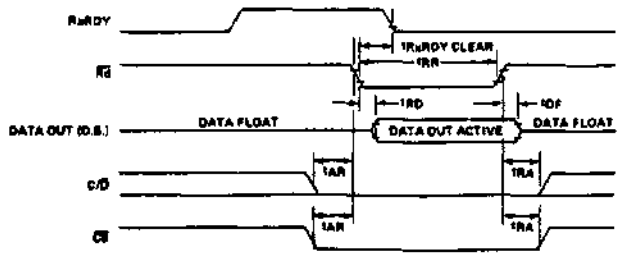
RECEIVER CLOCK AND DATA



WRITE DATA CYCLE (CPU → USART)

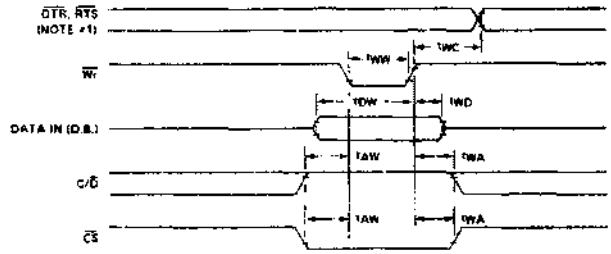


READ DATA CYCLE (CPU ← USART)

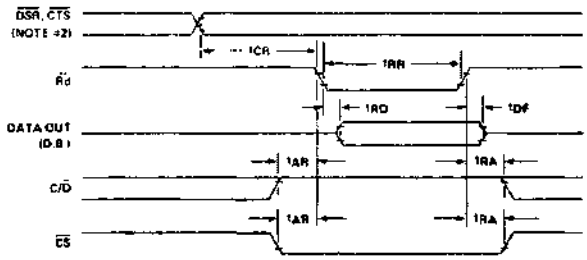


WAVEFORMS (Continued)

WRITE CONTROL OR OUTPUT PORT CYCLE (CPU → USART)

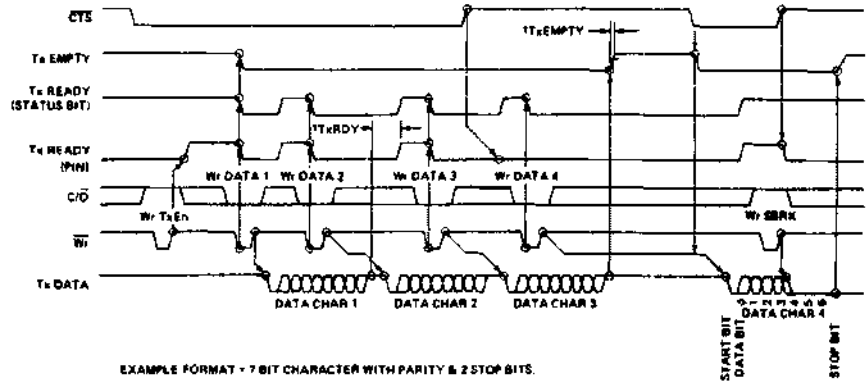


READ CONTROL OR INPUT PORT (CPU ← USART)



NOTE #1: T_{RC} INCLUDES THE RESPONSE TIMING OF A CONTROL BYTE.
NOTE #2: T_{CA} INCLUDES THE EFFECT OF CTS ON THE TxENBL CIRCUITRY.

TRANSMITTER CONTROL AND FLAG TIMING (ASYNC MODE)

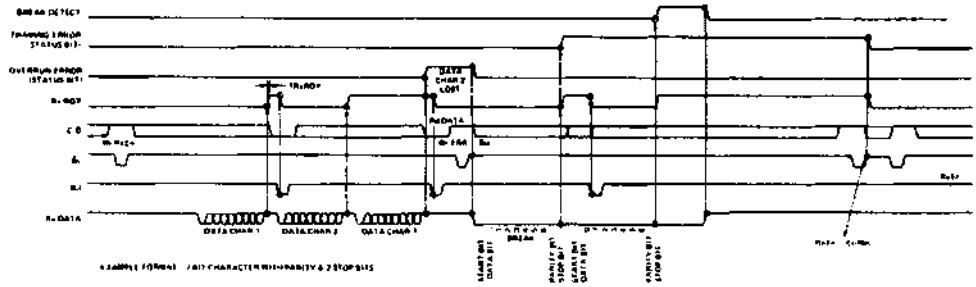


EXAMPLE FORMAT = 7 BIT CHARACTER WITH PARITY & 2 STOP BITS.

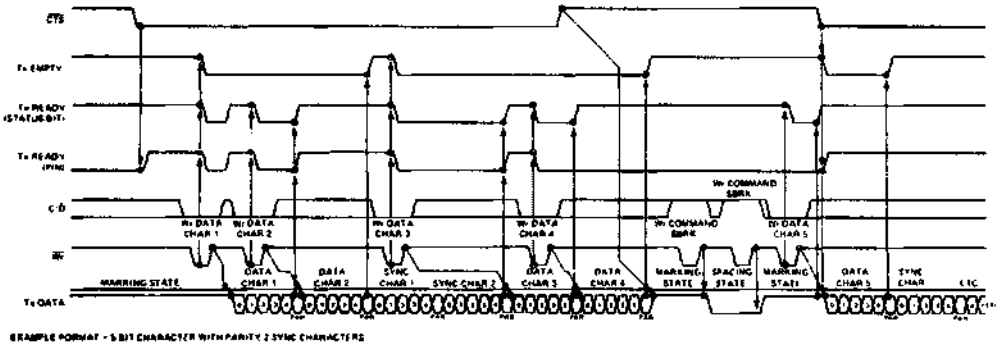
AFN-01573B

WAVEFORMS (Continued)

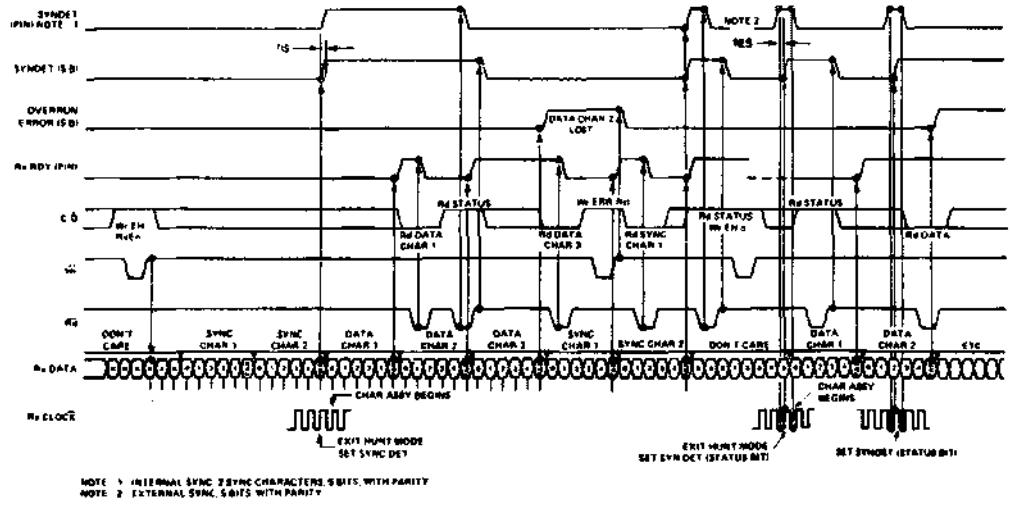
RECEIVER CONTROL AND FLAG TIMING (ASYNC MODE)



TRANSMITTER CONTROL AND FLAG TIMING (SYNC MODE)



RECEIVER CONTROL AND FLAG TIMING (SYNC MODE)



NOTE 1: INTERNAL SYNC, 2 SYNC CHARACTERS, 5 BITS, WITH PARITY
NOTE 2: EXTERNAL SYNC, 5 BITS WITH PARITY

8253/8253-5
PROGRAMMABLE INTERVAL TIMER

- MCS-85™ Compatible 8253-5
- 3 Independent 16-Bit Counters
- DC to 2 MHz
- Programmable Counter Modes
- Count Binary or BCD
- Single +5V Supply
- 24-Pin Dual In-Line Package

The Intel® 8253 is a programmable counter/timer chip designed for use as an Intel microcomputer peripheral. It uses nMOS technology with a single +5V supply and is packaged in a 24-pin plastic DIP.

It is organized as 3 independent 16-bit counters, each with a count rate of up to 2 MHz. All modes of operation are software programmable.

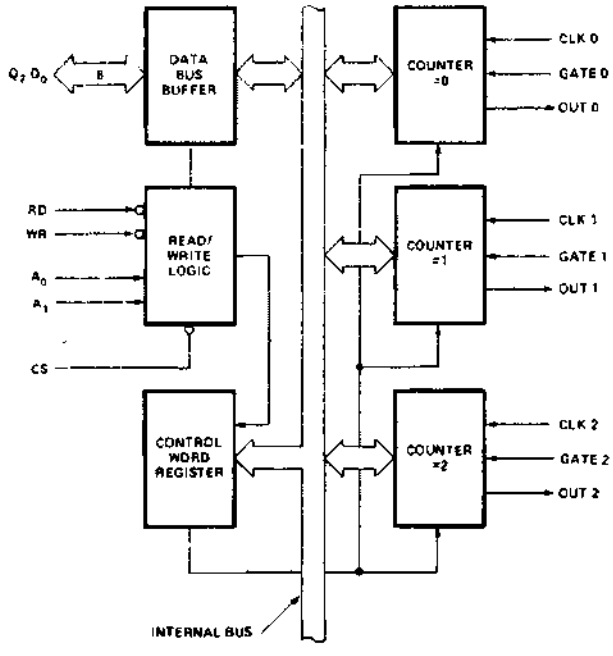


Figure 1. Block Diagram

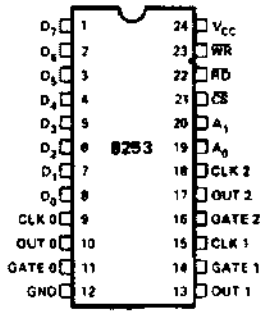


Figure 2. Pin Configuration

FUNCTIONAL DESCRIPTION

General

The 8253 is a programmable interval timer/counter specifically designed for use with the Intel™ Microcomputer systems. Its function is that of a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 8253 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in systems software, the programmer configures the 8253 to match his requirements, initializes one of the counters of the 8253 with the desired quantity, then upon command the 8253 will count out the delay and interrupt the CPU when it has completed its tasks. It is easy to see that the software overhead is minimal and that multiple delays can easily be maintained by assignment of priority levels.

Other counter/timer functions that are non-delay in nature but also common to most microcomputers can be implemented with the 8253.

- Programmable Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real Time Clock
- Digital One-Shot
- Complex Motor Controller

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the 8253 to the system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput CPU instructions. The Data Bus Buffer has three basic functions.

1. Programming the MODES of the 8253.
2. Loading the count registers.
3. Reading the count values.

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and in turn generates control signals for overall device operation. It is enabled or disabled by CS so that no operation can occur to change the function unless the device has been selected by the system logic.

$\overline{RD}$ (Read)

A "low" on this input informs the 8253 that the CPU is inputting data in the form of a counters value.

$\overline{WR}$ (Write)

A "low" on this input informs the 8253 that the CPU is outputting data in the form of mode information or loading counters.

A0, A1

These inputs are normally connected to the address bus. Their function is to select one of the three counters to be operated on and to address the control word register for mode selection.

$\overline{CS}$ (Chip Select)

A "low" on this input enables the 8253. No reading or writing will occur unless the device is selected. The $\overline{CS}$ input has no effect upon the actual operation of the counters.

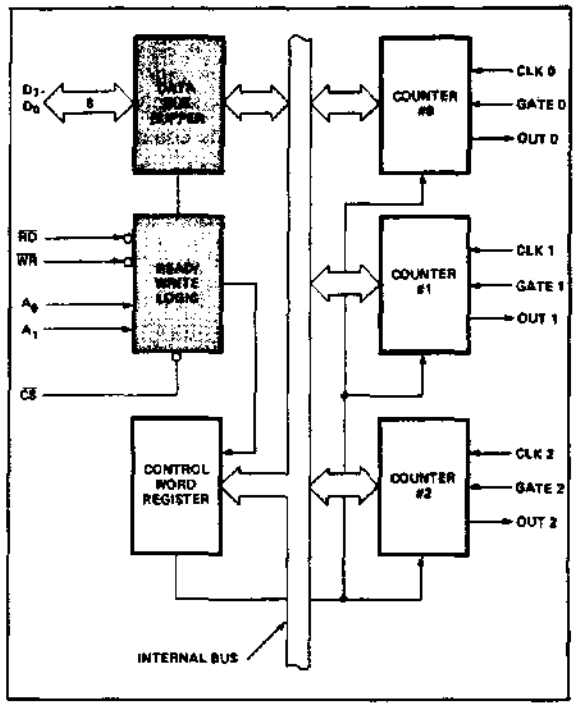


Figure 3. Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No-Operation 3-State
1	X	X	X	X	Disable 3-State
0	1	1	X	X	No-Operation 3-State

Control Word Register

The Control Word Register is selected when A0, A1 are 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operational MODE of each counter, selection of binary or BCD counting and the loading of each count register.

The Control Word Register can only be written into; no read operation of its contents is available.

Counter #0, Counter #1, Counter #2

These three functional blocks are identical in operation so only a single Counter will be described. Each Counter consists of a single, 16-bit, pre-settable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of MODES stored in the Control Word Register.

The counters are fully independent and each can have separate Mode configuration and counting operation, binary or BCD. Also, there are special features in the control word that handle the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications and special commands and logic are included in the 8253 so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

8253 SYSTEM INTERFACE

The 8253 is a component of the Intel™ Microcomputer Systems and interfaces in the same manner as all other peripherals of the family. It is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The $\overline{CS}$ can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an Intel® 8205 for larger systems.

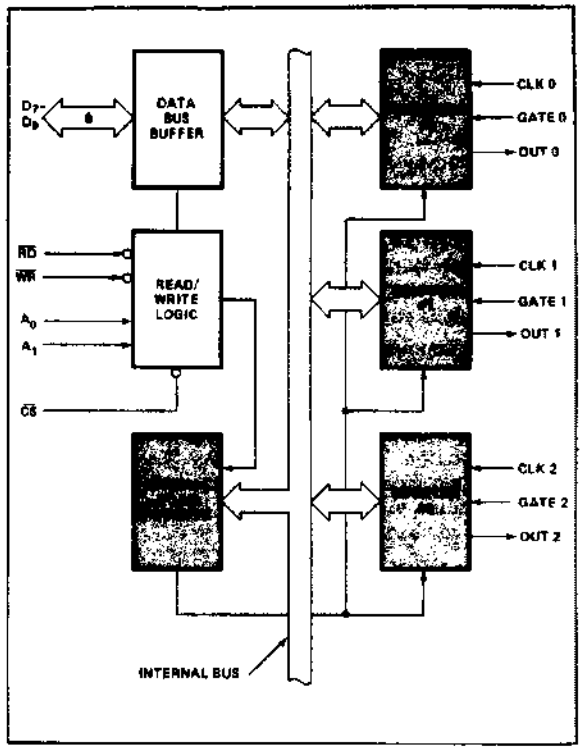


Figure 4. Block Diagram Showing Control Word Register and Counter Functions

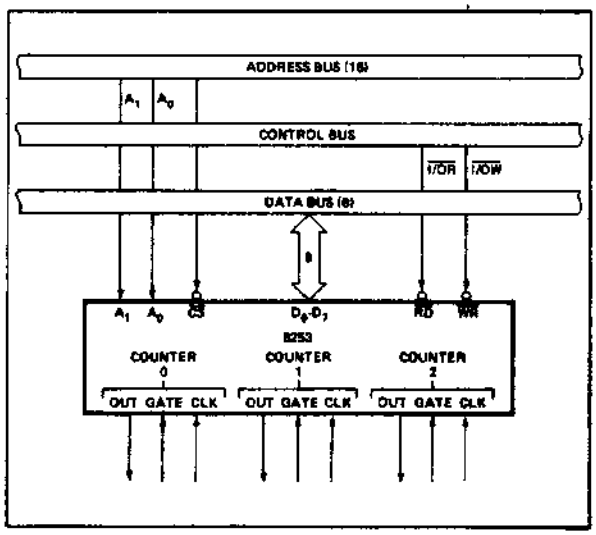


Figure 5. 8253 System Interface

OPERATIONAL DESCRIPTION

General

The complete functional definition of the 8253 is programmed by the systems software. A set of control words must be sent out by the CPU to initialize each counter of the 8253 with the desired MODE and quantity information. Prior to initialization, the MODE, count, and output of all counters is undefined. These control words program the MODE, Loading sequence and selection of binary or BCD counting.

Once programmed, the 8253 is ready to perform whatever timing tasks it is assigned to accomplish.

The actual counting operation of each counter is completely independent and additional logic is provided on-chip so that the usual problems associated with efficient monitoring and management of external, asynchronous events or rates to the microcomputer system have been eliminated.

Programming the 8253

All of the MODES for each counter are programmed by the systems software by simple I/O operations.

Each counter of the 8253 is individually programmed by writing a control word into the Control Word Register. (A0, A1 = 11)

Control Word Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Definition of Control

SC — Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

RL — Read/Load:

RL1	RL0	
0	0	Counter Latching operation (see READ/WRITE Procedure Section)
1	0	Read/Load most significant byte only.
0	1	Read/Load least significant byte only.
1	1	Read/Load least significant byte first, then most significant byte.

M — MODE:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

Counter Loading

The count register is not loaded until the count value is written (one or two bytes, depending on the mode selected by the RL bits), followed by a rising edge and a falling edge of the clock. Any read of the counter prior to that falling clock edge may yield invalid data.

MODE Definition

MODE 0: Interrupt on Terminal Count. The output will be initially low after the mode set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached the output will go high and remain high until the selected count register is reloaded with the mode or a new count is loaded. The counter continues to decrement after terminal count has been reached.

Rewriting a counter register during counting results in the following:

(1) Write 1st byte stops the current counting.
(2) Write 2nd byte starts the new count.

MODE 1: Programmable One-Shot. The output will go low on the count following the rising edge of the gate input.

The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

MODE 2: Rate Generator. Divide by N counter. The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. Thus, the gate input can be used to synchronize the counter.

When this mode is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

MODE 3: Square Wave Rate Generator. Similar to MODE 2 except that the output will remain high until one half the count has been completed (for even numbers) and go low for the other half of the count. This is accomplished by decrementing the counter by two on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the output is changed and the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the clock by 2. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by 2 until timeout. Then the whole process is repeated. In this way, if the count is odd, the output will be high for (N + 1)/2 counts and low for (N – 1)/2 counts.

MODE 4: Software Triggered Strobe. After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

If the count register is reloaded between output pulses, counting will continue from the new value. The count will be inhibited while the gate input is low. Reloading the counter register will restart counting beginning with the new number.

MODE 5: Hardware Triggered Strobe. The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

Modes \ Signal Status	Low Or Going Low	Rising	High
0	Disables counting	— —	Enables counting
1	— —	1) Initiates counting 2) Resets output after next clock	— —
2	1) Disables counting 2) Sets output immediately high	1) Reloads counter 2) Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	Disables counting	— —	Enables counting
5	— —	Initiates counting	— —

Figure 6. Gate Pin Operations Summary

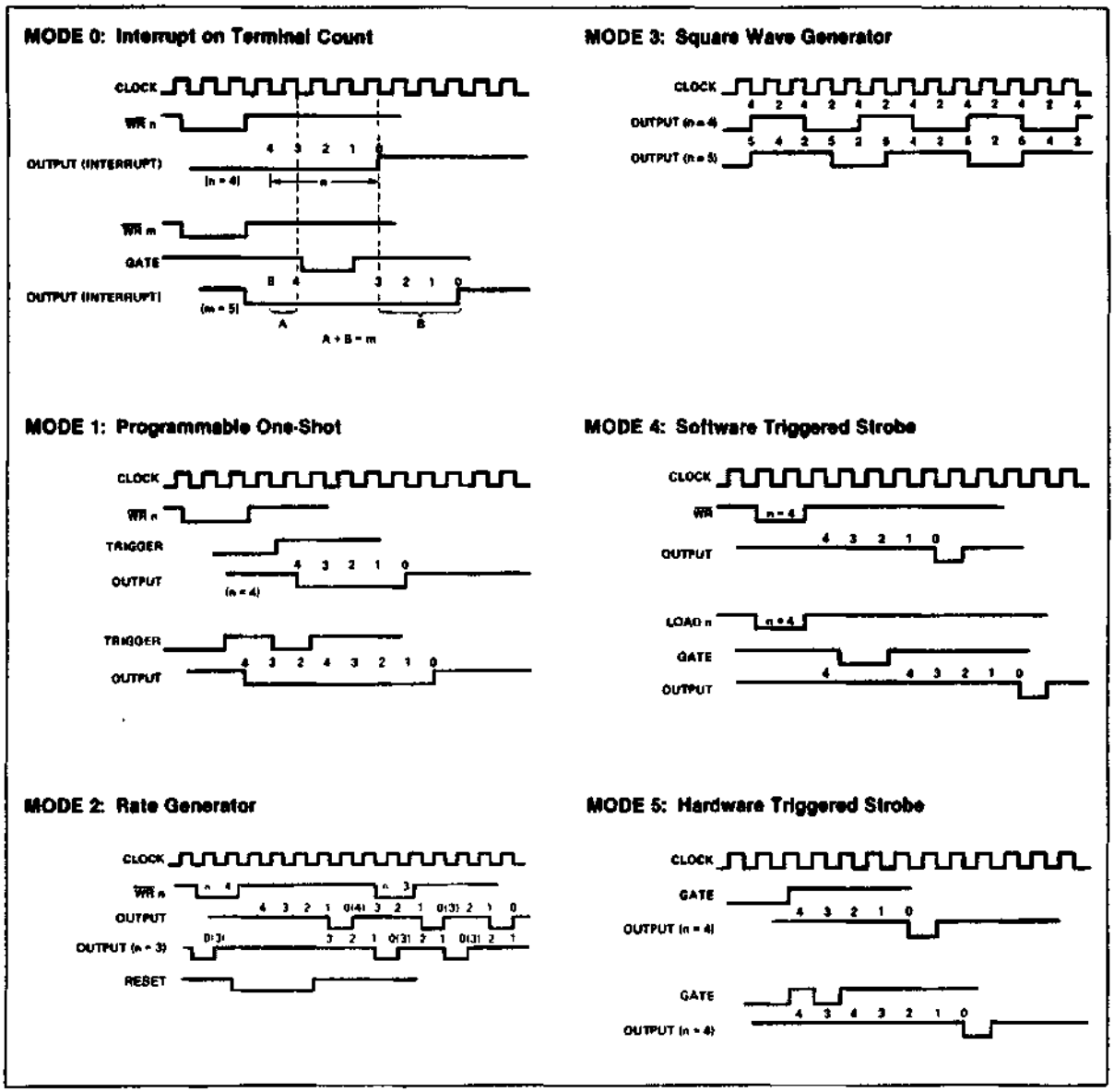


Figure 7. 8253 Timing Diagrams

8253 READ/WRITE PROCEDURE

Write Operations

The systems software must program each counter of the 8253 with the mode and quantity desired. The programmer must write out to the 8253 a MODE control word and the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

The actual order of the programming is quite flexible. Writing out of the MODE control word can be in any sequence of counter selection, e.g., counter #0 does not have to be first or counter #2 last. Each counter's MODE control word register has a separate address so that its loading is completely sequence independent. (SC0, SC1)

The loading of the Count Register with the actual count value, however, must be done in exactly the sequence programmed in the MODE control word (RL0, RL1). This loading of the counter's count register is still sequence independent like the MODE control word loading, but when a selected count register is to be loaded it must be loaded with the number of bytes programmed in the MODE control word (RL0, RL1). The one or two bytes to be loaded in the count register do not have to follow the associated MODE control word. They can be programmed at any time following the MODE control word loading as long as the correct number of bytes is loaded in order.

All counters are down counters. Thus, the value loaded into the count register will actually be decremented. Loading all zeroes into a count register will result in the maximum count (2^{15} for Binary or 10^4 for BCD). In MODE 0 the new count will not restart until the load has been completed. It will accept one of two bytes depending on how the MODE control words (RL0, RL1) are programmed. Then proceed with the restart operation.

	MODE Control Word Counter n
LSB	Count Register byte Counter n
MSB	Count Register byte Counter n

Note: Format shown is a simple example of loading the 8253 and does not imply that it is the only format that can be used.

Figure 8. Programming Format

			A1	A0
No. 1		MODE Control Word Counter 0	1	1
No. 2		MODE Control Word Counter 1	1	1
No. 3		MODE Control Word Counter 2	1	1
No. 4	LSB	Count Register Byte Counter 1	0	1
No. 5	MSB	Count Register Byte Counter 1	0	1
No. 6	LSB	Count Register Byte Counter 2	1	0
No. 7	MSB	Count Register Byte Counter 2	1	0
No. 8	LSB	Count Register Byte Counter 0	0	0
No. 9	MSB	Count Register Byte Counter 0	0	0

Note: The exclusive addresses of each counter's count register make the task of programming the 8253 a very simple matter, and maximum effective use of the device will result if this feature is fully utilized.

Figure 9. Alternate Programming Formats

Read Operations

In most counter applications it becomes necessary to read the value of the count in progress and make a computational decision based on this quantity. Event counters are probably the most common application that uses this function. The 8253 contains logic that will allow the programmer to easily read the contents of any of the three counters without disturbing the actual count in progress.

There are two methods that the programmer can use to read the value of the counters. The first method involves the use of simple I/O read operations of the selected counter. By controlling the A0, A1 inputs to the 8253 the programmer can select the counter to be read (remember that no read operation of the mode register is allowed A0, A1=11). The only requirement with this method is that in order to assure a stable count reading the actual operation of the selected counter must be inhibited either by controlling the Gate input or by external logic that inhibits the clock input. The contents of the counter selected will be available as follows:

first I/O Read contains the least significant byte (LSB).

second I/O Read contains the most significant byte (MSB).

Due to the internal logic of the 8253 it is absolutely necessary to complete the entire reading procedure. If two bytes are programmed to be read then two bytes must be read before any loading WR command can be sent to the same counter.

Read Operation Chart

A1	A0	RD	
0	0	0	Read Counter No. 0
0	1	0	Read Counter No. 1
1	0	0	Read Counter No. 2
1	1	0	Illegal

Reading While Counting

In order for the programmer to read the contents of any counter without effecting or disturbing the counting operation the 8253 has special internal logic that can be accessed using simple WR commands to the MODE register. Basically, when the programmer wishes to read the contents of a selected counter "on the fly" he loads the MODE register with a special code which latches the present count value into a storage register so that its contents contain an accurate, stable quantity. The programmer then issues a normal read command to the selected counter and the contents of the latched register is available.

MODE Register for Latching Count

A0, A1 = 11

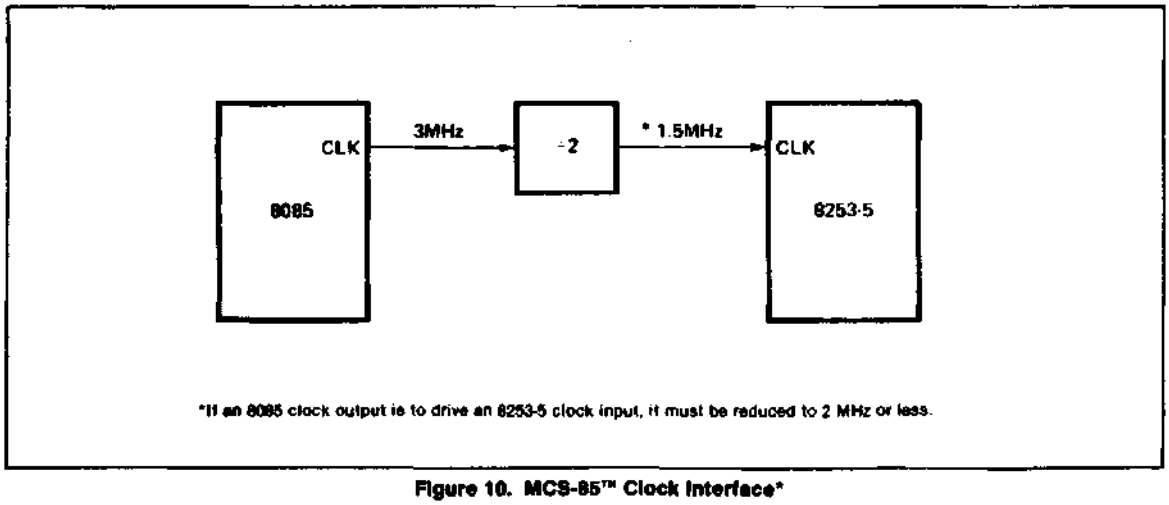
D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

SC1,SC0 — specify counter to be latched.

D5,D4 — 00 designates counter latching operation.

X — don't care.

The same limitation applies to this mode of reading the counter as the previous method. That is, it is mandatory to complete the entire read operation as programmed. This command has no effect on the counter's mode.



*If an 8085 clock output is to drive an 8253-5 clock input, it must be reduced to 2 MHz or less.

Figure 10. MCS-85™ Clock Interface*

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin
With Respect to Ground ..... −0.5 V to +7 V
Power Dissipation ..... 1 Watt

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permenent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ±10%)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.2	V_{CC}+.5V	V	
V_{OL}	Output Low Voltage		0.45	V	Note 1
V_{OH}	Output High Voltage	2.4		V	Note 2
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0V
I_{CC}	V_{CC} Supply Current		140	mA	

CAPACITANCE (T_A = 25°C, V_{CC} = GND = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}

A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%, GND = 0V)

Bus Parameters (Note 3)

READ CYCLE

Symbol	Parameter	8253		8253-5		Unit
		Min.	Max.	Min.	Max.	
t_{AR}	Address Stable Before $\overline{READ}$	50		30		ns
t_{RA}	Address Hold Time for $\overline{READ}$	5		5		ns
t_{RR}	$\overline{READ}$ Pulse Width	400		300		ns
t_{RD}	Data Delay From $\overline{READ}$[4]		300		200	ns
t_{DF}	$\overline{READ}$ to Data Floating	25	125	25	100	ns
t_{RV}	Recovery Time Between READ and Any Other Control Signal	1		1		μs

A.C. CHARACTERISTICS (Continued)

WRITE CYCLE

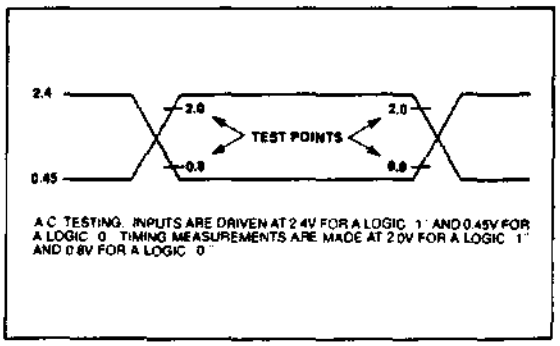
Symbol	Parameter	8253		8253-5		Unit
		Min.	Max.	Min.	Max.	
t_{AW}	Address Stable Before $\overline{WRITE}$	50		30		ns
t_{WA}	Address Hold Time for $\overline{WRITE}$	30		30		ns
t_{WW}	$\overline{WRITE}$ Pulse Width	400		300		ns
t_{DW}	Data Set Up Time for $\overline{WRITE}$	300		250		ns
t_{WD}	Data Hold Time for $\overline{WRITE}$	40		30		ns
t_{RV}	Recovery Time Between $\overline{WRITE}$ and Any Other Control Signal	1		1		μs

CLOCK AND GATE TIMING

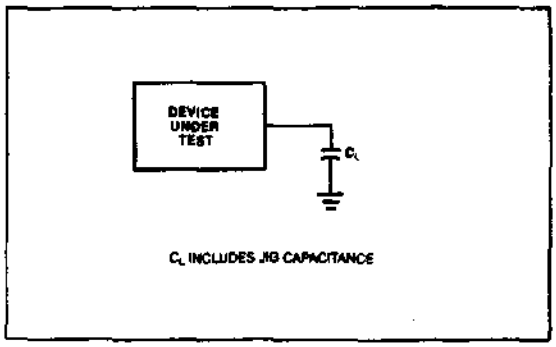
Symbol	Parameter	8253		8253-5		Unit
		Min.	Max.	Min.	Max.	
t_{CLK}	Clock Period	380	dc	380	dc	ns
t_{PWH}	High Pulse Width	230		230		ns
t_{PWL}	Low Pulse Width	150		150		ns
t_{GW}	Gate Width High	150		150		ns
t_{GL}	Gate Width Low	100		100		ns
t_{GS}	Gate Set Up Time to CLK↑	100		100		ns
t_{GH}	Gate Hold Time After CLK↑	50		50		ns
t_{OD}	Output Delay From CLK↓[4]		400		400	ns
t_{ODG}	Output Delay From Gate↓[4]		300		300	ns

NOTES:
1. I_{OL} = 2.2 mA.
2. I_{OH} = −400 μA.
3. AC timings measured at V_{OH} 2.2, V_{OL} = 0.8.
4. C_L = 150pF.

A.C. TESTING INPUT, OUTPUT WAVEFORM

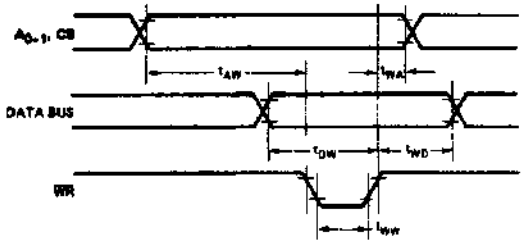


A.C. TESTING LOAD CIRCUIT

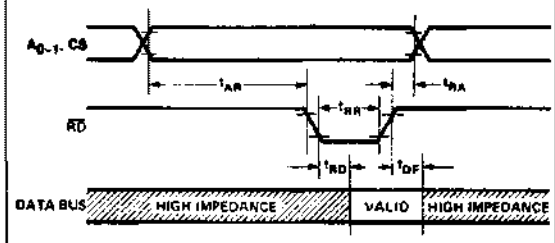


WAVEFORMS

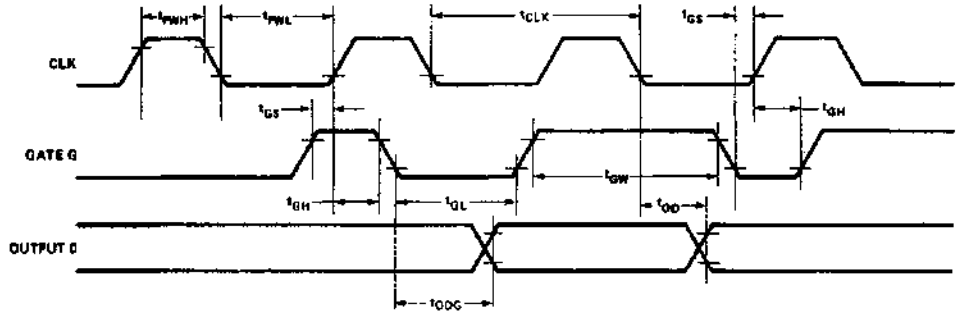
WRITE TIMING



READ TIMING



CLOCK AND GATE TIMING



4.0 FLOPPY DISK DRIVE CONTROLLER BOARD

GENERAL INFORMATION

The Nabu Floppy Disk Drive Controller Board (AFC-1100), can operate any combination of up to four full-size (8") or mini (5.25") floppy disk drives simultaneously on the S-100 bus. This controller is compatible with Shugart, Remex, Memorex, Pertec, and most other disk drives.

The AFC-1100 is interrupt driven and assigned the highest interrupt priority. It accommodates both single-density (IBM 3740) and double-density (IBM System 34) formats, with soft sector compatibility. Recording can be done on both sides of a diskette, thus allowing up to 1 Megabyte of formatted data to be stored on a 2-sided, double-density diskette.

Western Digital's FD1793, along with two other supporting chips, form the heart of the AFC-1100 controller. As well, phase lock loop (PLL) techniques are used in the controller to increase the reliability of data recovery.

SPECIFIC FEATURES

FD1793 Floppy Disk Formatter/Controller

The FD1793 floppy disk formatter/controller, (U11), is a powerful LSI chip which provides all required interface signals to a floppy disk drive. The eleven instructions which the FD1793 performs, enhance system throughput and minimize support from the processor.

A few supporting chips are also required by the FD1793 to complete the working floppy disk system. One of these is the phase lock loop data recovery circuit, which includes part of U5 (WD1691), a VCO, and a low pass filter. As mentioned, the use of the PLL technique enhances the reliability of the data recovery process. As well, any speed variations or track to track variations can also be handled better with a PLL.

Another supporting chip is the write precompensation circuit, which contains the remaining part of U5 and a WD2143 (U6). The precompensation applies only when the current track number on a double-density diskette is greater than 43.

Detailed information regarding the uses of the FD1793, WD1691, and WD2143 can be obtained from the manufacturer's data sheets included.

Device Addressing

The address decoder is designed such that the board's internal registers are located at port addresses F3H to F7H. The function of each port is as follows:

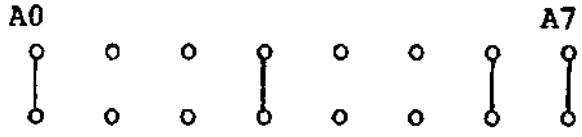
Port Address	Data Read	Data Write
F3H	Drive status	Drive command
F4H	Status register	Command register
F5H	Track register	Track register
F6H	Sector register	Sector register
F7H	Data register	Data register

Ports F4H to F7H correspond to the internal registers of the 1793 floppy controller chip. The meaning of the data bits is explained in the enclosed data sheet for the 1793 integrated circuit. Port F3H relates to disk drive parameters. The functions of the data bits are summarized as follows:

	Data Bit	Designation	Function
Drive Status	D0	DRSEL1	Drive 0 (A) selected
	D1	DRSEL2	Drive 1 (B) selected
	D2	DRSEL3	Drive 2 (C) selected
	D3	DRSEL4	Drive 3 (D) selected
	D4	SIDE 1	Side 1 of drive selected
	D5	-	5.25" drive selected
	D6	$\overline{\text{DDEN}}$	Single density selected
	D7	$\overline{\text{2-SIDED}}$	Single sided diskette in drive
Drive Command	D0	DRSEL1	Selects drive 0 (A)
	D1	DRSEL2	Selects drive 1 (B)
	D2	DRSEL3	Selects drive 2 (C)
	D3	DRSEL4	Selects drive 3 (D)
	D4	SIDE 1	Selects side 1 of drive
	D5	-	Selects 5.25" drive
	D6	$\overline{\text{DDEN}}$	Selects single density
	D7	-	Enables wait states

Jumper Connections

The interrupt vector jumper area is located in the upper right-hand corner of the board. The address is set to 0036H for the Nabu 1100 System. (With jumper means logic one).



The jumper selection labelled 'A', near the middle of the board, enables the user to select disk size (8" or 5.25") either by hardwired logic, or by software control. The Nabu 1100 System uses software selection.

Hardwire selection :

8" : Jumper 2 and 3

5.25" : No jumper

Software selection : Jumper 1 and 2

Timing Adjustments

The data recovery circuit is implemented by phase lock loop techniques. Therefore, input DC voltage and output clock frequency adjustments must be performed on the VCO (U7). Also, the four phase clock generator (U6) for the precompensation circuit, must be adjusted for proper operation.

The adjustments are performed on RR1, RR2, RR3, and RR4, which are located in the bottom left-hand corner of the board. Normally, these potentiometers are factory adjusted. Should any adjustments be required, they should be performed by qualified service personnel.

Connection of the Disk Drives

The 50-pin header strip (J2), connects all large (8") drives to the board; and the 34-pin header strip (J1 if it exists), connects all mini (5.25") drives to the board.

Only the even numbered pins (bottom row) are used for connection to the drives, while the odd numbered pins (top row) are grounded. The pins are numbered from right to left.

The 2-pin header on the right-hand side of J2, is used for interrupt priority connection. These pins are left open for the Nabu 1100 single user system. For a multi-user system, the input pin should be left open (highest interrupt priority) while the output pin should be connected to the board with next highest priority.

NABU AFC-1100 FLOPPY DISK DRIVE CONTROLLER BOARD PARTS LIST

Integrated Circuits:

U1	7805	5 V positive voltage regulator
U2	7812	12 V positive voltage regulator
U3, U29	74LS367	Hex bus driver
U4, U16	74LS123	Dual retriggerable monostable multivibrator with clear
U5	WD1691	Floppy support logic (Western Digital)
U6	WD2143	Four phase clock generator (Western Digital)
U7	74S124	Dual voltage-controlled oscillator
U8	74LS20	Dual 4-input NAND
U9, U10	7406	Hex inverter
U11	FD1793B	Floppy disk controller chip (Western Digital)
U12	74LS157	Quadruple 2-line-to-1-line multiplexer
U13, U20, U24, U25	74LS244	Octal buffer/line-driver with 3-state outputs
U14	74LS138	3-to-8-line decoder/demultiplexer
U15	74LS273	Octal D-type flip-flop
U17	74LS02	Quadruple 2-input NOR
U18, U21	74LS00	Quadruple 2-input NAND
U19	74LS04	Hex inverter
U22, U23, U26	74LS74	Dual D-type positive-edge-triggered flip-flop with preset and clear
U27, U28	74LS10	Triple 3-input NAND

Diodes:

D1, D2	1N914A	Silicon switching diode

Capacitors:

C1, C16	68 pF
C2, C4, C5	
C6, C7	10 µF, 35 V tantalum electrolytic
C3, C8-C9, C12, C14-C15, C17-C22	0.1 µF
C10	.33 µF stacked film capacitor
C11	82 pF
C13	47~51pF

Resistors:

R1-R6	150 Ω
R7	12 kΩ
R8,	5.1 kΩ
R9	3.6 kΩ

R10	4.7 k Ω
R11-R13	47 k Ω
R14-R16	10 k Ω
R17	6.2 k Ω
R18	4.7 k Ω
R19	1 k Ω
RR1	10 k Ω
RR2	100 k Ω
RR3, RR4	50 k Ω
RN1	1 k Ω

Quantity	Description
12	14 pin IC socket
7	16 pin IC socket
1	18 pin IC socket
6	20 pin IC socket
1	40 pin IC socket
1	50 pin right angle pin connector
1	2 pin right angle pin connector
2	TO-220 heat-sink
2	#6-32 x 3/8" machine screw
2	#6-32 nuts
1	p.c. board

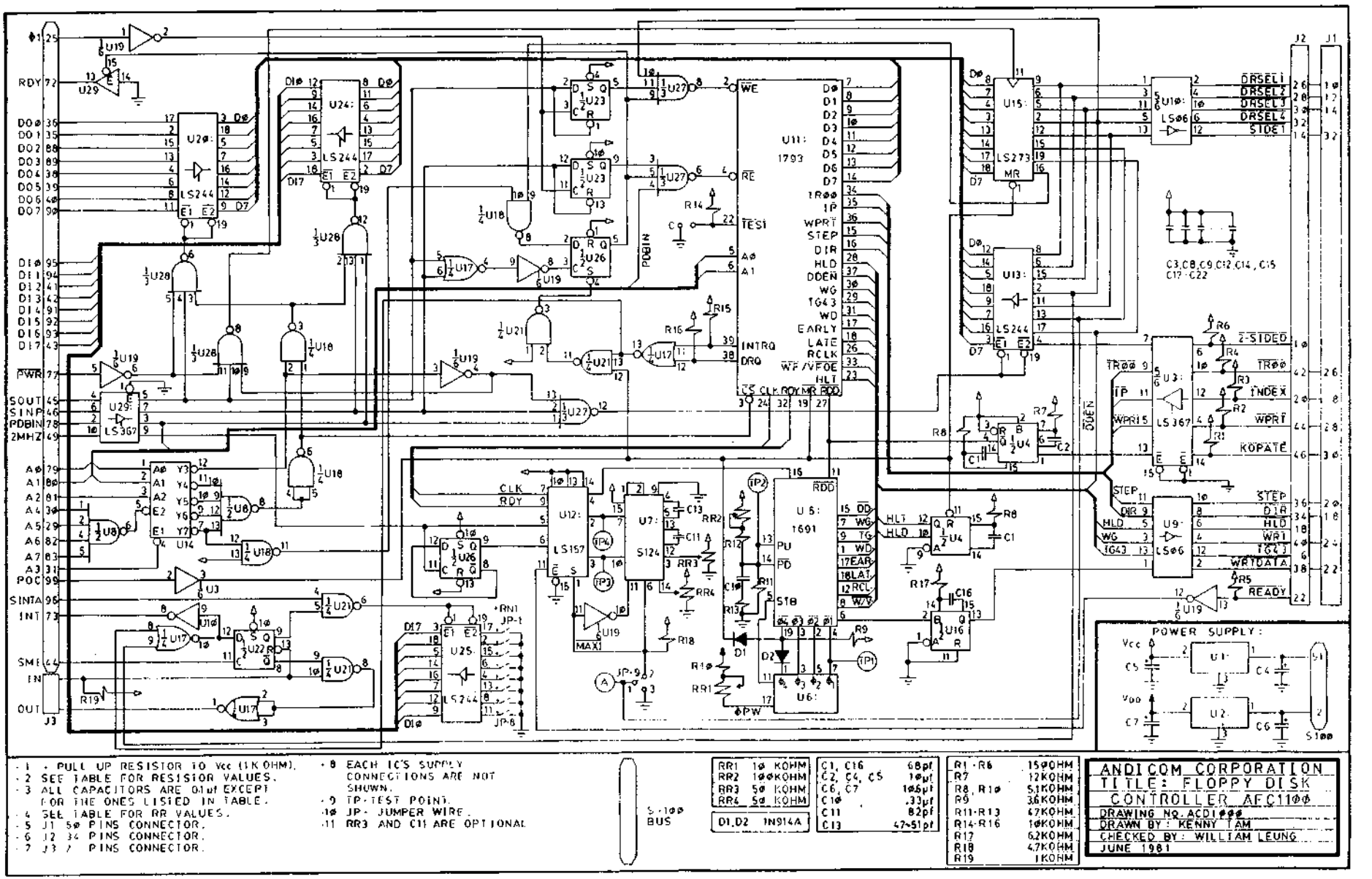
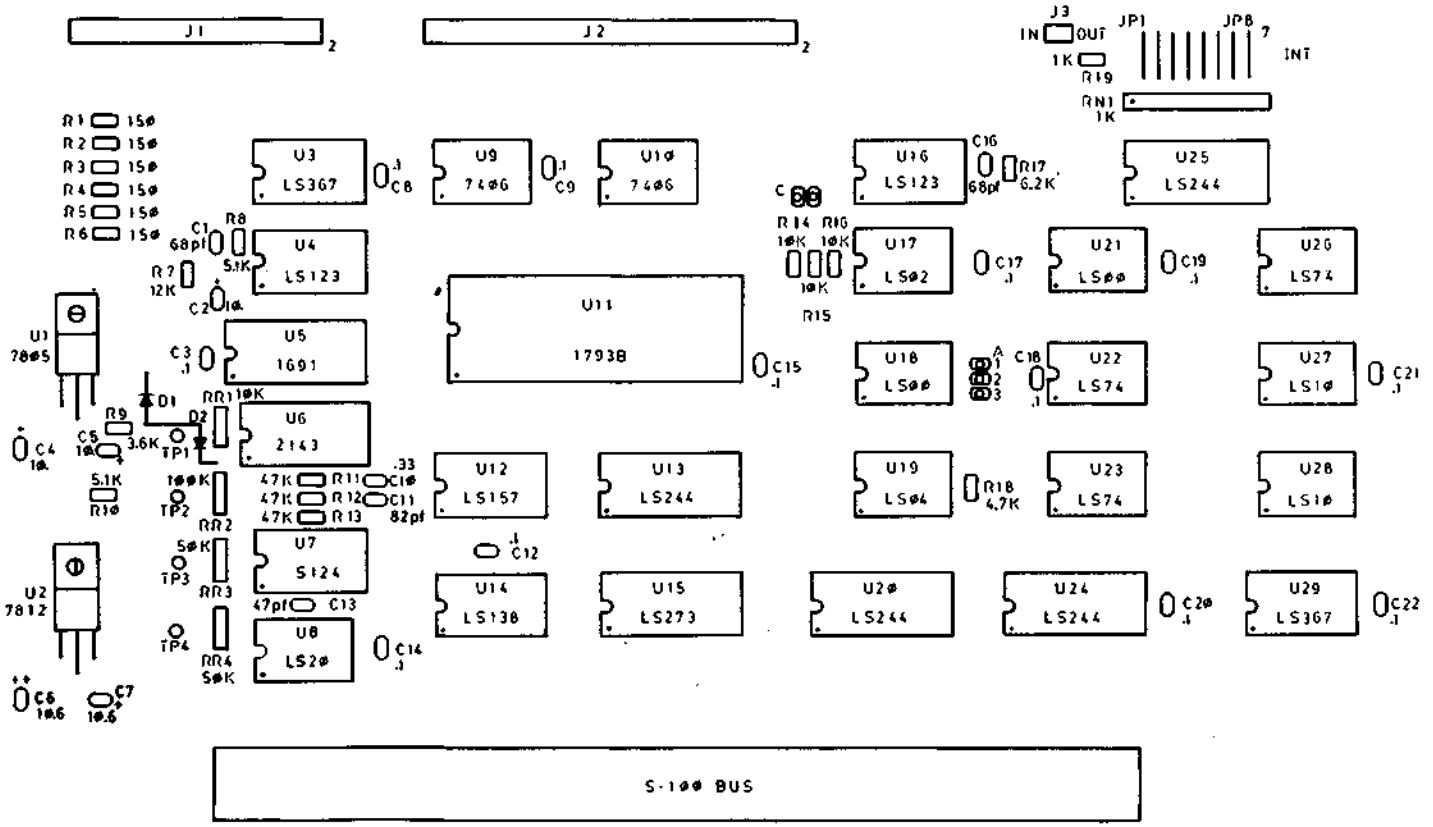


FIGURE 10- SCHEMATIC DIAGRAM OF FLOPPY DISK CONTROLLER BOARD



NOTE : R9, D1, AND D2 ARE LOCATED ON THE REVERSE SIDE OF THE BOARD.
ALL RESISTOR VALUES ARE IN OHMS.
ALL CAPACITOR VALUES ARE IN MICROFARADS UNLESS SPECIFIED.
D1, D2 ARE 1N914.

ANDICOM CORPORATION
TITLE: FLOPPY DISK CONTROLLER AFC 1100 COMPONENTS LAYOUT
DRAWING NO.: ACD 1001
DRAWN BY: K.TAM
CHECKED BY: W.LEUNG
JULY 1981

WESTERN DIGITAL
CORPORATION

FD179X Application Notes

NOVEMBER, 1980

INTRODUCTION

Over the past several years, the Floppy Disk Drive has become the most popular on-line storage device for mini and microcomputer systems. Its fast access time, reliability and low cost-per-bit ratio enables the Floppy Disk Drive to be *the* solution in mass storage for microprocessor systems. The drive interface to the Host system is standardized, allowing the OEM to substitute one drive for another with minimum hardware/ software modifications.

Since Floppy Disk Data is stored and retrieved as a self-clocking serial data stream, some means of separating the clock from the data and assembling this data in parallel form must be accomplished. Data is stored on individual Tracks of the media, requiring control of a stepper motor to move the Read/Write head to a predetermined Track. Byte sychronization must also be accomplished to insure that the parallel data is properly assembled. After all the design considerations are met, the final controller can consist of 40 or more TTL packages.

To alleviate the burden of Floppy Disk Controller design, Western Digital has developed a Family of LSI Floppy Disk controller devices. Through its own set of macro commands, the FD179X Controller Family will perform all the functions necessary to read and write data to the drive. Both the 8" standard and 5¼" minifloppy are supported with single or double density recording techniques. The FD179X is compatible with the IBM 3740 (FM) data format, or the System 34 (MFM) standards. Provisions for non-standard formats and variable sector lengths have been included to provide more storage capability per track. Requiring standard +5, +12 power supplies the FD179X is available in a standard 40 pin dual-in-line package.

The FD179X Family consists of 6 devices. The differences between these devices is summarized in Figure 1. The 1792 and 1794 are "single density only" devices, with the Double Density Enable pin (DDEN) left open by the user. Both True and inverted Data bus devices are available. Since the 179X can only drive one TTL Load, a true data bus system may use the 1791 with external inverting buffers to arrive at a true bus scheme. The 1795 and 1797 are identical to the 1791 and 1793, except a side select output has been added that is controlled through the Command Register.

SYSTEM DESIGN

The first consideration in Floppy Disk Design is to determine which type of drive to use. The choice ranges from single-density single sided mini-floppy to the 8" double-density double-sided drive. Figure 2 illustrates the various drive and data capacities associated with each type. Although the 8" double-density drive offers twice as much storage, a more complex data separator and the addition of Write Precompensation circuits are mandatory for reliable data transfers. Whether to go with 8" double-density or not is dependent upon PC board space and the additional circuitry needed to accurately recover data with extreme bit shifts. The byte transfer time defines the nominal time required to transfer one byte of data from the drive. If the CPU used cannot service a byte in this time, then a DMA scheme will probably be required. The 179X also needs a few microseconds for overhead, which is subtracted from the transfer time. Figure 3 shows the actual service times that the CPU must provide on a byte-by-byte basis. If these times are not met, bytes of data will be lost during a read or write operation. For each byte transferred, the 179X generates a DRQ (Data Request) signal on Pin 38. A bit is provided in the status register which is also set upon receipt of a byte from the Disk. The user has the option of reading the status register through program control or using the DRQ Line with DMA or interrupt schemes. When the data register is read, both the status register DRQ bit and the DRQ Line are automatically reset. The next full byte will again set the DRQ and the process continues until the sector(s) are read. The Write operation works exactly the same way, except a WRITE to the Data Register causes a reset of both DRQ's.

RECORDING FORMATS

The FD179X accepts data from the disk in a Frequency-Modulated (FM) or Modified-Frequency-Modulated (MFM) Format. Shown in Figures 4A and 4B are both these Formats when writing a Hexidecimal byte of 'D2'. In the FM mode, the 8 bits of data are broken up into "bit cells." Each bit cell begins with a clock pulse and the center of the bit cell defines the data. If the data bit = 0, no pulse is written; if the data = 1, a pulse is written in the center of the cell. For the 8" drive, each clock is written 4 microseconds apart.

In the MFM mode, clocks are decoded into the data stream. The byte is again broken up into bit cells, with the data bit written in the center of the bit cell if data = 1. Clocks are only written if both surrounding data bits are zero. Figure 4B shows that this occurs only once between Bit cell 4 and 5. Using this encoding scheme, pulses can occur 2, 3 or 4 microseconds apart. The bit cell time is now 2 microseconds: twice as much data can be recorded without increasing the Frequency rate due to this encoding scheme.

The 179X was designed to be compatible with the IBM 3740 (FM) and System 34 (MFM) Formats. Although most users do not have a need for data exchange with IBM mainframes, taking advantage of these well studied formats will insure a high degree of system performance. The 179X will allow a change in gap fields and sector lengths to increase usable storage capacity, but variations away from these standards is not recommended. Both IBM standards are soft-sector format. Because of the wide variation in address marks, the 179X can only support soft-sectored media. Hard sectored diskettes have continued to lose popularity, mainly due to the unavailability of a standard and the limitation of sector lengths imposed by the physical sector holes in the diskette.

PROCESSOR INTERFACE

The Interface of the 179X to the CPU consists of an 8-bit Bi-directional bus, read/write controls and optional interrupt lines. By selecting the device via the CHIP SELECT Line, each of the five internal registers can be accessed.

Shown below are the registers and their addresses:

PIN 3 CS	PIN 6 A_1	PIN 5 A_0	PIN 4 $\overline{RE}=0$	PIN 2 $\overline{WE}=0$
0	0	0	STATUS REG	COMMAND REG
0	0	1	TRACK REG	TRACK REG
0	1	0	SECTOR REG	SECTOR REG
0	1	1	DATA REG	DATA REG
1	X	X	HI-Z	HI-Z

Each time a command is issued to the 179X, the Busy bit is set and the INTRQ (Interrupt Request) Line is reset. The user has the option of checking the busy bit or use the INTRQ Line to denote command completion. The Busy bit will be reset whenever the 179X is idle and awaiting a new command. The INTRQ Line, once set, can only be reset by a READ of the status register or issuing a new command. The MR (Master Reset) Line does not affect INTRQ.

The A_0, A_1, Lines used for register selections can be configured at the CPU in a variety of ways. These lines may actually tie to CPU address lines, in which case the 179X will be memory-mapped and addressed like RAM. They may also be used under Program Control by tying to a port device such as the 8255, 6820, etc. As a diagnostic tool when checking out the CPU interface, the Track and Sector registers should respond like "RAM" when the 179X is idle (Busy = INTRQ = 0).

Because of internal synchronization cycles, certain time delays must be introduced when operating under Programmed I/O. The worst case delays are:

OPERATION	NEXT OPERATION	DELAY REQ'D
WRITE TO COMMAND REG	READ STATUS REGISTER	MFM = 14μs* FM = 28μs.
WRITE TO ANY REGISTER	READ FROM A DIFFERENT REG	NO DELAY

*NOTE: Times Double when CLK = 1MHz (5¼" drive)

Other CPU interface lines are CLK, $\overline{MR}$ and $\overline{DDEN}$. The CLK line should be 2MHz (8" drive) or 1MHz (5¼" drive) with a 50% duty cycle. Accuracy should be ±1% (crystal source) since all internal timing, including stepping rates, are based upon this clock.

The $\overline{MR}$ or Master Reset Line should be strobed a minimum of 50 microseconds upon each power-on condition. This line clears and initializes all internal registers and issues a restore command (Hex '03') on the rising edge. A quicker stepping rate can be written to the command register after a $\overline{MR}$, in which case the remaining steps will occur at the faster programmed rate. The 179X will issue a maximum of 255 stepping pulses in an attempt to expect the $\overline{TROO}$ line to go active low. This line should be connected to the drive's $\overline{TROO}$ sensor.

The $\overline{DDEN}$ line causes selection of either single density ($\overline{DDEN}$ = 1) or double density operation. $\overline{DDEN}$ should not be switched during a read or write operation.

FLOPPY DISK INTERFACE

The Floppy Disk Interface can be divided into three sections: Motor Control, Write Signals and Read Signals. All of these lines are capable of driving one TTL load and not compatible for direct connection to the drive. Most drives require an open-collector TTL interface with high current drive capability. This must be done on all outputs from the 179X. Inputs to the 179X may be buffered or tied to the Drives outputs, providing the appropriate resistor termination networks are used. Undershoot should not exceed −0.3 volts, while integrity of V_{IH} and V_{OH} levels should be kept within spec.

MOTOR CONTROL

Motor Control is accomplished by the STEP and DIRC Lines. The STEP Line issues stepping pulses with a period defined by the rate field in all Type I commands. The DIRC Line defines the direction of steps (DIRC = 1 STEP IN/DIRC = 0 STEP OUT).

Other Control Lines include the $\overline{IP}$ or Index Pulse. This Line is tied to the drives' Index L.E.D. *sensor* and makes an active transition for each revolution of the diskette. The $\overline{TROO}$ Line is another L.E.D. sensor that informs the 179X that the stepper motor is at its furthest position, over Track 00. The READY Line can be used for a number of functions, such as sensing "door open", Drive motor on, etc. Most drives provide a programmable READY Signal selected by option jumpers on the drive. The 179X will look at the ready signal prior to executing READ/WRITE commands. READY is *not* inspected during any Type I commands. All Type I commands will execute regardless of the Logic Level on this Line.

WRITE SIGNALS

Writing of data is accomplished by the use of the WD, WG, WF, TG43, EARLY and LATE Lines. The WG or Write Gate Line is used to enable write current at the drive's R/W head. It is made active prior to writing data on the disk. The WF or WRITE FAULT Line is used to inform the 179X of a failure in drive electronics. This signal is multiplexed with the VFOE Line and must be logically separated if required. Figure 5 illustrates three methods of demultiplexing.

The TG43 or "TRACK GREATER than 43" Line is used to decrease the Write current on the inner tracks, where bit densities are the highest. If not required on the drive, TG43 may be left open.

WRITE PRECOMPENSATION

The 179X provides three signals for double density Write Precompensation use. These signals are WRITE DATA, EARLY and LATE. When using single density drives (eighter 8" or 5¼"), Write Precompensation is not necessary and the WRITE DATA line is generally TTL Buffered and sent directly to the drive. In this mode, EARLY and LATE are left open.

For double density use, Write Precompensation is a function of the drive. Some manufacturers recommend Precompensating the 5¼" drive, while others do not. With the 8" drive, Precompensation may be specified from TRACK 43 on, or in most cases, all TRACKS. If the recommended Precompensation is not specified, check with the manufacturer for the proper configuration required.

The amount of Precompensation time also varies. A typical value will usually be specified from 100-300ns. Regardless of the parameters used, Write Precompensation must be done external to the 179X. When $\overline{DDEN}$ is tied low, EARLY or LATE will be activated at least 125ns. before and after the Write Data pulse. An Algorithm internal the 179X decides whether to raise EARLY or LATE, depending upon the previous bit pattern sent. As an example, suppose the recommended Precomp value has been specified at 150ns. The following action should be taken:

EARLY	LATE	ACTION TAKEN
0	0	delay WD by 150ns (nominal)
0	1	delay WD by 300ns (2X value)
1	0	do not delay WD

There are two methods of performing Write Precompensation:

1) External Delay elements
2) Digitally

Shown in Figure 6 is a Precomp circuit using the Western Digital 2143 clock generator as the delay element. The WD pulse from the 179X creates a strobe to the 2143, causing subsequent output pulses on the Ø1, Ø2 and Ø3 signals. The 5K Precomp adjust sets the desired Precomp value. Depending upon the condition of EARLY and LATE, Ø1 will be used for EARLY, Ø2 for nominal (EARLY = LATE = 0), and Ø3 for LATE. The use of "one-shots" or delay line in a Write Precompensation scheme offers the user the ability to vary the Precomp value. The Ø4 output resets the 74LS175 Latch in anticipation of the next WD pulse. Figure 7 shows the WD-EARLY/LATE relationship, while Figure 8 shows the timing of this write Precomp scheme.

Another method of Precomp is to perform the function digitally. Figure 9 illustrates a relationship between the WD pulse and the CLK pin, allowing a digital Precomp scheme. Figure 10 shows such a scheme with a preset Write Precompensation value of 250ns. The synchronous counter is used to generate 2MHz and 4MHz clock signals. The 2MHz clock is sent to the CLK input of the 179X and the 4MHz is used by the 4-bit shift register. When a WD pulse is not present, the 4MHz clock is shifting "ones" through the shift register and maintaining Q_D at a zero level. When a WD pulse is present, a zero is loaded at either A, B, or C depending upon the states of LATE, EN PRECOMP and EARLY. The zero is then shifted by the 4MHz clock until it reaches the Q_D output. The number of shift operations determines whether the WRITE DATA pulse is written early, nominal or late. If both FM and MFM operations is a system requirement, the output of this circuit should be disabled and the WD pulse should be sent directly to the drive.

DATA SEPARATION

The 179X has two inputs (RAW READ & RCLK) and one output (VFOE) for use by an external data separator. The RAW READ input must present clock and data pulses to the 179X, while the RCLK input provides a "window" or strobe signal to clock each RAW READ pulse into the device. An ideal Data Separator would have the leading edge of the RAW READ pulse occur in the exact center of the RCLK strobe.

Motor Speed Variation, Bit shifts and read amplifier recovery circuits all cause the RAW READ pulses to drift away from their nominal positions. As this occurs, the RAW READ pulses will shift left or right with respect to RCLK. Eventually, a pulse will make its transition outside of its RCLK window, causing either a CRC error or a Record-not-Found error at the 179X.

A Phase-Lock-Loop circuit is one method of achieving synchronization between the RCLK and RAW READ signals. As RAW READ pulses are fed to the PLL, minor adjustments of the free-running RCLK frequency can be made. If pulses are occurring too far apart, the RCLK frequency is *decreased* to keep synchronization. If pulses begin to occur closer together, RCLK is *increased* until this new higher frequency is achieved. In normal read operations, RCLK will be constantly adjusted in an attempt to match the incoming RAW READ frequency.

Another method of Data Separation is the Counter-Separator technique. The RCLK signal is again free-running at a nominal rate, until a RAW READ pulse occurs. The Separator then denotes the position of the pulse with respect to RCLK (by the counter value), and counts down to increase or decrease the current RCLK window. The next RCLK window will occur at a nominal rate and will continue to run at this frequency until another RAW READ pulse adjusts RCLK, but only the present window is adjusted.

Both PPL and Counter/Separator are acceptable methods of Data Separation. The PPL has the highest reliability because of its "tracking" capability and is recommended for 8" double density designs.

As a final note, the term "Data Separator" may be misleading, since the physical separation of clock and data bits are not actually performed. This term is used throughout the industry, and can better be described as a "Data Recovery Circuit" rather than a Data Separator.

The VFOE signal is an output from the 179X that signifies the head has been loaded and valid data pulses are appearing on the RAW READ line. It can be used to enable the Data Separator and to insure clean RCLK transitions to the 179X. Since some drives will output random pulses when the head is disengaged, VFOE can prevent an erratic RCLK signal during this time. If the Data Separator requires synchronization during a known pattern of one's or zero's, then RG (READ GATE) can be used. The RG signal will go active when the 179X is currently over a field of zeros or ones. RG is not available on the 1795/1797 devices, since this signal was replaced with the SSO (Side Select Output) Line.

Shown in Figure 11 is a 2½ IC Counter/Separator. The 74LS193 free runs at a frequency determined by the CRYCLK input. When a RAW READ pulse occurs, the counter is loaded with a starting count of '5'. When the RAW READ Line returns to a Logic 1, the counter counts down to zero and again free runs. The 74LS74 insures a 50% duty cycle to the 179X and performs a divide-by-two of the Q_D output.

Figure 12 illustrates another Counter/Separator utilizing a PROM as the count generator. Depending upon the RAW READ phase relationship to RCLK, the PROM is addressed and its data output is used as the counter value. A 16MHz clock is required for 8" double density, while an 8MHz clock can be used for single density.

Figure 13 shows a Phase-Lock-Loop data recovery circuit. The phase detector (U2, Figure 2) compares the phase of the SHAPED DATA pulse to the phase of VFO CLK ÷ 2. If VFO CLK ÷ 2 is lagging the SHAPED DATA pulse an output pulse on #9, U2 is generated. The filter/amplifier converts this pulse into a DC signal which increases the frequency of the VCO. If, correspondingly, CLK ÷ 2 is leading the SHAPED DATA pulse, an output pulse on #5, U2 is generated. This pulse is converted into a DC signal which decreases the frequency of the VCO. These two actions cause the VCO to track the frequency of the incoming READ DATA pulses. This correction process to keep the two signals in phase is constantly occurring because of spindle speed variation and circuit parameter variations.

The operating specifications for this circuit are as follows:

Free Running Frequency	2MHz
Capture Range	± 15%
Lock Up Time	50 microsec. "1111" or "0000" Pattern 100 Microsec "1010" Pattern

The RAW READ pulses are generated from the falling edge of the SHAPED DATA pulses. The pulses are also reshaped to meet the 179X requirements. VFO CLK ÷ 2 OR 4 is divided by 2 once again to obtain VFO CLK OUT whose frequency is that required by the 179X RCLK input. RCLK must be controlled by VFOE so VFOE is sampled on each rising edge of VFO CLK OUT. When VFOE goes active EN RCLK goes active in synchronization with VFO CLK OUT preventing any glitches on the RCLK output. When VFOE goes inactive EN RCLK goes inactive in synchronization with VFO CLK OUT, again preventing any glitches on the RCLK output.

Figure 14 illustrates a PPL data recovery circuit using the Western Digital 1691 Floppy Support device. Both data recovery and Write Precomp Logic is contained within the 1691, allowing low chip count and PLL reliability. The 74S124 supplies the free-running VCO output. The PUMP UP and PUMP DOWN signals from the 1691 are used to control the 74S124's frequency.

COMMAND USAGE

Whenever a command is successfully or unsuccessfully completed, the busy bit of the status register is reset and the INTRQ line is forced high. Command termination may be detected either way. The INTRQ can be tied to the host processor's interrupt with an appropriate service routine to terminate commands. The busy bit may be monitored with a user program and will achieve the same results through software. Performing both an INTRQ and a busy bit check is not recommended because a read of the status register to determine the condition of the busy bit will reset the INTRQ line. This can cause an INTRQ from not occurring.

RESTORE COMMAND

On some disk drives, it is possible to position the R/W head outward past Track 00 and prevent the TR00 line from going low unless a STEP IN is first performed. If this condition exists in the drive used, the RESTORE command will never detect a TR00. Issuing several STEP IN pulses before a RESTORE command will remedy this situation. The RESTORE and all other Type I commands will execute even though the READY bit indicates the drive is not ready (NOT READY = 1).

READ TRACK COMMAND

The READ TRACK command can be used to manually inspect data on a hard copy printout. Gaps, address marks and all data are brought in to the data register during this command. The READ TRACK command may be used to inspect diskettes for valid formatting and data fields as well as address marks. Since the 179X does not synchronize clock and data until the Index Address Mark is detected, data previous to this ID mark will not be valid. READ GATE (RG) is not actuated during this command.

READ ADDRESS COMMAND

In systems that use either multiple drives or sides, the read address command can be used to tell the host processor which drive or side is selected. The current position of the R/W head is also denoted in the six bytes of data that are sent to the computer.

TRACK	SIDE	SECTOR	CRS LENGTH	CRC 1	CRC 2

The READ ADDRESS command as well as all other Type II and Type III commands will not execute if the READY line is inactive (READY = 0). Instead, an interrupt will be generated and the NOT READY status bit will be set to a 1.

FORCED INTERRUPT COMMAND

The Forced Interrupt command is generally used to terminate a multiple sector command or to insure Type I status in the status register. The lower four bits of the command determine the conditional interrupt as follows:

I_0 = NOT-READY TO READY TRANSITION
I_1 = READY TO NOT-READY TRANSITION
I_2 = EVERY INDEX PULSE
I_3 = IMMEDIATE INTERRUPT

Regardless of the conditional interrupt set, any command that is currently being executed when the Forced Interrupt command is loaded will immediately be terminated and the busy bit will be reset indicating an idle condition.

Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred.

The conditional interrupt is enabled when the corresponding bit positions of the command ($I_3 - I_0$) are set to a 1. If $I_3 - I_0$ are all set to zero, no interrupt will occur, but any command presently under execution will be immediately terminated upon receipt of the Force Interrupt command (HEX D0).

As usual, to clear the interrupt a read of the status register or a write to the command register is required. The exception is when using the immediate interrupt condition (I_3 = 1). If this command is loaded into the command register, an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt; another forced interrupt command with $I_3 - I_0$ = 0 must be loaded into the command register in order to reset the INTRQ from this condition.

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition (I_1 = 1) and the Every Index Pulse (I_2 = 1) are both set, the resultant command would be HEX "DA". The "OR" function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.

DATA RECOVERY

Occasionally, the R/W head of the disk drive may get "off track", and dust or dirt may get trapped on the media. Both of these conditions will cause a RECORD NOT FOUND and/or a CRC error to occur. This "soft error" can usually be recovered by the following procedure:

1. Issue the command again
2. Unload and load the head and repeat step
3. Issue a restore, seek the track, and repeat step 1

If RNF or CRC errors are still occurring after trying these methods, a "hard error" may exist. This is usually caused by improper disk handling, exposure to high magnetic fields, etc. and generally results in destroying portions or tracks of the diskette.

FIGURE 1. DEVICE CHARACTERISTICS

DEVICE	SNGL DENSITY	DBLE DENSITY	INVERTED BUS	TRUE BUS	DOUBLE-SIDED
1791	X	X	X		
1792	X		X		
1793	X	X		X	
1794	X			X	
1795	X	X	X		X
1797	X	X		X	X

FIGURE 2. STORAGE CAPACITIES

SIZE	DENSITY	SIDES	UNFORMATTED CAPACITY (NOMINAL)		BYTE TRANSFER TIME	FORMATTED CAPACITY	
			PER TRACK	PER DISK		PER TRACK	PER DISK
5¼"	SINGLE	1	3125	109,375*	64μs	2304**	80,640
5¼"	DOUBLE	1	6250	218,750	32μs	4608***	161,280
5¼"	SINGLE	2	3125	218,750	64μs	2304	161,280
5¼"	DOUBLE	2	6250	437,500	32μs	4608	322,560
8"	SINGLE	1	5208	401,016	32μs	3328	256,256
8"	DOUBLE	1	10,416	802,032	16μs	6656	512,512
8"	SINGLE	2	5208	802,032	32μs	3328	512,512
8"	DOUBLE	2	10,416	1,604,064	16μs	6656	1,025,024

*Based on 35 Tracks/Side
**Based on 18 Sectors/Track (128 byte/sec)
***Based on 18 Sectors/Track (256 bytes/sec)

FIGURE 3. NOMINAL VS. WORSE CASE SERVICE TIME

SIZE	DENSITY	NOMINAL TRANSFER TIME	WORST-CASE 179X SERVICE TIME	
			READ	WRITE
5¼"	SINGLE	64μs	55.0μs	47.0μs
5¼"	DOUBLE	32μs	27.5μs	23.5μs
8"	SINGLE	32μs	27.5μs	23.5μs
8"	DOUBLE	16μs	13.5μs	11.5μs

FIGURE 4A. FM RECORDING

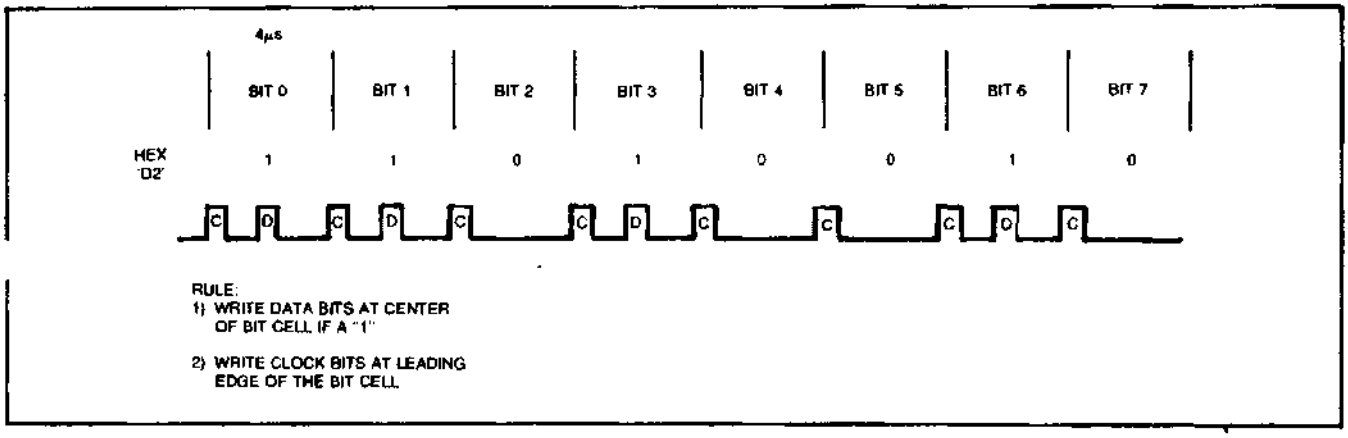


FIGURE 4B. MFM RECORDING

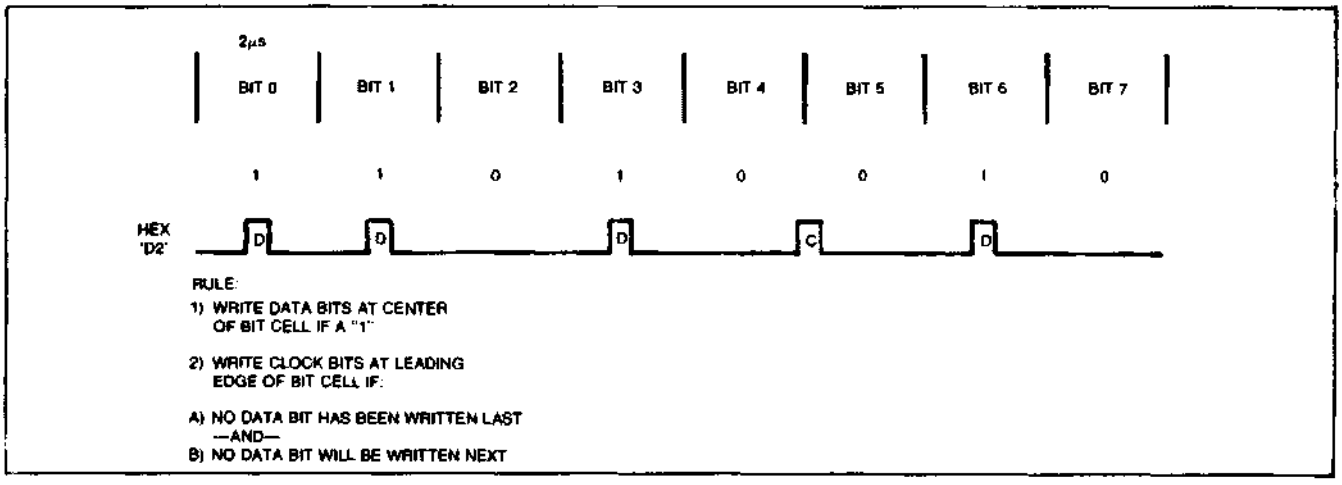
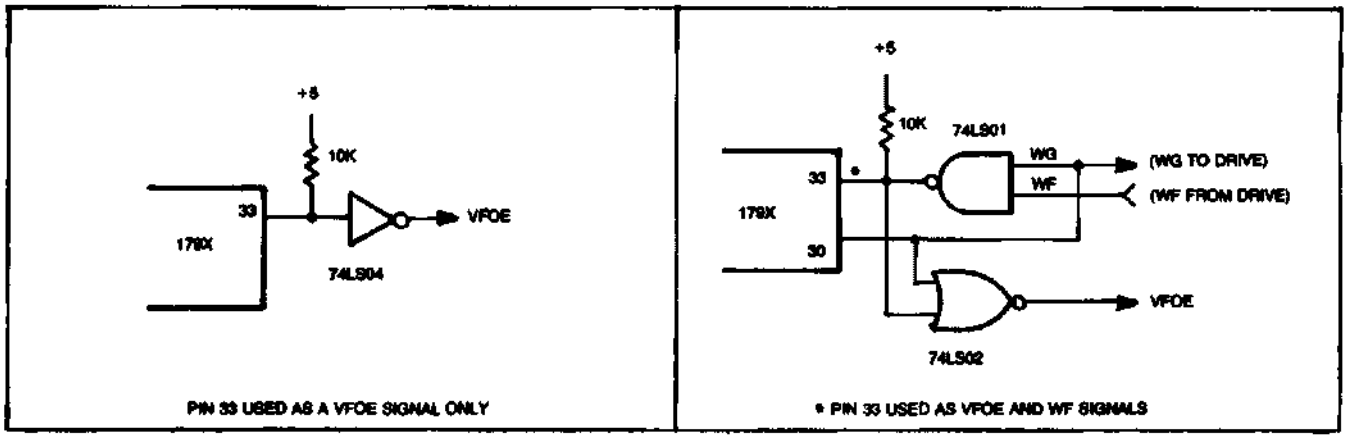
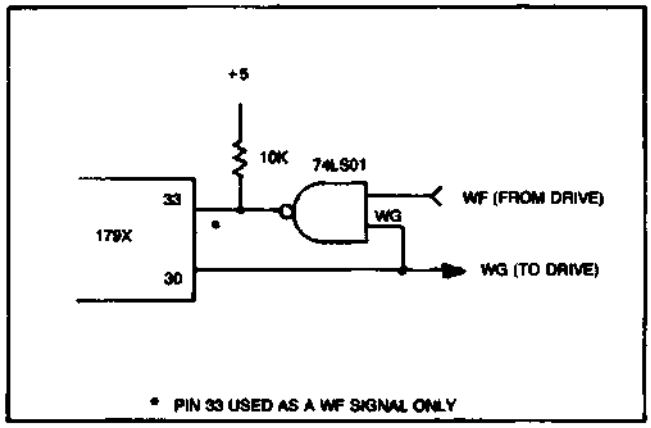


FIGURE 5. WF/VFOE DEMULTIPLEXING CIRCUITRY





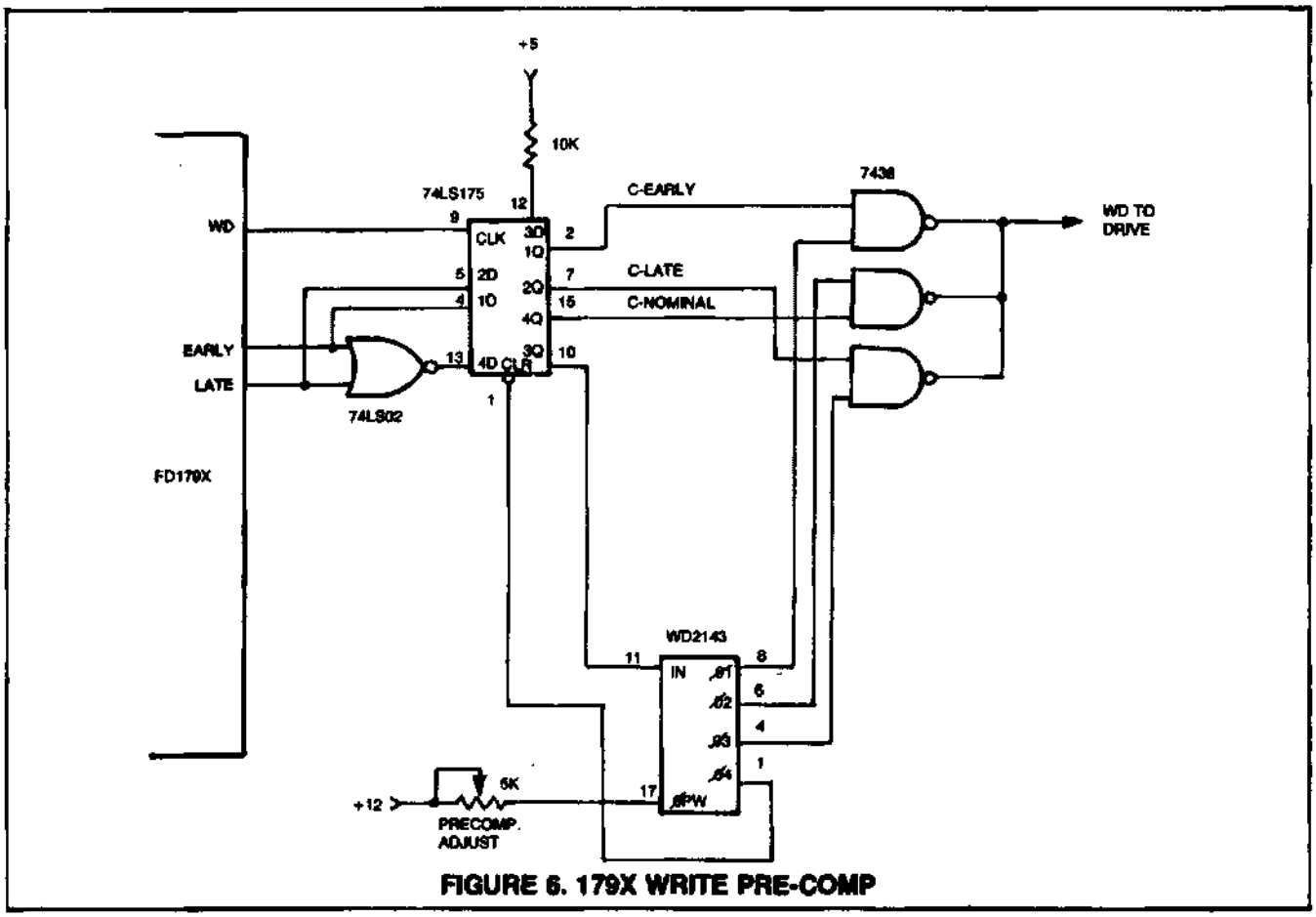


FIGURE 6. 179X WRITE PRE-COMP

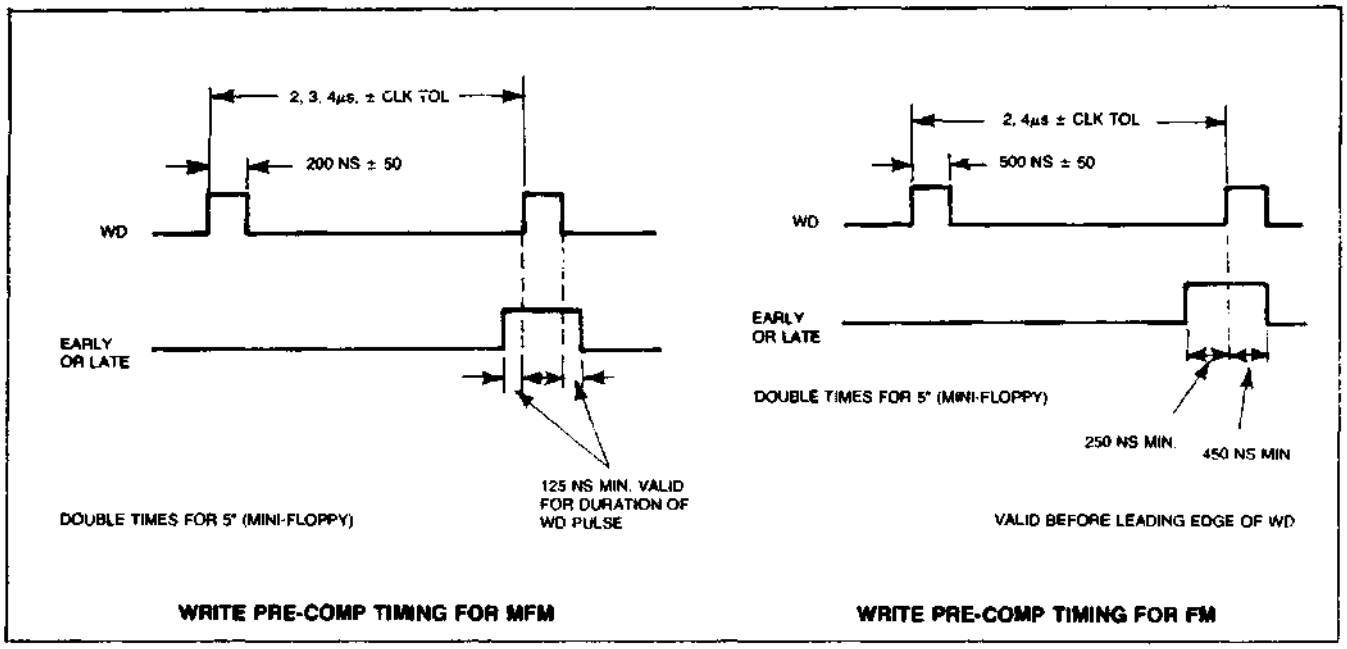


FIGURE 7. WRITE PRE-COMP TIMING

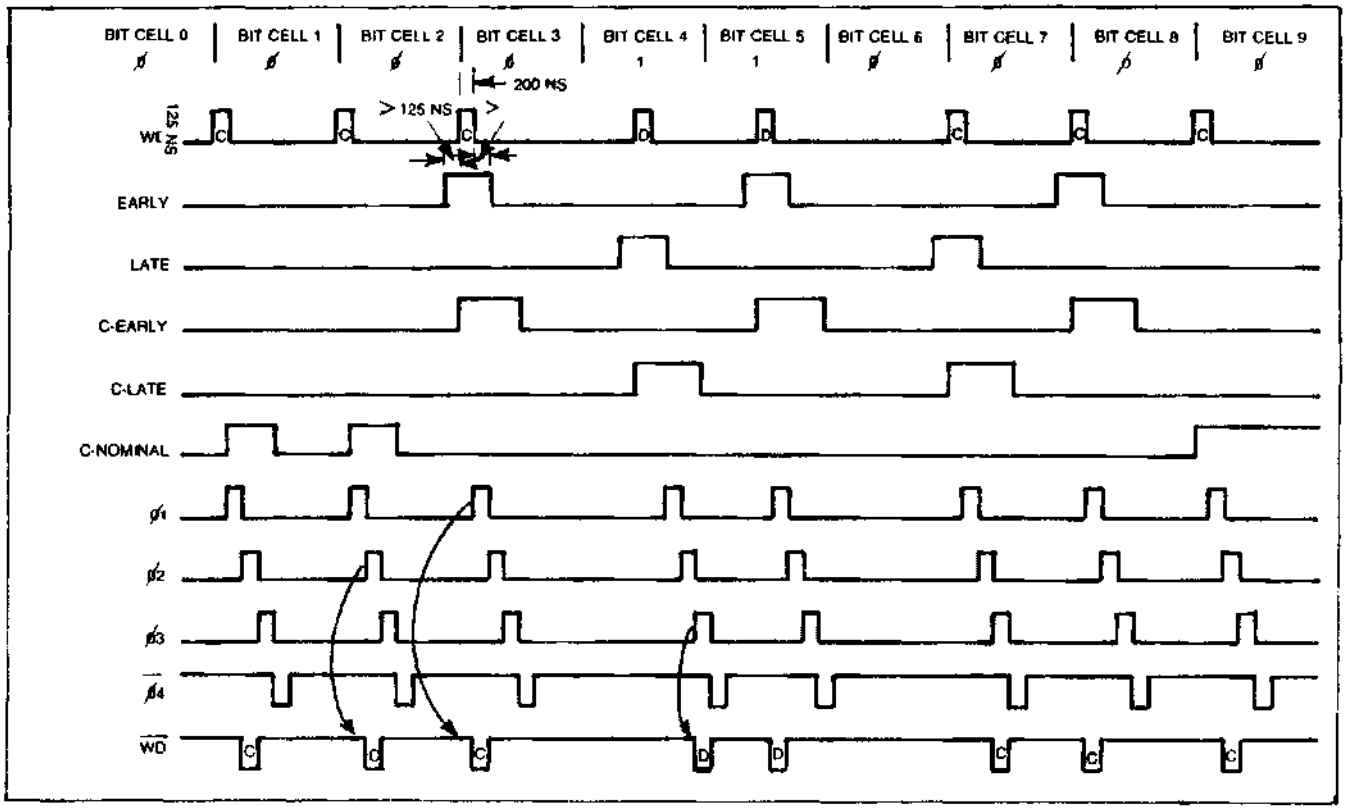


FIGURE 8. PRECOMP TIMING FOR CIRCUIT IN FIGURE 6

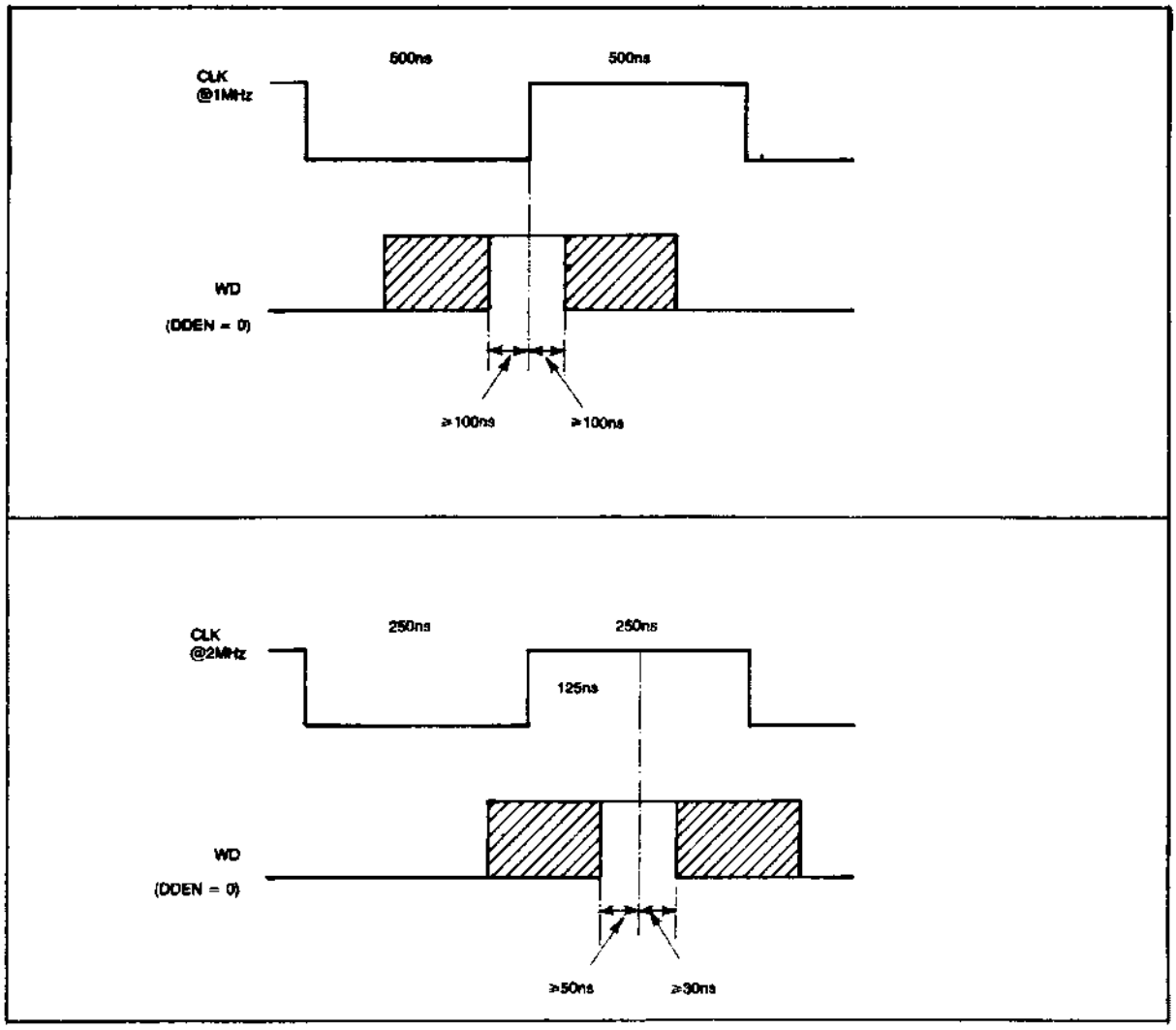


FIGURE 9. WD/CLK RELATIONSHIP FOR WRITE PRECOMP USE

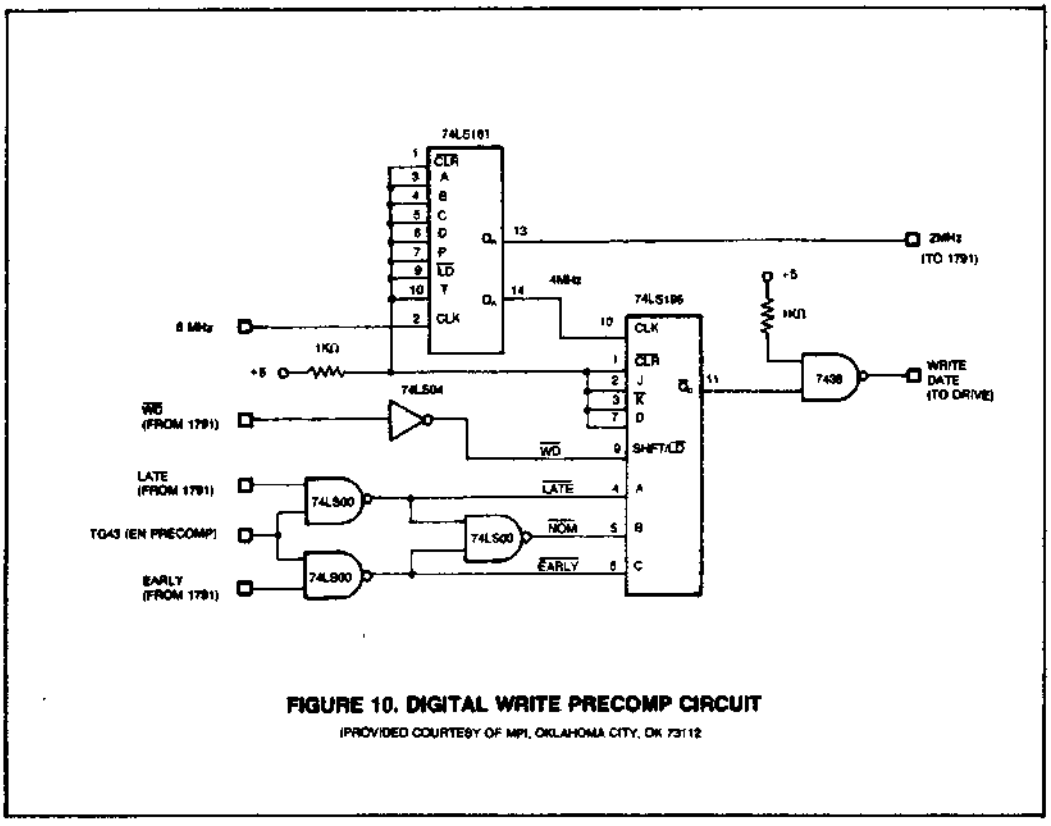
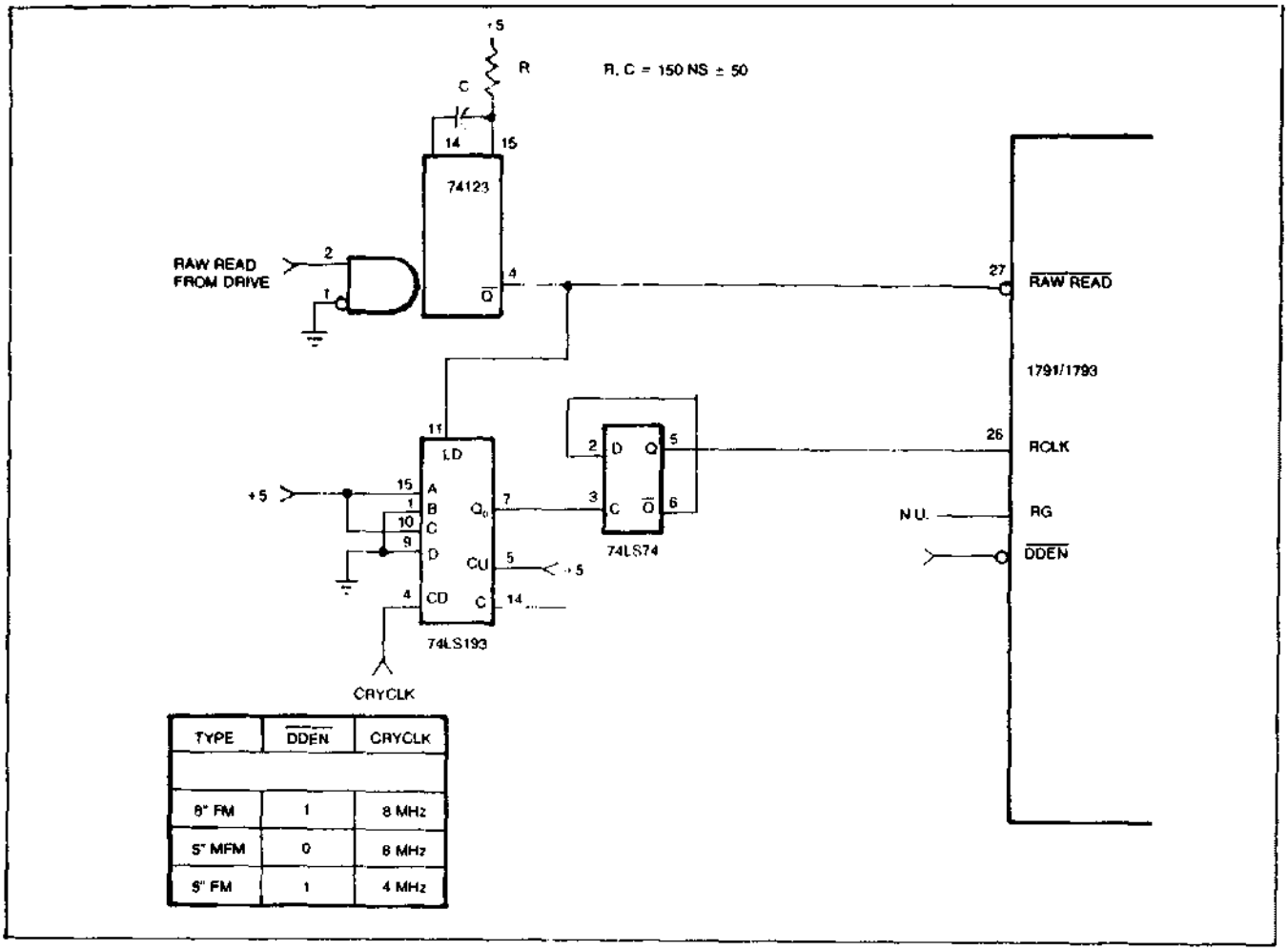


FIGURE 10. DIGITAL WRITE PRECOMP CIRCUIT

(PROVIDED COURTESY OF MPI, OKLAHOMA CITY, OK 73112



TYPE	$\overline{\text{DDEN}}$	CRYCLK
8" FM	1	8 MHz
5" MFM	0	8 MHz
5" FM	1	4 MHz

FIGURE 11. COUNTER/SEPARATOR

745288 PROGRAMMING TABLE

ADDRESS	DATA	ACTION TAKEN
00	01	NONE
01	01	RETARD BY 1 COUNT
02	02	
03	03	
04	03	RETARD BY 2 COUNTS
05	04	
06	05	
07	06	
08	0B	ADVANCE BY 2 COUNTS
09	0D	
0A	0C	
0B	0E	
0C	0F	
0D	0F	ADVANCE BY 1 COUNT
0E	00	
0F	01	
10	01	FREE RUN
11	02	
12	03	
13	04	
14	05	
15	06	
16	07	
17	08	
18	09	
19	0A	
1A	0B	
1B	0C	
1C	0D	
1D	0E	
1E	0F	
1F	00	

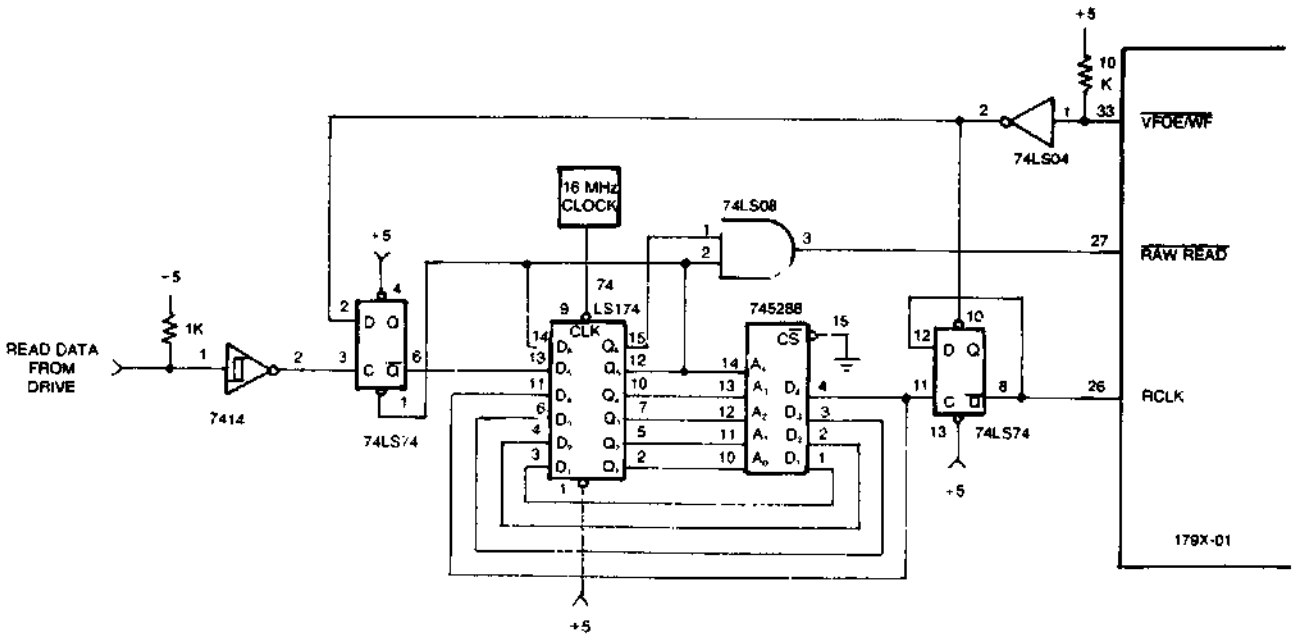


FIGURE 12. 179X DATA SEPARATOR

(PROVIDED COURTESY OF ANDROMEDA SYSTEMS, PANORAMA CITY, CA 91402)

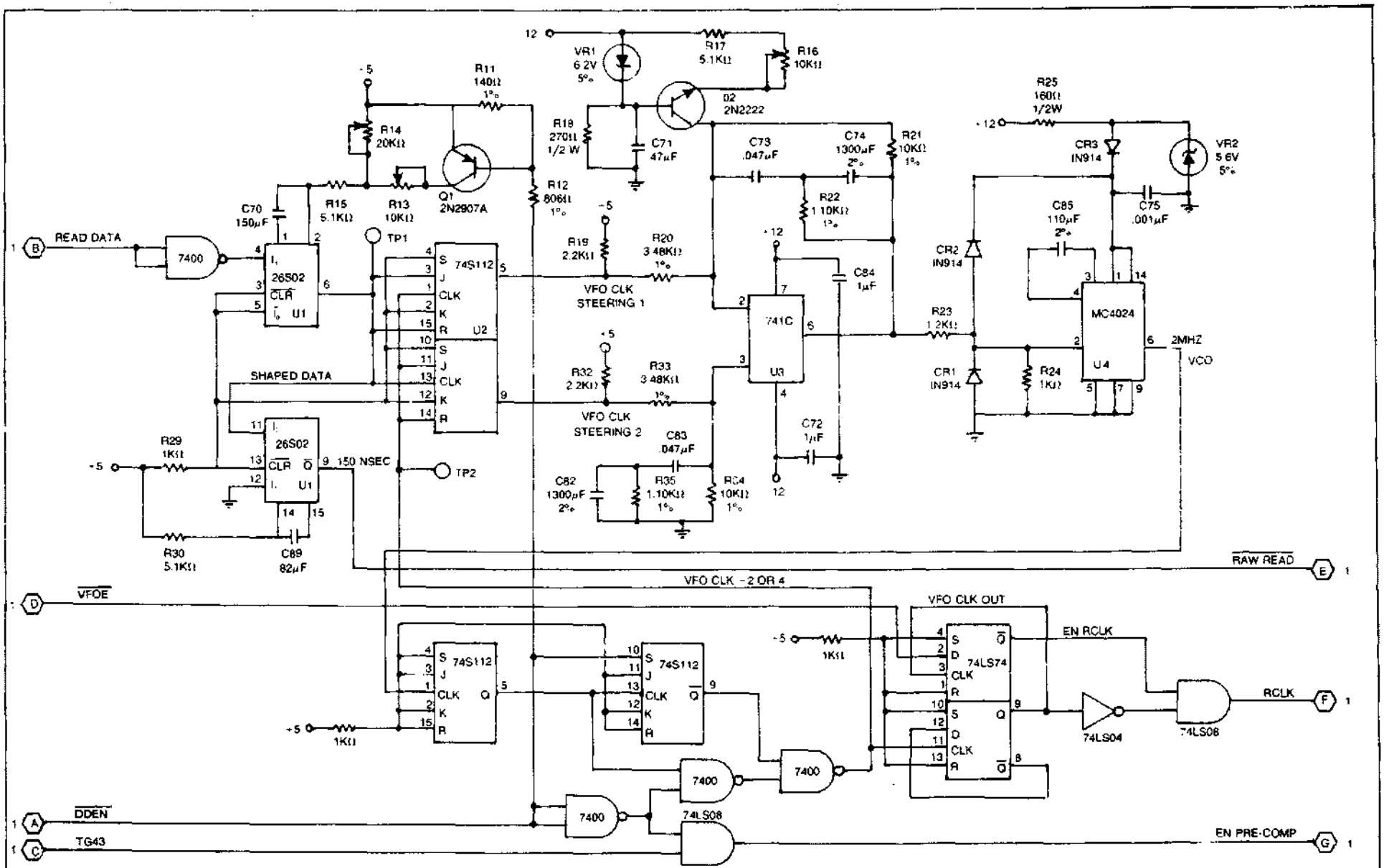
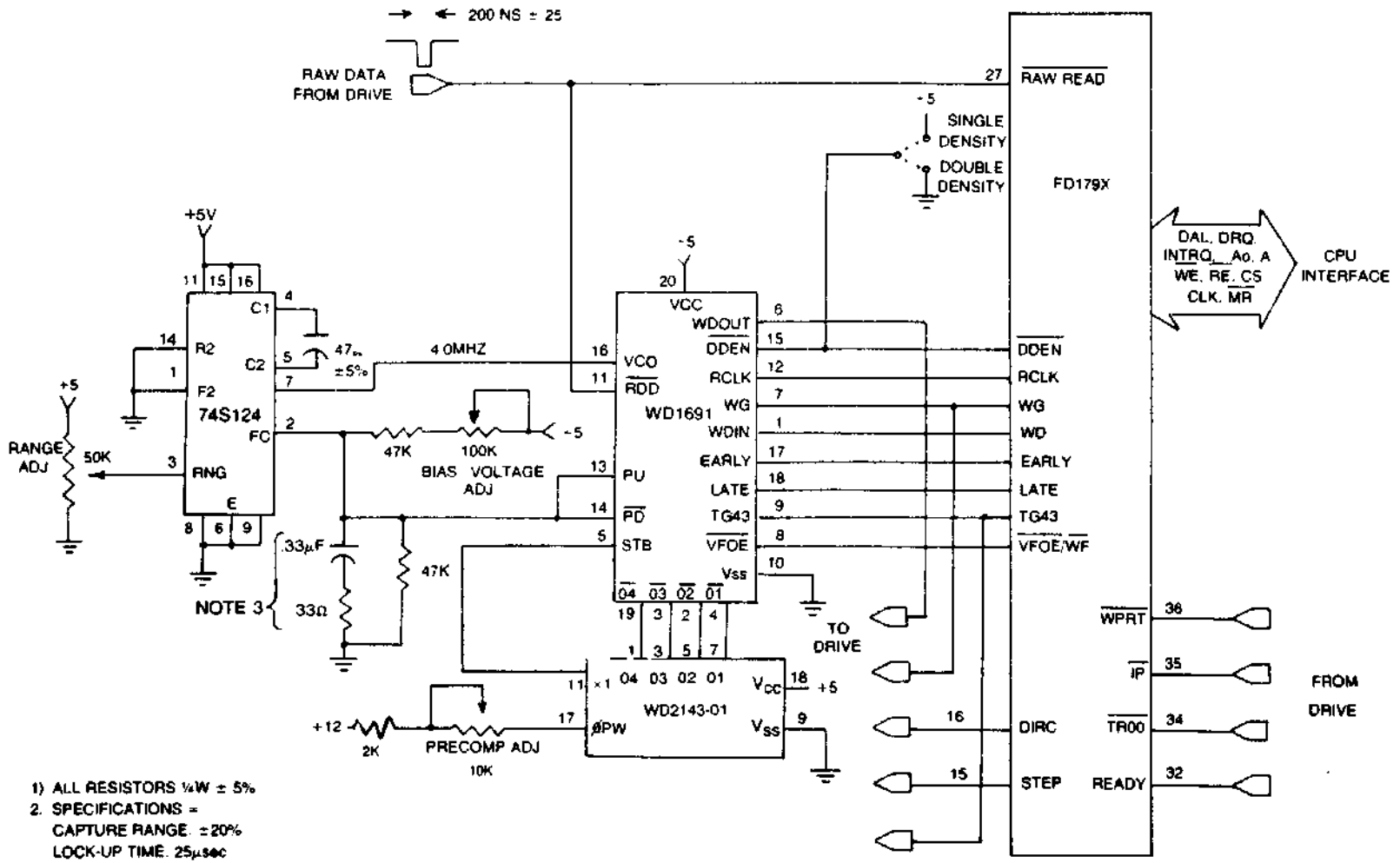


FIGURE 13. PLL DATA RECOVERY CIRCUIT

(PROVIDED COURTESY OF MPI, OKLAHOMA CITY, OK 73112)



1) ALL RESISTORS ¼W ± 5%
2. SPECIFICATIONS =
CAPTURE RANGE: ±20%
LOCK-UP TIME: 25µsec
(ALL ONE'S PATTERN, MFM)

3) FOR

5 1/4"	8
.68µf	.33µf
68Ω	33Ω

FIGURE 14. 8" SINGLE/DOUBLE DENSITY SYSTEM

COMMAND SUMMARY

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Sector	1	0	0	m	S	E	C	0
II	Write Sector	1	0	1	m	S	E	C	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

Note: Bits shown in TRUE form.

STEPPING RATES

CLK		2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
DDEN		0	1	0	1	X	X
R_1	R_0	TEST=1	TEST=1	TEST=1	TEST=1	TEST=0	TEST=0
0	0	3 ms	3 ms	6 ms	6 ms	184μs	368μs
0	1	6 ms	6 ms	12 ms	12 ms	190μs	380μs
1	0	10 ms	10 ms	20 ms	20 ms	198μs	396μs
1	1	15 ms	15 ms	30 ms	30 ms	208μs	416μs

FLAG SUMMARY

TYPE I COMMANDS

h = Head Load Flag (Bit 3)

h = 1, Load head at beginning
h = 0, Unload head at beginning

V = Verify flag (Bit 2)

V = 1, Verify on destination track
V = 0, No verify

r_1r_0 = Stepping motor rate (Bits 1-0)

Refer to Table 1 for rate summary

u = Update flag (Bit 4)

u = 1, Update Track register
u = 0, No update

FLAG SUMMARY

TYPE II & III COMMANDS

m = Multiple Record flag (Bit 4)

m = 0, Single Record
m = 1, Multiple Records

a_0 = Data Address Mark (Bit 0)

a_0 = 0, FB (Data Mark)
a_0 = 1, F8 (Deleted Data Mark)

E = 15 ms Delay (2MHz)

E = 1, 15 ms delay
E = 0, no 15 ms delay

S = Side Select Flat

S = 0, Compare for Side 0
S = 1, Compare for Side 1

C = Side Compare Flag

C = 0, disable side select compare
C = 1, enable side select compare

FLAG SUMMARY

TYPE IV COMMAND

Ii = Interrupt Condition flags (Bits 3-0)

I0 = 1, Not-Ready to Ready Transition
I1 = 1, Ready to Not-Ready Transition
I2 = 1, Index Pulse
I3 = 1, Immediate Interrupt

$I_3 - I_0$ = 0, Terminate with no Interrupt

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

WESTERN DIGITAL
CORPORATION

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NEWPORT BEACH, CA 92663 (714) 557-3550,TWX 910-595-1139

WESTERN DIGITAL
CORPORATION

FD 179X-02 Floppy Disk Formatter/Controller Family

MAY 1980

FEATURES

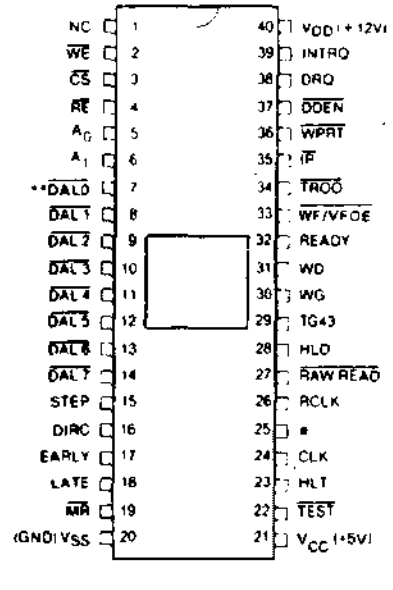
- TWO VFO CONTROL SIGNALS
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
- READ MODE
  - Single/Multiple Sector Read with Automatic Search or Entire Track Read
  - Selectable 128 Byte or Variable length Sector
- WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Formatting
- SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-Chip Track and Sector Registers/Comprehensive Status Information
- PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Side Select Compare
- WRITE PRECOMPENSATION
- WINDOW EXTENSION
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- FD1792/4 IS SINGLE DENSITY ONLY
- FD1795/7 HAS A SIDE SELECT OUTPUT

179X-02 FAMILY CHARACTERISTICS

FEATURES	1791	1793	1795	1797
Single Density (FM)	X	X	X	X
Double Density (MFM)	X	X	X	X
True Data Bus		X		X
Inverted Data Bus	X		X	
Write Precomp	X	X	X	X
Side Selection Output			X	X

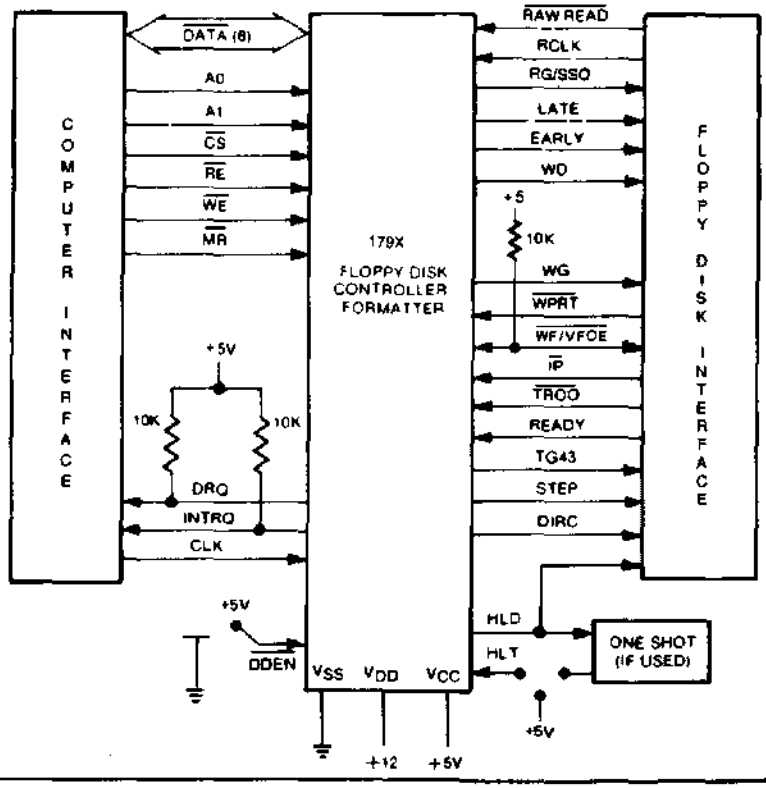
APPLICATIONS

FLOPPY DISK DRIVE INTERFACE
SINGLE OR MULTIPLE DRIVE CONTROLLER/ FORMATTER
NEW MINI-FLOPPY CONTROLLER



*1791/3 = RG 1795/7 = SSO
**1793/7 TRUE BUS

PIN CONNECTIONS



FD179X SYSTEM BLOCK DIAGRAM

GENERAL DESCRIPTION

The FD179X are MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD179X, which can be considered the end result of both the FD1771 and FD1781 designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD179X contains all the features of its predecessor the FD1771, plus the added features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD179X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bidirectional bus for data, status, and control word transfers. The FD179X is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD179X is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs. The 1793 is identical to the 1791 except the DAL lines are TRUE for systems that utilize true data busses.

The 1795/7 has a side select output for controlling double sided drives, and the 1792 and 1794 are "Single Density Only" versions of the 1791 and 1793. On these devices, DDEN must be left open.

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	NO CONNECTION	NC	Pin 1 is internally connected to a back bias generator and must be left open by the user.
19	$\overline{\text{MASTER RESET}}$	$\overline{\text{MR}}$	A logic low on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{\text{MR}}$ ACTIVE. When $\overline{\text{MR}}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V ±5%
40		V_{DD}	+12V ±5%
COMPUTER INTERFACE:			
2	$\overline{\text{WRITE ENABLE}}$	$\overline{\text{WE}}$	A logic low on this input gates data on the DAL into the selected register when $\overline{\text{CS}}$ is low.
3	$\overline{\text{CHIP SELECT}}$	$\overline{\text{CS}}$	A logic low on this input selects the chip and enables computer communication with the device.
4	$\overline{\text{READ ENABLE}}$	$\overline{\text{RE}}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{\text{CS}}$ is low.
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{\text{RE}}$ and $\overline{\text{WE}}$ control: A1 A0 $\overline{\text{RE}}$ $\overline{\text{WE}}$ 0 0 Status Reg Command Reg 0 1 Track Reg Track Reg 1 0 Sector Reg Sector Reg 1 1 Data Reg Data Reg
7-14	$\overline{\text{DATA ACCESS LINES}}$	$\overline{\text{DAL0}}$-$\overline{\text{DAL7}}$	Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by $\overline{\text{WE}}$ or transmitter enabled by $\overline{\text{RE}}$.
24	CLOCK	CLK	This input requires a free-running square wave clock for internal timing reference, 2 MHz for 8" drives, 1 MHz for mini-drives.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	EARLY	EARLY	Indicates that the WRITE DATA pulse occurring while Early is active (high) should be shifted early for write precompensation.
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated motors.
23	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged.
25	READ GATE (1791/3)	RG	A high level on this output indicates to the data separator circuitry that a field of zeros (or ones) has been encountered, and is used for synchronization.
25	SIDE SELECT OUTPUT (1795, 1797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When S = 1, SSO is set to a logic 1. When S = 0, SSO is set to a logic 0. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
31	WRITE DATA	WD	A 250 ns (MFM) or 500 ns (FM) pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$ / VFO ENABLE	$\overline{\text{WF}}$/$\overline{\text{VFOE}}$	This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a WF input. If WF = 0, any write command will immediately be terminated. When WG = 0, Pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1791/3, VFOE will remain low until the end of the Data Field.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FD179X that the Read/Write head is positioned over Track 00.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	This input informs the FD179X when the index hole is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	$\overline{\text{DOUBLE DENSITY}}$	$\overline{\text{DDEN}}$	This pin selects either single or double density operation. When $\overline{\text{DDEN}}$ = 0, double density is selected. When $\overline{\text{DDEN}}$ = 1, single density is selected. This line must be left open on the 1792/4

ORGANIZATION

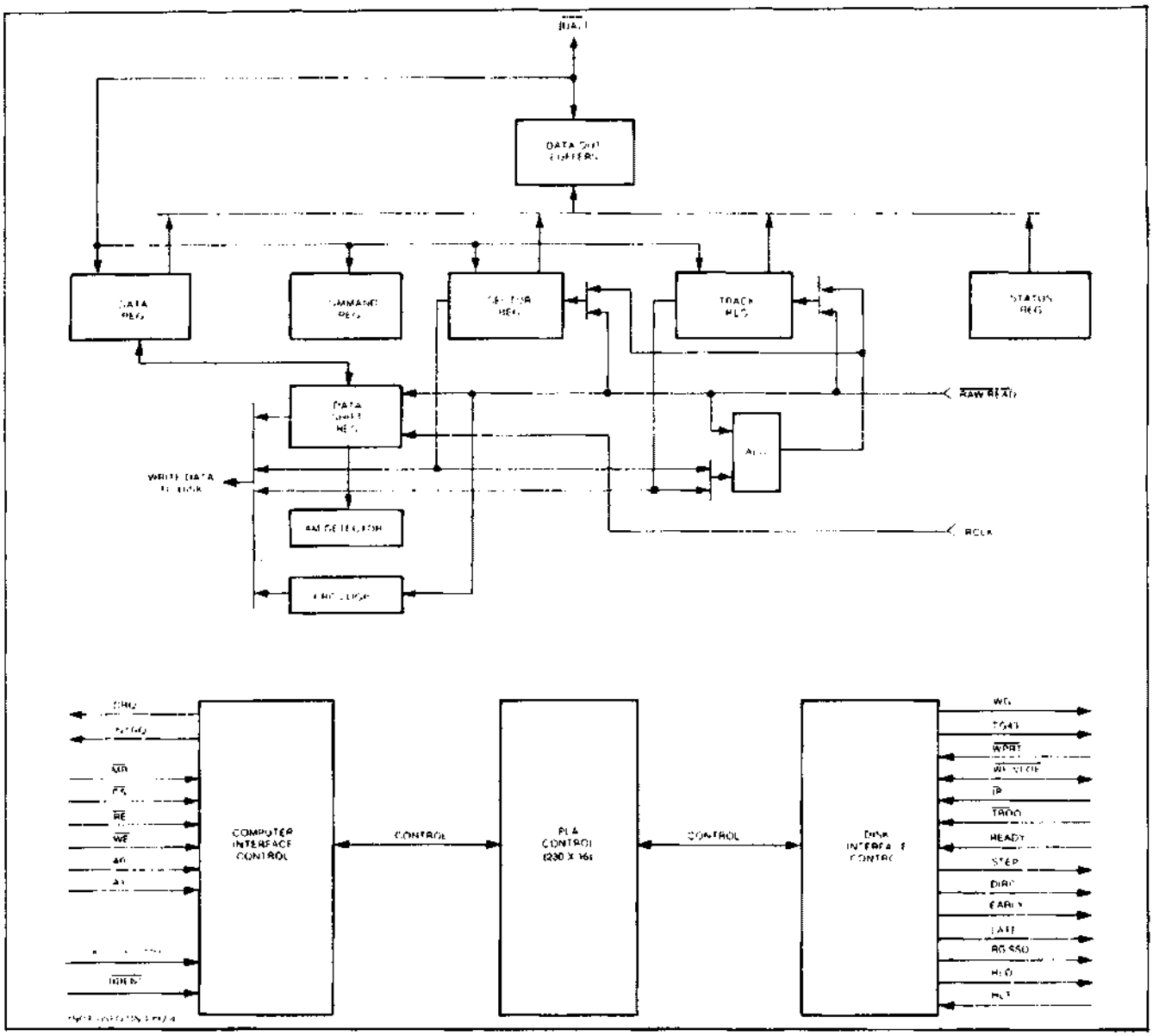
The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register—This 8-bit register assembles serial data from the Read Data input ($\overline{\text{RAW READ}}$) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register—This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register—This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.



FD179X BLOCK DIAGRAM

Sector Register (SR)—This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR)—This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR)—This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic—This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU)—The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control—All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD1791/3 has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN}$ = 0 double density (MFM) is assumed. When $\overline{DDEN}$ = 1, single density (FM) is assumed.

AM Detector—The address mark detector detects ID, data and index address marks during read and write operations.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines ($\overline{DAL}$) and associated control signals. The $\overline{DAL}$ are used to transfer Data, Status, and Control words out of, or into the FD179X. The $\overline{DAL}$ are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1-A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD179X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The 179X has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density. When the clock is at 2 MHz, the stepping rates of 3, 6, 10, and 15 ms are obtainable. When CLK equals 1 MHz these times are doubled.

HEAD POSITIONING

Five commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If $\overline{TEST}$ = 0, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

The rates (shown in Table 1) can be applied to a Step-Direction Motor through the device interface.

Step—A 2 μs (MFM) or 4 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

Direction (DIRC)—The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 μs before the first stepping pulse is generated.

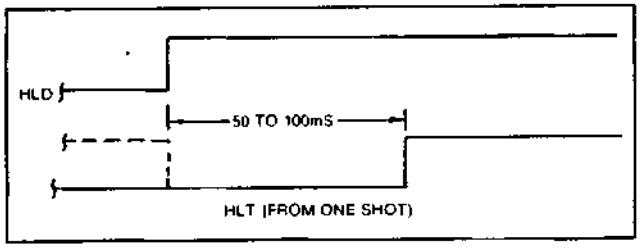
When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. The FD179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated.

Table 1. STEPPING RATES

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
$\overline{DDEN}$	0	1	0	1	X	X
R1 R0	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=0	$\overline{TEST}$=0
0 0	3 ms	3 ms	6 ms	6 ms	184μs	368μs
0 1	6 ms	6 ms	12 ms	12 ms	190μs	380μs
1 0	10 ms	10 ms	20 ms	20 ms	198μs	396μs
1 1	15 ms	15 ms	30 ms	30 ms	208μs	416μs

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the FD179X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load Timing (HLT) is an input to the FD179X which is used for the head engage time. When HLT = 1, the FD179X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FD179X.



HEAD LOAD TIMING

When both HLD and HLT are true, the FD179X will then read from or write to the media. The "and" of HLD and HLT appears as a status bit in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the FD179X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the FD179X then waits for HLT to occur.

For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{\text{DDEN}}$ should be placed to logical "1." For MFM formats, $\overline{\text{DDEN}}$ should be placed to a logical "0." Sector lengths are determined at format time by a special byte in the "ID" field. If this Sector length byte in the ID field is zero, then the sector length is 128 bytes. If 01 then 256 bytes. If 02, then 512 bytes. If 03, then the sector length is 1024 bytes. The number of sectors per track as far as the FD179X is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD179X is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track. (See Sector Length Table.)

For read operations, the FD179X requires $\overline{\text{RAW READ}}$ Data (Pin 27) signal which is a 250 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FD179X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FD179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG = 0), the $\overline{\text{VFOE}}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{\text{VFOE}}$ will go active when:

a) Both HLT and HLD are True
b) Settling Time, if programmed, has expired
c) The 179X is inspecting data off the disk

If $\overline{\text{WF}}/\overline{\text{VFOE}}$ is not used, leave open or tie to a 10K resistor to +5.

DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD179X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD179X terminates the current command, and sets the $\overline{\text{Write Fault}}$ bit (bit 5) in the Status Word. The $\overline{\text{Write Fault}}$ input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FD179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($\overline{\text{DDEN}}$ = 1) and 250 ns pulses in MFM ($\overline{\text{DDEN}}$ = 0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written early. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FD179X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

Whenever a Read or Write command (Type II or III) is received the FD179X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

COMMAND DESCRIPTION

The FD179X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 2.

Table 2. COMMAND SUMMARY

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Sector	1	0	0	m	F_2	E	F_1	0
II	Write Sector	1	0	1	m	F_2	E	F_1	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrrupt	1	1	0	1	I_3	I_2	I_1	I_0

Note: Bits shown in TRUE form.

Table 3. FLAG SUMMARY

TYPE I COMMANDS

h = Head Load Flag (Bit 3)

h = 1, Load head at beginning
h = 0, Unload head at beginning

V = Verify flag (Bit 2)

V = 1, Verify on destination track
V = 0, No verify

r_1r_0 = Stepping motor rate (Bits 1-0)

Refer to Table 1 for rate summary

u = Update flag (Bit 4)

u = 1, Update Track register
u = 0, No update

Table 4. FLAG SUMMARY

TYPE II & III COMMANDS

m = Multiple Record flag (Bit 4)

m = 0, Single Record
m = 1, Multiple Records

a_0 = Data Address Mark (Bit 0)

a_0 = 0, FB (Data Mark)
a_0 = 1, F8 (Deleted Data Mark)

E = 15 ms Delay (2MHz)

E = 1, 15 ms delay
E = 0, no 15 ms delay

(F_2) S = Side Select Flag (1791/3 only)

S = 0, Compare for Side 0
S = 1, Compare for Side 1

(F_1) C = Side Compare Flag (1791/3 only)

C = 0, disable side select compare
C = 1, enable side select compare

(F_1) S = Side Select Flag

(Bit 1, 1795/7 only)

S = 0 Update SSO to 0
S = 1 Update SSO to 1

(F_2) b = Sector Length Flag

(Bit 3, 1975/7 only)

	Sector Length Field			
	00	01	10	11
b = 0	256	512	1024	128
b = 1	128	256	512	1024

Table 5. FLAG SUMMARY

TYPE IV COMMAND

Ii = Interrupt Condition flags (Bits 3-0)

I0 = 1, Not-Ready to Ready Transition
I1 = 1, Ready to Not-Ready Transition
I2 = 1, Index Pulse
I3 = 1, Immediate Interrupt
I_3 -I_0 = 0, Terminate with no Interrupt

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field (r_0r_1), which determines the stepping motor rate as defined in Table 1.

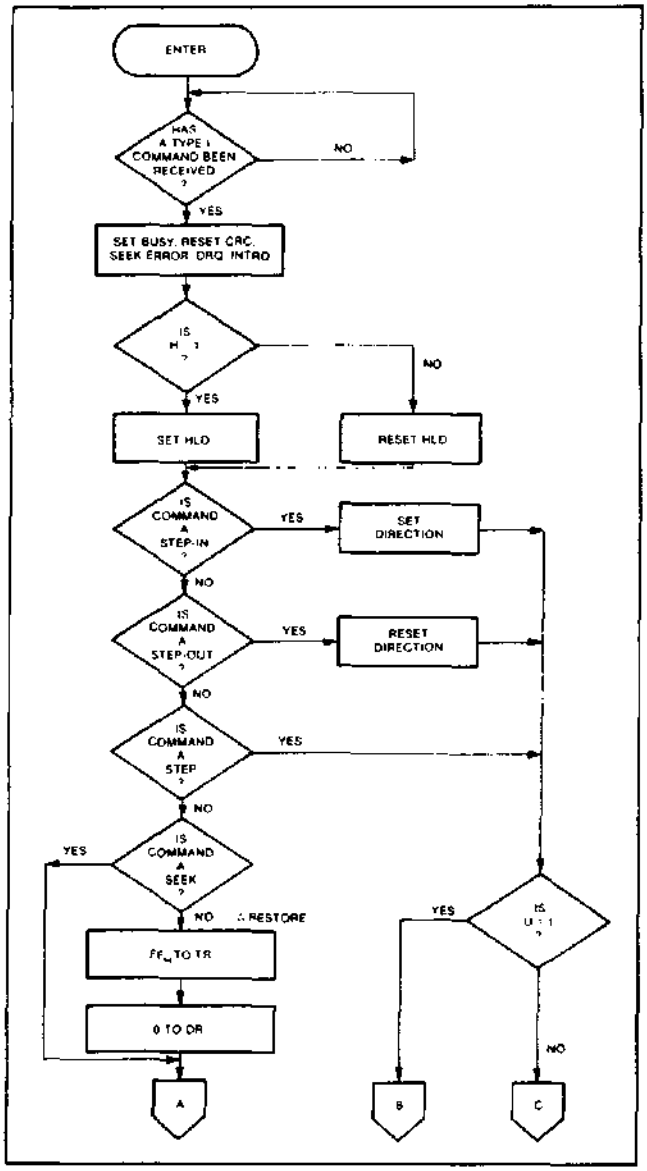
The Type I Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h = 1, the head is loaded at the beginning of the command (HLD output is made active). If h = 0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FD179X receives a command that specifically disengages the head. If the FD179X is idle (busy = 0) for 15 revolutions of the disk, the head will be automatically disengaged (HLD made inactive).

The Type I Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V = 1, a verification is performed, if V = 0, no verification is performed.

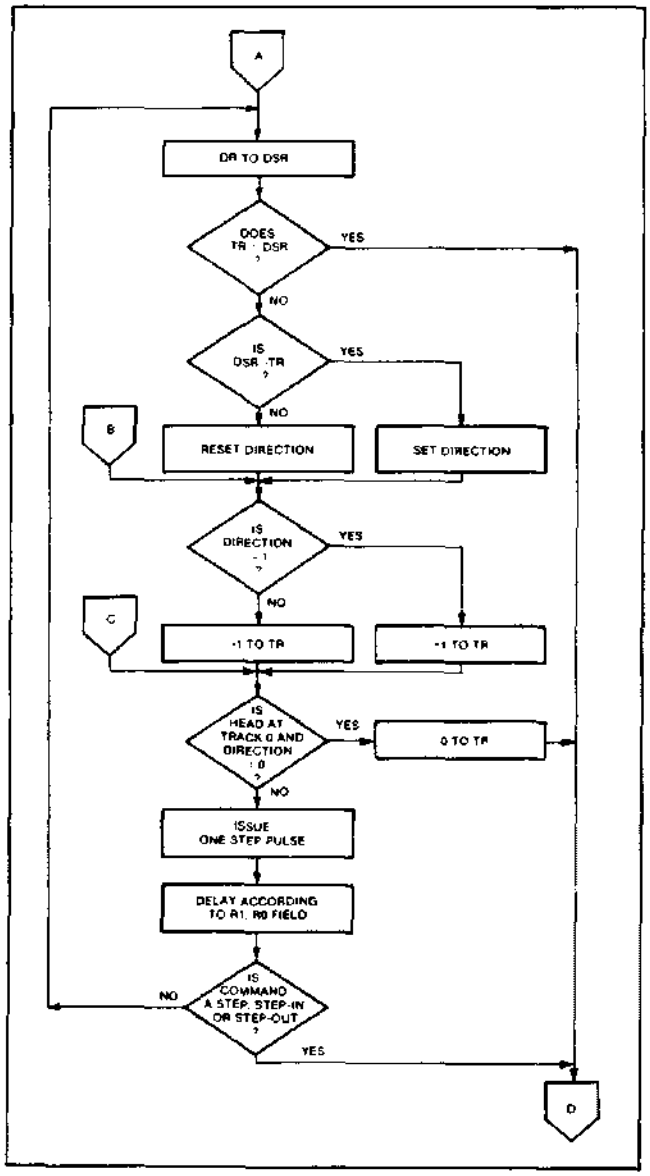
During verification, the head is loaded and after an internal 15 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match but there is valid ID CRC, an interrupt is generated, and Seek Error Status bit (Status bit 4) is set and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after four revolutions of the disk, the FD179X terminates the operation and sends an interrupt, (INTRQ).

The Step, Step-In, and Step-Out commands contain an Update flag (U). When U = 1, the track register is updated by one for each step. When U = 0, the track register is not updated.

On the 1795/7 devices, the SSO output is not affected during Type 1 commands, and an internal side compare does not take place when the (V) Verify Flag is on.



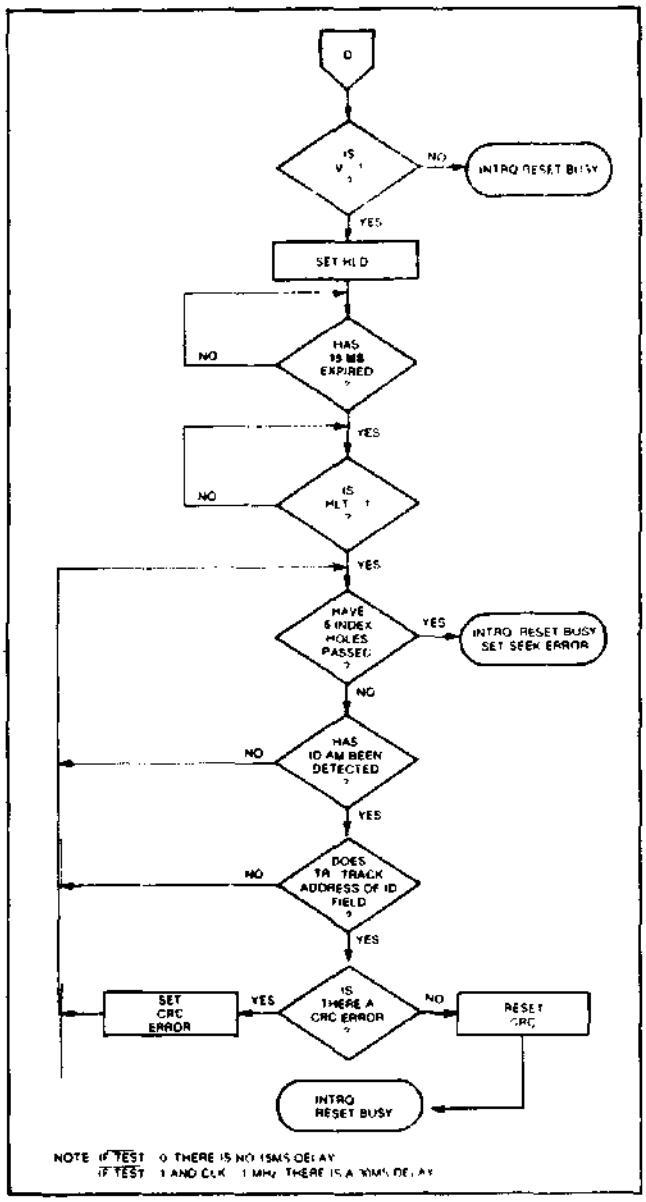
TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the rate field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FD179X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when $\overline{MR}$ goes from an active to an inactive state.



TYPE I COMMAND FLOW

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD179X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

Upon receipt of this command, the FD179X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the rate field, a verification takes place if the V flag is on. If the u flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the rate field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 0. If the u flag is on, the Track Register is decremented by one. After a delay determined by the rate field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

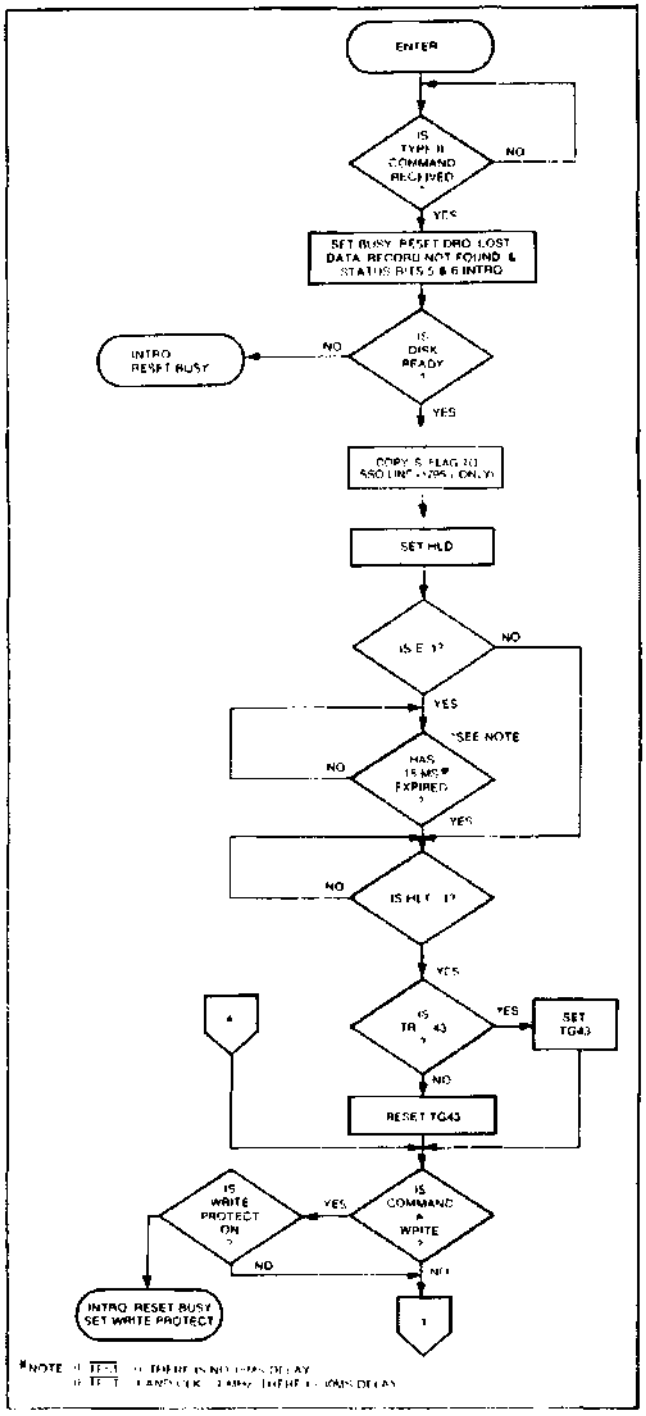
The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay. The ID field and Data Field format are shown on page 13.

When an ID field is located on the disk, the FD179X compares the Track Number on the ID field with the Track Register. If there is not a match, the next en-

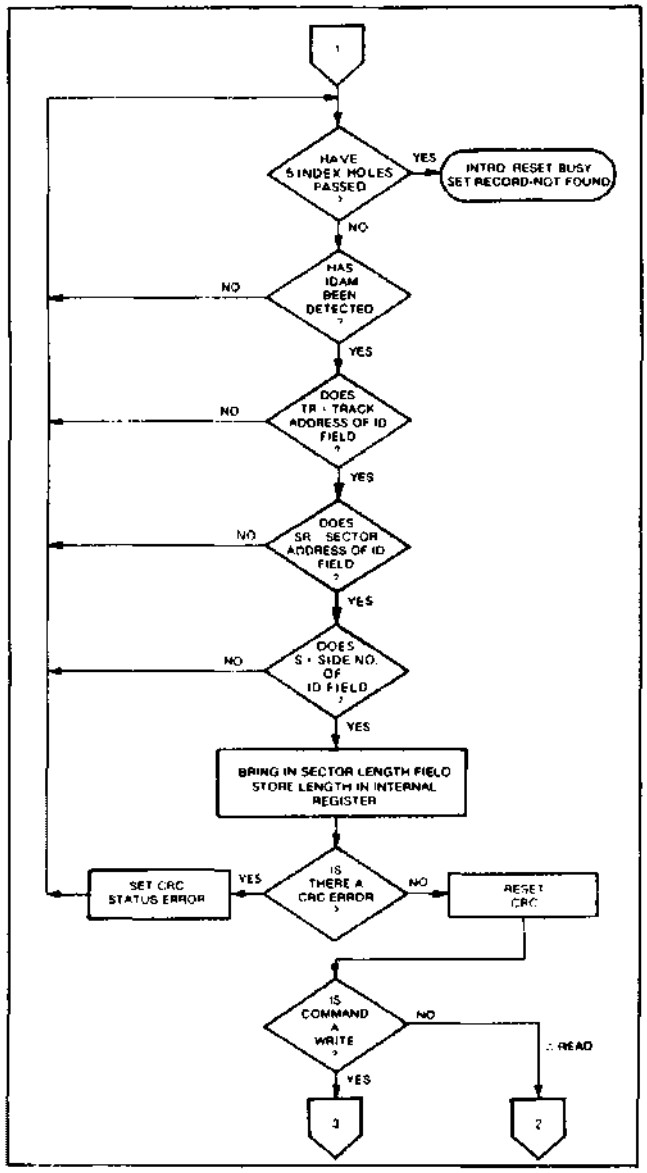
countered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD179X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

Sector Length Table	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD179X will continue to read or write multiple records and update the sector register until the sector regis-



TYPE II COMMAND



TYPE II COMMAND

ter exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

If the Sector Register exceeds the number of sectors on the track, the Record-Not-Found status bit will be set.

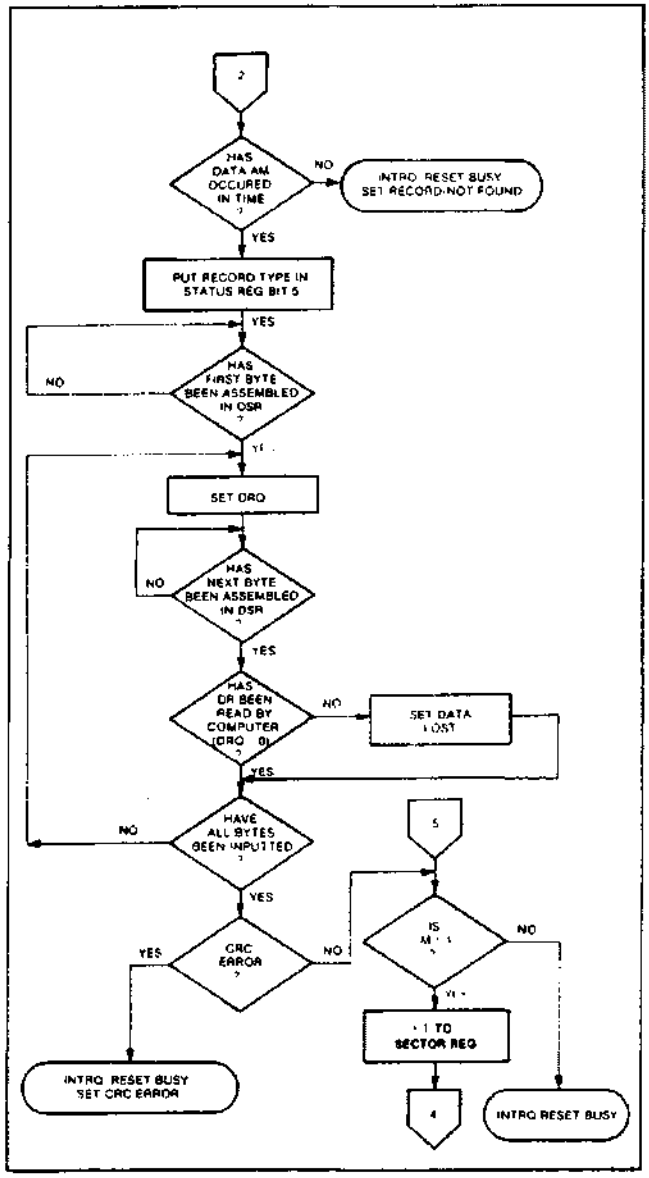
The Type II commands also contain side select compare flags. When C = 0, no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag. If the S flag compares with the side number recorded in the ID field, the 179X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The 1795/7 READ SECTOR and WRITE SECTOR commands include a 'b' flag. The 'b' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatability, the 'b' flag should be set to a one. The 's' flag allows direct control over the SSO Line (Pin 25) and is set or reset at the beginning of the command, dependent upon the value of this flag.

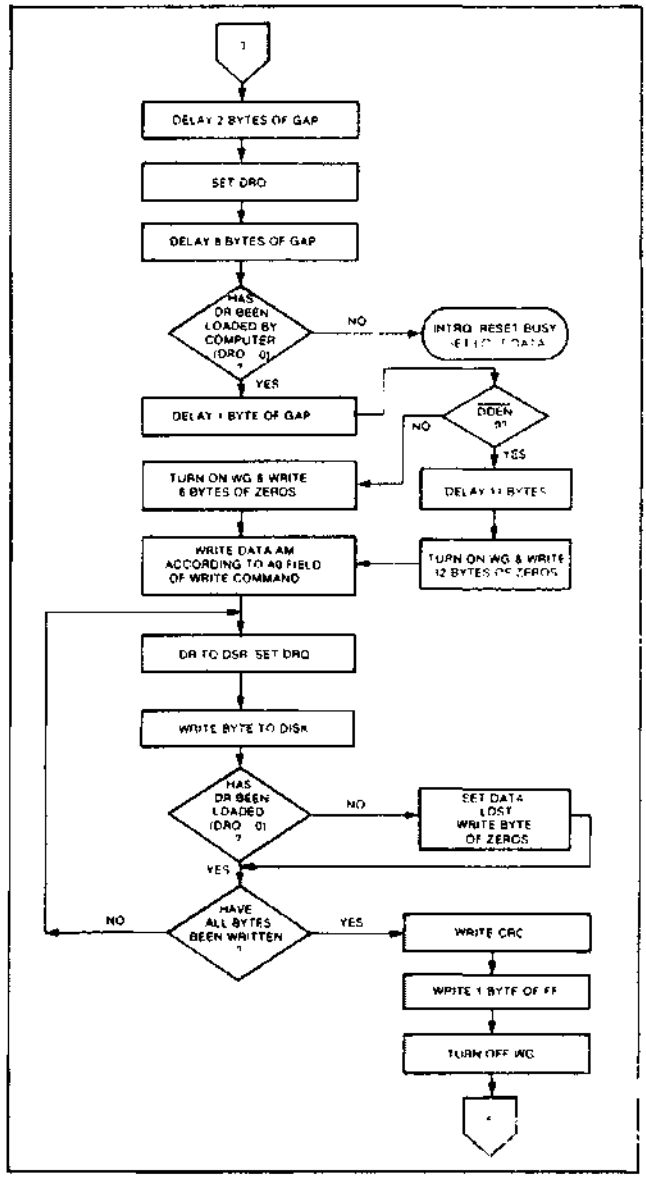
READ SECTOR

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the Record Not Found status bit is set and the operation is terminated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and



TYPE II COMMAND



TYPE II COMMAND

the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown below:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FD179X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The FD179X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated.

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the FD179X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

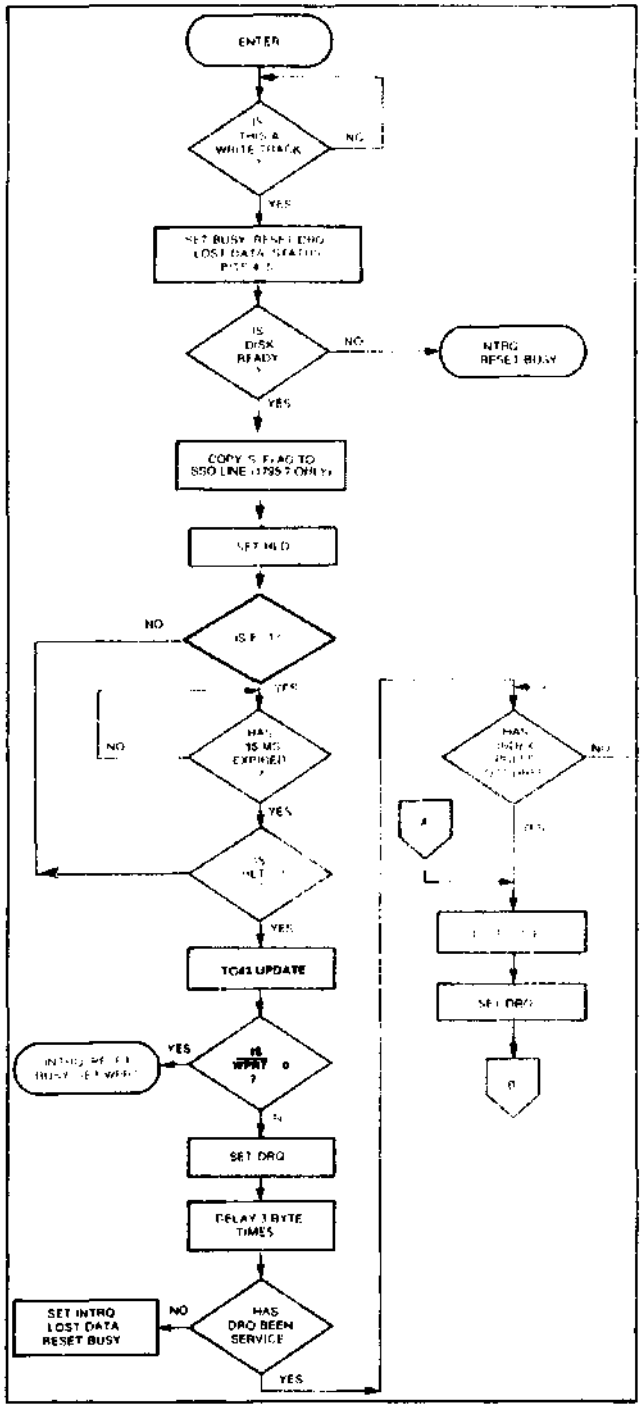
Upon receipt of the Read Track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. The accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated. RG is not activated during the Read Track Command. An internal side compare is not performed during a Read Track.

WRITE TRACK

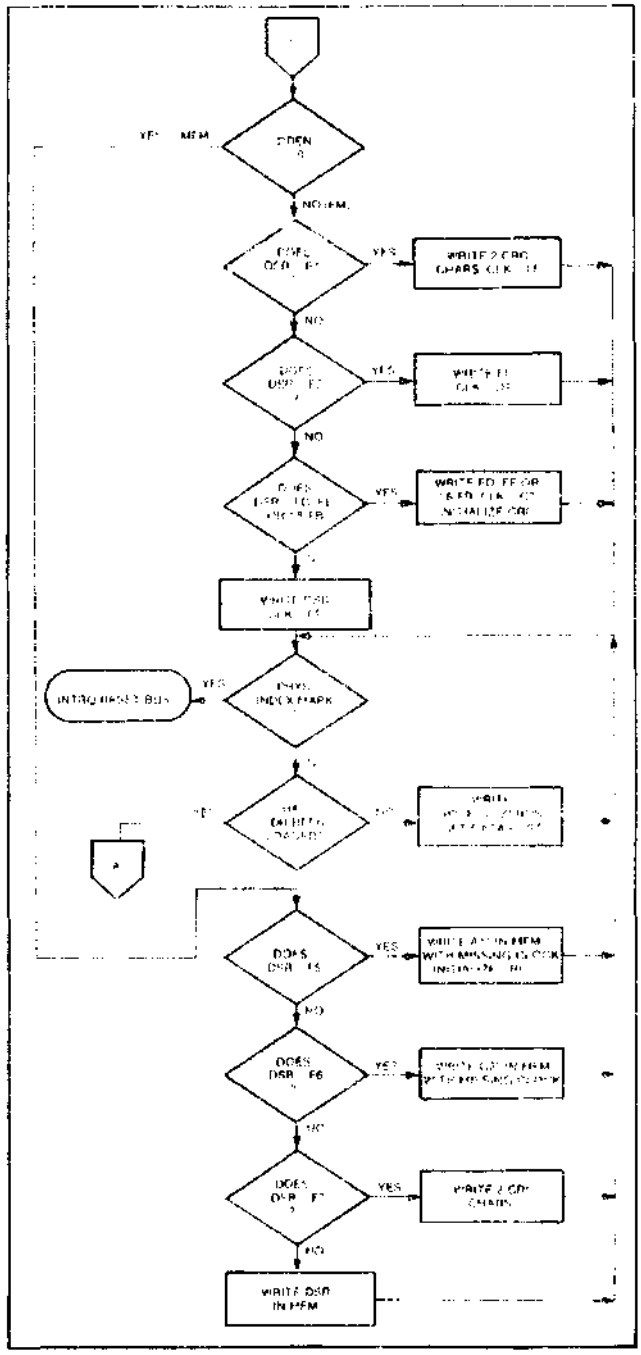
Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM.

GAP III	ID AM	TRACK NUMBER	SIDE NUMBER	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP II	DATA AM	DATA FIELD	CRC 1	CRC 2
ID FIELD										DATA FIELD		

In MFM only, IDAM and DATA AM are preceded by three bytes of A1 with clock transition between bits 4 and 5 missing.



TYPE III COMMAND WRITE TRACK



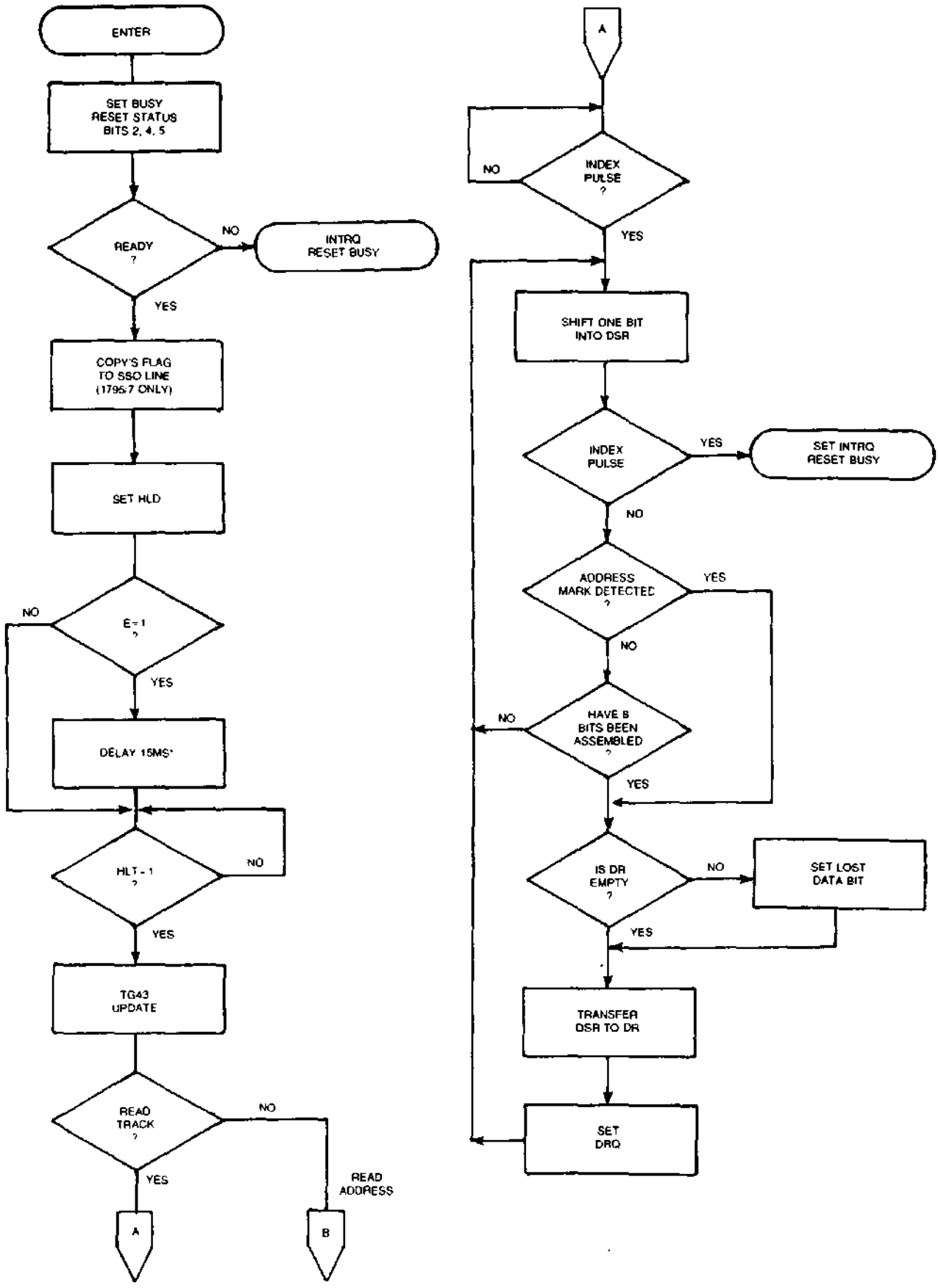
TYPE III COMMAND WRITE TRACK

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	FD179X INTERPRETATION IN FM ($\overline{DDEN}$ = 1)	FD1791/3 INTERPRETATION IN MFM ($\overline{DDEN}$ = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

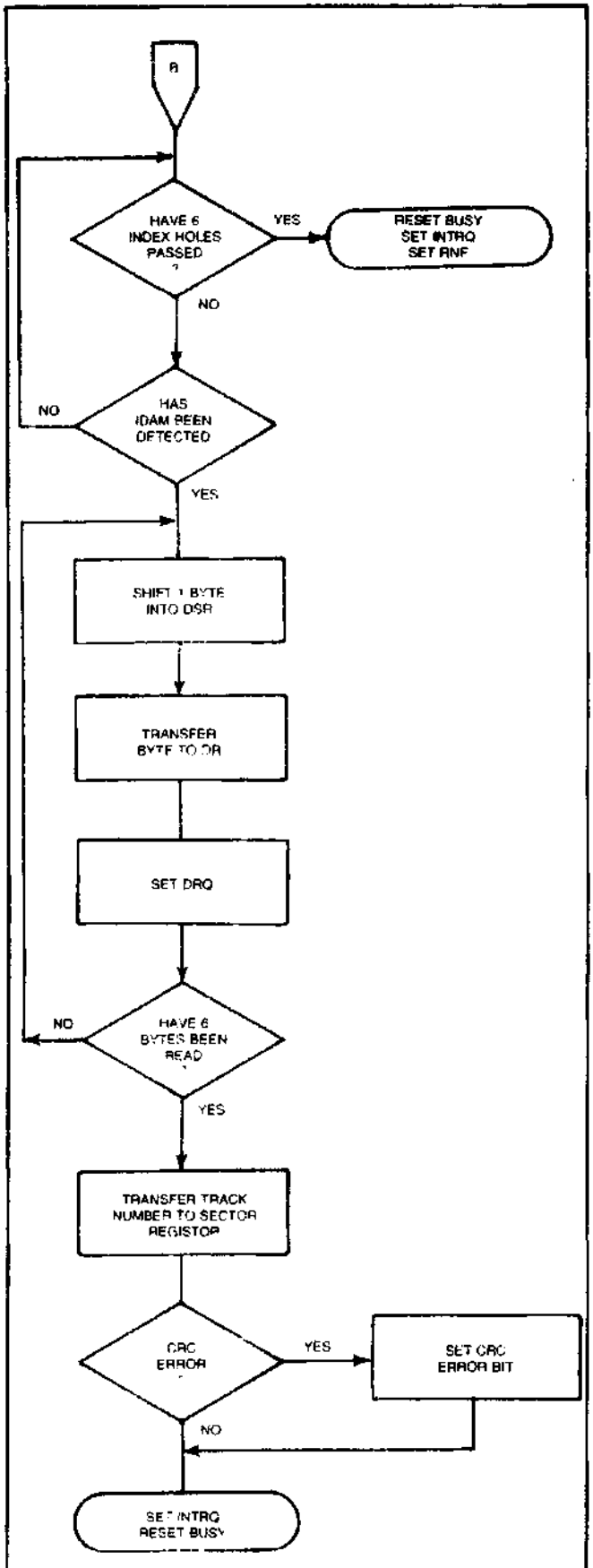
*Missing clock transition between bits 4 and 5

**Missing clock transition between bits 3 & 4



TYPE III COMMAND

Read Track/Address



TYPE III COMMAND

Read Track/Address

TYPE IV COMMAND

FORCE INTERRUPT

This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I_0 through I_3 field is detected. The interrupt conditions are shown below:

I_0 = Not-Ready-To-Ready Transition
I_1 = Ready-To-Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt (requires reset, see Note)

NOTE: If $I_0 - I_3 = 0$, there is no interrupt generated but the current command is terminated and busy is reset. *This is the only command that will enable the immediate interrupt to clear on a subsequent Load Command Register or Read Status Register.*

STATUS DESCRIPTION

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below.

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 6.

FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the FD179X raises the Data Request signal. At this point in time, the user loads the data register with desired data to be written on the disk. For every byte of information to be written on the disk, a data request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the FD179X detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation. For instance, in FM an FE pattern will be interpreted as an ID address mark (DATA-FE, CLK-C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

IBM 3740 FORMAT—128 BYTES/SECTOR

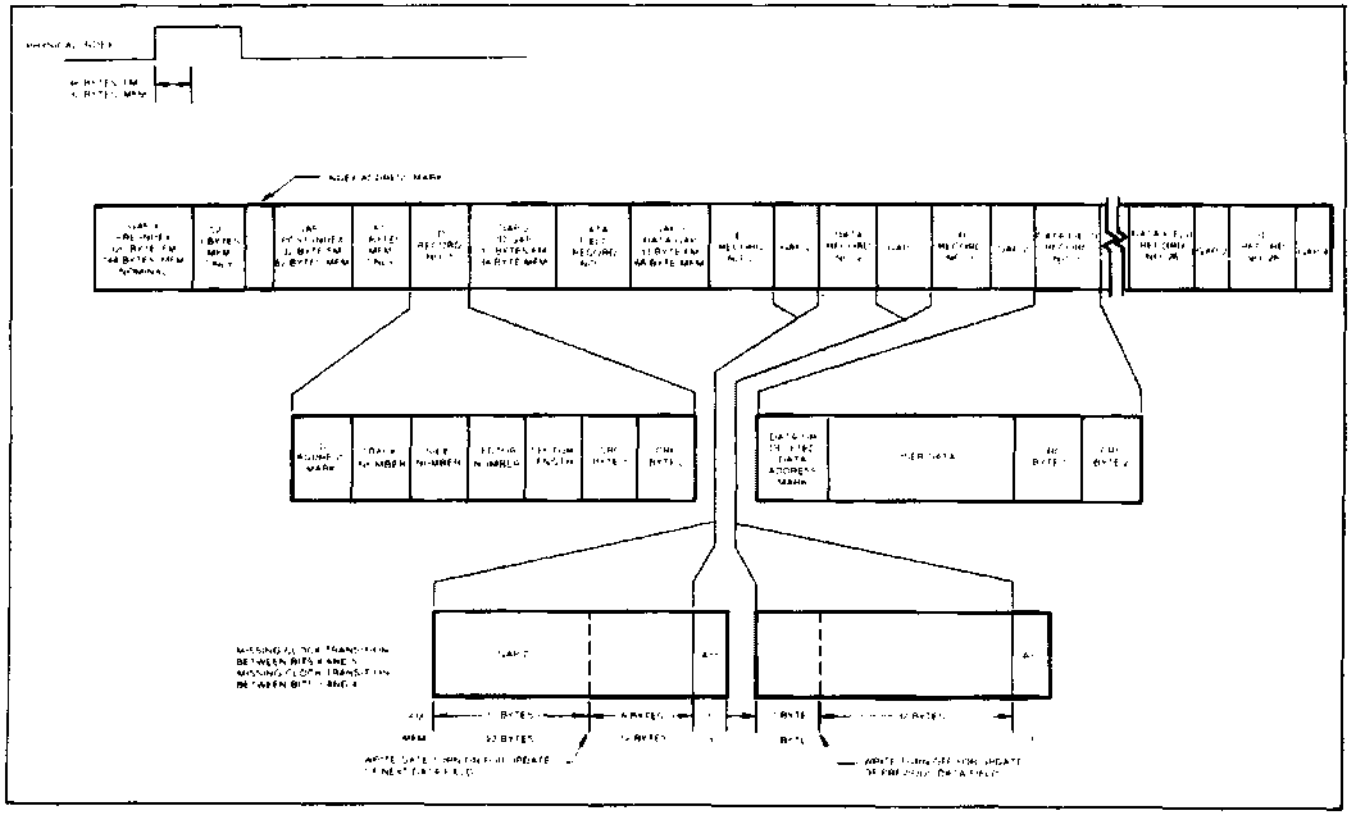
Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00)[1]
6	00
1	FC (Index Mark)
26	FF (or 00)
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00
1	F7 (2 CRC's written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	FF (or 00)
247**	FF (or 00)

*Write bracketed field 26 times

**Continue writing until FD179X interrupts out. Approx. 247 bytes.

1-Optional '00' on 1795/7 only.



IBM TRACK FORMAT

IBM SYSTEM 34 FORMAT- 256 BYTES/SECTOR

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
80	4E
12	00
3	F6
1	FC (Index Mark)
50*	4E
12	00
3	F5
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01
1	F7 (2 CRCs written)
22	4E
12	00
3	F5
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRCs written)
54	4E
598**	4E

*Write bracketed field 26 times
**Continue writing until FD179X interrupts out. Approx. 598 bytes

1. NON-IBM FORMATS

Variations in the IBM format are possible to a limited extent if the following requirements are met: sector size must be a choice of 128, 256, 512, or 1024 bytes; gap size must be according to the following table. Note that the Index Mark is not required by the 179X. The minimum gap sizes shown are that which is required by the 179X, with PLL lock-up time, motor speed variation, etc., adding additional bytes.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00 3 bytes A1
Gap III	10 bytes FF	24 bytes 4E 3 bytes A1
**	4 bytes 00	8 bytes 00
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.
**Byte counts are minimum, except exactly 3 bytes of A1 must be written.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

V_{DD} With Respect to V_{SS} (Ground) =15 to -0.3V

Max Voltage to Any Input With Respect to V_{SS} =15 to −0.3V

Operating Temperature 0°C to 70°C

Storage Temperature −55°C to +125°C

V_{DD} = ID ma Nominal V_{CC} = 35 ma Nominal

OPERATING CHARACTERISTICS (DC)

TA = 0°C to 70°C, V_{DD} = + 12V ± .6V, V_{SS} = OV, V_{CC} = + 5V ± .25V

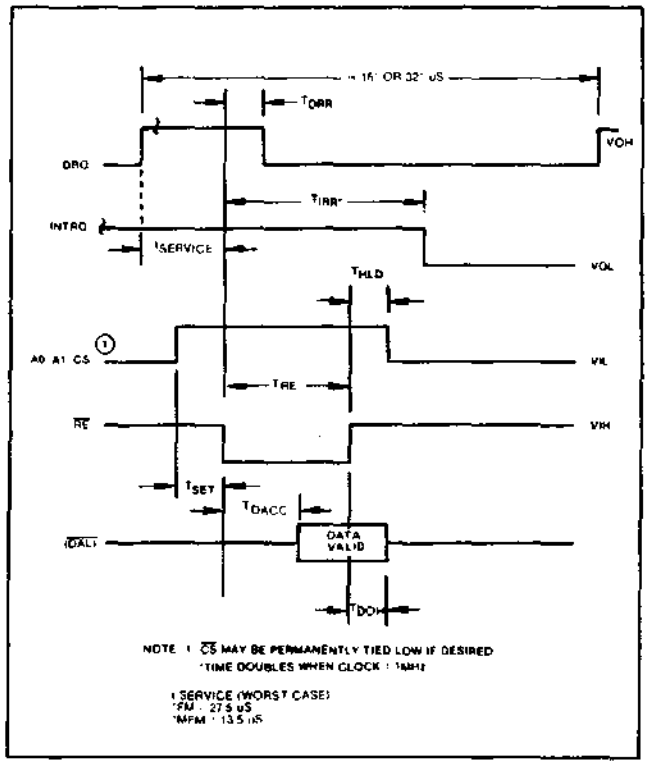
SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	CONDITIONS
I_{IL}	Input Leakage		10	μA	$V_{IN} = V_{DD}$
I_{OL}	Output Leakage		10	μA	$V_{OUT} = V_{DD}$
V_{IH}	Input High Voltage	2.6		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.8		V	I_O = −100 μA
V_{OL}	Output Low Voltage		0.45	V	I_O = 1.6 mA
P_D	Power Dissipation		0.5	W	

TIMING CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = + 12V ± .6V, V_{SS} = 0V, V_{CC} = +5V ± .25V

READ ENABLE TIMING

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{RE}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	400			nsec	C_L = 50 pf
TDRR	DRQ Reset from $\overline{RE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{RE}$		500	3000	nsec	See Note 5
TDACC	Data Access from $\overline{RE}$			350	nsec	C_L = 50 pf
TDOH	Data Hold From $\overline{RE}$	50		150	nsec	C_L = 50 pf



NOTE 1: $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED
*TIME DOUBLES WHEN CLOCK = 1MHz

†SERVICE (WORST CASE)
*FM = 27.5 uS
*MFM = 13.5 uS

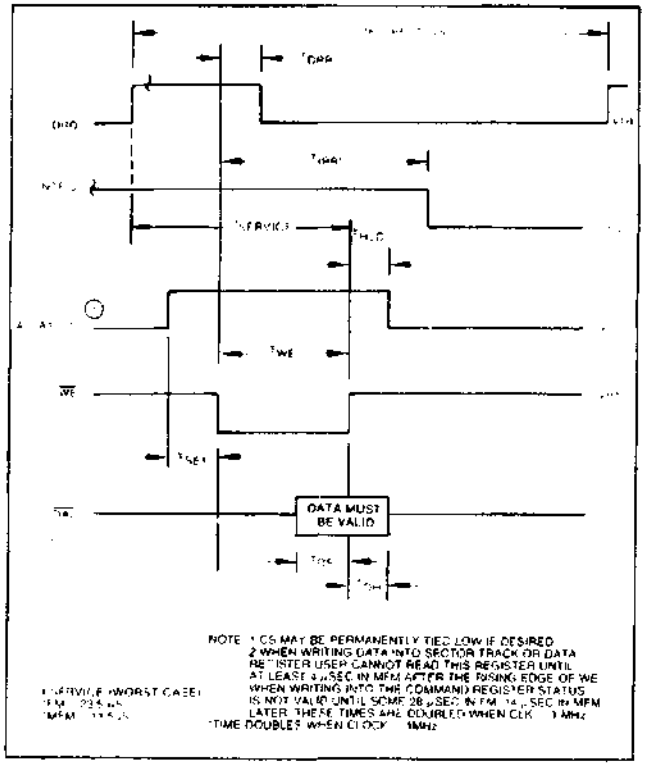
READ ENABLE TIMING

WRITE ENABLE TIMING

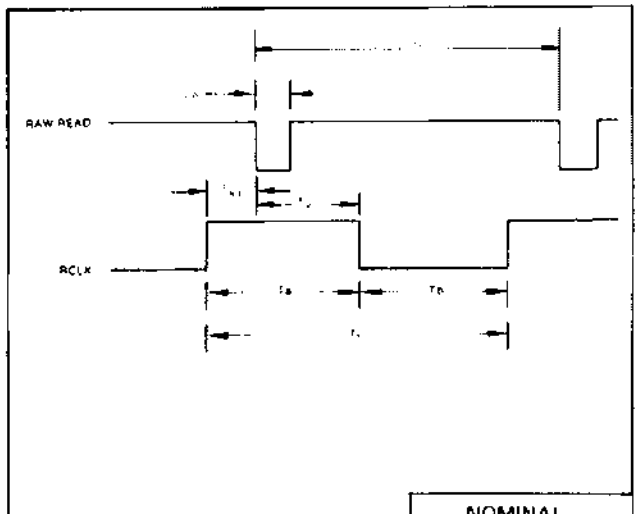
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{WE}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{WE}$		500	3000	nsec	See Note 5
TDS	Data Setup to $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	70			nsec	

INPUT DATA TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Tpw	$\overline{\text{Raw Read}}$ Pulse Width	100	200		nsec	See Note 1
tbc	$\overline{\text{Raw Read}}$ Cycle Time		1500		nsec	1800 ns @ 70°C
Tc	RCLK Cycle Time		1500		nsec	1800 ns @ 70°C
T_{x1}	RCLK hold to $\overline{\text{Raw Read}}$	40			nsec	See Note 1
T_{x2}	$\overline{\text{Raw Read}}$ hold to RCLK	40			nsec	



WRITE ENABLE TIMING

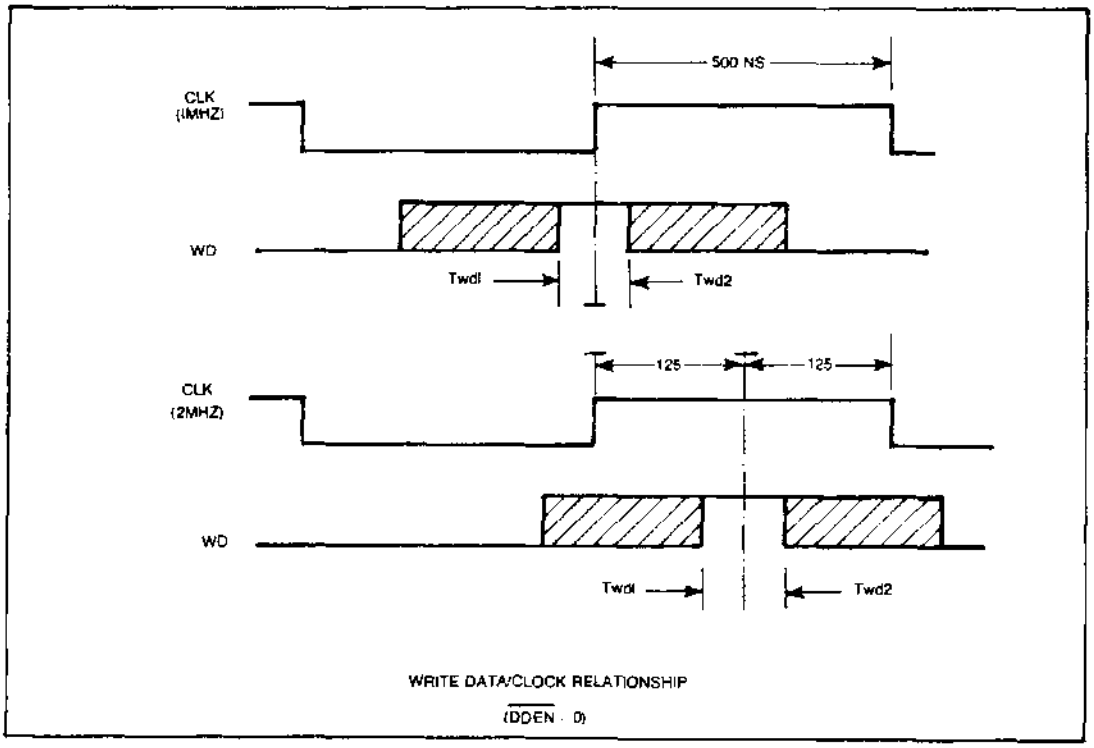


				NOMINAL		
DISKETTE	MODE	$\overline{DDEN}$	CLK	T_x	T_h	T_c
8"	MFM	0	2 MHz	1 μs	1 μs	2 μs
8"	FM	1	2 MHz	2 μs	2μs	4 μs
5"	MFM	0	1 MHz	2 μs	2μs	4 μs
5"	FM	1	1 MHz	4 μs	4 μs	8 μs

INPUT DATA TIMING

WRITE DATA TIMING: (ALL TIMES DOUBLE WHEN CLK = 1 MHz)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Twp	Write Data Pulse Width	450	500	550	nsec	FM
		150	200	250	nsec	MFM
Twg	Write Gate to Write Data		2		μsec	FM
			1		μsec	MFM
Tbc	Write data cycle Time		2,3, or 4		μsec	±CLK Error
Ts	Early (Late) to Write Data	125			nsec	MFM
Th	Early (Late) From Write Data	125			nsec	MFM
Twf	Write Gate off from WD		2		μsec	FM
			1		μsec	MFM
Twdl	WD Valid to Clk	100			nsec	CLK=1 MHZ
		50			nsec	CLK=2 MHZ
Twd2	WD Valid after CLK	100			nsec	CLK=1 MHZ
		30			nsec	CLK=2 MHZ



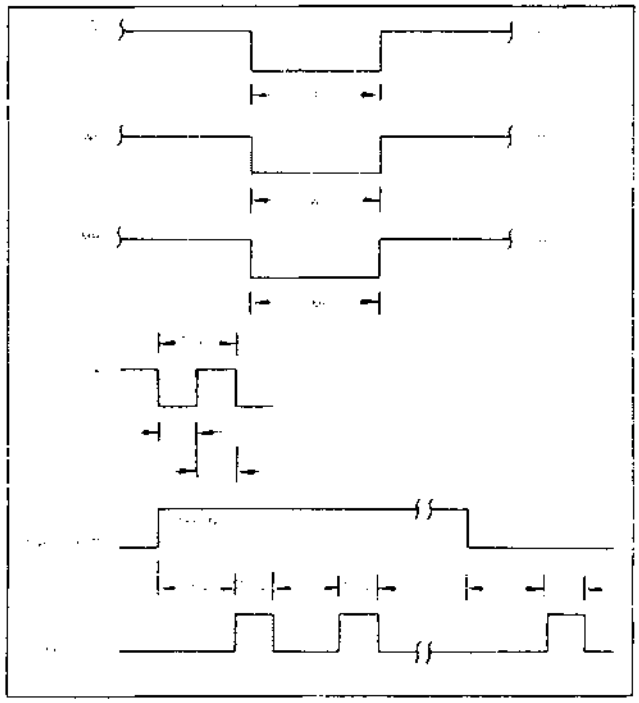
WRITE DATA/CLOCK RELATIONSHIP

($\overline{DDEN}$ = 0)

WRITE DATA TIMING

MISCELLANEOUS TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TCD_1	Clock Duty (low)	230	250	20000	nsec	
TCD_2	Clock Duty (high)	200	250	20000	nsec	
TSTP	Step Pulse Output	2 or 4			μsec	See Note 5
TDIR	Dir Setup to Step		12		μsec	± CLK ERROR
TMR	Master Reset Pulse Width	50			μsec	
TIP	Index Pulse Width	10			μsec	See Note 5
TWF	Write Fault Pulse Width	10			μsec	



MISCELLANEOUS TIMING

NOTES:

1. Pulse width on RAW READ (Pin 27) is normally 100-300 ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300 ns for MFM at CLK = 2 MHz and 600 ns for FM at 2 MHz. Times double for 1 MHz.
2. A PPL Data Separator is recommended for 8" MFM.
3. tbc should be 2 μs, nominal in MFM and 4 μs nominal in FM. Times double when CLK = 1 MHz
4. RCLK may be high or low during $\overline{\text{RAW READ}}$ (Polarity is unimportant).
5. Times double when clock = 1 MHz

Table 6. STATUS REGISTER SUMMARY

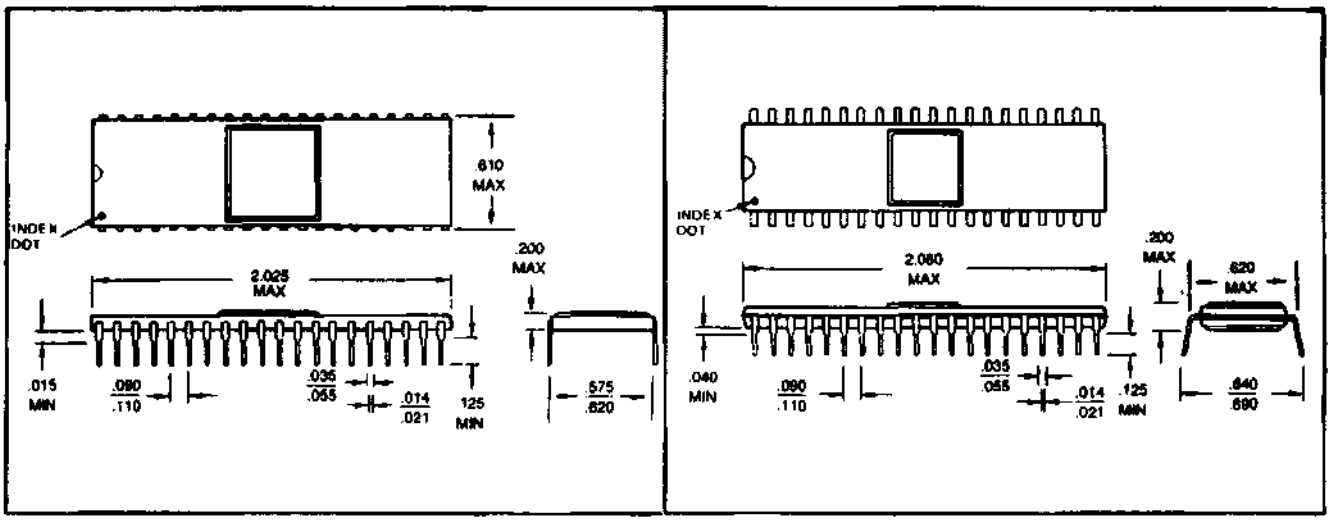
BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{WRPT}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{TROO}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{IP}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.



FD179XA-02 CERAMIC PACKAGE

FD179XB-02 PLASTIC PACKAGE

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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WESTERN DIGITAL
C O R P O R A T I O N

WD1691 FLOPPY SUPPORT LOGIC (F.S.L.)

JUNE, 1980

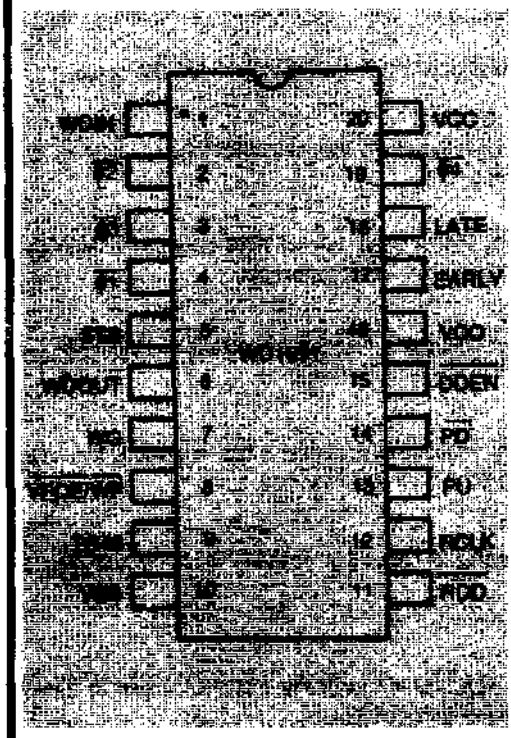
FEATURES

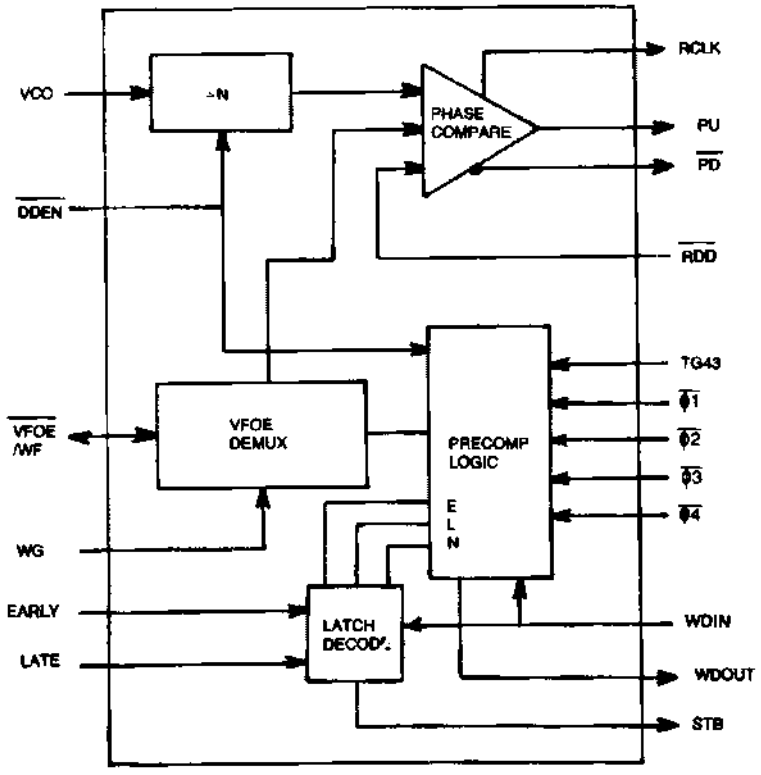
- Direct interface to the FD179X
- Eliminates external FDC Logic
- Data Separation/RCLK GENERATION
- Write Precompensation Signals
- $\overline{\text{VFOE}}/\overline{\text{WF}}$ Demultiplexing
- Programmable Density
- 8" or 5.25" Drive Compatible
- All inputs and outputs TTL Compatible
- Single +5V Supply

GENERAL DESCRIPTION

The WD1691 F.S.L. has been designed to minimize the external logic required to interface the 179X Family of Floppy Disk Controllers to a drive. With the use of an external VCO, the WD 1691 will generate the RCLK signal for the WD179X, while providing an adjustment pulse (PUMP) to control the VCO frequency. $\overline{\text{VFOE}}/\overline{\text{WF}}$ de-multiplexing is also accomplished and Write Precompensation signals have been included to interface directly with the WD2143 Clock Generator.

The WD1691 is implemented in N-MOS silicon gate technology and is available in a plastic or ceramic 20 pin dual-in-line package.





BLOCK DIAGRAM

PIN	NAME	SYMBOL	FUNCTION
1	WRITE DATA INPUT	WDIN	Ties directly to the FD179X WD pin.
2, 3, 4,19	PHASE 2. 3 1. 4	$\overline{\Phi 2}$ $\overline{\Phi 3}$ $\overline{\Phi 1}$ $\overline{\Phi 4}$	4 Phase inputs to generate a desired Write Precompensation delay. These signals tie directly to the WD2143 Clock Generator.
5	STROBE	STB	Strobe output from the 1691. Strobe will latch at a high level on the leading edge of WDIN and reset to a low level on the leading edge of 04.
6	WRITE DATA OUTPUT	WDOUT	Serial, pre-compensated Write data stream to be sent to the disk drive's WD line.
7	WRITE GATE	WG	Ties directly to the FD179X WG pin
8	VFO ENABLE WRITE FAULT	$\overline{VFOE}/\overline{WF}$	Ties directly to the FD179X $\overline{VFOE}/\overline{WF}$ pin.
9	TRACK 43	TG43	Ties directly to the FD179X TG43 pin, If Write Precompensation is required on TRACKS 44-76
10	V_{ss}	V_{ss}	Ground
11	READ DATA	$\overline{RDD}$	Composite clock and data stream input from the drive.
12	READ CLOCK	RCLK	RCLK signal generated by the WD1691, to be tied to the FD179X RCLK pin.
13	PUMP UP	PU	Tri-state output that will be forced high when the WD1691 requires an increase in VCO frequency.
14	PUMP DOWN	$\overline{PD}$	Tri-state output that will be forced low when the WD1691 required a decrease in VCO frequency
15	Double Density Enable	$\overline{DDEN}$	Double Density Select input. When Inactive (High), the VCO frequency is internally divided by two
16	Voltage Controlled Oscillator	VCO	A nominal 4.0MHz (8" drive) or 2.0MHz (5.25" drive) master clock input.
17, 18	EARLY LATE	EARLY LATE	EARLY and LATE signals from the FD179X, used to determine Write Precompensation.
20	V_{cc}	V_{cc}	+ 5V ± 10% power supply

DEVICE DESCRIPTION

The WD1691 is divided into two sections:

1) Data Recovery Circuit
2) Write precompensation Circuit

The Data Separator or Recovery Circuit has four inputs: DDEN, VCO, RDD, and VFOE/WF; and three outputs: PU, PD and RCLK. The VFOE/WF input is used in conjunction with the Write Gate signal to enable the Data recovery circuit. When Write Gate is high, a write operation is taking place, and the data recovery circuits are disabled, regardless of the state on any other inputs.

When VFOE/WF and WRITE GATE are low, the data recovery circuit is enabled. When the RDD line goes Active Low, the PU or PD signals will become active. If the RDD line has made its transition in the beginning of the RCLK window, PU will go from a HI-Z state to a Logic I, requesting an *increase* in VCO frequency. If the RDD line has made its transition at the end of the RCLK window, PU will remain in a HI-Z state while PD will go to a logic zero, requesting a *decrease* in VCO frequency. When the leading edge of RDD occurs in the center of the RCLK window, both PU and PD will remain tri-stated, indicating that no adjustment of the VCO frequency is needed. The RCLK signal is a divide-by-16 (DDEN=1) or a divide-by-8 (DDEN=0) of the VCO frequency.

WG	VFOE/WF	RDD	PU+PD
1	X	X	HI-Z
0	1	X	HI-Z
0	0	1	HI-Z
0	0	0	Enable

The Write Precompensation circuit has been designed to be used with the WD2143-01 clock generator. When the WD1691 is operated in a "single density only" mode, write precompensation as well as the WD2143-01 is not needed. In this case, $\overline{\phi 1}$, $\overline{\phi 2}$, $\overline{\phi 3}$, $\overline{\phi 4}$, and STB should be tied together, DDEN left open, and TG43 tied to ground.

In the double-density mode (DDEN=0), the signals Early and Late are used to select a phase input ($\overline{\phi 1}$ – $\overline{\phi 4}$) on the leading edge of WDIN. The STB line is latched high when this occurs, causing the WD2143-01 to start its pulse generation. $\overline{\phi 2}$ is used as the write data pulse on nominal (Early=Late=$\overline{\phi}$), $\overline{\phi 2}$ is used for early, and $\overline{\phi 3}$ is used for late. The leading edge of $\overline{\phi 4}$ resets the STB line in anticipation of the next write data pulse. When TG43=0 or DDEN=1, Precompensation is disabled and any transitions on the WDIN line will appear on the WDout line. If write precompensation is desired on all tracks, leave TG43 open (an internal pull-up will force a Logic I) while DDEN=0.

The signals, DDEN, TG43, and RDD have internal pull-up resistors and may be left open if a logic I is desired on any of these lines.

The minimum Voh level on PU is specified at 2.4V, sourcing 200ua. During PUMP UP time, this output will "drift" from a tri-state to .4V minimum. By tying PU and PD together, a PUMP signal is created that will be forced low for a decrease in VCO frequency and forced high for an increase in VCO frequency. To speed up rise times and stabilize the output voltage, a resistor divider can be used to set the tri-state level to approximately 1.4V. This yields a worst case swing of ± 1V; acceptable for most VCO chips with a linear voltage-to-frequency characteristic.

Both PU and PD signals are affected by the width of the RAW READ (RDD) pulse. The wider the RAW READ pulse, the longer the PU or PD signal (depending upon the phase relationship to RCLK) will remain active. If the RAW READ pulse exceeds 250ns, (VCO = 4MHz, DDEN = 0) or 500ns. (VCO = 4MHz, DDEN = 1), then both a PU and PD will occur in the same window. This is undesirable and reduces the accuracy of the external integrator or low-pass filter to convert the PUMP signals into a slow moving D.C. correction voltage.

Eventually, the PUMP signals will have corrected the VCO input to exactly the same frequency multiple as the RAW READ signal. The leading edge of the RAW READ pulse will then occur in the exact center of the RCLK window, and ideal condition for the FD179X internal recovery circuits.

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias ..... −25° to 70°C
Voltage on any pin with respect to Ground (vss) ..... −0.2 to +7V
Power Dissipation 1W

Storage Temp.—Ceramic—65°C to +150°C
Plastic—55°C to +125°C

NOTE: Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

DC ELECTRICAL CHARACTERISTICS

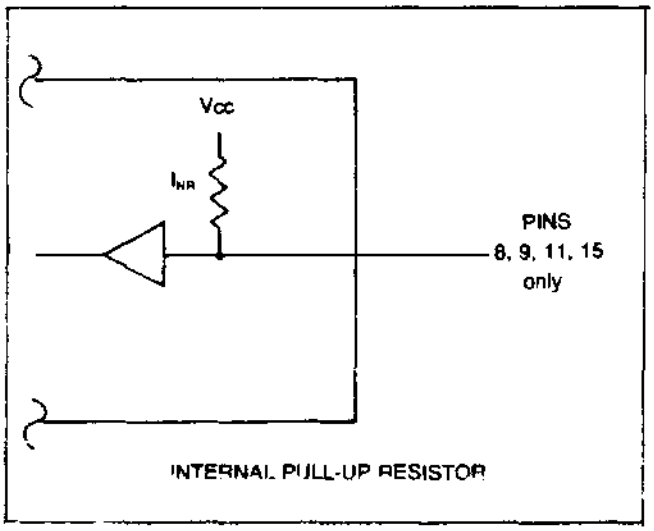
T_A = 0° to 70°C; V_{CC} = 5.0V±10%; V_{ss}=OV

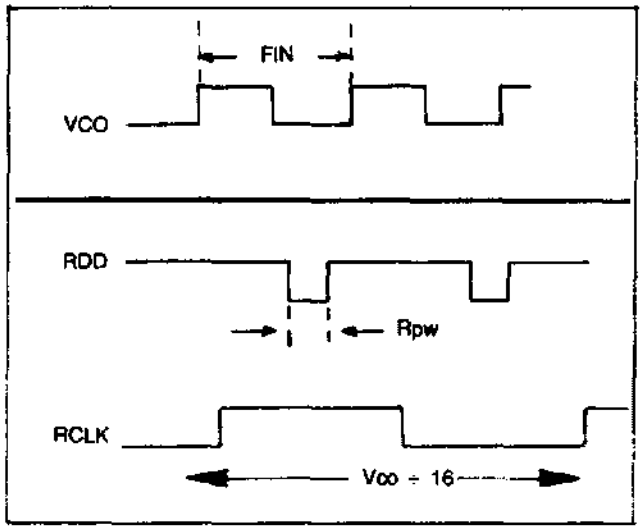
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.2		+0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL}=3.2MA
V_{OH}	High Level Output Voltage	2.4			V	I_{OH}=−200μa
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current		40	100	MA	All outputs open

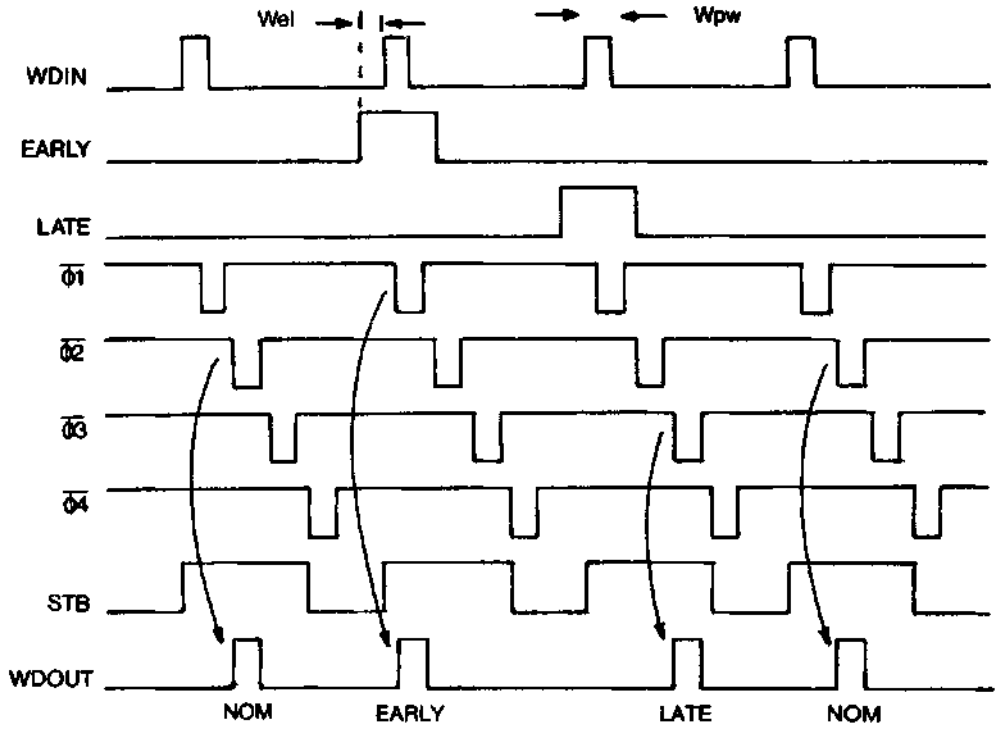
AC ELECTRICAL CHARACTERISTCS

T_A = 0° to 70°C, V_{cc} = 5V± 10%; Vss = OV

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
FIN	VCO Input Frequency	.5	4	6	MHz	$\overline{DDEN}$=0
		.5	2	6	MHz	$\overline{DDEN}$=1
R_{pw}	$\overline{RDD}$ Pulse Width	100	200		ns.	
W_{ei}	EARLY (LATE) to WDIN	100			ns.	
P_{on}	PUMP UP/DN Time	0		250	ns.	
W_{oi}	WDIN to WDOUT			80	ns.	$\overline{DDEN}$=1
I_{NR}	Internal Pull-up Resistor	4.0	6.5	10	KΩ	

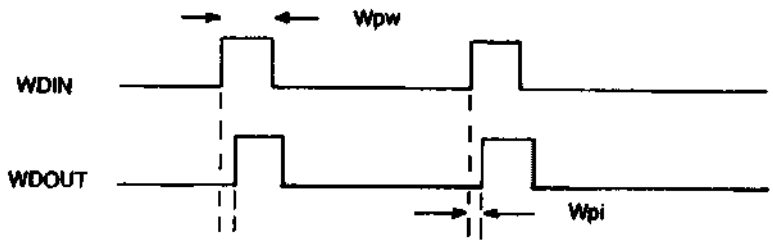






TG43 = "1"
DDEN = "0"

WRITE DATA TIMING (MFM)



TG43 = "0"
DDEN = "1"

WRITE DATA TIMING (FM)

TYPICAL APPLICATIONS

Figure 1 illustrates the 1691 to FD1771-01 floppy disk controller. The RCLK signal is used to gate the RAW data pulses which are inverted by the 74LS04 inverter. Since RCLK will be high during data and low during clock a 74LS08 is used to switch the proper clock or data pulse to the FD1771.

Shown in Figure 2 is a Phase-Lock Loop data separator and the support logic for a single and double-density 8" drive. The raw data (Both clock and data bits) are fed to the WD1691 and FD179X. The WD1691 outputs its PU or PD signal, which is integrated by the .33uf capacitor and 33ohm resistor to form a control voltage for the 74S124 VCO device. The 4.0MHZ nominal output of the VCO then feeds back to the WD1691 completing the loop. The WD2143-01 is also used, providing write precompensation when in double-density, from tracks 44-77. The $\overline{\text{DDEN}}$ line can either be controlled by a toggle switch or a logic level from the host system.

To adjust write precompensation, issue a command to the FD179X so that write data pulses are present. This can be done with a 'WRITE TRACK' command and the $\overline{\text{IP}}$ line open, or a continuous 'WRITE SECTOR' operation. With a scope on pin 4 of the WD1691, adjust the precomp pot for the desired value. This will range from 100 to 300 ns typically. The pulse width set on pin 4 (Ø1) will be the desired precomp delay from nominal.

The data separator must be adjusted with the $\overline{\text{RDD}}$ or $\overline{\text{VFOE/WF}}$ line at a Logic I. Adjust the bias voltage potentiometer for 1.4V on pin 2 of the 74S124. Then adjust the range control to yield 4.0MHZ on pin 7 of the 74S124.

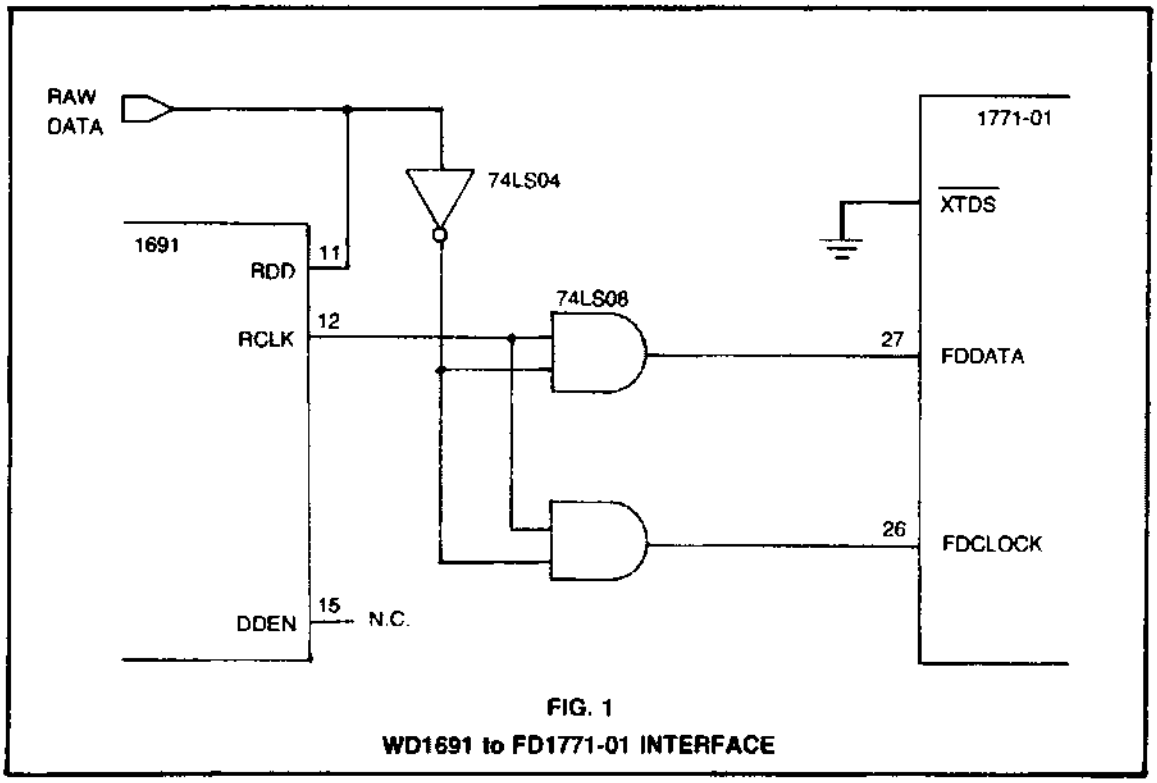


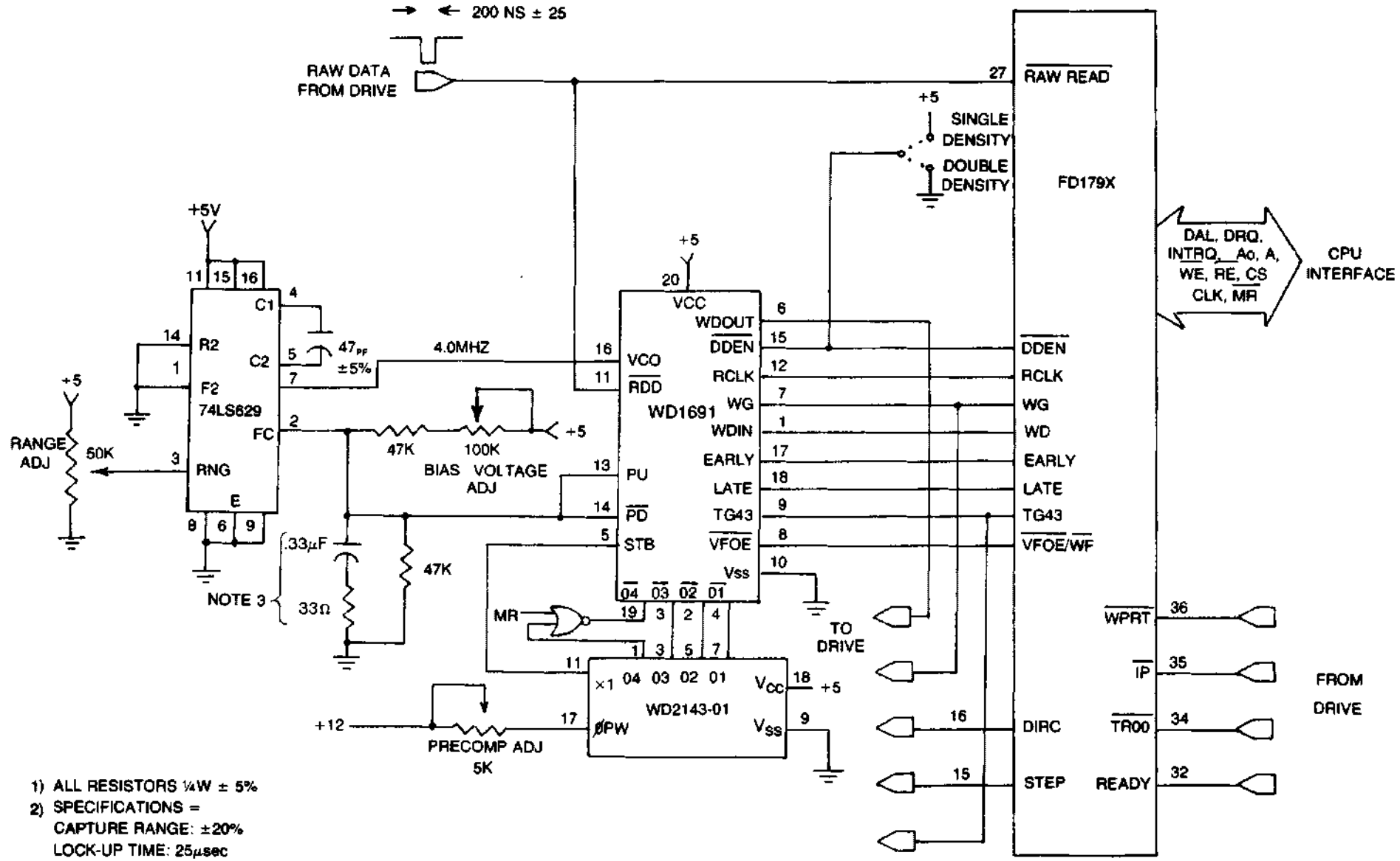
FIG. 1
WD1691 to FD1771-01 INTERFACE

SUBSTITUTING VCO's

There are other VCO circuits available that may be substituted for the 74S124. The specifications required are:

1) The VCO must free run at 4.0MHz with a 1.4V control signal. The WD1691 will force this voltage 1 Volt in either direction (i.e., .4V = decrease frequency, 2.4V = increase frequency). If a ± 15% capture range is desired, then a 1 Volt change on the VCO input should change the frequency by 15%. Capture range should be limited to about ± 25%, to prevent the VCO from breaking into oscillation and/or losing lock because of noise spikes (causing abnormally quick adjustments of the VCO frequency). Jitter in the VCO output frequency may further be reduced by increasing the integration capacitor/resistor, but this will also decrease the final capture range and lock-up time.
2) The sink output current of the WD1691 is 3.2ma minimum. The source output current is −200ua. Therefore, source current is the limiting factor. Insure that the input circuitry of the VCO does not require source current in excess of −200ua.

Another alternative is to use a voltage follower/level shifter circuit to match the input requirements of the VCO chosen. A more complex filter can be used to convert the PUMP UP/PUMP DOWN pulses to the varying DC voltage signal required by the VCO, achieving an optimum condition between lock-up time and high frequency rejection.

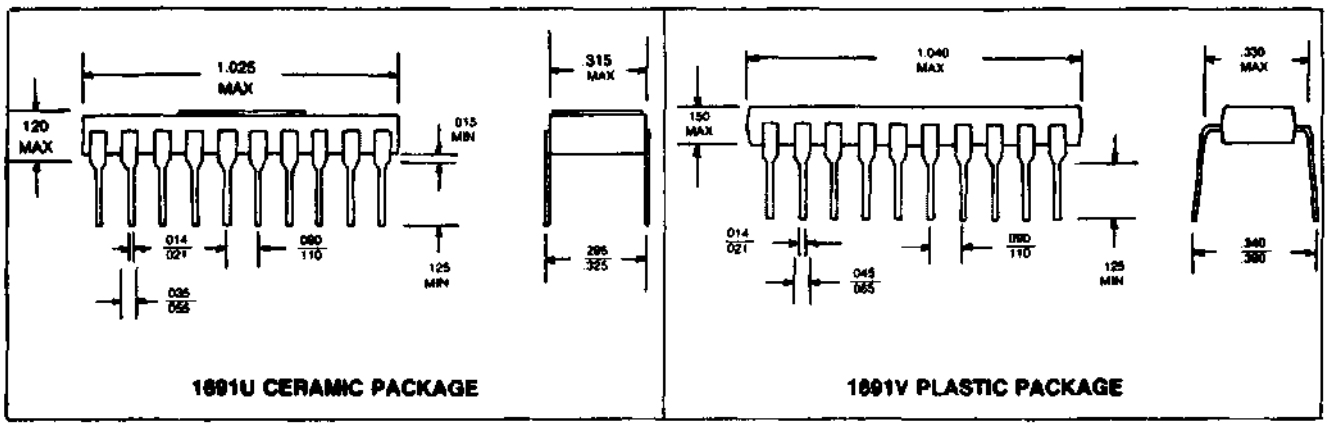


1) ALL RESISTORS ¼W ± 5%
2) SPECIFICATIONS =
   CAPTURE RANGE: ±20%
   LOCK-UP TIME: 25µsec
   (ALL ONE'S PATTERN, MFM)
3) FOR

	5 1/4"	8
	68µf	.33µf
	68Ω	33Ω

FIG. 2

8" SINGLE/DOUBLE DENSITY FLOPPY INTERFACE



This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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WESTERN DIGITAL
CORPORATION

WD2143-01 Four Phase Clock Generator

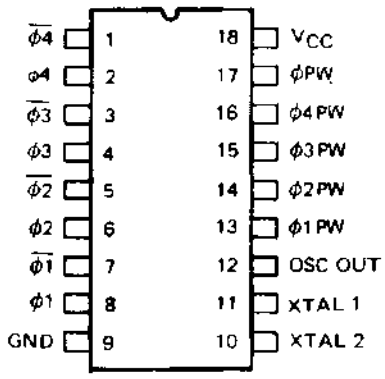
SEPTEMBER, 1980

FEATURES

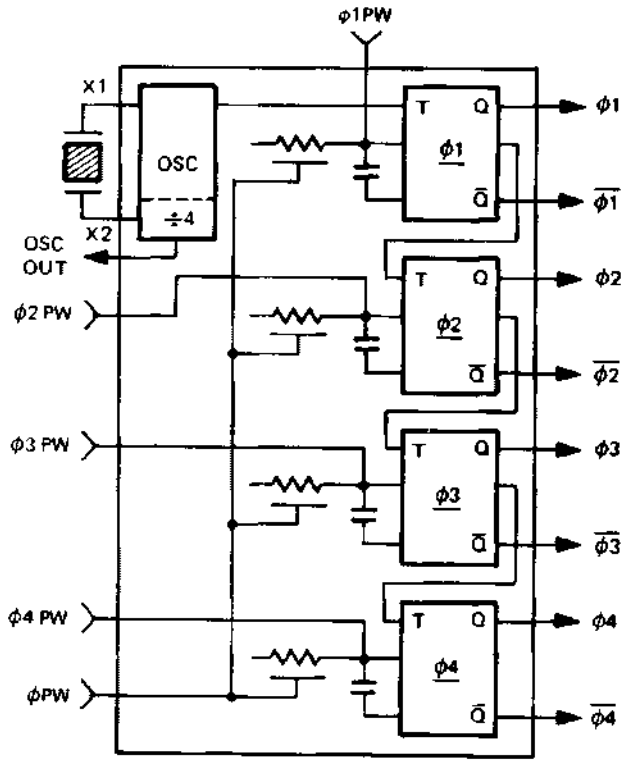
- TRUE AND INVERTED OUTPUTS
- SINGLE 5 VOLT SUPPLY
- TTL COMPATABLE
- ON CHIP OSCILLATOR
- XTAL OR TTL CLOCK INPUTS
- 3 MHz OPERATION
- TTL CLOCK OUTPUT
- PROGRAMMABLE PULSE WIDTHS
- PROGRAMMABLE PHASE WIDTHS
- NO EXTERNAL CAPACITOR
- NON-OVERLAPPING OUTPUTS

GENERAL DESCRIPTION

The WD2143-01 Four-Phase Clock Generator is a MOS/LSI device capable of generating four non-overlapping clocks. The output pulse widths are controlled by tying an external resistor to the proper control inputs. All pulse widths may be set to the same width by tying the ØPW line through an external resistor. Each pulse width can also be individually programmed by tying a resistor through the appropriate Ø1PW — Ø4PW control inputs. In addition, the OSC OUT line provides a TTL square wave output at a divide-by-four of the crystal frequency.



PIN CONNECTIONS



WD2143-01 BLOCK DIAGRAM

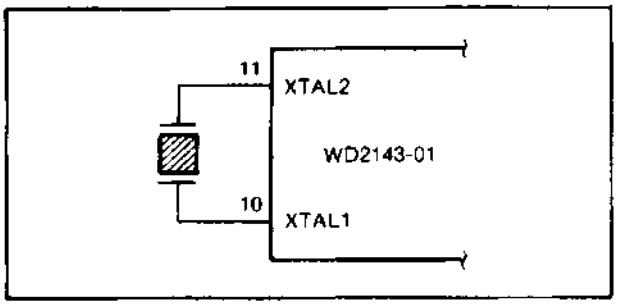
PIN NUMBER	SYMBOL	DESCRIPTION
1, 3, 5, 7	$\overline{\phi 1}$—$\overline{\phi 4}$	Four phase, non-overlapping outputs. These outputs are inverted (active low).
2, 4, 6, 8	Ø1-Ø4	Four Phase, non-overlapping outputs. These outputs are true (active high).
9	GND	Ground
10, 11	XTAL1 XTAL2	External XTAL connections. An external crystal tied to these pins will cause the oscillator to oscillate at the crystal frequency.
12	OSC OUT	A TTL compatable output that is a divide-by-four of the crystal frequency.
13-16	Ø1PW-Ø4PW	External resistor inputs to control the individual pulse widths of each output. These pins can be left open if ØPW is used.
17	ØPW	External resistor input to control all phase outputs to the same pulse widths.
18	V_{CC}	+5V ± 5% power supply input

DEVICE OPERATION

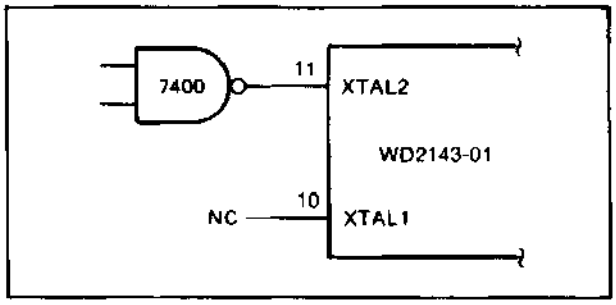
Each of the phase outputs can be controlled individually by typing an external resistor from Ø1PW-Ø4PW to a +5V supply. When it is desired to have Ø1 through Ø4 outputs the same width, the Ø1PW-Ø4PW inputs should be left open and an external resistor tied from the ØPW (Pin 17) input to +12V.

XTAL1 and XTAL2 can be connected directly to a series-resonant crystal, forcing the internal oscillator to oscillate to the crystal frequency. XTAL2 (pin 11) may also be driven by a TTL square wave with XTAL1 (pin 10) left open. Each of the four phase outputs provide both true and inverted signals, capable of driving 1 TTL load each.

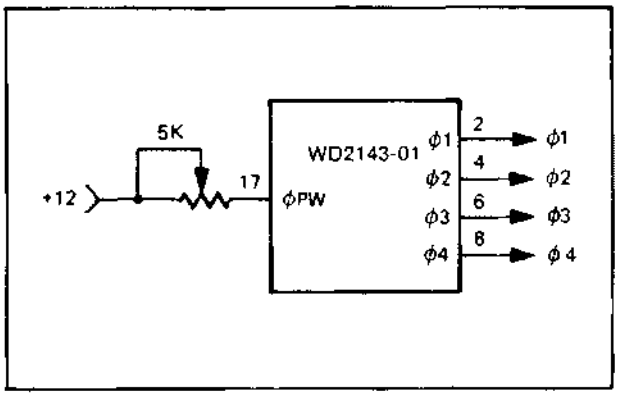
TYPICAL APPLICATIONS



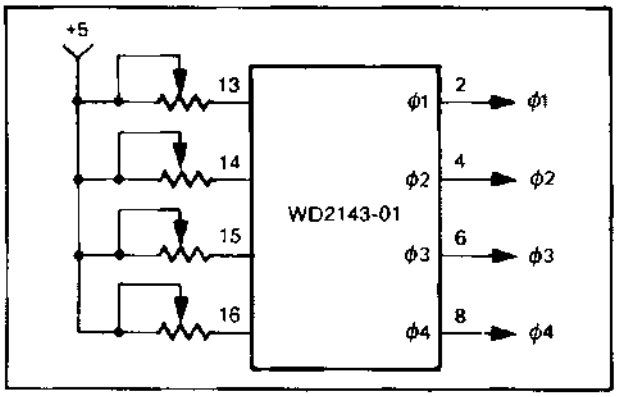
EXTERNAL CRYSTAL OPERATION



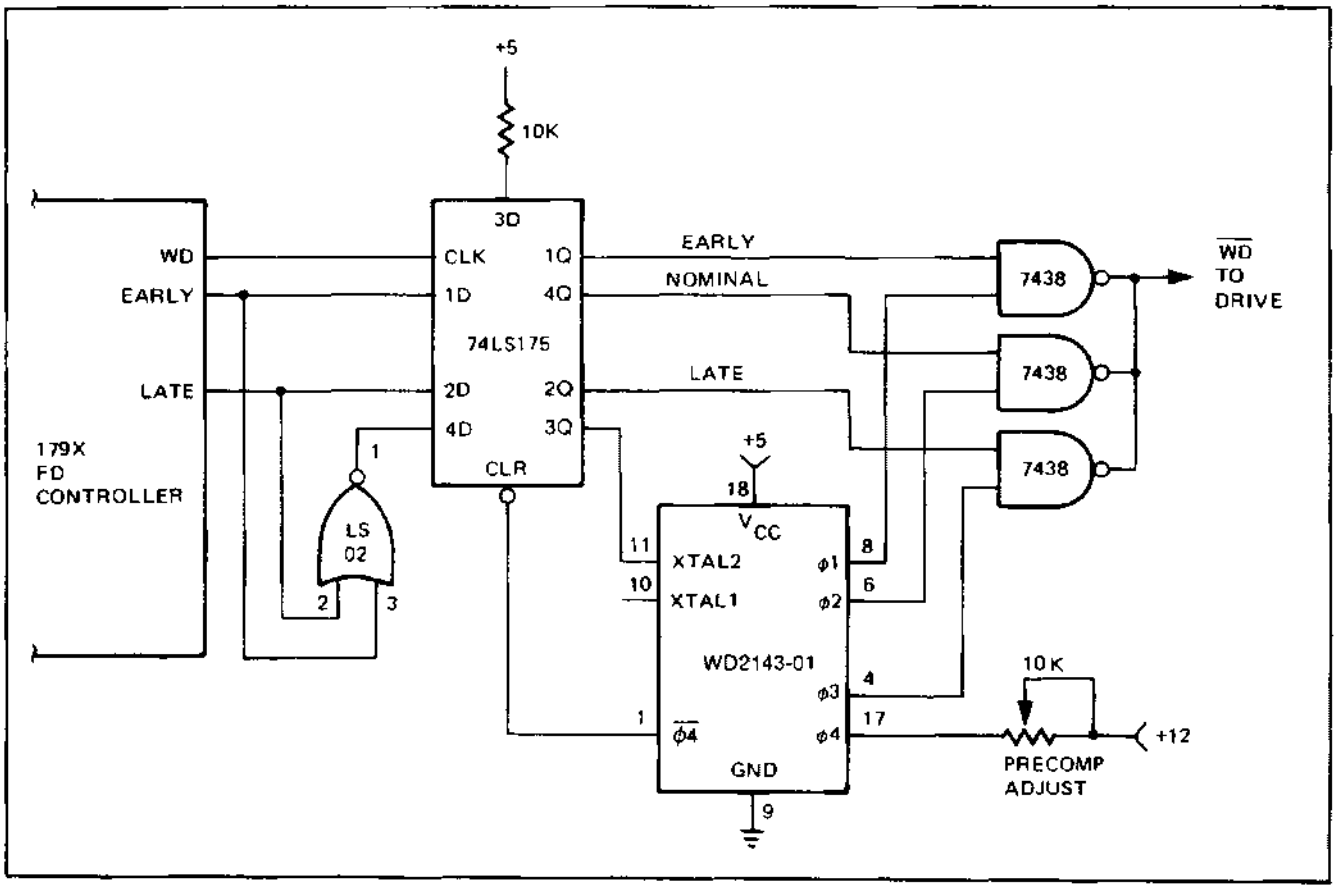
TTL SQUARE WAVE OPERATION



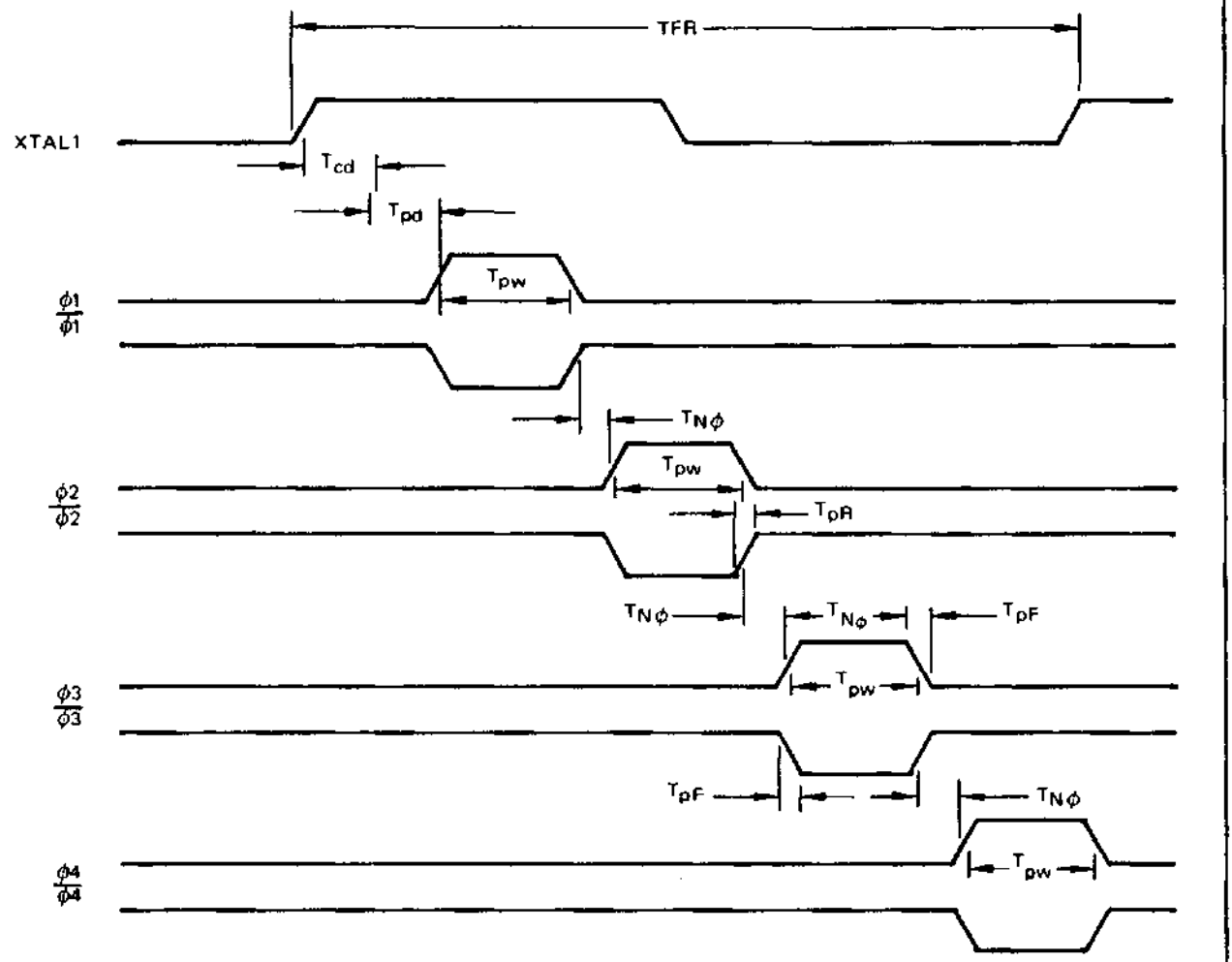
EQUAL PULSE WIDTH OUTPUTS



INDIVIDUAL PULSE WIDTH OUTPUTS



WRITE PRECOMP FOR FLOPPY DISK



NOTES:
T_{cd} MEASURED FROM 90% V_{oH} POINTS
T_{pW} MEASURED FROM 50% V_{oH} POINTS

WD2143-01 TIMING DIAGRAM

SPECIFICATIONS

Absolute Maximum Ratings		Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to the DC electrical characteristics specified.
Operating Temperature	0° to +70° C	
Voltage on any pin with respect to Ground	−0.5 to +7V	
Power Dissapation	1 Watt	
Storage Temperature	−55° to +125° C	

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V + 5% R(ØNPW) or R(ØPW) = 5K, GND = 0V T_A = 0° to 70° C

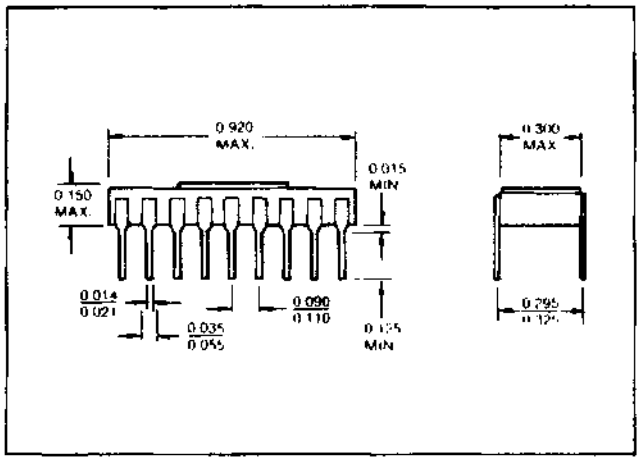
SYMBOL	PARAMETER	MIN.	MAX.	UNITS	CONDITIONS
V_{ol}	TTL low level output		0.4	V	I_{ol} = 1.6 ma.
V_{oh}	TTL high level output	2.4		V	I_{oh} = 100 ua.
V_{il}	XTAL in low voltage		0.8	V	
V_{ih}	XTAL in high voltage	2.4		V	
I_{cc}	Supply Current		80	ma	All outputs open

SWITCHING CHARACTERISTICS

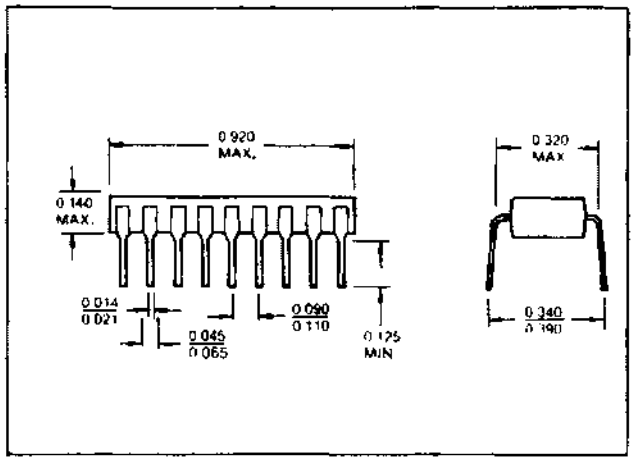
V_{CC} = 5V + 5%, GND = 0V T_A = 0° to 70° C

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	CONDITIONS
T_{cd}	XTAL in to OSC out (↑)		100	NS	
T_{pd}	OSC out to Ø1		100	NS	

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	CONDITIONS
T_{pw}	Pulse Width (any output)	100		NS	CL = 30pf ØPW = 5K
$T_{n\phi}$	Non-Overlap Time	20		NS	
T_{pr}	Rise Time (any output)		30	NS	CL = 30 pf
T_{pf}	Fall Time (any output)		25	NS	CL = 30 pf
TFR	OSC in Frequency External Resistor		3 100	mHz kΩ	 ØPW or ØnPW
T_{pw}	Pulse Width Differential		5	%	ØPW = 5K



WD2143L-01 CERAMIC PACKAGE



WD2143M-01 PLASTIC PACKAGE

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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Printed U.S.A.

The Keyboard/Terminal

Manufactured by Volker-Craig Limited

volker-craig limited

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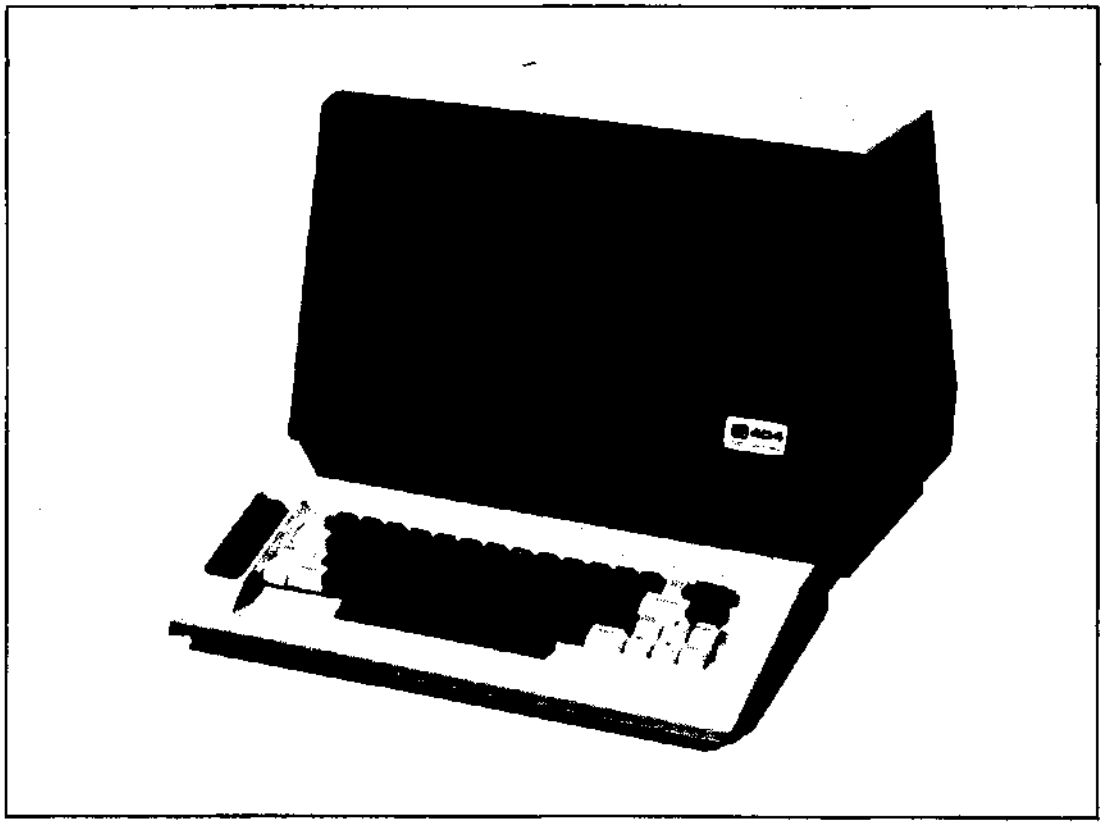
OPERATOR'S MANUAL

VIDEO DISPLAY TERMINAL

VC404



Applies to Terminal Starting S/N 60955-01
Manual P/N: 98-800-0021
Form No. 211 Rev. 3 June 1980

TABLE OF CONTENTS

SECTION 1

INTRODUCTION

1.1 GENERAL

This high-performance, teletype-compatible display terminal is an input-output device which transmits and receives information from a central processor or computer time-share system. This interactive terminal is designed to meet requirements in the telecommunications, data processing, and computer industries. Applications include small systems, time-sharing, information display systems, credit/banking systems, and minicomputer/microcomputer systems.

Data communication is possible using a modem and acoustic coupler or a direct computer-to-terminal connection via the EIA, RS232C (CCITT V.24) compatible interface connector at data rates up to 19200 baud. A 20 milliamp current loop cable interface is an optional accessory.

The basic terminal includes an upper/lower case typewriter style keyboard with control keys, communications electronics, and a 12" non-glare video display screen for a 24 line, 80 character per line format. Data entry occurs in either a bottom line mode with single line scroll up or a page mode. Options to the terminal include serial and parallel peripheral interfaces, coloured display screens, numeric pad and function keys, APL character set (non-overstrike), and many foreign keyboards and character sets.

1.2 DISPLAY TERMINAL FEATURES AND OPTIONS

The basic video display terminal is a stand-alone, ASCII, serial asynchronous computer peripheral for use on any system with an RS232C (CCITT V. 24) interface.

Standard features on the terminal include:

Detachable upper/lower case typewriter style keyboard.

Switch selectable upper/lower case.

Display of 1920 characters in a 24 line, 80 character per line format.

12" anti-glare display screen.

Normal or reverse video.

Four-Way cursor flashing or steady-block or underline selectable.

Front panel controls: Power Off/On, Local/Remote, Half/Full Duplex, Roll/Page, ASCII/APL switches.

Transparent/Tape Mode switch allows display of 95 or 128 characters. All control codes displayed when mode is On.

Bottom line entry in Roll Mode.

Page overwrite in Page Mode.

Automatic word wrap around on video display after the 80th character position.

Automatic alarm (Control G, BEL code).

Auto-Repeat, characters repeat at 15 char/sec.

Absolute x-y cursor addressing.

Clear to 'End of Line' and 'End ofScreen' functons.

8-position baud rate select switch on rear panel. Select from 110, 300, 600, 1200, 2400, 4800, 9600, 19200 baud.

Parity select switch on rear panel.

EIA RS232C (CCITT V.24) communications interface. (20mA. current loop accessory available.)

Serial or parallel peripheral interfaces (optional).

Optional numeric pad and function keys.

APL and many foreign keyboards and displays available.

EXPORT version (230V/50Hz) easily user-configurable.

1.3 TERMINAL OPTIONS

OPTION APL	Provides front panel switch selectable ASCII and APL character set (no overstrikes). APL is typewriter paired.
OPTION SPI	Serial Peripheral Interface. This switched EIA interface is bidirectional for use with a printer, cassette, floppy disc, or other serial peripheral devices. This port is enabled locally by depressing the PRINT key on the keyboard or remotely by the Control Q (Turn On) and Control S (Turn Off) ASCII codes. This option is implemented using a 25 pin DB Type connector located on the rear of the terminal.
OPTION PIP	Auxiliary Parallel Input. ASCII input port used with accessory items such as the Bar Code Reader Interface (BRI). There are 7 input bit lines plus a strobe bit line, power and control lines. This 25-Pin connector is located on the rear panel.
OPTION CDS	Coloured anti-glare display screen (specify Amber, Green).
OPTION KB1	Adds a numeric pad and function keys to the keyboard.

SECTION 2

OPERATION

2.1 OPERATING CONTROLS

The main controls for establishing the terminal's mode of operation, LOCAL, FULL, PAGE, and APL are located on the keyboard. These and other controls are as follows:

CONTROL	LOCATION	FUNCTION
POWER	Front	Controls power to terminal (Part of Brightness control).
LOCAL	Keyboard	When depressed, the terminal is in a LOCAL (Off-Line) mode. When up, the terminal is in REMOTE (On-Line) mode.
FULL	Keyboard	Switch selects HALF (Up) or FULL (Depressed) DUPLEX mode.
PAGE	Keyboard	Switch selects screen presentation mode, Page overwrite (depressed) or bottom line (Up) entry with scroll-up.
APL	Keyboard	When depressed, selects screen display. It is used with the APL character set.
BAUD RATE	Rear	Thumbwheel switch selects one baud rate from 110, 300, 600, 1200, 2400, 4800, 9600, 19200 baud.
BRIGHTNESS	Front	Control knob adjusts brightness of screen display and POWER on/off.
CAPS ONLY	Keyboard	When depressed, the terminal is in CAPS LOCK mode. Shifts lower-case alphabetic characters to upper-case.
PARITY	Rear	Toggle switch selects odd, even or no parity (normally mark; may be internally changed to space parity).
TRANSPARENT	Rear	Switch selects 95 or 128 character set display. All control codes displayed when switch is ON.

Switch Pos.	Baud Rate
0	110
1	300
2	600
3	1200
4	2400
5	4800
6	9600
7	19200

2.2 KEYBOARD FUNCTIONS

All keyboard keys generate ASCII codes with the exception of the BREAK Key. APPENDIX H identifies which codes are used for the individual characters and control functions. For example, Control M executes a carriage return. Characters repeat automatically if the key held depressed for more than .75 seconds. APPENDIX F shows keyboard layouts.

BREAK

The data output lines are put into a space condition for as long as the key is depressed.

CONTROL CHARACTERS

Control characters are transmitted by depressing the CTRL key and the character key simultaneously or by depressing the control key first and holding it down while depressing the character key. These codes are transmitted by the terminal.

CURSOR LEFT (Control H)

Moves the non-destructive cursor one character position to the left. If the cursor is positioned at the beginning of a line, issuing this command will have no effect.

CURSOR RIGHT (Control U)

Moves the non-destructive cursor one position to the right. When the cursor reaches the last character position in a line, it wraps around to the beginning of the next line. In PAGE mode the cursor moves from the last position of the last line to the first position of the first line when a cursor right command is issued.

CURSOR DOWN or LINE FEED, LF (Control J)

This command moves the non-destructive cursor down one line. If the cursor is on the bottom line the text scrolls up. In Page Mode the cursor moves to the top line.

CURSOR UP (Control Z)

Moves the non-destructive cursor up one position. If the cursor is on the top line, cursor remains fixed.

CURSOR HOME (Control Y)

Moves the non-destructive cursor to the upper left hand corner, without clearing screen.

CLEAR (Control X)

When this key is depressed, the entire screen is cleared of all information and the cursor moves to the upper left hand corner (allow 40 ms.).

CLEAR TO END OF LINE (Control V)

When this key is depressed. the line upon which the cursor is currently positioned is cleared from the cursor to the end of that line. the cursor position remains unchanged.

CLEAR TO END OF SCREEN (Control W)

When this key is depressed, all information is cleared from the cursor position to the end of the screen. The cursor position remains unchanged (allow 40 ms.).

RETURN (Control M)

When depressed, the cursor is moved to the beginning of the line on which it is positioned.

CONTROL P (X-Y Cursor Addressing)

Direct cursor positioning is provided following the receipt of the appropriate control code (Control P). The next character received will cause the cursor to move to a line position (Y direction) as defined in the table in APPENDIX A. In a similar manner, the next character will cause the cursor to move to a character position (X direction) as defined in the table. Note that motion can be inhibited in one direction or the other.

ESC (Escape)

When depressed, the ASCII code for the ESCAPE function is transmitted, but not displayed. When received, the code has no effect on terminal operation.

2.3 TURN-ON PROCEDURE

Become familiar with all controls, switches, and indicators on the terminal before attempting to sign on to any computer system. The following procedure should be followed when signing on:

1. Turn the BRIGHTNESS control knob clockwise to turn the power ON.
2. Place LOCAL switch on keyboard to LOCAL.
3. Depress a few character keys to fill the screen with a few lines of characters.
4. Adjust BRIGHTNESS control knob to display bright, crisp characters.
5. Execute a CONTROL X (or depress CLEAR key) to clear screen and home the cursor.
6. Set the PARITY ODD/EVEN/NO toggle switch on rear panel to required position.
7. Select the BAUD RATE to be used with the rear panel thumbwheel switch.
8. Set the LOCAL keyswitch to the Up position and the FULL Duplex (Up for HALF, down for FULL) keyswitch to the required position and begin sign-on procedure.

2.4 MODES OF OPERATION

LOCAL

In the LOCAL MODE, no signal transmission is made to the computer through the input/output connectors on the rear panel. LOCAL MODE may be used for testing keyboard functions or working in an off-line mode.

HALF DUPLEX, REMOTE

In this mode data is simultaneously displayed on the screen and transmitted to the computer each time a key is depressed.

FULL DUPLEX, REMOTE

In this mode, two way communications exists between terminal and computer. When a key is depressed, the data is transmitted to the computer and then displayed on the terminal screen only after the computer has echoed back the character for display verification. The terminal's operator is assured character-by-character verification of the transmitted data.

TRANSPARENT/TAPE

When the TRANSPARENT MODE switch located on the rear chasis is in the ON position all control codes received by the terminal from the computer or keyboard are displayed on the screen. No cursor control codes are active and all data is continuously displayed as one string, wrapping around at the 80th character position. Control characters are displayed preceded by a small c to identify them as such (i.e. Control G is C_G, Control X is C_X, etc.). This mode is extremely useful for debugging computer programs or monitoring completely the communications line data.

2.5 COMMUNICATIONS INTERFACE

This consists of a 25-PIN, rear panel input/output connector marked "SERIAL DATA (RS232-C DTE)" and conforms to the EIA RS232C (CCITT V.24) standards. The pin connections are described in APPENDIX B. A 20 mA current loop can beimplemented using a special cable assembly, Part Number CI04-2M.

RECOMMENDED EIA CABLING LENGTHS

BAUD RATE	MAXIMUM CABLE LENGTH (M)
110	2400
300	1200
600	600
1200	300
2400	150
4800	75
9600	40

For speeds greater than 2400 Baud and lengths greater than 15 meters, all data and control signals should be carried as twisted pairs using pins 1 to 7 as returns.

2.6 MODEMS AND ACOUSTICAL COUPLERS

If external modems and couplers are used, connection to the terminal is made through the 25 PIN RS232C (CCITT V.24) connector. When the computer operates in HALF DUPLEX mode the modem and the terminal must be operating in different modes, otherwise, characters will be repeated on the terminal display screen due to the signal echo back from the modem and the locally generated character.

SECTION 3
INSTALLATION

3.1 INITIAL INSPECTION

Inspect the terminal for physical damage. Check the switches, connectors, and video screen. The original shipping carton should be kept for possible future shipping of the terminal.

3.2 CLAIMS FOR TRANSIT DAMAGE

If physical damage is evident or instrument does not perform correctly when received, notify the nearest Volker-Craig Ltd. Sales/Service office. Arrangements will be made for repair or replacement of the terminal.

VISIBLE DAMAGE

1. Accept the merchandise and sign the receipt as damaged.
2. Keep all packing materials.
3. Notify Volker-Craig Ltd. shipping department of the damage, waybill number, and all other pertinent information.
4. Call the carrier and request an immediate inspection.
5. Return the merchandise via the same carrier to Volker-Craig Ltd. INCLUDE A COPY OF THE CARRIER'S INSPECTION REPORT WITH THE SHIPMENT.

HIDDEN DAMAGE

1. CALL THE CARRIER AND REQUEST AN IMMEDIATE INSPECTION.
2. Notify Volker-Craig Ltd. shipping department.
3. Keep all packing materials.
4. Return the merchandise via the same carrier to VCL. INCLUDE A COPY OF THE CARRIER'S INSPECTION REPORT WITH THE SHIPMENT.

3.3 INSTALLATION

The Volker-Craig Terminal can be installed in a number of configurations and locations. Its portability lends itself to being moved easily from one location to another as user requirements change. For use with a telephone, an acoustic coupler can be plugged in directly.

All cable connections are made at the rear panel of the terminal. The following cable connections are necessary:

1. Power cable from terminal to AC outlet 115V +/-10VAC, 50/60 Hz. With the export model these units require the power cable to be connected to an AC outlet 230V +/-20VAC 50/60 Hz. The internal refresh rate switch must agree with the line frequency.
2. Video cable from terminal rear panel connector marked VIDEO to monitor (If remote slave monitor is required, impedance = 75 ohms).
3. One of the following interfaces is required:
   A. An RS232C (CCITT V.24) 25-pin connector and cable from central computer, multiplexer, or external modem, to the rear panel connector marked SERIAL DATA.
   B. If a 20 mA. current loop interface is required, connection is made to the same connector using a special interface cable (P/N CI04-2M).

SECTION 4

SALES-SERVICE SUPPORT

4.1 WARRANTY

Volker-Craig Ltd. warrants all products against defects in materials and workmanship for a period of ninety (90) days from the date of shipment. The warranty is limited to the servicing and adjustment of any product returned to Volker-Craig Ltd. for that purpose. Included is the replacement or repair of any product or any part thereof. Transportation charges must be prepaid by the purchaser.

This warranty shall not apply to any product or part thereof that is defective or unworkable due to abuse, mishandling, accident, alteration, negligence, or improper installation. Volker-Craig Ltd. reserves the right to service equipment at the customer's site. No other warranty is expressed or implied and Volker-Craig Ltd. is not liable for consequential damages.

4.2 SERVICE REQUESTS

Volker-Craig Ltd. is concerned with "after sales" service support. To ensure fast and efficient service we suggest the following procedure when calling VCL main plant or any sales/service office.

1. Give the Volker-Craig model number and serial number of the defective instrument (an Instrument History file and Unit Control Record is kept on each instrument).
2. Supply the exact physical location of the equipment, i.e., building, department, room number, and/or person to contact for further information.
3. Describe to the best of your ability the nature of the trouble so that we may form a "mental picture" of the problem. (Many service problems are solved over the telephone).
4. The necessary action to solve the outstanding problem will be taken by VCL personnel as quickly as possible.

APPENDIX A

DIRECT X-Y CURSOR ADDRESS COMMAND (CTRL P,Y,X)

The cursor address command allows the cursor to move to the screen position specified by the next two characters. The 7 bit ASCII code for the first character entered gives the Y-Position and the 7-bit ASCII code for the second character entered gives the X-Position. The character co-ordinates are in binary format (offset by 20 Hex).

X-POSITION	CHARACTER
0	(Space)
1	!
2	"
3	#
4	$
5	%
6	&
7	'
8	(
9	)
10	*
11	+
12	,
13	-
14	.
15	/
16	0
17	1
18	2
19	3
20	4
21	5
22	6
23	7
24	8
25	9
26	:
27	;
28	<
29	=
30	>
31	?
32	@
33	A
34	B
35	C
36	D
37	E
38	F
39	G
40	H

X-POSITION	CHARACTER
41	I
42	J
43	K
44	L
45	M
46	N
47	O
48	P
49	Q
50	R
51	S
52	T
53	U
54	V
55	W
56	X
57	Y
58	Z
59	[
60	\
61	]
62	^ (circumflex)
63	_ (underscore)
64	` (grave accent)
65	a
66	b
67	c
68	d
69	e
70	f
71	g
72	h
73	i
74	j
75	k
76	l
77	m
78	n
79	o
No motion	p

Y-POSITION	CHARACTER
0	(Space)
1	!
2	"
3	#
4	$
5	%
6	&
7	'
8	(
9	)
10	*
11	+
12	,
13	-
14	.
15	/
16	0
17	1
18	2
19	3
20	4
21	5
22	6
23	7
No motion	8

APPENDIX B

SERIAL DATA CONNECTOR SIGNALS

Asynchronous Serial Data EIA RS232C (CCITT V.24) Connector Signals (25-PIN Female D-Connector)

Pin Number	Signal Description
1	Chassis Ground
2	Output (Transmit Data)
3	Input (Receive Data)
4	Request to send (Note 1)
5	Clear to send (Note 2)
7	Signal Ground
11	Supervisory Transmit (Note 3)
18	-12V DC
20	Data Terminal Ready (Note 4)

Note 1 In LOCAL mode RTS is OFF. In REMOTE mode RTS turns ON when a character is to be transmitted. RTS turns OFF after a control code has been transmitted.

Note 2 CTS must be ON or open circuited to enable data to be sent. In LOCAL mode this signal is ignored.

Note 3 In LOCAL mode SA is OFF. In REMOTE mode SA is OFF except when the BREAK key is depressed or when the PRINTER BUSY signal is ON at the Serial Peripheral Interface (see APPENDIX C).

Note 4 In LOCAL mode DTR is OFF. In REMOTE mode DTR is ON except when the PRINTER READY signal is OFF at the Serial Peripheral Interface (see APPENDIX C).

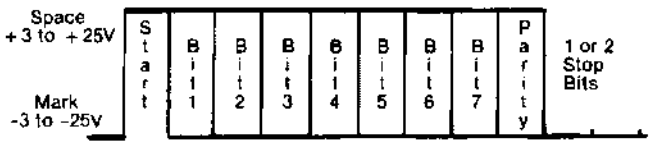
Note 5 All other pins have no internal connections.

RS232 SIGNAL DEFINITION

Marking condition is indicated by a negative voltage from 3 to 25. A Spacing condition is indicated by a positive voltage from 3 to 25.

DATA idle (MARK)

The lease significant bit (LSB) is received first during serial transmission.



There are 2 stop bits at 110 baud and 1 stop bit at all other speeds.

APPENDIX C

OPTIONS

1. APL/ASCII

This option allows the APL (no overstrikes) or ASCII character sets to be selected by the front panel APL/ASCII switch. The APL character set is typewriter paired and the keyboard is defined by clear decals with white legends located on the front of the ASCII keycaps.

2. SERIAL PERIPHERAL INTERFACE (OPTION SPI) (AUDILIARY 25 PIN RS232C PORT)

This bidirectional EIA interface is switched on/off from the keyboard by depressing the illuminating "PRINT" key. With the key depressed, it can also be controlled by means of control codes. Control Q (DC1) will turn on the port and Control S (DC3) will turn off the port (the light will extinguish).

The 25 pin female D-connector signal descriptions and assignments follow RS232C (CCITT V.24) pin conventions (viewed as a modem port). The connector is located on the rear panel.

PIN NUMBER	DESCRIPTION
PIN 1	GROUND
PIN 2	INPUT (Transmit) DATA
PIN 3	OUTPUT (Receive) DATA
PIN 5	ON level (Clear to Send-Note 1)
PIN 6	ON level (Data Set Ready-Note 1)
PIN 7	GROUND
PIN 8	ON level (Carrier Detect-Note 1)
PIN 11	Printer Busy (Supervisory TX-Note 2)
PIN 20	Printer Ready (Data Terminal Ready-Note 3)

NOTES:

Note 1 Pins 5, 6 and 8 are tied to a positive voltage

Note 2 Control signal from printer on pin 11 is propagated to pin 11 on the main I/O connector if SPI is ON.

Note 3 Data Terminal Ready signal from printer is propagated to pin 20 on main I/O connector if SPI is ON. If not used, signal will default to ON.

3. AUXILIARY PARALLEL INPUT (OPTION PIP)

This option provides an auxiliary TTL compatible parallel input to allow connecting parallel devices such as Bar Code Reader Interface or detached numeric key cluster to the auxiliary input of the terminal's control (CON) card. When the auxiliary input is activated by the external device, the terminal's keyboard is disconnected. Once the data from the auxiliary device has been presented to the terminal, it is handled the same as keyboard data. The Input Acknowledge signal goes high when data can be accepted.

The option is terminated on a 25 pin connector mounted on the rear panel of the terminal.

PIN NUMBER	SIGNAL DESCRIPTION
PIN 1	SIGNAL GROUND
PIN 2	INPUT BIT 0
PIN 3	INPUT BIT 1
PIN 4	INPUT BIT 2
PIN 5	INPUT BIT 3
PIN 6	INPUT BIT 4
PIN 7	INPUT BIT 5
PIN 8	INPUT BIT 6
PIN 9	INPUT BIT 7 (not used)
PIN 10	INPUT STROBE'
PIN 11	INPUT ACKNOWLEDGE
PIN 12	INPUT SELECT'
PIN 13	+5VDC

4. COLOURED DISPLAY SCREEN (OPTION CDS)

This option allows the selection of a coloured anti-glare display screen instead of the standard grey/white display. Specify amber or green.

5. NUMERIC AND FUNCTION KEYS (OPTION KB1)

A numeric pad and function keys are added to the keyboard layout. This option is most useful for data entry applications and terminal requirements where user definable key commands are necessary. Twelve function keys appear as the top row of keys on the keyboard. These 12 keys issue the following ASCII Control Codes:

PF1 CTRL A (SOH)	PF7 CTRL R (DC2)
PF2 CTRL B (STX)	PF8 CTRL T (DC4)
PF3 CTRL C (ETX)	PF9 CTRL \ (FS)
PF4 CTRL D (EOT)	PF10 CTRL] (GS)
PF5 CTRL E (ENQ)	PF11 CTRL ^ (RS)
PF6 CTRL F (ACK)	PF12 CTRL - (US)

APPENDIX D

ACCESSORIES

CURRENT LOOP ADAPTOR CABLE (CI04-2M)

To operate the terminal in a current loop, a current loop cable (P/N CI04-2M) must be ordered with the terminal. This cable contains an interface which connects the EIA levels to current loops. The cable is plugged into the 25-PIN SERIAL DATA connector. Current loop terminations do not appear directly on a rear panel connector. The Voltage-Current conversion circuitry is located within the cable.

CURRENT LOOP SIGNAL DEFINITION

A marking condition is indicated by a current flow of 20mA. A spacing condition is indicated by a lack of current flow. The least significant bit is the first data bit during communication.

RS232C DATA COMMUNICATIONS CABLE (CE01-2M)

Terminal to data set cable, 2 metres in length. This cable carries the signals between pins 1, 2, 3, 4, 7, and 20.

MAC

Modem and coupler. Designed for data communications over standard phone lines at rates to 300 baud. Modem circuitry is located in the external acoustic phone coupler. Plugs into SERIAL DATA connector using an RS232C Terminal to Data Set cable (Part No. CE01-2M)

MTI

Multiple Terminal Interface. Small compact switching box connects up to five terminals to one serial printer. Any one of five terminals is selected by a front panel rotary switch.

BRI

Bar Code Reader Interface. Connects Monarch Marking System 2243 parallel scanner to the terminal via the auxiliary parallel input option, OPTION PIP.

APPENDIX E

INTERNAL SETTINGS

BACKPLANE BOARD (BAC-1):

It is possible to operate the terminal on a line voltage of 230VAC (+ or - 20V) or 115VAC (+ or - 10V). At either voltage the frequency may be 50 or 60 Hertz. The video refresh is not affected and this is separately adjustable.

At the rear left corner of the main printed circuit board (when viewed from the front), two pairs of terminal posts can be seen. For 230V operation the black/yellow and the black/white wires should be connected to the posts marked "230". For 115V operations, these wires should be connected to the posts marked "115".

CONTROL BOARD (CON-1):

At IC (Integrated Circuit) location G6, six jumper pairs provide for the following features:

LABEL	FEATURE
TSP	When installed, this jumper permits normal operation in the transparent (or tape) mode. When not installed, the terminal will not display the control codes.
FDX	When installed, RTS is held high (ON) in FULL Duplex, but operates normally in HALF Duplex. Both FDX and RTS jumpers should not be installed at the same time.
RTS	When installed, this jumper ties the RTS signal high (ON state). Without it, RTS is controlled by the terminal. Do not install both RTS and FDX jumper straps.
SPC	When installed, the NO PARITY position of the PARITY switch produces a SPACING condition. Otherwise, NO PARITY produces a MARKING condition.
FILL	Jumpering this pair causes a fast screen fill of the last character typed on the keyboard.
RPT	Jumpering this pair causes the last character typed to repeat at the maximum rate allowed by the BAUD RATE setting.

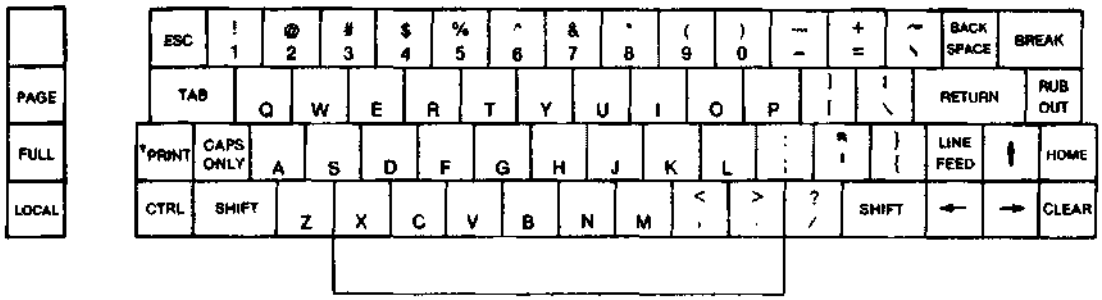
DISPLAY BOARD (DIS-2):

On the Display board, in IC location G4, there are four jumper pairs. These can control the following features:

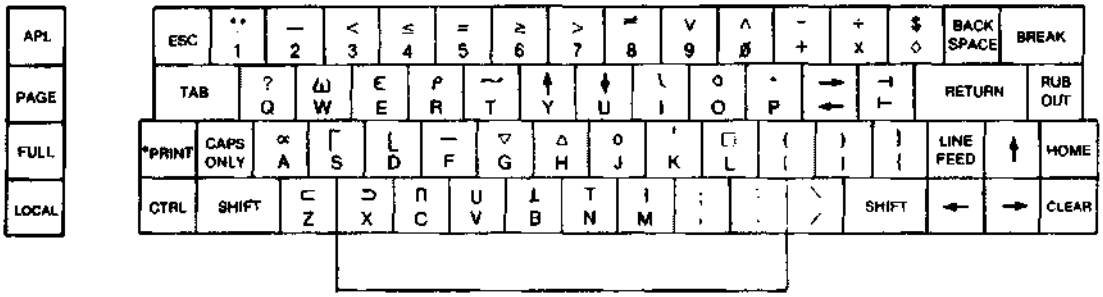
LABEL	FEATURE
FLASH/STDY	When installed, the cursor will flash. Without the jumper, the cursor will remain stationary.
LINE/BLK	When installed, the cursor is an underscore. Otherwise it is a solid block.
50/60	When installed, the refresh rate of the video is 50HZ. When not installed, the refresh rate is 60HZ. This rate should correspond to the power line frequency.
REV/NORM	When this jumper is installed, the screen display consists of black characters on a white background. When not installed, normal video, i.e. white characters on a black background, is effected.

APPENDIX F

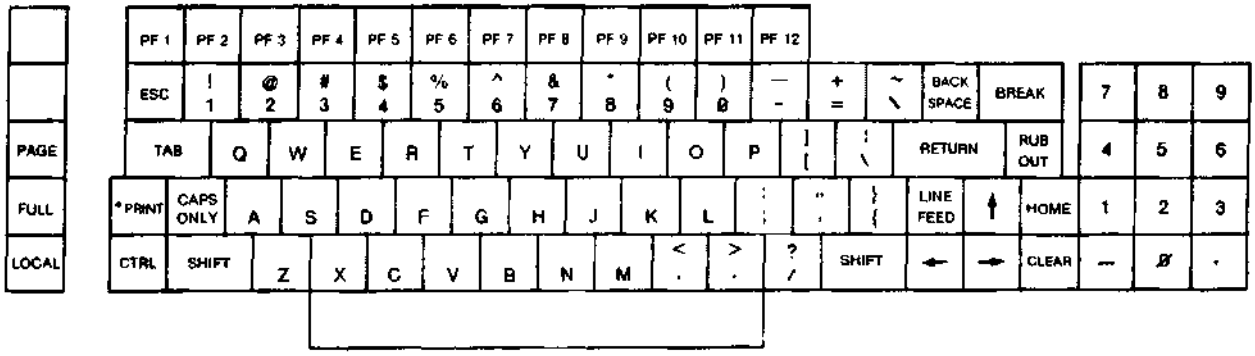
VCL KEYBOARD LAYOUTS



TYPEWRITER LAYOUT (STANDARD)



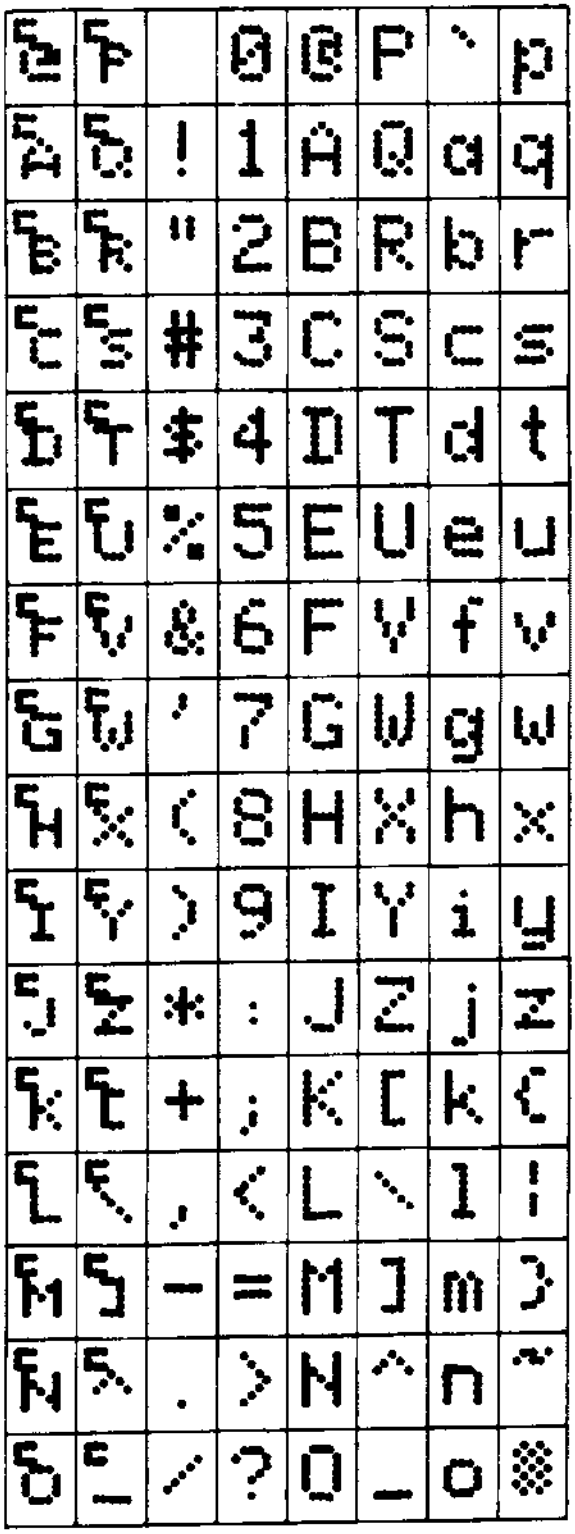
TYPEWRITER-PAIRED APL (OPTION APL)



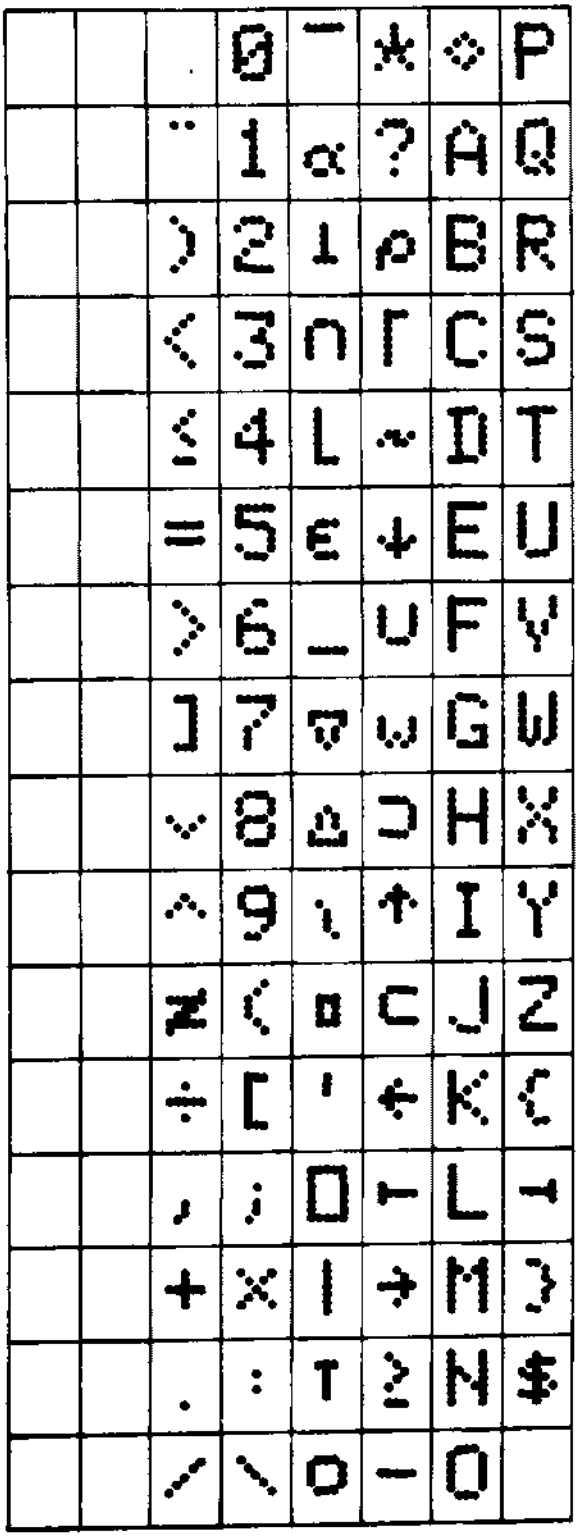
*WITH OPTION SPI

TYPEWRITER LAYOUT WITH NUMERIC PAD AND FUNCTION KEYS (OPTION KB1)

VCL CHARACTER FONTS



UPPER/LOWER CASE ASCII
(STANDARD)



TYPEWRITER PAIRED APL
(OPTION APL)

APPENDIX H VC404 ASCII ENCODING CHART

(Including Hex-code Equivalents)

					← CONTROL CHARACTERS* →		← DISPLAYED CHARACTERS					→
				B7	0	0	0	0	1	1	1	1
				B6	0	0	1	1	0	0	1	1
				B5	0	1	0	1	0	1	0	1
				COL →	0	1	2	3	4	5	6	7
B4	B3	B2	B1	ROW ↓								
0	0	0	0	0	NUL @ 00	DLE (CURSOR ADDRESS) P 10	20	0 30	@ 40	P 50	` 60	p 70
0	0	0	1	1	SOH A 01	DC1 (SPI ON) Q 11	! 21	1 31	A 41	Q 51	a 61	q 71
0	0	1	0	2	STX B 02	DC2 R 12	" 22	2 32	B 42	R 52	b 62	r 72
0	0	1	1	3	ETX C 03	DC3 (SPI OFF) S 13	# 23	3 33	C 43	S 53	c 63	s 73
0	1	0	0	4	EOT D 04	DC4 T 14	$ 24	4 34	D 44	T 54	d 64	t 74
0	1	0	1	5	ENQ E 05	NAK (CURSOR RIGHT) U 15	% 25	5 35	E 45	U 55	e 65	u 75
0	1	1	0	6	ACK F 06	SYN (CLEAR TO EOL) V 16	& 26	6 36	F 46	V 56	f 66	v 76
0	1	1	1	7	BEL (BELL) G 07	ETB CLEAR TO EOS W 17	' 27	7 37	G 47	W 57	g 67	w 77
1	0	0	0	8	BS (CURSOR LEFT) H 08	CAN (CLEAR) X 18	(28	8 38	H 48	X 58	h 68	x 78
1	0	0	1	9	HT I 09	EM (HOME) Y 19	) 29	9 39	I 49	Y 59	i 69	y 79
1	0	1	0	10	LF (CURSOR DOWN) J 0A	SUB (CURSOR UP) Z 1A	* 2A	: 3A	J 4A	Z 5A	j 6A	z 7A
1	0	1	1	11	VT K 0B	ESC [1B	+ 2B	; 3B	K 4B	[5B	k 6B	{ 7B
1	1	0	0	12	FF L 0C	FS \ 1C	, 2C	< 3C	L 4C	\ 5C	l 6C	| 7C
1	1	0	1	13	CR (CARRIAGE RETURN) M 0D	GS] 1D	- 2D	= 3D	M 4D	] 5D	m 6D	} 7D
1	1	1	0	14	SO N 0E	RS ^ 1E	. 2E	> 3E	N 4E	^ 5E	n 6E	~ 7E
1	1	1	1	15	SI O 0F	US _ 1F	/ 2F	? 3F	O 4F	_ 5F	o 6F	DEL 7F

00 Hex-Code

Displayed characters

Terminal Functions

Codes generated and transmitted by terminal but no action taken on display.

*All control Characters displayed in Transparent/Tape Mode i.e. HT as ^{C}I, STX as ^{C}B.

VC404 Specifications

Terminal Type	TTY compatible.	
Configuration	VC404 VC404/EXP VC404/RO	Export version 230V, 50/60 Hz. Also 100V, 50/60 Hz. Receive only terminal (Deletes keyboard from VC404).
Communication	Code	ASCII
	Type	Serial asynchronous.
	Speed	110, 300, 600, 1200, 2400, 4800, 9600, 19200 baud, externally switch selectable.
	Method	Character by character (conversational).
	Mode	Full or half duplex
	Parity	Odd/Even/Mark/Space, switch selectable.
	Interface	EIA RS232C, CCITT-V.24 (20 mA current loop accessory available).
Screen Presentation	Display Unit	30 cm (12 inch) non-glare CRT.
	Display Format	24 lines X 80 characters, 1920 characters.
	Character Type	5 X 7 dot matrix (7 X 10 field).
	Character Size	2 mm x 4 mm
	Character Generation	ROM/PROM.
	Refresh Rate	60 Hz., 50 Hz. switch selectable.
	Refresh Memory	Static RAM.
	Character Set	128 ASCII characters, upper/lower case.
Keyboard	Detached typewriter keyboard with Auto Repeat, Line Feed, Back Space, Cursor Up, Cursor Right, Home, Clear Screen, Escape, Break, Tab, and Caps Lock Keys.	
Data Entry	Roll Mode: Bottom line with single line roll-up. Page Mode: Page overwrite.	
Terminal Functions	Cursor	Non-destructive, blinking block cursor.
	Control Functions	Left, Right, Up, Down, Home, Clear and Home, Direct X-Y cursor addressing using cursor control command, EOL (Clear to End of Line), EOS (Clear to End of Screen).
Audible Alarm	On receipt of Control G (BEL code) from computer or keyboard.	
Operator Controls	Front Panel: Power Off/On, Display Brightness. Rear Panel: Baud Rate, Parity, Transparent/Tape Mode. Keyboard: Local/Remote, Half/Full Duplex, Roll/Page, ASCII/APL.	
Power	115 ± 10 VAC, 50/60 Hz. 50 VA Normal Operating Power, 2A CSA Approval maximum input current unit and attached peripheral, Optional 230 ± 20 VAC 50/60 Hz, 50 VA.	
Overload Protection	Terminal: 1A Fast Blow (0.6A Fast Blow with 230V Option) Display: Internal 3A Fast Blow	
Physical	VC404 VC404/RO Keyboard (KB404 Standard) Keyboard (KB1)	41 cm. W X 52 cm. D X 34 cm. H, 14 kg. 41 cm. W X 37 cm. D X 34 cm. H, 12 kg. 41 cm. W X 20 cm. D X 7 cm. H, 2 kg. 53 cm. W X 22 cm. D X 7 cm. H, 3 kg.
Documentation	VC404 Operator's Manual. VC404 Service Manual (Optional).	

Options

Option APL:	APL/ASCII Switchable Character Set — Typewriter Paired (no overstrikes)
Option SPI:	Switched Serial Bidirectional Peripheral Interface
Option PIP:	Parallel Interface Port
Option CDS:	Coloured Anti-Glare Display Screen (specify Amber, Green)
Option KB1:	Numeric Pad and Twelve Function Keys
Option SSO:	Split Speed Option. Transmit and receive speeds can differ.
Option CCS:	Custom Character Set (Swedish, German, French, etc.)

Interface Cables

CE01-2M: RS232C (CCITT-V.24) Terminal to Data Set Cable

CI04-2M: 20 mA. Current Loop Adaptor Cable

Specifications subject to revision without notice.

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TERMINALS OPERATOR'S GUIDE

NEC

NEC Information Systems, Inc.

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1-79

PROPRIETARY NOTICE

Specifications remain subject to change to allow the introduction of design improvements.

Printed in U.S.A.

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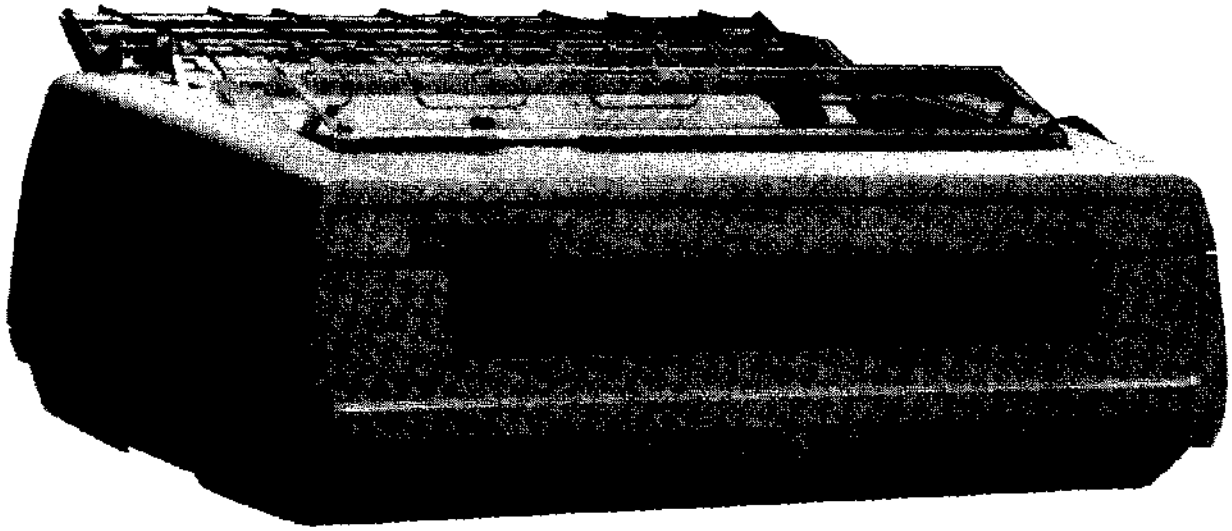
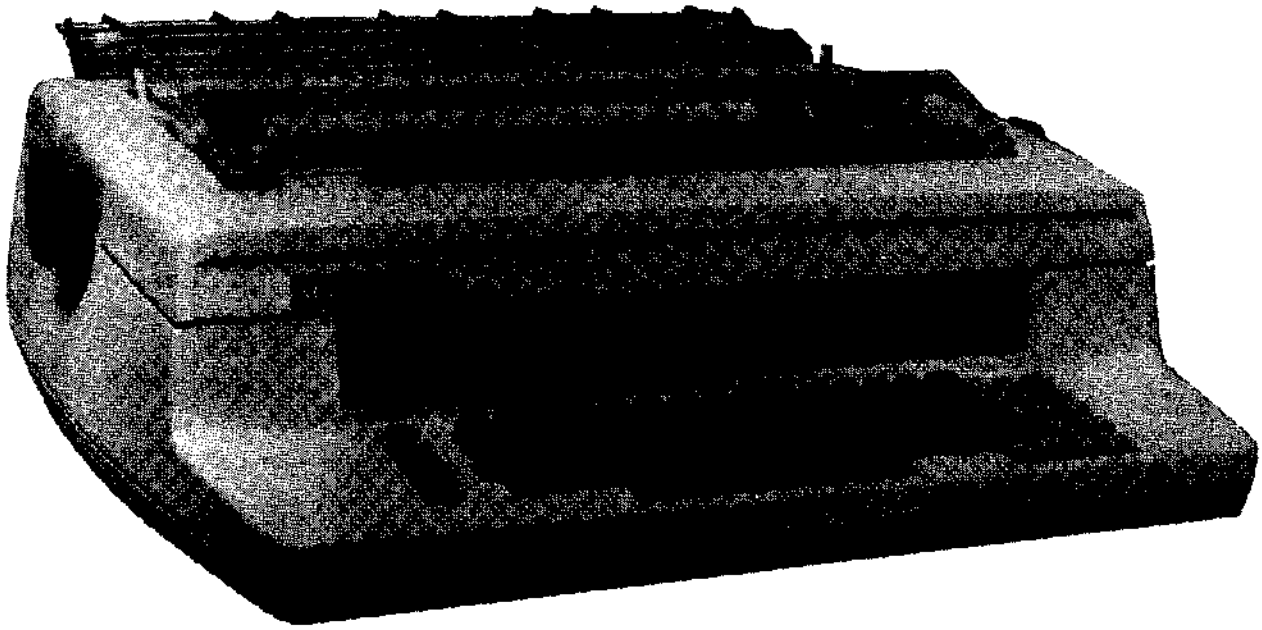


Model 5510 SPINWRITER



Model 5520 SPINWRITER

CHAPTER 1

INTRODUCTION

This guide provides you with a general description, operating instructions, maintenance and replacement procedures, and a troubleshooting guide for SPINWRITER Terminals. Included are specifications, use of operator controls, procedures for replacing certain items, and suggestions to help you maintain high quality printing. A glossary has been added for your use.

1.1 DESCRIPTION

SPINWRITER Terminals are serial-impact character printers which use a microprocessor to control printing operations. Servo motors control carriage movement, print element positioning, ribbon movement and paper movement. The SPINWRITER provides high quality printing at rates up to 55 characters per second (maximum). When used in a standard communication network, the SPINWRITER can communicate in either half duplex or full duplex mode at rates up to 1200 baud. The printing element used by the SPINWRITER is a unique, reinforced plastic "thimble" which contains up to 128 fully formed characters of various typefaces. Thimbles that contain up to 125 characters have a cutout so that you can see the last character printed. The ribbons used are made of black or red/black nylon fabric or of black multi-strike film; the ribbons are contained in easily replaceable cartridges.

You may select the printing format at 10 or 12 characters per inch and up to 163 characters per line. Bidirectional printing, fine-line plotting, and graphing are available. You can position the print thimble within 1/120th inch horizontally and 1/48th inch vertically.

1.2 SPECIFICATIONS

Table 1-1 lists specifications for SPINWRITER Terminals. These specifications should be adhered to for SPINWRITER installation and operation.

Table 1-1 SPINWRITER Terminals Specifications

FEATURE	SPECIFICATION
Print Speed	Standard speed selectable at 110, 300 or 1200 baud....up to 55 characters/in. (maximum) Optional baud rates: 110, 150, 300 110, 200, 300 110, 300, 600
Character Set	128 characters (maximum)
Print Line	136 columns at 10 characters/in. 163 columns at 12 characters/in.
Paper Width	16 in. (maximum)
Paper Thickness	0.027 in. (maximum)
Carriage Return Time	400 ms (maximum)
Horizontal Resolution	120 positions/in.
Vertical Resolution	48 positions/in.
Line Feed Speed	40 ms per 1/6 in. (plus 53 ms settling)
Spacing Speed	16 ms at 12 characters/in.
Tabbing	Horizontal and vertical in any direction
Copy Thickness Control	5-step switching (by operator)
Impression Control	3 levels (by operator)
Overall Dimensions	Width: 24.8 in. (630 mm) Height: 8.68 in. (220.5 mm) Depth 5510: 16.3 in. (415 mm) Depth 5520: 21.1 in. (535 mm)
Weight	5510/15: 45.5 lbs (20.7 kg) including covers and power supply 5520/25: 51 lbs (23.2 kg) including covers and power supply

Table 1-1 SPINWRITER Terminals Specifications (contd)

FEATURE	SPECIFICATION
Power Requirements	115 Vac, ±15%, 50/60 Hz @3.5 amps or 230 Vac, ±15%, @2 amps (option)
Environment	Operating: 40°F (5°C) to 100°F 38°C)
	Storage: -4°F (-20°C) to 158°F (70°C)
Humidity	Operating: 10% to 85% (No Condensation)
	Storage: 10% to 95% (No Condensation)
Altitude	Operating: Sea Level to 10,000 ft
	Storage: Sea Level to 25,000 ft
Acoustic Noise	67 dBA (without Covers)
	60 dBA (with Covers)
INTERFACES	
Model	
5510/20	RS-232-C, Current Loop
5515/25	Diablo-Compatible Plus (Models 1610/1620), RS-232-C - Current Loop Xerox-Compatible Plus (Models 1700/1710)

1.3 RELATED DOCUMENTS

The following documents, relating to the SPINWRITER Terminals, are available from NEC Information Systems, Inc.

SPINWRITER Terminals Product Description, Doc. No. 10005

SPINWRITER Maintenance Manual, Doc. No. 10000

SPINWRITER Theory of Operations Manual, Doc. No. 10001

CHAPTER 2

OPERATING INSTRUCTIONS

This chapter tells you how to operate the SPINWRITER. It describes the control panel switches and indicators, and the keyboard functions; it gives you instructions on how to load the paper and position it, and outlines step-by-step procedures to run the machine. Specific operations vary with the SPINWRITER used and the options included; however, you can use the general information provided here for almost all your needs. Figure 2-1 shows SPINWRITER controls and external components.

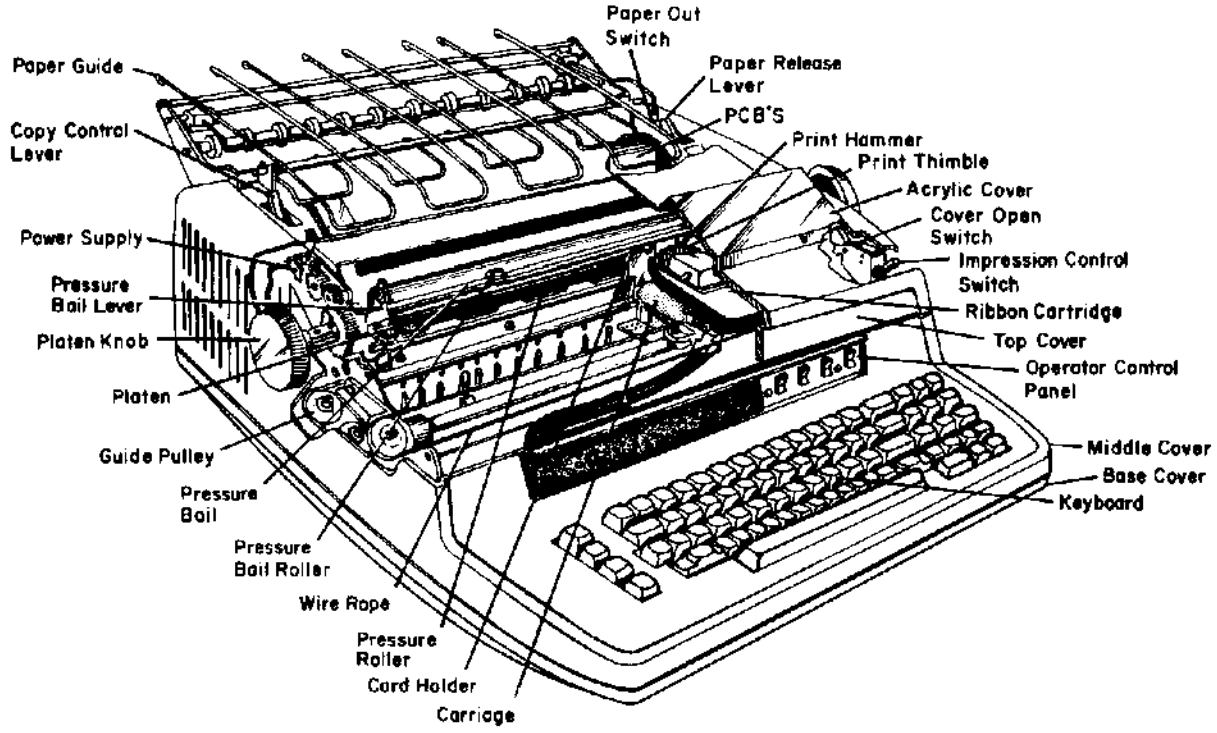


Figure 2-1 SPINWRITER Controls and External Components

2.1 OPERATOR CONTROL PANEL

Table 2-1 lists the controls and indicators on the control panel. The switches on the panel are protected by an acrylic panel. Figure 2-2 shows the two variations of control panels: A is the control panel for Models 5510/5515 and 5520/5525 and B is the control panel for Model 5510 with a remote/local switch.

Table 2-1 Operator Control Panel

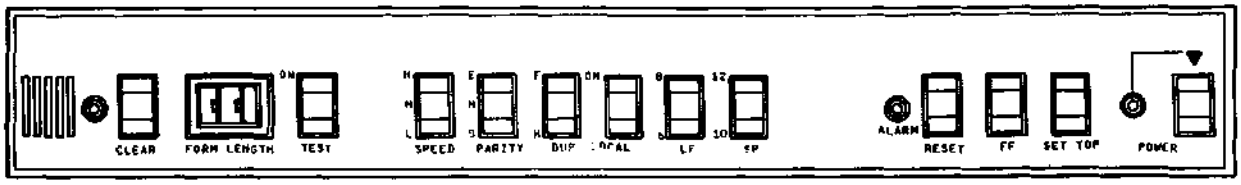
PANEL LABEL	SWITCH/ INDICATOR	FUNCTION
POWER	2-Position Rocker Switch	Controls ac power to SPINWRITER.
POWER	Indicator	Illuminates when ac power is applied.
SET TOF (Top of Form)	Spring-Loaded Rocker Switch	Stores contents of FORM LENGTH thumbwheel switches. Note: Position paper at desired first line before pressing this switch.
FF (Form Feed)	Spring-Loaded Rocker Switch	Moves paper to top line of next form.
ALARM	Indicator	Illuminates if one of following occurs: Parity Error, Framing Error, Cover Open, Paper Out, Ribbon End, Check Condition, Buffer Overflow.
	Audible Alarm	1. Sounds for about 1/2 second when errors are produced. 2. Sounds for about 1/2 second upon receipt of Bell Code. 3. For a check condition, a repeating audible alarm is produced.
RESET	Spring-Loaded Switch	Clears ALARM indicator if alarm condition is cleared. Light is extinguished.
SP 10-12 (Space)	2-Position Rocker Switch	Selects either 10 or 12 characters/in. It is set at 10 for 10-pitch thimbles and 12 for 12-pitch thimbles. NOTE The number of characters/ in. is set by internal program control (Escape code, see 2.2.1).

Table 2-1 Operator Control Panel (contd)

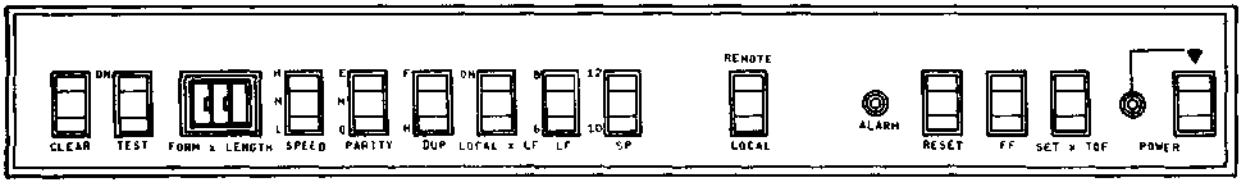
PANEL LABEL	SWITCH/ INDICATOR	FUNCTION
LF 6-8 (Line Feed)	2-Position Rocker Switch	Selects either 6 or 8 lines/ in. for line spacing. NOTE The number of lines/inch is set by internal program (Escape code, see 2.2.1).
LOCAL LF	2-Position Rocker Switch	Enables auto line feed when set at ON, and when carriage return pressed.
DUP F-H (Full, Half)	2-Position Rocker Switch	Selects full or half duplex. At full duplex, data is transmitted but no local printing is performed. At half duplex, data is printed and transmitted.
PARITY E-M-O (Even, Mark, Odd)	3-Position Rocker Switch	Selects odd, even, mark (for mark setting, there is no parity check and mark polarity is generated).
SPEED H-M-L (High, Medium, Low)	3-Position Rocker Switch	Selects high, medium, or low communication speed. Standard configuration of 110, 300, 1200 baud. (For other configurations, contact your local service representative.)
TEST	2-Position Rocker Switch	Enables self-test mode (see 2.6) when placed in ON position. For Model 5525, LOCAL switch on keyboard must be pressed and locked.

Table 2-1 Operator Control Panel (contd)

PANEL LABEL	SWITCH/ INDICATOR	FUNCTION
FORM LENGTH	Two 10-Position Thumbwheel Switches	1. Specify form length -- number of lines from 1 to 99. Read only when printer is powered on and SET TOF is pressed. 2. When in self-test, thumbwheel switch designation, times 10 equals desired column width. (Applies for settings 03 through 13)
CLEAR	Spring-Loaded Rocker Switch	Clears SPINWRITER; equivalent to power ON/OFF clear. NOTE The character set is controlled by an internal program control.
REMOTE/ LOCAL (5510 with Remote/ Local Switch)	2-Position Rocker Switch	In REMOTE position, SPINWRITER receives and transmits data. In LOCAL position, the SPINWRITER is off-line and all data transmissions stop.



A. Control Panel for 5510, 5515, 5520, and 5525



B. Control Panel for Model 5510 with Remote/Local Switch

Figure 2-2 SPINWRITER Terminals Operator Control Panels

2.2 KEYBOARD (Models 5520/5525 Only)

The SPINWRITER keyboard is divided into three sections as shown in Figure 2-3: (A) alphanumeric, (B) numeric, and (C) control.

2.2.1 Alphanumeric Section

Most of the keys in the alphanumeric section function like those on a typewriter. For example, when you press the SHIFT key or SHIFT LOCK key and any of the alphanumeric keys (letter or number), an upper case character prints.

a. Repeat Keys

When you press and hold the SPACE, BACKSPACE, RETURN, LINE FEED, -, or _ keys, the code automatically repeats.

b. Special Keys

Control (CTRL), Escape (ESC), LINE FEED, and Delete (DEL) are special keys. Use the CTRL and ESC keys to vary normal printing operations, carriage movement, or paper movement. These keys are discussed in the following paragraphs.

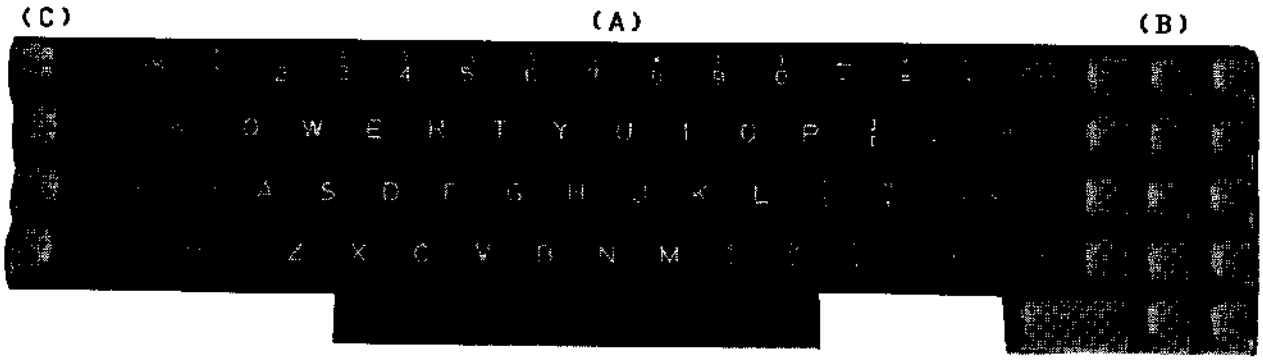


Figure 2-3 Keyboard Layout (Models 5520/5525 Only)

CTRL

The CTRL key, when used with another key, generates a special function or action. For example, when you press "CTRL" and "J" at the same time, a Line Feed occurs. When you press the "CTRL" and "K" keys at the same time, a vertical tab is performed. You can also use the CTRL key for other functions (see Table A-1 in Appendix A).

ESC

The Escape key also generates a special function or machine action when used with another key,. For example, pressing ESC and M (or m) at the same time sets the left margin. Table A-2 lists additional functions performed with the ESC key.

Similarly, using the ESC key with other keys sets horizontal tabulations (Table A-3) and vertical tabulations (Table A-4). To vary spacing between characters and between lines, use the ESC key as detailed in Table A-5. (Table A-6, ASCII Coding Chart, is added for reference purposes.)

For CTRL and ESC key functions for Diablo-Compatible and Xerox-Compatible Plus, see the following tables in Appendix B:

Table B-1: ESC Key Functions

Table B-2: ASCII Coding Chart

Table B-3: Decimal Values for ASCII character for Horizontal Motion Index (HMI)--spacing between character; Vertical Motion Index (VMI)--spacing between lines.

LINE FEED

Press LINE FEED key to advance the paper by one line. No carriage return occurs unless AUTO LINE FEED has been selected internally.

DEL

DEL key, in remote mode, transmits the delete code instead of printing it. In the local mode, this key does not operate.

2.2.2 Numeric Section

The numeric pad (15-key pad) inputs numeric data. Do not use the SHIFT and CTRL keys when inputting numerical data. To help you locate your position on the numeric pad, the number 5 has a raised piece.

2.2.3 Control Section

The control section includes the following keys.

a. LOCAL (Remote)

Press this key to enter the local mode; the key automatically locks. In local mode, the SPINWRITER operates as a typewriter. When you release the LOCAL key, the unit enters the remote mode.

In remote mode, the SPINWRITER receives and transmits data.

b. UC ONLY (Upper Case Only)

When you press this key, it locks in place; and the upper case alphabet replaces the lower case alphabet. This key is effective only on alphabet keys. When you press the key again, it unlocks and the machine prints the lower case alphabet. The incoming data is not affected by the position of this key.

c. BREAK

When you press this switch, a Break signal clears all data in the print buffer.

d. AUTO LF

Pressing AUTO LF and the RETURN key gives you a double line feed. You must have both AUTO LF and LOCAL LF set at ON.

2.3 PAPER POSITIONING AND PRINTING ADJUSTMENTS

Figure 2-4 illustrates the controls you will use to position paper and to make adjustments for print quality. The numbers in the following paragraphs correspond to the numbers in the figure.

(1) Platen knobs. These knobs allow the platen to be rotated manually to insert paper and position it properly. The right knob provides variable platen action; when you push the knob in, the platen rolls freely in either direction. You can change the position of the writing line by using this variable platen function.

(2) Copy control lever. This lever moves the platen forward or backward to compensate for different form thicknesses (number of carbons). Place it all the way forward for a single copy, and all the way rearward for an original and five carbon copies. Intermediate positions provide for form thicknesses between these two extremes. When printing on a form of several copies with this lever moved toward the rear, you may have to increase the print hammer intensity for optimum print quality by changing the impression control switch (see Figure 2-4, 9).

(3) & (4) Pressure bail levers and pressure bail. The pressure bail holds the paper against the platen. This is necessary for optimum print quality and quietness. To insert paper, pull the bail forward, away from the platen, by moving one of the levers. When using a pin-feed platen or a forms-tractor assembly, move the pressure bail forward away from the platen. The pin-feed paper clamps or the forms-tractor assembly doors hold the paper in the optimum position for proper operation.

(5) Ribbon Selector Switch. The ribbon selector switch is located under the top cover under the ribbon cartridge black lever. Place this switch to the left for black ribbon or multi-strike ribbons, and to the right for red/black ribbons.

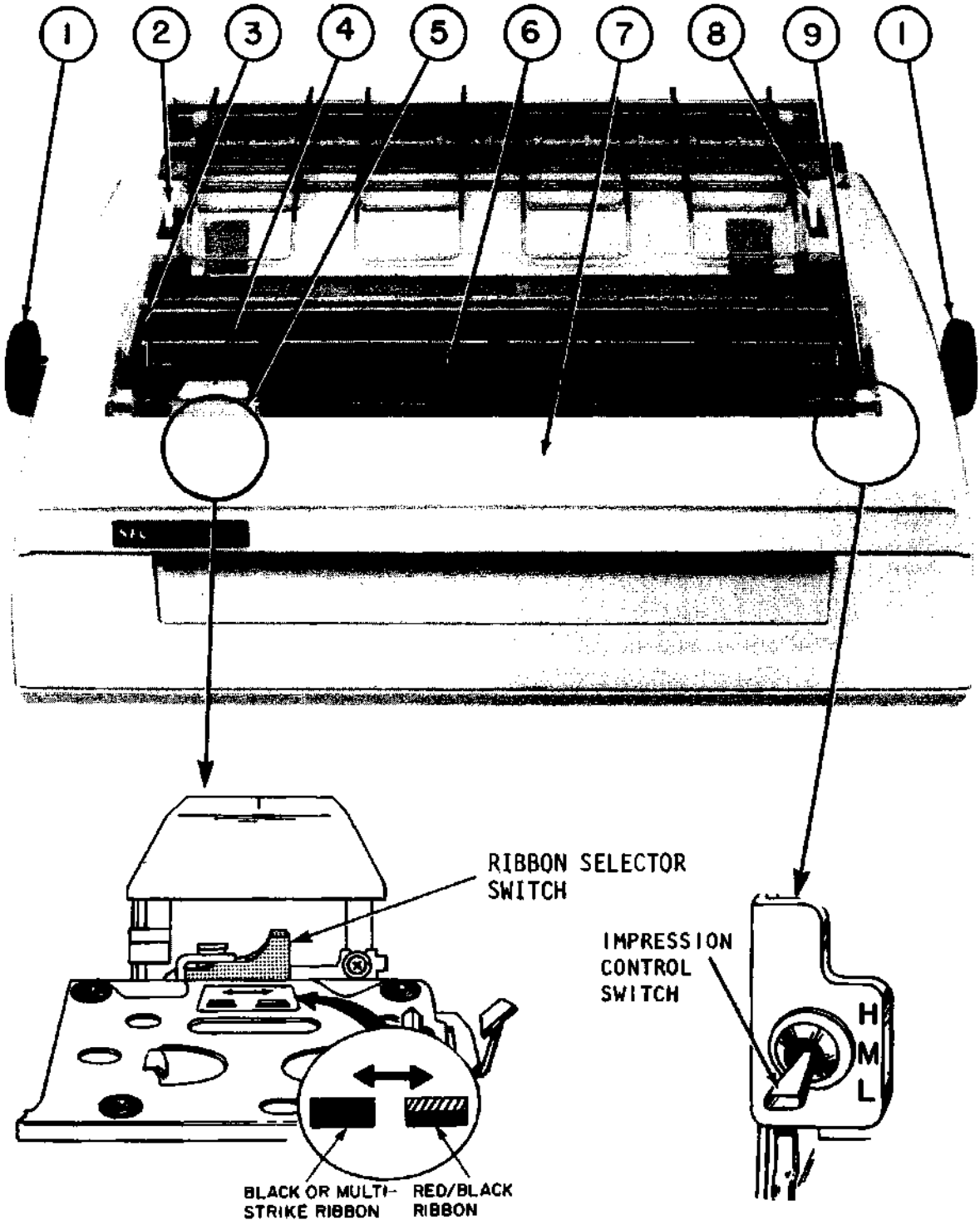


Figure 2-4 Printer Controls

(6) Silencer hood with combination scale. The silencer hood lowers the printer operation noise level. A long and short hood are available, but a short hood must be used with a forms tractor assembly or a pin-feed platen. When you raise the hood, a switch is activated which inhibits printing; therefore, the hood must be closed for printing. The scale on the hood provides a visual indication of the print head position along the typing line. It is marked for both 10 and 12 characters per inch.

(7) Top cover. The top cover raises easily by lifting upward. It provides access to the printer mechanism when it becomes necessary to replace a ribbon cartridge, to change the print thimble, or to change the hammer impression control switch. When you raise the cover, a switch is activated which inhibits printing; the audible alarm sounds and the alarm on the control panel lights. Therefore, be sure the cover is closed tightly.

(8) Paper release lever. In the forward position, this lever releases tension on the paper, allowing you to reposition or remove the paper. Place the lever in the backward position when printing on a friction-feed platen to ensure proper feeding of the paper. PLACE IT FORWARD WHEN PRINTING ON A PIN-FEED PLATEN OR WHEN USING A FORMS TRACTOR ASSEMBLY.

(9) Impression control switch. This three-position switch located under the top cover controls the printing impression. You may set this switch as follows: L-low for minimum impact pressure which may be required for small typefaces (12 pitch); M-medium for normal impact pressure which is required for most single copy printing; H-high for maximum impact pressure normally only for multiple copies. Poor print quality may result from the incorrect setting of this switch; and in addition, too high an impression setting may result in reduced font life.

2.4 PAPER LOADING INSTRUCTIONS

The SPINWRITER has three different types of paper feed: friction feed, pin-feed, and forms-tractor paper feed. When loading paper, refer to the procedure below that applies to the particular type of paper feed for your machine. Figure 2-5 shows rear paper-feed path. Rear feed is similar to paper placement in a typewriter. Figure 2-6 shows you how to load the paper through the bottom of the SPINWRITER. Bottom feed is an optimal feature.

NOTE

If you use a single sheet of paper in the SPINWRITER, raise the paper guide to deactivate the paper out switch.

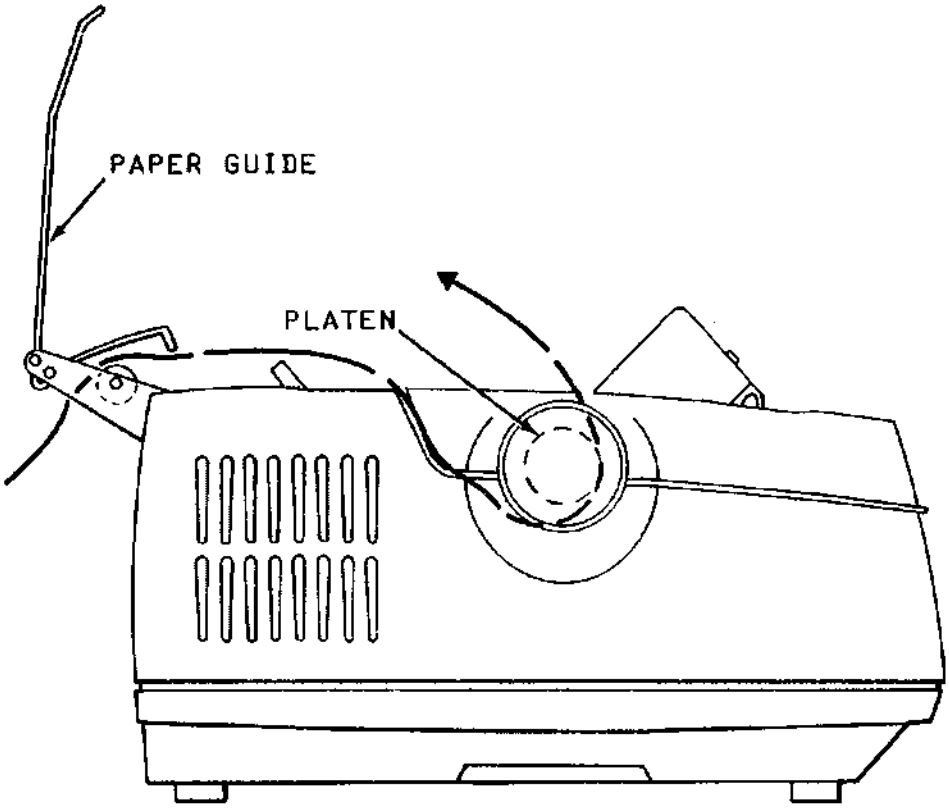


Figure 2-5 Rear Paper-Feed Path

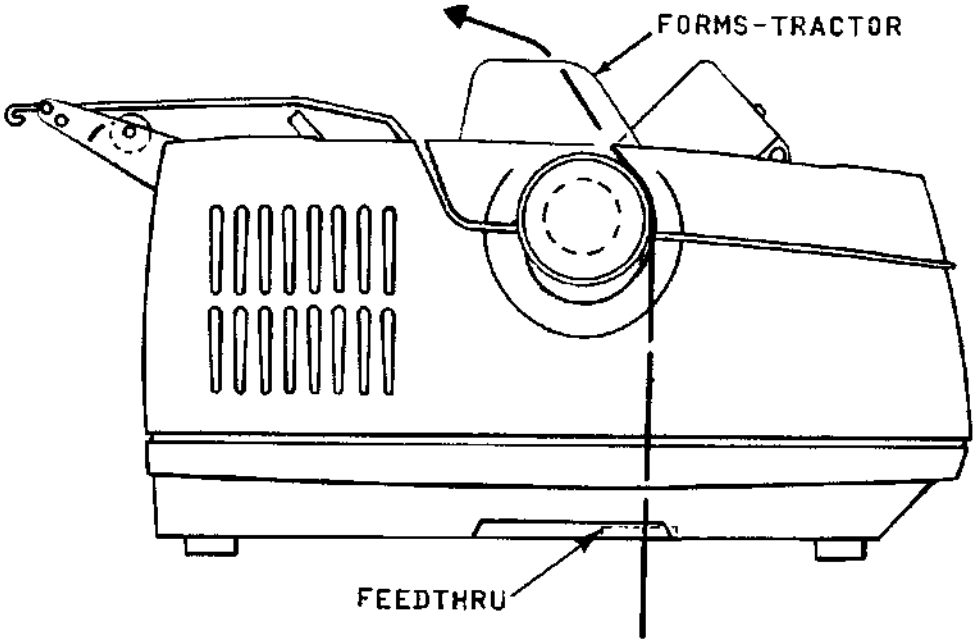


Figure 2-6 Bottom Paper-Feed Path - (Optional Feature)

2.4.1 Friction-Feed Paper Loading

a. Raise paper guide and silencer hood.

b. Move the pressure bail away from the platen.

c. Pull paper release lever forward.

d. Insert paper with printing surface down as shown in Figure 2-5.

e. Push paper release lever backward.

f. Push in and rotate the right knob of the platen to move the paper.

g. Pull paper release lever forward.

h. Align the paper horizontally and vertically.

i. Push paper release lever backward.

j. Push paper bail toward the platen.

k. Move paper to desired top of form position.

l. Adjust copy control lever. Place this lever in extreme forward position for a single copy, and adjust it gradually toward rear as the number of copies increases.

m. Lower the paper guide and silencer hood.

2.4.2 Pin-Feed Paper Loading

a. Raise paper guide and silencer hood.

b. Move the pressure bail away from the platen.

c. Pull paper release lever forward; it must REMAIN in the FORWARD position.

d. Release the paper cutter bail from the platen.

e. Insert paper as shown in Figure 2-5 or 2-6 with printing surface down (for rear feed).

f. Align paper feed holes with the left and right pin on the platen; then lower the cutter bail to the platen.

g. Pull paper toward the back lightly to remove slack.

h. Push in and rotate the right knob of the platen to position the paper to the first line position.

i. Lower the paper guide and silencer hood.

2.4.3 Forms-Tractor Paper Loading

a. Raise paper guide if rear feed is used, and raise the silencer hood.

b. Move the pressure bail away from the platen.

c. Pull paper release lever forward; it must remain in the FORWARD position.

d. Open tractor doors.

e. Insert paper as shown in Figure 2-5 or 2-6 with printing side down (for rear feed).

f. Align paper feed holes with the pins of the left and right tractor assemblies.

g. Close left tractor door.

h. Align right tractor with paper feed holes. You may have to move the tractor assemblies to do this. Release the locking knobs and slide the assemblies to the desired position.

i. Push in and rotate the right knob of the platen to position the paper to the first line position.

j. Lower the paper guide and the silencer hood.

2.5 SPINWRITER PREPARATION

NOTE

Before you apply power to the SPINWRITER, make sure that the carriage is not positioned to the extreme left or to the extreme right.

a. Raise the top cover and check that the impression control switch (see 2.3,9) and the ribbon selector switch (see 2.3,5) are in the correct positions.

b. Make sure paper, ribbon, and print thimble are properly installed.

c. Check to make sure that all front panel control switches are properly set (see Table 2-1).

d. Close the cover.

e. Connect the power cord to an ac outlet.

f. Set the POWER switch to the ON position; observe that the POWER indicator lights, and the carriage moves to the first print position.

g. Place Remote/Local switch on keyboard in desired position (see Table 2-1).

2.6 TYPICAL OPERATING PROCEDURES

To operate the SPINWRITER in the remote mode, you must follow specific procedures. These procedures are determined by the device that the SPINWRITER will communicate with (host device). To communicate between the SPINWRITER and the host device, make sure the operating characteristics of both are compatible. You must establish transmission speed (baud rate), type of data transmission (half or full duplex), and type of parity (see Table 2-1). All SPINWRITER control switches, other than the SP switch, should be set before establishing a communication link. The SP switch is set according to the type of printing thimble used.

2.7 SELF-TEST MODE

SPINWRITER models have a built-in, self-test program which give you a repeated printout of alphanumerics and symbols. Figure 2-7 shows a typical test pattern printout. Press the FORM LENGTH switches (see Table 2-1) to vary the column width and line spacing of the printout. In the Test Mode, with a FORM LENGTH setting of 13, the machine prints the test pattern in 130 columns, as shown in Figure 2-7. If you set the FORM LENGTH switch at any other number, the test pattern is pointed in 30 columns.

Observe the test pattern results. If the machine is malfunctioning, describe these results to your service representative who may provide verbal instructions on how to correct a problem.

To print the test pattern, proceed as follows:

a. Place the TEST switch in the ON position.

b. Press the LOCAL key on the keyboard, and place the TEST switch in the ON position.

c. Place the TEST switch in the OFF position to stop the test.

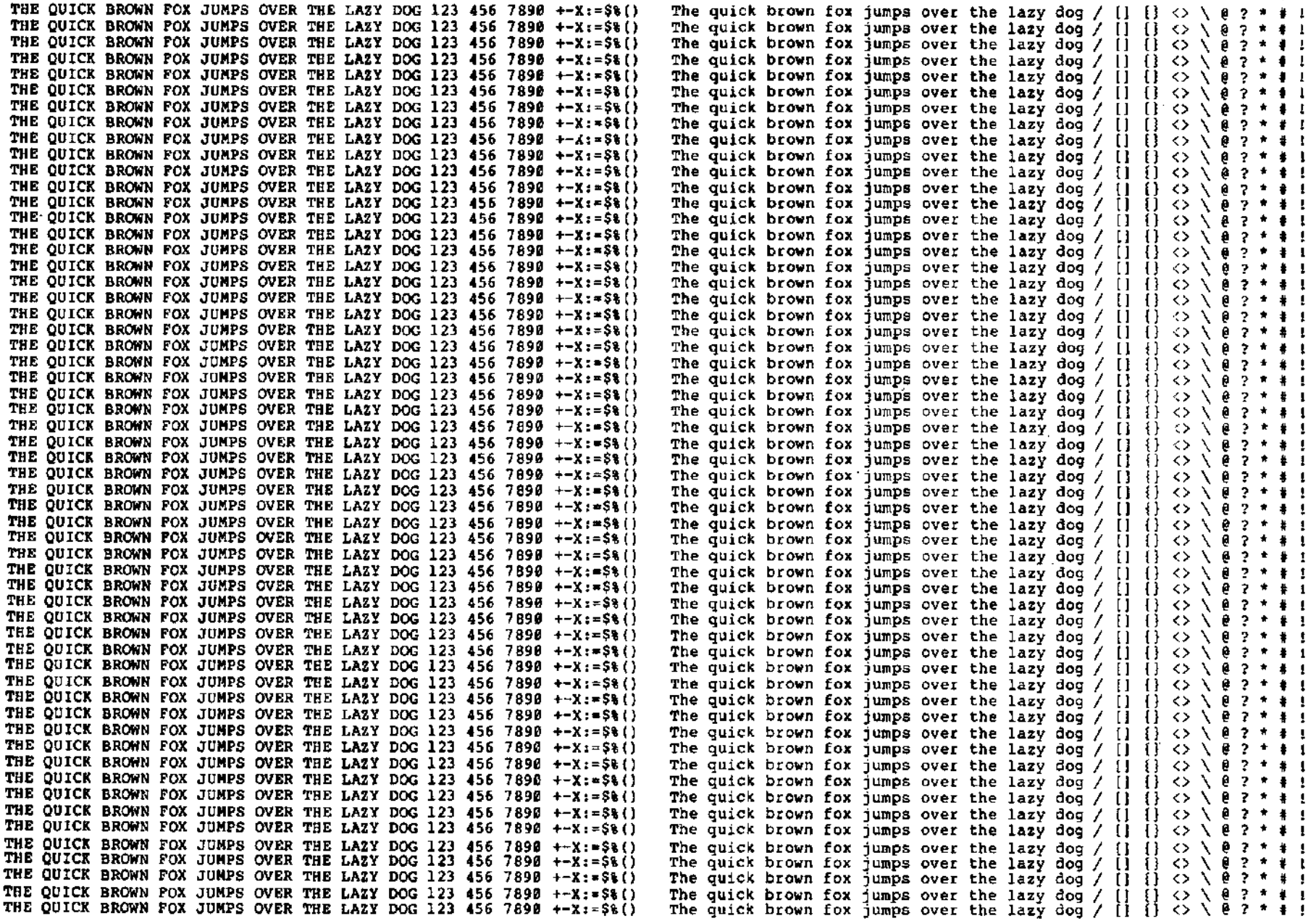


Figure 2-7 Typical Test Pattern Printout

2.8 TROUBLESHOOTING GUIDE

Table 2-2 lists several problems which you may encounter, their causes, and the corrective action which you should take. If, after taking corrective action procedures, the machine is still not functioning properly, call your service representative.

Table 2-2 Troubleshooting Guide

PROBLEM INDICATION	CAUSE	CORRECTIVE ACTION
Does not print (Fan not running)	Power Source	1. Is SPINWRITER connected to ac power? 2. Is POWER switch in ON position?
Does not print No carriage movement Audible alarm sounds once	Cover Open Ribbon End	1. Is cover closed tightly? 2. Check ribbon cartridge. If using a multi-strike ribbon, ensure that ribbon is not at end (window on cartridge will be full). 3. Press RESET switch.
Audible alarm sounds once	Paper Out	1. Check paper supply. 2. Is paper loaded correctly? 3. Press RESET switch.
Does not print No carriage movement Repeating audible alarm	Carriage is in extreme left or right position	1. Turn POWER off. 2. Move carriage to center of machine 3. Turn POWER on. 4. Carriage should move to left margin position.
Carriage movement but does not print	Ribbon broken or not installed properly Thimble broken or not installed properly	1. Replace, if necessary. 2. Are ribbon and thimble installed correctly?
Printing but no carriage movement Alarm may sound	Broken carriage cable Obstruction in path of carriage	Call Service Representative

Table 2-2 Troubleshooting Guide (contd)

PROBLEM INDICATION	CAUSE	CORRECTIVE ACTION
Paper Tearing	Paper not properly loaded Obstruction in paper path If using forms tractors, too much tension may exist Paper release lever may be engaged	1. Check paper loading. 2. Adjust tractors. 3. Check paper release lever (see 2.3).
Printing Light or not sharp	Ribbon worn, jammed or broken Ribbon or thimble not installed properly Copy control lever set incorrectly Impression switch set incorrectly Damaged platen or thimble	1. Replace, if necessary (see 3.2, 3.3). 2. Check installation. 1. Check position of copy control (see 2.3). 2. Check switch setting. 3. Inspect for mars, and/or abrasions Replace, if necessary.
REMOTE OPERATIONS		
Alarm indicator lights Audible alarm sounds once ¬ symbol printed	Parity or framing error	1. Check PARITY and SPEED switches for compatibility with host device (see Table 2-1). 2. Press RESET
Alarm indicator lights Audible alarm sounds repeatedly	Check condition	1. Press CLEAR switch. 2. The printer is set at initial state.
Does not print No carriage movement	No data input	Make sure host device which SPINWRITER is communicating with is operating properly.
Alarm indicator lights Audible alarm	Buffer overflow	1. Check host device for proper operation 2. Press RESET switch.

CHAPTER 3

MAINTENANCE AND REPLACEMENT PROCEDURES

This chapter suggests ways to help you maintain high quality printing. It includes procedures for replacing ribbons, thimbles, and other assemblies.

3.1 MAINTAINING HIGH QUALITY PRINT

To ensure high print quality, proper attention should be given to such items as different printer control settings, paper quality, ribbon quality, etc.

- Select the proper ribbon....multi-strike ribbons give you sharper impressions than a fabric ribbon. Dried or malfunctioning ribbons result in faded print images.

- Choose high quality paper to obtain the best print image....sharpest characters and maximum black-and-white contrast.

- Select the proper copy control lever setting....all the way forward for single copy and moved rearward as necessary for additional copies.

- Set the impression control switch for the best print image.... low for small typefaces (12 pitch), medium for normal impact pressure, and high for large typefaces or multiple copies.

- Set the space pitch setting so that it matches the pitch of the thimble being used....a mismatch will result in cramped or widely spaced characters.

- Align paper correctly with enough tension so that it does not tear or wrinkle.

- Keep the platen clean and free of mars and scratches.

- Establish quality standards for certain jobs....similar jobs will be prepared in a similar manner and require similar quality.

3.2 RIBBON CARTRIDGE REPLACEMENT

Replace the ribbon cartridge as follows:

a. Turn POWER off and raise the top cover.

b. Hold the ribbon cartridge lightly; at the same time, push down on the two locking tabs which hold the cartridge in place, lift the cartridge out (see Figure 3-1).

c. Take the new cartridge and rotate the manual feed knob in the direction indicated by the arrow to establish tension on the ribbon.

d. Place the new ribbon cartridge over the mounting plate; insert the ribbon between the card holder and card holder bracket.

e. Insert the ribbon in the ribbon sensor if a multi-strike ribbon is being used (see Figure 3-2).

f. Press the ribbon cartridge downward until the locking tabs engage.

NOTE

It may be necessary to rotate the manual feed knob on the cartridge in the direction indicated by the arrow to ensure proper seating.

g. Check tension on the ribbon (see step c).

h. Close the top cover and restore ac power.

3.3 PRINT THIMBLE REPLACEMENT

The print thimble may be replaced as follows:

a. Turn POWER off and raise the cover.

b. Remove the ribbon cartridge (see 3.2).

c. Push hammer lock lever toward the platen (Figure 3-2), at the same time tilt the hammer cover toward the front.

d. Slide the lock piece, at the center of the print thimble, horizontally and then to the upright position.

NOTE

When handling print thimble, hold it at the base to avoid possible damage to the character type areas.

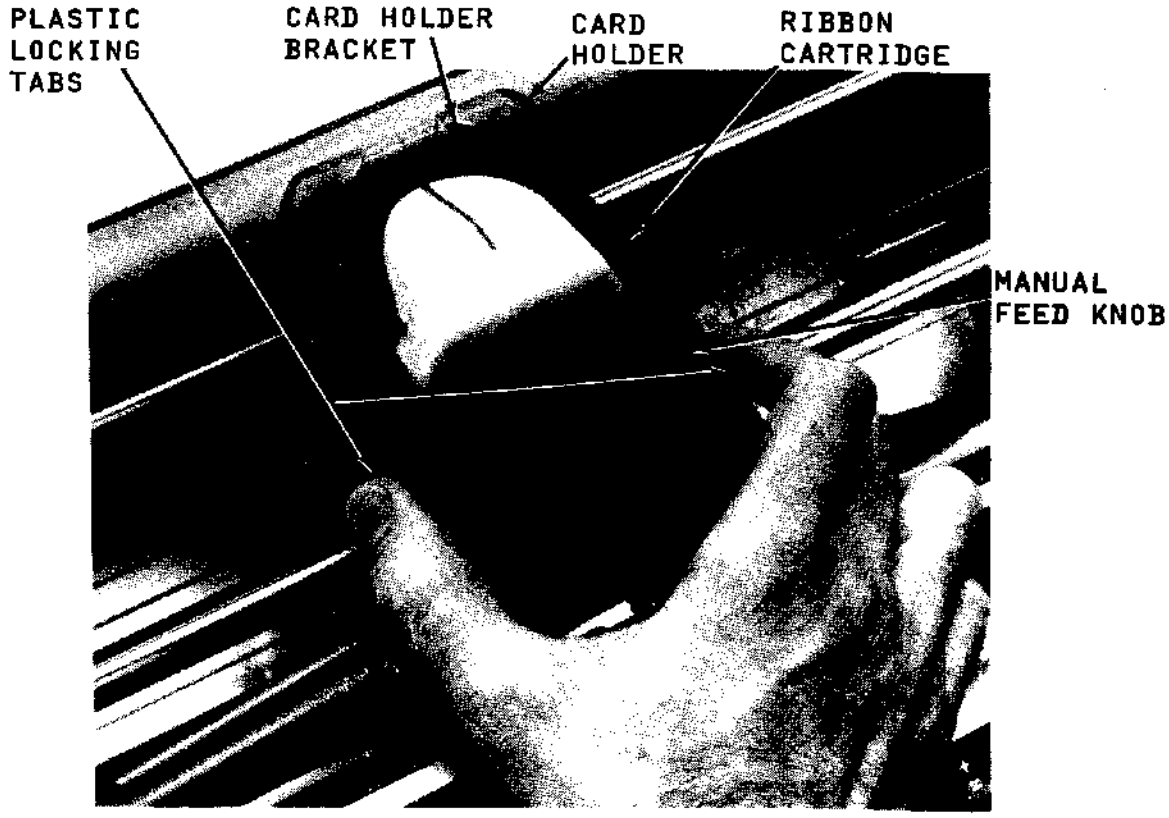


Figure 3-1 Ribbon Cartridge Removal

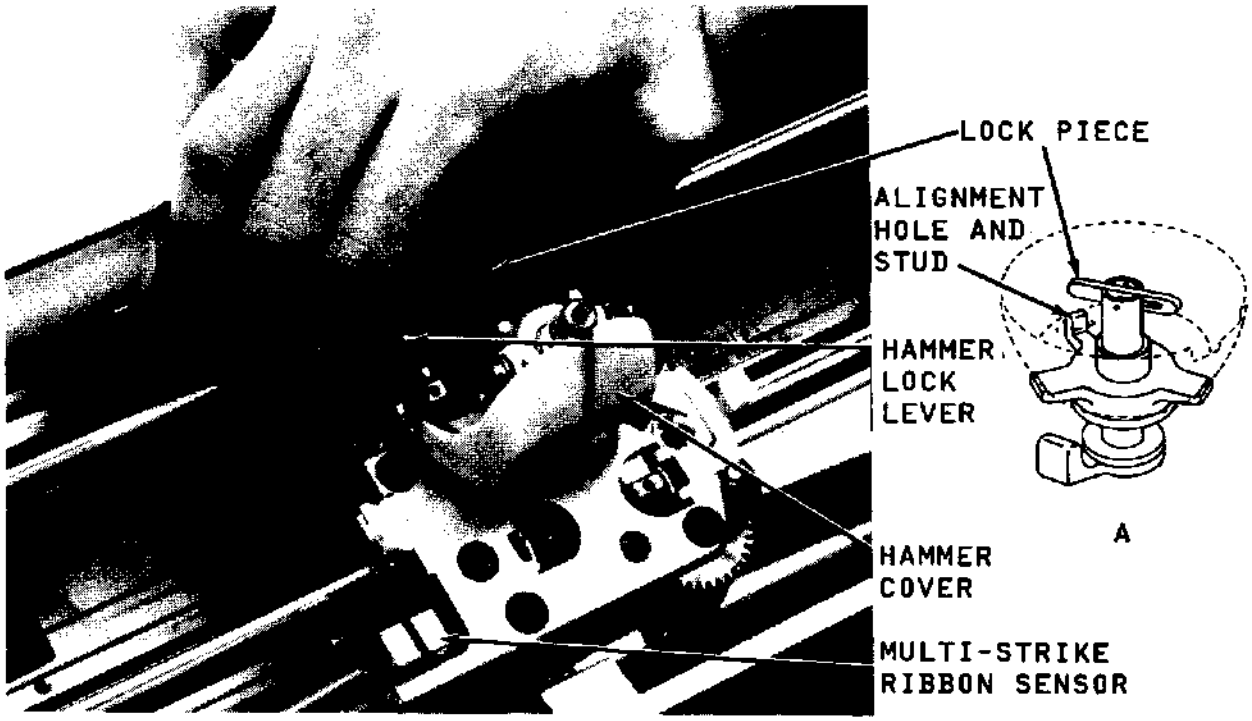


Figure 3-2 Print Thimble Removal

e. Lift the print thimble upward from the carriage.

f. Place new print thimble in position aligning the square hole with the stud (Figure 3-2A).

NOTE

Be sure that the replacement thimble (10 or 12) and the pitch setting match, and use light pressure on the base of the thimble to ensure that it is seated fully downward.

g. Lay the lock piece flat and slide it until it is positioned as shown in Figure 3-2A.

h. Push the hammer and its cover into the locked position.

i. Install the ribbon cartridge.

j. Close the cover and restore ac power.

3.4 FRICTION-FEED ASSEMBLY REMOVAL

If this option is installed, it can be removed in the following manner:

a. Turn POWER off and raise the top cover.

b. Move the pressure bail away from the platen.

c. Press the lock levers and simultaneously raise the assembly upward and toward the rear of the printer as shown in Figure 3-3.

d. Close the cover and restore ac power.

3.5 FORMS-TRACTOR ASSEMBLY REMOVAL

If this option is installed, it can be removed as follows:

a. Turn POWER off and raise the top cover.

b. Move the pressure bail away from the platen.

c. Press the locking levers and raise the assembly upward and toward the rear of the printer to remove it (Figure 3-4).

d. Close the top cover and restore ac power.

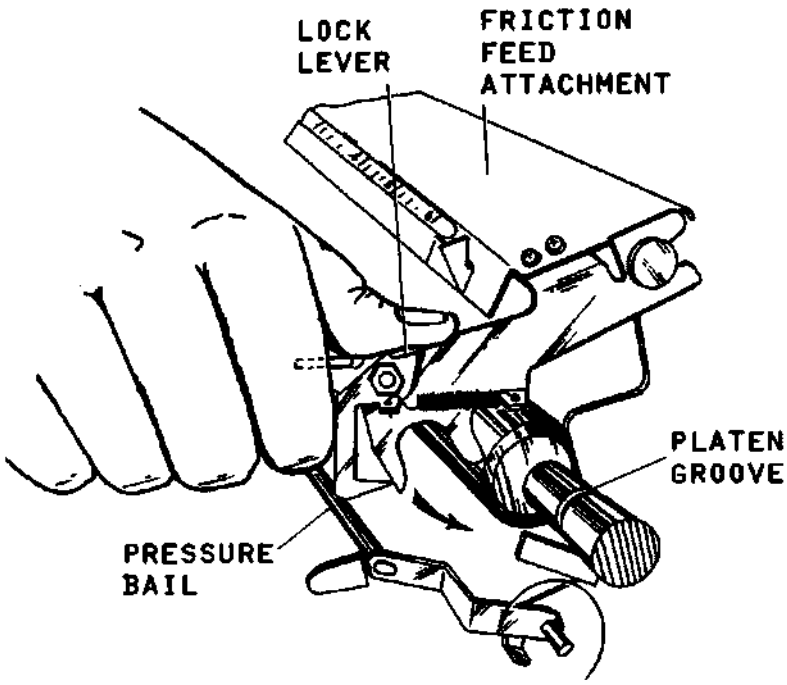


Figure 3-3 Friction-Feed Attachment Removal
(Right Side Only)

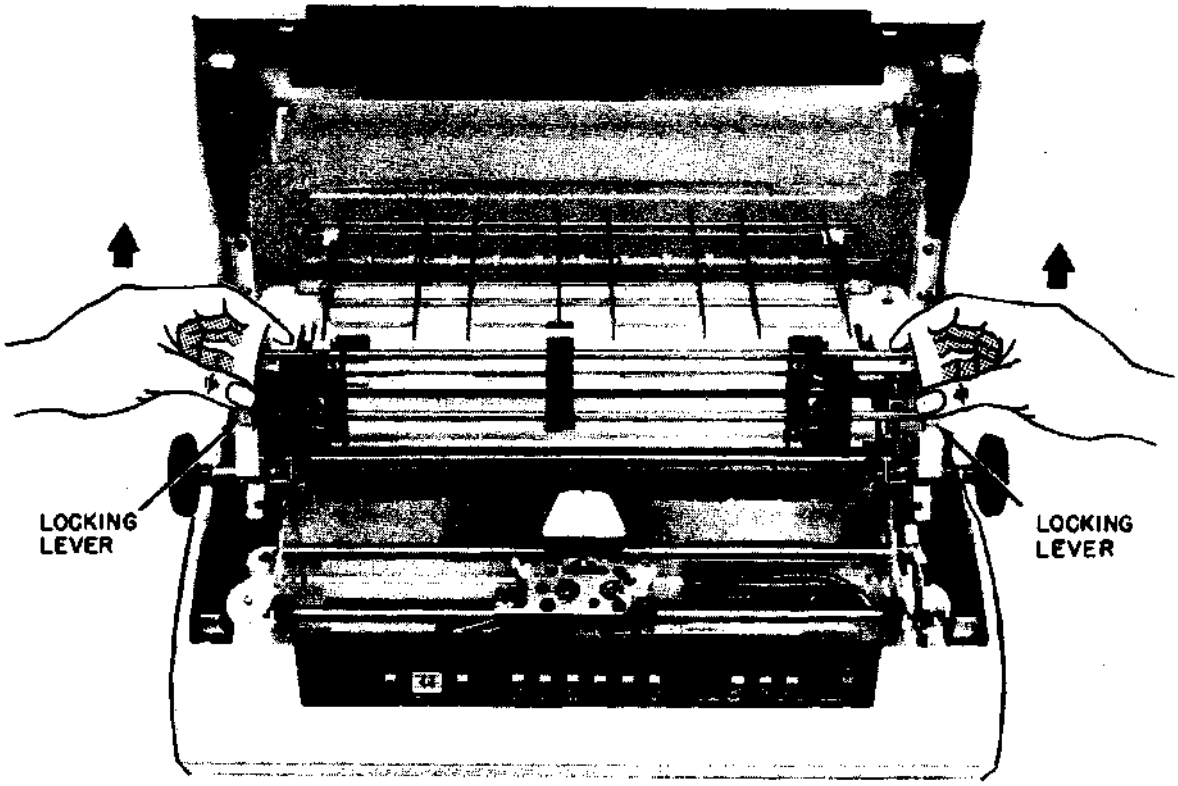


Figure 3-4 Forms-Tractor Assembly Removal

3.6 PIN-FEED PLATEN REMOVAL

If this option is installed, it can be removed as follows:

a. Turn POWER off and raise the top cover.

b. Move the pressure bail away from the platen.

c. Press the locking tabs and lift the platen from the printer (Figure 3-5).

d. Insert the replacement platen into position aligning the platen gear with the line feed idle gear. Press the locking tabs, and press the platen downward until it locks in place.

e. Close the top cover and restore ac power.

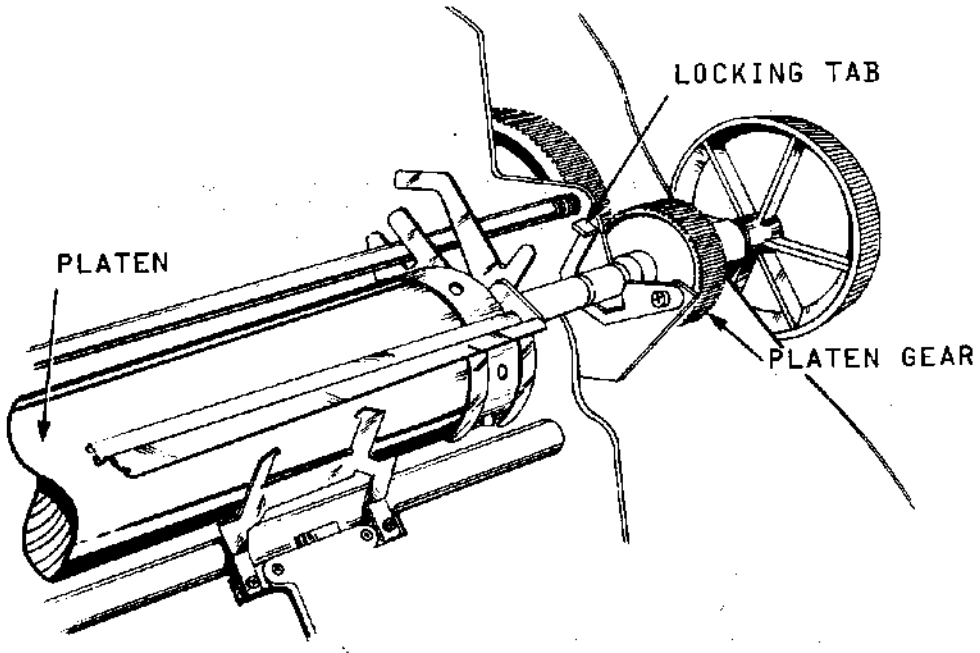


Figure 3-5 Pin-Feed Platen Removal

3.7 FRICTION-PLATEN REMOVAL

The friction platen may be removed as follows:

a. Turn POWER off and raise the top cover.

b. Remove the friction-feed attachment or forms-tractor assembly, if installed.

c. Press the locking tabs and lift the platen upward out of the printer (see Figure 3-6).

d. Insert the replacement platen into position aligning the platen gear with the line feed idle gear.

NOTE

Because it is possible to install the platen backwards, be sure that the widest gear is on the right as the platen is installed from the front.

e. Grasp the platen knobs, press the locking tabs, and press platen downward until it locks into place.

f. Close the top cover and restore ac power.

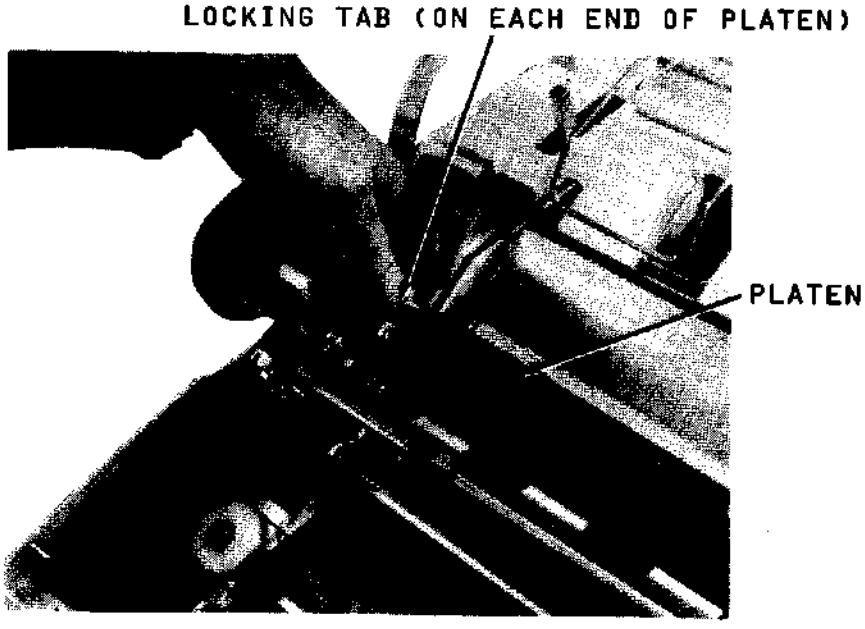


Figure 3-6 Friction-Platen Removal

APPENDIX A

MODELS 5510/20

Table A-1 CTRL Control Key Functions

1st	CTRL
2nd	
A (or a)	SOH (Start of Heading)
B (or b)	STX (Start of Text)
C (or c)	ETX (End of Text)
D (or d)	EOT (End of transmission)
E (or e)	ENQ (Enquiry)
F (or f)	ACK (Acknowledge)
G (or g)	BEL (Bell)
H (or h)	BS (Backspace)
I (or i)	HT (Horizontal Tab)
J (or j)	LF (Line Feed)
K (or k)	VT (Vertical Tab)
L (or l)	FF (Form Feed)
M (or m)	CR (Carriage Return)
N (or n)	SO (Shift Out)
O (or o)	SI (Shift In)
P (or p)	DLE (Data Link Escape)
Q (or q)	DC 1 (Device Control 1)
R (or r)	DC 2 (Device Control 2)
S (or s)	DC 3 (Device Control 3)
T (or t)	DC 4 (Device Control 4)
U (or u)	NAK (Negative Acknowledge)
V (or v)	SYN (Synchronous Idle)
W (or w)	ETB (End of Transmission Block)
X (or x)	CAN (Cancel)
Y (or y)	EM (End of Medium)
Z (or z)	SUB (Substitute)
_ (underline)	US (Unit Separator)
[or {	ESC (Escape)
~ ^	RS (Record Separator)
] }	GS (Group Separator)
\ or |	FS (File Separator)

Example:

To set vertical tab, press the following keys in this order:

1st key CTRL
2nd key K (or k)

Table A-2 ESCAPE Key Functions

ESC 1	Set Horizontal Tab
ESC 2	Reset Horizontal Tab (Individual)
ESC 3	Print in Red
ESC 4	Print in Black
ESC 5	Set Vertical Tab
ESC 6	Reset Vertical Tab (Individual)
*ESC 7	Clear all Tabs and FF Length
ESC 9	Reverse Line Feed
ESC <	Reverse Print (Right-to-Left) On
ESC =	Read and Store Operator Control Switches
ESC >	Forward Print (Left-to-Right) On
*ESC ?	Set Format Mode
*ESC @ CR	Reset Format Mode
ESC J or j	Set Right Margin
ESC K or k	Reset Right Margin
*ESC L or l	Set FF Length
ESC M or m	Set Left Margin
ESC O or o	Reset Left Margin

(Tables A-3 through A-5 list additional ESC functions for Models 5510/5520.)

Examples:

To set the left margin, press the following keys in this order:

1st key ESC
2nd key M (or m)

* You can set FORM FEED (FF) length from the keyboard or from a remote location by using the ESC keys as follows:

1. ESC L (or l)
2. ESC ?

These actions load the number of line feeds into the machine for FF length and Format Mode. Additional ESC key functions reset machine as follows:

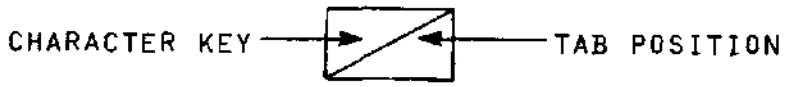
3. ESC L (sets new FF length)
4. ESC @ CR (resets Format mode)

The new FF count will continue to be used until you change FF by any of the following actions:

1. PWR OFF
2. CLEAR
3. ESC L (or l)
4. ESC 7

Table A-3 Horizontal Tab Function

1st	ESC											
2nd	P		Q		R		S		T		U	
3rd	@ 1	P 17	@ 33	P 49	@ 65	P 81	@ 97	P 113	@ 129	P 145	@ 161	
	A 2	Q 18	A 34	Q 50	A 66	Q 82	A 98	Q 114	A 130	Q 146	A 162	
	B 3	R 19	B 35	R 51	B 67	R 83	B 99	R 115	B 131	R 147	B 163	
	C 4	S 20	C 36	S 52	C 68	S 84	C 100	S 116	C 132	S 148		
	D 5	T 21	D 37	T 53	D 69	T 85	D 101	T 117	D 113	T 149		
	E 6	U 22	E 38	U 54	E 70	U 86	E 102	U 118	E 134	U 150		
	F 7	V 23	F 39	V 55	F 71	V 87	F 103	V 119	F 135	V 151		
	G 8	W 24	G 40	W 56	G 72	W 88	G 104	W 120	G 136	W 152		
	H 9	X 25	H 41	X 57	H 73	X 89	H 105	X 121	H 137	X 153		
	I 10	Y 26	I 42	Y 58	I 74	Y 90	I 106	Y 122	I 138	Y 154		
	J 11	Z 27	J 43	Z 59	J 75	Z 91	J 107	Z 123	J 139	Z 155		
	K 12	[28	K 44	[60	K 76	[92	K 108	[124	K 140	[156		
	L 13	\ 29	L 45	\ 61	L 77	\ 93	L 109	\ 125	L 141	\ 157		
	M 14	] 30	M 46	] 62	M 78	] 94	M 110	] 126	M 142	] 158		
	N 15	^ 31	N 47	^ 63	N 79	^ 95	N 111	^ 127	N 143	^ 159		
	O 16	_ 32	O 48	_ 64	O 80	_ 96	O 112	_ 128	O 144	_ 160		



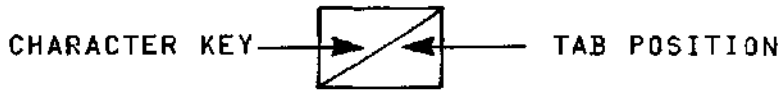
Example:

To tab directly to horizontal position 59, press the following keys in this order:

1st key ESC
2nd key Q (or q)
3rd key Z (or z)

Table A-4 Absolute Vertical Tab Functions

1st	Reverse				Forward			
	ESC				ESC			
2nd	X		Y		Z		{	
3rd	@ 0	P 16	@ 32	P 48	@ 0	P 16	@ 32	P 48
	A 1	Q 17	A 33	Q 49	A 1	Q 17	A 33	Q 49
	B 2	R 18	B 34	R 50	B 2	R 18	B 34	R 50
	C 3	S 19	C 35	S 51	C 3	S 19	C 35	S 51
	D 4	T 20	D 36	T 52	D 4	T 20	D 36	T 52
	E 5	U 21	E 37	U 53	E 5	U 21	E 37	U 53
	F 6	V 22	F 38	V 54	F 6	V 22	F 38	V 54
	G 7	W 23	G 39	W 55	G 7	W 23	G 39	W 55
	H 8	X 24	H 40	X 56	H 8	X 24	H 40	X 56
	I 9	Y 25	I 41	Y 57	I 9	Y 25	I 41	Y 57
	J 10	Z 26	J 42	Z 58	J 10	Z 26	J 42	Z 58
	K 11	[27	K 43	[59	K 11	[27	K 43	[59
	L 12	\ 28	L 44	\ 60	L 12	\ 28	L 44	\ 60
	M 13	] 29	M 45	] 61	M 13	] 29	M 45	] 61
	N 14	^ 30	N 46	^ 62	N 14	^ 30	N 46	^ 62
	O 15	_ 31	O 47	_ 63	O 15	_ 31	O 47	_ 63



Example:

To tab to a vertical position 26 lines before the preset line (reverse), press the following keys in this order:

1st key ESC
2nd key X (or x)
3rd key Z (or z)

Table A-5 Spacing and Form Advance Control

		Spacing		Form Advance	
1st	2nd	3rd	(inches)	3rd	(inches)
ESC	]	@	0	P	1/48
		A	1/120	Q	2/48
		B	2/120	R	3/48
		C	3/120	S	4/48
		D	4/120	T	5/48
		E	5/120	U	6/48 (1/8)
		F	6/120	V	7/48
		G	7/120	W	8/48 (1/6)
		H	8/120	X	9/48
		I	9/120	Y	10/48
		J	10/120 (1/12)	Z	11/48
		K	11/120	[	12/48
		L	12/120 (1/10)	\	13/48
		M	13/120	]	14/48
		N	14/120	^	15/48
		O	15/120	_	16/48

Examples:

1. To space characters 12/120-inch apart, press the following keys in this order:

   1st ESC
   2nd]
   3rd L (or l)

2. To space lines 6/48-inch apart (8 lines/inch), press the following keys in this order:

   1st ESC
   2nd]
   3rd U

Table A-6 ASCII Coding Chart

					COMMUNI-CATION CODES *		PRINTABLE CHARACTERS					
b_7 ——					0	0	0	0	1	1	1	1
b_6 ——					0	0	1	1	0	0	1	1
b_5 ——					0	1	0	1	0	1	0	1
Bits	b_4 ↓	b_3 ↓	b_2 ↓	b_1 ↓	Column → / Row ↓	0	1	2'	3	4	5	6	7
	0	0	0	0	0	NUL	DLE	SP	0	@	P	`	p
	0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
	0	0	1	0	2	STX	DC2	"	2	B	R	b	r
	0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
	0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
	0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
	0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
	0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
	1	0	0	0	8	BS	CAN	(	8	H	X	h	x
	1	0	0	1	9	HT	EM	)	9	I	Y	i	y
	1	0	1	0	10	LF	SUB	*	:	J	Z	j	z
	1	0	1	1	11	VT	ESC	+	;	K	[	k	{
	1	1	0	0	12	FF	FS	,	<	L	\	l	|
	1	1	0	1	13	CR	GS	-	=	M	]	m	}
	1	1	1	0	14	SO	RS	.	>	N	^	n	~
	1	1	1	1	15	SI	US	/	?	O	_	o	DEL

*See Table A-1 for definitions of ASCII code.

NOTE: Both column 4 and 5 (capital letter S) and column 6 and 7 (small letter s) of all ESC code sequences have same function (except DEL code).

APPENDIX B

MODELS 5515/25

Table B-1 Diablo-Compatible Plus and Xerox-Compatible Plus Escape Key Functions

CODE(S)	FUNCTION
ESC 1	Set Horizontal Tab Stop
ESC 2	Clear All Tab Stops
ESC 3	Graphics On
ESC 4	Graphics Off
ESC 5	Forward Print On
ESC 6	Backward Print On
ESC 8	Clear Individual Tab Stop
ESC 9	Set Left Margin
ESC 0	Set Right Margin
ESC A	Print in Red
ESC B	Print in Black
ESC D	Negative Half-Line Feed
ESC U	Half-Line Feed
ESC LF	Negative Line Feed
ESC HT (n)	Absolute Horizontal Tab
ESC VT (n)	Absolute Vertical Tab
ESC RS (n)	Define Vertical Motion Index (VMI)
ESC US (n)	Define Horizontal Motion Index (HMI)

1. To set left margin, press the following keys in this order:

   1st key ESC
   2nd key 9

2. To set absolute vertical tab at 52, the following 3-key ESC sequence is used:

   1st key ESC
   2nd key CTRL with K (specifies vertical tab see Table B-2)
   3rd key 5 (print position desired plus one. Table B-3 shows decimal values for ASCII characters.

3. To set absolute horizontal tab at 65 the following 3-key ESC sequence is used:

1st key ESC	
2nd key Tab	
3rd key B	(print position desired plus one per Table B-3)

4. To change spacing between characters (HMI) and between lines (VMI), press ESC key, the CTRL key and another key at the same time, and the desired setting PLUS 1. See Table B-3 for decimal values of the ASCII characters.

   To set HMI at 10, press the following keys in this order:

1st key ESC	
2nd keys CTRL with -	(See Table B-2)
3rd keys CTRL K	(print position desired plus one per Table B-3)

5. To set VMI at 53, press the following keys in this order:

1st key ESC	
2nd keys CTRL with +	(see Table B-2)
3rd key 6	(see Table B-3)

6. To set Graphics, use the ESC 3 key; to Reset, use ESC 4.

While in the Graphics mode, carriage movement is completely separated from printing: i.e., printing a character does not automatically move the carriage. The carriage is moved only by executing a tab, space, carriage return, or backspace operation.

The tab commands operate the same as they do in Normal mode. In Graphics mode, however, the space and backspace commands move the carriage only 1/60 inch instead of the horizontal index selected.

Paper movement commands can be used extensively in Graphics. Vertical Tab (VT) and Form Feed (FF) operations are unchanged, but Line Feed (LF) and Negative Line Feed (ESC LF) cause only 1/48 inch of paper movement, instead of the full line (VMI) movement performed in Normal mode.

Table B-2 ASCII Coding Chart

CONTROL MODE	ASCII CODE	UNSHIFTED MODE	ASCII CODE (HEXADECIMAL)	SHIFTED MODE	ASCII CODE
NUL	00	NUL	00	NUL	00
ESC	1B	ESC	1B	ESC	1B
NUL	00	1	31	!	21
NUL	00	2	32	@	40
NUL	00	3	33	#	23
NUL	00	4	34	$	24
NUL	00	5	35	%	25
NUL	00	6	36	^	5E
NUL	00	7	37	&	26
NUL	00	8	38	*	2A
{	7B	9	39	(	28
}	7D	0	30	)	29
US	1F	-	2D	_	5F
RS	1E	=	3D	+	2B
GS	1D	`	60	~	7E
BS	08	BS	08	BS	08
NUL	00	NUL	00	NUL	00
HT	09	HT	09	HT	09
DC1	11	q	71	Q	51
ETB	17	w	77	W	57
ENQ	05	e	65	E	45
DC2	12	r	72	R	52
DC4	14	t	74	T	54
EM	19	y	79	Y	59
NAK	15	u	75	U	55
HT	09	i	69	I	49
SI	0F	o	6F	O	4F
DLE	10	p	70	P	50
ESC	1B	[	5B	]	5D
FS	1C	\	5C	|	7C
LF	0A	LF	0A	LF	0A
		CTRL LOCK			
SOH	01	a	61	A	41
DC3	13	s	73	S	53
EOT	04	d	64	D	44
ACK	06	f	66	F	46
BEL	07	g	67	G	47
BS	08	h	68	H	48
LF	0A	j	6A	J	4A
VT	0B	k	6B	K	4B
FF	0C	l	6C	L	4C
;	3B	;	3B	:	3A
'	27	'	27	"	22
GS	1D	{	7B	}	7D
CR	0D	CR	0D	CR	0D
		CTRL Function SHIFT			
SUB	1A	z	7A	Z	5A
CAN	18	x	78	X	58
ETX	03	c	63	C	43
SYN	16	v	76	V	56
STX	02	b	62	B	42
SO	0E	n	6E	N	4E
CR	0D	m	6D	M	4D
,	2C	,	2C	<	3C
.	2E	.	2E	>	3E
/	2F	/	2F	?	3F

Table B-3 Decimal Values for ASCII Characters

Tens	Units 0	1	2	3	4	5	6	7	8	9
0		SOH	STX	ETX	EOT	ENQ	ACK	BEL	BS	HT
10	LF	VT	FF	CR	SO	SI	DLE	DC1	DC2	DC3
20	DC4	NAK	SYN	ETB	CAN	EM	SUB	ESC	FS	GS
30	RS	US	SP	!	"	#	$	%	&	
40	(	)	*	+	,	-	.	/	0	1
50	2	3	4	5	6	7	8	9	:	;
60	<	=	>	?	@	A	B	C	D	E
70	F	G	H	I	J	K	L	M	N	O
80	P	Q	R	S	T	U	V	W	X	Y
90	Z	[	\	]	^	_	`	a	b	c
100	d	e	f	g	h	i	j	k	l	m
110	n	o	p	q	r	s	t	u	v	w
120	x	y	z	{	|	}	~			

GLOSSARY

Absolute tabbing	-	The machine tabs directly to specified print column or line (no previous tab set has been made).
Baud rate	-	The number of characters transmitted per second.
Bidirectional	-	The machine prints while the print head is moving either right or left.
Buffer overflow	-	Buffer overflow occurs when data is transmitted faster than the 256-character buffer can accept it.
Character set	-	A set or style of alphabetic, numeric, and special characters (symbols).
Forms tractor unit	-	A device for aligning and feeding continuous forms through the printer.
Framing error	-	Data is transmitted to the SPINWRITER in an incorrect format: an error will result from an incorrect baud rate setting or the wrong number of internally programmed start and stop bits.
Parity	-	An internally programmed computer checking method in which the total number of binary 1s or 0s is computed and checked Parity must be compatible between computer system and host device.
Space pitch	-	The number of characters per inch printed.

NEC

NEC Information Systems, Inc.

USER'S COMMENTS FORM

Document: SPINWRITER Terminals Operator's Guide

Document No.: 10003-01

Please suggest improvements to this manual.

Please list any errors in this manual. Specify by page.

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SA850/851 Bi-Compliant™ Double Sided Diskette Storage Drive

Service Manual

Shugart

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

1.0 THEORY OF OPERATIONS

1.1 GENERAL OPERATIONS

The SA850/851 Diskette Drive consists of read/write and control electronics, drive mechanism, read/write heads, track positioning mechanism, and removable Diskette. These components perform the following functions:

- Interpret and generate control signals.
- Move read/write heads to the desired track.
- Read and write data.

The relationship and interface signals for the internal functions of the SA850/851 are shown in Figure 1.

The Head Positioning Actuator positions the read/write heads to the desired track on the Diskette. The Head Load Actuator loads the read/write heads against the Diskette and data may then be recorded or read from the Diskette.

The electronics are packaged on the PCB. The PCB contains:

1. Index Detector Circuits (Sector/Index for SA851).
2. Head Position Actuator Driver
3. Head Load Solenoid Driver
4. Read/Write Amplifier and Transition Detector.
5. Data/Clock Separation Circuits (SA851).
6. Write Protect
7. Drive Ready Detector Circuit.
8. Drive Select Circuits.
9. Side Select Circuit.
10. In Use and Door Lock Circuits
11. Write Current Switching/Read Compensation

1.1.1 HEAD POSITIONING

The read/write heads are accurately positioned by a Fasflex™ metal band/stepping motor actuator system. A precision stepping motor is used to precisely position the head/carriage assembly through the use of a unique metal band/capstan concept. Each 3.6° rotation of the stepping motor moves the read/write head one track in discrete increments.

1.1.2 DISKETTE DRIVE SPINDLE

The Diskette drive motor rotates the spindle at 360 rpm through a belt-drive system. 50 or 60 Hz power is accommodated by changing the drive pulley and belt. A registration hub, centered on the face of the spindle, positions the Diskette. A clamp that moves in conjunction with the latch handles fixes the Diskette to the registration hub.

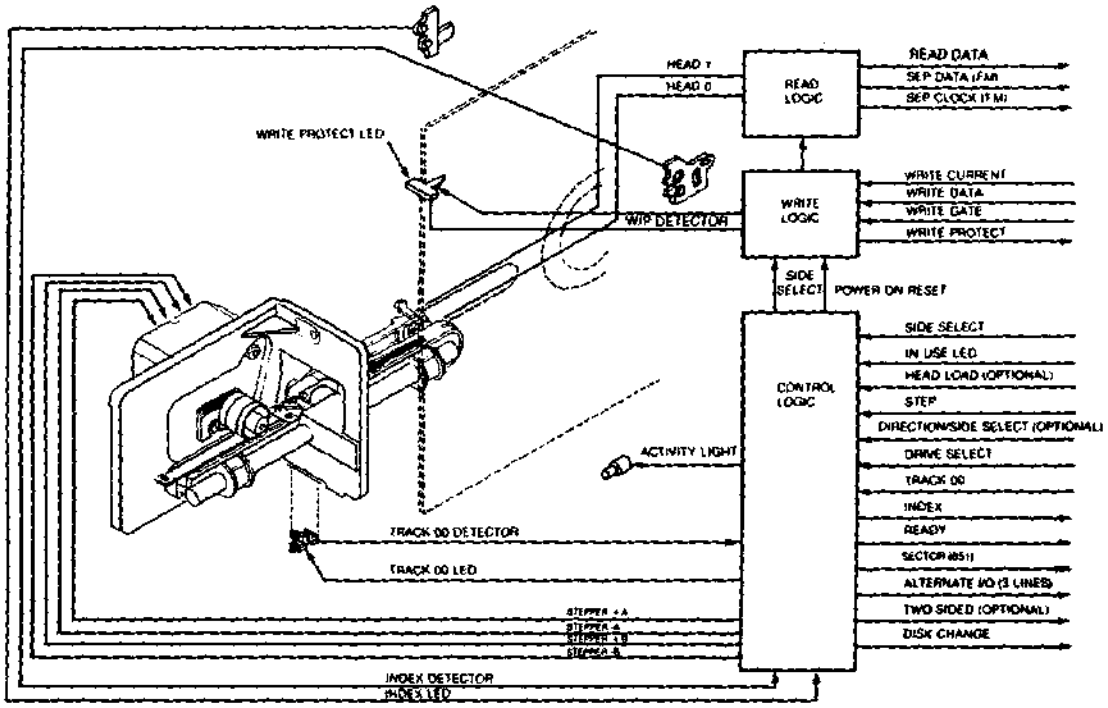


FIGURE 1. SA850/851 FUNCTIONAL DIAGRAM

1.1.3 READ/WRITE HEADS

The proprietary heads are a single element ceramic read/write head with straddle erase elements to provide erased areas between data tracks. Thus normal interchange tolerances between media and drives will not degrade the signal to noise ratio and insures diskette interchangeability.

The read/write heads are mounted on a carriage which is positioned by the Fasflex™ actuator. The head carriage assembly utilizes a combination flexured/rigid head mounting system. This allows the flexured head to load the media against its rigidly mounted counterpart (see Figure 2).

The diskette is held in a plane perpendicular to the read/write head by a platen located on the base casting. This precise registration assures perfect compliance with the read/write heads. The read/write heads are in direct contact with the diskette. The head surface has been designed to obtain maximum signal transfer to and from the magnetic surface of the diskette.

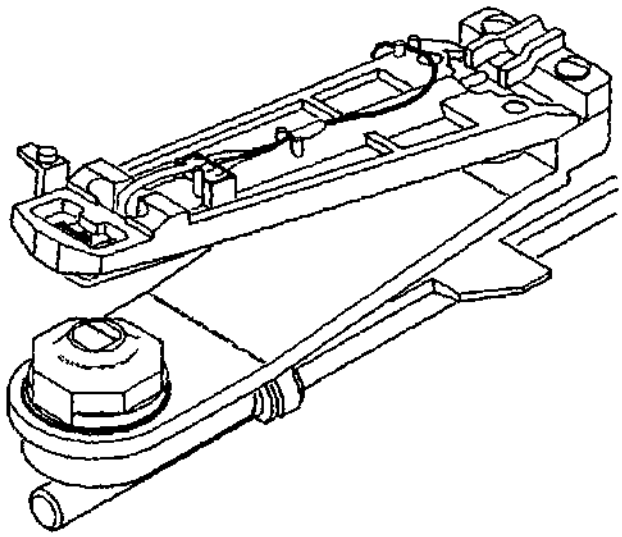


FIGURE 2. BI-COMPLIANT READ/WRITE HEAD

1.2 RECORDING FORMAT

The format of the data recorded on the Diskette is totally a function of the host system. Data is recorded on the diskette using frequency modulation as the recording mode, i.e., each data bit recorded on the diskette has an associated clock bit recorded with it, this is referred to as FM encoding. Data written on and read back from the diskettes takes the form as shown in Figure 3. The binary data pattern shown represents a 101.

1.2.1 BIT CELL

As shown in Figure 4, the clock bits and data bits (if present) are interleaved. By definition, a Bit Cell is the period between the leading edge of one clock bit and the leading edge of the next clock bit.

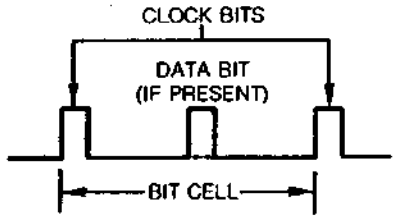


FIGURE 3. DATA PATTERN

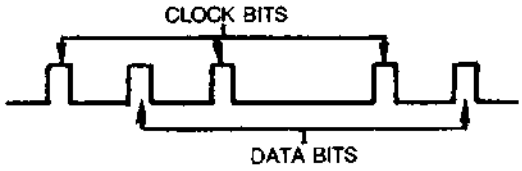


FIGURE 4. BIT CELL

1.2.2 BYTE

A Byte, when referring to serial data (being written onto or read from the disk drive), is defined as eight (8) consecutive bit cells. The most significant bit cell is defined as bit cell 0 and the least significant bit cell is defined as bit cell 7. When reference is made to a specific data bit (i.e., data bit 3), it is with repsect to the corresponding bit cell (bit cell 3).

During a write operation, bit cell 0 of each byte is transferred to the disk drive first with bit cell 7 being transferred last. Correspondingly, the most significant byte of data is transferred to the disk first and the least significant byte is transferred last.

When data is being read back from the drive, bit cell 0 of each byte will be transferred first with bit cell 7 last. As with reading, the most significant byte will be transferred last from the drive to the user.

Figure 4 illustrates the relationship of the bits within a byte and Figure 6 illustrates the relationship of the bytes for read and write data.

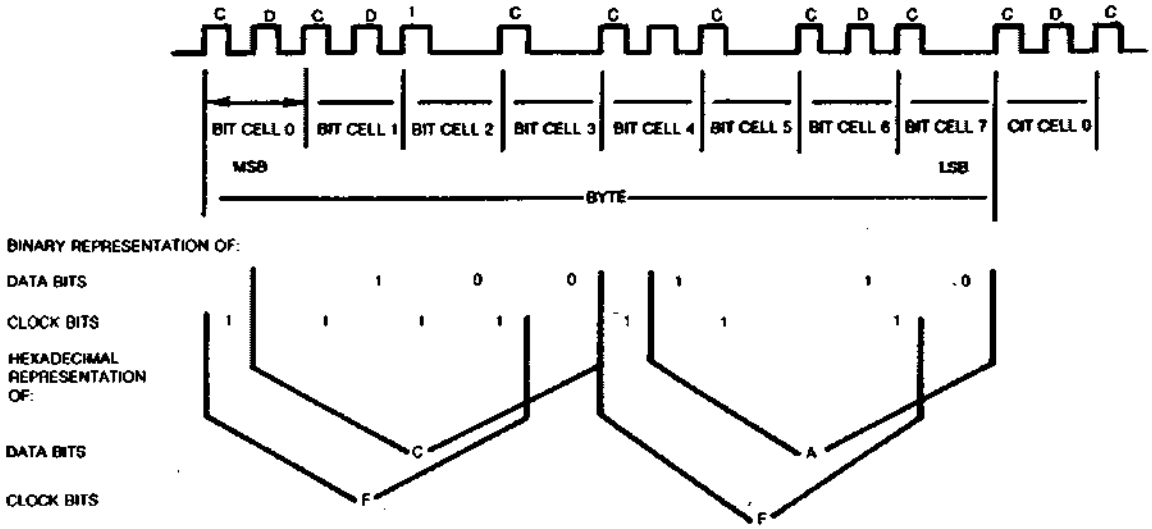


FIGURE 5. BYTE

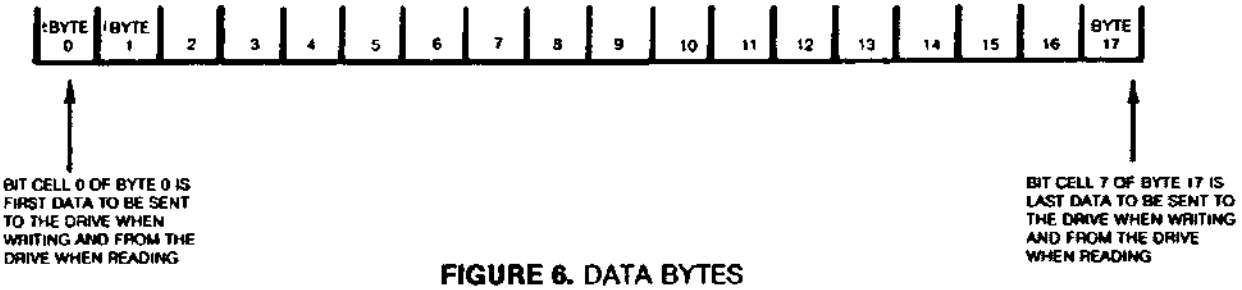


FIGURE 6. DATA BYTES

1.2.3 RECORDING FORMAT (DOUBLE DENSITY)

Double capacity can be obtained by use of MFM (modified frequency modulation) and M²FM (modified, modified frequency modulation) rather than FM (frequency modulation) which is the standard method of encoding data on the diskette.

The differences between FM, MFM and M²FM encoding are shown in Figure 7. Note that MFM and M²FM result in a 1 to 1 relationship between the "flux changes per inch" and the bits per inch recorded on the diskette. This also results in a doubling of the data transfer rate, from 250 to 500 KBS, when compared to FM.

Data error rate performance equal to standard capacity diskettes using FM encoding can be achieved by using:

- The SA850/851 diskette drive with its proprietary ceramic/ferrite read/write head.
- Phase locked loop (VFO) data separator
- Write precompensation.

Provision of the phase locked loop data separator and write precompensation circuitry is the responsibility of the user of the SA850/851 diskette drive.

Shugart Associates will provide design information, as required, to SA850/851 users who desire to incorporate double capacity diskette drives in their products.

The bit cell for MFM and M²FM encoded data is one half the duration of the bit cell for FM encoded data. Also, unlike FM, and MFM and M²FM bit cell does not always contain a clock bit at its leading edge. This lack of clock bit makes data separation more complex. Also, the window size is half the FM window size, which results in less tolerance to bit shift. The only reliable method to separate MFM and M²FM encoded data is through use of a phase locked loop (VFO) type of data separator. The VFO, once synchronized, tracks the data and generates clock and data windows, improving the bit shift tolerance over the conventional "hard" data separators commonly used in FM recording, which use windows of fixed timing.

1.2.3.1 RULES OF ENCODING

FM Encoding:

- Write data bits at the center of the bit cell.
- Write clock bits at the leading edge of the bit cell.

MFM Encoding:

- Write data bits at the center of the bit cell.
- Write clock bits at the leading edge of the bit cell if:
  1) There is no data bit written in the previous bit cell, and
  2) There will be no data bit written in the present bit cell.

M²FM Encoding:

- Write data bits at the center of the bit cell.
- Write clock bits at the leading edge of the bit cell if:
  1) There is no data bit or clock bit written in the previous bit cell, and
  2) There will be not data bit written in the present bit cell.

NOTE: In M²FM/MFM, the write oscillator frequency is doubled, while maintaining the same flux changes per inch as FM. Thus, the bit cell in M²FM/MFM is ½ that in FM. Data transfer rate is also doubled, since a 1 to 1 relationship exists between flux changes per inch and bits per inch (2 to 1 in FM).

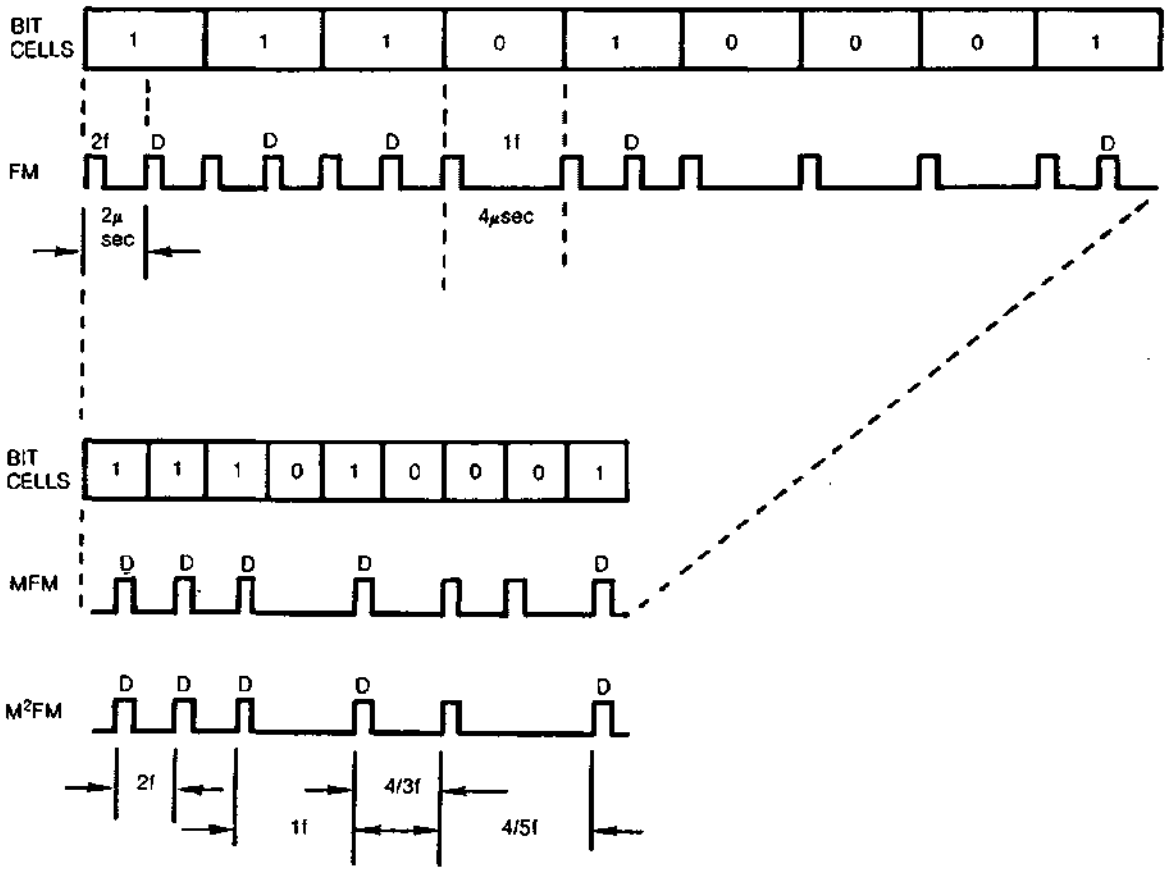


FIGURE 7. FM, MFM AND M²FM ENCODING

1.2.4 TRACKS

The SA850/851 drive is capable of recording up to 154 tracks of data. The tracks are numbered 0-76 for each side. Each track is made available to the read/write heads by accessing the head with a stepper motor and carriage assembly and selecting the desired side of the diskette. Track accessing will be covered in Section 3.

Basic Track Characteristics:

No. Data bits/track Single Density	41,300 bits
No. Data bits/track Double Density	82,600 bits
Index Pulse Width	1.8 ± .6 ms
Index/Sector Pulse Width (SA851 only)	.4 ± .2 ms

1.2.5 TRACK FORMAT

Tracks may be formatted in numerous ways and is dependent on the using system. The SA850/851 use index and sector recording formats respectively.

1.2.5.1 SECTOR RECORDING FORMAT

In this Format, the using system may record up to 32 sectors (records) per track. Each track is started by a physical index pulse and each sector is started by a physical sector pulse. This type of recording is called hard sectoring. Figure 8 shows a typical Sector Recording Format for 1 of 32 sectors.

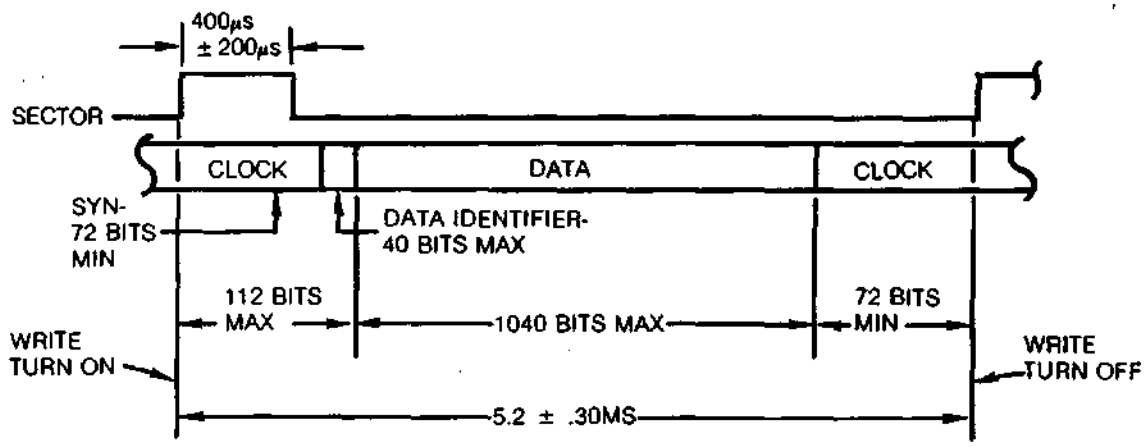


FIGURE 8. SA801 SECTOR RECORDING FORMAT

1.2.5.2 SOFT SECTOR RECORDING FORMAT

In this Format, the using system may record one long record or several smaller records. Each track is started by a physical index pulse and then each record is preceded by a unique recorded identifier. This type of recording is called soft sectoring.

1.2.6 TYPICAL TRACK INDEX FORMAT

Figure 9 shows a track Format, which is IBM compatible, using index Recording Format with soft sectoring.

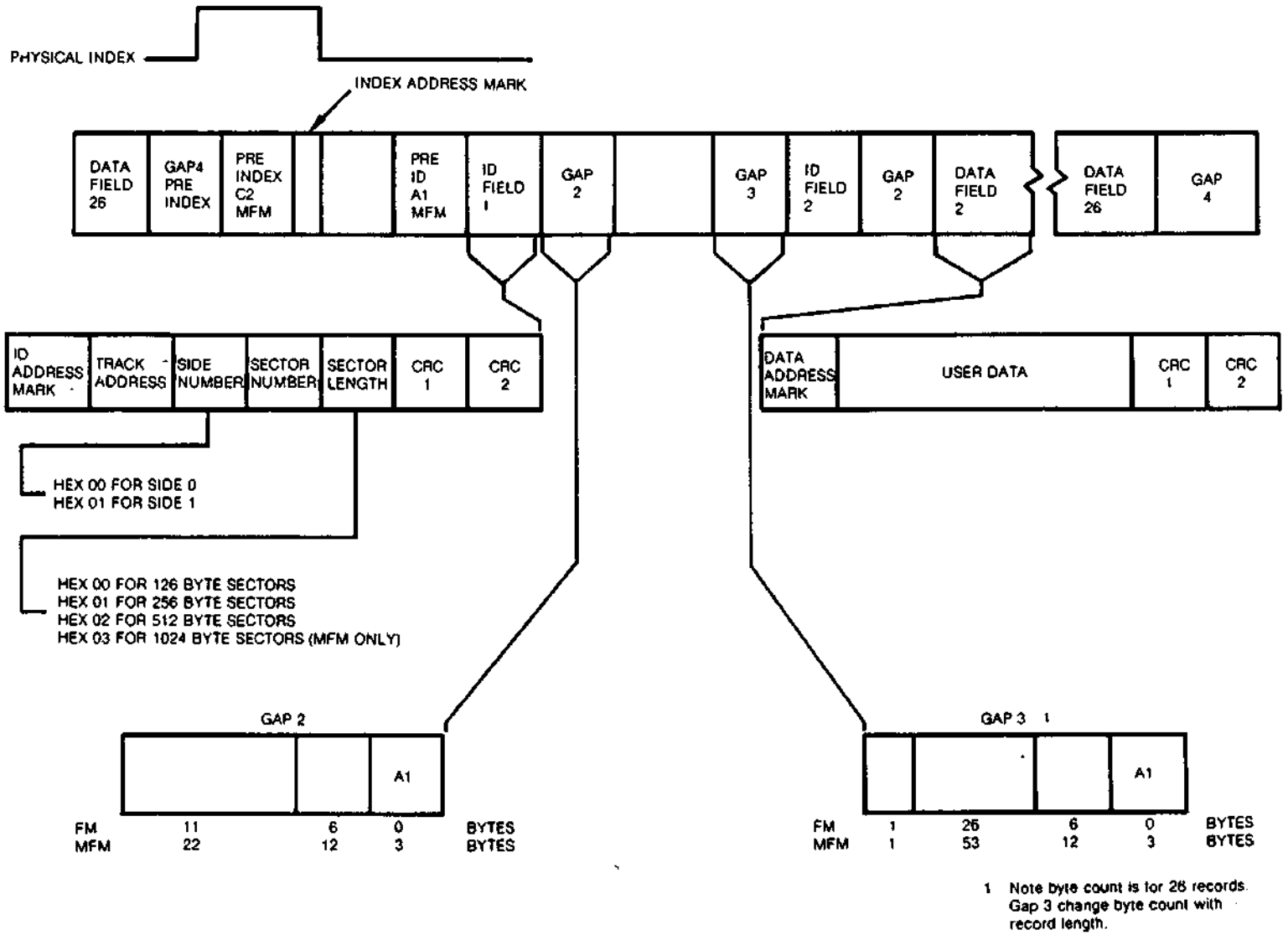


FIGURE 9. TRACK FORMAT

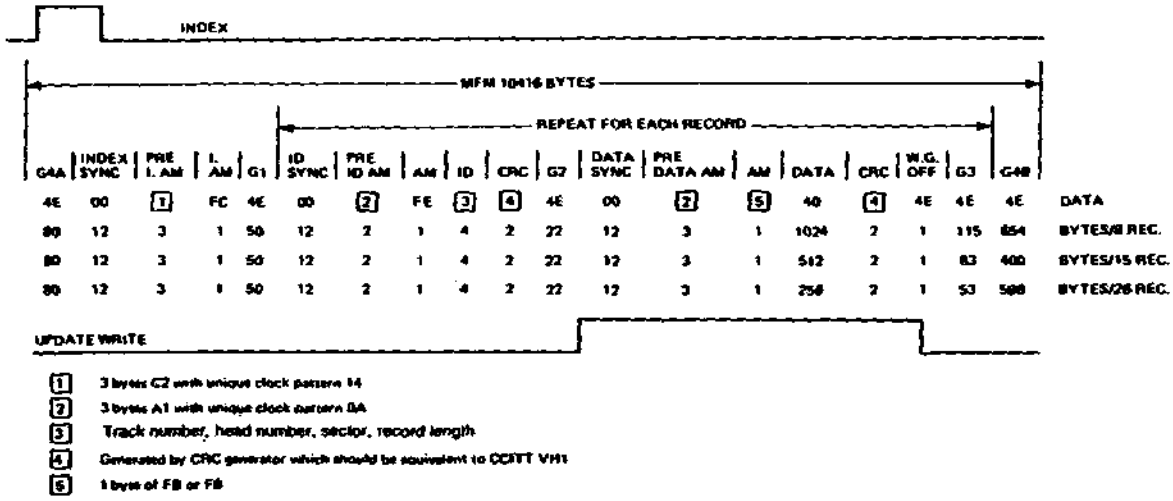


FIGURE 10. MFM TRACK FORMAT COMPARISON

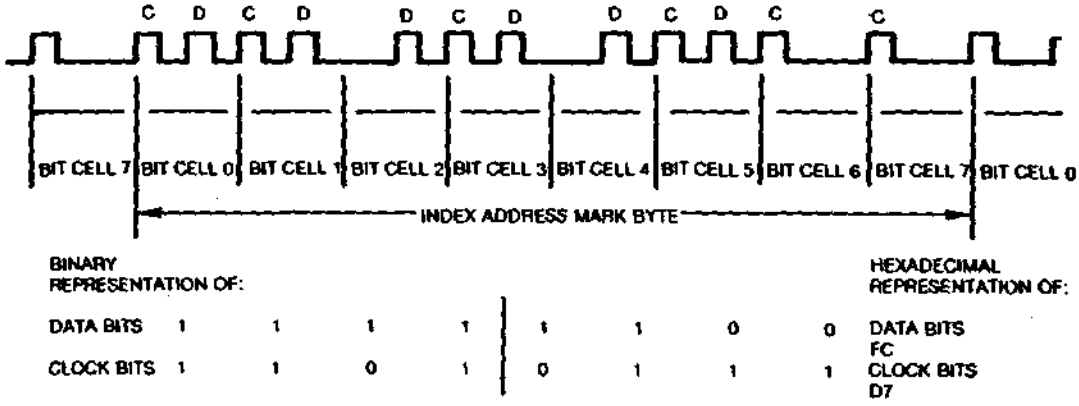
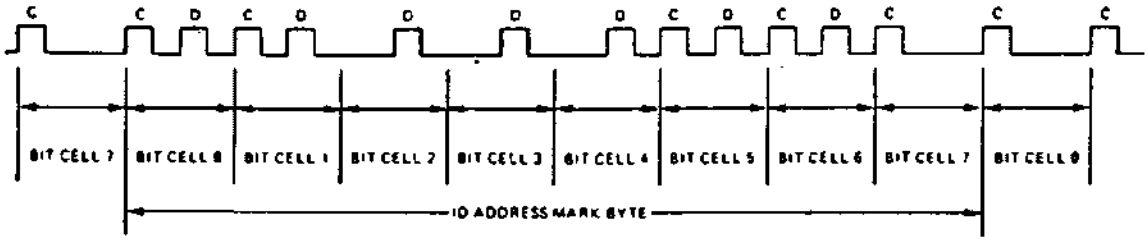
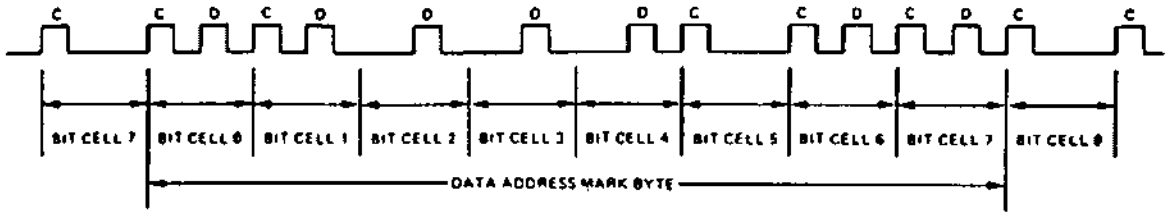


FIGURE 11. INDEX ADDRESS MARK FM



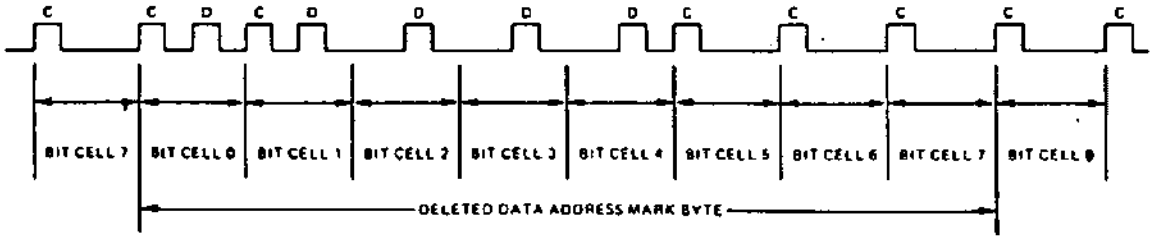
BINARY REPRESENTATION OF:									HEXADECIMAL REPRESENTATION OF:
DATA BITS	1	1	1	1	1	1	1	0	DATA BITS FE
CLOCK BITS	1	1	0	0	0	1	1	1	CLOCK BITS C7

FIGURE 12. ID ADDRESS MARK FM



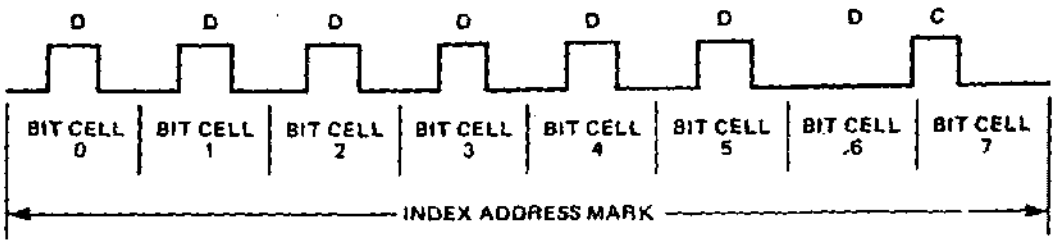
BINARY REPRESENTATION OF:									HEXADECIMAL REPRESENTATION OF:
DATA BITS	1	1	1	1	1	0	1	1	DATA BITS FB
CLOCK BITS	1	1	0	0	0	1	1	1	CLOCK BITS C7

FIGURE 13. DATA ADDRESS MARK FM



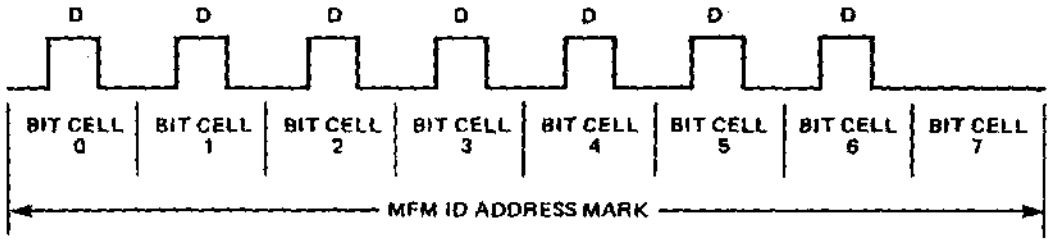
BINARY REPRESENTATION OF:									HEXADECIMAL REPRESENTATION OF:
DATA BITS	1	1	1	1	1	0	0	0	DATA BITS F8
CLOCK BITS	1	1	0	0	0	1	1	1	CLOCK BITS C7

FIGURE 14. DELETED DATA ADDRESS MARK FM



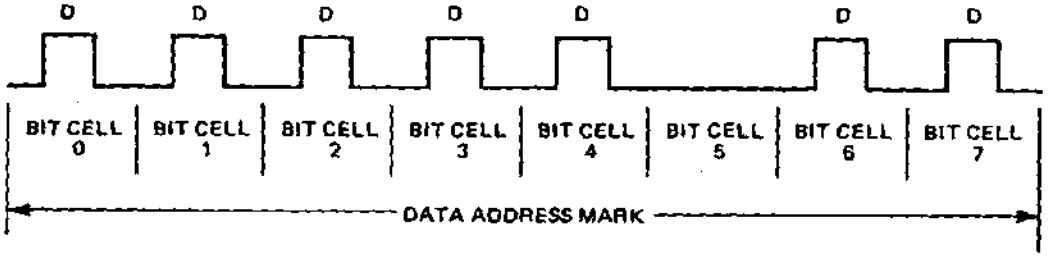
BINARY REPRESENTATION OF:									HEXADECIMAL REPRESENTATION OF:
DATA BITS	1	1	1	1	1	1	1	0	FC
CLOCK BITS			0	0	0			1	01

FIGURE 15. MFM INDEX ADDRESS MARK



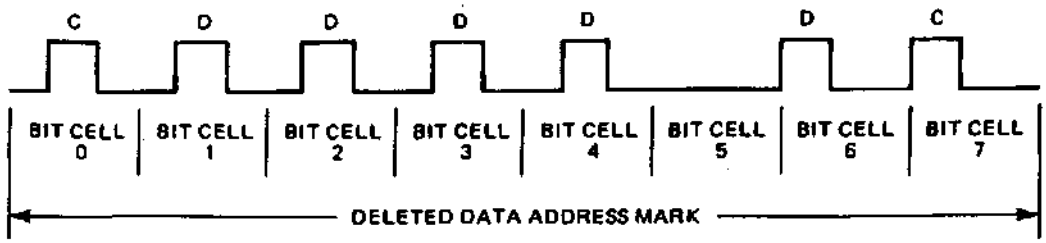
BINARY REPRESENTATION OF:									HEXADECIMAL REPRESENTATION OF:
DATA BITS	1	1	1	1	1	1	1	0	FE
CLOCK BITS	0	0	0	0	0	0	0	0	00

FIGURE 16. MFM ID ADDRESS MARK



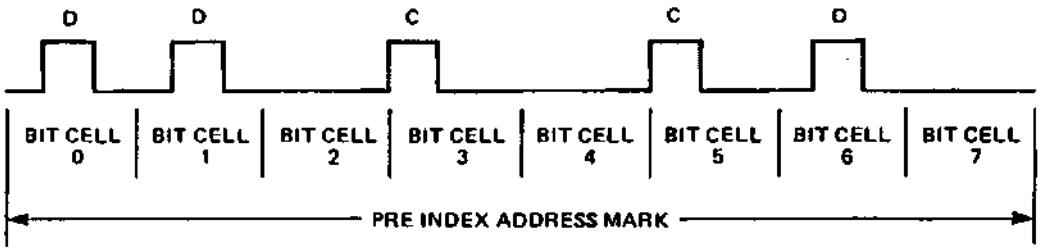
BINARY REPRESENTATION OF:									HEXIDECIMAL REPRESENTATION OF:
DATA BITS	1	1	1	1	1	0	1	1	FB
CLOCK BITS	0	0	0	0	0	0	0	0	00

FIGURE 17. MFM DATA ADDRESS MARK



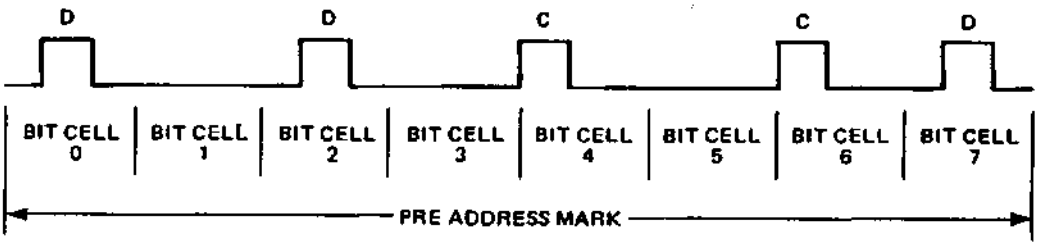
BINARY REPRESENTATION OF:									HEXIDECIMAL REPRESENTATION OF:
DATA BITS	1	1	1	1	1	0	0	0	F8
CLOCK BITS	0	0	0	0	0	0	1	1	03

FIGURE 18. MFM DELETED DATA ADDRESS MARK



BINARY REPRESENTATION OF:									HEXIDECIMAL REPRESENTATION OF:
DATA BITS	1	1	0	0	0	0	1	0	C2
CLOCK BITS	0	0	0	1	0	1	0	0	14

FIGURE 19. MFM INDEX PRE ADDRESS MARK



BINARY REPRESENTATION OF:									HEXIDECIMAL REPRESENTATION OF:
DATA BITS	1	0	1	0	0	0	0	1	A1
CLOCK BITS	0	0	0	0	1	0	1	0	0A

FIGURE 20. MFM PRE ID/DATA ADDRESS MARK

1.2.6.1 Index is the physical detector indicating one revolution of the media and is used to initiate formal operations, generate the Ready signal in the storage device, insure one complete revolution of the media has been searched, and for a deselect storage device signal after a certain number of revolutions.

Gap 1- **G4A** is from the physical index address mark sync and allows for physical index variation, speed variation and interchange between Storage Devices.

Sync is a fixed number of bytes for Separator synchronization prior to the address mark. It includes a minimum of two bytes plus worst case Separator sync up requirements.

Index Pre Address Mark (MFM) - Three bytes of C2 with unique clock bits not written per the encode rules. Refer to Figure 19.

Index Address Mark (FM) - is a unique byte to identify the index field and is not written per the encode rules. Refer to Figure 11.

Index Address Mark (MFM) - is one byte of FC and it is written per the encode rules. Refer to Figure 15.

G1 is from index address mark to ID field address mark sync.

ID Field - **Sync** is a fixed number of bytes for Separator synchronization prior to AM. Includes a minimum of two bytes plus worst case Separator sync up requirements.

ID Pre Address Mark (MFM) - Three bytes of A1 with unique clock bits not written per the encode rules. Refer to Figure 19.

ID Address Mark (FM) - is a unique byte to identify the ID field and not written per the encode rules. Refer to Figure 12.

ID Address Mark (MFM) - is one byte of FE and it is written per the encode rules. Refer to Figure 16.

ID - is a four byte address containing track number, head number, record number, and record length.

CRC - is two bytes for cyclic redundancy check.

Gap 2 - **Gap** from IDCRC to data AM sync and allows for speed variation, oscillator variation and erase core clearance of IDCRC bytes prior to write gate turn on for an update write.

Data Field - **Sync** is a fixed number of bytes for Separator synchronization prior to the AM. Includes a minimum of two bytes plus worst case separator sync up requirements.

Pre Data Address Mark (MFM) - Three bytes of A1 with unique clock bits not written per the encode rules. Refer to Figure 20.

Data Address Mark (FM) - is a unique byte to identify the Data Field and it is not written per the encode rules. Refer to Figure 13.

Data Address Mark (MFM) - is one byte of FB or F8 and it is written per the encode rules. Refer to Figure 18.

Data - is the area for user data.

CRC - is two bytes for cyclic redundancy check.

WG OFF (Write Gate Off) - is one byte to allow for the Write Gate turn off after an update write.

Gap 3 - Gap from WG OFF to next ID AM sync and allows for the erase core to clear the Data Field CRC bytes, speed and write oscillator variation, read preamplifier recovery time and system turn around time to read the following ID Field.

Gap 4 - **G4B** is the last gap prior to physical index and allows for speed and write oscillator variation during a format write and physical index variation.

1.3.0 TRACK ACCESSING

- Carriage Actuator Motor
- Actuator Control Logic
- Reverse Seek
- Forward Seek
- Track 00 Flag

1.3.1 Seeking the read/write heads from one track to another is accomplished by selecting the desired direction utilizing the Direction Select interface line, loading the read/write heads, and then pulsing the Step line. Multiple track accessing is accomplished by repeated pulsing of the Step line until the desired track has been reached. Each pulse on the Step line will cause the read/write heads to move one track either in or out depending on the Direction Select line.

1.3.2 The Carriage Actuator Motor used on the SA850/851 is a four phase, 3.6 degree, permanent magnet stepper motor.

1.3.2.1 There are four stator poles with four teeth per pole extending axially the length of the rotor. The rotor contains 25 teeth per half, spaced 14.4 degrees apart, with each being displaced one tooth pitch relative to each other. The rotor is permanently magnetized with one gear (half) being the north pole and the other the south pole. The four winding per phase are those which when energized will magnetize the poles causing the rotor to move ¼ of a gear tooth pitch or 1 step.

1.3.3 ACTUATOR CONTROL LOGIC (FIGURE 21)

1.3.3.1 POWER ON RESET

The Step Counter (FF A and FF B) is a modified Gray Code counter that counts 0, 1, 3 and 2. At power on, the Step Counter is reset causing the not outputs to be active. When the door is closed and the heads loaded the not outputs actuate the 1 and 4 drivers. With these drivers active the position zero windings are excited causing the rotor to align as shown in Figure 22. (Note, depending on the previous state of the stator windings, the heads may move up to two tracks).

1.3.3.2 FORWARD SEEK

- Seek forward five tracks.
- Assuming:
  Present position of the read/write heads to be track 00.

  Direct Select at a minus level (from the host system).

  Write Gate inactive.

  Five Step pulses to be received (from the host system).

  Step Counter reset (drivers 1 and 4 active).

Minus Direction Select is inverted and becomes + Direction Select. Since the Step Counter is reset (low), a high is at one input of Exclusive OR A and a low at Exclusive OR B. + Direction Select is high and inverts both signals present at Exclusive OR's A and B, causing the input to FFB to be high.

When the first Step pulse is sent to the control logic, it is anded with -Read Gate and then clocks FF A off and FF B on. this enables drivers 1 and 3 causing the Actuator Motor to move 3.6° in a clockwise direction, which in turn moves the carriage assembly one track towards the center of the diskette. Figure 21 (Track 01, Count 1).

With FF A off and FF B on, a low is presented to Exclusive OR A A and B allowing + Direction Select to pass to both FFS. Upon receipt of the next Step pulse both FFS are clocked on, enabling drivers 2 and 3. Figure 22 (Track 02, Count 3).

With both FFS on, a low is at Exclusive OR A and a high at Exclusive OR B which presents + Direction Select to FF A. The next Step pulse clocks FF A on and FF B off enabling drivers 2 and 4. Figure 25 (Track 03, Count 2).

This process is continued until the host system stops sending step pulses at Track 05. At that time FF A is off and FF B on enabling drivers 1 and 3. Figure 23 (Count 1).

1.3.3.3 REVERSE SEEK

- Seek in a reverse direction five tracks.
- Assuming:
  Present position of the read/write heads to be track 05. Direction Select at a positive level (from the host system).

  Write Gate inactive.

  Five step pulses to be received.

  FF A is off and FF B is on, drivers 1 and 3 active.

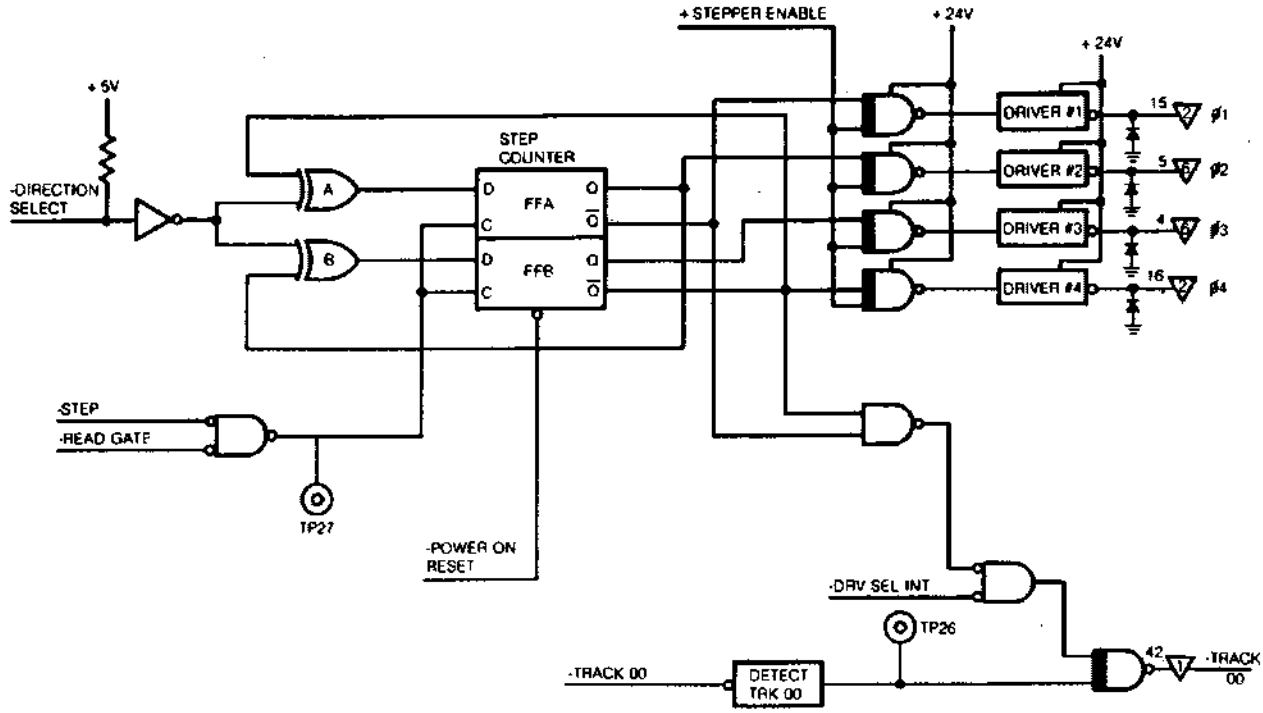
Plus Direction Select is inverted and becomes -Direction Select. With FF A off and FF B on lows are presented to Exclusive ORs A and B. With the first step pulse the FFS are clocked off enabling the 1 and 4 drivers causing the actuator motor to move 3.6 degrees in a counter-clockwise direction, moving the carriage one track towards the outside of the diskette. Figure 22 (Track 04, Count 0).

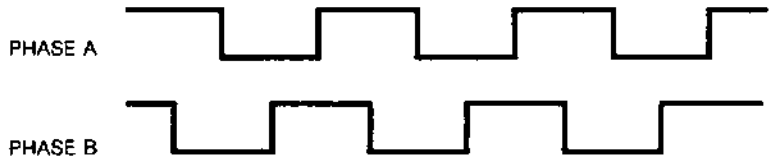
With both FFS off a high is presented to Exclusive OR A and a low to Exclusive OR B. the next Step pulse clocks FF A on and FF B off enabling drivers 2 and 4. Figure 25 (Track 03, Count 2).

This process continues until the fifth Step pulse. With lows at the Exclusive ORs, and FF's are clocked off enabling drivers 1 and 4. Figure 21 (Track 00, Count 0).

1.3.4 TRACK ZERO INDICATOR

Track 00 Pin 42 is provided to the host system to indicate the read/write heads are at track zero. The Track Zero Flag on the carriage assembly is adjusted so that the flag covers the photo transistor at track one. When FF A and B are clocked off the actuator moves to track zero, the Q outputs and Drive Select Internal are anded together and then ANDed with the Track Zero detect to send the Track Zero indication to the host system. (Figure 21)





TRACK	00	01	02	03	04	05	06	07	08	09	10	11
STEP COUNT	0	1	3	2	0	1	3	2	0	1	3	2

FIGURE 21. ACTIVATOR CONTROL LOGIC

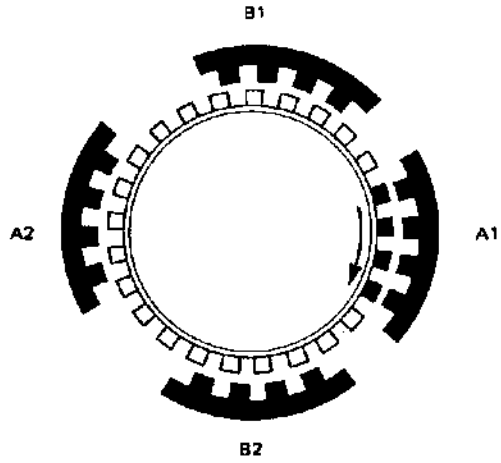


FIGURE 22. COUNT 0

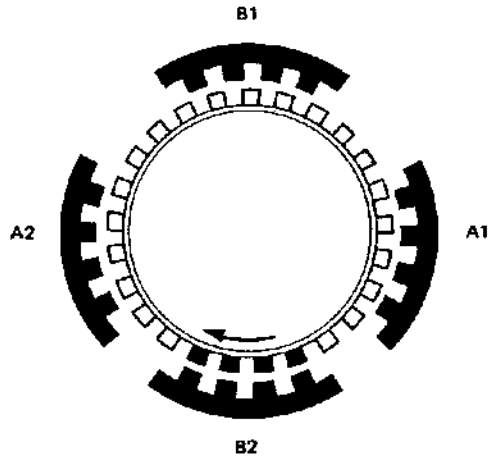


FIGURE 23. COUNT 1

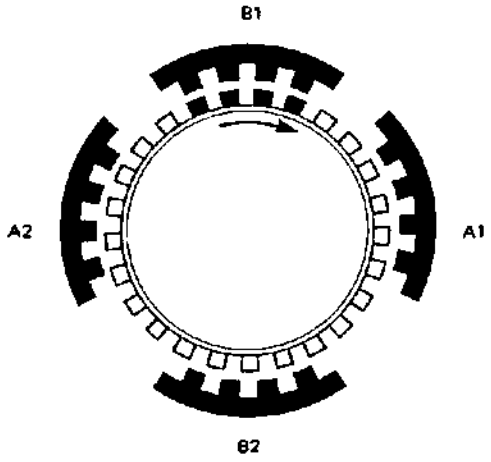


FIGURE 24. COUNT 2

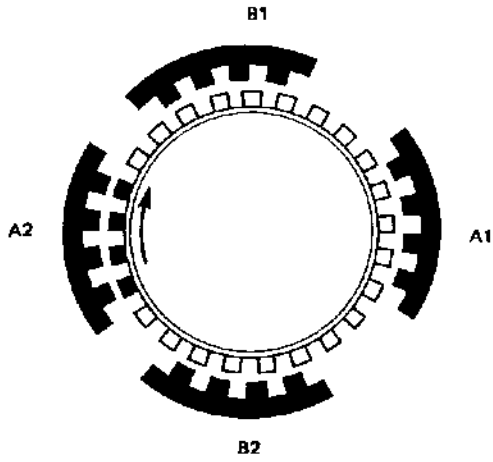


FIGURE 25. COUNT 3

1.4.0 READ-WRITE OPERATIONS

- SA850/851 uses double frequency NRZI recording method.
- The read/write heads are similar to a ring with a gap and a coil wound at some point on the ring.
- During a write operation, a bit is recorded when the flux direction in the ring is reversed by rapidly reversing the current in the coil.
- During a read operation, a bit is read when the flux direction in the ring is reversed as a result of a flux reversal on the diskette surface.

1.4.1 The SA850/851 drive uses the double-frequency (2F) horizontal non return to zero (NRZI) method of recording. Double frequency is the term given to the recording system that inserts a clock bit at the beginning of each bit cell time thereby doubling the frequency of recorded bits. This clock bit, as well as the data bit, are provided by the using system. See Figure 26.

1.4.2 The read/write heads are similar to a ring with a gap and a coil wound some point on the ring. When current flows through the coil, the flux induced in the ring fringes at the gap. As the diskette recording surface passes by the gap, the fringe flux magnetizes the surface in a horizontal direction. See Figure 27.

1.4.3 During a write operation, a bit is recorded when the flux direction in the ring is reversed by rapidly reversing the current coil. The fringe flux is reversed in the gap and hence the portion of the flux flowing through the oxide recording surface is reversed. If the flux reversal is instantaneous in comparison to the motion of the diskette, it can be seen that the portion of the diskette surface that just passed under the gap is magnetized in one direction while the portion under the gap is magnetized in the opposite direction. This flux reversal represents a bit. See Figure 28.

1.4.4 During a read operation, a bit is read when the flux direction in the ring is reversed as a result of a flux reversal on the diskette surface. The gap first passes over an area that is magnetized in one direction, and a constant flux flows through the ring coil. The coil registers no output voltage at this point. When a flux transition passes under the gap, the flux flowing through the ring and coil will make a 180° reversal. This means that the flux reversal in the coil will cause a voltage output pulse. See Figure 29.

1.4.5 Figure 30 shows the 1F and 2F recording flux transitions with pulse relationship.

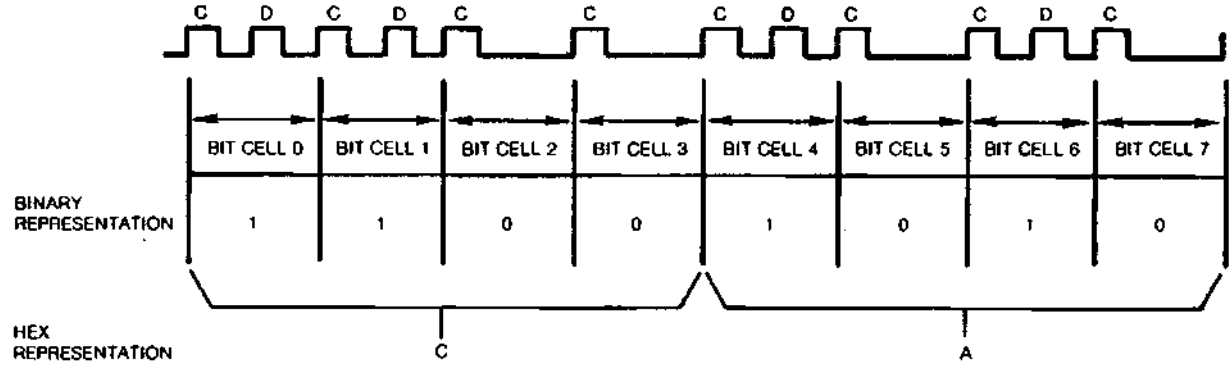


FIGURE 26. BYTE

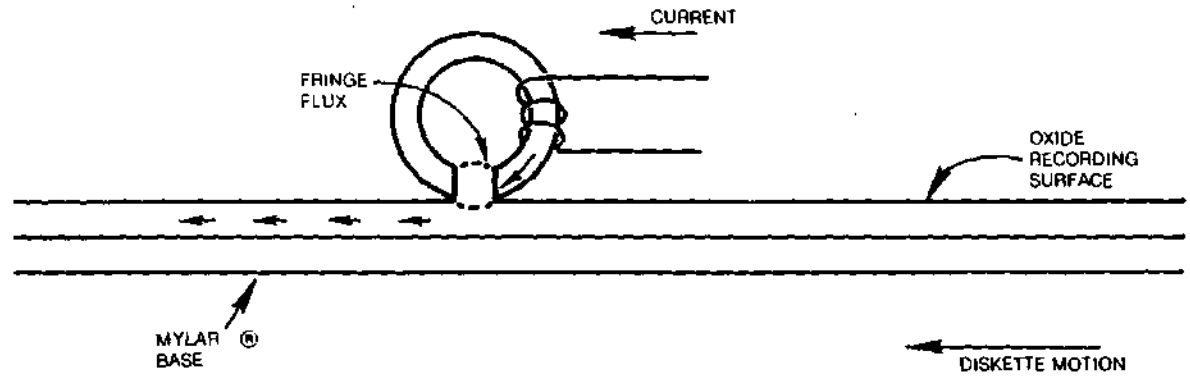


FIGURE 27. BASIC R/W HEAD

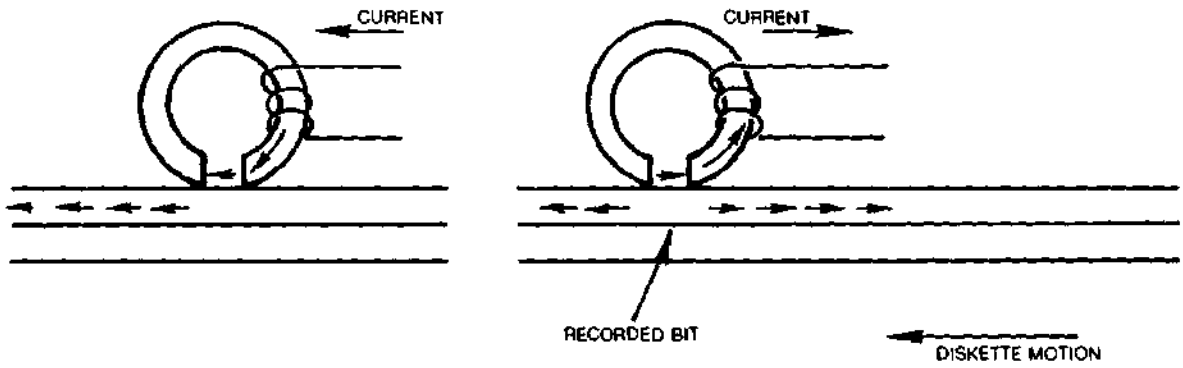


FIGURE 28. RECORDED BIT

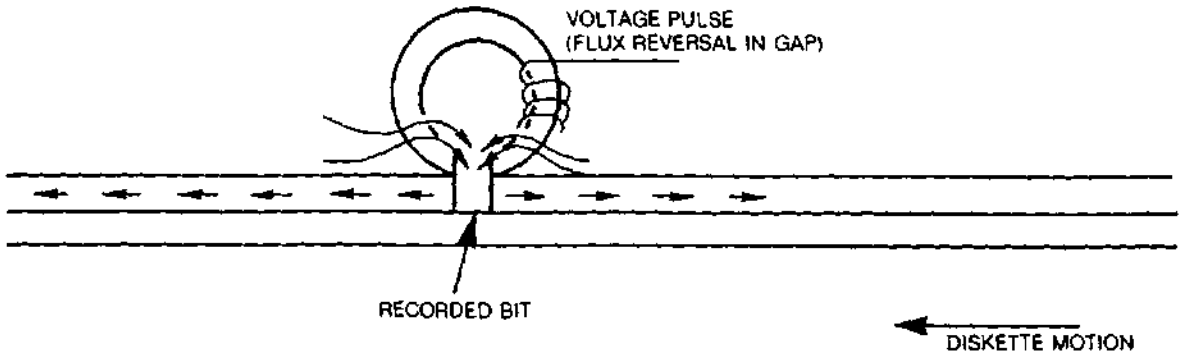


FIGURE 29. READING A BIT

1.5.0 READ/WRITE HEAD

- The read/write heads contain two coils each.
- When writing, the head erases the outer edges of the track to insure there is erased areas between adjacent tracks.

1.5.1 Each of the read/write heads contain two coils. Two read/write coils are wound on a single core, center tapped and one erase coil is wound on a yoke that spans the track being written. The read/write and erase coils are connected as shown in Figure 31.

1.5.2 On a write operation, the erase coil is energized. This causes the outer edges of the track to be trim erased so as the track being recorded will not exceed the .012" track width. The trim erasing allows for minor deviations in read/write head current so as one track is recorded, it will not "splash over" to adjacent tracks.

1.5.3 Each bit written will be directed to alternate read/write coils, thus causing a change in the direction of current flow through the read/write head. This will cause a change in the flux pattern for each bit. The current through either of the read/write coils will cause the old data to be erased as new data is recorded.

1.5.4 On a read operation, as the direction of flux changes on the diskette surface as it passes under the gap, current will be induced into one of the windings of the read/write head. This will result in a voltage output pulse. When the next data bit passes under the gap, another flux change in the recording surface takes place. This will cause current to be induced in the other coil causing another voltage output pulse.

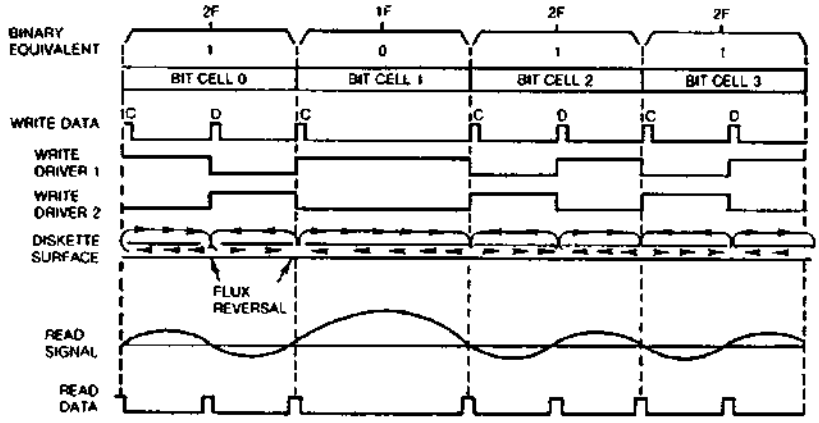


FIGURE 30. 1F AND 2F RECORDING FLUX AND PULSE RELATIONSHIP

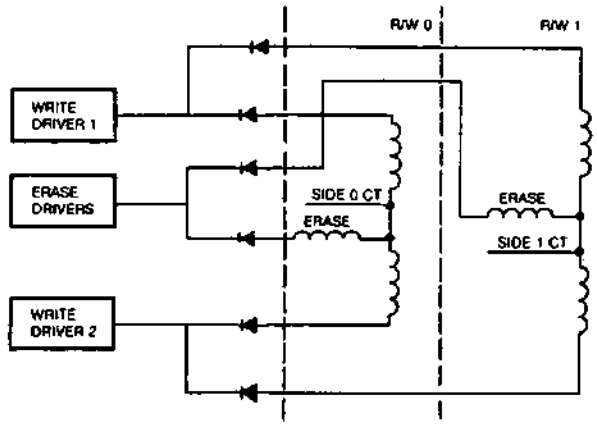


FIGURE 31. READ/WRITE HEADS

1.6.0 WRITE CIRCUIT OPERATION (FIGURE 32)

- The binary connected Write Data Trigger toggles with each pulse on the Write Data line.
- The Write Data Trigger alternately drives one or the other of the Write Drivers.
- Write Gate allows write current to flow to the Write Driver circuits.
- Write Current sensed allows Erase Coil current.
- Heads are selected by grounding the appropriate center tap.

1.6.1 Write data pulses (clock & data bits) are supplied by the using system. The Write Trigger "toggles" with each pulse. The Q and $\overline{Q}$ outputs are fed to alternate Write Drivers.

1.6.2 Write Gate, from using system, and not Write Protect, are anded together to provide write current.

1.6.3 The output of one of the Write Drivers allows write current to flow through one-half of the read/write coil of each head. When the Write Data Trigger toggles, the other Write Driver provides the write current to the other half one the read/write coils.

1.6.4 When write current is sensed flowing to the Write Drivers, a signal is generated to provide trimmer erase coil current.

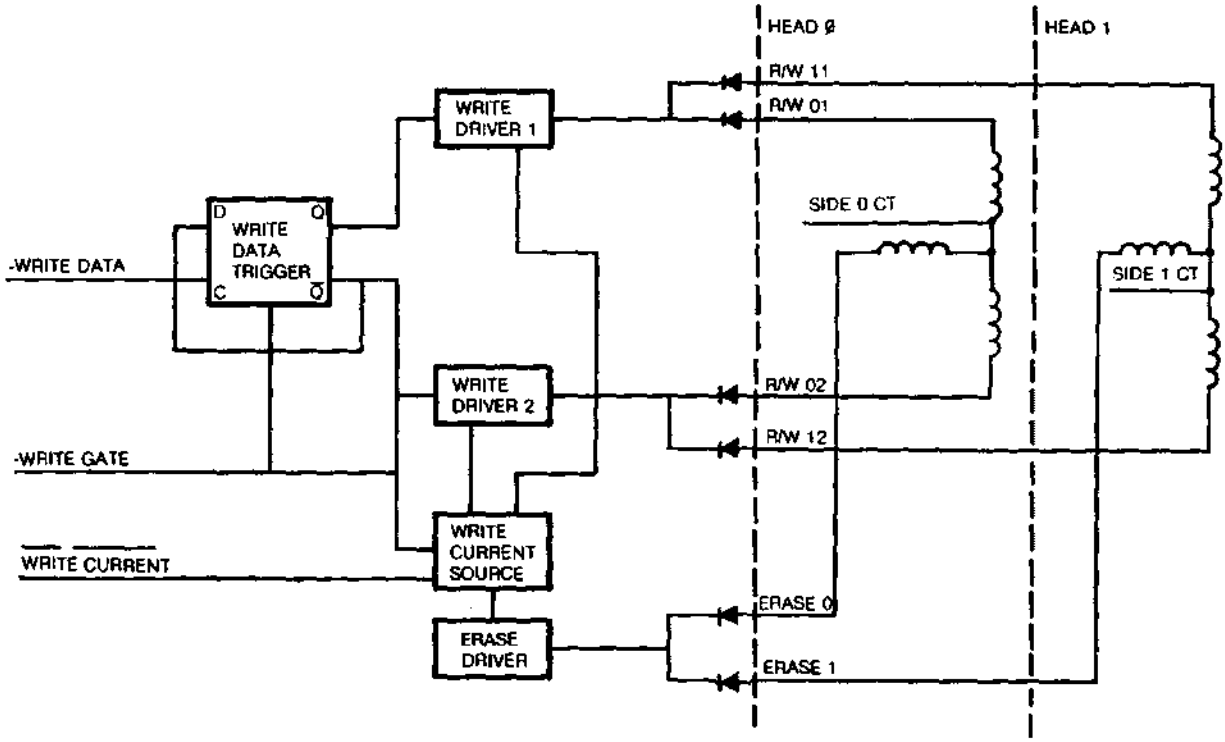


FIGURE 32. WRITE CIRCUIT FUNCTIONAL DIAGRAM

1.7.0 READ CIRCUIT OPERATION (FIGURE 33)

- Duration of all read operations is under control of the using system.
- When the heads are loaded, the read signal amplitude becomes active and is fed to the amplifier.
- As long as the heads are loaded and write gate is not active, the read signal is amplified and shaped, the square wave signals are sent to the host system.
- The data separator separates the read data into clock pulses and data pulses (SA851 only).

1.7.1 When the using system requires data from the diskette drive, the using system must first load the heads and select the side. With loading of the heads and write gate being inactive, the read signal is fed to the amplifier section of the read circuit. After amplification, the read signal is fed to a filter where noise spikes are removed. The read signal is then fed to the differential amplifier.

1.7.2 Since a pulse occurs at least once every 4μs and when data bits are present once every 2μs, the frequency of the read data varies. The read signal amplitude decreases as the frequency increases. Note the signals on Figure 31. The differential amplifier will amplify the read signals to even levels and make square waves out of the read signals (sine waves).

1.7.3 The data separator (SA851 only) is a single time constant separator, that is, the clock and data pulses must fall within pre-specified time frames or windows (single density only).

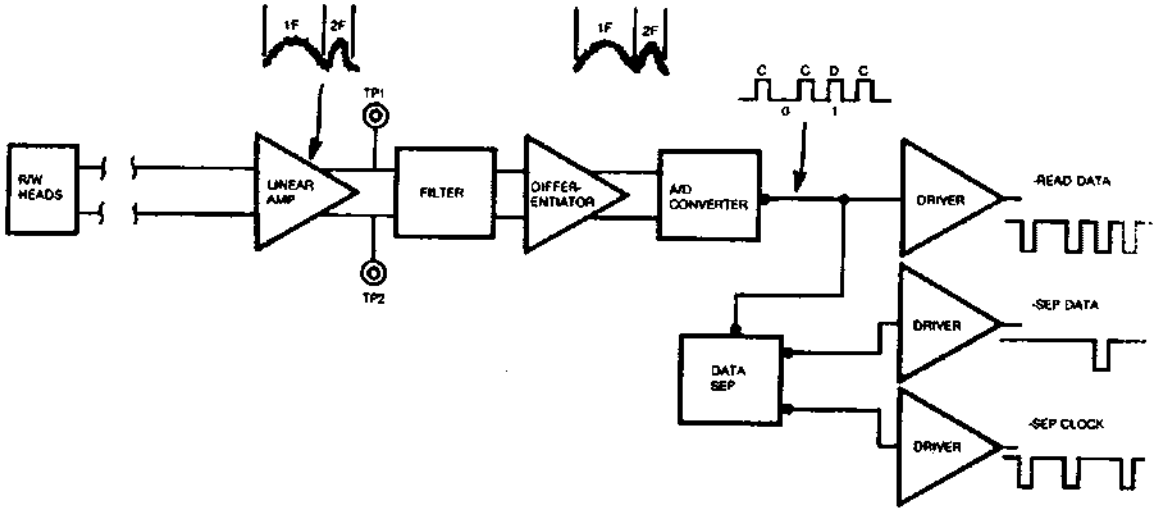


FIGURE 33. READ CIRCUIT FUNCTIONAL DIAGRAM

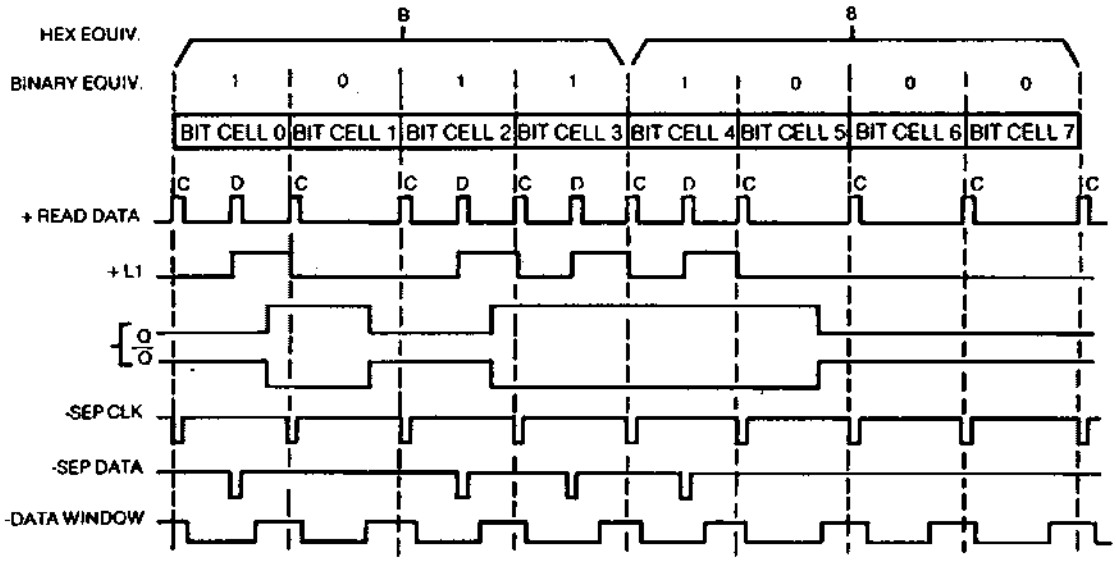


FIGURE 34. DATA SEPARATION TIMING DIAGRAM

1.8.0 INTERFACE

The Electrical interface between the SA850/851 drive and the host system is via three connectors. The first connector, J1, provides the signal interface; the second connector, J5, provides the DC power; and the third connector, J4, provides the AC power and frame ground.

1.8.1 J1/P1 CONNECTOR

Connection to J1 is through a 50 pin PCB edge card connector. The pins are numbered 1 through 50 with the even numbered pins on the component side of the PCB and the odd numbered pins on the non-component side. Pin 2 is located on the end of the PCB connector closest to the AC motor capacitor and is labeled 2. A key slot is provided between pins 4 and 6 for optional connector keying. Refer to Figure 35.

1.8.2 AC POWER (REFER TO TABLE 1)

The AC power to the drive is via the connector P4/J4 located to the rear of the drive and below the AC motor capacitor. The P4/J4 pin designations are outlined in Table 1 for standard as well as optional AC power.

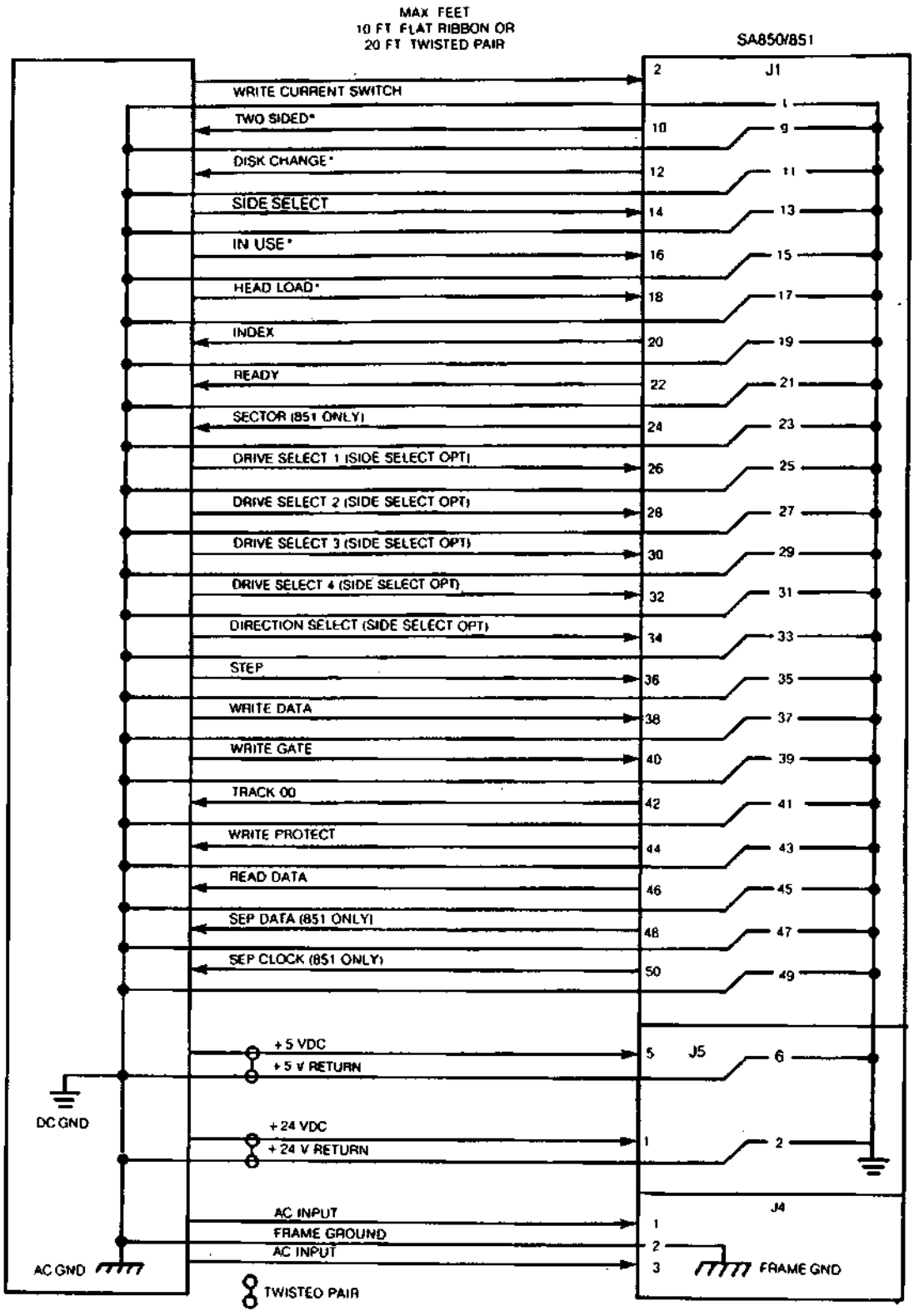
1.8.3 DC POWER (REFER TO TABLE 2)

DC power to the drive is via connector P5/J5 located on the non-component side of the PCB near the P4 connector. The two DC voltages and their specifications along with their P5/J5 pin designators, are outlined in Table 2.

1.8.4 OUTPUT LINES

There are five standard output lines from the SA850, and eight standard output lines from the SA851. Also, there are two optional output lines and eight alternate outputs available from either the SA850 or SA851. The output signals are driven with an open collector output stage capable of sinking a maximum of 40 ma at a logical zero level or true state with a maximum voltage of 0.4V measured at the driver. When the line driver is in a logical one or false state, the driver is off and the collector current is a maximum of 250 microamperes.

Refer to Figure 36 for the recommended circuit.



* These lines are alternate input/output lines and they are enabled by jumper plugs.
Not shown are pins 4, 6 and 8 which are alternate I/O pins.

FIGURE 35. INTERFACE CONNECTIONS

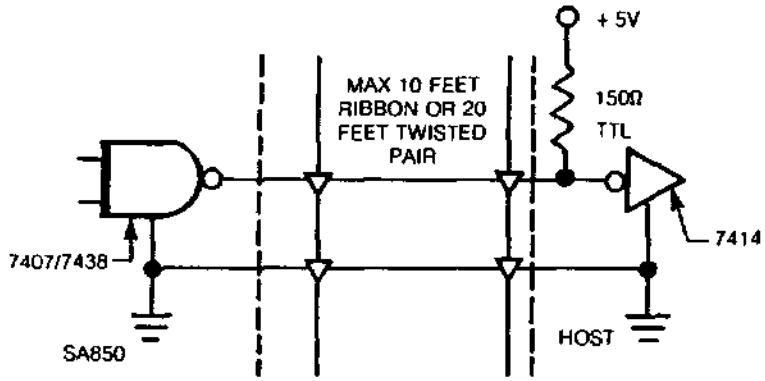


FIGURE 36. INTERFACE SIGNAL DRIVER/RECEIVER

P4 PIN	60 Hz		50 Hz	
	115 V (Standard)	208/230 V	110V	220V
1 2 3	85-127 VAC Frame Gnd 85-127 V Rtn	170-253 VAC Frame Gnd 170-253 V Rtn	85-127 VAC Frame Gnd 85-127 V Rtn	170-253 VAC Frame Gnd 170-253 V Rtn
MAX CURRENT	0.35 Amps	0.25 Amps	0.35 Amps	0.25 Amps
FREQ TOLERANCE	±0.5 Hz		±0.5 Hz	

TABLE I.

P5 PIN	DC VOLTAGE	TOLERANCE	CURRENT	MAX RIPPLE (p to p)
1	+24 VDC	±2.4 VDC	1.0A Max* 0.85A Typ	100 mv
2	+24 V Return			
6	+5 V Return			
5	+5 VDC	±0.25 VDC	1.1A Max 1.0A Typ	50 mv

*If either customer installable option described in sections 7.1 and 7.3 are used, the current requirement for the +24-VDC is a multiple of the maximum +24V current times the number of drives on the line.

TABLE 2

2.0 MAINTENANCE SECTION

2.1.0 MAINTENANCE FEATURES

2.1.1 ALIGNMENT DISKETTE

The SA122 Alignment Diskette is used for alignment of the SA850/851. The following adjustments can be made using the SA122. Adjustments are checked on head zero and head one. The drive under test should be jumpered to the 850 position.

1. R/W Head radial alignment using track 38.
2. Index Photo-Detector Adjustment using tracks 01 and 76.
3. Track 00 is recorded with standard IBM 3740 format.
4. TK 75 has 1f + 2f signal.

NOTE: Caution should be exercised in using the SA122 Alignment Diskette. Tracks 00, 01, 36, 37, 38, 39, 40, 75, and 76 should not be written on. To do so will destroy pre-recorded tracks.

2.1.2 SA809 EXERCISER

The SA809 Exerciser is built on a PCB whose dimensions are 8" × 8". The exerciser PCB can be used in a stand alone mode or it can be built into a test station or used in a tester for field service.

The Exerciser is designed to enable the user to make all adjustments and check outs required on the SA850/851 drives, when used with the SA122 Alignment Diskette.

The exerciser has no intelligent data handling capabilities but can write both 1f and 2f frequencies. The exerciser can enable read in the drive to allow checking of read back signals.

2.1.3 SPECIAL TOOLS

The following specials tools are available for performing maintenance on the SA850/851.

Description	Part Number
Alignment Diskette	SA122
Cartridge Guide Adj. Tool	50377-1
Exerciser	50619-0
Spanner Wrench	50752-0
Head Penetration Tool Set	51218-0

2.2.0 DIAGNOSTIC TECHNIQUES

2.2.1 INTRODUCTION

Incorrect operating procedures, faulty programming, damaged diskettes, and "soft errors" created by airborne contaminants, random electrical noise, and other external causes can produce errors falsely attributed to drive failure or misadjustment.

Unless visual inspection of the drive discloses an obvious misalignment or broken part, attempt to repeat the fault with the original diskette, then attempt to duplicate fault on second diskette.

2.2.2 "SOFT ERROR" DETECTION AND CORRECTION

Soft errors are usually caused by:

1. Airborne contaminants that pass between the read/write head and the disk. Usually these contaminants can be removed by the diskette self-cleaning wiper.

2. Random electrical noise that usually last for a few microseconds.

3. Small defects in the written data and/or track not detected during the write operation that may cause a soft error during a read.

The following procedures are recommended to recover from the above mentioned soft errors:

1. Reread the track ten (10) times or until such time as the data is recovered.

2. If data is not recovered after using step 1, access the head to the adjacent track in the same direction previously moved, then return to the desired track.

3. Repeat Step 1.

4. If data is not recovered, the error is not recoverable.

2.2.3 WRITE ERROR

If an error occurs during a write operation, it will be detected on the next revolution by doing a read operation, commonly called a "write check". To correct the error, another write and write check operation must be done. If the write operation is not successful after ten (10) attempts have been made, a read operation should be attempted on another track to determine if the media or the drive is failing. If the error still persists the diskette should be replaced and the above procedure repeated. If the failure still exists, consider the drive defective. If the failure disappears, consider the original diskette defective and discard it.

2.2.4 READ ERROR

Most errors that occur will be "soft" errors. In these cases, performing an error recovery procedure will recover the data.

2.2.5 SEEK ERROR

1. Actuator malfunction.

To recover from a seek error recalibrate to track 00 and perform another seek to the original track.

2.2.6 TEST POINTS 850/851

1. Read data signal
2. Read data signal
5. Signal ground
6. Signal ground
7. Signal ground
11. + Head load
12. -Index and 851 sector pulses (single sided disk)
13. -Index and 851 sector pulses (double sided disk)
16. + Read data
17. -Data separator timing (long data window)
18. -Data separator timing (short data window)
25. + Write protect
26. + Detect track 00
27. + Gated step pulses
28. Signal ground
I. -Separated index (interface)
R. -Ready (interface)
S. -Separated sector 851 (interface)

2.2.7 CONNECTORS

2.2.7.1 J1/P1 provide the signal interface to the host system. The pin designators are as listed below.

2. Write Current Switch
4. Alternate I/O
6. Alternate I/O
8. Alternate I/O
10. Two Sided (optional)
12. Disk Change (optional)
14. Side Select
16. In Use (optional)
18. Head Load (optional)
20. Index
21. Ready
24. Sector (851 only)
26. Drive Select 1 (or Side Select Option)
28. Drive Select 2 (or Side Select Option)
30. Drive Select 3 (or Side Select Option)
32. Drive Select 4 (or Side Select Option)
34. Direction Select (or Side Select Option)
36. Step
38. Write Data
40. Write Gate
42. Track 00
44. Write Protect
46. Read Data
48. FM Sep Data (851 only)
50. FM Sep Clock (851 only)

NOTE: All odd numbered pins are ground.

2.2.7.2 J2/P2 provide control signals and power to the Head Load Actuator, the Head Position actuator dropping resitors, In Use LED and Door Lock solenoid and the detector assemblies. The pin designators are as listed below:

A. Key
B. +In Use LED
C. +Track 00 LED
D. +Write Protected
E. +Index LED
F. +Door Closed
H. -Door Closed
J. Not used
K. -Door Locked
L. -Track 00
M. +Write Protected
N. +Index/Sector 0 Detector
P. +Index/Sector 1 Detector
R. Key
S. +Stpr Wndg/Res A
T. +Stpr Wndg/Res B
U. -Head Load
1. Key
2. Ground
3. Ground
4. Ground
5. Ground
6. Ground
7. Not Used
8. Not Used
9. +24V Door Lock
10. +5V Track 00 Detector
11. +5V Write Protect
12. +5V Index (0 & 1) Detector
13. Not Used
14. Key
15. +Stpr Res A
16. +Stpr Res B
17. +24V Head Load

2.2.7.3 J3/P3 J3/P3 provides to interface to the Read/Write coils and the trim erase coils of the magnetic recording heads. The pins are listed below:

1. Shield 0
2. Key
3. Read/Write 01
4. Side 0 CT
5. Read/Write 02
6. Erase 0
7. Erase 1
8. Read/Write 12
9. Side 1 CT
10. Read/Write 11
11. Key
12. Shield 1

2.2.7.4 J4/P4 provide AC power and ground as listed below:

1. -AC Motor Power A
2. -Frame Ground
3. AC Motor Power B

2.2.7.5 J5/P5 J5/P5 provide DC power and ground as listed below:

1. +24 Volts DC
2. +24 Volt Ground Return
3. Not Used
4. Not Used
5. +5 Volts DC
6. +5 Volts Ground Return

2.2.7.6 J6/P6 J6/P6 provide power to the Head Positioning actuator as listed below:

1. +Stpr Wndg/Res B
2. Key
3. +Stpr Wndg/Res A
4. +Stpr Wndg B
5. +Stpr Wndg A

2.3.0 PREVENTATIVE MAINTENANCE

2.3.1 INTRODUCTION

The prime objective of any preventive maintenance activity is to provide maximum machine availability to the user. Every preventative maintenance operation should assist in realizing this objective. Unless a preventive maintenance operation cuts machine downtime, it is unnecessary.

Visual inspection is the first step in every scheduled maintenance operation. Always look for corrosion, dirt, wear, binds, and loose connections. Noticing these items during PM may save downtime later.

Remember, do not do more than recommended preventative maintenance on equipment that is operating satisfactorily.

2.3.2 PREVENTIVE MAINTENANCE PROCEUDRES

Details of preventative maintenance operations are listed in Table 3. During normal perventative maintenance, perform only those operations listed on the chart for that preventive maintenance period. Observe all safety procedures.

UNIT	FREQ. MONTHS	CLEAN	OBSERVE
Read/Write Heads	N/A	No maintenance required	Do not touch or clean
Actuator band, capstan and shaft	12	Clean all oil, dust, and dirt only if necessary	
Belt	12		Frayed or weakened areas
Base	12	Clean base	Inspect for loose screws connectors, and switches
Read/Write Head	12		Check for proper alignment

TABLE 3

2.3.3 CLEANLINESS

Cleanliness cannot be overemphasized in maintaining the SA850/851. Do not lubricate the SA850/851; oil will allow dust and dirt to accumulate. To prevent damage the read/write heads should not be cleaned or touched.

2.3.4 CAUTIONS

The heads should never touch each other. Whenever removing or installing the heads insure a clean piece of lens tissue is inserted between the heads to prevent them from touching.

a. Never open the cartridge guide access without first unloading the heads from the load bail (Section 2.4.3).

b. Insure the up stop is in proper adjustment so the diskette will clear the heads when it is inserted (Section 4.6.2).

c. Make sure the door lock is functioning properly so as not to remove a diskette while the heads are loaded.

d. The Read/Write heads are factory aligned with a four track offset. Loosening the head mounting screw will destroy the alignment and the actuator assembly will have to be returned to the factory for alignment.

2.4.0 REMOVALS, ADJUSTMENTS

NOTE: Read the entire procedure before attempting a removal and/or adjustment.

2.4.1 MOTOR DRIVE

2.4.1.1 DRIVE MOTOR ASSEMBLY: REMOVAL AND INSTALLATION

a. Extract 3 contacts to disconnect motor from AC connector (J4).

b. Loosen two screws holding capacitor clamp to the base. Remove rubber boot and disconnect motor leads from capacitor.

c. Remove connectors from PCB and remove PCB.

d. Remove belt from drive pulley.

e. Remove 4 screws holding the motor to the base casting and remove motor.

2.4.1.2 MOTOR DRIVE PULLEY

a. Remove connectors from PCB and remove PCB.

b. Remove belt from drive pulley.

c. Loosen set screw and remove pulley.

d. Reverse procedure for installation.

NOTE: When installing a new pulley, the drive pulley must be aligned with the spindle pulley so that the belt tracks correctly.

2.4.2 HEAD COVER SHIELD REMOVAL

a. Loosen the two screws holding cover to the guide opening assembly.

b. Slide cover back toward drive and remove the cover.

2.4.3 CARTRIDGE GUIDE ACCESS

a. Remove head cover shield (Section 2.4.2).

b. Position head to approximately track 00 by turning the actuator shaft.

c. Open cartridge guide by pressing pushbar on front of drive.

d. Insert a clean piece of lens tissue between the heads to prevent them from touching each other and gently lower the moveable head arm assembly.

e. Loosen the two screws holding the cartridge to door latch plate.

CAUTION: Insure the head load arm is off the load bail first.

f. Release safety catch on guide open assembly by pressing it towards the back of the drive.

g. Swing cartridge guide out.

h. To restore the cartridge guide to its normal position reverse the procedure and adjust per Section 2.4.9.2.

2.4.4 SECTOR/INDEX LED ASSEMBLY: REMOVAL AND INSTALLATION

a. Disconnect the wires to LED terminals (solder joints).

b. Remove the screw holding the LED assembly to the cartridge guide.

c. Reverse the procedure for installation.

d. Check index timing and readjust if necessary. Refer to Section 2.4.7.2.

2.4.5 WRITE PROTECT DETECTOR

2.4.5.1 WRITE PROTECT DETECTOR: REMOVAL AND INSTALLATION

a. Remove connectors from PCB and remove PCB.

b. Extract wires from P2 connector, pins 4, D, 11, and M.

c. Remove cable clamps.

d. Remove head cover shield (Section 2.4.2).

e. Remove screw holding the detector bracket and remove assembly.

f. Reverse procedure for reinstalling. Connect the wires to P2 by the following: Red to (4), Black to (D), White to (11), and Gray to (M).

2.4.5.2 WRITE PROTECT DETECTOR ADJUSTMENT

a. Insert a diskette into drive. Write protect notch or hole must be open.

b. Set oscilloscope to AUTO sweep, 2V/div. and monitor TP25.

c. Loosen screw on detector assembly and adjust until maximum amplitude is achieved. Tighten screw. Be sure the detector assembly is not to far forward as to restrict the diskette when it is inserted.

2.4.6 HEAD LOAD MECHANISM ASSEMBLY

2.4.6.1 HEAD LOAD MECHANISM: REMOVAL AND INSTALLATION

a. Install a diskette.

b. Remove head cover shield (section 2.4.2).

c. Extract wires from P2 connector pins 17 and U.

d. Unfasten the four mounting screws and remove the actuator assembly.

e. To install, reverse the above procedure. Reference section 2.4.6.2 to adjust.

f. When installing, make sure that the fasteners for mounting the solenoid body do not interfere with the armature.

2.4.6.2 HEAD LOAD MECHANISM ADJUSTMENT

a. Apply power to the drive and insert a double-sided diskette (SA150). Step to track 00 and select side 1 head.

b. Select the drive and insure the head is loading. With the head loaded a clearance of .020" ± .012" should be obtained between the bail on the head load solenoid and the lift tab on the head arm (see Figure 37). To adjust this clearance turn the screw located on top of the armature (see Figure 37). Clockwise will decrease the clearance and counter-clockwise will increase the clearance.

   Load the head a couples of times and reverify the clearance required.

c. Step to track 76 and load the head, check the clearance between the bail and the lift tab. Lift tab *must* not be in contact with the bail, and clearance must be a minimum of .008" and no greater than .032"

d. Return to track 00.

   (1) Sync oscilloscope on TP 11 (+ Head Load). Set time base to 10 msec/division. Connect one probe to TP1 and the other to TP2. Ground the probes on TP5. Set the inputs to AC couple, add and invert one input. Set the vertical deflection to 200 mv/division.
   (2) Select the side 1 head, energize the head load solenoid and observe the read signal on the oscilloscope. The read signal should begin between 35 and 45 msec (see Figure 38).
   (3) If the read signal begins sooner than 35 msec loosen screw holding the loader spring adjustment plate. Slide plate towards the solenoid body (see Figure 37). If the read signal begins after 50 msec, slide the plate away from the solenoid body.

   **When energizing the head load solenoid do not exceed one per second.*

e. A properly adjusted head load mechanism should load between 35 and 45 msec and the read signal should settle out in 50 msec. There should be no read signal between 0 and 30 msec.

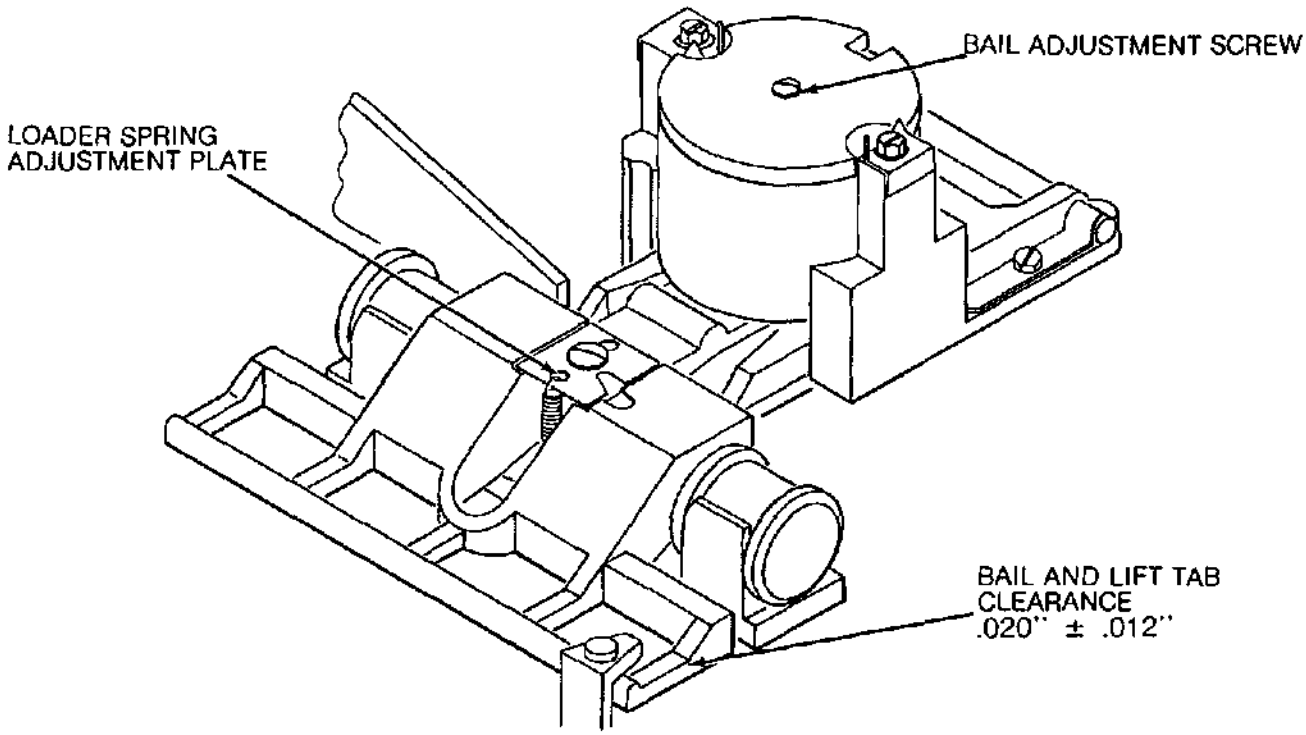


FIGURE 37. HEAD LOAD MECHANISM ADJUSTMENT

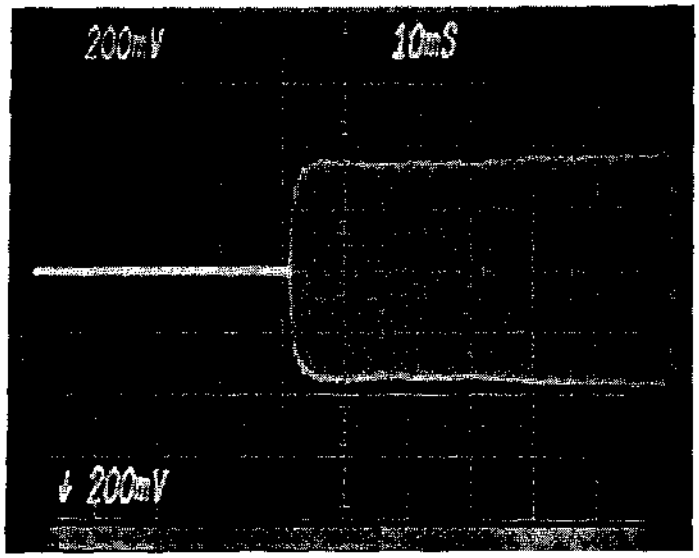


FIGURE 38. HEAD LOAD TIMING

2.4.7 INDEX/SECTOR PHOTO TRANSISTOR ASSEMBLY

2.4.7.1 INDEX/SECTOR PHOTO TRANSISTOR ASSEMBLY: REMOVAL AND INSTALLATION

a. Disconnect P2 connector from PCB.

b. Remove wires from Door Closed switch ORG Common, Grey N/C, and Red N/O. Extract wires from P2 connector Pins 12 BLK, N GREEEN, P BRN, 6 ORG, F GRAY, and H RED.

c. Remove the cable clamp holding wires for detector.

d. Remove screw holding detector to the base plate and remove assembly.

e. To install reverse procedure.

2.4.7.2 INDEX/SECTOR ADJUSTMENT

a. Insert Alignment Diskette (SA122).

b. Step carriage to track 01.

c. Sync oscilloscope, external negative, on TP12 (-Index). Set time base to 50μsec/division.

d. Connect one probe TP1 and the other to TP2. Ground probes to the PCB. Set the inputs to AC. Add and invert one channel. Set vertical deflection to 500MV/division.

e. Observe the timing between the start of the sweep and the first data pulse. This should be 200 ± 100μsec. If the timing is not within tolerance, continue on with the adjustment.

f. Loosen the holding screw in the Index Transducer until the transducer is just able to be moved.

g. Observing the timing, adjust the transducer until the timing is 200 ± 100μsec. Insure that the transducer assembly is against the registration surface on the base casting.

h. Tighten the holding screw.

i. Recheck the timing.

j. Seek to track 76 and reverify that the timing is 200 ± 100μsec.

2.4.8 SPINDLE ASSEMBLY

a. Remove head cover shield (Section 2.4.2).

b. Switch out cartridge guide (Section 2.4.3).

c. Remove drive belt.

d. Remove the nut and 2 spring washers holding the spindle pulley. The Spanner Wrench 50752 must be used to hold spindle.

CAUTION: The pre-loaded rear bearing may fly out when spindle pulley is removed.

e. Withdraw spindle hub from opposite side of baseplate.

f. Reverse the procedure for installation.

g. Tighten nut to 20 in./lbs., insuring that the spring washers are compressed. Add a drop of LOCTITE #290 to the threads.

2.4.8.1 CLAMP HUB REMOVAL

a. Remove hub clamp plate.

b. Remove clamp hub and spring.

c. To install, reverse the procedure. No adjustment necessary.

2.4.9 CARTRIDGE GUIDE

2.4.9.1 CARTRIDGE GUIDE REMOVAL

a. Perform steps, 2.4.3, 2.4.4, 2.4.5 and 2.4.6.1.

b. Loosen cartridge guide stop.

c. Remove E-ring from pivot shaft.

d. Remove pivot shaft.

e. Tilt the cartridge guide slightly, and remove it from the upper pivot.

f. To install the cartridge guide, reverse the procedure.

g. Perform steps 2.4.5.2 and 2.4.5.2.

2.4.9.2 CARTRIDGE GUIDE ADJUSTMENT

a. Insert the shoulder screw (tool P/N 50377-1) through the adjustment hole in the cartridge guide and screw completely into the base casting (hand tight).

b. Move the handle into the latched position and hold lightly against the latch.

c. Tighten two screws holding the cartridge guide to the latch plate.

d. Remove the tool and check to determine if the flange on the clamp hub clears the cartridge guide when the spindle is rotating. If the clamp hub rubs on the cartridge guide, repeat the adjustment procedure.

e. Adjust the cartridge guide stop so that it is within .005 inch of the base casting.

f. Check index alignment (Sector 2.4.7.2).

g. Insert diskette, close and open door, then check for proper operation.

2.4.10 HEAD AMPLITUDE CHECK

These checks are only valid when writing and reading back as described below. If the amplitude is below the minimum specified, before re-writing and re-checking, insure that the diskette is not "worn" or otherwise shows evidence of damage on either side. Insure head load down stop is properly adjusted (Section 2.4.6.2).

a. Install good media.

b. Select the drive and step to TK 76.

c. Sync the oscilloscope on TP12 (-Index) for single sided diskettes, TP13 for double sided diskettes, connect one probe on TP2 and one on TP1, on the drive PCB. Ground the probes to the PCB and invert one input. Set volts per division to 50mv and time base to 20 Msec per division.

d. Write the entire track with 2F signal (all one's).

e. The average minimum read back amplitude peak to peak, should be 130 millivolts for side 0 and 130 millivolts for side 1.

If the output is below minimum and different media is tried and the output is still low, it will be necessary to install a new head and actuator assembly.

2.4.10.1 HEAD ACTUATOR ASSEMBLY: REMOVAL AND INSTALLATION

a. Remove the connectors and the PCB.

b. Remove cable clamp holding R/W head cable on PCB side of drive.

c. Remove the grommet from the cable bracket on head side.

d. Unload heads (Refer to Section 2.4.3, Steps D & E).

e. Remove the two or four screws holding actuator assembly to the base casting.

f. Carefully remove heads and actuator assembly from the drive. Take care as not to snag the heads, load arms, or read/write head cable on the casting.

g. To install, procede as follows:

(1) Hold assembly at a slight angle towards you when installing (approximately 15°CCW viewed from rear).

(2) Rotate actuator into position against the ledge while simultaneously lifting the arm tab with the bail so that the heads are separated and the protective paper between them falls free.

(3) Position the actuator casting firmly and squarely against the ledge on the base casting and secure with two or four screws and washers (install the locating screw nearest the ledge first).

2.4.10.2 HEAD PENETRATION ADJUSTMENT

a. The tools necessary to perform this alignment procedure will consist of penetration gauge tool set, screwdriver and ¼" nut driver (see Figure 39).

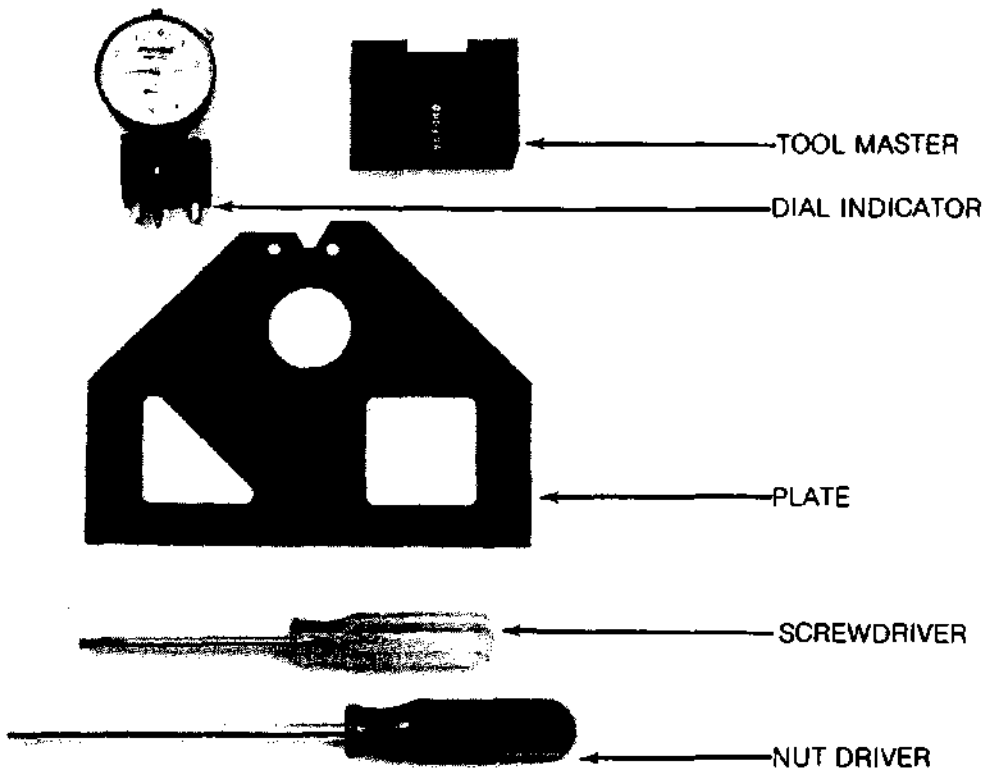


FIGURE 39. HEAD PENETRATION TOOLS

b. Set up the penetration dial indicator on the penetration tool master. Check penetration tool to make sure it's indicating surfaces are clean and properly set; (long hand on zero and small hand on three) while it's resting on the penetration tool master. See Figure 40.

NOTE: When the tool is not being used, it should be kept where it won't be dropped or knocked off the work bench.

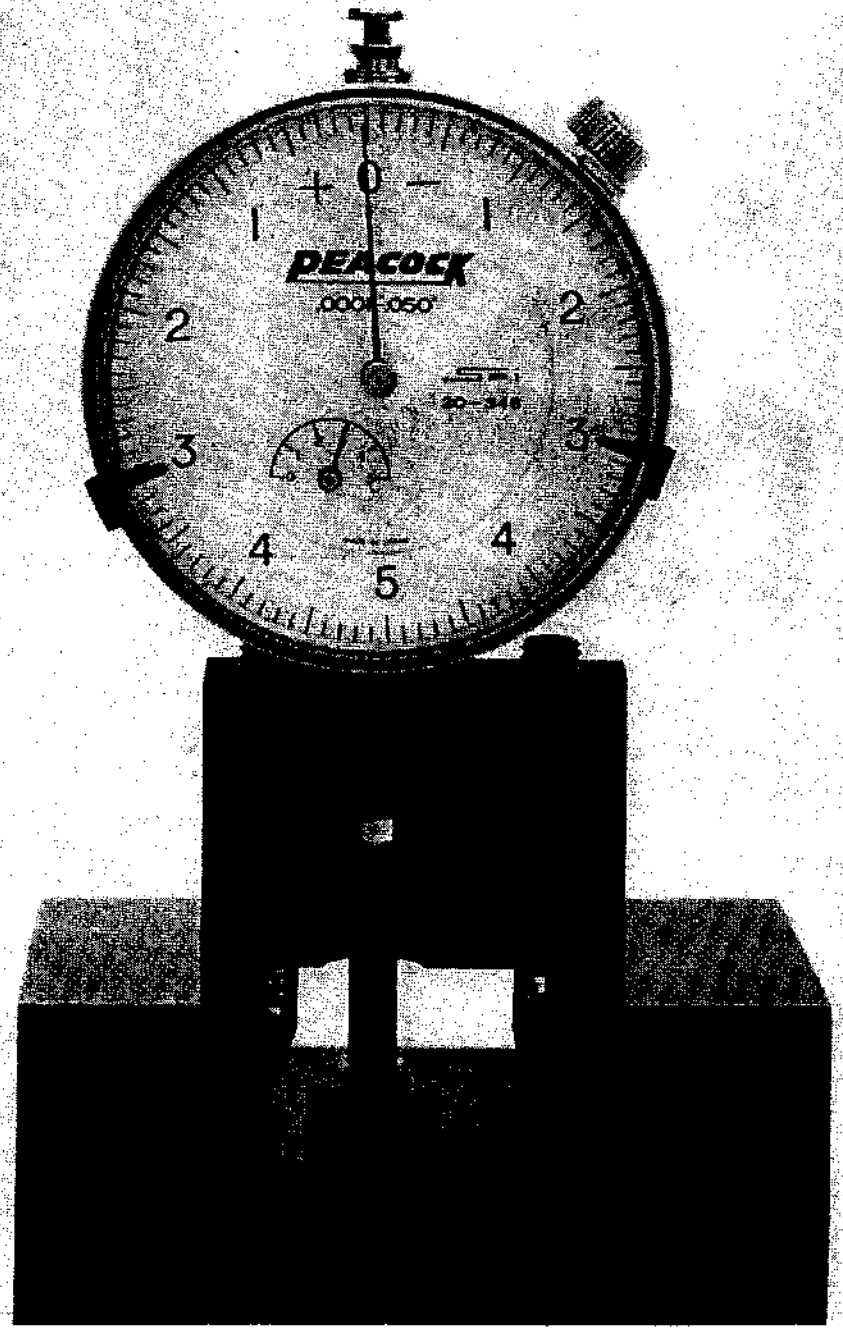


FIGURE 40. DIAL INDICATOR

c. With the drive in the horizlonal position, remove HAC shield and door open, slide the penetration plate into the drive with the tappered end in first and counter bore side up. Slide the plate up and over the spindle until it's squarely over the spindle and close the door. See Figure 41.

NOTE: The penetration plate is made of harden tool steel and care should be used not to damage spindle or any other part of the drive during insertion of extraction.

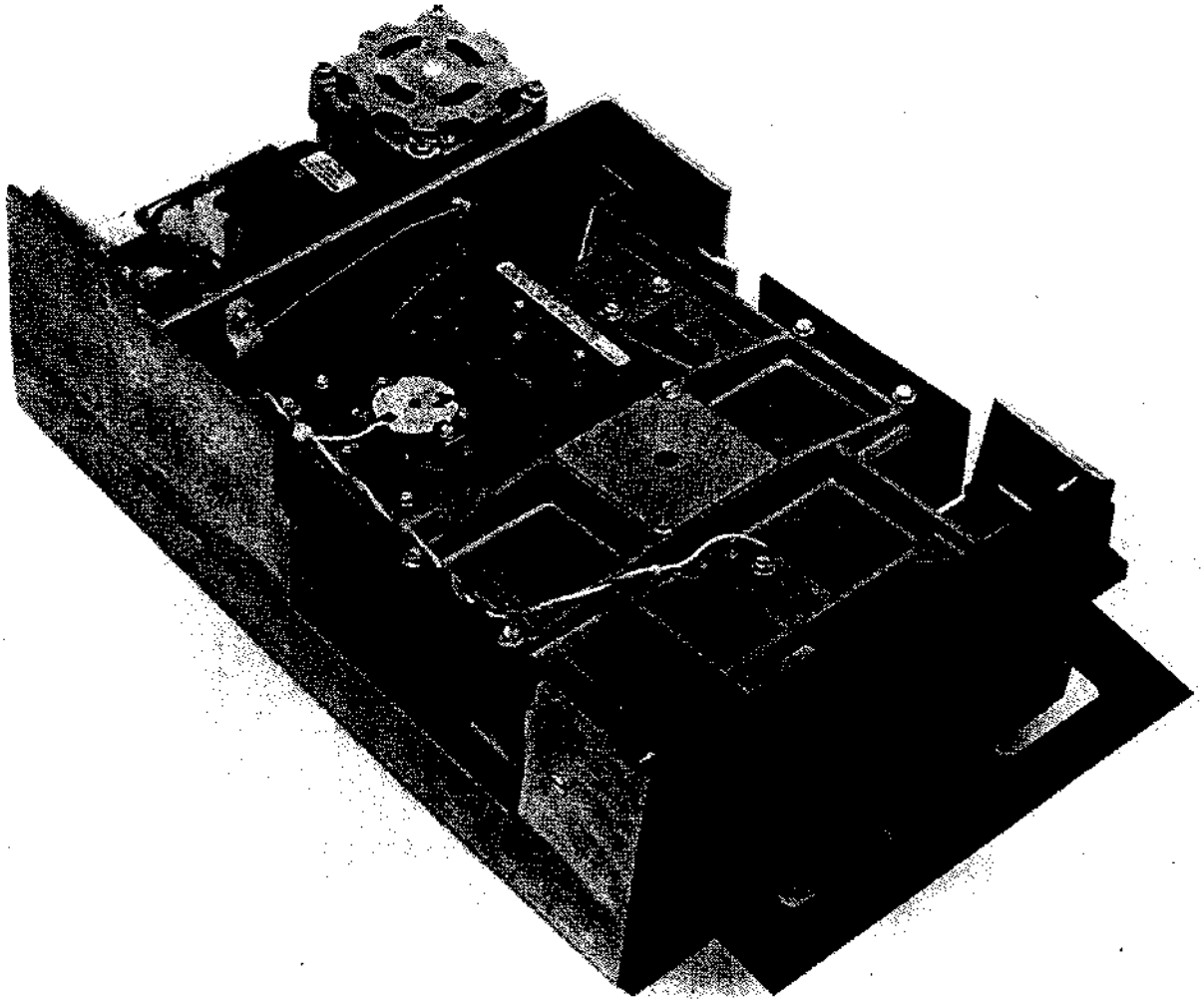


FIGURE 41. PENETRATION PLATE INSTALLATION

d. Next install the indicator block into the penetration plate until you feel the block snap into place. See Figure 42.

NOTE: Make sure all surfaces are clean, the block is squarely and fully snapped onto the plate. Also avoid handling the block by the indicator.

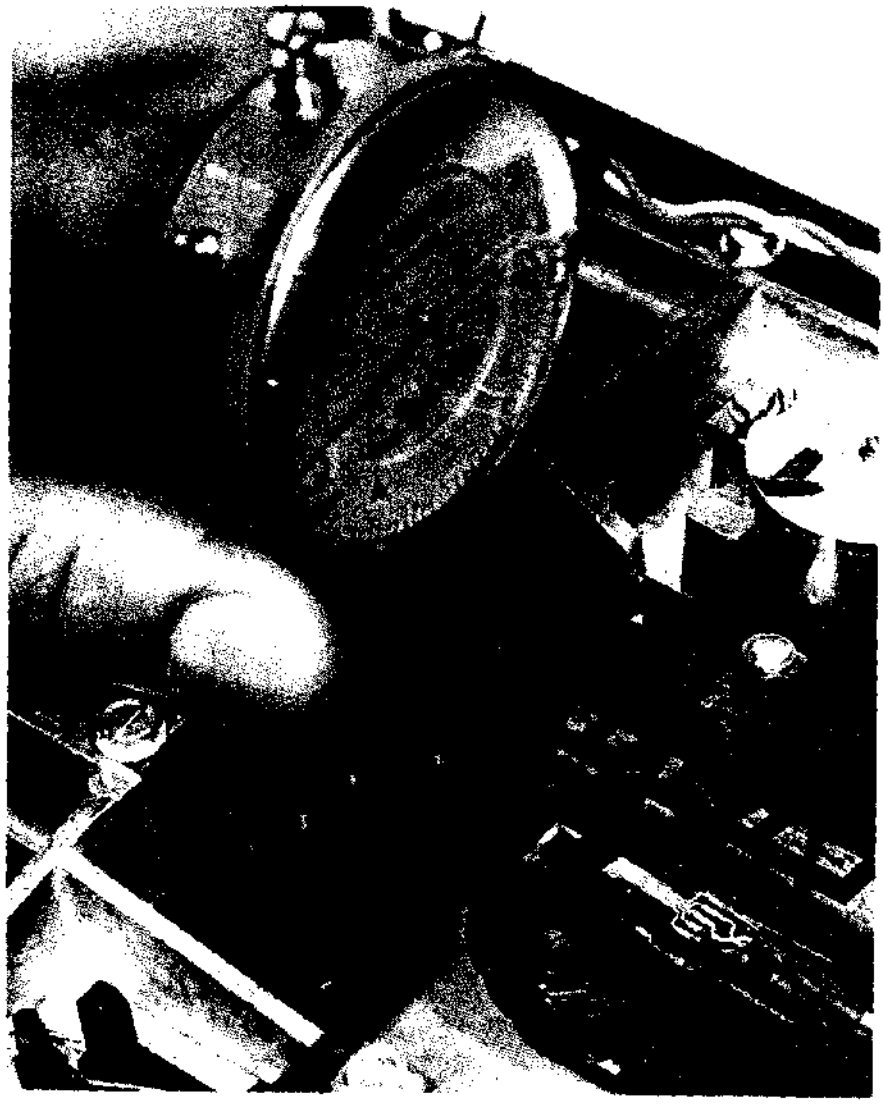


FIGURE 42. DIAL INDICATOR INSTALLATION

e. The shaft the extends from the stepper motor can be used to move the head up far enough so the gauge point is indicating off the tab, on the side zero head as shown in Figure 43.

f. Check the dial indicator for the proper setting. The long hand should be between + 3 and -3 with the short hand pointing at three. If penetration setting is out of this range then continue with procedure starting at step 7. See Figure 44.

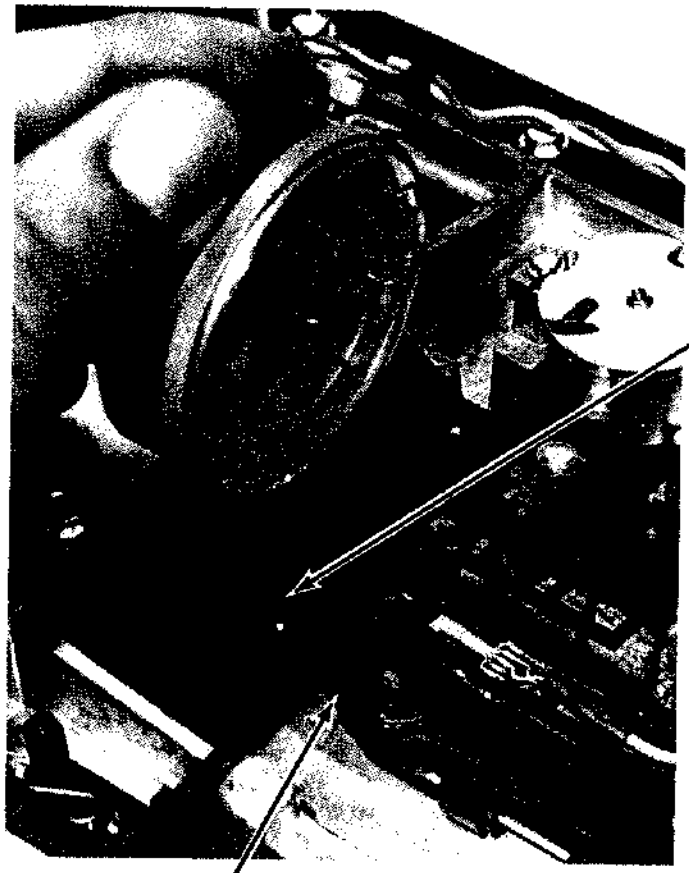


FIGURE 43. INSTALLATION CHECK

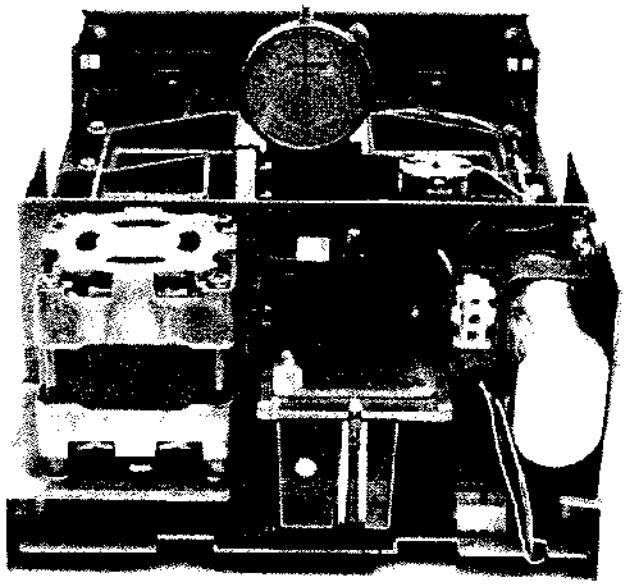


FIGURE 44. CORRECT PENETRATION

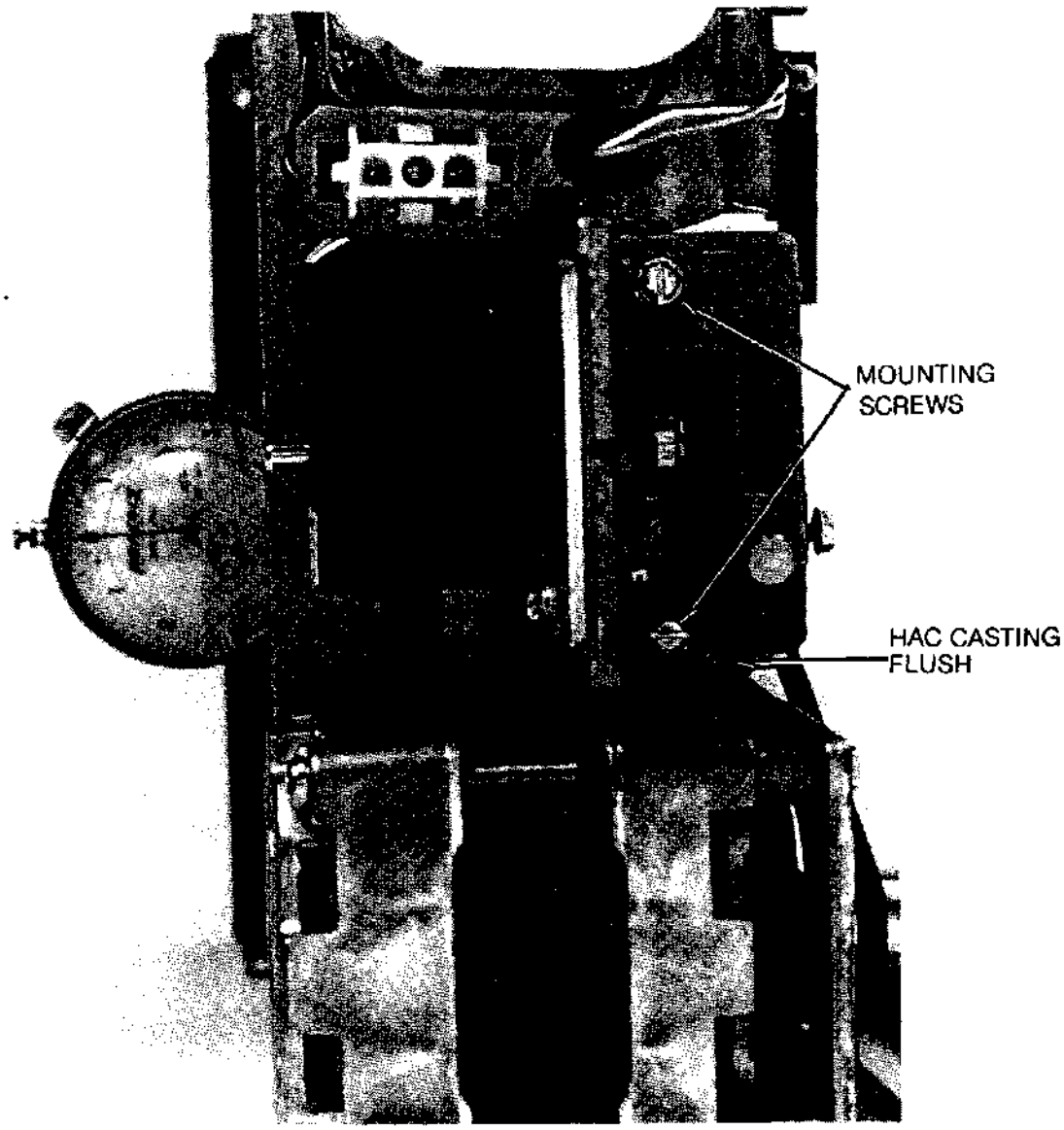


FIGURE 45. PENETRATION ADJUSTMENT

g. With the penetration gauge installed set the drive up in the vertical position, the AC motor should be closest to the bench.

h. Loosen the two or four mounting screws using a ¼" nut driver.

i. Adjust HAC assembly left to right until the reading on the penetration gauge reads; small hand on three and long hand on zero ± .003.

A. If small hand is on the left side of three, the HAC assembly must go to the right.
B. If small hand is on the right side of three, the HAC assembly must go to the left.

j. When penetration is set tighten the two or four mounting screws using a ¼" nut driver.

k. As you tighten the two mounting screws, make sure the HAC casting is flush (making contact) with the machined lip on the base casting.

l. Check penetration gauge again to insure proper alignment. If not return to procedure step 7.

m. Remove the indicator block (remember to handle with care). Open the door and remove the penetration gauge.

n. Replace the HAC shield.

2.4.10.3 HEAD RADIAL ALIGNMENT

NOTE: The actuator assembly is aligned at the factory and adjustment is not normally required after replacing a head and actuator assembly. If after checking and the lobes are within 70% of each other, alignment is not recommended.

a. Insert Alignment Diskette (SA122).

NOTE: Alignment diskette should be at room conditions for at least 1 hour before alignment checks.

b. Steps the heads to track 38.

c. Sync the oscilloscope, external negative, on TP12 (-Index). Set the time base to 20Msec per division. This will display over one revolution.

d. Connect one probe to TP1 and the other to TP2. Ground the probes to the PCB. Set the inputs to AC, Add and invert one channel. Set the vertical deflection to 100MV/division.

e. The amplitude of the two lobes must be within 70% of each other. If the lobes do not fall within this specification continue on with the procedure (Refer to Figure 46).

f. Loosen the two or four mounting screws, which hold the motor plate to the support bracket (Refer to Figure 47).

g. Move the plate, by rotating the eccentric adjusting nut.

h. When the lobes are of an equal amplitude, tighten the motor plate mounting screws (Refer to Figure 47).

i. Check the adjustment by stepping off track and returning. Check in both directions and readjust as required.

j. Whenever the Head Radial Alignment has been adjusted the Track 00 detector adjustment must be checked. (Section 2.4.11.2).

2.4.10.4 READ/WRITE HEADS AZIMUTH CHECK

The azimuth is not field adjustable. If, after performing this check the waveform on the oscilloscope is not within + 18' replace the Head Actuator Assembly.

a. Install Alignment Diskette SA122. Select the drive and step to track 76.

b. Sync the scope external negative on TP12, set time base to .5 MSec per division.

c. Connect one probe to TP1 and the other to TP2. Invert one channel and ground the probes to TP5 & 6. Set the inputs to AC, ADD, and 50 MV per division.

d. Compare waveform to Figure 48. If not within the range shown replace the Head Actuator Assembly 2.4.10.1

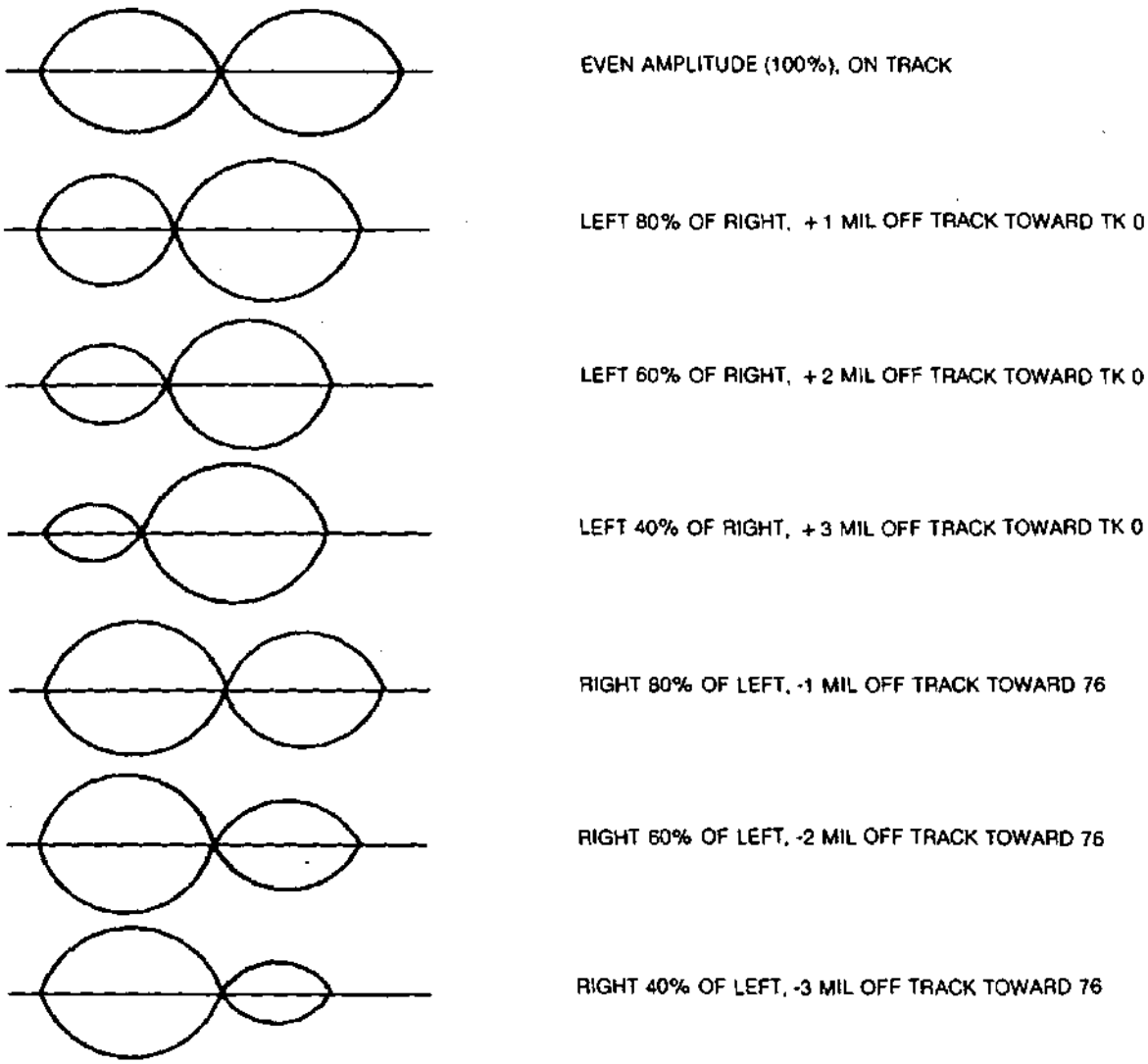


FIGURE 46. HEAD RADIAL ALIGNMENT

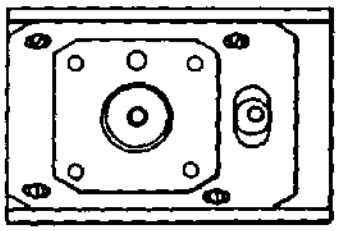


FIGURE 47. MOTOR PLATE

2.4.11 DOOR LOCK SOLENOID AND IN USE LED ASSEMBLY REMOVAL

a. Perform steps 2.4.12a and 2.4.12h.

b. Remove door lock assembly

c. Reverse procedure to install new assembly.

d. Adjust of the door lock should not be necessary. If it has to be, the gap between the armature tab and the latch should be .015 ± .010. This adjustment can be made by loosening the two screws on the armature.

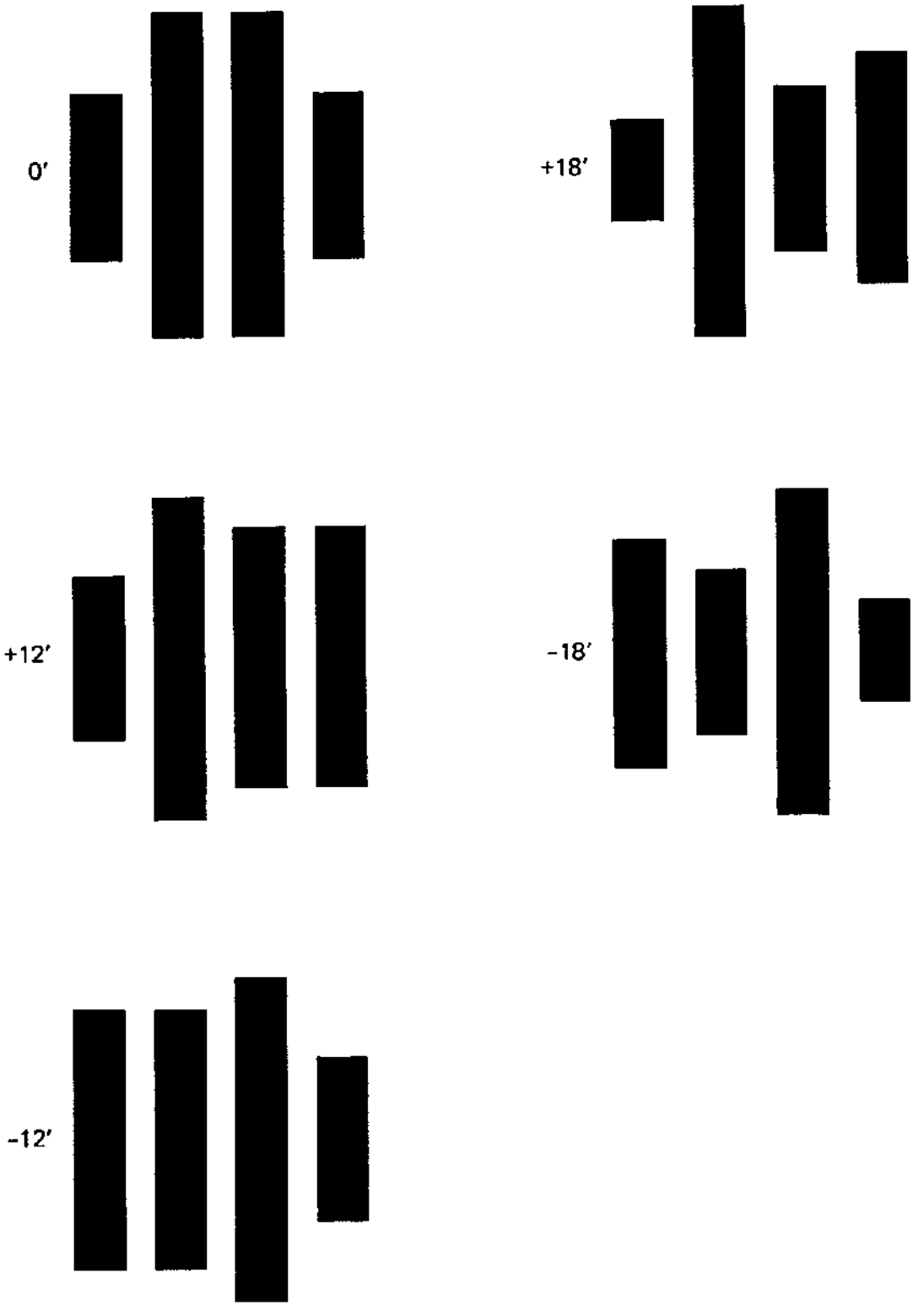


FIGURE 48. AZIMUTH BURST PATTERNS

2.4.12 TRACK 00 DETECTOR: REMOVAL AND INSTALLATION

a. Remove head cover shield (Section 2.4.2).

b. Swing cartridge guide open (Section 2.4.3).

c. Manually rotate stepper shaft and move carriage to track 77.

d. Remove screw holding bracket to base casting and remove bracket and detector.

e. Remove PCB connector and remove PCB.

f. Extract cable from P2 connector; Pin 3 BRN, C BLACK, 10 ORANGE, and L RED.

g. Remove cable clamps and remove Detector assembly.

h. To install, reverse the procedure.

i. Adjust according to Section 2.4.11.2.

2.4.12.1 TRACK 00/76 STOP ADJUSTMENT

a. Not field adjustable.

2.4.12.2 TRACK 00 DETECTOR ASSEMBLY ADJUSTMENT

a. Check head radial alignment and adjust if necessary before making this adjustment.

b. Insert diskette.

c. Connect oscilloscope to TP26. Set vertical deflection of 1v/division and sweep to continuous.

d. Step carriage to track 02. TP26 should go low. Adjust the detector assembly towards the actuator assembly if not low.

e. Check the adjustment by stepping the heads between tracks 00 and 02, observing that TP26 is low at track 02 and high at track 00. A perfect adjustment is if you have a square wave on a scope.

2.4.13 FRONT PLATE ASSEMBLY REMOVAL

a. Insert the cartridge guide adjustment tool (P/N 50377-1) through the adjustment hole in the cartridge guide and screw completely into the base hold casting (hand tight).

b. Remove the door lock wires from P2, Pin 2-black, B-brown, 9-violet and K-blue.

c. Remove the cable clamp holding the door lock wires.

d. Remove the two alien head screws holding the handle to the front plate and remove the handle.

e. Remove the four screws holding the front plate to the base casting.

f. Remove two screws holding door lock assembly to the front plate.

g. Remove two allen head screws holding the In Use LED to the door lock assembly.

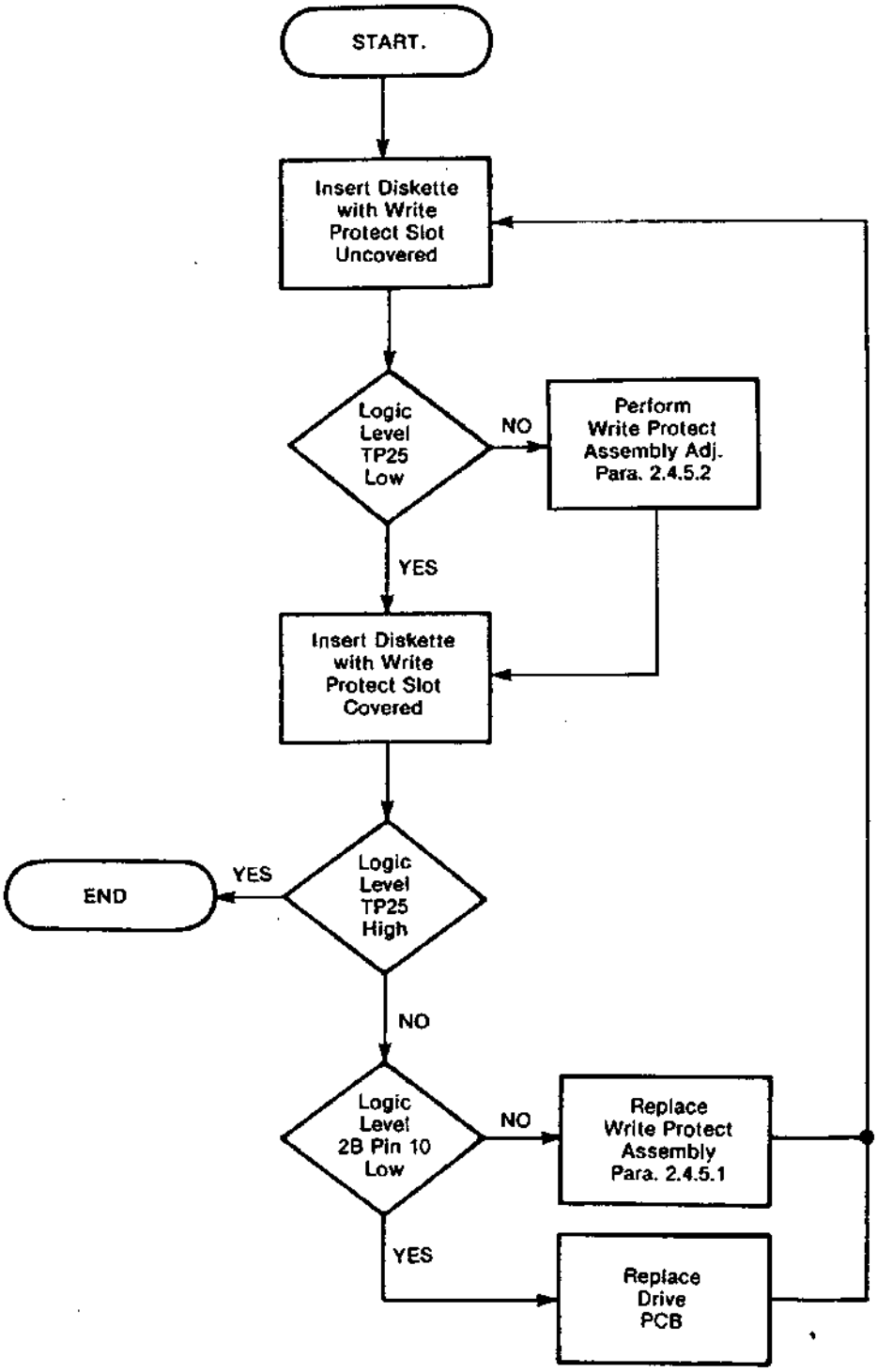
h. Grasp both ends of the push button and bow outwards to remove LED.

i. Reverse procedure to install.

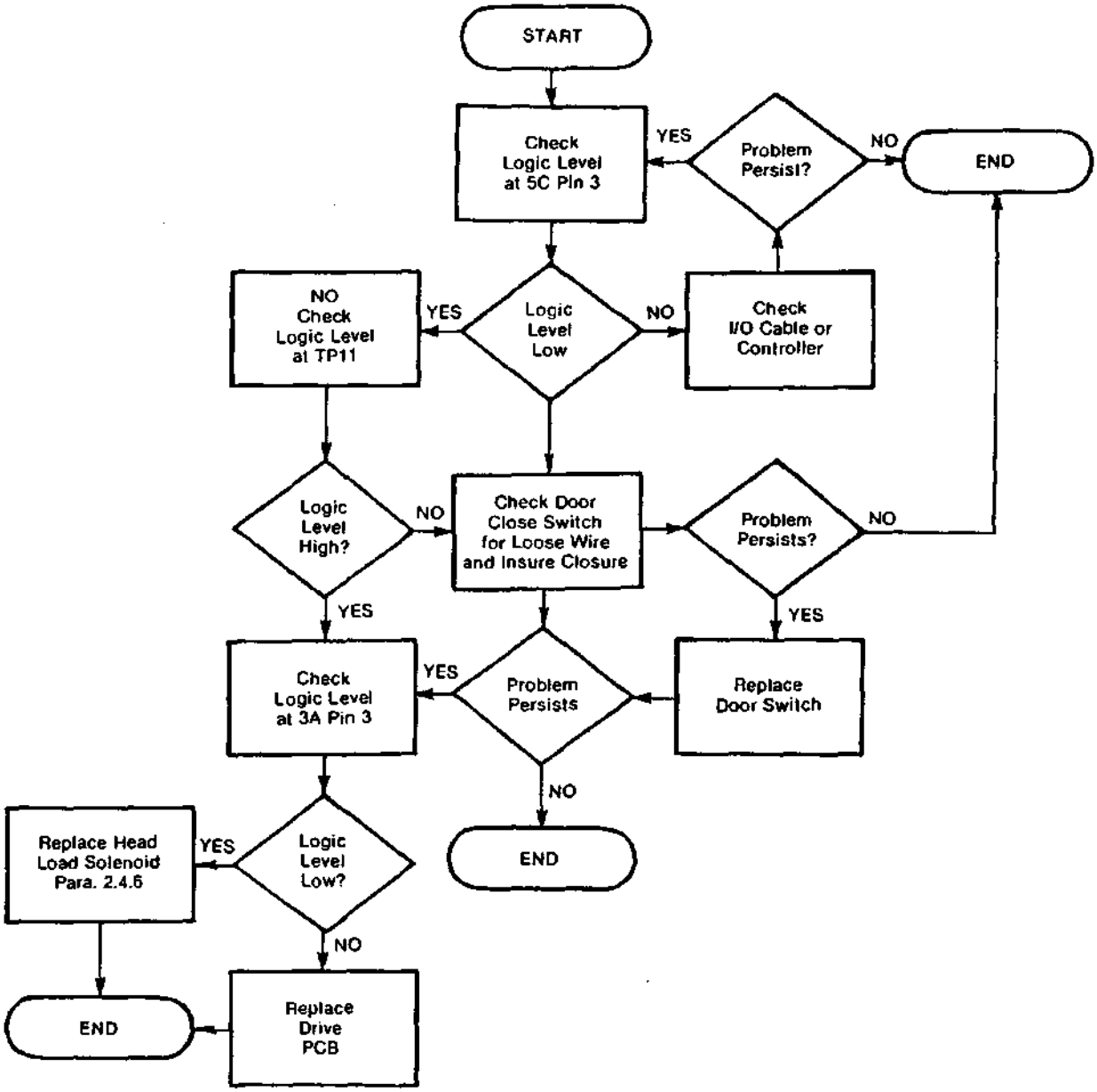
j. Check Index adjustment (Section 2.4.7.2).

Flow Charts

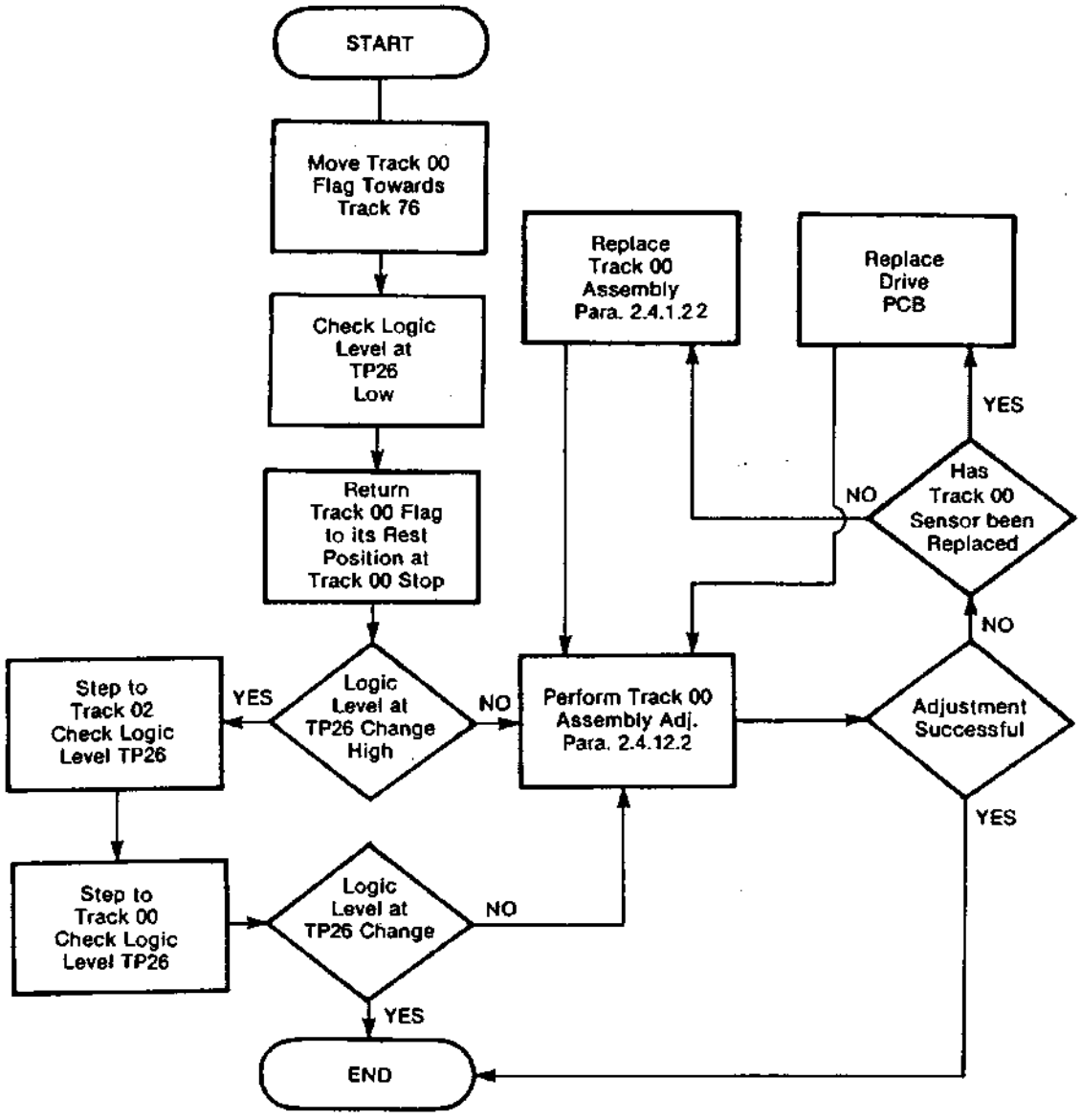
WRITE PROTECT INOPERATIVE



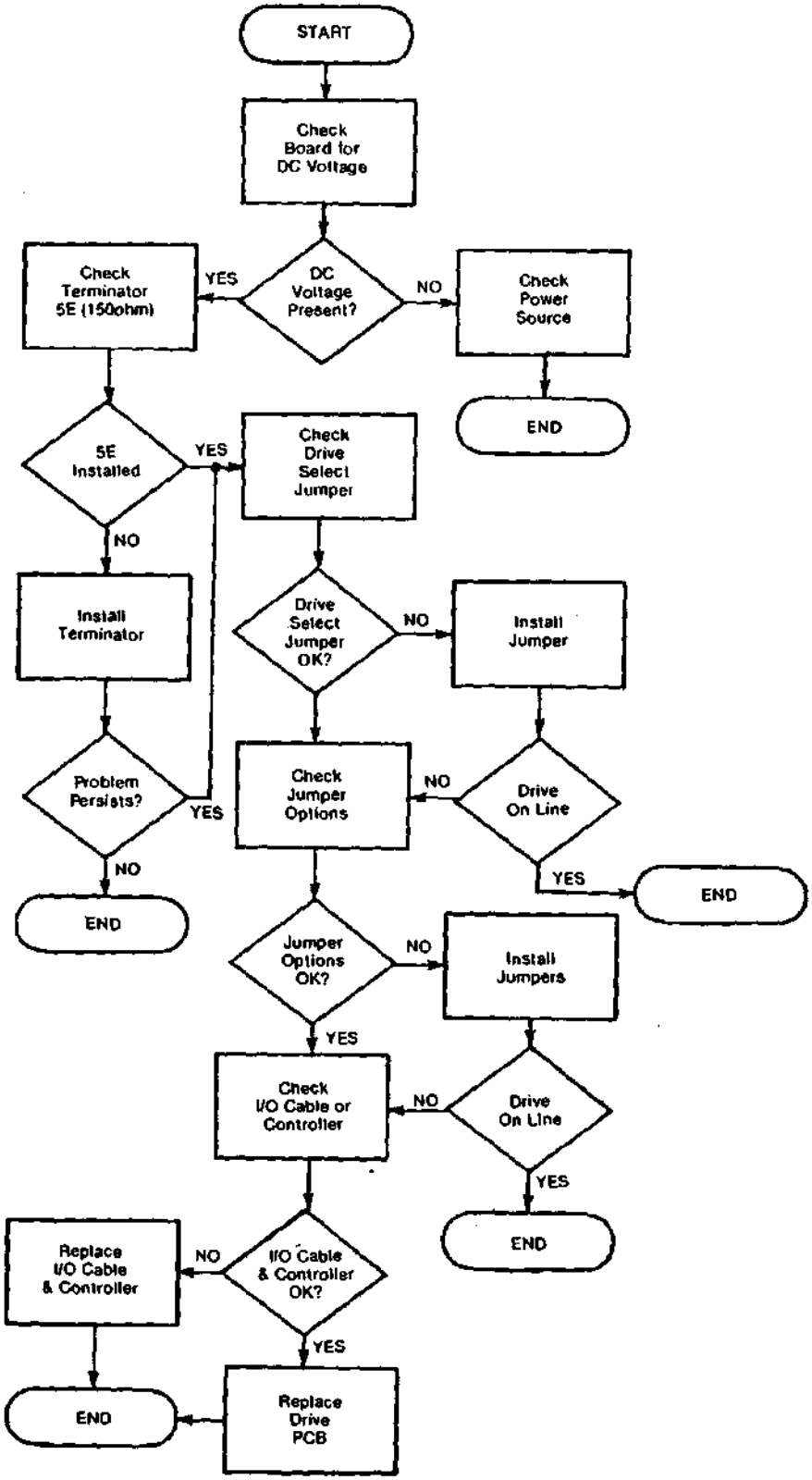
HEAD LOAD INOPERATIVE



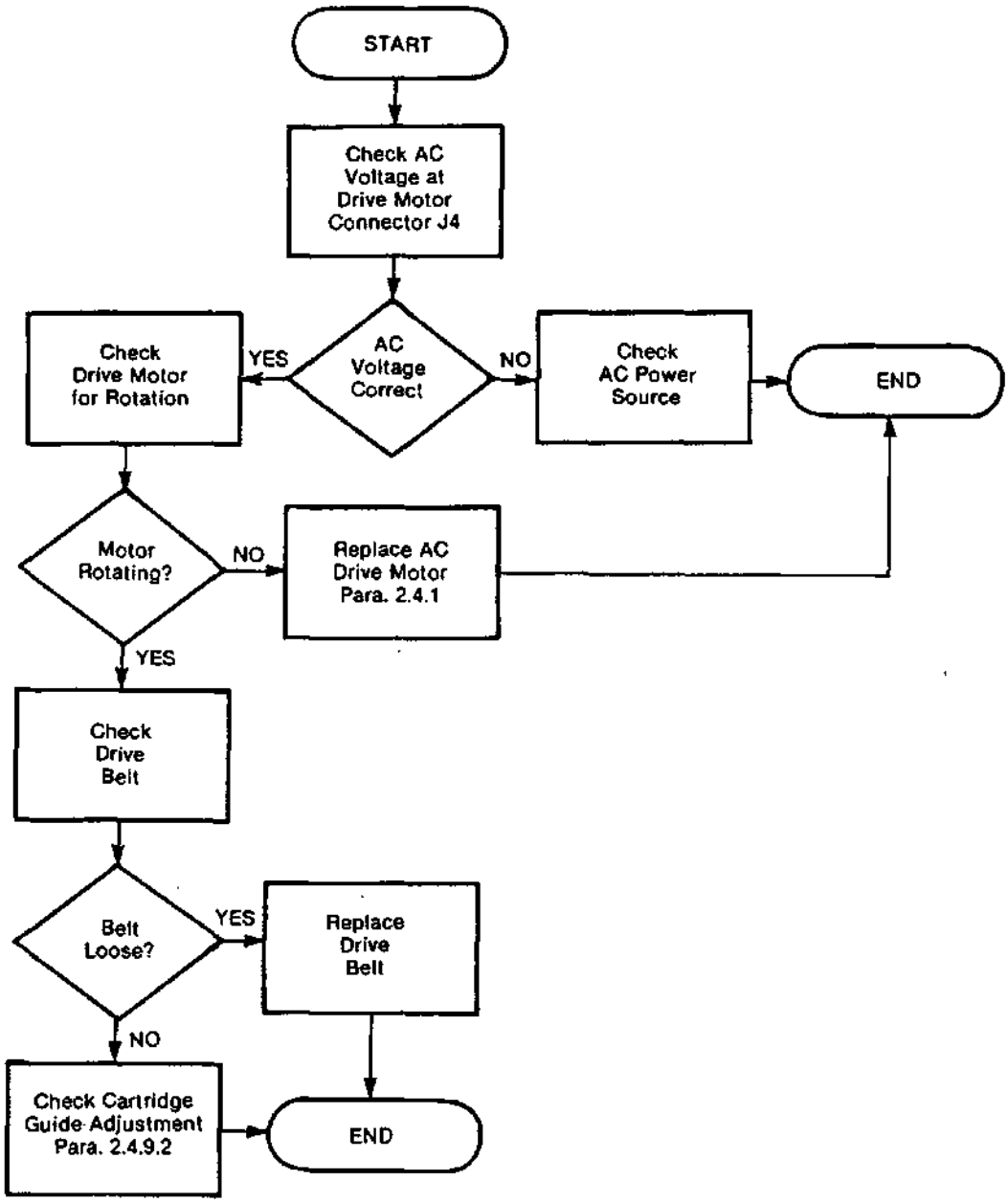
TRACK 00 INDICATOR INOPERATIVE



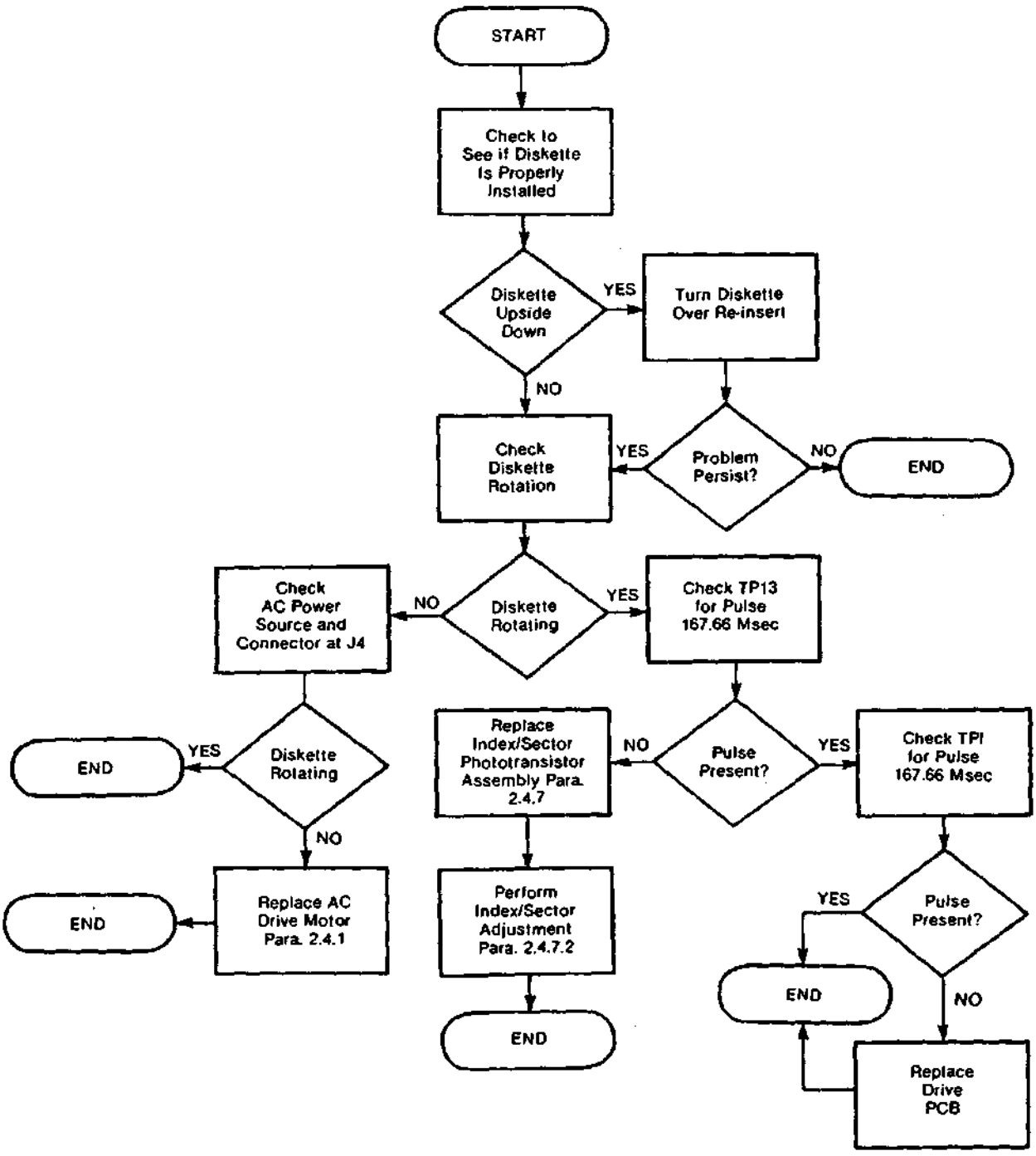
DRIVE NOT COMING ON LINE



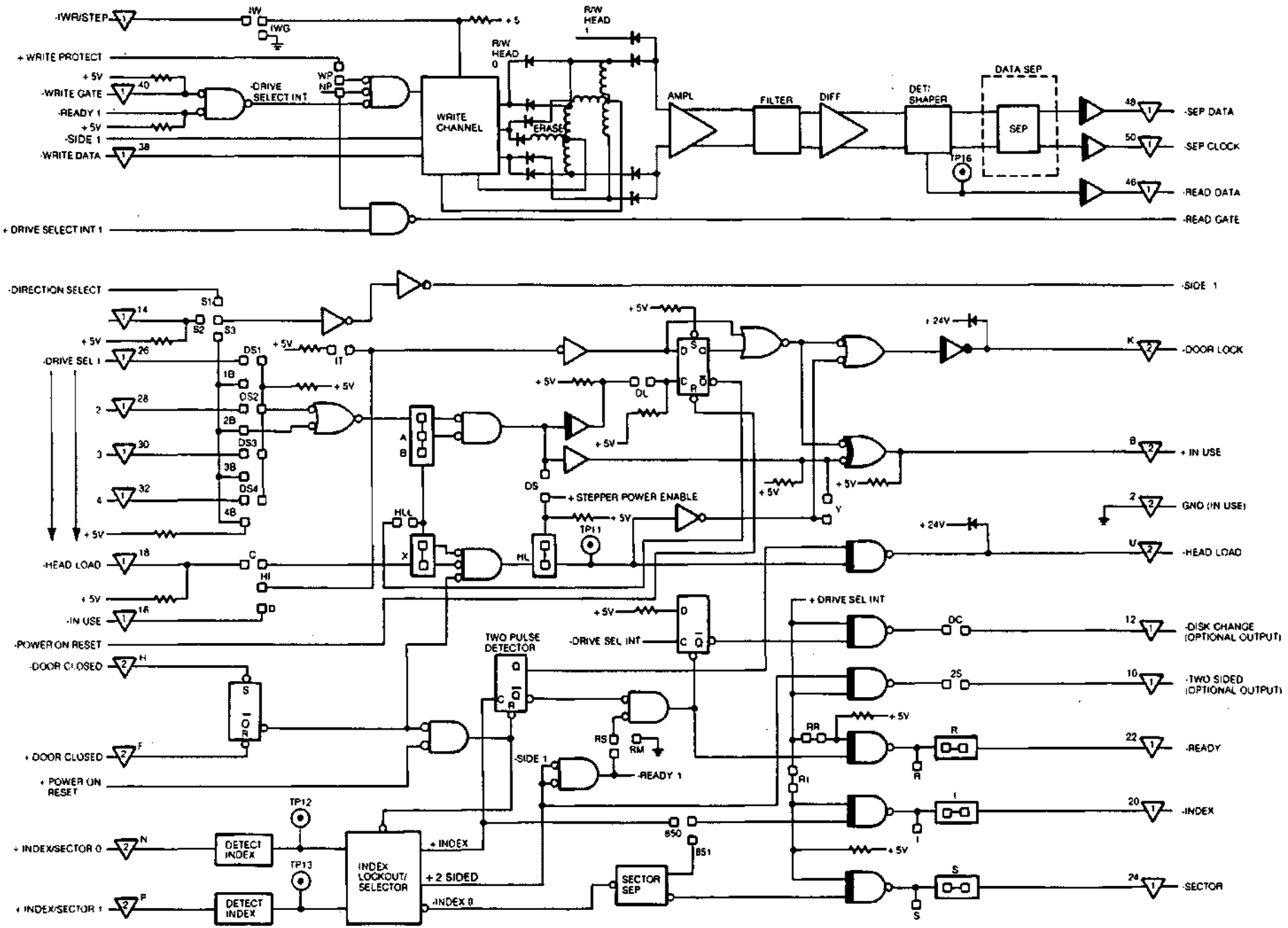
DISKETTE NOT ROTATING

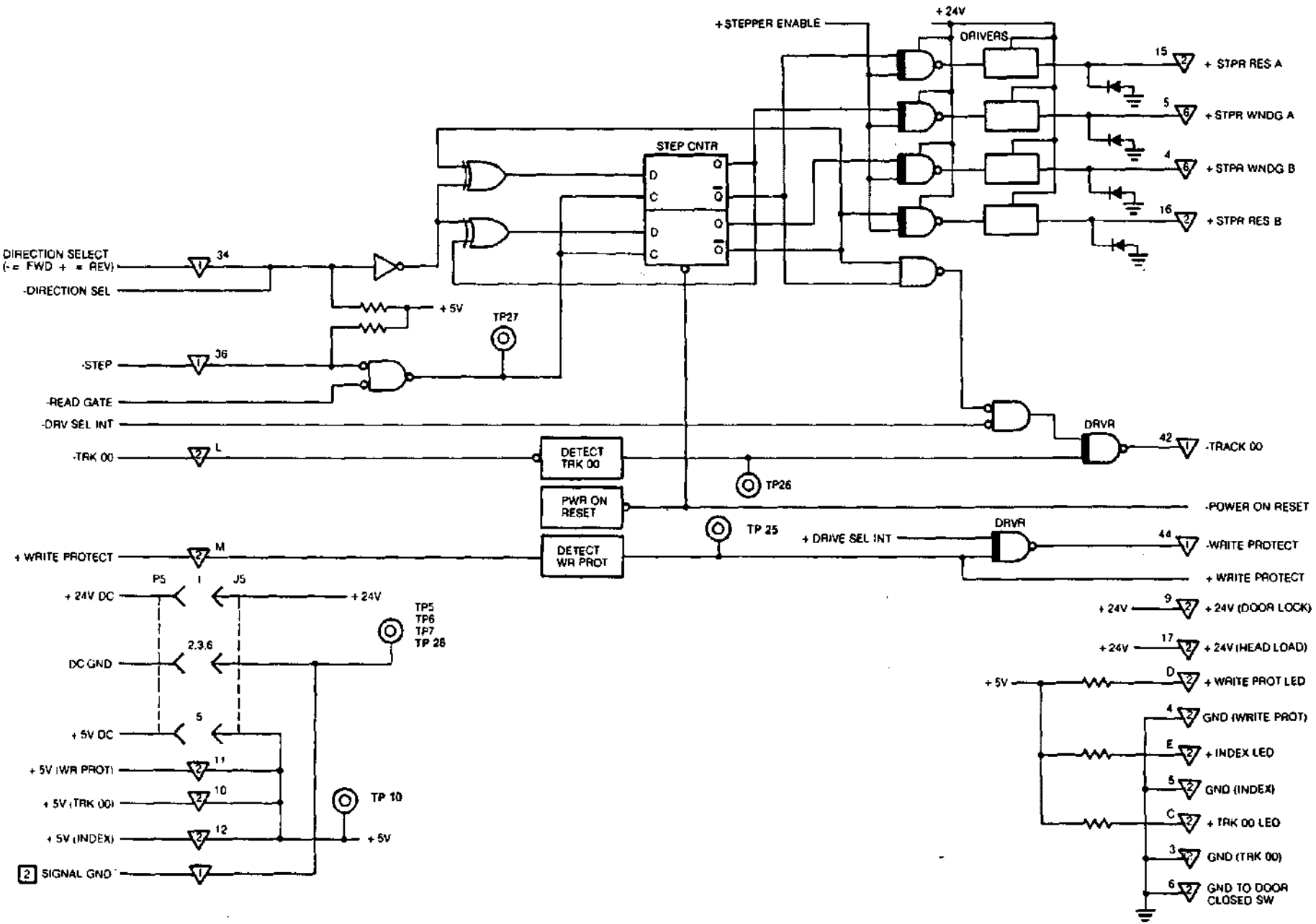


INDEX PULSE INOPERATIVE



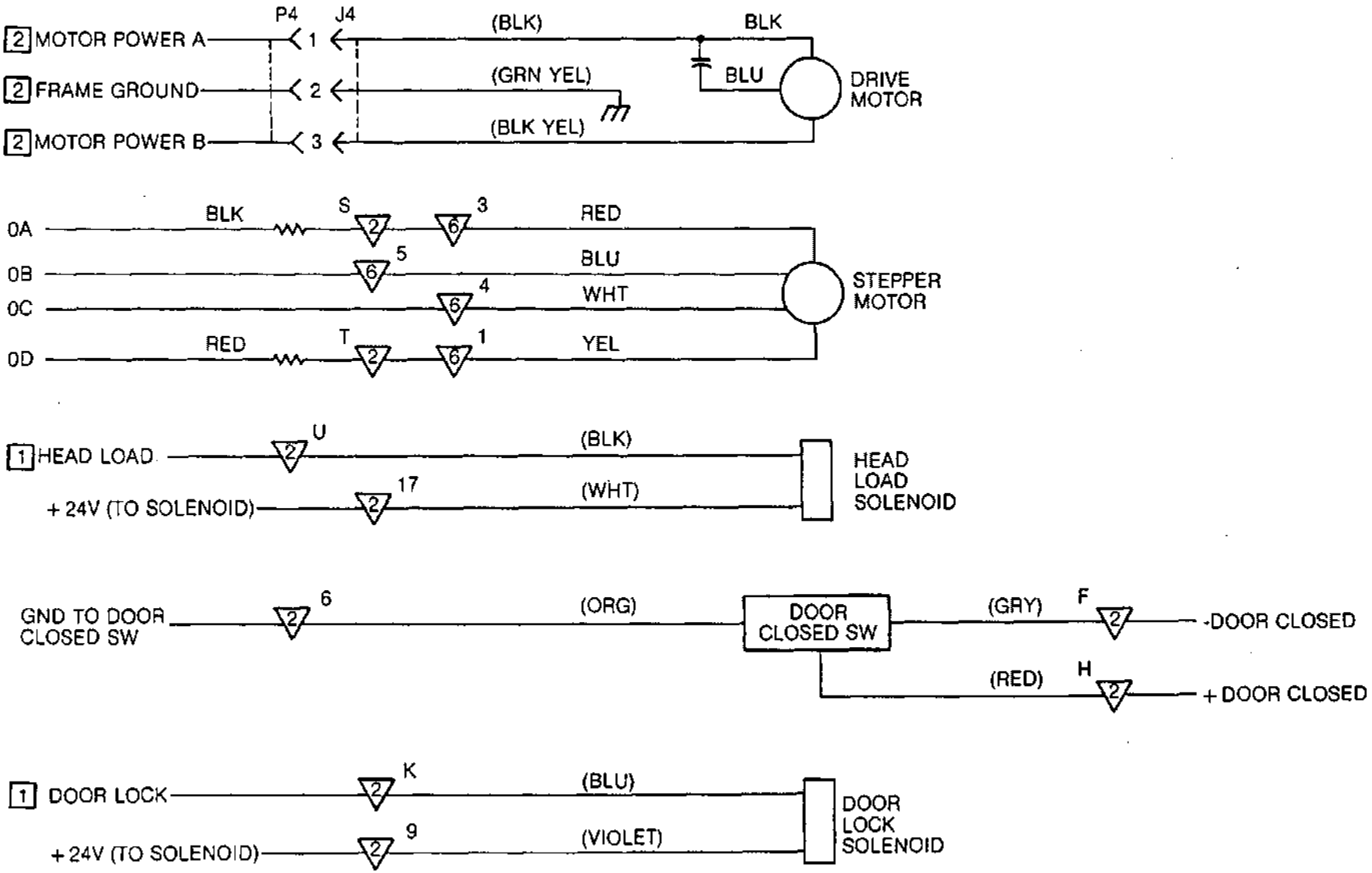
Logic Diagrams


-IWR/STEP
IW
IWG
+ WRITE PROTECT
+ 5V
-WRITE GATE
-READY 1
+ 5V
-SIDE 1
-WRITE DATA
40
38
-DRIVE SELECT INT
WP
NP
WRITE CHANNEL
+ 5
R/W HEAD 1
R/W HEAD 0
ERASE
AMPL
FILTER
DIFF
DET/ SHAPER
DATA SEP
SEP
TP16
48
-SEP DATA
50
-SEP CLOCK
46
-READ DATA
-READ GATE
+ DRIVE SELECT INT 1
-DIRECTION SELECT
S1
S2
S3
14
+ 5V
-DRIVE SEL 1
26
28
30
32
DS1
DS2
DS3
DS4
1B
2B
3B
4B
IT
A
B
HLL
X
HL
DS
+ STEPPER POWER ENABLE
TP11
DL
Q
C
R
Y
-HEAD LOAD
18
C
HI
-IN USE
16
D
-POWER ON RESET
-DOOR CLOSED
H
+ DOOR CLOSED
F
+ POWER ON RESET
S
I
O
2
TWO PULSE DETECTOR
-DRIVE SEL INT
+ DRIVE SEL INT
-SIDE 1
-READY 1
RS
RM
RR
RI
R
I
S
DC
2S
TP12
TP13
+ INDEX/SECTOR 0
N
+ INDEX/SECTOR 1
P
DETECT INDEX
INDEX LOCKOUT/ SELECTOR
+ INDEX
+ 2 SIDED
-INDEX 0
SECTOR SEP
850
851
+ 24V
K
-DOOR LOCK
B
+ IN USE
2
GND (IN USE)
U
-HEAD LOAD
12
-DISK CHANGE (OPTIONAL OUTPUT)
10
-TWO SIDED (OPTIONAL OUTPUT)
22
-READY
20
-INDEX
24
-SECTOR



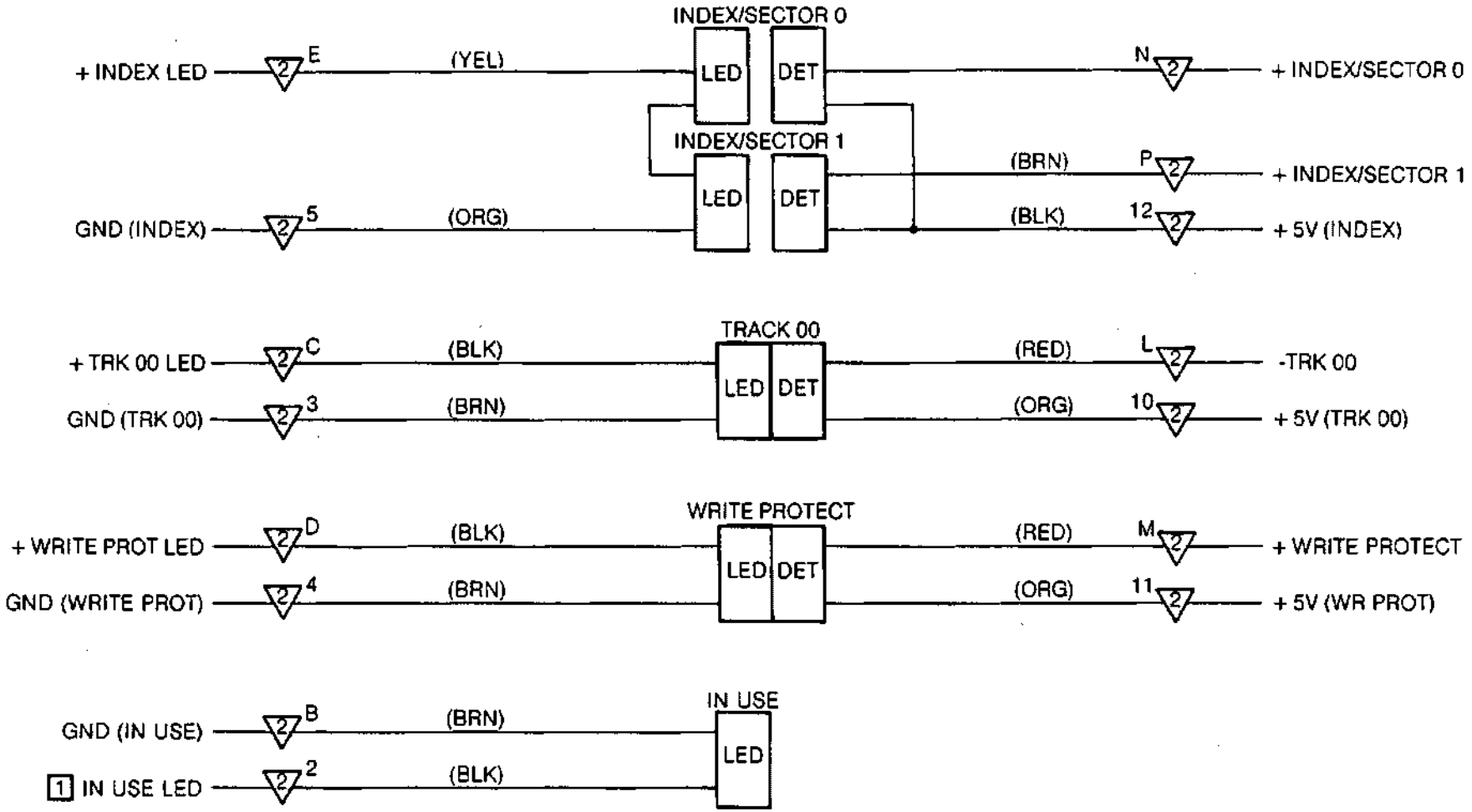
NOTES:

1. CONNECTOR SYMBOL REFERENCE 1 = J1, 2 = J2, 5 = J5.
2. ALL ODD NUMBERED PINS ON J1 CONNECTOR ARE GROUND.



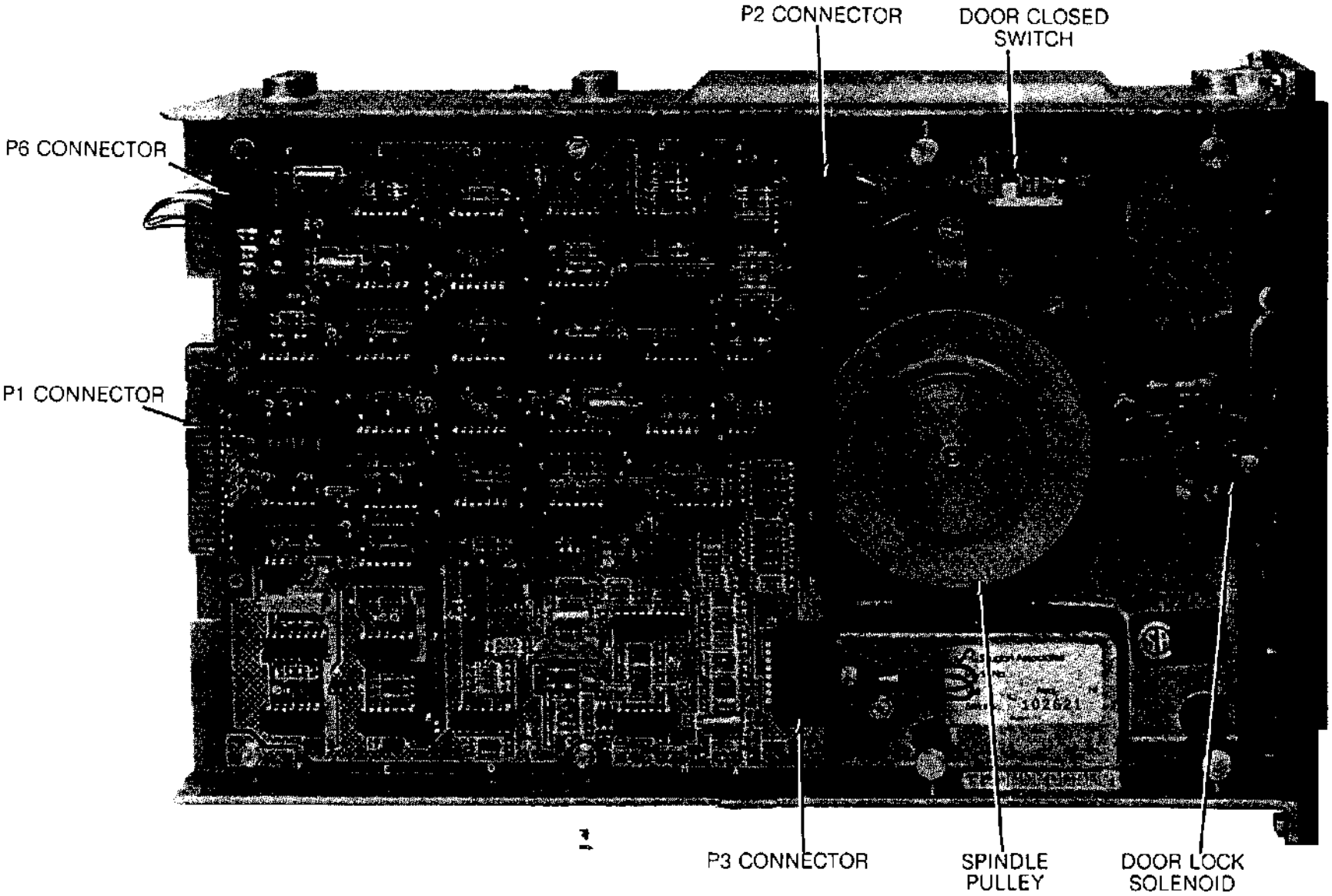
NOTES:

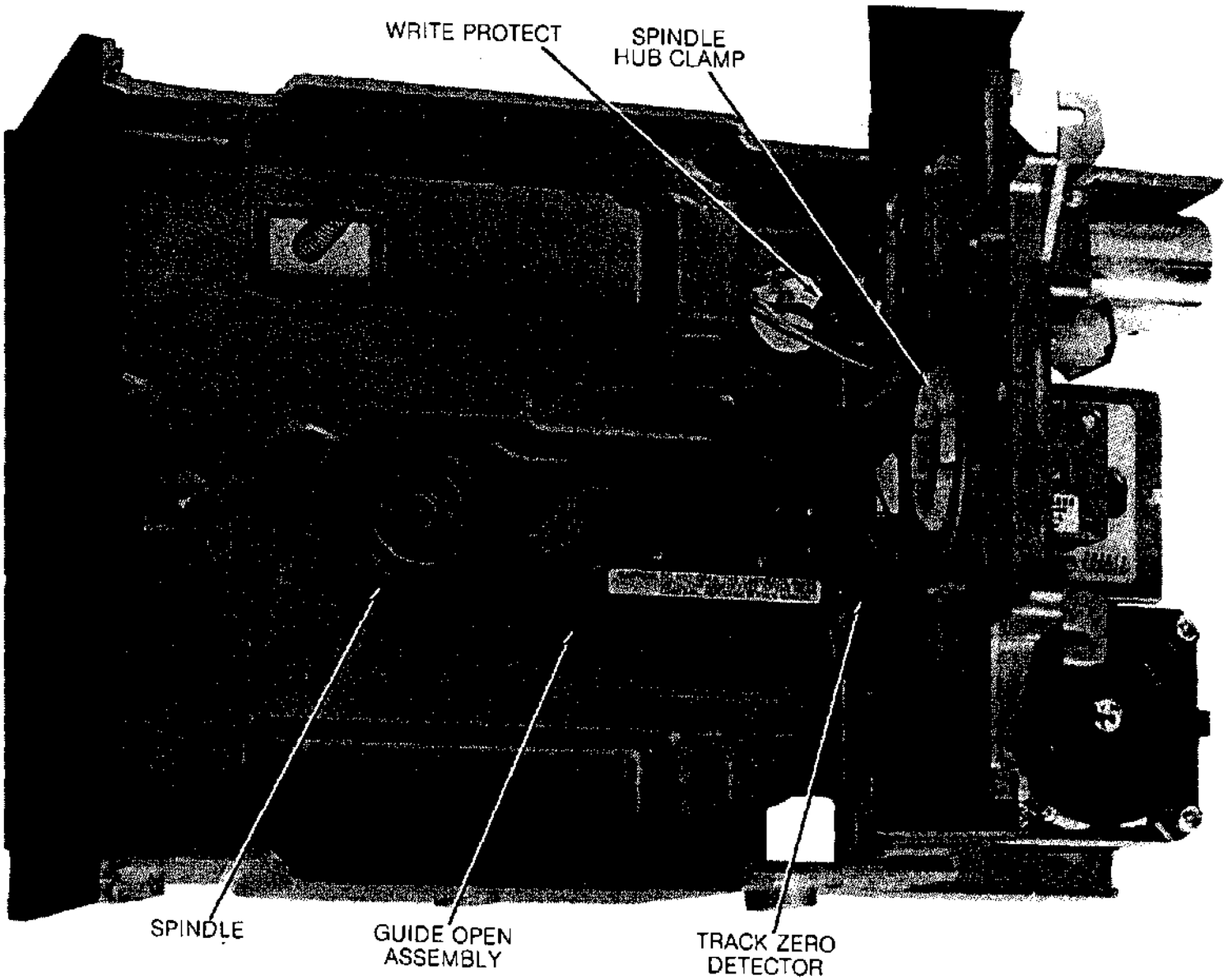
1. GND WHEN ACTIVE AND + 24 WHEN INACTIVE.
2. 115 OR 230 VAC.

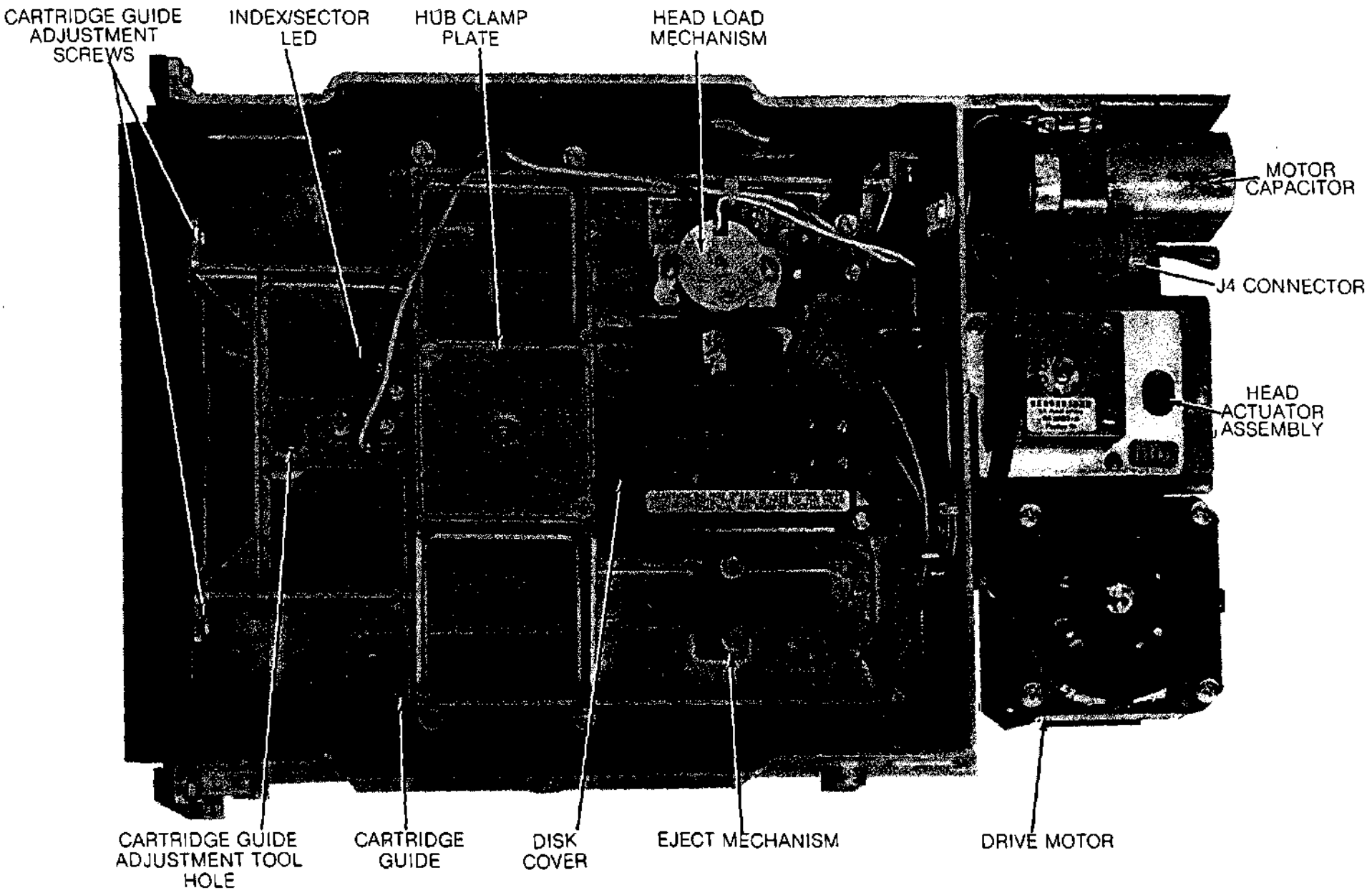


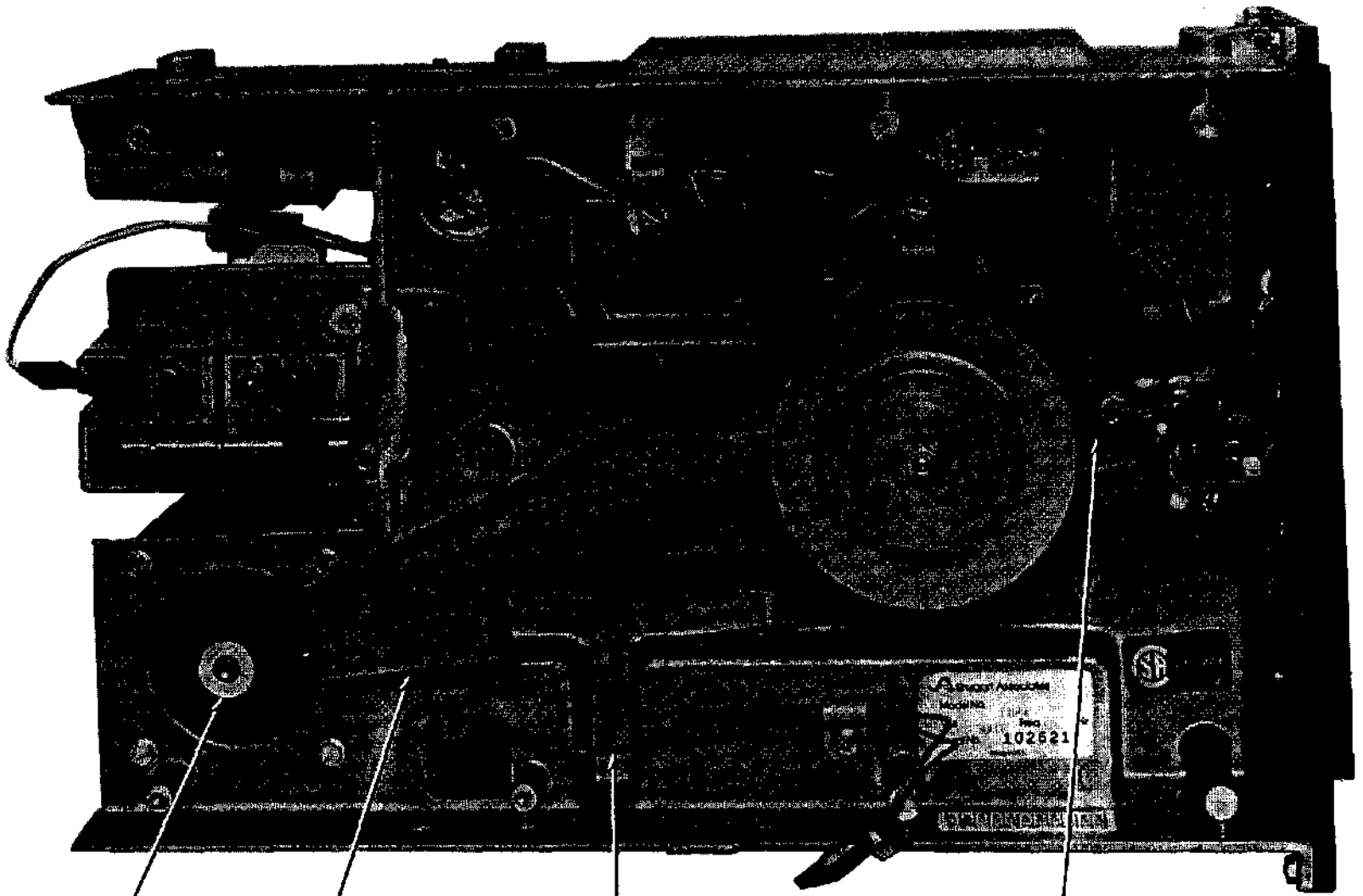
NOTES:
1 GND WHEN INACTIVE AND + 1.5VDC WHEN ACTIVE.

Physical Locations


P2 CONNECTOR
DOOR CLOSED SWITCH
P6 CONNECTOR
P1 CONNECTOR
P3 CONNECTOR
SPINDLE PULLEY
DOOR LOCK SOLENOID


WRITE PROTECT
SPINDLE HUB CLAMP
SPINDLE
GUIDE OPEN ASSEMBLY
TRACK ZERO DETECTOR


CARTRIDGE GUIDE ADJUSTMENT SCREWS
INDEX/SECTOR LED
HUB CLAMP PLATE
HEAD LOAD MECHANISM
MOTOR CAPACITOR
J4 CONNECTOR
HEAD ACTUATOR ASSEMBLY
CARTRIDGE GUIDE ADJUSTMENT TOOL HOLE
CARTRIDGE GUIDE
DISK COVER
EJECT MECHANISM
DRIVE MOTOR


DRIVE MOTOR
PULLEY
DRIVE
BELT
R/W HEAD
CABLE
INDEX/SECTOR
PHOTO TRANSISTOR

Illustrated Parts Catalog

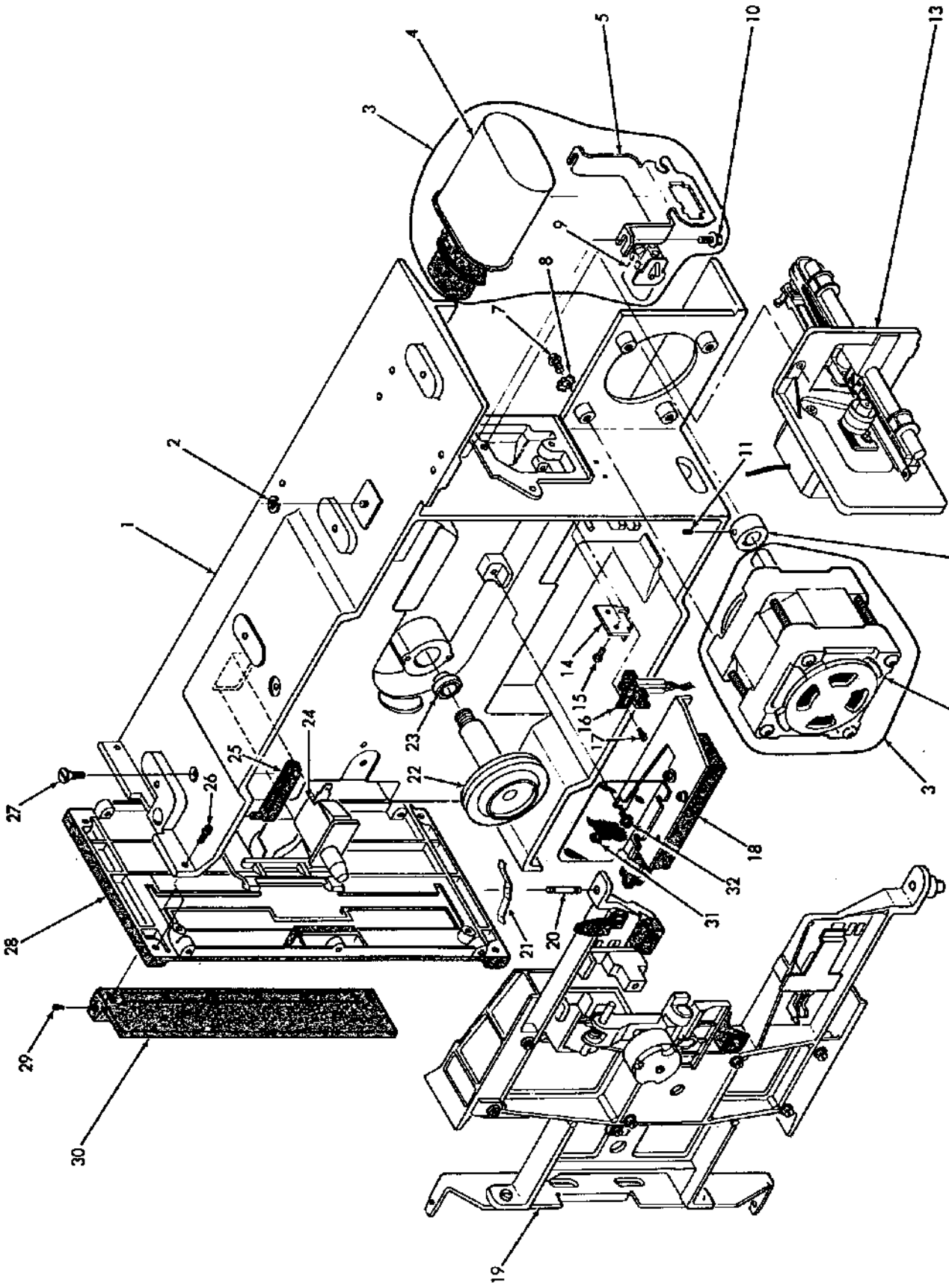
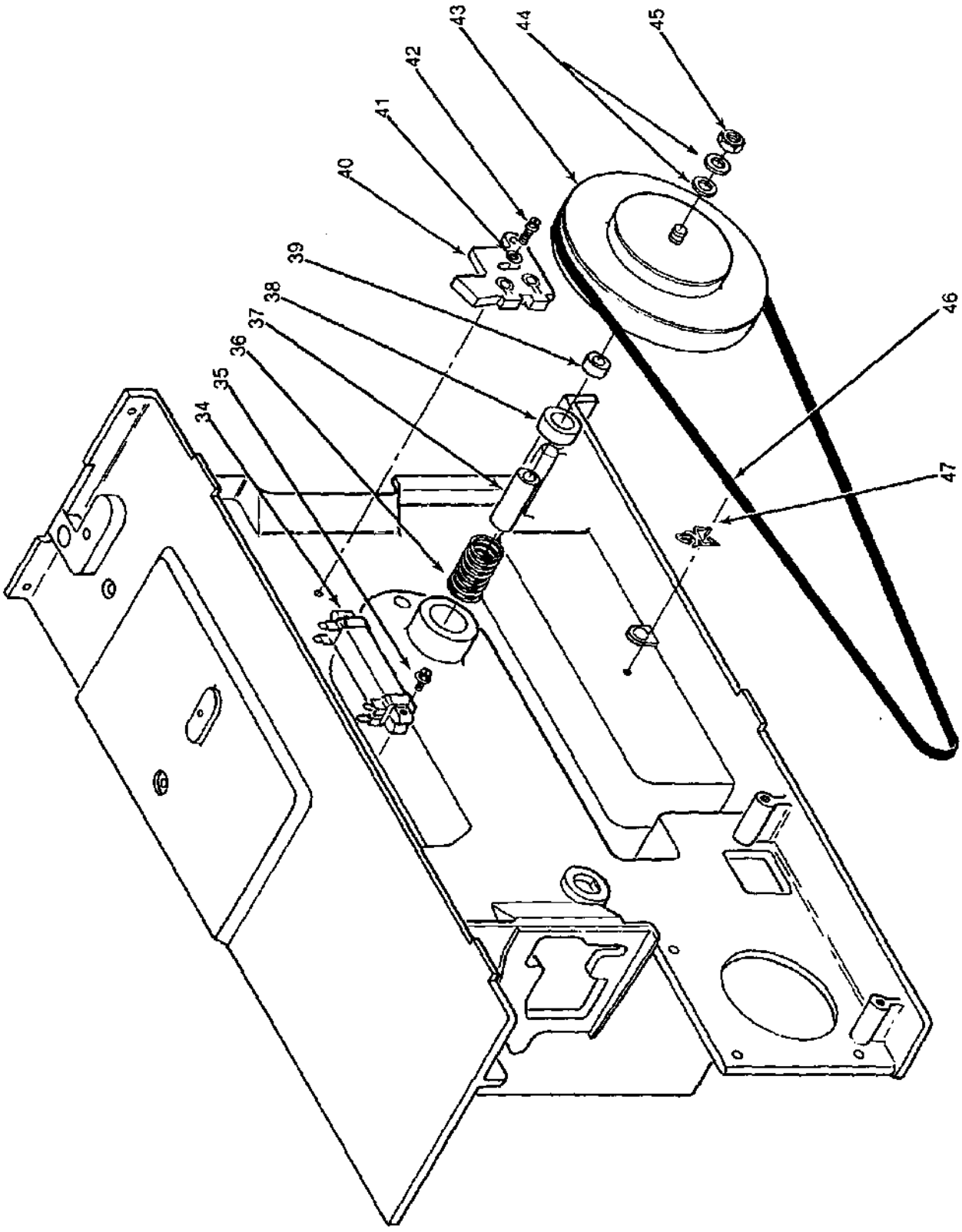


FIGURE 49. (1 of 2)


34
35
36
37
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39
40
41
42
43
44
45
46
47

FIGURE & REF NUMBER	PART NUMBER	DESCRIPTION	QTY PER ASM
49-1		DRIVE ASSEMBLY SA850/851	
2	11305	CLIP (RETAINING RING)	1
3	50747	MOTOR ASSEMBLY, 115V, 50/60 HZ	1
	50748	MOTOR ASSEMBLY, 230V, 50/60 HZ	1
4	15004	CAPACITOR	1
5	50746	BRACKET	1
6	50744	MOTOR 115V, 50/60 HZ	1
	50745	MOTOR 230V, 50/60 HZ	1
7	12028	SCREW HEX HEAD 8-32 × .75	4
8	10013	WASHER	4
9	15669	HOUSING, 3 PIN CONNECTOR	1
10	12015	SCREW, 8-32 × .312	2
11	11904	SCREW, SET 6-32 × .125	1
12	50358	PULLEY, 60 HZ	1
	50357	PULLEY 50 HZ	1
13	51127	HEAD ACTUATOR ASSEMBLY	1
14	51056	BRACKET, TRACK 0C	1
15	12013	SCREW, 6-32 × .312	2
16	51027	TRACK 00 ASSEMBLY	1
17	12053	SCREW	1
18	51063	GUIDE OPEN ASSEMBLY	1
19	51134	CARTRIDGE GUIDE ASSEMBLY (SEE FIGURE 50)	1
20	50167	PIVOT	1
20	50670	PIVOT (RACK MOUNT)	1
21	50168	BIAS SPRING	1
22	51198	SPINDLE	1
23	10801	FLANGED BEARING, SPINDLE	1
24	17200	DOOR OPEN SWITCH	1
25	50559	DEFLECTOR	2
26	12013	SCREW 6-32 × .438	4
27	12032	SCREW #8 × .50 2	2
28		FRONT PLATE ASSEMBLY (SEE FIGURE 51)	
29	11905	SCREW	2
30	50142	HANDLE	1
31	12011	SCREW, HEX HD 4-40	4
32	12053	SCREW	2
33	51058	COVER	1
34	51028	RESISTOR ASM	1
35	12026	SCREW	2
36	50166	SPRING, SPINDLE	1
37	50018	SPACER, SPINDLE LONG	1
38	10800	BALL BEARING	1
39	50019	SPACER SPINDLE SHORT	1
40	51046	PHOTO XSTR ASM	1
41	12026	SCREW	2
42	12036	SCREW	1
43	50016	PULLEY SPINDLE	1
44	12509	WASHER, SPRING #8	2
45	10025	NUT 8-32	1
46	50356	BELT, 60 HZ	1
46	50355	BELT, 50 HZ	1
47	10426	CABLE CLAMP	1

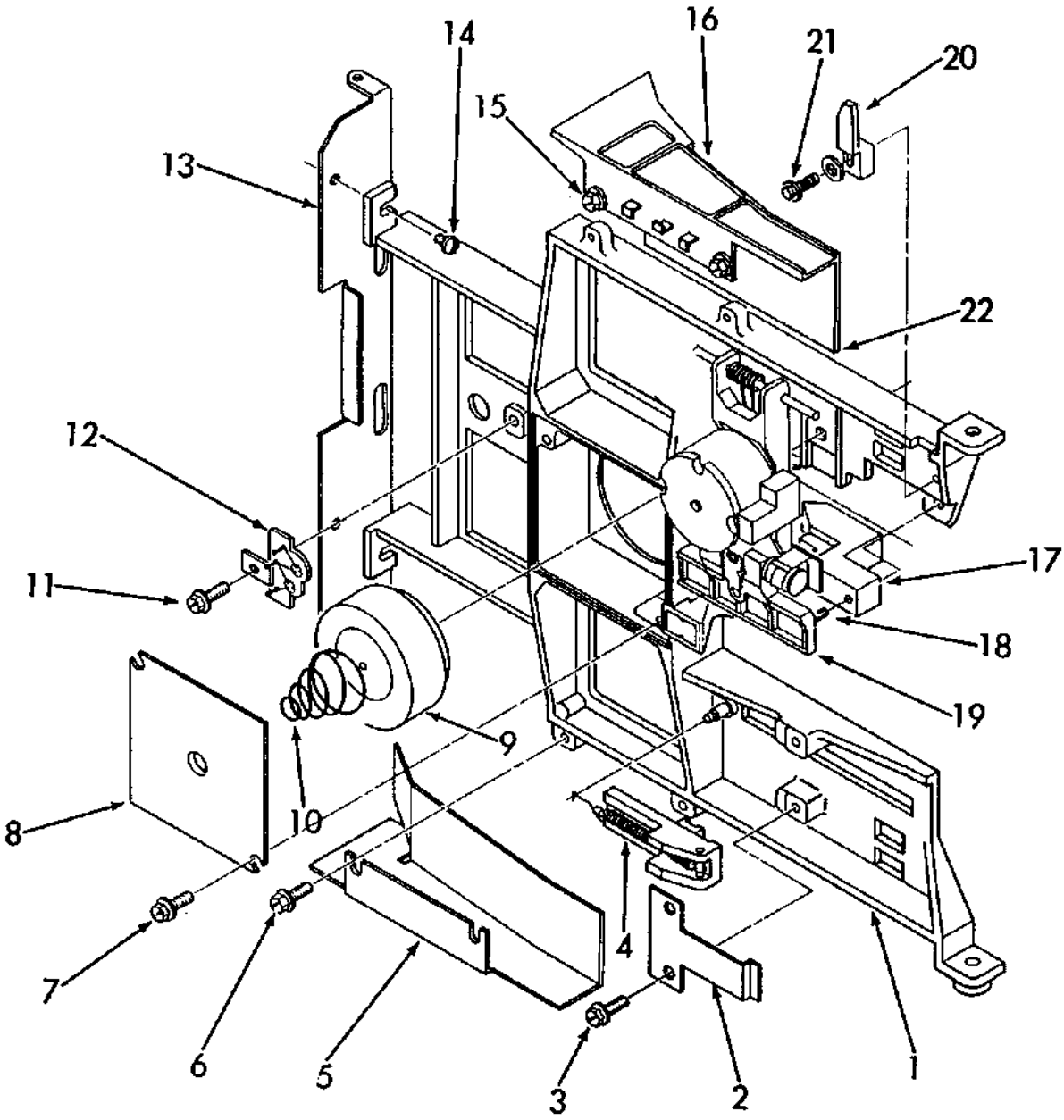


FIGURE 50.

FIGURE & REF NUMBER	PART NUMBER	DESCRIPTION	QTY PER ASM
50-1	51134	CARTRIDGE GUIDE ASSEMLBY	1
2	50555	SPRING, EJECTOR	1
3	12015	SCREW, 8-32	2
4	50609	EJECTOR ASSEMBLY	1
5	51062	STRIPPER BOTTOM	1
6	12015	SCREW, 8-32	2
7	12020	SCREW, 8-32	2
8	50546	PLATE, HUB CLAMP	1
9	50254	HUB ASSEMBLY	1
10	50031	SPRING, CLAMP	1
11	12016	SCREW, 8-32	1
12	51029	LED ASSEMBLY	1
13	50151	LATCH	1
14	10187	SCREW 6-32	2
15	12015	SCREW 8-32	2
16	51061	STRIPPER, TOP	1
17	50313	WRITE PROTECT ASSEMBLY	1
18	12026	SCREW	1
19	51176	HEAD LOAD MECHANISM	1
20	51075	LIMITER	1
21	10014	#8 WASHER	1
22	12020	SCREW 8-32	1

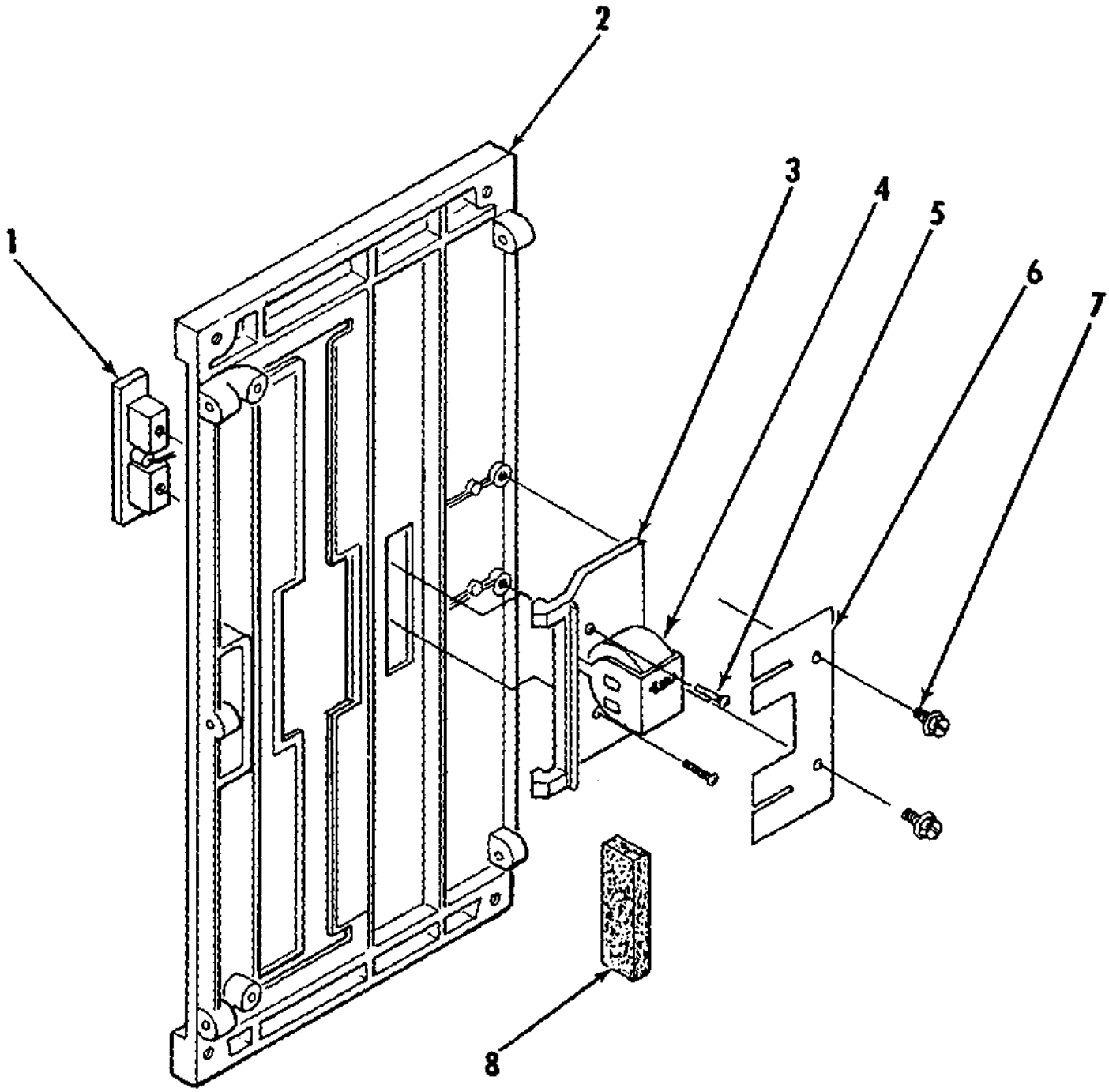
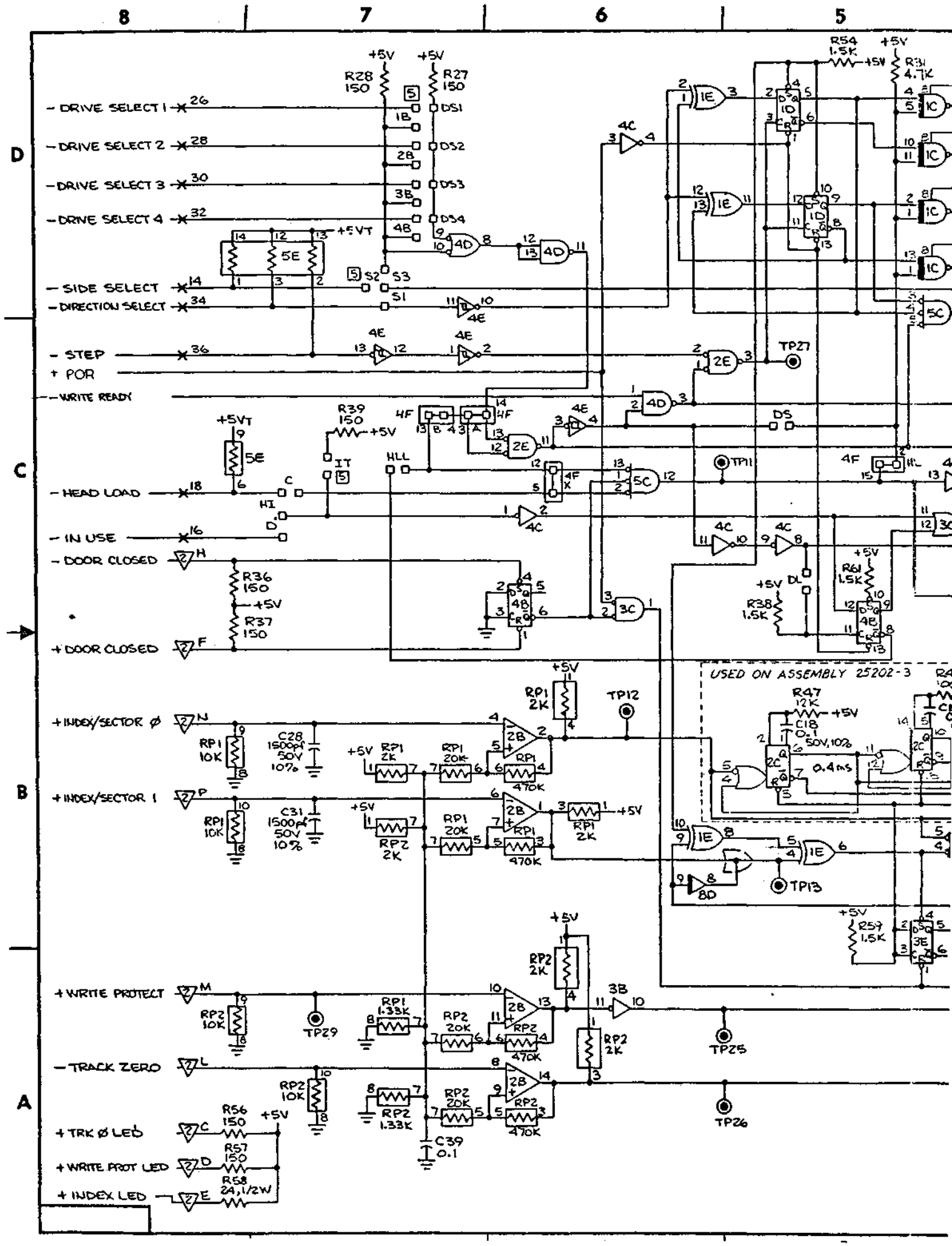
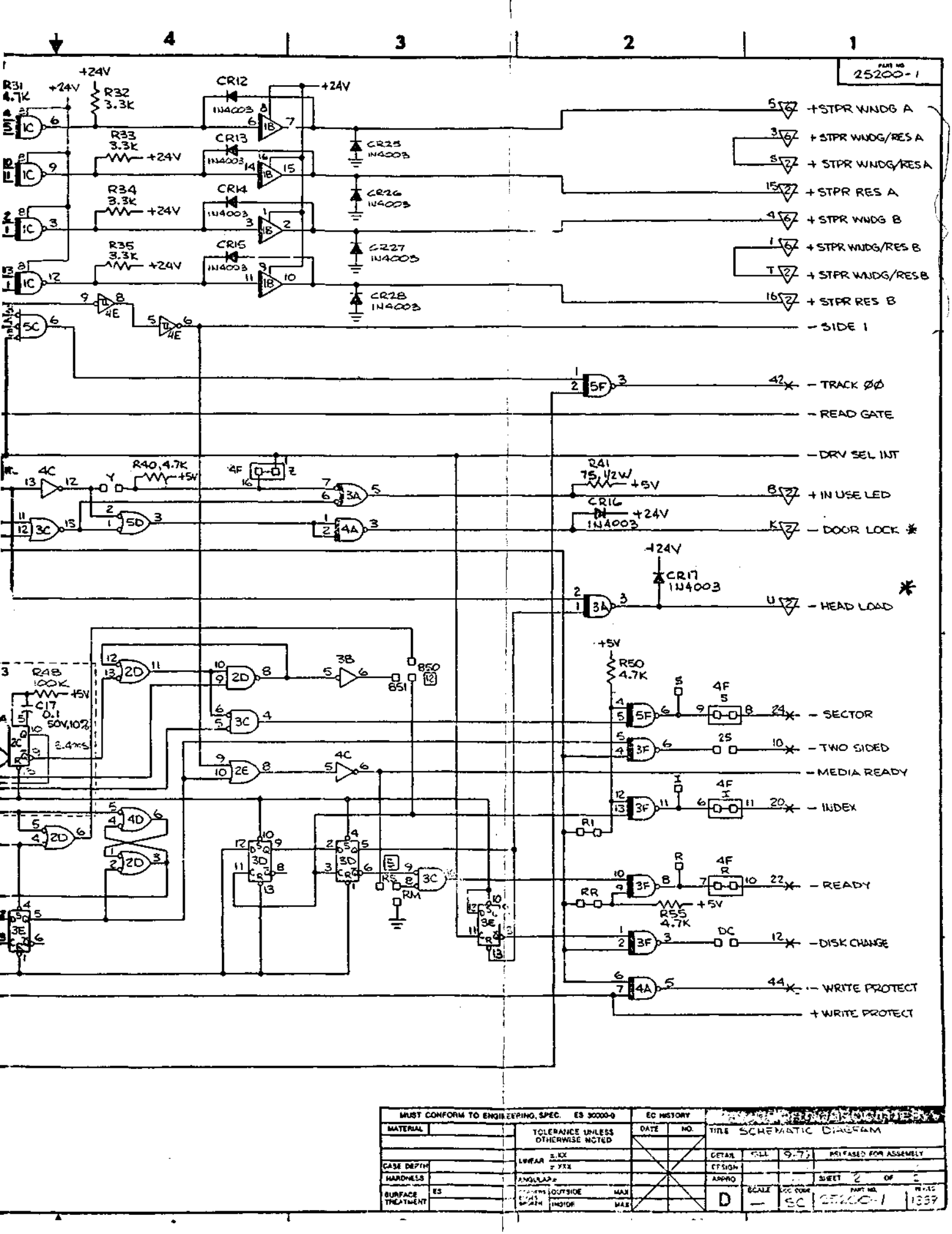


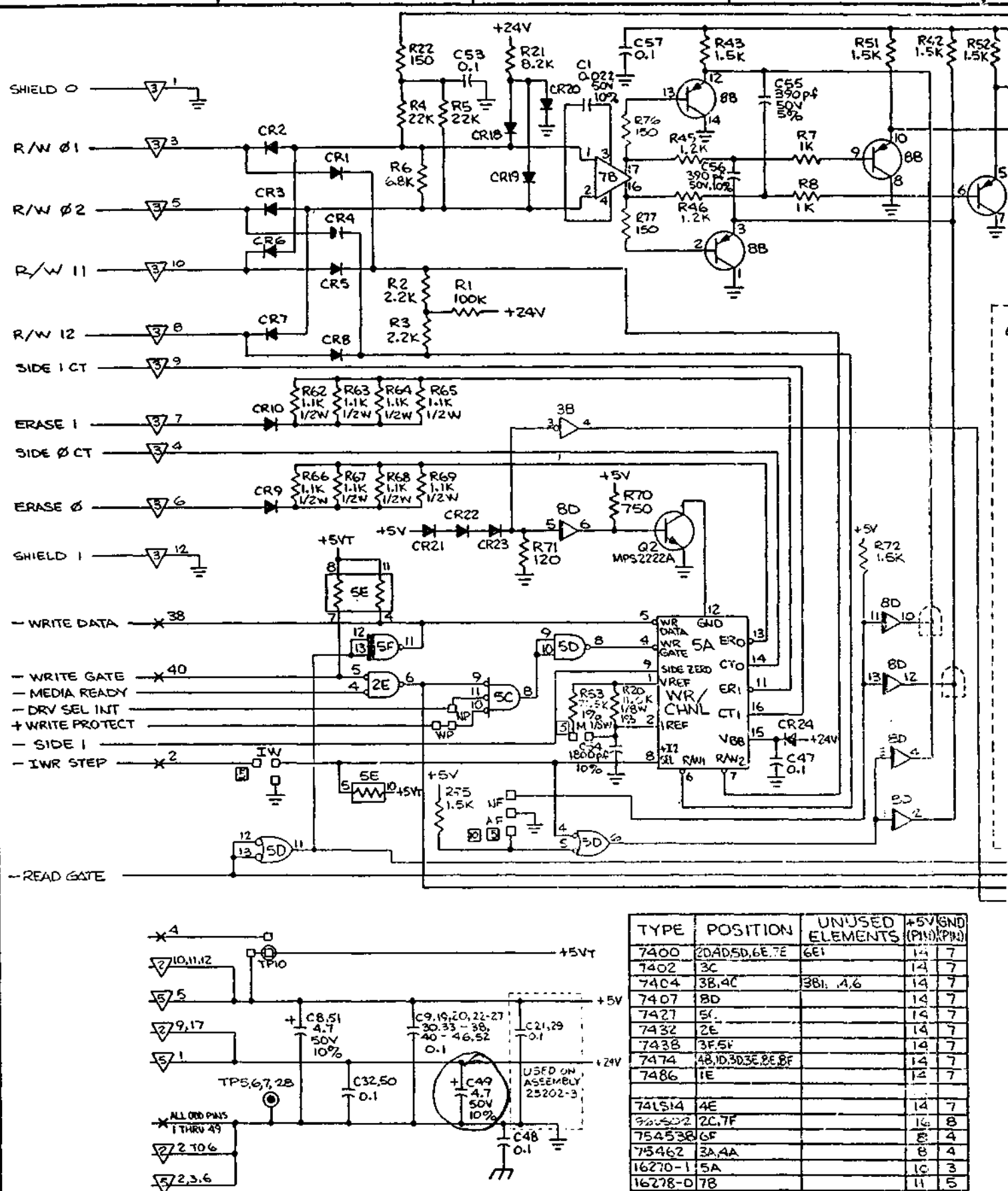
FIGURE 51

FIGURE & REF NUMBER	PART NUMBER	DESCRIPTION	QTY PER ASM
51	51037	FRONT PLATE ASSEMBLY LITE/LOCK	
	51043	FRONT PLATE ASSEMBLY LITE/LOCK (RACK MOUNT)	
-1	50587	PUSH BAR	1
-2	50349	FRONT PLATE	1
	50667	FRONT PLATE (RACK MOUNT)	1
-3	51038	LATCH ASSEMBLY, DOOR LOCK	1
-4	10002	SOLENOID	1
-5	12035	SCREW 4-40 × .250	2
-6	50691	SPRING LATCH INTERLOCK	1
-7	12013	SCREW 6-32 × .312	2
-8	50183	BUMPER	1

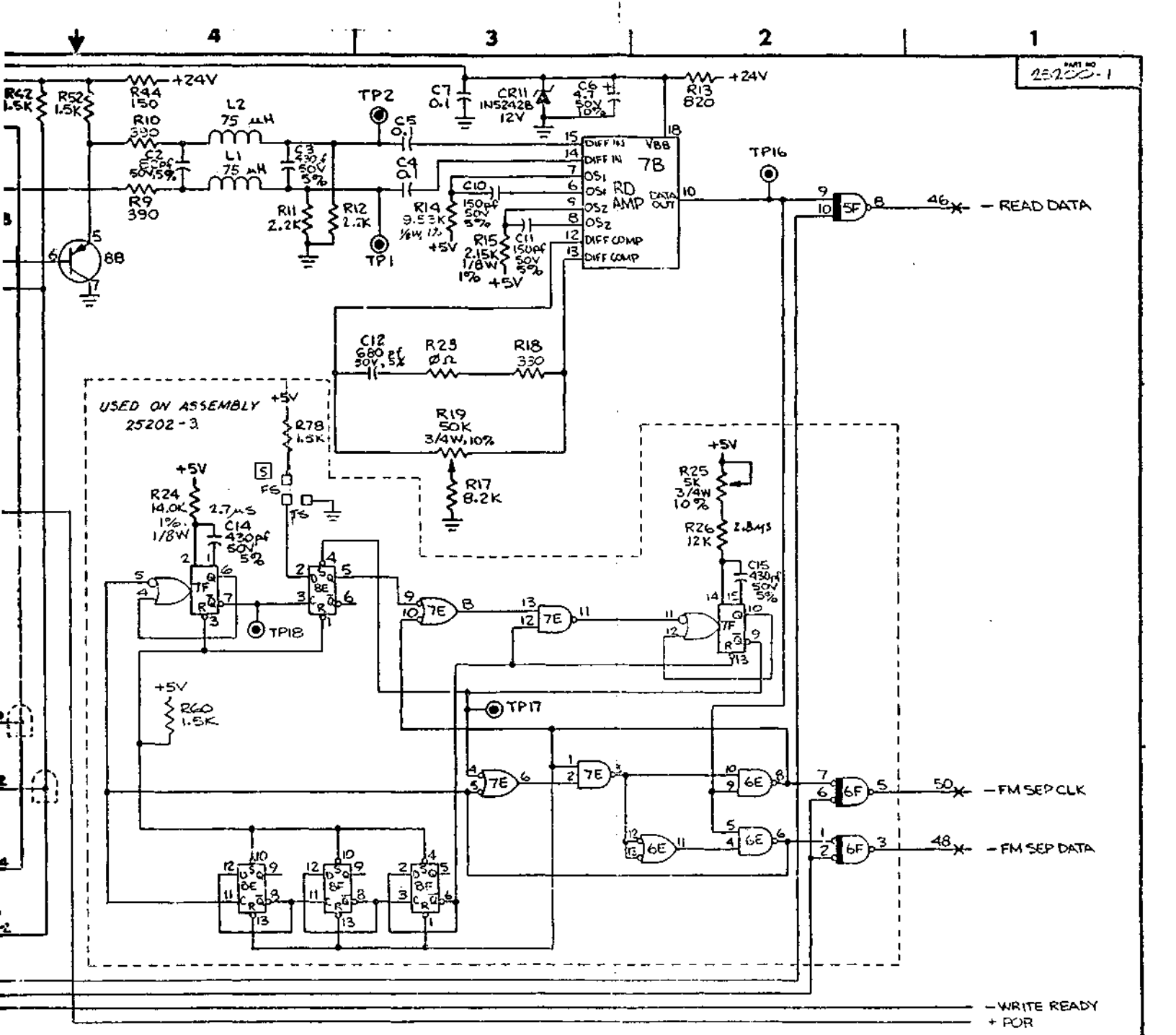
Schematic Diagrams


8
7
6
5
D
C
B
A
– DRIVE SELECT 1
– DRIVE SELECT 2
– DRIVE SELECT 3
– DRIVE SELECT 4
– SIDE SELECT
– DIRECTION SELECT
– STEP
+ POR
– WRITE READY
– HEAD LOAD
– IN USE
– DOOR CLOSED
+ DOOR CLOSED
+ INDEX/SECTOR Ø
+ INDEX/SECTOR 1
+ WRITE PROTECT
– TRACK ZERO
+ TRK Ø LED
+ WRITE PROT LED
+ INDEX LED
+5V
+5VT
R28 150
R27 150
R54 1.5K
R31 4.7K
R39 150
R36 150
R37 150
R61 1.5K
R38 1.5K
R47 12K
R57 1.5K
R56 150
R57 150
R58 24, 1/2W
RP1 2K
RP1 10K
RP1 20K
RP1 470K
RP1 1.33K
RP2 2K
RP2 10K
RP2 20K
RP2 470K
RP2 1.33K
C28 1500pf 50V 10%
C31 1500pf 50V 10%
C18 0.1 50V, 10%
C39 0.1
0.4ms
USED ON ASSEMBLY 25202-3
TP11
TP12
TP13
TP25
TP26
TP27
TP29
DS
DL
HI
HLL
IT


4
3
2
1
PART NO 25200-1
+24V
R31 4.7K
R32 3.3K
R33 3.3K
R34 3.3K
R35 3.3K
CR12 IN4003
CR13 IN4003
CR14 IN4003
CR15 IN4003
CR25 IN4003
CR26 IN4003
CR27 IN4003
CR28 IN4003
+STPR WNDG A
+STPR WNDG/RES A
+ STPR WNDG/RES A
+ STPR RES A
+STPR WNDG B
+STPR WNDG/RES B
+ STPR WNDG/RES B
+ STPR RES B
– SIDE 1
– TRACK ØØ
– READ GATE
– DRV SEL INT
R40, 4.7K +5V
R41 75, 1/2W +5V
CR16 IN4003 +24V
+ IN USE LED
– DOOR LOCK *
CR17 IN4003
– HEAD LOAD
R48 100K +5V
C17 0.1 50V, 10%
2.4mS
R50 4.7K +5V
– SECTOR
– TWO SIDED
– MEDIA READY
– INDEX
R1
– READY
RR
R55 4.7K +5V
– DISK CHANGE
– WRITE PROTECT
+ WRITE PROTECT
MUST CONFORM TO ENGINEERING SPEC. ES 30000-0
EC HISTORY
DATE
NO.
MATERIAL
TOLERANCE UNLESS OTHERWISE NOTED
LINEAR ± .XX ± .XXX
ANGULAR ±
CASE DEPTH
HARDNESS
SURFACE TREATMENT ES
OUTSIDE MAX
INSIDE MAX
TITLE SCHEMATIC DIAGRAM
DETAIL GLL 9-7-
RELEASED FOR ASSEMBLY
DESIGN
APPRO
SHEET 2 OF
SCALE —
SIZE D
CAGE CODE 9C
PART NO. 25200-1
REV 1337



TYPE	POSITION	UNUSED ELEMENTS	+5V (PIN)	GND (PIN)
7400	2DAD5D,6E,7E	6E1	14	7
7402	3C		14	7
7404	3B,4C	3B1, .4,6	14	7
7407	8D		14	7
7421	5C		14	7
7432	2E		14	7
7438	3F,5F		14	7
7474	4B,1D,3D3E,8E,8F		14	7
7486	1E		14	7
74LS14	4E		14	7
9615602	2C,7F		16	8
7545381	6F		8	4
75462	3A,4A		8	4
16270-1	5A		10	3
16278-D	7B		11	5
LM339	2B		3	12
RPK.150Ω	5E		–	–
SHUNT	4F		–	–
TPQ390X	8B		–	–
ULN2074B	1B		–	4&5,9
UHP407	1C		14	7



+5V PIN	GND (PIN)
1	7
2	7
3	7
4	7
5	7
6	7
7	7
8	7
9	7
10	7
11	7
12	7
13	
14	7
15	8
16	4
17	4
18	3
19	5
20	12
21	–
22	–
23	–
–	45/48
24	7

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL CAPACITORS ARE IN MICROFARADS, 50V, +80, -20%.
2. ALL DIODES ARE IN4148.
3. ALL INDUCTORS ARE IN MICROHENRYS, ±10%.
4. ALL RESISTORS ARE IN OHMS, 1/4 W, ± 5%.
5. SHORTING PLUGS INSTALLED.
6. CONNECTOR SYMBOL REFERENCE: ✳ = J1, ▽ = J2, ③ = J3, ④ = J4, ⑤ = J5 & ⑥ = J6.
7. -O-O- INDICATES CUT-TRACE OPTION.
8. -□ □- INDICATES JUMPER OPTION.
9. -□-□-16 INDICATES SHUNT JUMP/CUT-TRACE OPTION.
10. PREFERRED CONFIGURATION: SHORT AF FOR FM, MFM; SHORT NF FOR M²FM.
11. -WW- INDICATES RESISTOR PACK
12. JUMPER OPTION "850/851" IS AS FOLLOWS:
    ASSEMBLY 25201-3 – 850
    ASSEMBLY 25202-3 – JUMPER FOR APPROPRIATE DRIVE MODEL.

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C57	C13, 16
CR2	
L2	
Q2	Q1
R78	R16, 29, 30, 49, 73, 74
TP29	TP3, 4, 8, 9, 14, 15, 19 TO 24
RP2	

USED ON ASSEMBLY
25201-3
25202-3

MUST CONFORM TO ENGINEERING SPEC ES 30000-0		EC HISTORY		TITLE SCHEMATIC DIAGRAM			
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	DATE	NO.				
FINISH	LINEAR ± .XX ± .XXX			DETAIL	SIZE D	RELEASED FOR ASSEMBLY	
CASE DEPTH				DESIGN			
HARDNESS	ANGULAR ±			APPRO		SHEET 1 OF 2	
SURFACE TREATMENT ES	CUTOUT & DRAW OUTSIDE MAX / INSIDE MAX			SCALE D	SIZE CODE SC	PART NO 25202-1	REV C

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LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

1.1 GENERAL DESCRIPTION

The SA850/851 diskette storage drives are enhanced double-headed versions of the standard Shugart SA800/801 drives. SA850/851 drives provide up to four times the on-line storage capacity, faster access time, and lower heat dissipation along with improved reliability and maintainability.

SA850/851 drives read and write in single or double density on standard diskettes and on both sides of two-sided diskettes. The drives are exactly the same size as Shugart SA800/801 drives and are plug compatible. The SA850/851 drives are also media compatible with IBM 3740 and S/32 single-sided drives as well as IBM 4964 and 3600 series two-sided units.

The proprietary Fasflex™ actuator utilizes a flexible metal band for sure low friction head movement and a fast 3 ms track-to-track access time. In addition, Shugart's Bi-Compliant™ read/write head assembly provides superior compliance resulting in excellent data integrity.

Other valuable features include: programmable door lock and write protect plus dual index sensor to differentiate between single and two-sided diskettes.

The SA850/851 will prove highly cost-effective in applications such as: intelligent terminals, minicomputer/microcomputer systems, small business systems as well as word processing systems and intelligent calculators.

Key Features

- Storage capacity of up to four times that of SA800 and other standard floppy drives.
- Single or double density (standard).
- Same physical size as standard SA800/801 product family.
- SA800/801 I/O compatibility.
- Improved access time over standard drives - 3 ms track-to-track.
- Proprietary Fasflex™ actuator.
- Bi-Compliant read/write head assembly.
- Write protect and programmable door lock are standard for improved data security.
- Lower Heat dissipation.
- Improved AC connector.

1.2 SPECIFICATION SUMMARY

1.2.1 PERFORMANCE SPECIFICATIONS

Capacity	Single Density	Double Density
Unformatted		
Per Disk	800 kilobytes	1600 kilobytes
Per Surface	400 kilobytes	800 kilobytes
Per Track	5.2 kilobytes	10.4 kilobytes
IBM Format (128 byte sectors)		
Per Disk	500 kilobytes	1000 kilobytes
Per Surface	250 kilobytes	500 kilobytes
Per Track	3.3 kilobytes	6.66 kilobytes
Transfer Rate	250 kilobits/sec.	500 kilobits/sec.
Latency (Avg.)	83 ms	83 ms
Access Time		
Track to Track	3 ms	3 ms
Average (including settling)	91 ms	91 ms
Settling Time	15 ms	15 ms
Head Load Time	50 ms	50 ms

1.2.2 FUNCTIONAL SPECIFICATIONS

	Single Density	Double Density
Rotational Speed	360 rpm	360 rpm
Recording Density (inside track)	3408 bpi	6816 bpi
Flux Density	6816 fci	6816 fci
Track Density	48 tpi	48 tpi
Cylinders	77	77
Tracks	154	154
Heads	2	2
Physical Sectors		
SA850/R	0	0
SA851/R	32	32
Index	1	1
Encoding Method	FM	MFM/M^{2}FM
Media Requirements		
SA850	SA150/IBM Diskette 2D	SA150/IBM Diskette 2D
SA851	SA151	SA151
Alignment Diskette	SA122	SA122

1.2.3 PHYSICAL SPECIFICATIONS

	Operating	Shipping	Storage
Environment Limits			
Ambient Temperature	40° to 115°F	-40° to 144°F	-8° to 117°F
Relative Humidity	20 to 80%	1 to 95%	1 to 95%
Maximum Wet Bulb	85°F	No condensation	No condensation

AC Power Requirements
50/60 Hz ± 0.5 Hz
100/115 VAC Installations = 85 to 127V @ .35A Max.
200/230 VAC Installations = 170 to 253V @ .25A Max.

DC Voltage Requirements
+24VDC ± 10% 1.0A Max.
+ 5VDC ± 5% 1.1A Max.

Mechanical Dimensions (exlusive of front panel)

	SA850R/851R	SA850/851
Height =	4.62 in. (117 mm)	4.62 in. (117 mm)
Width =	8.55 in. (217 mm)	9.50 in. (241 mm)
Depth =	14.25 in. (362 mm)	14.25 in. (362 mm)

Heat Dissipation	Typical	Maximum
BTU/Hr.	200	245
Watts	60	72

1.2.4 RELIABILITY SPECIFICATIONS

MTBF:	5000 POH under heavy usage. 8000 POH under typical usage.
MTTR:	30 minutes
Component Life:	15,000 POH
Error Rates:	
Soft Read Errors:	1 per 10^9 bits read.
Hard Read Errors:	1 per 10^{12} bits read.
Seek Errors:	1 per 10^6 seeks.
Media Life:	
Passes per Track	3.5×10^6
Insertions:	30,000 +

2.0 FUNCTIONAL CHARACTERISITICS

2.1 GENERAL OPERATION

SA850/851 Diskette Storage Drives consist of read/write and control electronics, drive mechanism, Bi-Compliant read/write heads and a track positioning mechanism. These components perform the following functions:

Interpret and generate control signals.
Move read/write heads to the selected track.
Read and write data.

The Fasflex™ Head Positioning Actuator positions the read/write heads to the desired track on the diskette. The Head Load Solenoid loads the read/write heads against the diskette and data may then be recorded on or read from the diskette.

2.2 READ/WRITE AND CONTROL ELECTRONICS

The electronics are packaged on one PCB. The PCB contains:

1. Index Detector Circuits (Sector/Index for 851)
2. Head Position Actuator Driver.
3. Head Load Solenoid Driver.
4. Read/Write Amplifier and Transition Detector.
5. Data/Clock Separation Circuits (SA851 only).
6. Write Protect
7. Drive Ready Detector Circuit.
8. Drive Select Circuits.
9. Side Select Circuit.
10. In Use and Door Lock Circuits.
11. Write Current Switching/Read Compensation.

2.3 DRIVE MECHANISM

The Diskette drive motor rotates the spindle at 360 rpm through a belt-drive system. 50 or 60 Hz power is accommodated by changing the drive pulley and belt. A registration hub, centered on the face of the spindle, positions the Diskette. A clamp that moves in conjunction with the cartridge guide fixes the Diskette to the registration hub.

2.4 POSITIONING MECHANISM

The read/write heads are accurately positioned by Fasflex™ metal band/stepping motor actuator system. A precision stepping motor is used to precisely position the head/carriage assembly through the use of a unique metal band/capstan concept. Each 3.6° rotation of the stepping motor moves the read/write head one track in discrete increments.

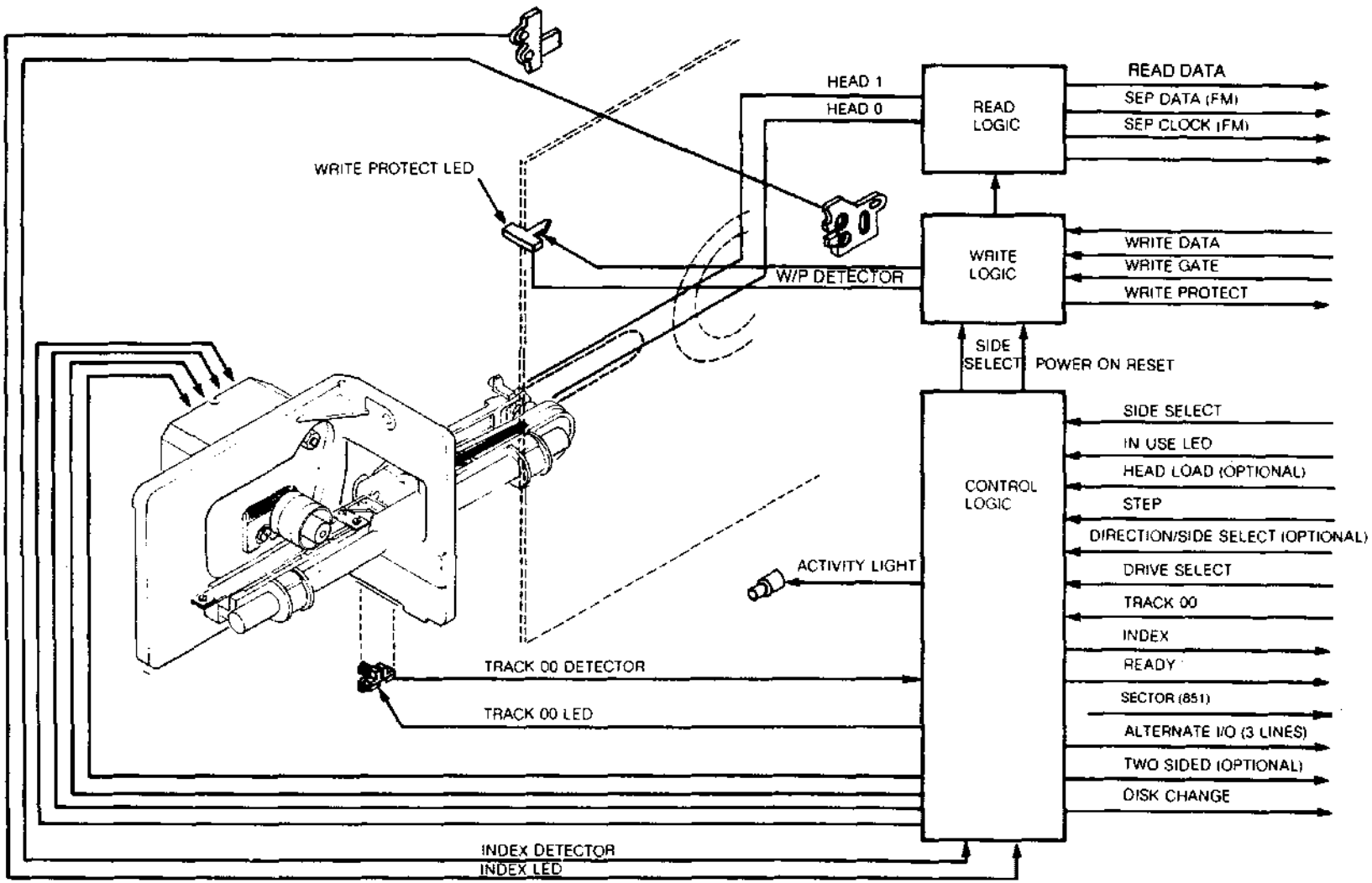


FIGURE 1. SA850/851 FUNCTIONAL DIAGRAM

2.5 READ/WRITE HEADS

The proprietary heads are a single element ceramic read/write head with straddle erase elements to provide erased areas between data tracks. Thus normal interchange tolerances between media and drives will not degrade the signal to noise ratio and insures diskette interchangeability.

The diskette is held in a plane perpendicular to the read/write heads by a platen located on the base casting. This precise registration assures perfect compliance with the read/write heads. The flexure-mounted head is loaded against its rigidly mounted counterpart via the head load solenoid. The read/write heads are in direct contact with the diskette. The head surface has been designed to obtain maximum signal transfer to and from the magnetic surface of the diskette.

3.0 FUNCTIONAL OPERATIONS

3.1 POWER SEQUENCING

Applying AC and DC power to the SA850/851 can be done in any sequence, however, once AC power has been applied, a 2 second delay must be introduced before any Read or Write operation is attempted. This delay is for stabilization of the Diskette rotational speed. Also, after application of DC power, a 90 millisecond delay must be introduced before a Read, Write, or Seek operation or before the control output signals are valid. After powering on, initial position of the read/write heads with respect to data tracks is indeterminable. In order to assure proper positioning of the read/write heads prior to any read/write operation after powering on, a Step Out operation should be performed until the Track 00 indicator becomes active.

3.2 DRIVE SELECTION

Drive selection occurs when a drive's Drive Select line is activated. Only the drive with this line active will respond to input lines or gate output lines. Under normal operation, the Drive Select line will load the read/write head, apply power to the stepper motor, enable the input lines and output lines, light the Activity LED on the front of the drive and lock the door. Optional modes of drive selection are discussed in Section 7.

3.3 TRACK ACCESSING

Seeking the read/write head from one track to another is accomplished by:

a. Activating Drive Select line.

b. Selecting desired direction utilizing Direction Select line.

c. Write Gate being inactive.

d. Pulsing the Step line.

Multiple track accessing is accomplished by repeated pulsing of the Step line until the desired track has been reached. Each pulse on the Step line will cause the read/write heads to move one track either in or out depending on the Direction Select line. Head movement is initiated on the trailing edge of the Step Pulse.

3.3.1 STEP OUT

With the Direction Select line at a plus logic level (2.5V to 5.25V) a pulse on the Step line will cause the read/write heads to move one track away from the center of the disk. The pulse(s) applied to the Step line and the Direction Select line must have the timing characteristics shown in Figure 2.

3.3.2 STEP IN

With the Direction Select line at a minus logic level (0V to .4V), a pulse on the Step line will cause the read/write heads to move one track closer to the center of the disk. The pulse(s) applied to the Step line must have the timing characteristics shown in Figure 2.

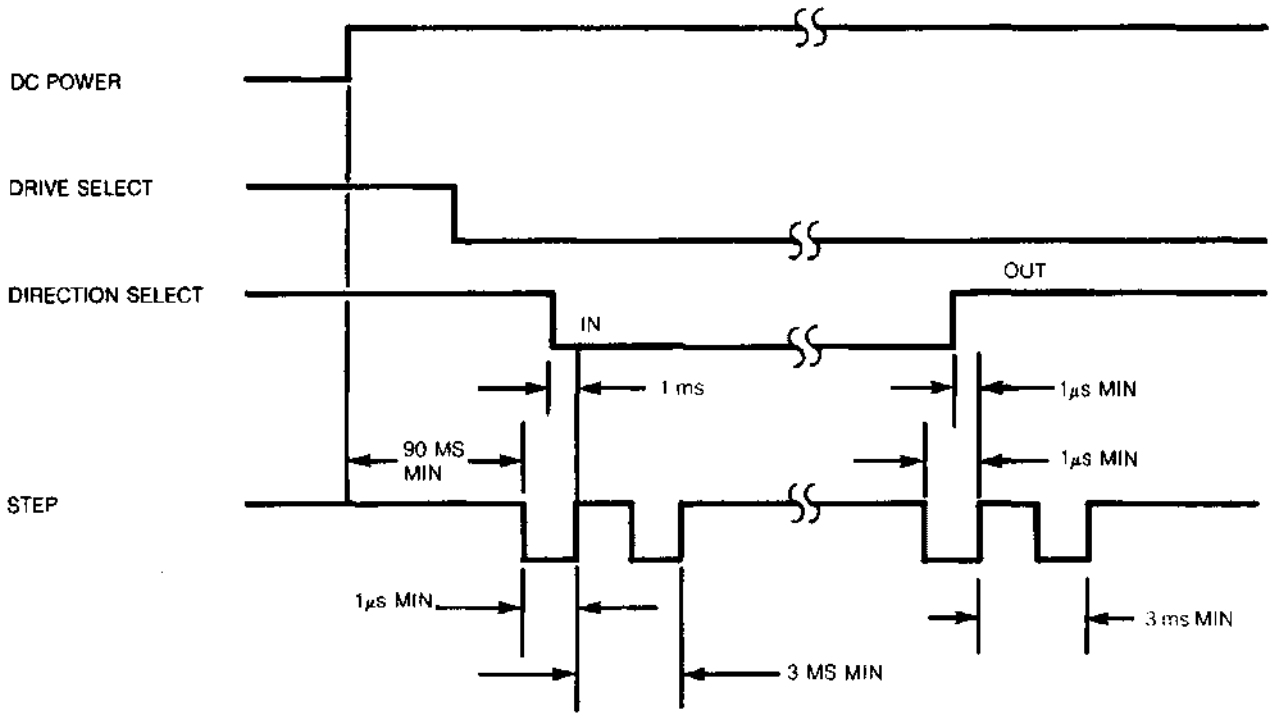
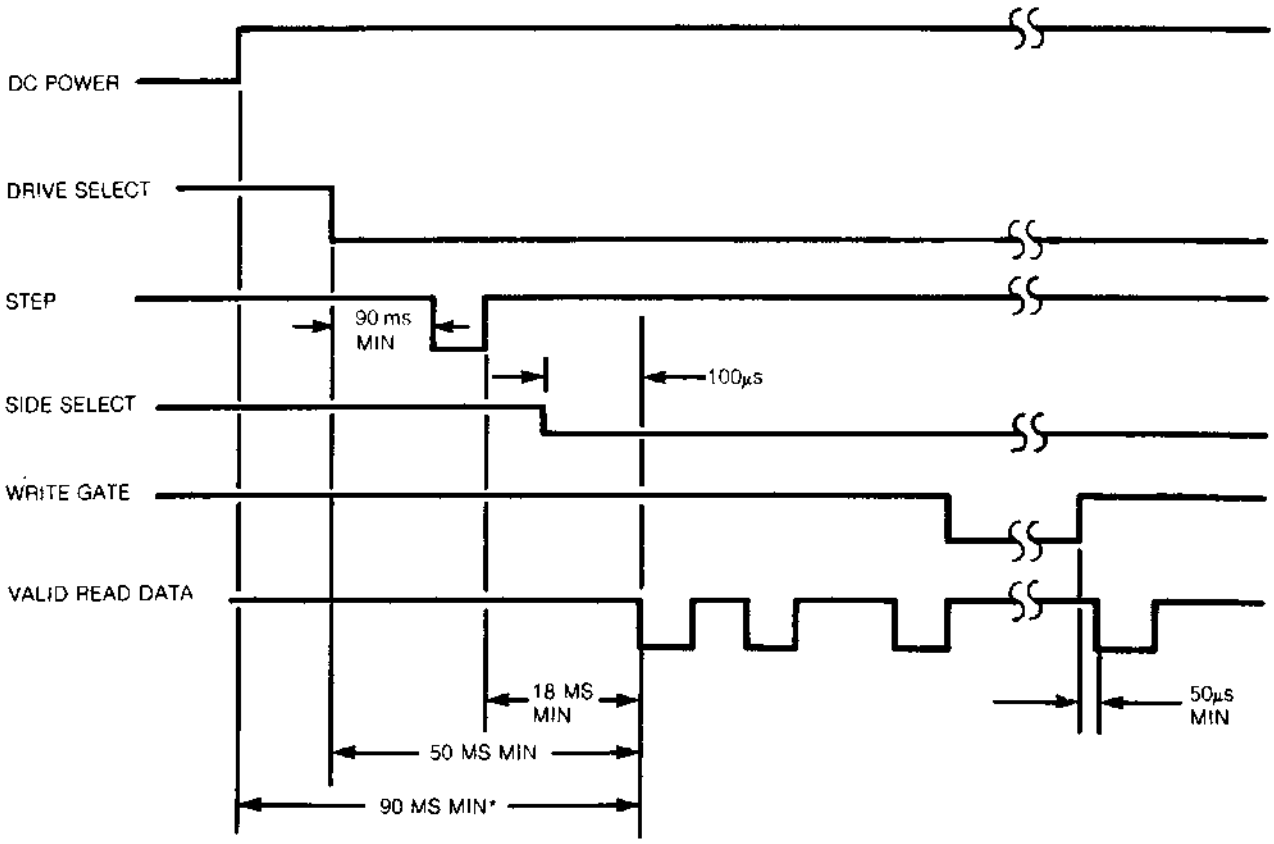


FIGURE 2. TRACK ACCESS TIMING

3.4 SIDE SELECTION

In the standard SA850/851, head selection is controlled via the I/O signal line designated Side select. A plus logic level on the Side Select line selects the read/write head on the side 0 surface of the diskette. A minus logic level selects the side 1 read/write head. When switching from one side to the other, a 100μs delay is required after Side Select changes state before a read or write operation can be initiated. Figure 3 shows the use of Side Select prior to a read operation.

Two jumper-selectable Side Select options are also available. Either of these can be implemented to make use of existing controller and cable harness design. These options are described fully in Section 7.



*2 SECONDS IF AC AND DC POWER ARE APPLIED AT THE SAME TIME

FIGURE 3. READ INITATE TIMING

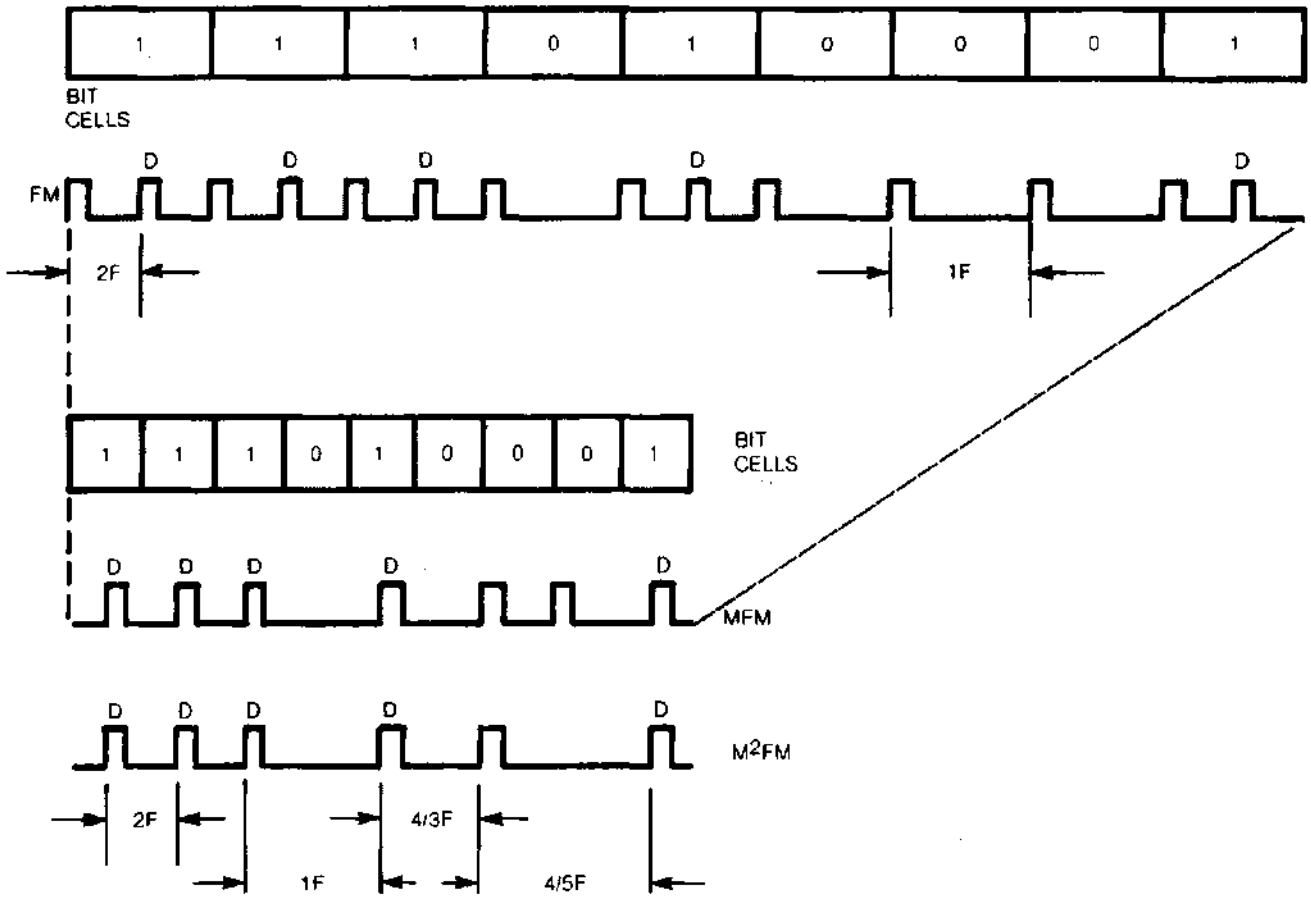
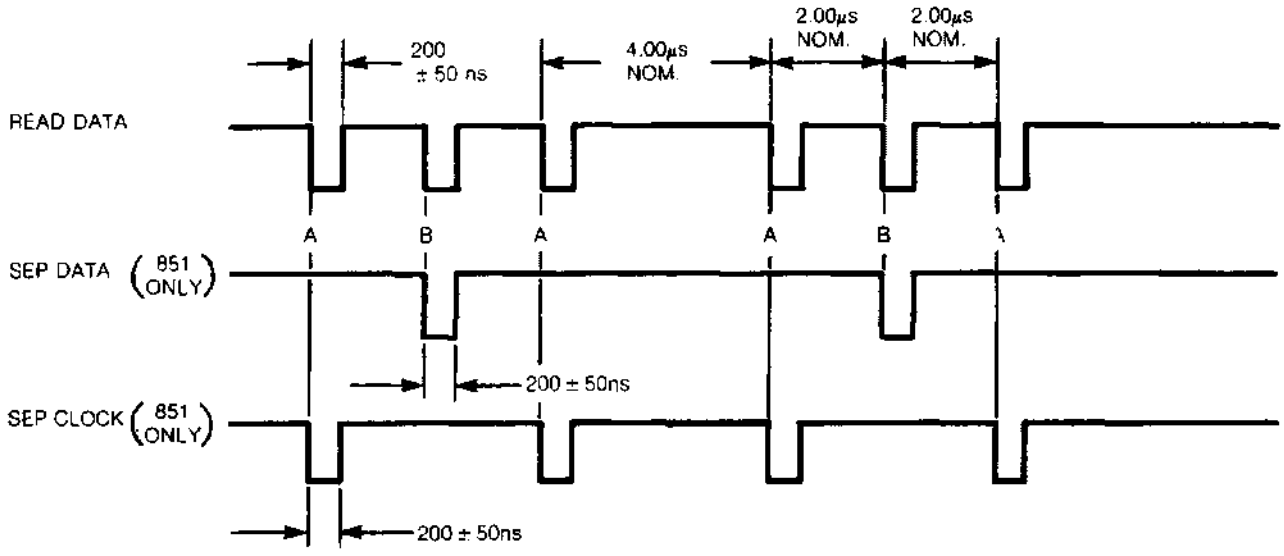


FIGURE 4. FM, MFM AND M²FM CODE COMPARISONS



A = LEADING EDGE OF BIT MAY BE ± 400ns FROM ITS NOMINAL POSITION.
B = LEADING EDGE OF BIT MAY BE ± 200ns FROM ITS NOMINAL POSITION

FIGURE 5. READ SIGNAL TIMING (FM ENCODING)

3.5 READ OPERATION

Reading data from the SA850/851 Diskette Storage drive is accomplished by:

a. Activating Drive Select line.

b. Selecting head.

c. Write Gate being inactive.

The timing relationships required to initiate a read sequence are shown in Figure 3. These timing specifications are required in order to guarantee that the read/write head position has stabilized prior to reading.

The coding scheme of the recorded data can be FM, MFM or M²FM. The first of these, FM, provides single-density recording. The superior efficiency of the other two codes permit their bit cell period to be ½ that of the FM code, thereby providing double-density recording. Differences among FM, MFM and M²FM encoding are concerned with the use of clock bits in the write data stream.

FM encoding rules specify a clock bit at the start of every bit cell. See Figure 4. MFM and M²FM encoding rules allow clock bits to be omitted from some bit cells, with the following prerequisites:

a. MFM - The clock bit is omitted from the current bit cell if either the preceding bit cell or the current bit cell contains a data bit. See Figure 4.

b. M²FM - The clock bit is omitted from the current bit cell if the preceding bit cell contained any bit (clock or data) or if the current bit cell contains a data bit. See Figure 4.

In all three of these encoding schemes, clock bits are written at the start of their respective bit cells and data bits at the center of their bit cells.

The timing of the read signals, Read Data, Separated Data and Separated Clock are shown in Figure 5 (FM encoding).

In the standard SA851, data separation of FM data is performed by the drive electronics. Data bits are presented to the controller on the Sep Data line and clock bits are presented on the Sep Clock line. In systems using the SA850 or when MFM/M²FM encoding is used, data separation is performed outside the drive. IN such cases, the Read Data line carries both clock bits and data bits. Separation is MFM or M²FM encoded read data should be controlled by a phase-locked loop oscillator (PLO) circuit.

For additional information regarding the use of MFM and M²FM encoding with SA850/851 drives, refer to Shugart Associates' Double Density Design Guide.

3.6 WRITE OPERATION

Writing data to the SA850/851 is accomplished by:

a. Activating the Drive Select line.

b. Selecting head.

c. Activating the Write Gate line.

d. Pulsing the Write Data line with the data to be written.

e. Head Current switching.

The timing relationships required to initiate a write data sequence are shown in Figure 6. These timing specifications are required in order to guarantee that the read/write head position has stabilized prior to writing.

Write data encoding can be FM, MFM or M^{2}FM. If either double-frequency encoding scheme is used (MFM or M^{2}FM) the write data should be precompensated to counter the effects of bit shift. The amount and direction of compensation required for any given bit in the data stream depends on the pattern it forms with nearby bits.

For more details regarding data encoding and formatting for SA850/851 drives, refer to Shugart Associates' Double Density Design Guide.

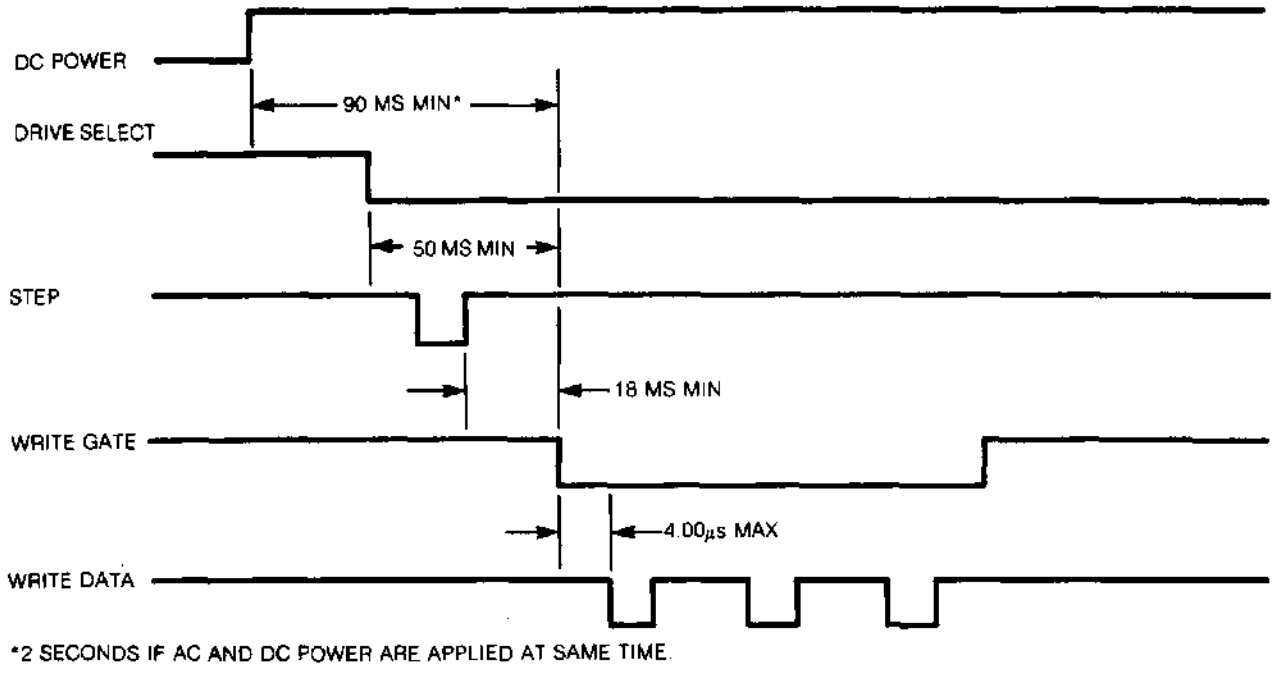


FIGURE 6. WRITE INITIATE TIMING

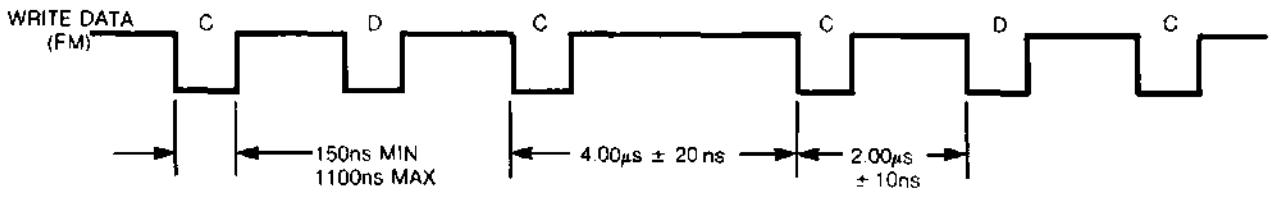
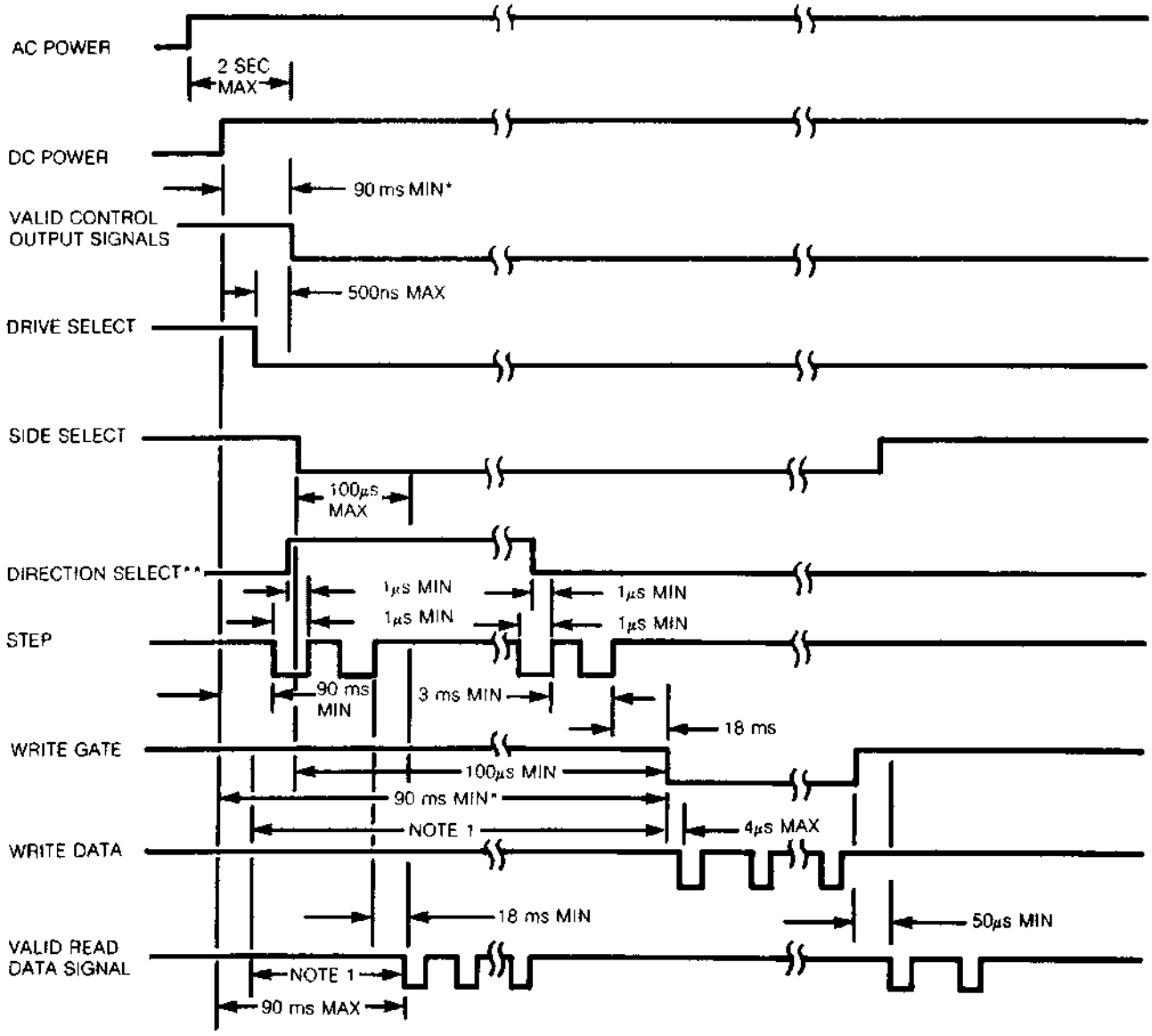


FIGURE 7. WRITE DATA TIMING (FM ENCODING)

3.7 SEQUENCE OF EVENTS

The timing diagram shown in Figure 8 shows the necessary sequence of events with associated timing restrictions for proper operation.

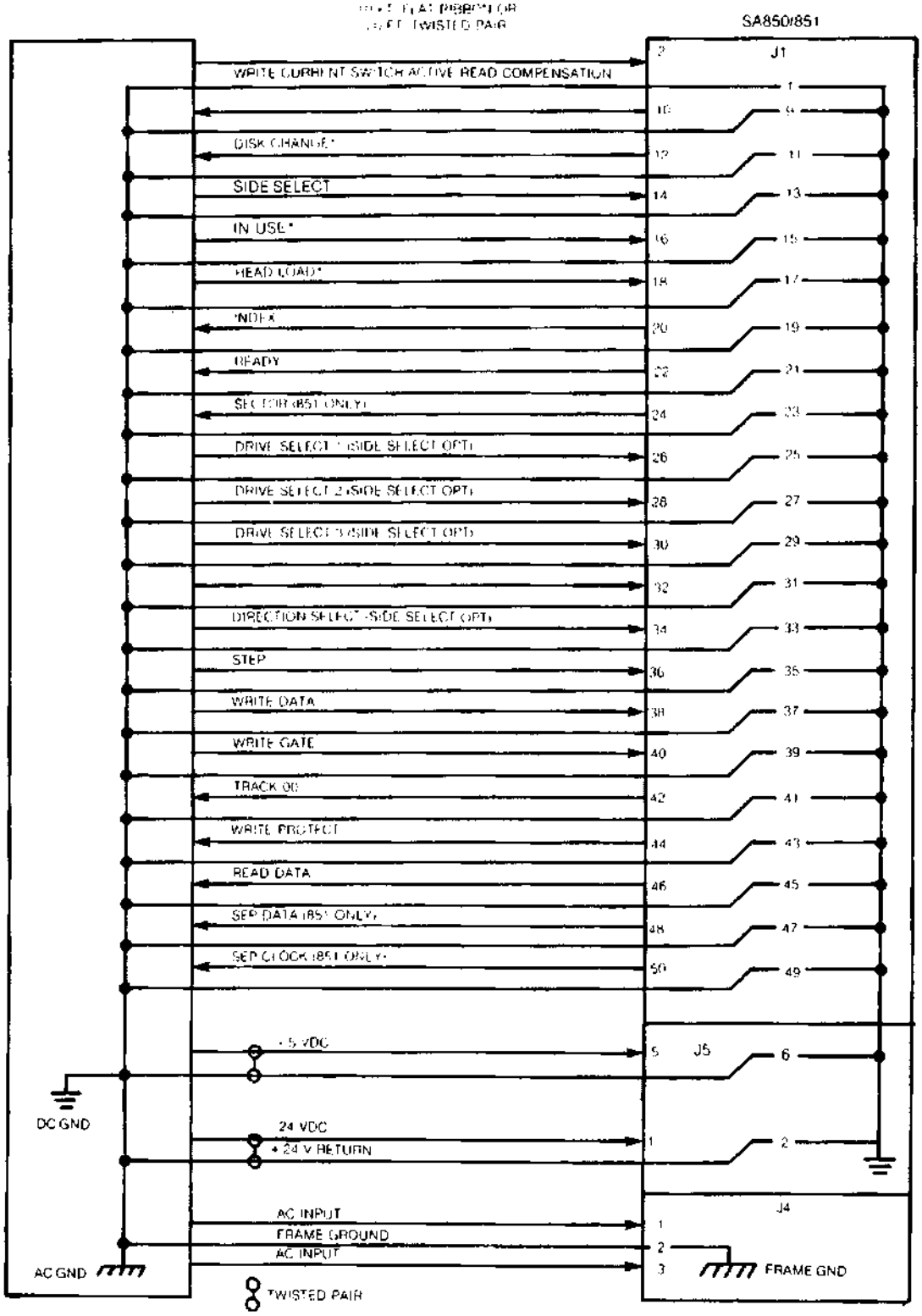


*2 SECONDS IF AC AND DC POWER ARE APPLIED AT SAME TIME.

**WHEN CHANGING DIRECTION ON THE HEAD A 15 MS DELAY MUST BE INTRODUCED.

NOTE 1 50 ms minimum delay must be introduced after Drive Select to allow for proper head load settling. If stepper power is to be applied independent of Head Load, then a 15 ms minimum delay must be introduced to allow for stepper settling. See section 7 on optional customer installable features.

FIGURE 8. GENERAL CONTROL AND DATA TIMING REQUIREMENTS



* These lines are alternate input/output lines and they are enabled by jumper plugs. Reference Section 7 for uses of these lines. Not shown are pins 4, 6 and 8 which are alternate I/O pins.

FIGURE 9. INTERFACE CONNECTIONS

4.0 ELECTRICAL INTERFACE

The interface of the SA850/851 Diskette drive can be divided into two categories:

1. Signal
2. Power

The following sections provide the electrical definition for each line.

Reference Figure 9 for all interface connections.

4.1 SIGNAL INTERFACE

The signal interface consists of two categories:

1. Control
2. Data transfer

All lines in the signal interface are digital in nature and either provide signals to the drive (input), or provide signals to the host (output), via interface connector P1/J1.

4.1.1 INPUT LINES

There are thirteen (13) signal input lines, ten (10) are standard and three (3) are user installable options (reference section 7).

The input signals are of two types, those intended to be multiplexed in a multiple drive system and those which will perform the multiplexing. The input signals to be multiplexed are:

1. Direction Select
2. Step
3. Write Data
4. Write Gate
5. Side Select
6. Head Current Switch/Active Read Compensation
7. In Use
8. Head Load

The input signals which are intended to do the multiplexing are:

1. Drive Select 1
2. Drive Select 2
3. Drive Select 3
4. Drive Select 4

The input circuit lines have the following electrical specifications. Reference Figure 10 for the recommended circuit.

True = Logical zero = Vin ± 0.0V to +0.4V @ Iin = 40 ma (max)

False = Logical one = Vin + 2.5V to +5.25V @ Iin = 250μa (open)

Input Impedance = 150 ohms

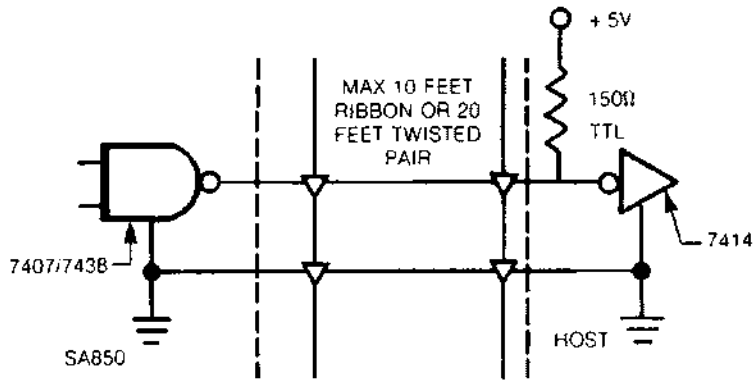


FIGURE 10. INTERFACE SIGNAL DRIVER/RECEIVER

4.1.1.1 INPUT LINE TERMINATION

The SA850/851 has been provided with a removable resistor pack for terminating the seven input lines that are to be multiplexed.

In order for the drive to function properly, the last drive on the interface must have these seven lines terminated. Termination of these lines can be accomplished by either of two methods.

1. As shipped from the factory, the resistor pack is installed in location 5E. These packs can be removed from all drives except the last one on the Inteface.

2. External termination may be used provided the terminator is beyond the last drive. Each of the five lines should be terminated by using a 150 ohm, ¼ watt resistor, pulled up to +5VDC.

The same removable resistor pack is also provided for terminating the optional input lines.

4.1.1.2 DRIVE SELECT 1 - 4

Drive Select when activated to a logical zero level, activates the multiplexed I/O lines and loads the read/write head. In this mode of operation only the drive with this line active will respond to the input lines and gate the output lines.

Four separate input lines, Drive Select 1, Drive Select 2, Drive Select 3, and Drive Select 4, are provided so that up to four drives may be multiplexed together in a system and have separate Drive Select lines. Traces 'DS1', 'DS2', 'DS3', and 'DS4' have been provided to select which Drive Select line will activate the interface signals for a unique drive. As shipped from the factory, a shorting plug is installed on 'DS1'. To select another Drive Select line, this plug should be moved to the appropriate 'DS' pin.

4.1.1.3 SIDE SELECT

This interface line defines which side of a two-sided diskette is used for reading or writing. An open circuit, or logical one, selects the read/write head on the side 0 surface of the diskette. A short to ground, or logical zero, selects the read/write head on the diskette's side 1 surface. When switching from one head to the other, a 100μs delay is required before any read or write operation can be initiated.

Two optional methods of side selection are available and can be implemented by the user through appropriate jumper connections. These options are described in Sections 7.9 and 7.10.

4.1.1.4 DIRECTION SELECT

This interface line is a control signal which defines direction of motion the read/write heads will take when the Step line is pulsed. An open circuit or logical one defines the direction as "out" and if a pulse is applied to the Step line the read/write heads will move away from the center of the disk. Conversely, if this input is shorted to ground or a logical zero level, the direction of motion is defined as "in" and if a pulse is applied to the step line, the read/write heads will move towards the center of the disk.

A jumper-selectable option is available, which allows the Direction Select line to be time shared for both the Direction Select and Side Select functions. That is, during head positioning operations, the Direction Select line controls direction of head motion and during read or write operations, the Direction Select line determines which head is selected. Details regarding the implementation of this option are provided in Section 7.9.

NOTE: A 15ms delay must be introduced when changing direction (i.e., the last step in pulse to first step out-pulse or vice versa).

4.1.1.5 STEP

This interface line is a control signal which causes the read/write heads to move with the direction of motion as defined by the Direction Select line.

The access motion is initiated on each logical zero to logical one transition, or the trailing edge of the signal pulse. Any change in the Direction Select line must be made at least 1μs before the trailing edge of the Step pulse. Refer to Figure 2 for these timings.

4.1.1.6 WRITE GATE

The active state of this signal (logical zero) enables Write Data to be written on the diskette. The inactive state (logical one) enables the read data logic (Separated Data, Separated Clock, and Read Data) and stepper logic. Refer to Figure 6 for Write Initiate timing information.

4.1.1.7 WRITE DATA

This inteface lines provides the data to be written on the diskette. Each transition from a logical one level to a logical zero level will cause the current through the read/write head to be reversed, thereby writing a data bit. This line is enabled by Write Gate being active. Refer to Figure 7 for timing information.

4.1.1.8 HEAD LOAD (ALTERNATE INPUT)

This customer installable option, when enabled by jumpering Trace "C" and activated to a logical zero level and the diskette access door is closed, will load the read/write heads against the diskette. Refer to section 7.15for uses and method of installation.

4.1.1.9 IN USE (ALTERNATE INPUT)

This customer installable option, when enabled by jumpering Trace "D" and activated to a logical zero level will turn on the Activity LED in the door push button and will lock the door. This signal is an "OR" function with Drive Select. Refer to section 7.6 for uses and method of installation.

4.1.1.10 WRITE CURRENT SWITCH/ACTIVE READ COMPENSATION

Reference section 7.13

4.1.2 OUTPUT LINES

There are five standard output lines from the SA850, and eight standard output lines from the SA851. Also, there are two optional output lines and three alternate outputs available from either the SA850 or SA851. The output signals are driven with an open collector output stage capable of sinking a maximum of 40 ma at a logical zero level or true state with a maximum voltage of 0.4V measured at the driver. When the line driver is in a logical one or false state, the driver is off and the collector current is a maximum of 250 microampers.

Refer to Figure 10 for the recommended circuit.

4.1.2.1 TRACK 00

The active state of this signal, or a logical zero indicates when the drive's read/write heads are positioned at track zero (the outermost track) and the access circuitry is driving current through phase one of the stepper motor. This signal is at a logical one level, or false state, when the selected drive's read/write heads are not at track 00.

4.1.2.2 INDEX

This interface signal is provided by the drive once each revolution of the diskette (166.67 ms) to indicate the beginning of the track. Normally this signal is a logical one and makes the transition to the logical zero level for a period of 1.8 ms (0.4 ms on SA851) once each revolution. The timing for this signal is shown in Figure 11.

To correctly detect Index at the control unit, Index should be false at Drive Select time; that is, the controller should see the transition from false to true after the drive has been selected.

For additional methods of detecting Index, refer to section 7.5.

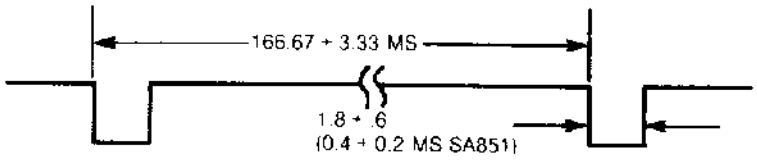


FIGURE 11. INDEX TIMING

4.1.2.3 SECTOR (SA851 only)

This interface signal is provided by the drive 32 times each revolution. Normally, this signal is a logical one and makes the transition to a logical zero for a period of 0.4 ms each time a sector hole on the Diskette is detected. Figure 12 shows the timing of this signal and its relationship to the Index pulse.

NOTE: Index/Sector pulses should not be used for loading the Read/Write heads as this may cause unusual media wear in one spot on the diskette.

4.1.2.4 READY

This interface signal indicates that two index holes have been sensed after properly inserting a diskette and closing the door, or that two index holes have been sensed following the application of + 5V power to the drive. Three holes have to be sensed for two sided diskettes.

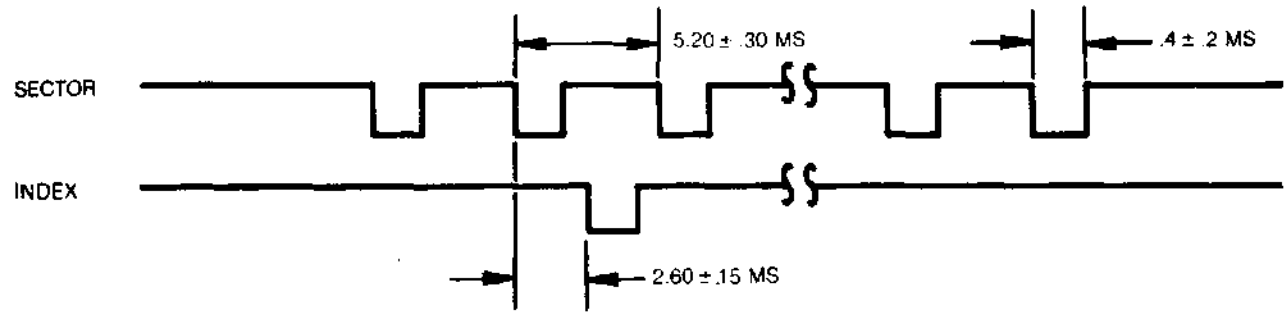


FIGURE 12. SECTOR TIMING

If a single sided diskette is installed, READY will be active (logical zero) if SIDE 0 is selected, but false (logical 1) if SIDE 1 is selected. Conversely, if a two-sided diskette is installed, READY will be active when either side of the diskette is selected.

For additional methods of using the Ready line, refer to section 7.4.

4.1.2.5 READ DATA

This interface line provides the "raw data" (clock and data together) as detected by the drive electronics. Normally, this signal is a logical one level and becomes a logical zero level for the active state. Reference Figure 5 for the timing and bit shift tolerance within normal media variations.

4.1.2.6 SEP DATA (SA851 only)

This interface line furnishes the data bits as separated from the "raw data" by use of the internal data separator. Normally, this signal is a logical one level and becomes a logical zero level for the active state. Reference Figure 5 for the timing

4.1.2.7 SEP CLOCK (SA851 only)

This interface line furnishes the clock bits as separated from the "raw data" by use of the internal data separator. Normally, this signal is a logical one level and becomes a logical zero level for the active state. Reference Figure 5 for the timing.

4.1.2.8 WRITE PROTECT

This interface signal is provided by the drive to give the user an indication when a Write Protected Diskette is installed. The signal is a logical zero level when it is protected. Under normal operation, the drive will inhibit writing with a protected diskette installed in addition to notifying the interface.

For other methods of using Write Protect, refer to section 7.7

4.1.2.9 DISK CHANGE (OPTIONAL OUTPUT)

Reference section 7.8.

4.1.2.10 TWO SIDED (OPTIONAL OUTPUT)

Reference section 7.12.

4.1.3 ALTERNATE I/O PINS

These interface pins have been provided for use with customer installable options. Refer to section 7 for methods of use.

4.2 POWER INTERFACE

The SA850/851 Diskette Storage Drive requires both AC and DC power for operation. The AC power is used for the spindle drive motor and the DC power is used for the electronics and the stepper motor.

4.2.1 AC POWER

The AC power to the drive is via the connector P4/J4 located to the rear of the drive and below the AC motor capacitor. The P4/J4 pin designations are outlined in Table 1 for standard as well as optional AC power.

P4 PIN	60 Hz		50 Hz	
	115 V (Standard)	208/230 V	110V	220V
1	85-127 VAC	170-253 VAC	85-127 VAC	170-253 VAC
2	Frame Gnd	Frame Gnd	Frame Gnd	Frame Gnd
3	85-127 V Rtn	170-253 V Rtn	85-127 V Rtn	170-253 V Rtn
MAX CURRENT	0.35 Amps	0.25 Amps	0.35 Amps	0.25 Amps
FREQ TOLERANCE	±0.5 Hz		±0.5 Hz	

TABLE 1

4.2.2 DC POWER

DC power to the drive is via connector P5/J5 located on the non-component side of the PCB near the P4 connector. The two DC voltages and their specifications along with their P5/J5 pin designators, are outlined in Table 2.

P5 PIN	DC VOLTAGE	TOLERANCE	CURRENT	MAX RIPPLE (p to p)
1	+24 VDC	±2.4 VDC	1.0A Max* 0.85A Typ	100 mv
2	+24 V Return			
6	+5 V Return			
5	+5 VDC	±0.25 VDC	1.1A Max 1.0A Typ	50 mv

*If either customer installable option described in sections 7.1 and 7.3 are used, the current requirement for the +24-VDC is a multiple of the maximum +24V current times the number of drives on the line.

TABLE 2

5.0 PHYSICAL INTERFACE

The electrical interface between the SA850/851 and the host system is via three connectors. The first connector, J1, provides the signal interface; the second connector, J5, provides the DC power; and the third connector, J4, provides the AC power and frame ground.

This section describes the physical connectors used on the drive and the recommended connectors to be used with them. Refer to Figure 16 for connector locations.

5.1 J1/P1 CONNECTOR

Connection to J1 is through a 50 pin PCB edge card connector. The dimensions for this connector are shown in Figure 13. The pins are numbered 1 through 50 with the even numbered pins on the component side of the PCB and the odd numbered pins on the non-component side. Pin 2 is located on the end of the PCB connector closest to the AC motor capacitor and is labeled 2. A key slot is provided between pins 4 and 6 for optional connector keying.

The recommended connectors for P1 are tabulated below.

TYPE OF CABLE	MANUFACTURER	CONNECTOR P/N	CONTACT P/N
Twisted Pair, #18 (crimp or solder)	AMP	1-583718-1	583616-5 (crimp) 583854-3 (solder)
Twisted Pair, #18 (solder term.)	VIKING	3VH25/1JN-5	NA
Flat Cable	3M "Scotchflex"	3415-0001	NA

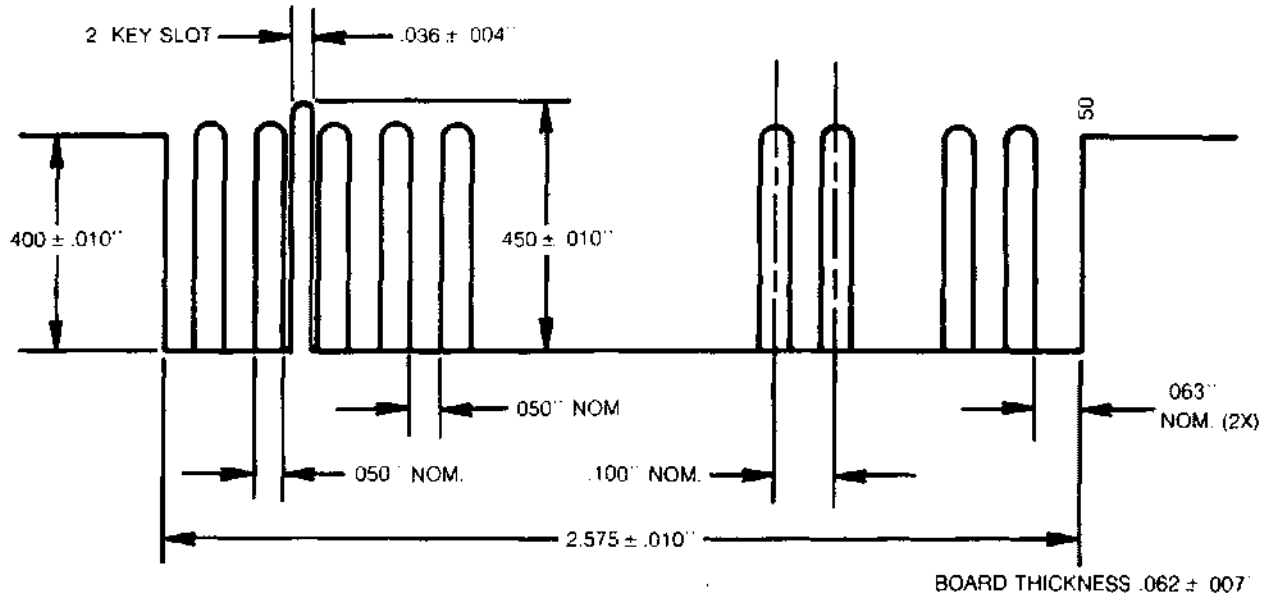


FIGURE 13. J1 CONNECTOR DIMENSIONS

5.2 J5/P5 CONNECTOR

The DC power connector, J5, is mounted on the non-component side of the PCB and is located below the AC motor capacitor. J5 is a 6 pin AMP Mate-N-Lok connector P/N 1-380999-0. The recommended mating connector (P5) is AMP P/N 1-480270-0 utilizing AMP pins P/N 60619-1. J5 pins are labeled on the component side of the PCB with pin 5 located nearest J1/P1. Figure 14 illustrates J5 connector as seen on the drive PCB from non-component side.

5.3 J4/P4 CONNECTOR

The AC power connector, J4, is mounted on the AC motor capacitor bracket and is located just below the capacitor. J4 connector is a 3 pin connector AMP P/N 1-480701-0 with pins P/N 350687-1, 2 EA. and 350654-1, 1 EA. The recommended mating connector (P4) is AMP P/N 1-480700-0 utilizing pins 350550-1. Figure 15 illustrates J4 connector as seen from the rear of the drive.

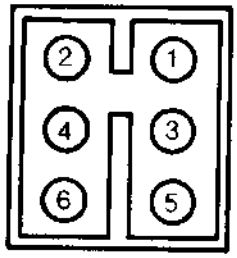


FIGURE 14. J5 CONNECTOR

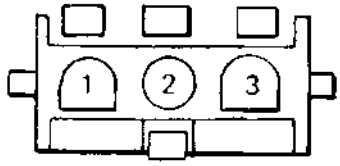


FIGURE 15. J4 CONNECTOR

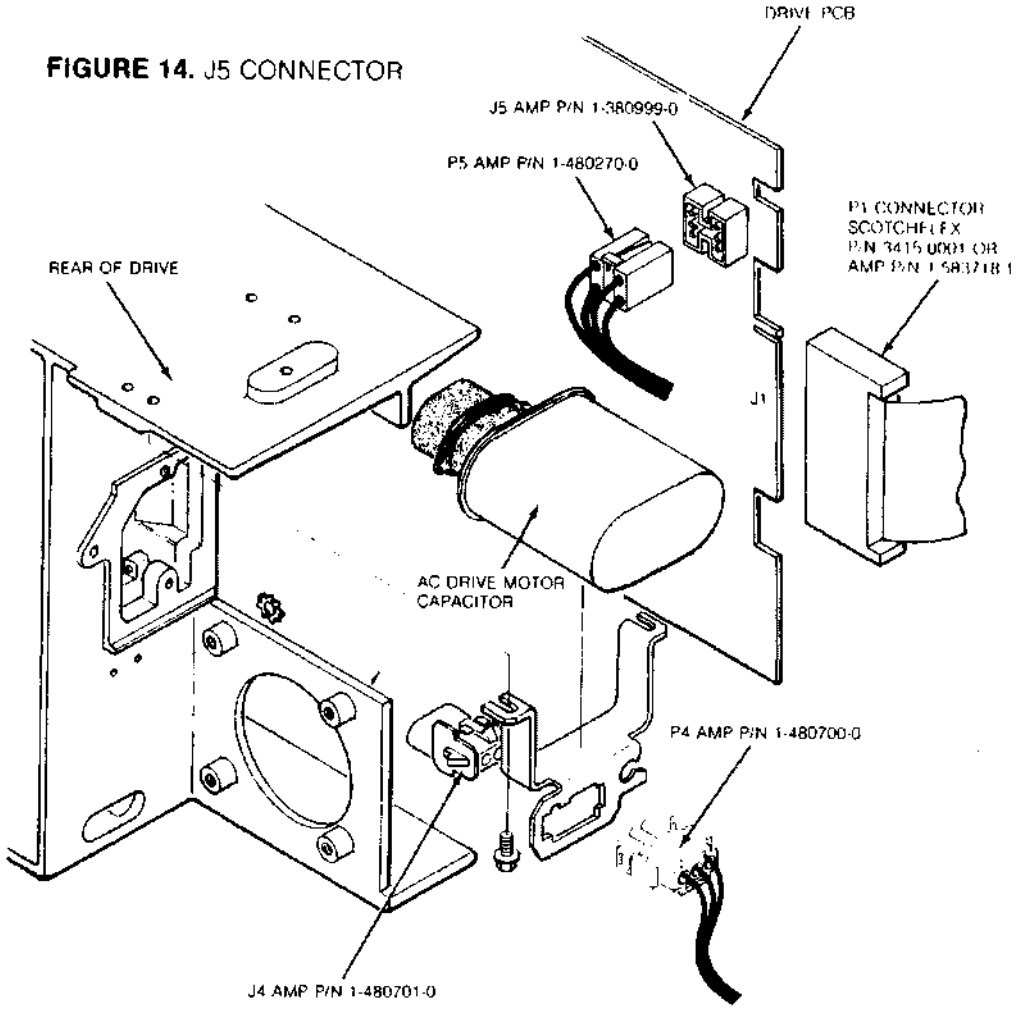


FIGURE 16. INTERFACE CONNECTOR-PHYSICAL LOCATION DIAGRAM

6.0 DRIVE PHYSICAL SPECIFICATIONS

This section describes the mechanical dimensions and mounting recommendations for the SA850/851.

6.1 DRIVE DIMENSIONS

Reference Figure 18 and 19 for dimensions of the SA850/851.

6.2 MOUNTING RECOMMENDATIONS

The SA850/851 is capable of being mounted in one of the following positions (refer to Figure 17):

1. Vertical - Door opening to the left or right.
2. Horizontal - Door opening up (PCB down).
3. Upright - To mount the drive in this position remove the spring hook attached to the eject mechanism and attach the eject spring to the post the spring hook was attached to.

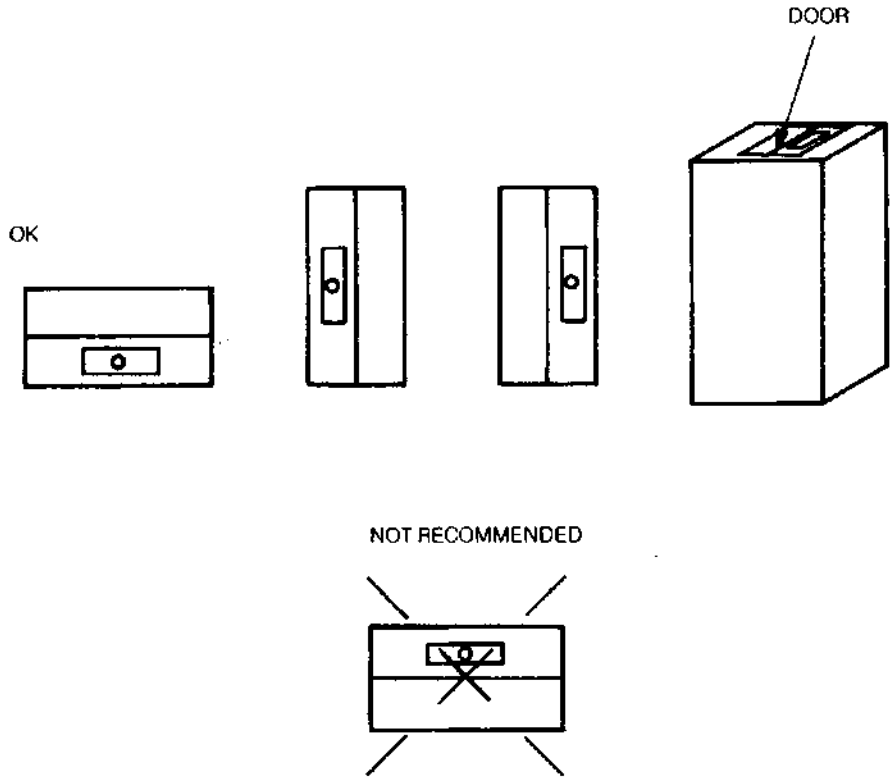


FIGURE 17. RECOMMENDED MOUNTING

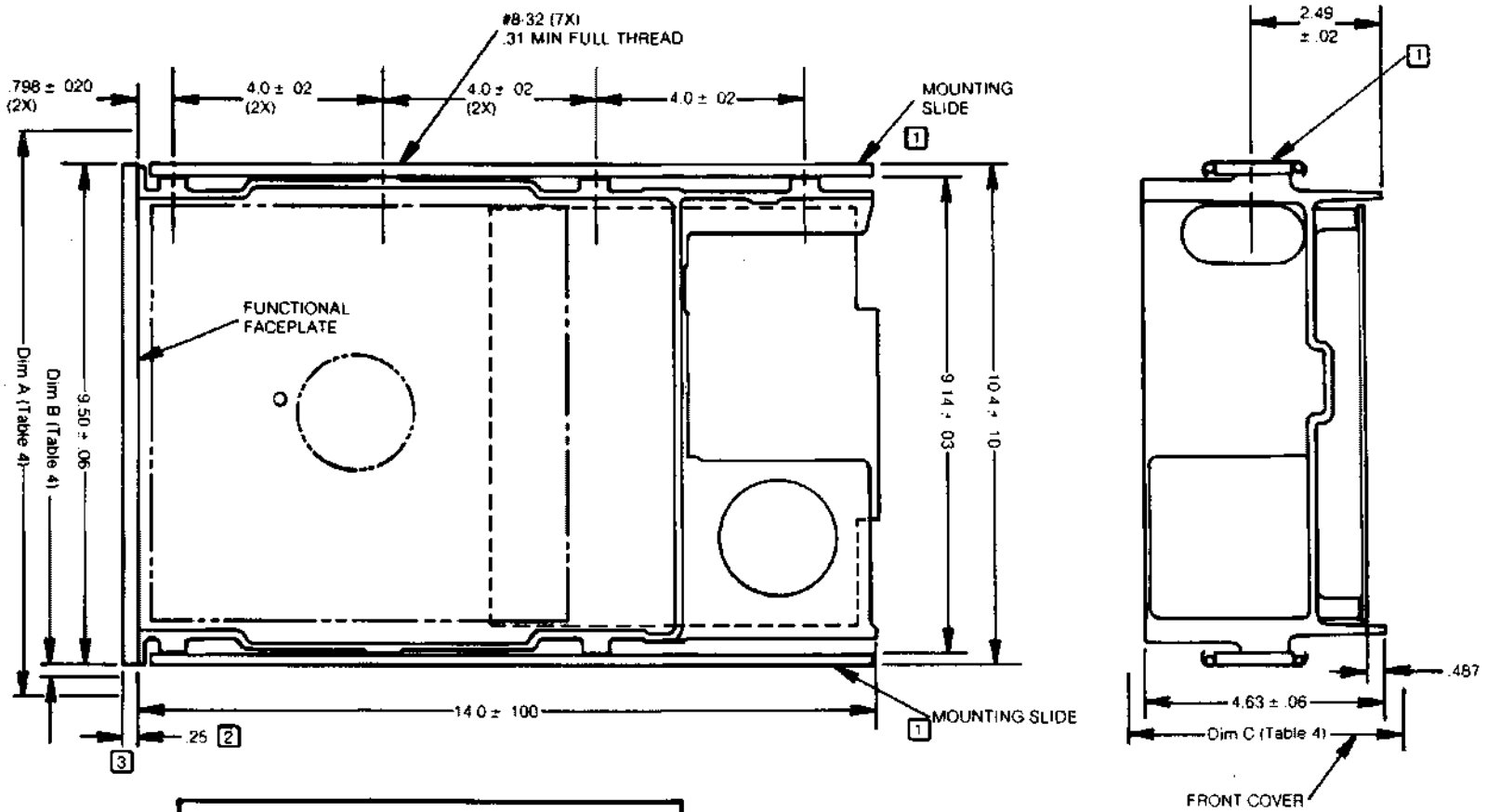


FIGURE 18. SA850/851 DISKETTE STORAGE DRIVE DIMENSIONS

Decorative Cover Dimensions			
Cover Size	Dim A	Dim B	Dim C
4-5/8 × 10-1/2	10.50	240	4.62
5-1/4 × 10	10.00	240	5.25
5-1/4 × 11	11.00	.740	5.25
Tolerance	± .03	± .030	± .03

1. If drive is mounted on slides, drive will extend 14 inches from operating position for servicing.
2. With cosmetic cover this dimension is .38".
3. Handle extend .375" beyond faceplate.
4. All dimensions are in inches.

1 Dimension is from end of base casting.

2 Comestic front cover height.

3 Functional front plate height

4 Cosmetic front cover width.

5 Functional front plate width.

6 Cosmetic front cover thickness.

7 Functional front plate thickness.

8 Cosmetic front cover color comes only in tan.

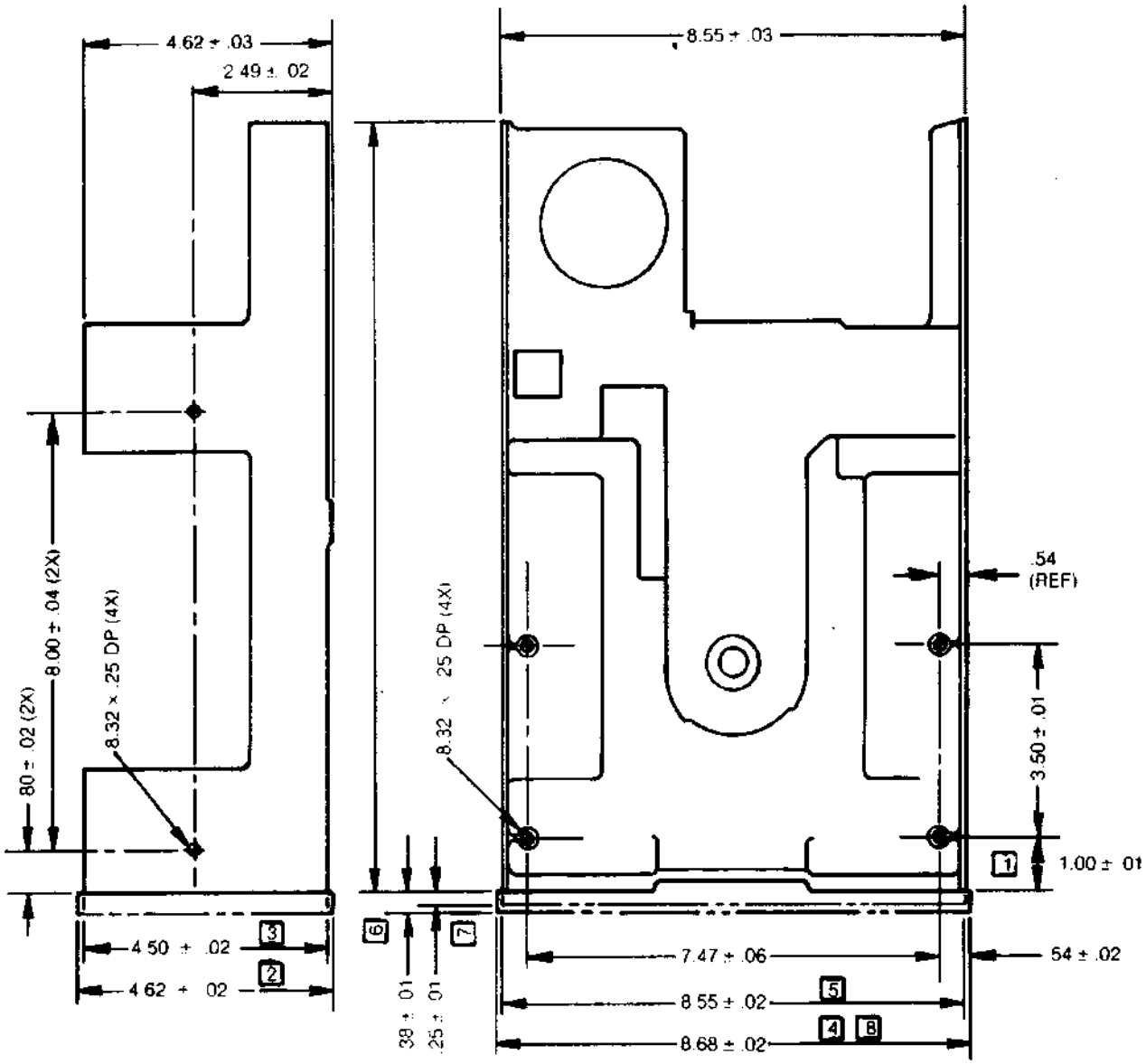
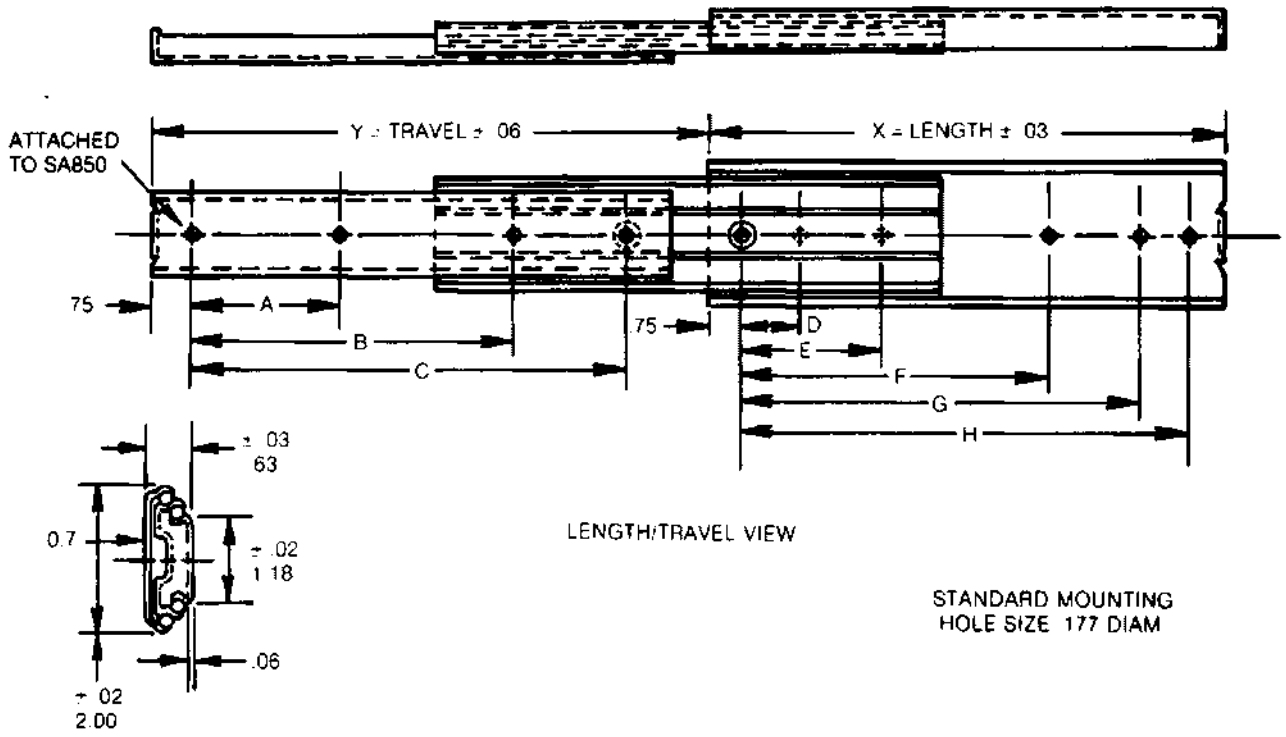


FIGURE 19. SA850/851R DIMENSIONS

6.3 CHASSIS SLIDE

Available as an optional accessory is a chassis slide kit P/N 50239. This kit contains two slides, one locking and one non-locking, and seven screws. Dimensions of the slide are shown in Figure 19.



X	Y	A	B	C	D	E	F	G	H
14	15	4.00	8.00	12 00	1.00	3.50	8.50	11.50	12.50

FIGURE 20. SLIDE MOUNTING DIMENSIONS

6.4 DECORATIVE FACE PLATE

The SA850/851 may be ordered with one of the following decorative face plates:

SIZE	COLOR
4 5/8 × 10 1/2	Tan
4 5/8 × 10 1/2	White
5 1/4 × 10	Tan
5 1/4 × 10	White
5 1/4 × 11	Tan
5 1/4 × 11	White
"R" Series-4 5/8 × 8 11/16	Tan

If another color is required to match the system's color scheme, the face plate may be painted. The following information should be utilized to avoid potential problems in the painting process.

1. The front cover is made from GE's LEXAN. Dimensional stability of LEXAN is from -60°F to + 250°F. If the paint used requires baking, the temperature should not exceed + 250°F, including any hot spots which can contact the cover.

2. LEXAN is a polycarbonate. Any paint to be used should be investigated to insure that it does not contain chemicals that are solvents to polycarbonates.

7.0 CUSTOMER INSTALLABLE OPTIONS

The SA850/851 can be modified by the user to function differently than the standard method as outlined in sections 3 and 4. These modifications can be implemented by adding or deleting connections and by use of the Alternate I/O pins. Some options are capable or being connected by use of a shorting plug, Shugart P/N 15648 or AMP P/N 53013-2. This section will discuss a few examples of modifications and how to install them. The examples are:

1. Select drive without loading head or enabling stepper.
2. Select drive and enable stepper without loading head.
3. Load head without selecting drive or enabling stepper.
4. Radial Ready.
5. Radial Index/Sector.
6. In Use (Activity LED) optional input.
7. Write Protect options.
8. Side selection.
9. Write Current Switch.
10. Ready Standard/Ready Modified.
11. Head Load Latch.
12. Active Read Compensation Filter.

CUSTOMER CUT/ADD TRACE OPTIONS

TRACE DESIGNATOR	DESCRIPTION	SHIPPED FROM FACTORY	
		OPEN	SHORT
5E	Terminations for Multiplexed Standard Inputs		Plugged
DS1	Drive Select 1 Input Pin		Plugged
DS2,3,4	Drive Select 2,3,4 Input Pins	X	
1B,2B,3B,4B	Side Select Option Using Drive Select	X	
RR	Radial Ready		X
RI	Radial Index and Sector		X
R (SHUNT 4F)*	Option Shunt for Ready Output		X
2S	Two-Sided Status Output	X	
850/851	Sector Option Enable	850	851
I (SHUNT 4F)*	Index Output		X
S (SHUNT 4F)*	Sector Output		X
DC	Disk Change Option	X	
HL (SHUNT 4F)*	Stepper Power From Head Load		X
DS	Stepper Power From Drive Select	X	
WP	Inhibit Write When Write Protected		X
NP	Allow Write When Write Protected	X	
D	Alternate Input-In Use	X	
M	Multi-Media Option		Plugged
DL	Door Lock Latch Option		X
A,B,X.(SHUNT 4F)*	Radial Head Load		X
C	Alternate Input-Head Load	X	
Z (SHUNT 4F)*	In Use From Drive Select		X
Y	In Use From Head Load	X	
S1	Side Select Option Using Direction Select	X	
S2	Standard Side Select Input		Plugged
S3	Side Select Option Using Drive Select	X	
TS, FS**	Data Separation Option Select	TS	FS Plugged
IW	Write Current Switch		Plugged***
RS	Ready Standard		Plugged
RM	Ready Modified	X	
HLL	Head Load Latch	X	
IT	In Use Terminator		Plugged
HI	Head Load or In Use to the In Use Circuit	X	
F****.	Remove for MFM encoding install for M²FM	X	
AF*****	Install for FM or MFM encoding		Plugged
NF*****	Install for M²FM encoding.	X	

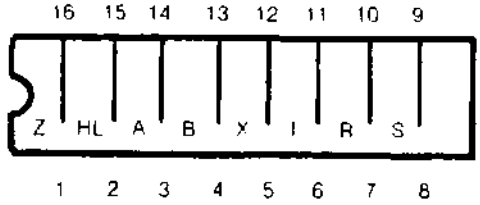
*A 16 pin programmable shunt Shugart P/N 15658 (location 4F) is provided for the eight most commonly used cut track options. These traces are usually shorted as shipped from the factory. The traces can be opened as follows:

1. Cut the trace using a Strap Cutter AMP P/N 435705.

**The SA851 offers a standard data separator, as in the SA801, and an optional data separator which properly separates data and clock bits through the soft-sectored IBM standard format and address mark area. Trace "FS" offers the standard separator and Trace "TS" offers the optional separator. Either separator may be selected through a shorting plug.

***Write current switch is plugged to the interface

****MLC 10 ONLY.
*****MLC 11 ONLY.



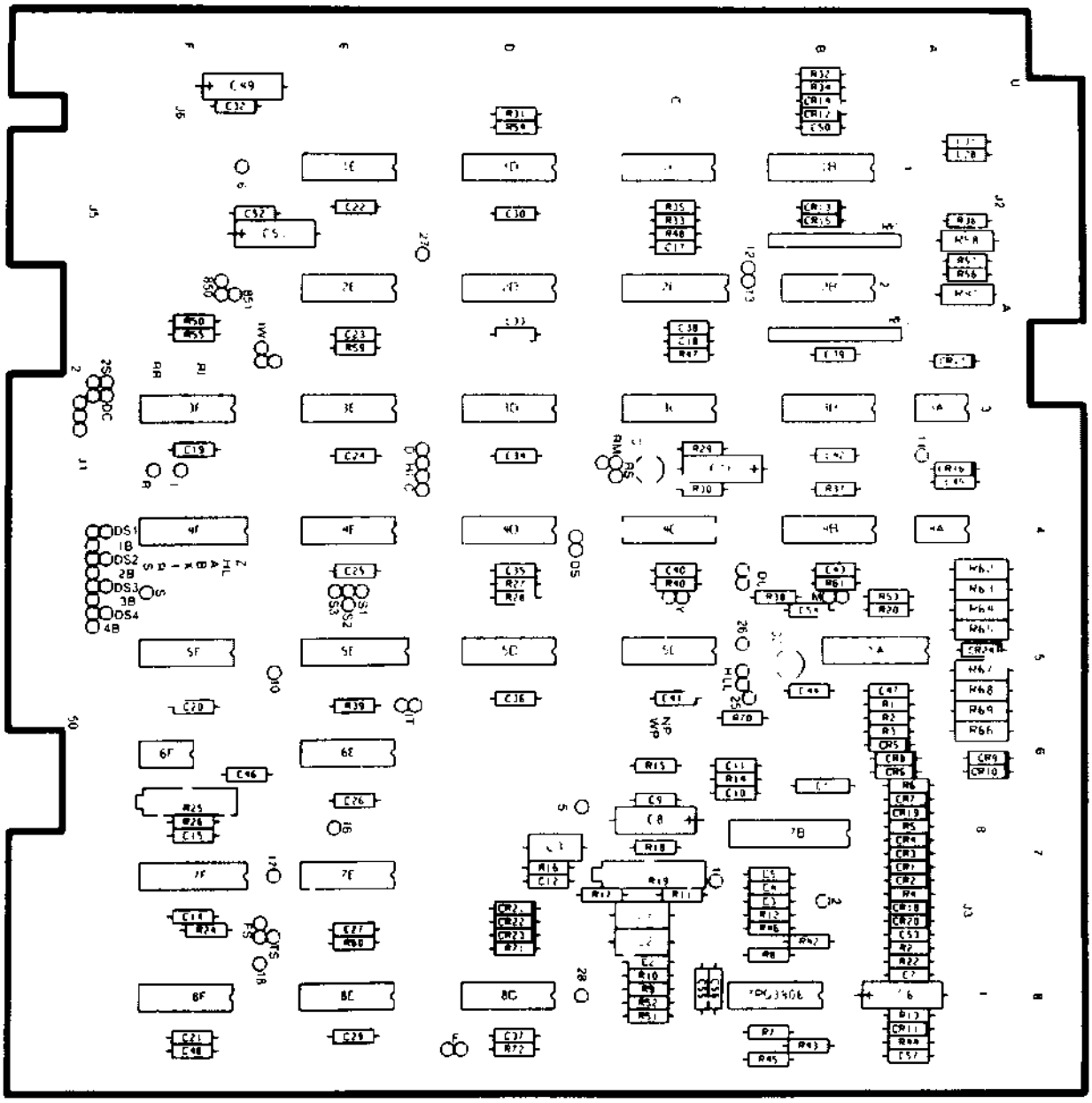


FIGURE 21. MLC 10 COMPONENT LOCATIONS (P/N 25188)

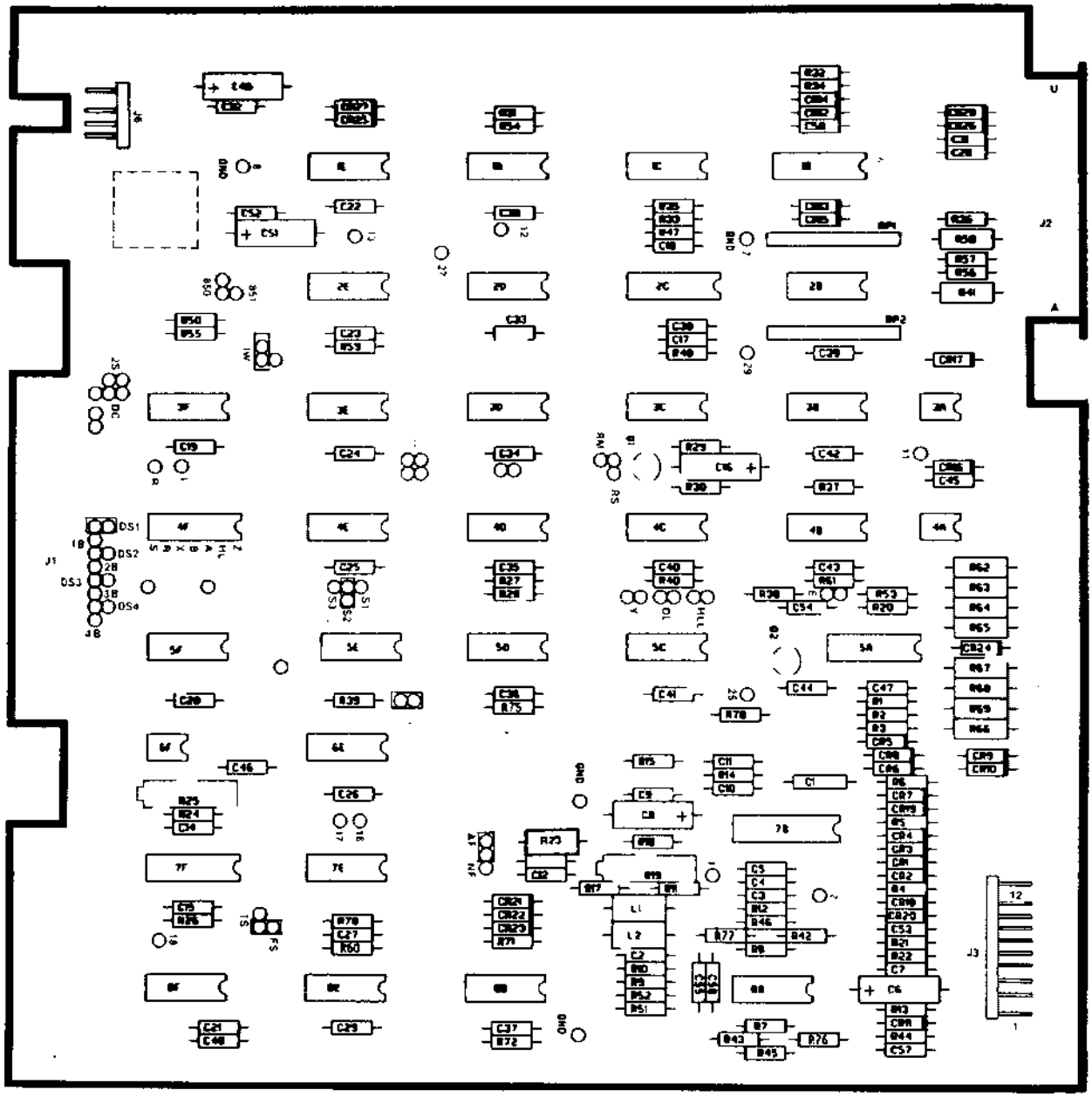


FIGURE 22. MLC 11 PCB COMPONENT LOCATIONS (P/N 25200)

7.1 SELECT DRIVE WITHOUT LOADING HEADS OR ENABLING STEPPER

This option would be advantageous to the user who requires a drive to be selected at all times. Normally, when a drive is selected, its heads are loaded and the stepper motor is energized. The advantage of this option would be that the output control signals could be monitored while the heads were unloaded thereby extending the head and media life. When the system requires the drive to perform a Read, Write, or Seek, the controller would activate the Head Load line (pin 18) which in turn would load the heads and energize the stepper motor. After the Head Load line is activated, a 50 ms delay must be introduced before Write Gate and Write Data may be applied or before Read Data is valid.

To install this option on a standard drive, the following traces should be deleted or added:

1. Cut trace 'X'.
2. Jumper trace 'C'.

7.2 SELECT DRIVE AND ENABLE STEPPER WITHOUT LOADING HEADS

This option is useful to the user who wishes to select a drive and perform a seek operation without the heads being loaded or with door open. An example use of this option is that at power on time, an automatic recalibrate (reverse seek to track zero) operation could be performed with the drive access door open. Normally for a seek to be performed, the door must be closed and the heads loaded. When a Read or Write operation is to be performed, the heads must be loaded. After the Head Load line is activated, a 50 ms delay must be introduced before Write Gate and Write Data may be applied or before Read Data is valid.

To install this option on a standard drive, the following traces should be deleted or added:

1. Cut trace 'B'.
2. Jumper trace 'DS'.
3. Cut trace 'HL'.
4. Jumper trace 'C'.

Figure 23 illustrates the circuitry.

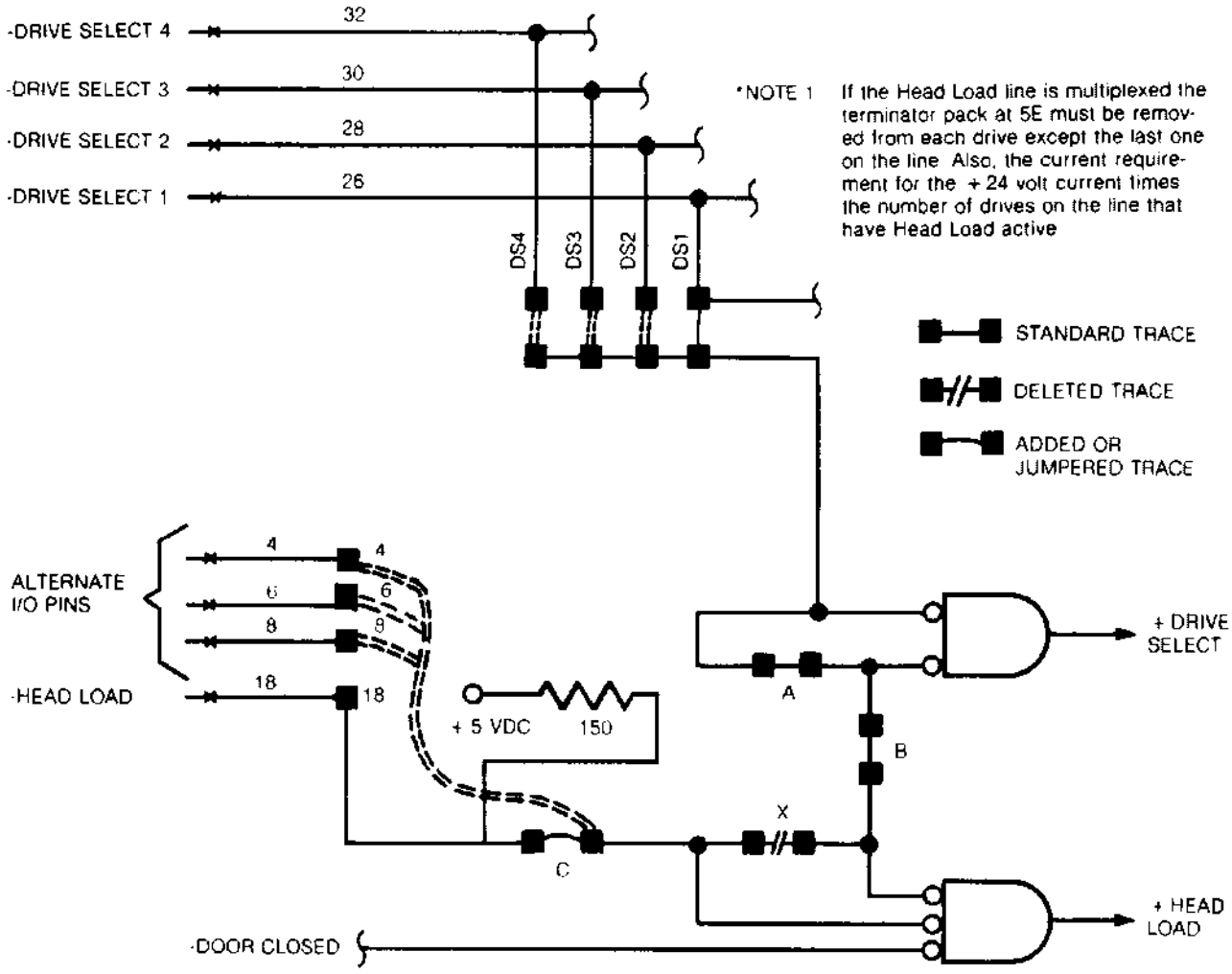


FIGURE 23. SELECT DRIVE WITHOUT LOADING HEAD CIRCUIT

7.3 LOADS HEADS WITHOUT SELECTING DRIVE OR ENABLING STEPPER

This option is useful in disk to disk copy operations. It allows the user to keep the heads loaded on all drives thereby eliminating the 50 ms head load time. The heads are kept loaded on each drive via an Alternate I/O pin. Each drive may have its own Head Load line (Radial or Simplexed) or they may share the same line (Multiplexed). When the drive is selected, an 15 ms delay must be introduced before a Read or Write operation can be performed. This is to allow the read/write heads to settle after the stepper motor is energized. With this option installed, a drive can only be selected with both -Drive Select and -Head Load active.

To install this option on standard drive; the following traces should be deleted or added:

1. Cut trace 'A'.
2. Jumper trace 'DS'.
3. Cut trace 'HL'.

*4. Jumper trace 'C'.

*If the -Head Load line is multiplexed, termination pack 5E jumper must be removed from each drive except the last one on the line.

Figures 24 and 25 illustrates the circuitry.

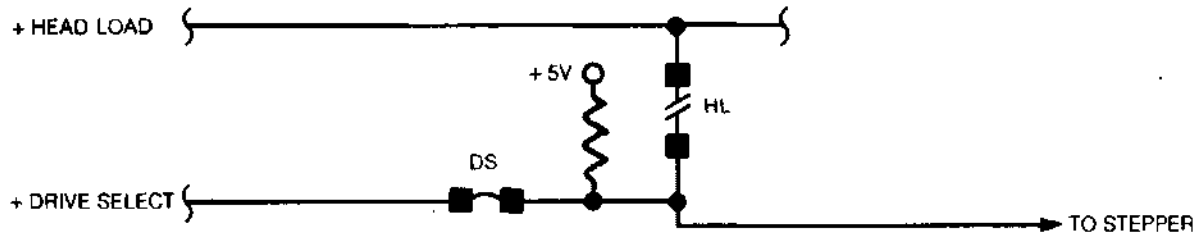
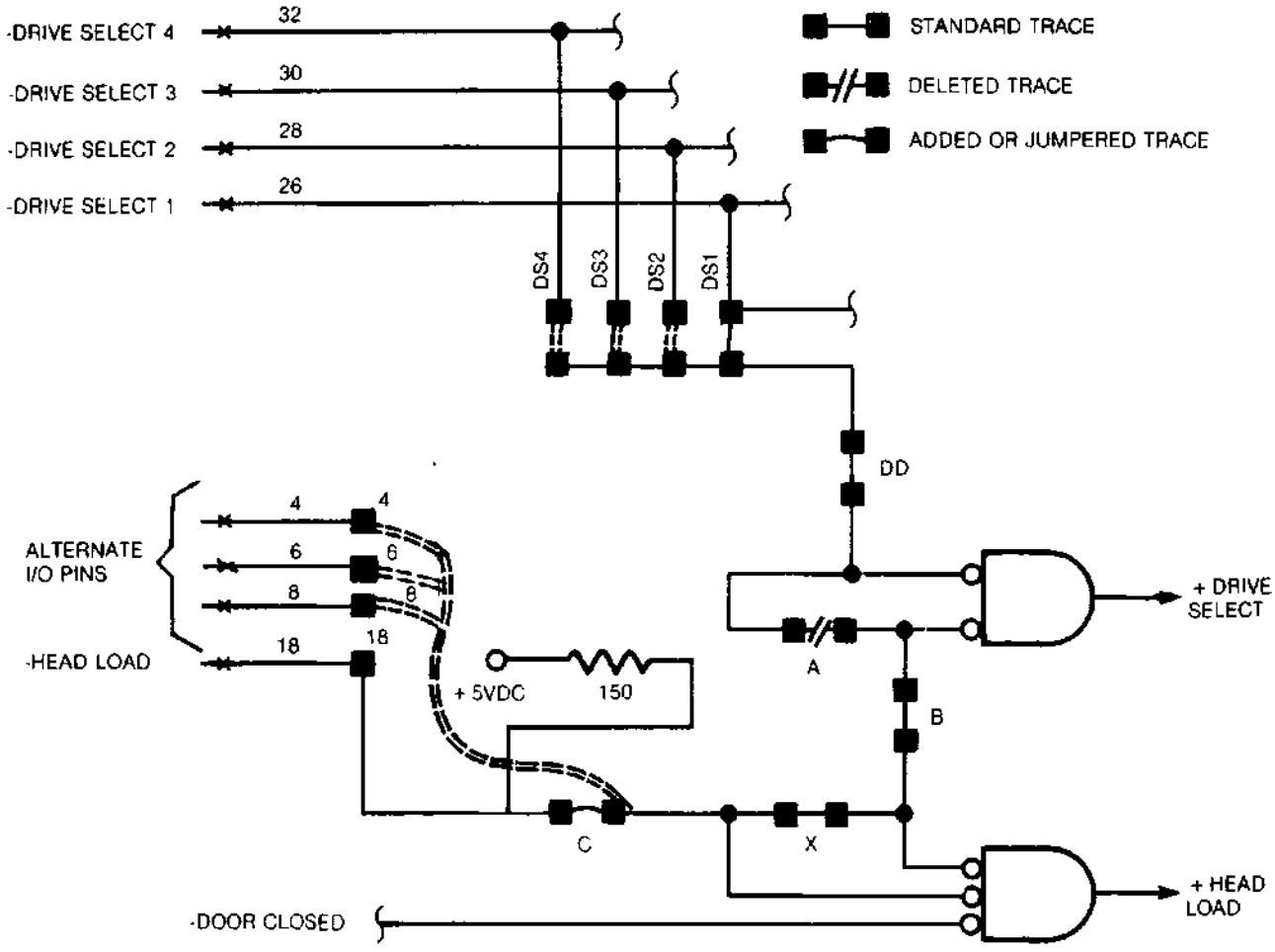


FIGURE 24. STEPPER MOTOR ENABLE CIRCUIT



*If the -Head Load line is multiplexed, termination pack 5E must be removed from each drive except the last one on the line.

FIGURE 25. LOAD HEAD WITHOUT SELECTING DRIVE OR ENABLING STEPPER CIRCUIT

7.4 RADIAL READY

This option enables the user to monitor the Ready line of each drive on the interface. This can be useful in detecting when an operator has removed or installed a Diskette in any drive. Normally, the Ready line from a drive is only available to the interface when it is selected.

To install this option on a standard drive, the following traces should be deleted or added:

1. Cut trace 'RR'.

*2. Cut trace 'R'.

*3. Add a wire from pad "R" to one of the Alternate I/O pins.

*One of the drives on the interface may use pin 22 as its Ready line, therefore steps 2 and 3 may be eliminated on this drive. All the other drives on the interface must have their own Ready line, therefore step 2 and 3 must be incorporated.

Figure 26 illustrates the circuitry.

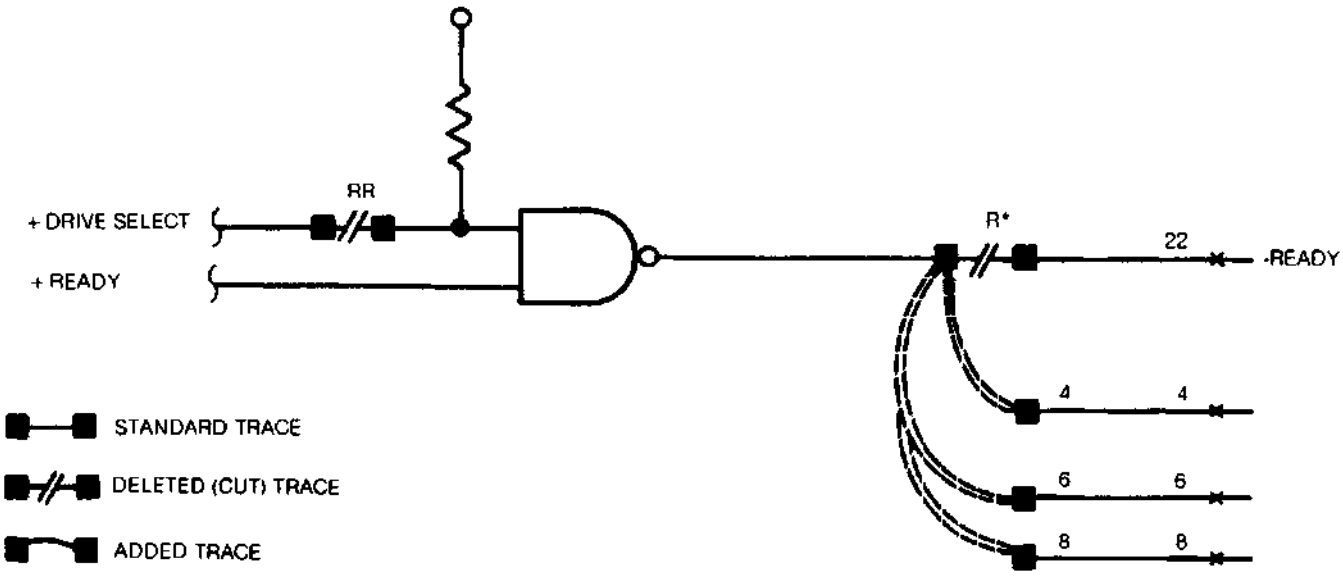


FIGURE 26. RADIAL READY CIRCUIT

7.5 RADIAL INDEX/SECTOR

This option enables the user to monitor the Index and Sector lines at all times so that the drive may be selected just prior to the sector that is to be processed. This option can be used to reduce average latency.

To install this option on a standard drive the following traces should be deleted or added:

1. Cut trace 'RI'.

*2. Cut trace 'I'.

*3. Cut trace 'S'.

*4. Add a wire from trace 'I' to one of the Alternate I/O pins.

*5 Add a wire from trace 'S' to one of the Alternate I/O pins.

*One of the drives on the interface may use pin 20 (-Index) and pin 24 (-Sector) as its Index and Sector lines, therefore steps 2 - 5 may be eliminated for this drive. All other drives on the interface must have their own Index and Sector lines, therefore, steps 2 - 5 must be incorporated.

Figure 27 illustrates the circuitry.

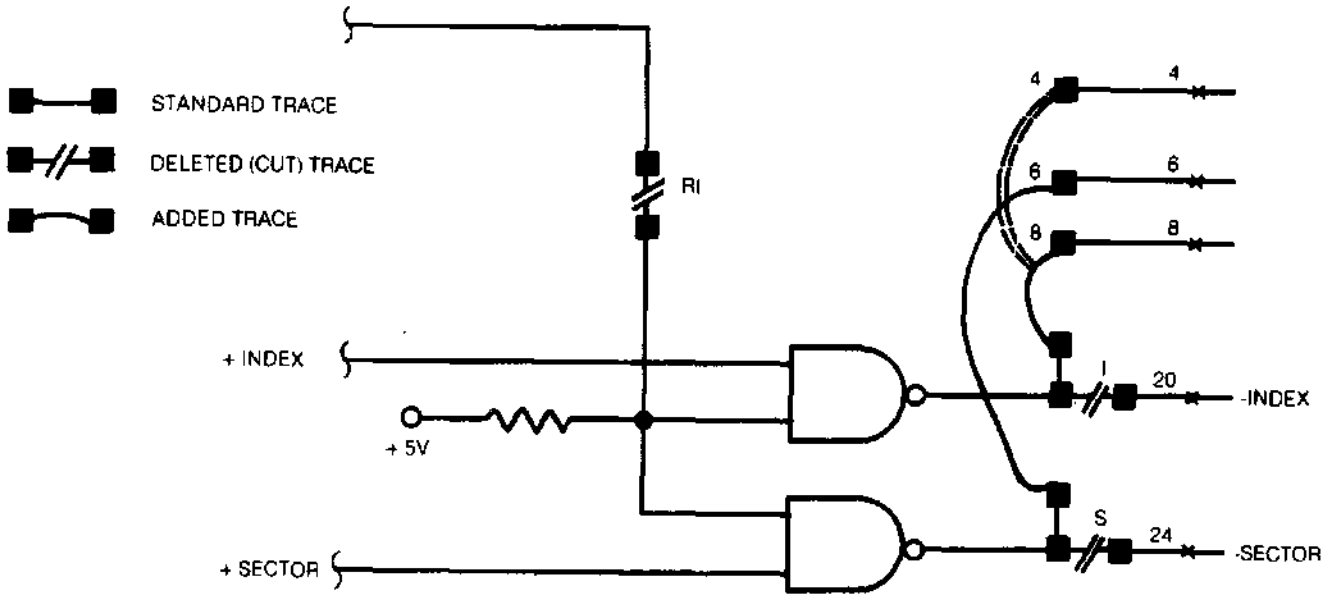


FIGURE 27. RADIAL INDEX/SECTOR CIRCUIT

7.6 IN USE ALTERNATE INPUT (ACTIVITY LED)

This alternate input, when activated to a logical zero level, will turn on the Activity LED mounted in the push bar on the front panel and locks the door of the drive.

To install this option on standard drive, jumper trace 'D' to trace "HI" and activate the interface line pin 16.

This signal is an "OR" function with Drive Select or Head Load. Figure 28 illustrates the circuitry. For other uses, reference section 7.15.

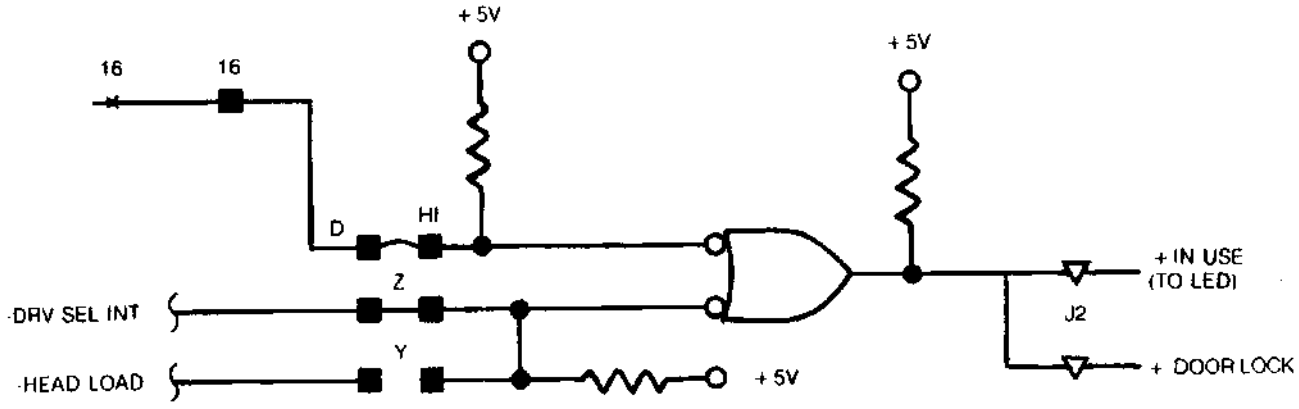


FIGURE 28. IN USE/ACTIVITY LED CIRCUIT

7.7 WRITE PROTECT OPTIONAL USE

As shipped from the factory, the optional Write Protect feature will internally inhibit writing when a Write Protected Diskette is installed. With this option installed, a Write Protected Diskette will not inhibit writing, but it will be reported to the interface. This option may be useful in identifying special use Diskettes.

To install this option on a drive with the Write Protect feature, the following traces should be added or deleted:

1. Cut trace 'WP'.
2. Connect trace 'NP'.

Figure 29 illustrates the circuitry.

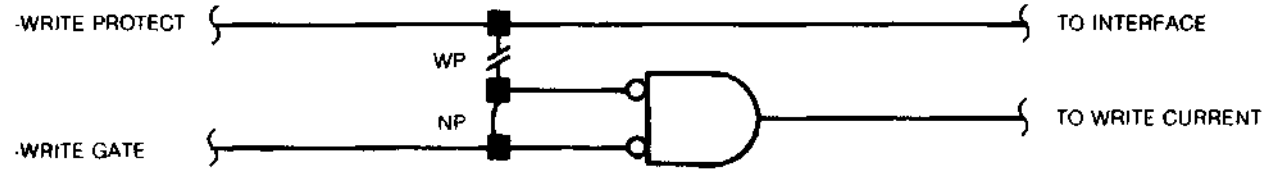


FIGURE 29. WRITE PROTECT CIRCUIT

7.8 DISK CHANGE (OPTIONAL OUTPUT)

This customer installable option is enabled by jumpering trace 'DC'. It will provide a true signal (logical zero) onto the interface (pin 12) when Drive Select is activated if while deselected the drive has gone from a Ready to a Not Ready (Door Open) condition. This line is reset on the true to false transition of Drive Select if the drive has gone Ready. Timing of this line is illustrated in Figure 30. The circuitry is illustrated in Figure 31.

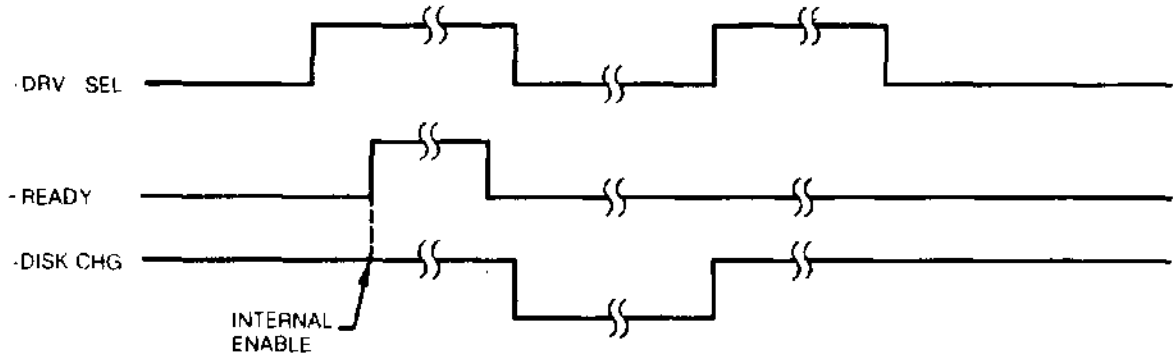


FIGURE 30. DISK CHANGE TIMING

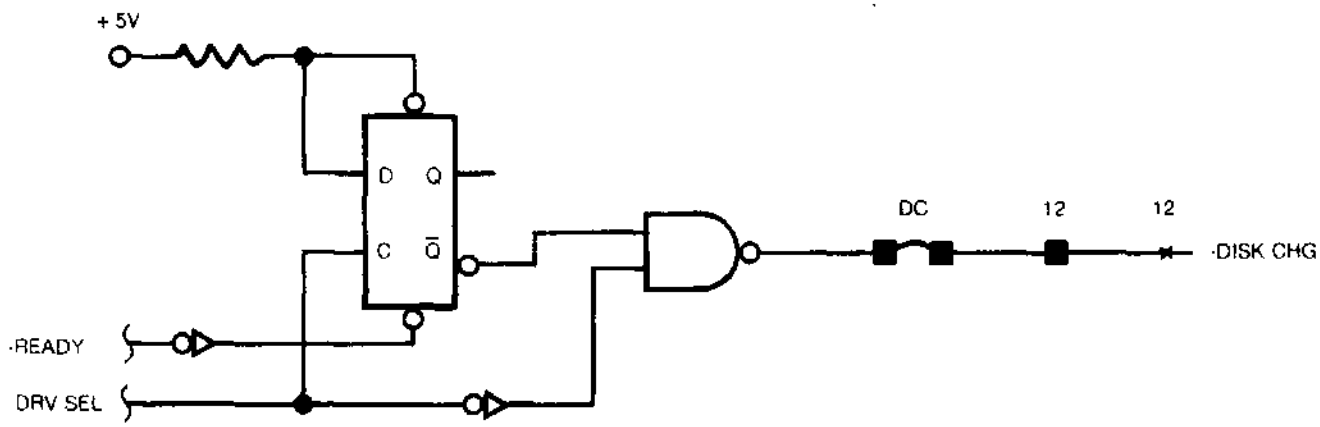


FIGURE 31. DISK CHANGE CIRCUIT

7.9 SIDE SELECTION, USING DIRECTION SELECT

The Side Select function can be controlled via the Direction Select line, if desired. With this option, the Direction Select line controls the direction of head motion during stepping operations and controls side (head) selection during read/write operations. To implement this option, simply move jumper S2 to location S1.

Figure 32 illustrates the circuitry.

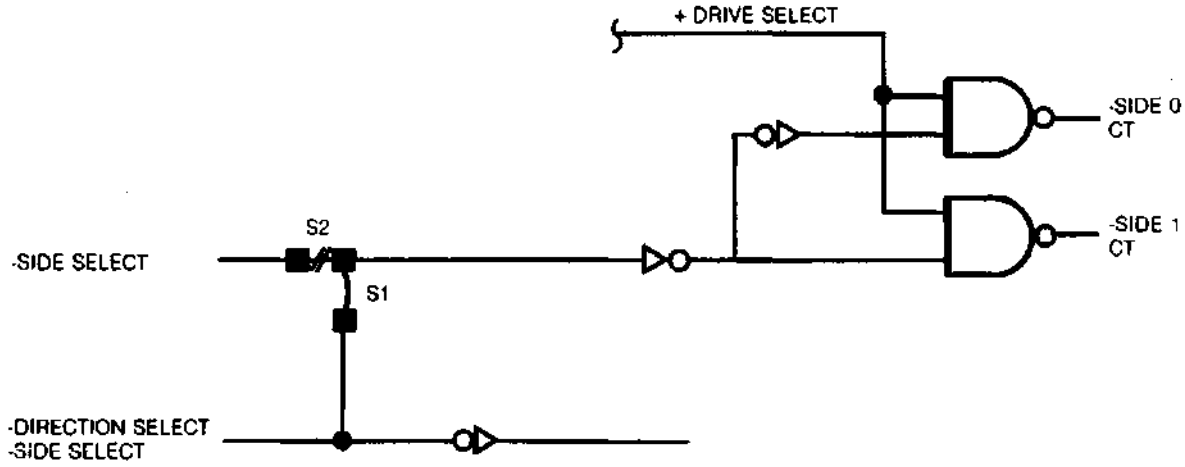


FIGURE 32. SIDE SELECTION, USING DIRECTION SELECT

7.10 SIDE SELECTION USING DRIVE SELECT

In systems containing no more than two SA850/851 drives per controller, each read/write head can be assigned a separate drive address. In such cases, the four Drive Select line can be used to select the four read/write heads. To implement this option, move jumper S2 to S3 and add a jumper to nB (n = 1, 2, 3 or 4). For example, the first drive may have jumpers installed at DS1 and 2B while the second drive has jumpers at DS3 and 4B. With this jumper configuration installed, the four Drive Select lines have the following side selection functions.

1. Drive Select 1 selects side 0 of first drive.
2. Drive Select 2 selects side 1 of first drive.
3. Drive Select 3 selects side 0 of second drive.
4. Drive Select 4 selects side 1 of second drive.

Figure 33 illustrates the circuitry.

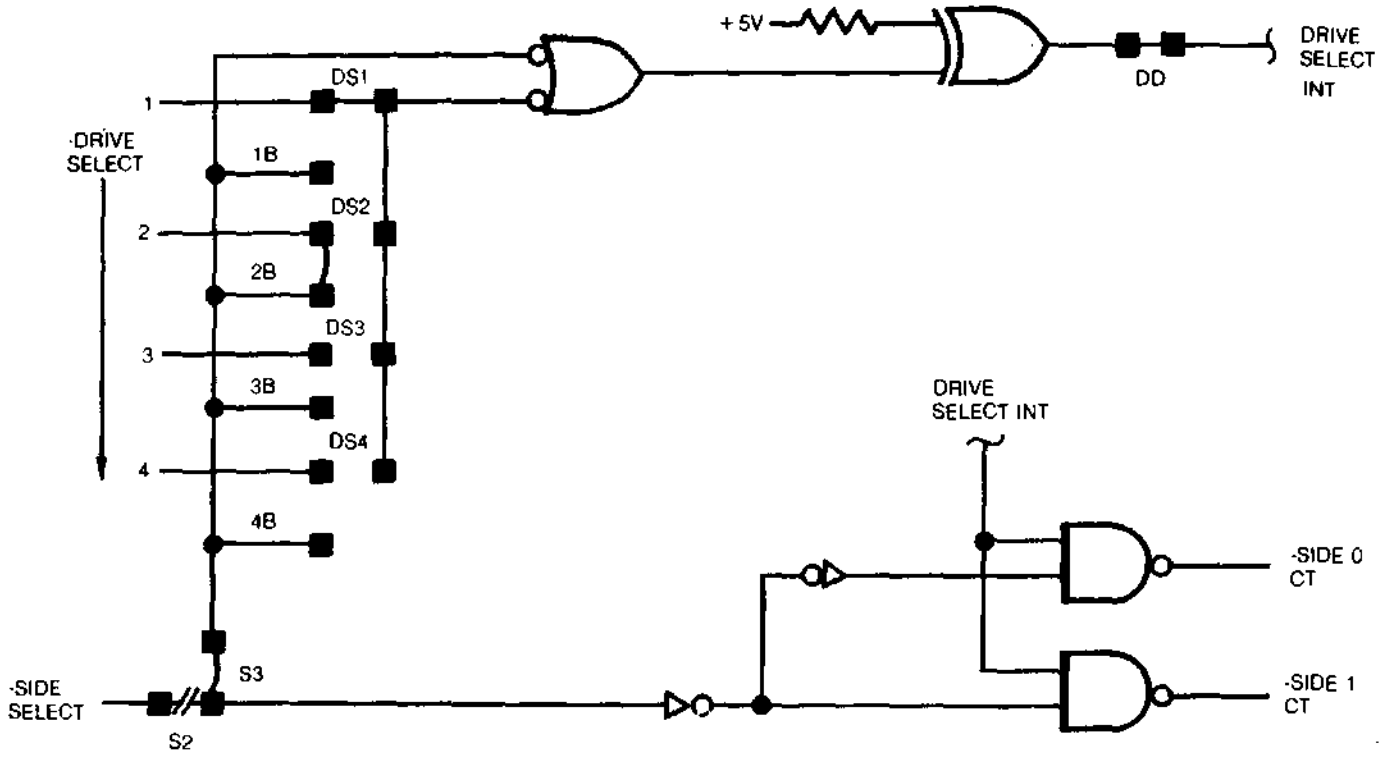


FIGURE 33. SIDE SELECTION, USING DRIVE SELECT

7.11 DOOR LOCK LATCH

The door lock circuit can be latched on under Drive Select control so that the door can remain locked without maintaining the active state of In Use. To implement this option, jumper DL, and then D to HI. Then, if the appropriate Drive Select line is activated while In Use is active, a latch will be set, which holds the door lock circuit active. To unlock the door, Drive Select is again activated while In Use is inactive.

Figure 34 illustrates the circuitry for this option.

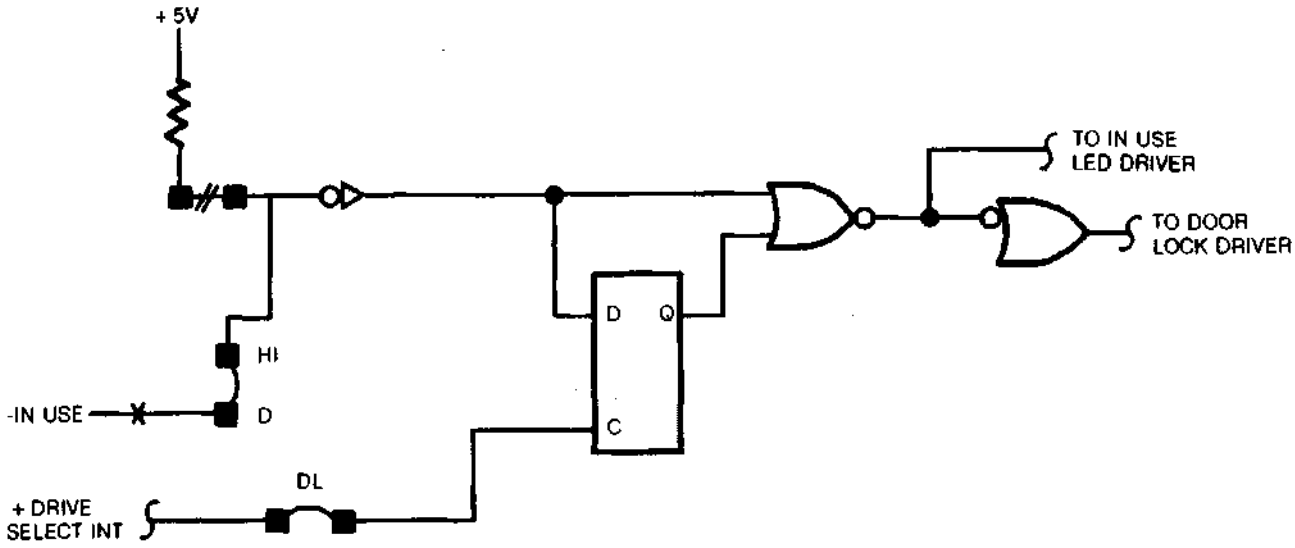


FIGURE 34. DOOR LOCK LATCH CONTROL

7.12 TWO-SIDED (OPTIONAL OUTPUT)

This signal indicates whether a Two-Sided (True Output) or a Single-Sided (False Output) Diskette is installed. To implement this option, install a jumper at 2S.

7.13 HEAD CURRENT SWITCH/ACTIVE READ COMPENSATION

This interface signal is used for two different functions depending on whether the drive is in a write or read mode.

7.13.1 HEAD CURRENT SWITCH

When the interface signal is activated to a logical zero level, the lower value of the write current is selected for writing on tracks 43 through 76.

To enable head current switching, short trace "IW" (to connect to the interface).

To disable head current switching and select only the lower value of the write current, move the shorting plug at trace "IW" to the ground position and short trace "M".

Trace "M" is used to increase the values of both the lower and higher write currents available when current switching.

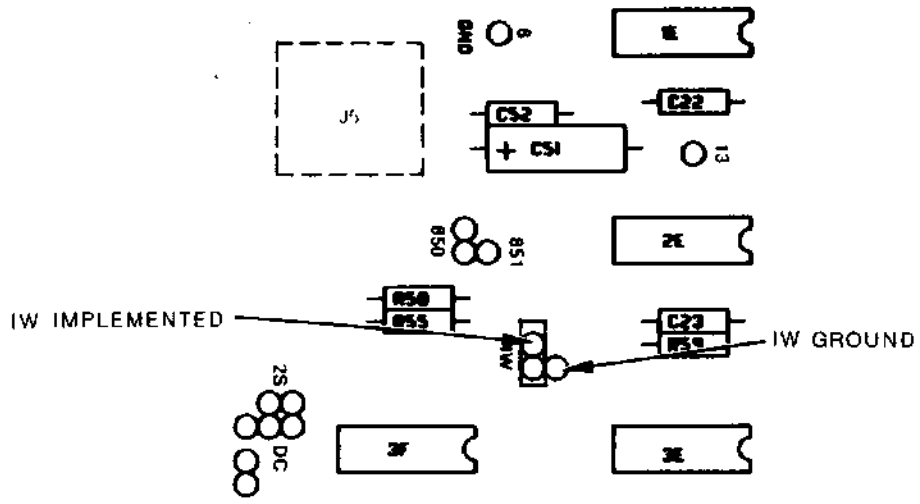


FIGURE 35. IW JUMPER OPTION

7.13.2 ACTIVE READ FILTER

When the interface signal is activated to a logical zero level, the read signal is passed through an active filter network for reading tracks 60 through 76. Performance will improve when reading a diskette that has been recorded without write precompensation.

To control the active read filter from the interface, short trace "IW" (to connect to the interface), remove jumpers AF and NF. When the interface is activated to a logical zero level, read compensation is selected as if AF were added. When the interface is activated to a +5V level, read compensation is selected as if NF were added.

For optimum performance for FM or MFM encoding, jumper trace AF, for M^2FM encoding jumper trace NF.

7.14 READY STANDARD/READY MODIFIED

As shipped the "RS" jumper is plugged and the drive's Ready Circuit will function as in the past. With the shorting plug in the "RM" position, the Ready Circuit is modified so that the drive will stay ready. This option is useful for those customers using the Direction Select line as Slide Select, so that when using single sided media the drive will stay ready when side 1 is selected.

7.15 HEAD LOAD LATCH

This option enables the heads to remain loaded when the drive is deselected. To enable this option, jumper traces "DL" and "HLL". The head load can then be latched by either of two interface lines - Head Load (pin 18) or In Use (pin 16). If Head Load is to be used jumper pin "C" to pin "HI" and remove the "IT" jumper (refer to figure 36). If In Use is to be used jumper pin "D" to pin "HI" (refer to figure 37). In both cases, trace "A" on shunt 4F must be cut. To load and latch the heads the user must activate either the Head Load or In Use lines and select the drive. When the drive is deselected, the heads will stay loaded and the door locked. To unload the heads, the Head Load or In Use line must be inactive when the drive is selected.

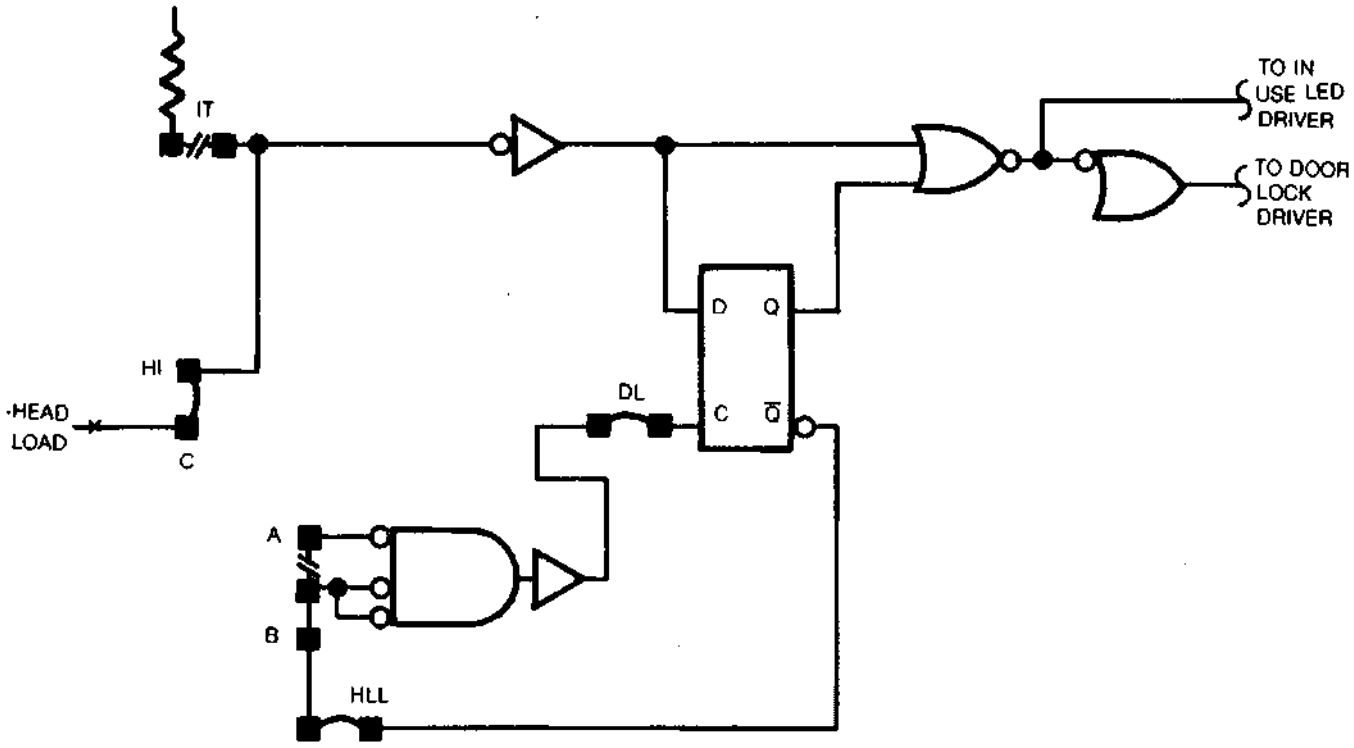


FIGURE 36. HEAD LOAD LATCH USING HEAD LOAD

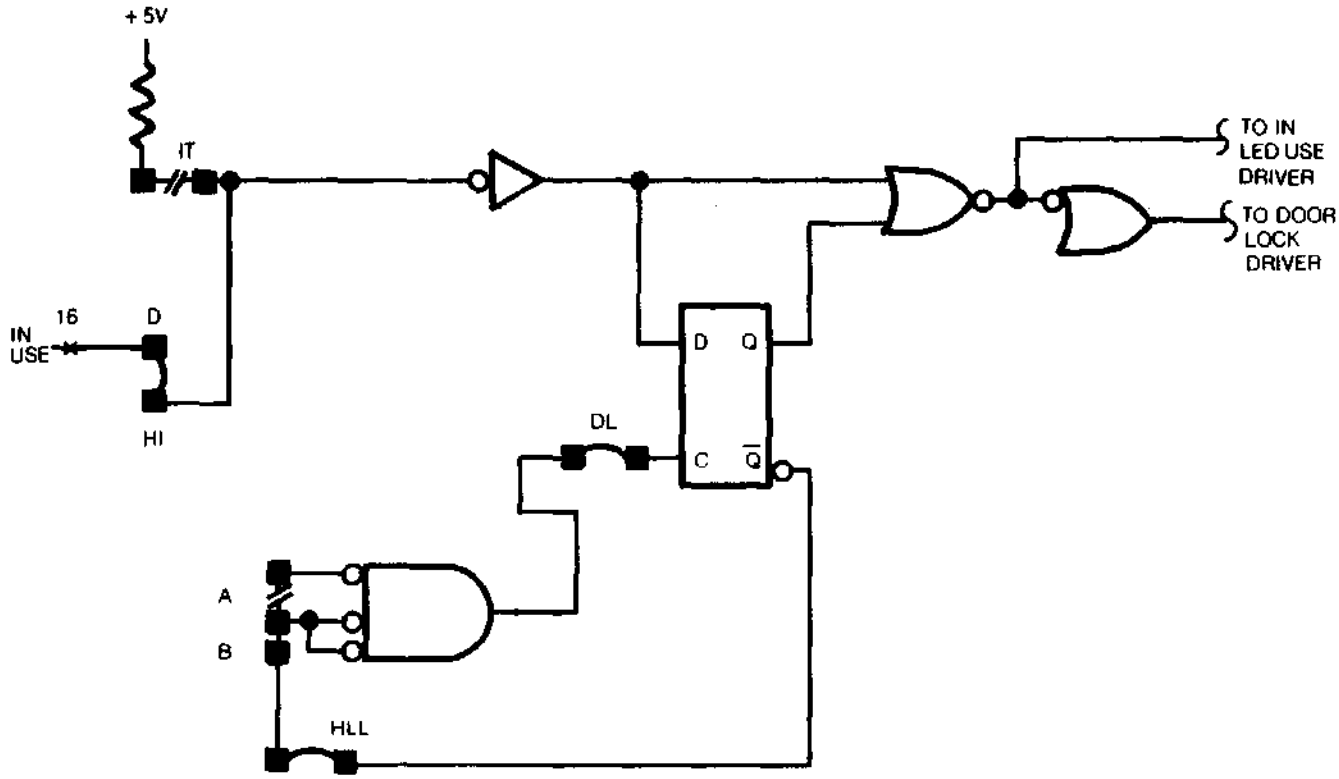


FIGURE 37. HEAD LOAD LATCH USING IN USE

8.0 OPERATION PROCEDURES

The SA850/851 was designed for ease of operator use to facilitate a wide range of operator oriented applications. The following section is a guide for the handling and error recovery procedures on the diskette and diskette drive.

8.1 DISKETTE LOADING AND HANDLING

The diskette is a flexible disk enclosed in a plastic jacket. The interior of the jacket is lined with a wiping material to clean the disk of foreign material. Figure 38 shows the proper method of loading a diskette in the SA850/851 Diskette Storage Drive. To load the diskette, depress latch, insert the diskette with the label facing out. Move the latch handle to the left to lock diskette on drive spindle. The diskette can be loaded or unloaded with all power on and drive spindle rotating.

When removed from the drive, the diskette is stored in an envelope. To protect the diskette, the same care and handling procedures specified for computer magnetic tape apply. These precautionary procedures are as follows:

1. Return the diskette to its storage envelope whenever it is removed from drive.
2. Keep diskettes away from magnetic fields and from ferromagnetic materials which might become magnetized. Strong magnetic fields can destory recorded data on the disk.
3. Replace storage envelopes when they become worn, cracked or distorted. Envelopes are designed to protect the disk.
4. Do not write on the plastic jacket with a lead pencil or ball-point pen. Use a felt tip pen.
5. Heat and contamination from a carelessly dropped ash can damage the disk.
6. Do not expose diskette to heat or sunlight.
7. Do not touch or attempt to clean the disk surface. Abrasions may cause loss of stored data.

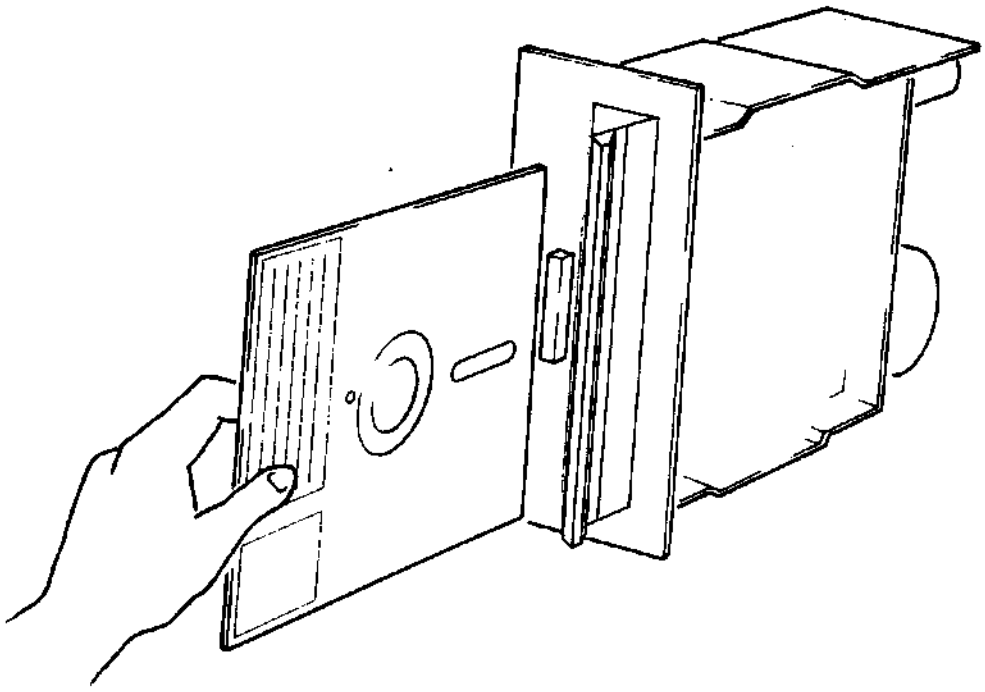


FIGURE 38. LOADING SA850/851

8.2 WRITE PROTECT — SA150/151 DISKETTES

The SA150/151 diskettes have the capability of being write protected. The write protect feature is selected by the slot in the SA150/151. When the slot is open it is protected; when covered, writing is allowed. The slot is closed by placing a tab over the front of the slot, and the tab folded over covering the rear of the slot. The Diskette can then be write protected by removing the tab. See Figure 39.

8.3 WRITE PROTECT, IBM DISKETTES

IBM Diskettes are not manufactured with a write protect slot punched out as are the Shugart Diskettes. To Write Protect one of these diskettes, a slot must be punched out as specified in Figure 40. The operation of the write protect is that which is outlined in paragraph 8.2

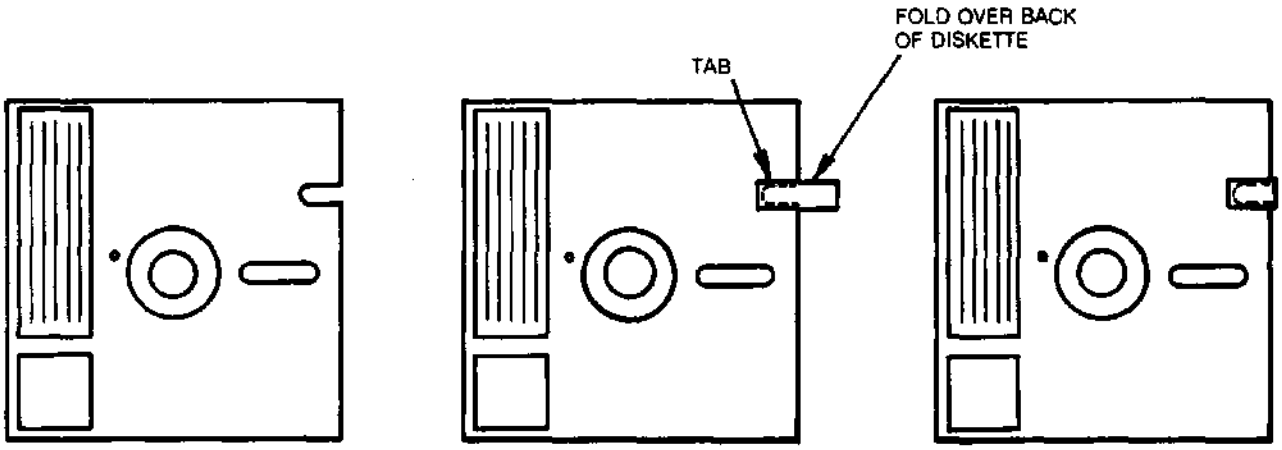


FIGURE 39. DISKETTE WRITE PROTECTED

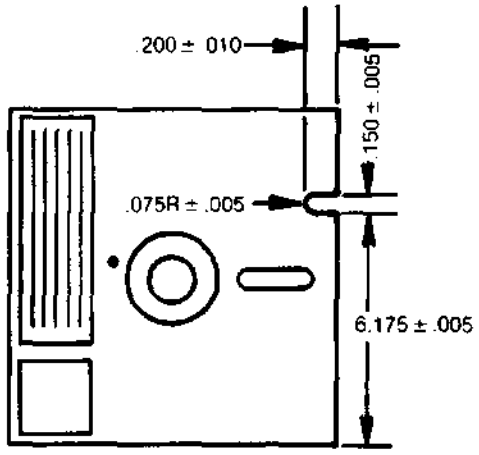


FIGURE 40. WRITE INHIBIT NOTCH SPECIFICATIONS

9.0 ERROR DETECTION AND CORRECTION

9.1 WRITE ERROR

If an error occurs during a write operation, it will be detected on the next revolution by doing a read operation, commonly called a "write check". To correct the error, another write and write check operation must be done. If the write operation is not successful after ten (10) attempts have been make, a read operation should be attempted on another track to determine if the media or the drive is failing. If the error still persists, the disk should be considered defective and discarded.

9.2 READ ERROR

Most errors that occur will be "soft" errors; that is, by performing an error recovery procedure the data will be recovered.

Soft errors are caused by:

1. Airborne contaminants that pass between the read/write head and the disk. These contaminants will generally be removed by the cartridge self-cleaning wiper.

2. Random electrical noise which usually lasts for a few microseconds.

3. Small defects in the written data and/or track not detected during the write operation which may cause a soft error during a read.

The following procedures are recommended to recover from the above mentioned soft errors:

1. Reread the track ten (10) times or until such time as the data is recovered.

2. If data is not recovered after using step 1, access the head to the adjacent track in the same direction previously moved, then return to the desired track.

3. Repeat step 1.

4. If data is not recovered, the error is not recoverable.

10.0 RESHIPMENT PRECAUTION

Be sure to insert the shipping disk that was shipped with the unit, close the door, and install the latch stop when reshipping the drive.

The packaging material must be clean and dry as determined by visual inspection. Figure 41 shows how to repackage the disk drive using the original shipping containers. Figure 42 shows the pallet pattern and the minimum/maximum pallet size to use if reshipped in large enough quantities.

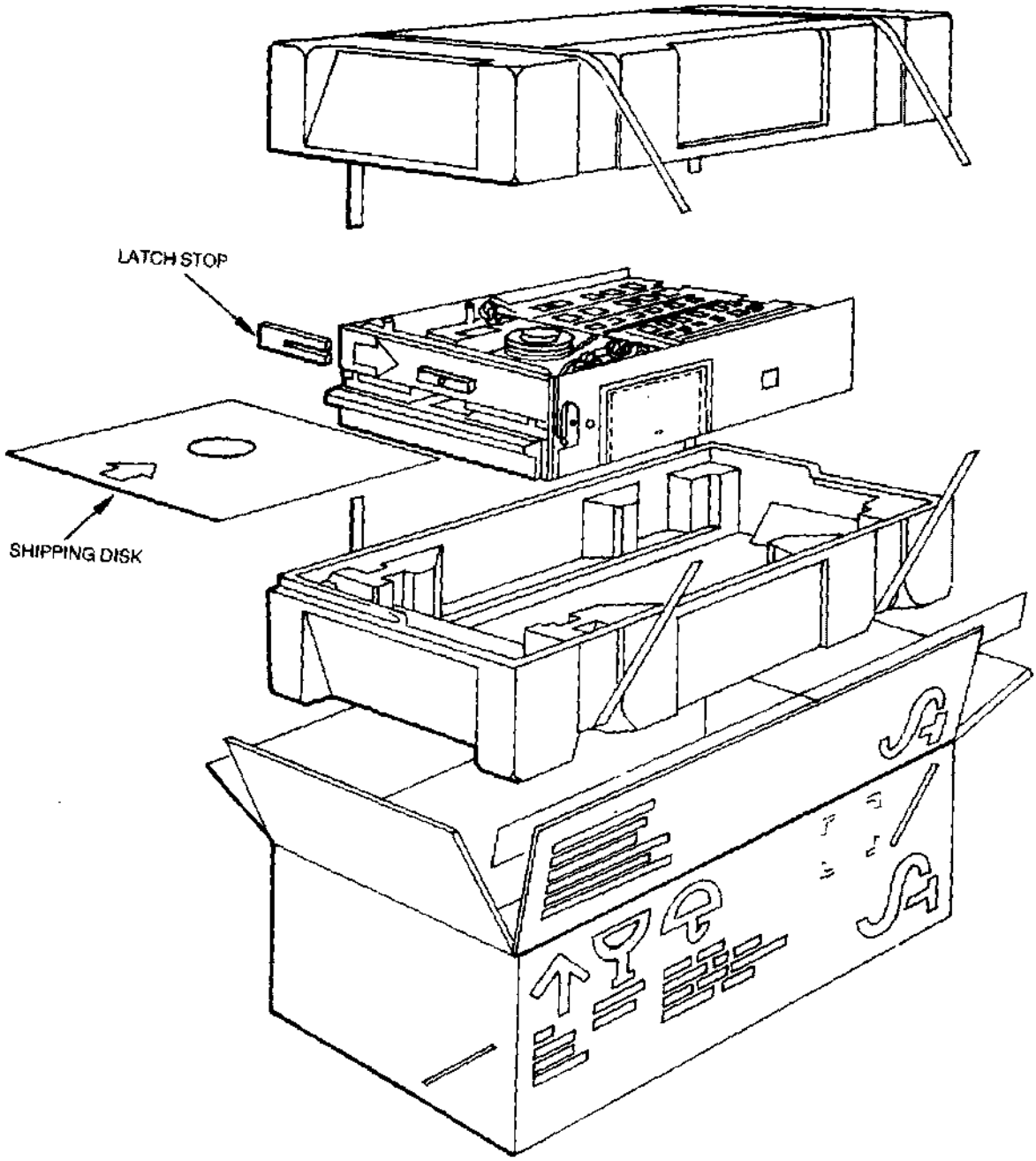
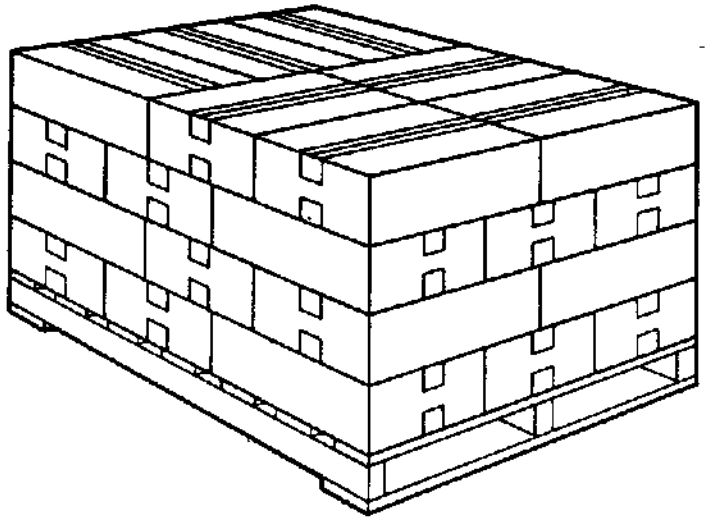
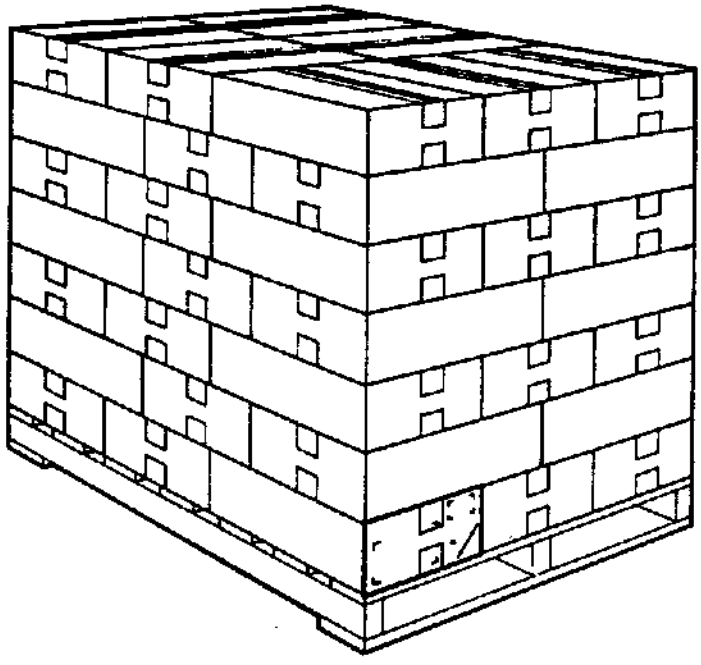


FIGURE 41. PACKAGE ASSEMBLY



MINIMUM LOAD



MAXIMUM LOAD

FIGURE 42. PALLET LOADING

APPENDIX A - ORDERING INFORMATION

The table below can be used to construct a part number for a unique drive configuration

ABCDEF

AB	MODEL
850 BC	75

C	VOLTAGE FREQUENCY	
	60	50
115	1	3
230	2	4

D	MODEL
850	1
851	2
850-4	3

E	FEATURE
STD.	1
RACK	2

F	OPTIONS
NONE	0

DECORATIVE FACE PLATES

Size	Color	Part Numbers
4-5/8 × 10-1/2	Tan	50264
4-5/8 × 10-1/2	White	50263
5-1/4 × 10	Tan	50261
5-1/4 × 10	White	50260
5-1/4 × 11	Tan	50258
5-1/4 × 11	White	50257
Rack Mount 4-5/8 × 8-11/16	Tan	50675

Primary Voltage and Frequency	Part Numbers		
	Motor ASM*	Motor Pulley	Belt
115 VAC, 60 Hz	50747	50358	50356
115 VAC, 50 Hz	50747	50357	50355
230 VAC, 60 Hz	50748	50358	50356
230 VAC, 50 Hz	50748	50357	50355

*Motor assemblies include - motor, capacitor, and connector