2.0 64K DYNAMIC MEMORY BOARD

GENERAL INFORMATION

The Nabu Memory Board ADM-1000, uses industry standard 4116 dynamic random-access memories (RAM's); which provide low cost and low power consumption. Reliability of the board is enhanced by the low support-IC count, and the use of a precision delay line for critical timing.

Address lines and data lines are fully buffered by line drivers/receivers with hysteresis at the inputs to improve noise immunity. The memory board offers a full 64K bytes of read/write memory; however only 62K bytes are available to the user in the Nabu 1100 System, since 2K bytes are allocated to the disk bootstrap program in ROM. A signal called PHANTOM from the S-100 bus, can be utilized to allow user ROM to overlay the RAM.

In the Nabu 1100 System, the access time of the memory chips is 150 nanoseconds (ns), permitting operation at 4 MHz, with no wait states added. The use of slower memory chips is not recommended. Memory refresh is done automatically by the Z-80A CPU after each instruction fetch. This mode of refresh is totally transparent to the programmer and does not slow down the CPU operation.

SPECIFIC FEATURES

Memory Organization

The 4116 RAM chip has a 16K x 1 organization, with eight chips connected in parallel to form a 16K byte memory bank. Four memory banks are implemented on the memory board.

The jumper options on the left side of the board are used for selecting memory banks. Each bank can be enabled or disabled, by installing or removing each corresponding jumper. In this way, up to 64K bytes of memory space can be obtained.

The jumpers are numbered as follows:

Jumper	Bank #	RAM IC's Needed	Address Space
JP-1:	1	RAM 1 - RAM 8,	0000H - 3FFFH
JP-2:	2	RAM 9 - RAM 16,	4000H - 7FFFH
JP-3:	3	RAM 17 - RAM 24,	8000H - BFFFH
JP-4:	4	RAM 25 - RAM 32,	C000H - FFFFH

Each bank is enabled by installing the appropriate jumper.

Memory Refresh

As mentioned, the memory refresh is done automatically by the Z-80A CPU through the S-100 bus. The CPU contains a 7-bit memory refresh counter, which is incremented automatically after each instruction fetch. The data in the counter is sent out on the lower portion of the address bus along with two refresh control signals, $\overline{\text{RFSH}}$ (pin 66) and $\overline{\text{MREQ}}$ (pin 65); while the CPU is decoding and executing the fetched instruction. This refresh operation must be performed at least every two milliseconds in order to retain data.

An interrupt request/acknowledge cycle in the system does not affect the memory refresh operation, since only two wait states are added to this cycle for identifying the interrupting

I/O device. However, a bus request/acknowledge cycle used in Direct Memory Access (DMA), for instance, can cause a memory refresh problem if very long DMA cycles are used. Therefore, the DMA controller must perform the necessary refresh function.

A user supplied S-100 bus compatible board which uses wait states can also be used in the Nabu 1100 System, providing the wait states added do not exceed the 2 ms limit. However, caution should be used in adding boards with wait states, unless the number and frequency of wait states is strictly controlled.

Data Buffers and PHANTOM

All data-in and data-out lines of the memory chips are buffered by U9 and U14. The data-in lines are always enabled and the data-out lines are controlled by U5, whose four inputs are conditioned by PDBIN, SMEMR, $\overline{\text{MREQ}}$, $\overline{\text{PHANTOM}}$, and by two high address bits (A15 and A14). Reading of the RAM contents is not allowed when U5 is disabled; however writing into the RAM is still permissible.

$\overline{\text{PHANTOM}}$ is normally pulled high through a resistor. This line is primarily used for system bootstrapping by overlaying the RAM with ROM (not used in the Nabu 1100 System). This is done by pulling $\overline{\text{PHANTOM}}$ low at system start-up, copying the ROM contents into the RAM which occupies the same address, and executing the bootstrap program from the RAM after pulling $\overline{\text{PHANTOM}}$ high. In this way, a full 64K bytes of read/write memory is obtained.

NABU ADM-1000 64K DYNAMIC MEMORY BOARD
PARTS LIST

Integrated Circuits:

U1	74LS75	Quadruple latch
U2	74LS42	4-line-to-10-line decoder
U3, U4	74LS00	Quadruple 2-input NAND
U5	74LS20	Dual 4-input NAND
U6	74LS132	Quadruple 2-input NAND with Schmitt-triggered inputs
U7, U8	74S157	Quadruple 2-line-to-1-line Schottky multiplexer
U9, U14	74LS241	Octal buffer/line-driver with 3-state outputs
U10-U13	74LS14	Hex inverter with Schmitt-triggered inputs
U15	STTLDM-355	TTL-compatible logic-delay module
U16	7805	5 V positive voltage regulator
U17	7812	12 V positive voltage regulator
RAM1-RAM32	4116	16384-bit dynamic RAM (150 ns)

Diodes:

D1	1N4733A	5.1 V, 1.0 W, 5 % zener diode

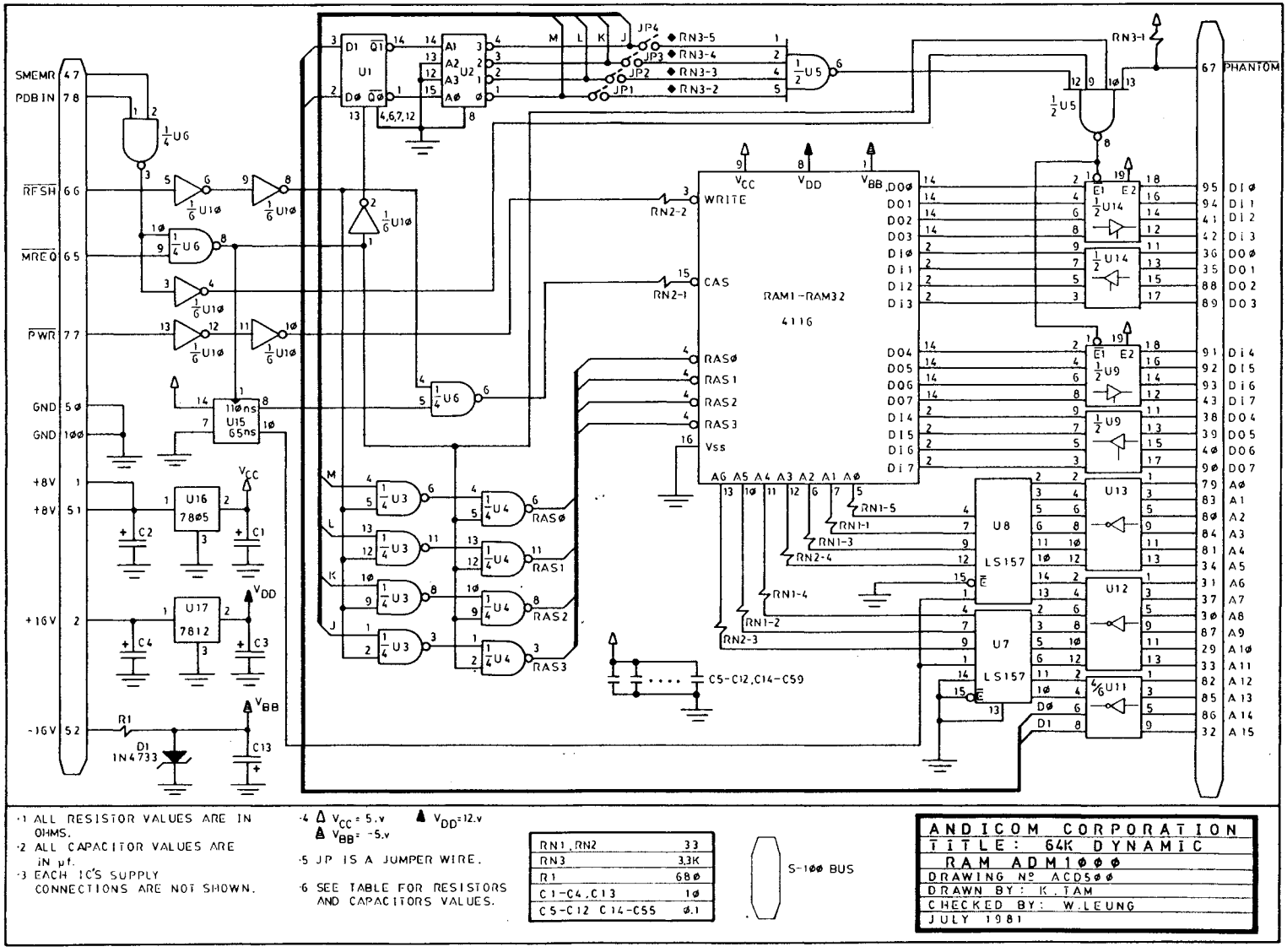
Capacitors:

C1-C4, C13	10 µF, 25 V tantalum electrolytic
C5-C12, C14-C59	0.1 µF

Resistors:

R1	680Ω , 0.5 W, 10%
RN1,RN2	5-resistor pack of 33Ω resistors
RN3	5-resistor pack of 3.3 kΩ resistors with common pin #1

Quantity	Description
36	16 pin IC socket
9	14 pin IC socket
2	20 pin IC socket
2	6-32 x 3/8" machine screw
2	#6-32 nuts
2	Delta 291-0.36-AB-H
1	p.c. board



·1 ALL RESISTOR VALUES ARE IN OHMS.
·2 ALL CAPACITOR VALUES ARE IN μf.
·3 EACH IC'S SUPPLY CONNECTIONS ARE NOT SHOWN.
·4 △ V_{CC} = 5.v ▲ V_{DD}=12.v ▲ V_{BB} = -5.v
·5 JP IS A JUMPER WIRE.
·6 SEE TABLE FOR RESISTORS AND CAPACITORS VALUES.

RN1, RN2	33
RN3	3.3K
R1	68Ø
C1-C4, C13	1Ø
C5-C12 C14-C55	Ø.1

S-1ØØ BUS

ANDICOM CORPORATION
TITLE: 64K DYNAMIC RAM ADM1ØØØ
DRAWING Nº ACD5ØØ
DRAWN BY: K.TAM
CHECKED BY: W.LEUNG
JULY 1981

FIGURE 4: SCHEMATIC DIAGRAM OF DYNAMIC MEMORY BOARD

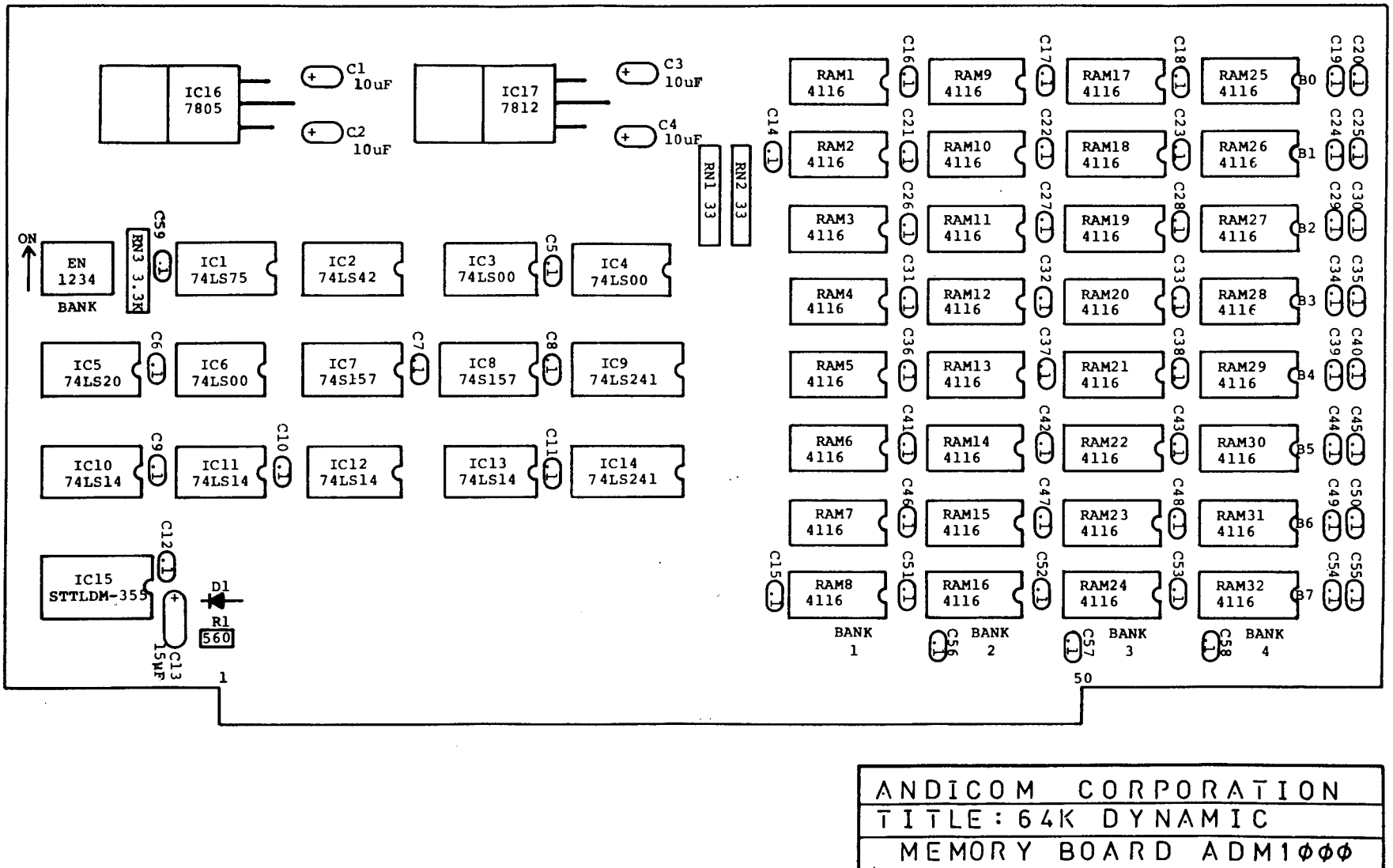


FIGURE 5: DYNAMIC MEMORY BOARD LAYOUT

NEC Microcomputers, Inc.

NEC
μPD416
μPD416-1
μPD416-2
μPD416-3
μPD416-5

16384 x 1 BIT DYNAMIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The NEC μPD416 is a 16384 words by 1 bit Dynamic MOS RAM. It is designed for memory applications where very low cost and large bit storage are important design objectives.

The μPD416 is fabricated using a double-poly-layer N channel silicon gate process which affords high storage cell density and high performance. The use of dynamic circuitry throughout, including the sense amplifiers, assures minimal power dissipation.

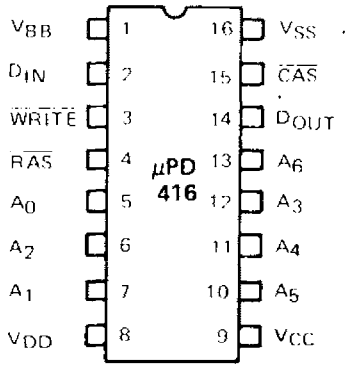
Multiplexed address inputs permit the μPD416 to be packaged in the standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is available in either ceramic or plastic. Noncritical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

FEATURES

- 16384 Words x 1 Bit Organization
- High Memory Density – 16 Pin Ceramic and Plastic Packages
- Multiplexed Address Inputs
- Standard Power Supplies +12V, -5V, +5V
- Low Power Dissipation; 462 mW Active (MAX), 40 mW Standby (MAX)
- Output Data Controlled by $\overline{CAS}$ and Unlatched at End of Cycle
- Read-Modify-Write, $\overline{RAS}$-only Refresh, and Page Mode Capability
- All Inputs TTL Compatible, and Low Capacitance
- 128 Refresh Cycles
- 5 Performance Ranges:

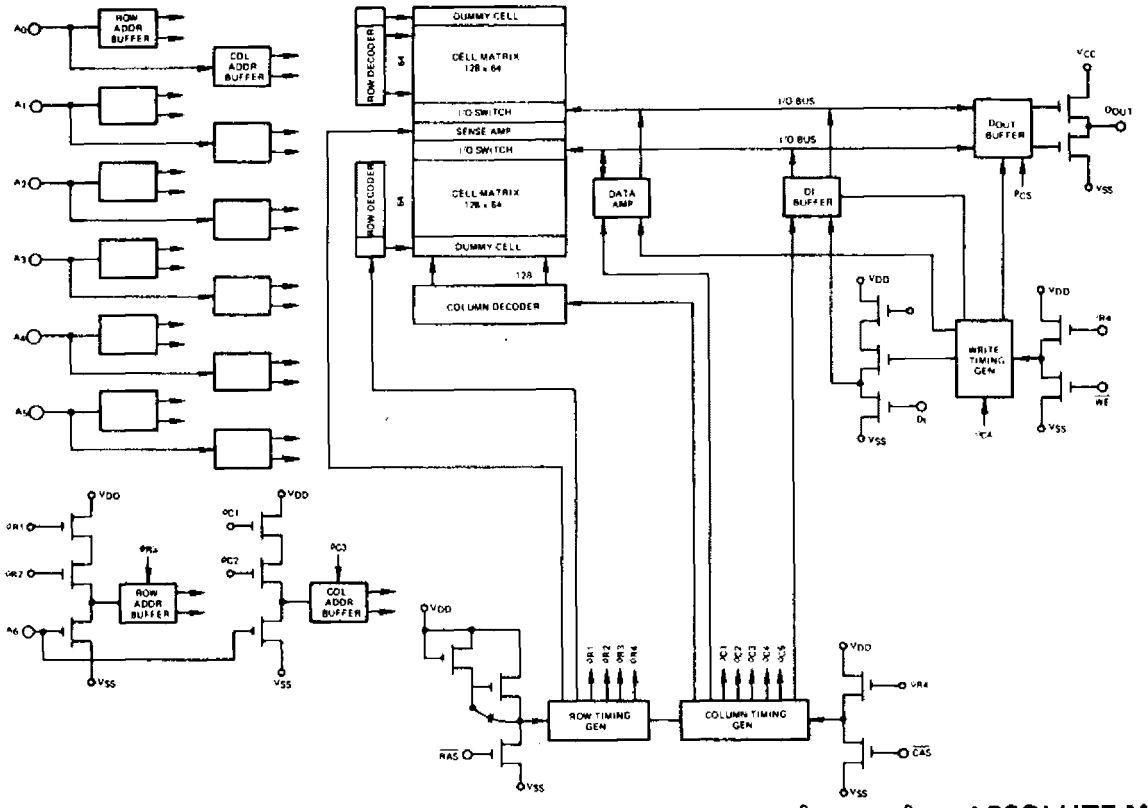
	ACCESS TIME	R/W CYCLE	RMW CYCLE
μPD416	300 ns	510 ns	575 ns
μPD416-1	250 ns	410 ns	465 ns
μPD416-2	200 ns	375 ns	375 ns
μPD416-3	150 ns	375 ns	375 ns
μPD416-5	120 ns	320 ns	320 ns

PIN CONFIGURATION



A_0-A_6	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write
V_{BB}	Power (-5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
All Output Voltages ①	−0.5 to +20 Volts
All Input Voltages ①	−0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC}, V_{SS} ①	−0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC} ②	−1.0 to +15 Volts
Short Circuit Output Current	50 mA
Power Dissipation	1 Watt

Notes: ① Relative to V_{BB}
② Relative to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{BB} = −5V ± 10%, V_{CC} = +5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance (A_0-A_6), D_{IN}	C_{I1}		4	5	pF	
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}		8	10	pF	
Output Capacitance (D_{OUT})	C_O		5	7	pF	

AC CHARACTERISTICS

T_a = 0°C to +70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS μPD416 MIN	μPD416 MAX	μPD416-1 MIN	μPD416-1 MAX	μPD416-2 MIN	μPD416-2 MAX	μPD416-3 MIN	μPD416-3 MAX	μPD416-5 MIN	μPD416-5 MAX	UNIT	TEST CONDITIONS
Random read or write cycle time	t_{RC}	510		410		375		320		320		ns	③
Read-write cycle time	t_{RWC}	575		465		375		375		320		ns	③
Page mode cycle time	t_{PC}	330		275		225		170		160		ns	
Access time from $\overline{RAS}$	t_{RAC}		300		250		200		150		120	ns	④ ⑥
Access time from $\overline{CAS}$	t_{CAC}		200		165		135		100		80	ns	⑤ ⑥
Output buffer turn-off delay	t_{OFF}	0	80	0	60	0	50	0	40	0	35	ns	⑦
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	35	3	35	ns	②
$\overline{RAS}$ precharge time	t_{RP}	200		150		120		100		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	300	10,000	250	10,000	200	32,000	150	32,000	120	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	200		165		135		100		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	200	10,000	165	10,000	135	10,000	100	10,000	80	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	40	100	35	85	25	65	20	50	15	40	ns	⑧
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	-20		-20		-20		-20		0		ns	
Row address set-up time	t_{ASR}	0		0		0		0		0		ns	
Row address hold time	t_{RAH}	40		35		25		20		15		ns	
Column address set-up time	t_{ASC}	-10		-10		-10		-10		-10		ns	
Column address hold time	t_{CAH}	90		75		55		45		40		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	190		160		120		95		80		ns	
Read command set-up time	t_{RCS}	0		0		0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		0		0		ns	
Write command hold time	t_{WCH}	90		75		55		45		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	190		160		120		95		80		ns	
Write command pulse width	t_{WP}	90		75		55		45		40		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	120		85		70		50		50		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	120		85		70		50		50		ns	
Data-in set-up time	t_{DS}	0		0		0		0		0		ns	⑨
Data-in hold time	t_{DH}	90		75		55		45		40		ns	⑨
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	190		160		120		95		80		ns	
CAS precharge time (for page mode cycle only)	t_{CP}	120		100		80		60		60		ns	
Refresh period	t_{REF}		2		2		2		2		2	ms	
$\overline{WRITE}$ command set-up time	t_{WCS}	-20		-20		-20		-20		0		ns	⑩
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	140		125		95		70		80		ns	⑩
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	240		200		160		120		120		ns	⑩

Notes:

① AC measurements assume t_T = 5 ns.

② V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}

③ The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_a ≤ 70°C) is assured.

④ Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.

⑤ Assumes that $t_{RCD} \geq t_{RCD}$ (max).

⑥ Measured with a load equivalent to 2 TTL loads and 100 pF.

⑦ t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

⑧ Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}

⑨ These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

⑩ t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) $\geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

DC CHARACTERISTICS

T_a = 0°C to +70°C (1), V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Supply Voltage	V_{DD}	10.8	12.0	13.2	V	(2)
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	(2) (3)
Supply Voltage	V_{SS}	0	0	0	V	(2)
Supply Voltage	V_{BB}	− 4.5	−5.0	−5.5	V	(2)
Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7		7.0	V	(2)
Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	V_{IH}	2.4		7.0	V	(2)
Input Low (Logic 0) Voltage, all inputs	V_{IL}	− 1.0		0.8	V	(2)
Operating V_{DD} Current	I_{DD1}			35	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} Min. (4)
Standby V_{DD} Current	I_{DD2}			1.5	mA	$\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance
Refresh V_{DD} Current — All Speeds except μPD416-5	I_{DD3}			25	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = 375 ns (4)
Refresh V_{DD} Current — μPD416-5	I_{DD3}			27	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = 375 ns (4)
Page Mode V_{DD} Current	I_{DD4}			27	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = 225 ns (4)
Operating V_{CC} Current	I_{CC1}				μA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = 375 ns (5)
Standby V_{CC} Current	I_{CC2}	-10		10	μA	$\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance
Refresh V_{CC} Current	I_{CC3}	−10		10	μA	$\overline{RAS}$ cycling, $\overline{CAS}$ - V_{IHC}, t_{RC} = 375 ns
Page Mode V_{CC} Current	I_{CC4}				μA	$\overline{RAS}$ - V_{IL}, $\overline{CAS}$ cycling, t_{PC} 225 ns (5)
Operating V_{BB} Current	I_{BB1}			200	μA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} 375 ns
Standby V_{BB} Current	I_{BB2}			100	μA	$\overline{RAS}$ = V_{IHC}, D_{OUT} High Impedance
Refresh V_{BB} Current	I_{BB3}			200	μA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}, t_{RC} = 375 ns
Page Mode V_{BB} Current	I_{BB4}			200	μA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = 225 ns
Input Leakage (any input)	$I_{I(L)}$	−10		10	μA	V_{BB} = −5V, 0V ≤ V_{IN} ≤ +7V, all other pins not under test = 0V
Output Leakage	$I_{O(L)}$	−10		10	μA	D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V
Output High Voltage (Logic 1)	V_{OH}	2.4			V	I_{OUT} = −5 mA (3)
Output Low Voltage (Logic 0)	V_{OL}			0.4	V	I_{OUT} = 4.2 mA

Notes: (1) T_a is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and high power dissipation is permissible, however, provided AC operating parameters are met. See Figure 1 for derating curve.

(2) All voltages referenced to V_{SS}.

(3) Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

(4) I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. See Figures 2, 3 and 4 for I_{DD} limits at other cycle rates.

(5) I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.

DERATING CURVES

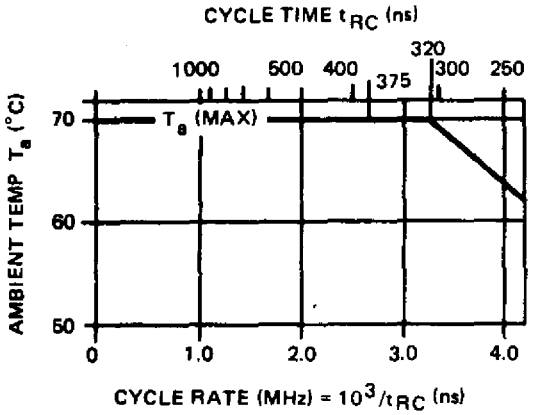


FIGURE 1

Maximum ambient temperature versus cycle rate for extended frequency operation. T_a (max) for operation at cycling rates greater than 2.66 MHz (t_{CYC} < 375 ns) is determined by T_a (max) [°C] = 70 – 9.0 x (cycle rate [MHz] –2.66). For μPD416-5, it is T_a (max) [°C] = 70 – 9.0 (cycle rate [MHz] – 3.125).

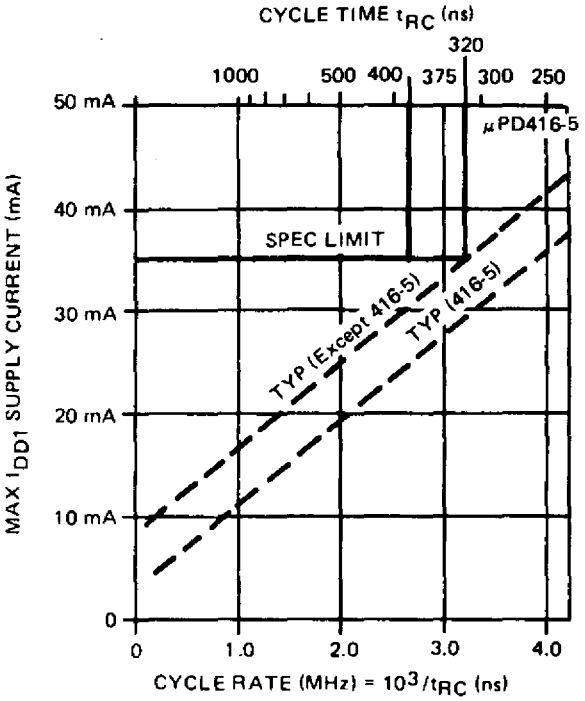


FIGURE 2

Maximum I_{DD1} versus cycle rate for device operation at extended frequencies.

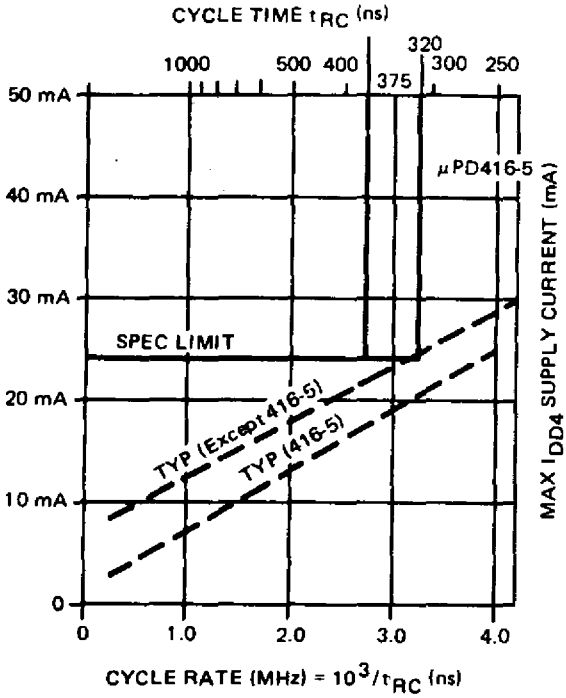


FIGURE 3

Maximum I_{DD3} versus cycle rate for device operation at extended frequencies.

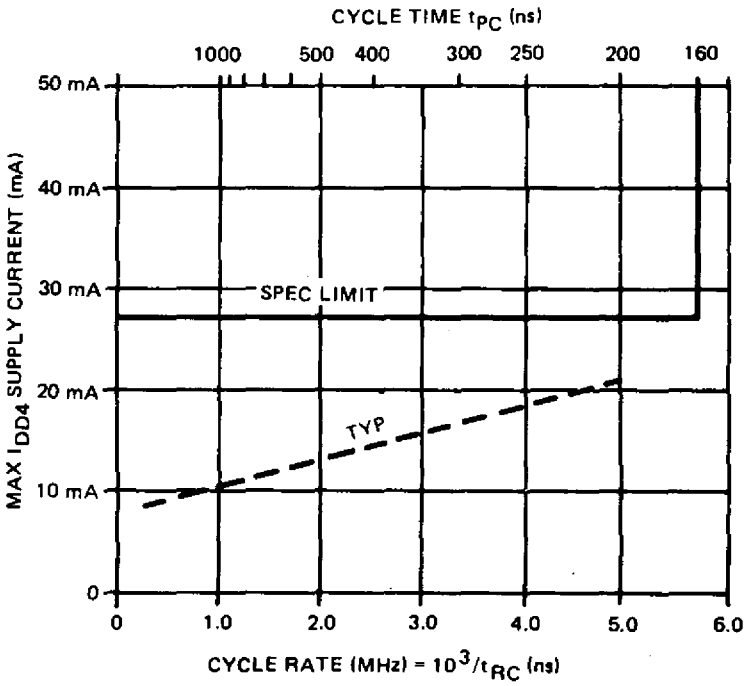
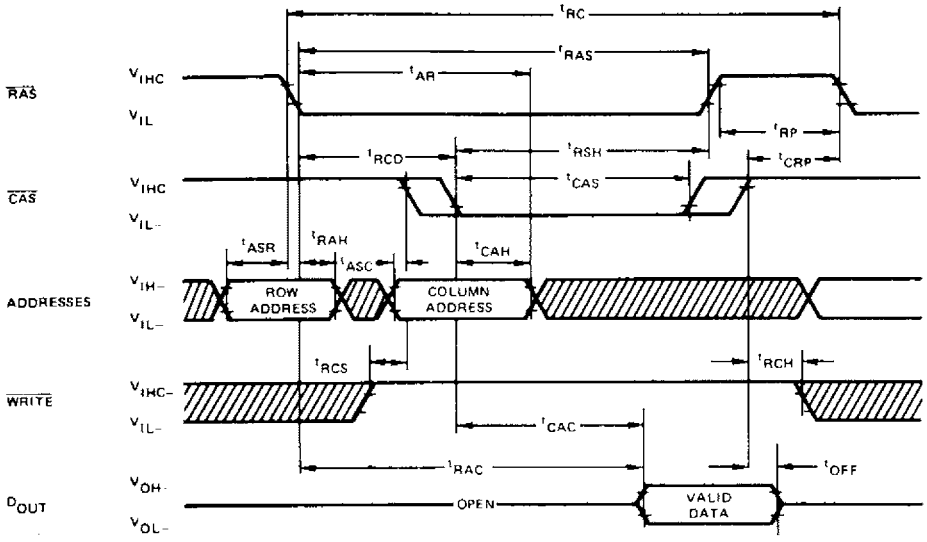


FIGURE 4

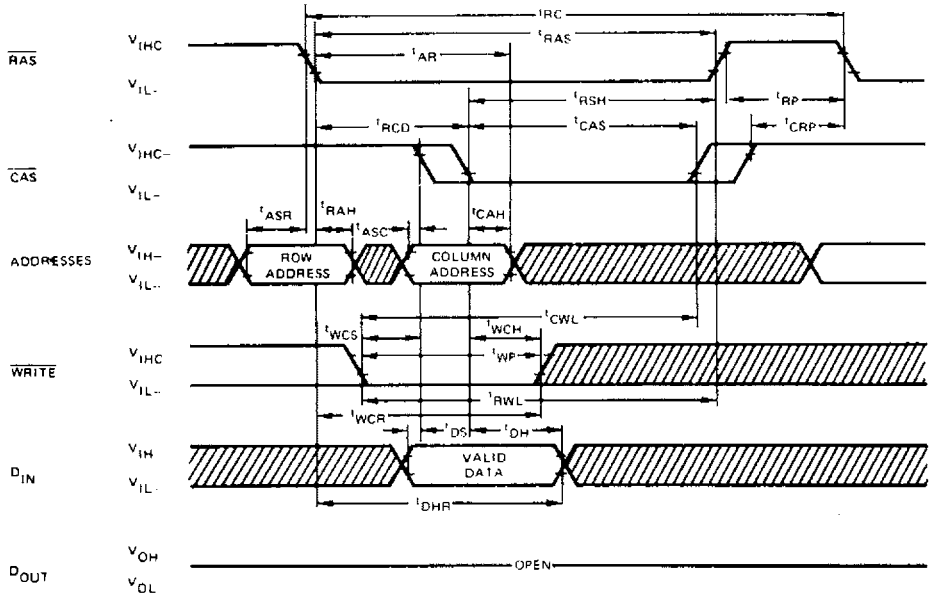
Maximum I_{DD4} versus cycle rate for device operation in page mode.

TIMING WAVEFORMS

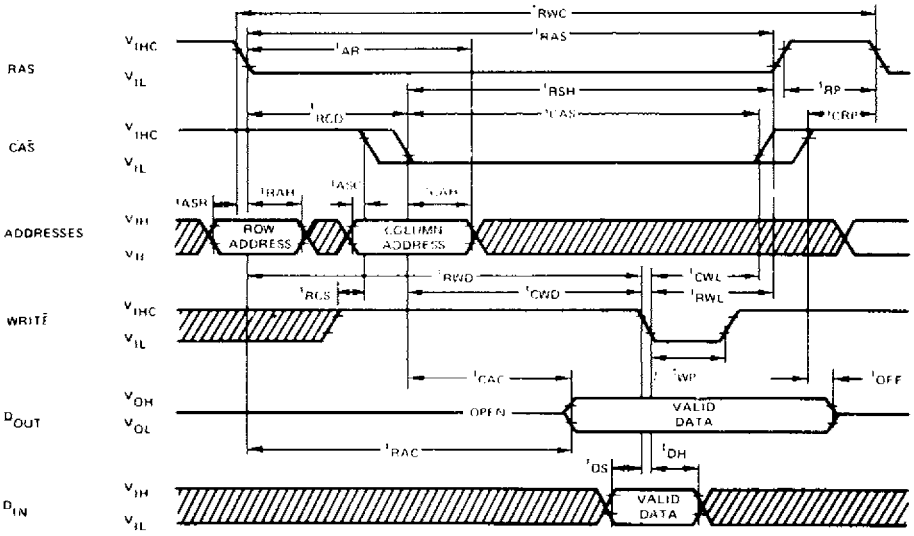
READ CYCLE



WRITE CYCLE

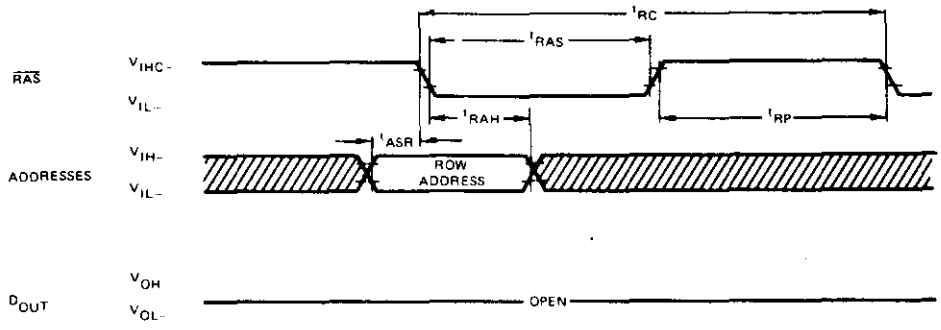


READ-WRITE/READ-MODIFY–WRITE CYCLE



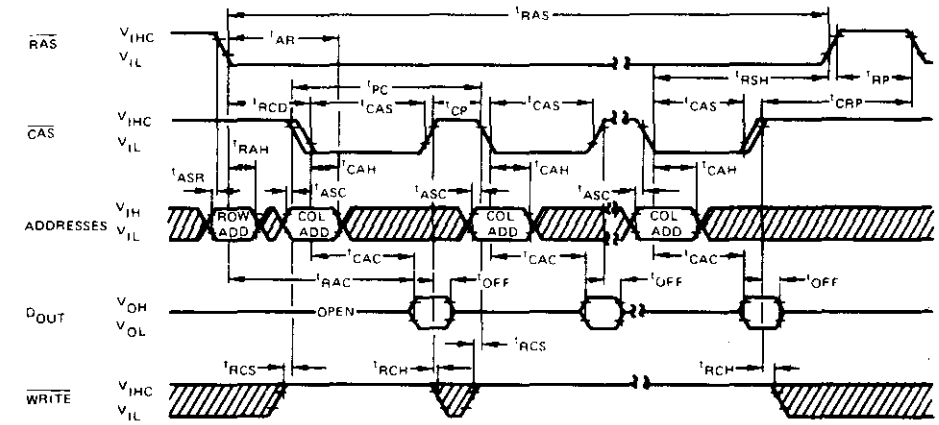
TIMING WAVEFORMS (CONT.)

"RAS-ONLY" REFRESH CYCLE

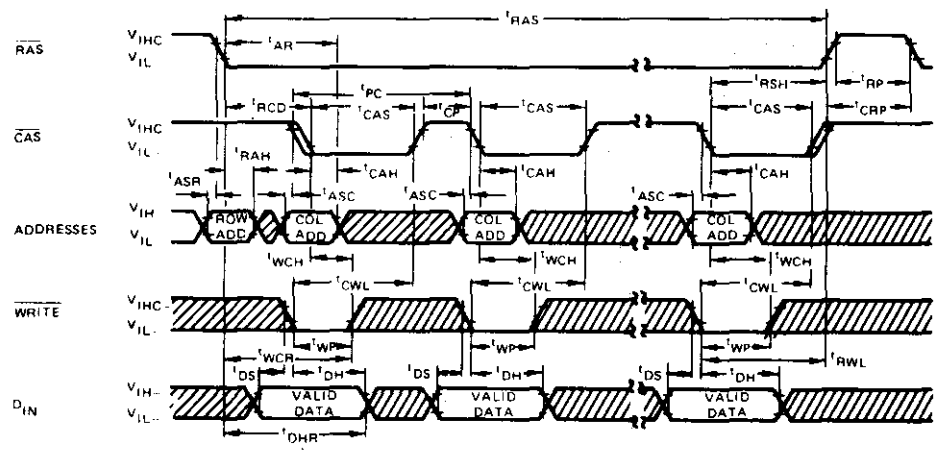


Note: CAS = V_{IHC}, WRITE = Don't Care

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



ADDRESSING

The 14 address bits required to decode 1 of 16,384 bit locations are multiplexed onto the 7 address pins and then latched on the chip with the use of the Row Address Strobe ($\overline{RAS}$), and the Column Address Strobe ($\overline{CAS}$). The 7 bit row address is first applied and $\overline{RAS}$ is then brought low. After the $\overline{RAS}$ hold time has elapsed, the 7 bit column address is applied and $\overline{CAS}$ is brought low. Since the column address is not needed internally until a time of t_{CRD} MAX after the row address, this multiplexing operation imposes no penalty on access time as long as $\overline{CAS}$ is applied no later than t_{CRD} MAX. If this time is exceeded, access time will be defined from $\overline{CAS}$ instead of $\overline{RAS}$.

DATA I/O

For a write operation, the input data is latched on the chip by the negative going edge of $\overline{WRITE}$ or $\overline{CAS}$, whichever occurs later. If $\overline{WRITE}$ is active before $\overline{CAS}$, this is an "early WRITE" cycle and data out will remain in the high impedance state throughout the cycle. For a READ, WRITE, OR READ-MODIFY-WRITE cycle, the data output will contain the data in the selected cell after the access time. Data out will assume the high impedance state anytime that $\overline{CAS}$ goes high.

PAGE MODE

The page mode feature allows the μPD416 to be read or written at multiple column addresses for the same row address. This is accomplished by maintaining a low on $\overline{RAS}$ and strobing the new column addresses with $\overline{CAS}$. This eliminates the setup and hold times for the row address resulting in faster operation.

REFRESH

Refresh of the memory matrix is accomplished by performing a memory cycle at each of the 128 row addresses every 2 milliseconds or less. Because data out is not latched, "$\overline{RAS}$ only" cycles can be used for simple refreshing operation.

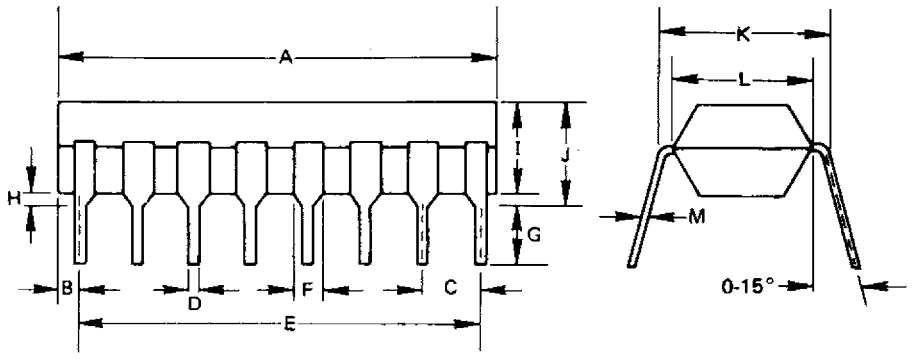
CHIP SELECTION

Either $\overline{RAS}$ and/or $\overline{CAS}$ can be decoded for chip select function. Unselected chip outputs will remain in the high impedance state.

POWER SEQUENCING

In order to assure long term reliability, V_{BB} should be applied first during power up and removed last during power down.

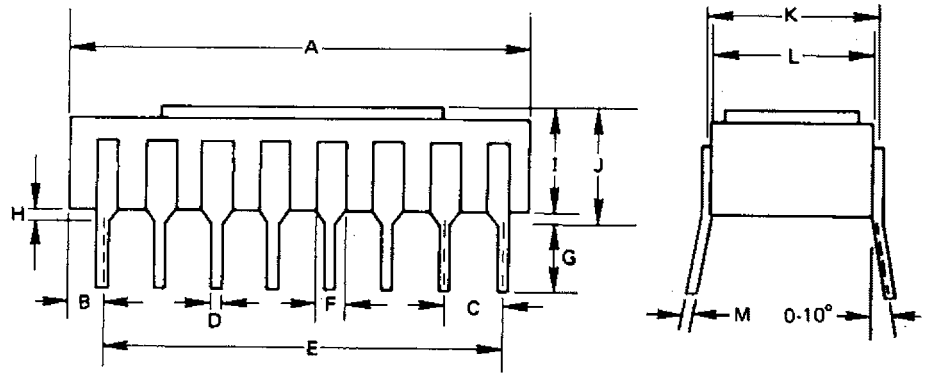
PACKAGE OUTLINE μPD416C



(Plastic)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

μPD416D



(Ceramic)

ITEM	MILLIMETERS	INCHES
A	20.5 MAX.	0.81 MAX.
B	1.36	0.05
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	3.5 MIN.	0.14 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.20 MAX.
K	7.6	0.30
L	7.3	0.29
M	0.27	0.01