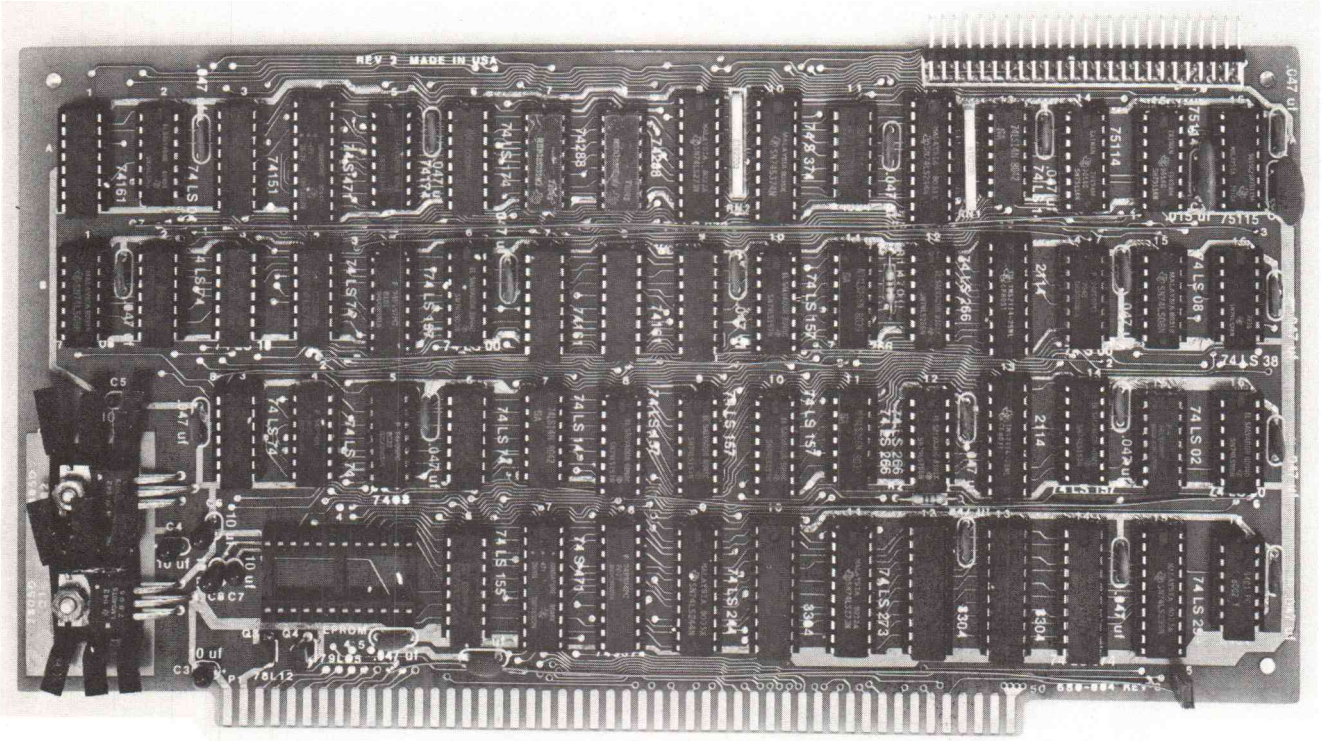
MICROMATION HARD DISK CONTROLLER

THEORY OF OPERATION

D01 040 Rev 4

MICROMATION HARD DISK CONTROLLER



Micromation's Hard Disk Controller is an integral part of the MARINER and M/SYSTEM computer systems. It provides the hardware interface for an 8" Winchester-type, hard disk drive with over 20 megabytes of formatted data storage area. As such, it complements single and multi-user M/NET systems by not only extending the system file storage capability beyond that available on floppy disk drive based computers but dramatically improving system performance as well. That is, hard disk accesses are performed significantly faster on a hard disk than a floppy diskette.

This speed advantage is perhaps most important in the M/NET multi-user environment. M/NET, the multi-processor architecture for S-100 based computer systems introduced by Micromation in 1980, allocates a separate CPU and 64K of memory to each operator -- an independent computer within the computer. This unique approach, employed in both the free-standing MARINER and functional rackmount M/SYSTEM cabinets, emphasizes high performance and low cost because the users are sharing the expensive peripherals, including the hard disk drive. It is here that speed is most important; operators become very impatient waiting for their program to load or to access data files.

Several Hard Disk Controller design features contribute to the system performance. For instance, the platters are formatted in 512 byte sectors to reduce access time overhead. In addition, the Controller has an on-board RAM buffer and sequential state machine. Thus, the system master (Micromation's Z-64 card) need only pass a command and parameters to the controller and transfer/retrieve data to/from the buffer. The remainder of the operation (head stepping, sector seeking, data read/write) is performed completely transparently to the master freeing it to perform other tasks. In the multi-user environment, the Controller indicates an operation is done via a system interrupt.

HOW TO USE THIS MANUAL

The Hard Disk Controller Manual is but one of the M/NET system volume provided to system integrators. Its function is to provide general theoretical support to those who wish or need to have an understanding of board operation. Note that this manual is not intended for end users nor does it contain installation or configuration information regarding the hard disk drive and controller. This information is contained in the M/NET User's Guide and M/NET Installation Guide, respectively.

This manual is divided into three sections. Section I provides an overview of the controller and it operations. It is intended to provide the reader with a conceptual understanding of the workings of the controller, in preparation for the detailed explanations contained in the remaining two sections. The section is complete to itself, and may be used independently of the rest of the manual to gain a less specific understanding of the theory of operation of the controller.

Section II provides a complete discussion of the interface between the controller and the host processor. This section will be of particular interest to those readers concerned with the software aspects of the system.

Finally, Section III contains a complete discussion of the hardware functions of the controller. Particular attention is paid to the sequential state machine, which is the heart of the controller.

TABLE OF CONTENTS

TABLE OF FIGURES

SECTION I

INTRODUCTION

1. MICROMATION HARD DISK CONTROLLER FEATURES

The Micromation Hard Disk Controller is a high performance Disk Controller designed to interface the Fujistu 8 inch Winchester hard disks to Micromation single and multi-user computer systems. It is a single S-100 board which provides all of the logic and control functions necessary to allow the users of Micromation M/NET systems to benefit from the performance and 20 megabyte storage capacity afforded by a Winchester hard disk.

The Hard Disk Controller is used in both single and multi-user M/NET systems. When used in a single user system, the controller provides the access speed and storage capacity required by many high performance stand-alone applications. Multi-user systems which employ the controller provide a per-user cost and performance which exceeds that available in single user, floppy disk based systems.

2. THE FUJITSU M2301 AND M2302 HARD DISK DRIVES

The Micromation Hard Disk Controller is designed to operate with the Fujistu M2302 drive. The unit provides 20.99 Megabytes of formatted storage. The M2302 contains 4 disk platters, providing 8 recording surfaces. The lower surface serves a dual purpose; it is one of the recording surfaces, as well as containing the clock servo track used to generate the PLO signal which synchronizes all read, write, and format operations between the controller and the disk drive.

The M2302 utilizes a unique head positioning band actuator which provides rapid head positioning to reduce access time significantly. In addition, the drive control logic provides two seek modes allowing individual steps; track to track, or a high speed seek operation optimized for the distance of the seek according to an ideal velocity curve stored in ROM.

3. OVERVIEW OF THE MICROMATION HARD DISK CONTROLLER

The Micromation Hard Disk Controller provides three important functions necessary for the control the Fujitsu drives. First, it provides the interface between the operating system and the head positioning logic allowing the proper sector to be selected. Secondly, it provides all of the buffering necessary to allow the Micromation system to transfer parallel data from memory to the disk and back. All high speed parallel-to-serial and serial-to-parallel conversion is performed by the controller. Finally, it transmits all status information from the drive to the operating system necessary to ensure error-free operation.

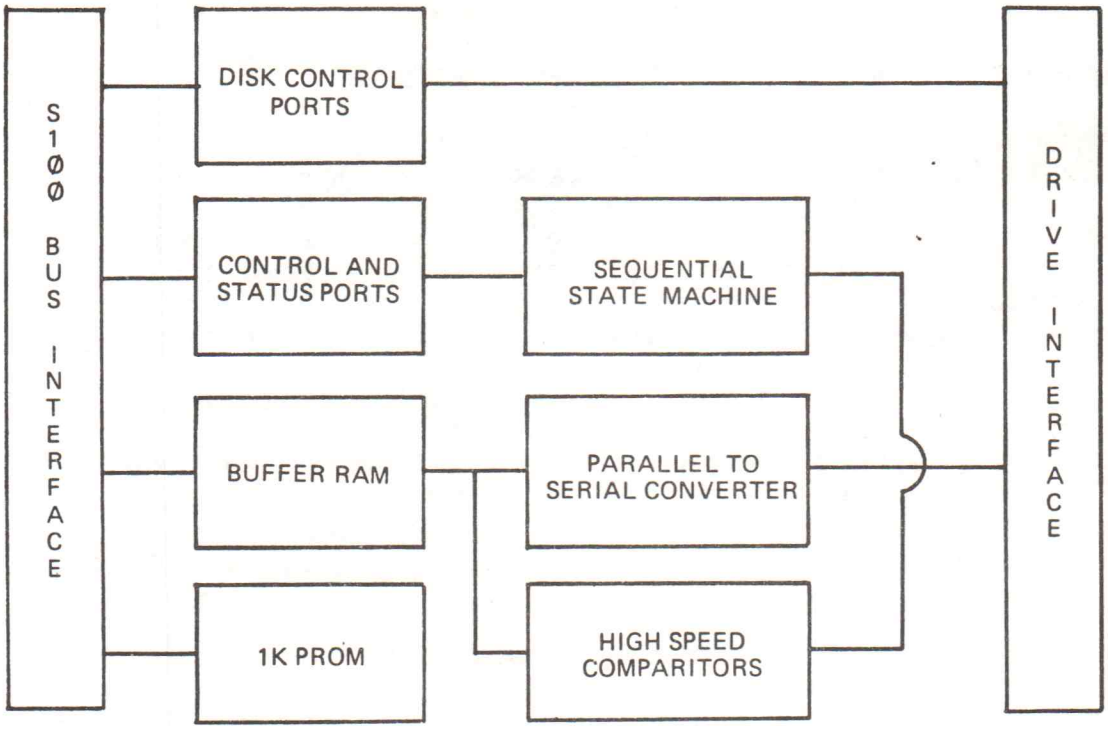


FIGURE I - 1

MICROMATION HARD DISK CONTROLLER BLOCK DIAGRAM

In order to understand the operation of the controller, it is helpful to divide the board into a number of functional units. Figure I - 1 shows the major functional blocks which comprise the Micromation Hard Disk Controller. Each block performs a function, largely independent of the other sections. Thus a divide-and-conquer approach to the explanation of the controller board will facilitate the understanding of its operation.

3-1 The S-100 Bus Interface

The controller board appears to its host system as a dedicated block of memory, 2K bytes in length, starting at F000H and running contiguously to F7FFH. The lower 1K bytes are assigned to the 24 pin socket IC-4D. This socket may be filled with a 2708 (1K bytes) PROM. This socket has no function on the controller other than to provide program storage for the operating system or for user supplied routines. It is currently unused by the Micromation single and Multi-user operating systems; however, it is best reserved for future expansion.

System memory addresses F400H through F7FFH contain the RAM buffer used by the controller board to transfer data to and from the hard disk. This static RAM memory consists of two 2114 (1K X 4) devices, IC-13B and IC-13C. The control logic of the control-

ler disables the S-100 control signals going to the buffer RAM when an actual sector transfer is underway, thus preventing potential conflict between the host processor and the on-board DMA logic. The PROM socket is not deselected during disk transfers and may be accessed by the host processor during the transfers.

The Fujitsu drive requires several control signals, in addition to the read, write, and clock signals for proper operation. These signals control the drive and head selection, head positioning, and general drive status.

Two I/O ports are used for these control signals. They appear as the CONTPORT (Control Port) which is addressed at 81H and STATPORT (Status Port) at 80H. CONTPORT may be written to only, and STATPORT may only be read. The host processor positions the head over the desired track using these ports.

Once the head is positioned over desired sector, the high speed data transfer occurs either to or from the disk. These transfers are executed by the sequential state machine portion of the controller, and not by the host system. In order to communicate with the sequential state machine, three additional I/O ports are used. They are the CODEPORT (Code Port), addressed at 82H, OPPORT (Operation Port) at 81H, and SECPORT (Sector Port) at 80H. CODEPORT is a write-only port used to pass commands to the sequential state machine, OPPORT is a read-only port which reports the status of the operation underway to the host system, and SECPORT is a write only port which is used to pass the desired sector number to the sequential state machine.

FUNCTION	I/O or MEM	RD or WR	ADDRESS
PROM*	MEMORY	READ ONLY	F000H TO F3FFH
BUFFER RAM	MEMORY	RD AND WR	F400H TO F7FFH
STATUS PORT	I/O	READ ONLY	80H
CONTROL PORT	I/O	WRITE ONLY	81H
SECTOR PORT	I/O	WRITE ONLY	80H
OPERATION PORT	I/O	READ ONLY	81H
CODE PORT	I/O	WRITE ONLY	82H

* The PROM is not used in either single or multi-user M/NET systems.

FIGURE I - 2

MEMORY BLOCK AND I/O PORT FUNCTION TABLE

In summary, the S-100 interface consists of two memory blocks and five I/O ports. The addresses and functions of these interface components are summarized in Figure I - 2 above.

3-2 Drive Interface

The hard disk drive is interfaced to the controller via a 50 pin flat cable connected to header J1. All control, data, and clock signals are passed between the controller and the drive over this cable. The signals on this cable may be divided into four functional groups; drive and head selection, head positioning, read/write data and clock signals, and drive status signals. Figure I - 3 gives the pin assignments and signal names for each of the four groups.

PIN	DESCRIPTION	SOURCE
	DRIVE AND HEAD SELECTION SIGNALS	
2	HEAD SELECT 0	CONTROLLER
4	HEAD SELECT 1	"
6	HEAD SELECT 2	"
8	HEAD SELECT 3	"
16	DRIVE SELECT	"
	HEAD POSITIONING SIGNALS	
24	DIRECTION	CONTROLLER
26	STEP	"
32	TRACK 00	DISK DRIVE
	READ/WRITE DATA AND CLOCK SIGNALS	
10	INDEX	DISK DRIVE
14	SECTOR	"
30	WRITE GATE	CONTROLLER
36	READ GATE	"
39	-WRITE DATA *	"
40	+WRITE DATA *	"
42	-WRITE CLOCK *	"
43	+WRITE CLOCK *	"
45	+PLO CLOCK *	DISK DRIVE
46	-PLO CLOCK *	"
48	+READ DATA *	"
49	-READ DATA *	"
	DRIVE STATUS SIGNALS	
12	READY	DISK DRIVE
28	FAULT CLEAR	CONTROLLER
34	WRITE FAULT	DISK DRIVE

* Indicates a balanced transmission signal

FIGURE I - 3

J1 PIN ASSIGNMENTS

In order to understand the purpose of each of the signals listed in Figure I - 3, we will examine a typical read/write sequence from start to finish. In general, four distinct phases occur in each read, write, or format operation, as listed below.

1. The drive is selected by bringing the DRIVE SELECT line low. The controller must then sample the READY line to ensure that the drive is ready to accept a command. Finally, the desired read/write head must be enabled by placing the binary coded number of the head on HEAD SELECT Ø - 3.

2. The head must be positioned over the desired track. This operation is accomplished with the STEP and DIRECTION lines. The tracks are numbered from Ø to 243, starting with Track Ø at the outer rim of the platter. If the head is currently positioned over Track Ø, the TRACK ØØ signal goes low. Note that all of the read/write heads move at once, since the hard disk drive employs a common head carriage. The controller must determine how many tracks the head carriage must move from its current position to the desired track, as well as the direction of the movement. The DIRECTION line determines whether or not the head carriage will move inward (if it is "1") or outward (toward Track ØØ if it is "Ø"). The drive will move one track for each pulse on the STEP line, in the direction indicated by the DIRECTION line.

3. Once the head is positioned over the desired track, the proper sector must be located. The disk drive signals the controller when the first sector is under the head by pulsing the INDEX line. In addition, each time a new sector is under the head, the SECTOR line is pulsed. Thus if the controller wishes to find the 14th sector on a given track, it waits for the INDEX pulse, and then counts 14 pulses on the SECTOR line. At this point, the head is over the desired sector, and data can be read or written. Depending on the operation selected, the WRITE GATE or READ GATE will go high, and data will be read from the disk on the READ DATA lines or written to the disk on the WRITE DATA lines. In order to synchronize the reading and writing of the data to and from the drive, the PLO lines are provided to indicate the proper bit clock timing.

4. When the read, write, or format operation is complete, the drive status may checked to make sure that the operation was completed successfully. The WRITE FAULT line is checked by the host processor if the operation was a write data or format, and the sector ID field is verified.

3-3 Sequential State Machine

The timing requirements of the drive selection and head positioning circuitry of the drive allow the Z-64 host processor to perform the necessary control in software. However, the data transfer rate supported by the hard disk drive far exceeds the capacity of the Z-64 to provide software control of the process. Therefore, a hardwired controller must be used to supervise the data transfer.

The Micromation Hard Disk Controller is capable of executing three read/write operations; read a sector, write a sector, and format a sector. Each of the operations may be further divided into reading and writing the ID field and reading and writing the DATA field portions of a sector. The sequential state machine is designed to perform these two sub-operations in the correct manner so as to execute the larger task of read, write, or format a sector.

In order to better understand the operation of the sequential state machine we must first examine the actual sector format. Figure I - 4 shows the format used on the controller. The sector is divided into two major sections or fields as we mentioned earlier; the ID field and the DATA field. Each of these two fields contains four subfields. These subfields are listed below.

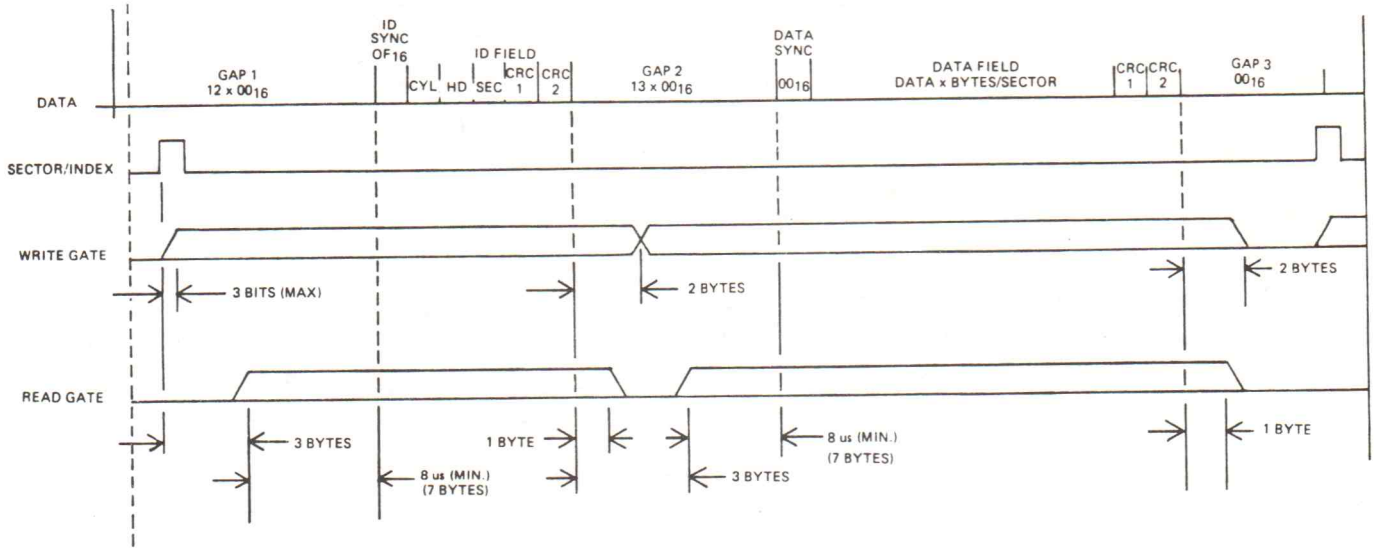


FIGURE I - 4

SECTOR FORMAT

A description of each sector field follows.

Gap: The first subfield is the Gap. The gap is a series of ØØH bytes designed to compensate for the displacement of the read/write head, circuit tolerances, and prevent any spurious transients, resulting from the removal of the write current from the head, from destroying any data.

Sync Byte: The Sync Byte marks the beginning of valid data in the field. The controller logic looks for the Sync Byte after the Gap in order to obtain byte synchronization with the incoming data stream. A sync byte is necessary due to the fact that there is a possibility of a timing skew between the Sector and Index pulses and the PLO clock.

ID or DATA: In the ID field, the head, track, sector, and any other identifying information follows the Sync Byte. In a DATA field the 512 data bytes follow the Sync Byte.

CRC Byte: The final subfield is the CRC (Cyclic Redundancy Check) Bytes. These are two bytes appended to the data or header information by the controller when the data is written to provide a means of determining whether or not the data was correctly read.

The sequential state machine then, must be capable of both reading and writing a sector ID field and a sector DATA field conforming to the format shown in Figure I - 4.

The sequential state machine is reset, or started when the controller logic indicates that the desired sector (loaded into SECPORT by the operating system) has been reached. The state machine then examines the format bit in the Control Port, and writes a new ID field to the disk if the operation is FORMAT A SECTOR, or reads the ID field if READ A SECTOR or WRITE A SECTOR has been selected. During non-format operations, the ID field is read in from the disk, and it is checked to verify that a seek error has not occurred, and that the head is correctly positioned. If a seek error is detected, the operation is aborted, and the error is reported to the operating system.

If the ID field is successfully read and verified, or when the writing is complete, in the case of a FORMAT A SECTOR operation, the sequential state machine begins the transfer of the data between the buffer and the disk. In FORMAT and WRITE operations, data is transferred from the buffer to the disk, and from the disk to the buffer during READ operations.

At the end of the read or write DATA field phase, the state machine informs the host processor that the operation is complete, and in the case of a read, that the desired data may now be read from the RAM buffer by the operating system. At this point the cycle is complete and the state machine enters a FINISH state, waiting for the next operation.

SECTION II

SYSTEM INTERFACE

1 COMMANDS

The Micromation Hard Disk Controller supports three commands from the host processor; Read a sector, Write a sector, and Format a sector. The following section details the protocol between the host processor and the controller necessary to execute each of these commands.

1-1 Head Positioning

Prior to issuing a READ, WRITE, or FORMAT command to the controller, the host processor must be certain that the correct head is selected, that the head is over the proper track, and that the desired sector has been located. The timing of these events is slow enough that these tasks are implemented by the host processor.

The first task the operating system must perform during a head positioning operation is the conversion between logical drive, track, and sector information, to physical track, sector, and head number information. The actual conversion algorithm is not important to the understanding of the controller operation. Suffice it to say that the end product of the conversion is a track number, sector number, and head number defining the actual sector of interest.

There are three I/O port which are used by the operating system to correctly position the head over the desired sector; CONTPORT (81H Write), STATPORT (80H Read), and SECPORT (80H Write). Figure II - 1 below lists each of the ports and the function of each of the bits in the ports.

STATPORT 80H READ		CONTPORT 81H WRITE		SECPORT 80H READ	
BIT	FUNCTION	BIT	FUNCTION	BIT	FUNCTION
D0	NO CONNECTION	D0	/STEP	D0	0 OF SECTOR #
D1	" "	D1	DIRECTION	D1	1 " " "
D2	" "	D2	/FAULT CLEAR	D2	2 " " "
D3	" "	D3	/DRIVE SELECT	D3	3 " " "
D4	/WRITE FAULT	D4	HEAD ADDRESS 0	D4	4 " " "
D5	TRACK 00	D5	" " 1	D5	5 " " "
D6	/SEEK DONE	D6	" " 2	D6	6 " " "
D7	/READY	D7	" " 3	D7	SEEK INT ENABLE

FIGURE II - 1

BIT ASSIGNMENTS FOR I/O PORTS

When the host system is reset, the drive must be initialized. This is accomplished by setting bits D2 and D3 in CONTPORT low, selecting the drive and clearing the Write Fault flip-flop in the drive control logic. When power is applied to the drive unit, there is a delay of 20 seconds while the DC spindle motor brings the platters to their proper rotational speed. During this time, the /READY line from the drive is high, indicating that the drive may not be accessed.

When the READY line goes low, the controller must determine what track the heads are currently on. While in most cases the heads will be over track 0, this is not guaranteed and the host processor must test bit D5 of STATPORT. If the TRACK 0 bit is not set, the host system must step the head carriage one track at a time, as described below, until it is over track 0. Once the drive responds with a Track 0 indication, the operating system keeps the current track number in memory so that the drive need only be reset to track 0 if an ID error is encountered.

The hard disk drive supports two seek modes, a single step and an accelerated seek. In the single step mode, the drive responds to each pulse on the STEP line as it occurs. This mode is useful when resetting the drive to track 0 during power-on initialization and after an ID error is encountered. The minimum track to track step time for the drive is 30ms. Therefore, the host processor must be certain that the head is not stepped faster than this when looking for track 0. This will allow for the heads to settle mechanically, and actuate the internal TRACK 00 indicator.

The accelerated seek mode allows for more rapid positioning of the head when the seek involves a large number of steps. The controller pulses the STEP line once for each desired step, as with the single step mode. However, the disk drive control logic accelerates and decelerates the track to track motion of the head based on an ideal velocity curve stored in ROM for the number of tracks to be traversed.

The hard disk drive differentiates between the two seek modes by determining the rate of the pulse stream on the STEP line. If the STEP line is pulsed at a rate of less then 1 KHz, the single step mode is selected. The accelerated seek mode is selected when the STEP line pulse rate is between 3 KHz and 3 MHz. Pulse rates between 1 KHz and 3 KHz and over 3 MHz are prohibited. The drive control logic responds to pulse widths as short as 100 ns. Therefore the host processor need not be concerned with this requirement, since it can not generate a pulse width any shorter than about 5000 ns.

The direction of the seek is controlled in both modes by bit D1 of CONTPORT for both seek modes. When this bit is set, the direction of the seek is toward the center of the platter and from a lower numbered track to a higher numbered track. If the bit is not set, the seek is towards the rim of the platter and Track 0.

At the start of a seek operation, in either mode, the SEEK COMPLETE line will go high and remain there until the seek, including settling time, is complete. The line will go low and remain there until the next seek operation is initiated. The host processor may poll the STATPORT and test bit D6 to determine if the seek is complete, or bit D7 of SECPORT may be set which instructs the controller to issue an interrupt when the SEEK COMPLETE line from the drive goes low.

Once the seek is complete the host processor must select the proper head and the desired sector. The head is selected by placing the binary head code in bits D4 through D7 of CONTPORT. The actual head assignments are shown in Figure II - 2. The sector number is selected in a similar manner by placing the binary coded sector number in bits D0 through D6 of SECPORT. Note however, that the controller does not determine if a valid sector number is being requested. The standard 512 byte sectors used with the Micromation operating systems yield 21 sectors per track. Since the sector counter is reset every disk revolution (by the Index line), any sector number larger than 21 will not be found by the controller.

Once these steps listed above have been performed by the host processor, the controller is ready to accept a FORMAT, READ, or WRITE command. The procedure for these commands are listed in the following paragraphs. While each of these three operations are distinctly different, the sector selection protocol which precedes them is identical.

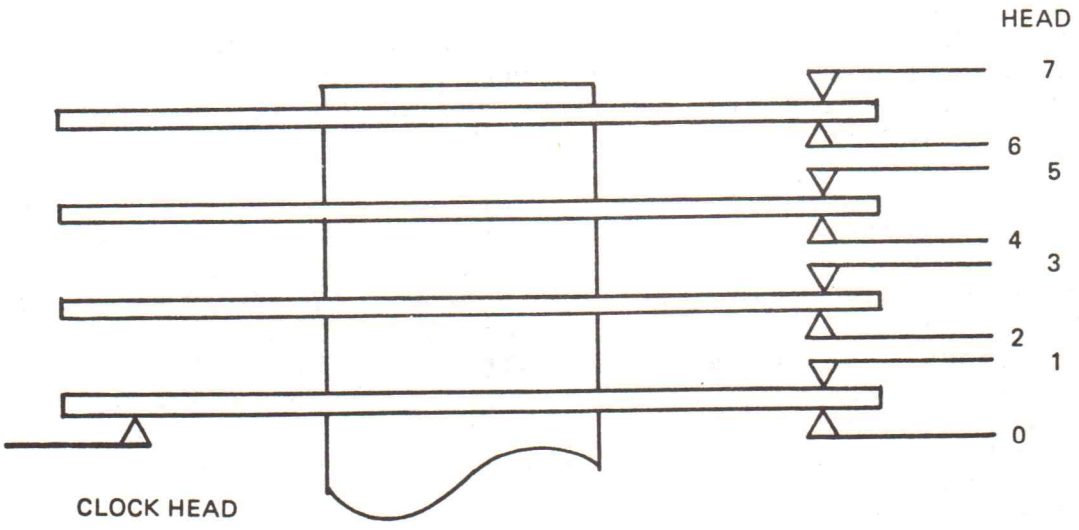


FIGURE II - 2

READ/WRITE HEAD NUMBERS

1-2 Read, Write, and Format Commands

The READ, WRITE and FORMAT commands are executed by the controller's sequential state machine. The host system communicates with the state machine via two I/O ports, CODEPORT (82H Write) and OPPORT (81H Read). Figure II - 3 lists each of the two ports and the function of each of the bits in each port.

CODEPORT 82H WRITE		OPPORT 81H READ	
BIT	FUNCTION	BIT	FUNCTION
D0	READ/WRITE SEL	D0	SSM STATUS CODE
D1	FORMAT SEL	D1	" " "
D2	START DISK OP	D2	" " "
D3	INTERRUPT EN	D3	" " "
D4	ADDRESS PRESET	D4	" " "
D5	" "	D5	FINISH
D6	" "	D6	QA COUNTER
D7	" "	D7	QB "

FIGURE II - 3

BIT ASSIGNMENTS FOR COMMAND I/O PORTS

CODEPORT Bits D0 and D1 (READ/WRITE SEL and FORMAT SEL, respectively) select the type of operation to be performed according to the truth table below.

D0	D1	Operation
0	0	Write A Sector
0	1	Read A Sector
1	0	Format A Sector
1	1	Format A Sector

CODEPORT Bit D2 is used to signal the state machine to begin an operation. The operating system must make certain that all parameters are set up prior to setting this bit high. **The Interrupt Enable bit D3** is set when the operating system requires an interrupt to be generated when the sector operation is complete. **The FINISH bit, D5 of OPPORT,** will also indicate the end of the transfer, so that polled operation is supported. The Micromation M/NET multi-user systems use the interrupt driven mode, while the polled mode is used in single user systems.

The **CODEPORT ADDRESS PRESET bits D4 through D7** allow the controller hardware to read and write sector lengths other than 512 bytes. The switch settings must correspond with the sector length defined by the switch bank on the hard disk drive. Refer to the Fujitsu hard disk reference manual for these switch settings and sector lengths. When using 512 byte sectors the upper

nibble of CODEPORT should always be set to 1000 binary with D7 set to binary 1.

Once the command contained in D0 and D1 of the CODEPORT has been transferred to the state machine for execution by setting bit D2 high, the state machine will execute the command without further intervention by the host processor. However, if the host wishes to determine the status of the operation underway, it may read OPPORT and examine bits D0 through D4. These bits contain a five bit code indicating the current state of the sequential state machine. The code ranges from 00H to 1FH, and correspond to the states described in the state diagram in Section 3 of this manual, as follows.

CODE	STATE
06H	0CH
0CH	06H
0EH	0EH
11H	11H
14H	05H
16H	0DH
1CH	07H

In addition to the status code, OPPORT bit D5 indicates the completion of the operation. The FINISH line goes low at the beginning of the operation, and high at the completion. The single user Micromation operating system uses this bit to signal the end of the transfer. The two remaining bits in OPPORT are primarily used for testing and debugging the controller. They are the two least significant bits of the DMA address counter, and indicate a transfer underway.

2 DATA TRANSFER

The on-board RAM buffer is used as the buffer for data between the controller and the host processor. The buffer contains 1K of memory starting with address F400H and running to F7FFH. The sector size used in the Micromation single user and Multi-user operating systems is 512 bytes. Thus, the buffer is actually divided into 512 bytes of data buffer, and 512 free bytes, the first 64 of which are used by the state machine for ID header identification.

The controller logic does not contain the on-board logic required to generate the ID field. Since the ID field contains the track, sector, and head numbers of the sector, each ID field is unique. Figure II - 4 shows the format of the ID fields used in the Micromation Hard Disk system. Therefore, the host system must provide the controller with the ID field for each sector. The lower 64 bytes of the RAM buffer are reserved for this purpose. The host processor must place the ID field into the buffer prior to instructing the controller to begin an operation.

During a FORMAT operation, the ID field contained in the buffer is written to the disk. During READ and WRITE operations, the ID field from the disk is read by the controller, and compared on a byte by byte basis with the ID field contained in the buffer. If the two match, the controller has found the desired sector.

SYNC BYTE ØDH	TRACK	HEAD	SECTOR	CRC1	CRC2

FIGURE II - 4

SECTOR ID FIELD FORMAT

The controller requires the data buffer to be positioned in the uppermost bytes of the RAM buffer. This in conjunction with the ID field in the lower 64 bytes yields the address map shown in Figure II - 5.

During a WRITE operation, the data to be written to the sector are moved into the upper 512 bytes of the buffer. Conversely, the data read from a sector during a READ operation is available in the buffer at the successful completion of the operation. A FORMAT operation requires the data field in each sector to be initialized to a specified value. The Micromation operating systems use the hexadecimal value E5H. Thus, the operating system must fill the buffer with this initialization value prior to initiating a FORMAT command.

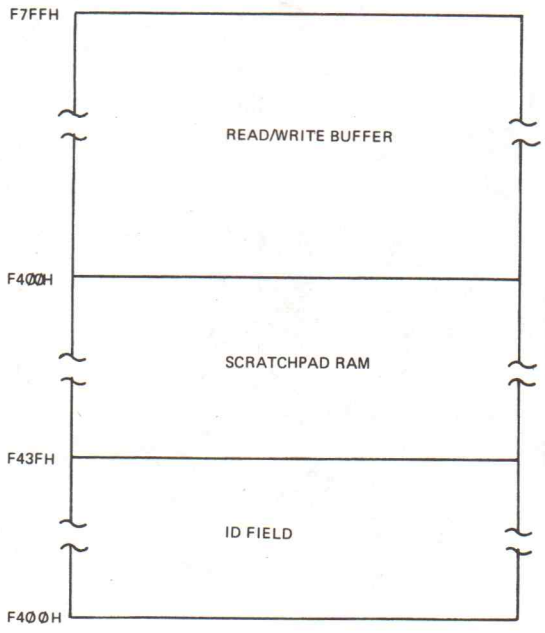
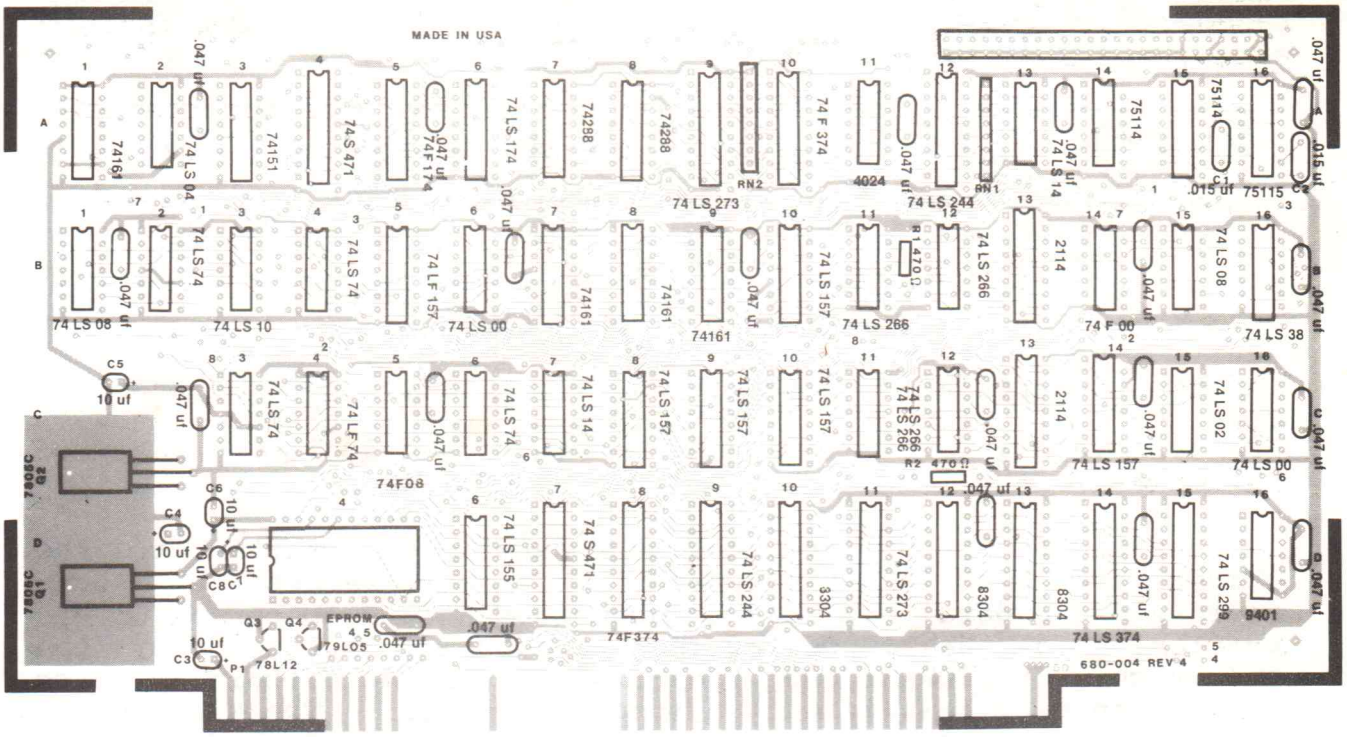


FIGURE II - 5

BUFFER RAM MEMORY MAP

SECTION III

HARDWARE DESCRIPTION



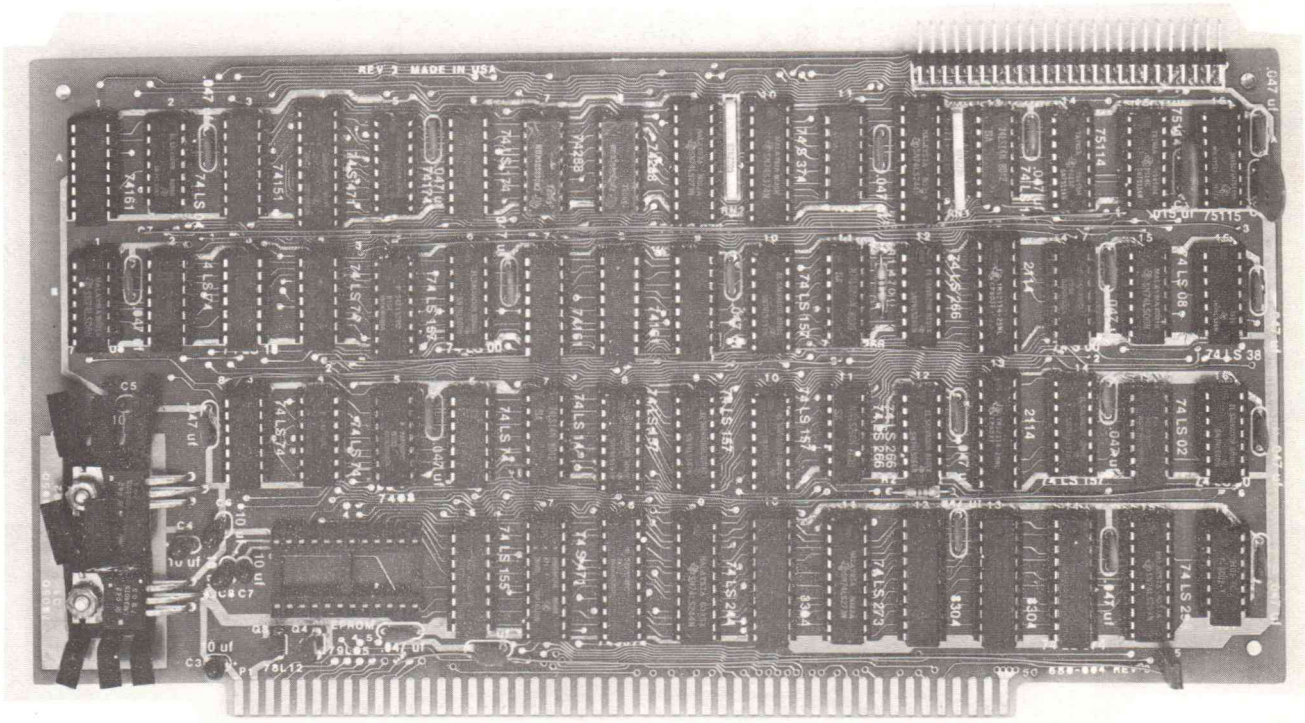


FIGURE III - 1

HARD DISK CONTROLLER PHOTO AND SILKSCREEN

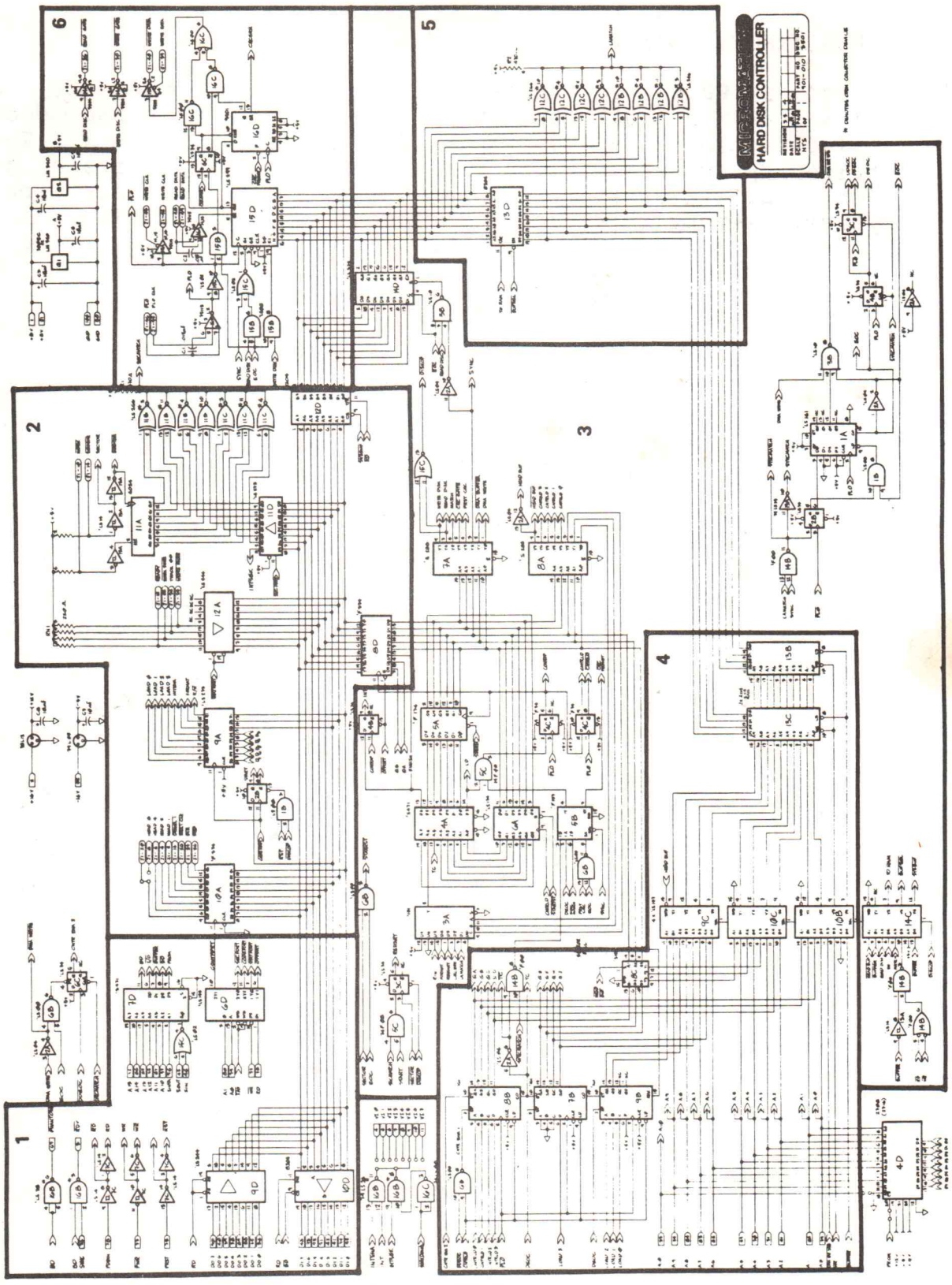


FIGURE III - 2

SEGMENTED SCHEMATIC DIAGRAM

1 BUS MEMORY INTERFACE

The S-100 bus interface to the two memory components (buffer RAM and PROM socket) consists of the address lines and decoders, a bi-directional data bus, and several control lines. The controller provides phantom memory control and wait state generation, as well as multiplexing the buffer RAM between the host system's memory space and the sequential state machine.

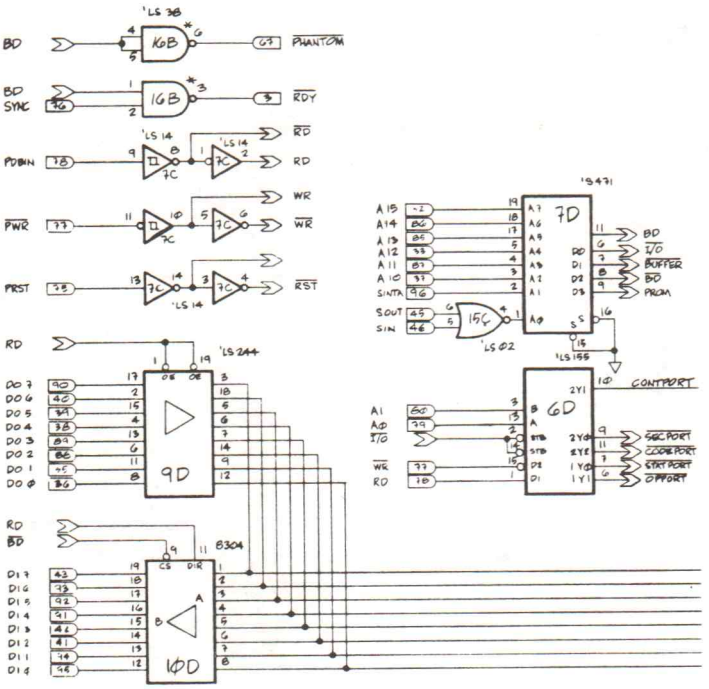


FIGURE III - 3

ADDRESS DECODING LOGIC
S-100 BUS INTERFACE

1-1 Address Decoding

The S-100 bus address lines **A0 - A15** are decoded by a decoder PROM IC-7D. Figure III - 3 show the address decoding circuitry for the memory and I/O ports. The outputs of the PROM enable selected devices on the controller board. The board enable signal **BD** is generated whenever the address lines **A10 - A15** select the PROM (F000H - F3FFH) or the buffer RAM (F400H - F5FFH). When the memory is selected, the **BD** line is inverted and controls the **/PHANTOM** (S-100 pin 67) line on the bus. The PHANTOM line disables any overlapping system memory. This signal allows the controller board to be compatible with host processors with a full 64K of memory, such as the Z-64. In addition to **A10 - A15,** the processor interrupt acknowledge signal **SINTA** is input to the decoder PROM to disable the controller board during an interrupt acknowledge cycle.

The **BD** signal is also used to generate a single wait state each time the board is accessed. This ensures that the minimum access time requirements of the on-board memory will be meet. The **BD** signal is ANDed with the processor **SYNC** signal, using IC-16B, to generate **/RDY.**

Although PROM memory would always be available to the host processor, the buffer RAM is removed from the system's memory during disk transfers to eliminate contention between the host processor and the sequential state machine. The address and control lines to the RAM are multiplexed using IC-9C, IC-10C, and IC-10B. The **/DISKOP** signal, which is generated by the state machine, is used as the control signal for the multiplexers. This signal is low when a sector transfer is under way, and effectively blocks all address and control signals generated by the host processor.

1-2 Bi-Directional Data Bus

The S-100 bus contains separate data input and output lines. These lines are combined using IC-9D and IC-10D to form an internal bi-directional data bus. This internal bus connects to all of the on-board memory and I/O components.

The direction of data flow on the internal bus and through the buffers is controlled by the **RD** line which is generated from the bus signal **PDBIN. PDBIN** is an output from the processor that strobes data from the controller to the processor.

2 I/O Port Interface

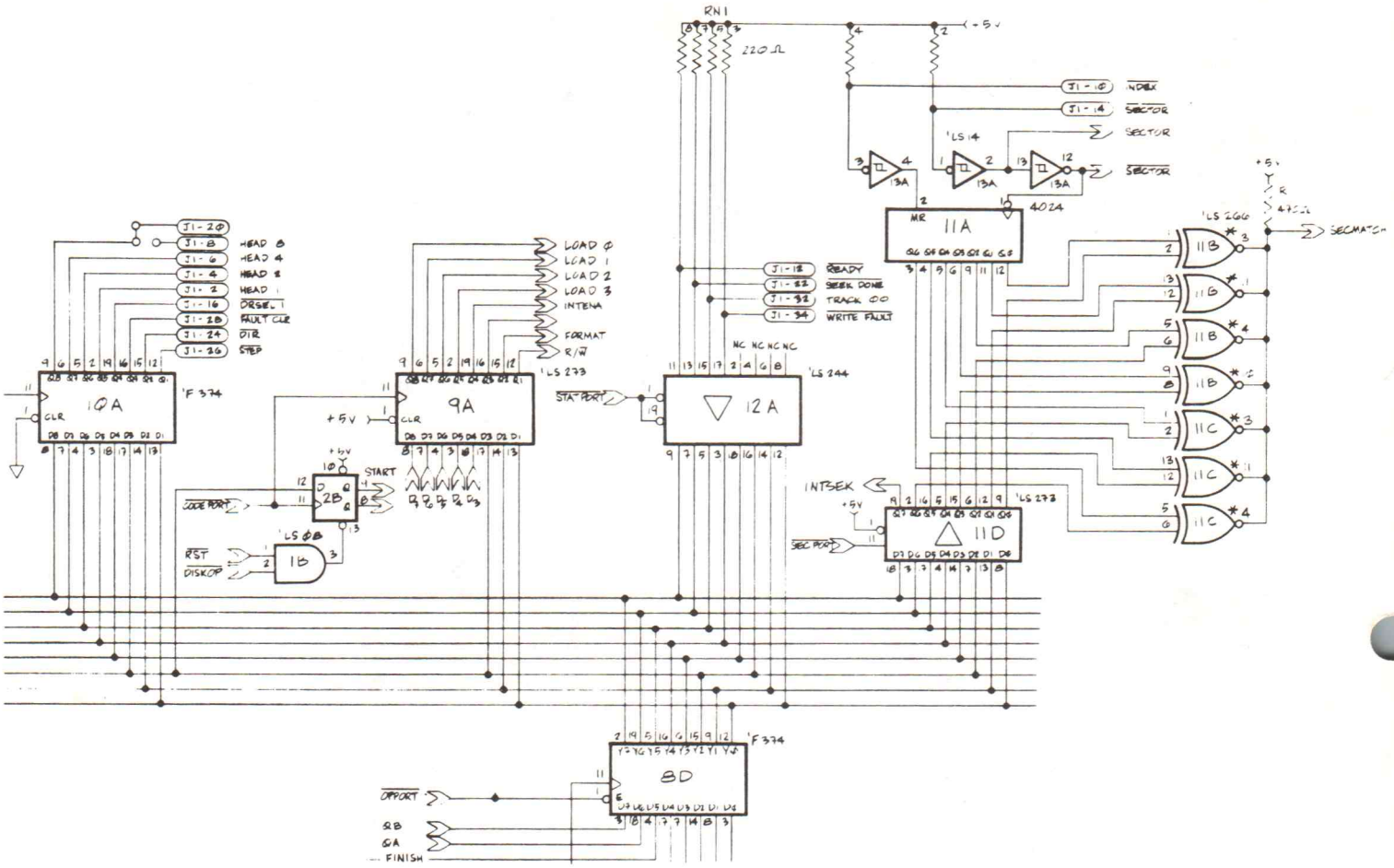


FIGURE III - 4

I/O PORT INTERFACE

The operating system controls the hard disk drive and state machine via 5 I/O ports. The I/O signal from the address decoder (shown in Figure III - 4) is used to enable the I/O port decoder IC-6D. This decoder uses the lower two address bits A0 and A1, the internal read and write controls, and the I/O signal to select the proper port.

Each of the five ports consists of a latch. Data is transferred to or from the internal data bus when the select line from the decoder strobes one of the latches. The five latches are IC-10A, IC-9A, IC-12A, IC-11D, and IC-8D. These are CONTPORT, CODEPORT, STATPORT, SECPORT, and OPPORT, respectively. Figure III - 4 illustrates the logic.

Regarding the data direction vis-a-vis each port:

CONTPORT CODEPORT SECPORT	all read from the data bus
STATPORT OPPORT	both output to the data bus

The SECPORT is used to determine when the sector sought matches that found on the platter. The sector value is loaded into the SECPORT before the seek is begun. When the INDEX hole on the drive is encountered, the signal resets the 4024 counter at IC-11A. Subsequently, each sector hole encountered increments the counter by one. When the values in IC-11A and IC-11D match, the open collectors IC-11B and IC-11C render an active SECMATCH.

Notice that the CONTPORT latch outputs directly to the hard disk drive to select the head and drive, clear the fault bit, and set the /DIR (direction) and /STEP bits.

CODEPORT outputs to the sequential state machine and the DMA address multiplexer logic as well as enabling the interrupt signal signal.

STATPORT transfers status signals from the drive to the data bus. These signals indicate that the drive is ready, the seek is completed, the head is at track 00, and that a write fault has happened.

Finally, OPPORT is tied to the sequential state machine and is read to determine the current state.

3 Sequential State Machine

The sequential state machine controls the data transfers between the hard disk and the buffer RAM. The high data transfer rates encountered in hard disk systems cannot be processed by the host processor using software techniques, and therefore requires some form of hardware control.

Figure III - 5 shows the format of a disk sector, and correlates the state machine states with the format during each of the three operations. The state machine codes discussed in Section II, 1-1 of this manual indicate which state the state machine is in. The state machine codes may be read by the host processor through OPPORT (81H, read). A comparison between Figures III - 5 and III - 6 will give a better understanding of the process performed by the state machine.

	GAP1	ID SYNC	TR/HE/SEC DATA FIELD	CRC1 CRC2	GAP2	DATA SYNC	DATA	CRC1 CRC2	GAP3
1)	01 18	1F	1D	1C	19	16	12	13	11
2)	01 02 03	07	05	04	06 08 10	16	12	13	11
3)	01 02 03	07	05	04	06 08 09	0E	0A	0B	0C 0D

Where 1) is a FORMAT operation
2) is a READ operation
3) is a WRITE operation

FIGURE III - 5

DISK SECTOR FORMAT AND CORRESPONDING MACHINE STATE

3-1 State Diagram

The key to understanding the operation of the sequential state machine is a familiarity with the tasks to be performed by the machine, and the conditions which are used to control the progress from one state to another. A type of flowchart, called a state diagram, is usually used to show these conditions. Figure III - 5 is the state diagram for the controller.

The task performed during each state is given inside each of the circles (representing a finite state). The duration of the state is listed to the left of each state, and is given in terms of byte clocks. A code indentifying each state is listed to the right of each state. Finally, the conditions which determine the flow of the state machine at junction points is given at all decision points.

The state machine is reset to its initial state each time the host processor sets the START OPERATION bit D2 in CODEPORT, and the sector counter value matches the sector number written to SECPORT by the operating system. This will occur when the SECTOR

line from the drive interface increments the sector counter IC-11A, and the output of the comparator formed by IC-11B and IC-11C show a match with the value contained on the output of the SECPORT latch IC-11D. The sector counter is reset to zero by each INDEX pulse from the drive.

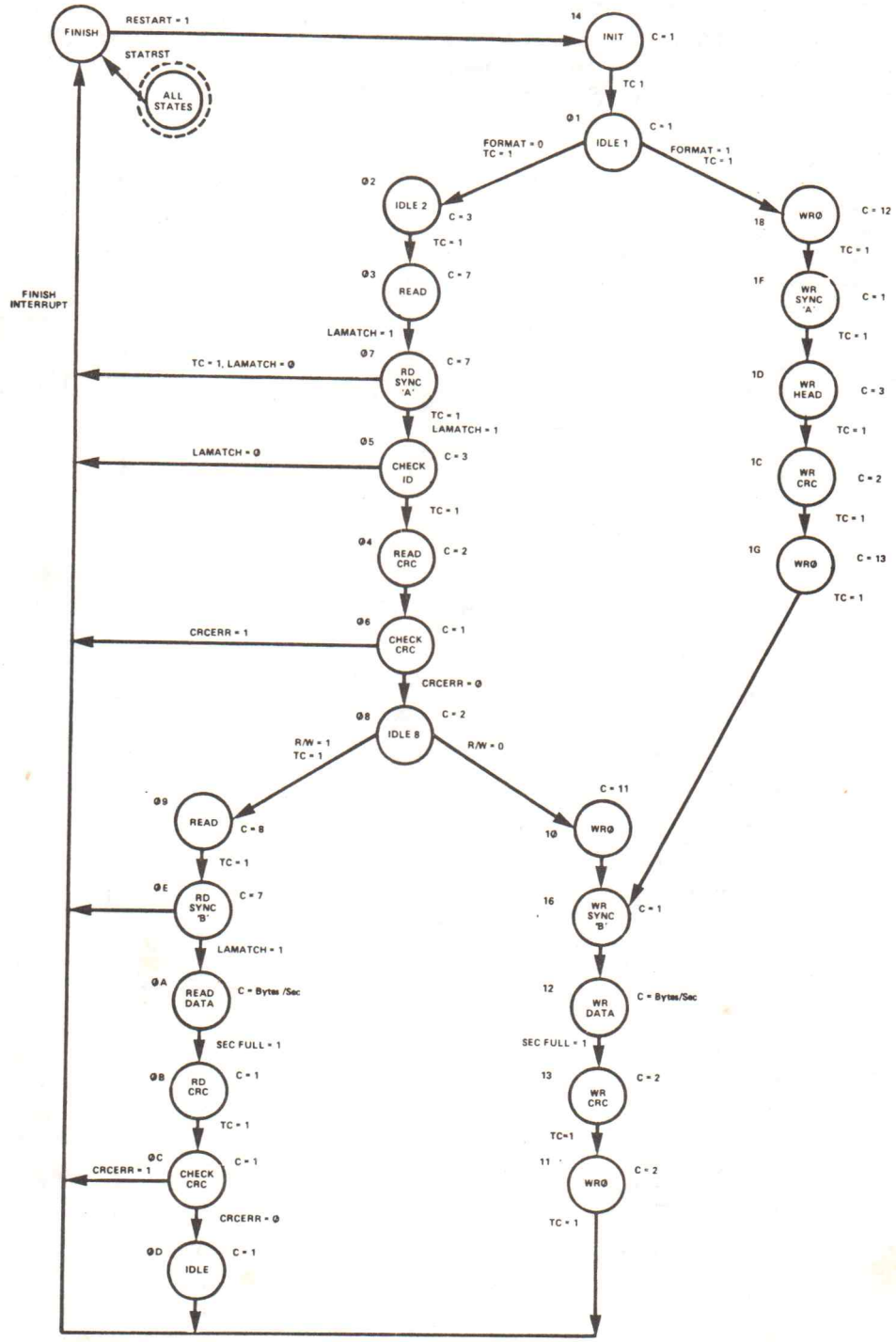


FIGURE III - 6

SEQUENTIAL STATE MACHINE STATE DIAGRAM

3-2 Sequential State Machine Circuitry

The sequential state machine consists of control PROM IC-4A, hex latches IC-5A and IC-6A, decode PROMs IC-7A and IC-8A, and control multiplexer IC-3A. The state machine circuitry is shown in Figure III - 7A and 7B. The control PROM starts each state by outputing the five bit code which identifies the current state. IC-5A, one of the hex latches, strobes the value through to the inputs of the two decode PROMs, IC-7A and IC-8A, as well as to the input of the second hex latch IC-6A.

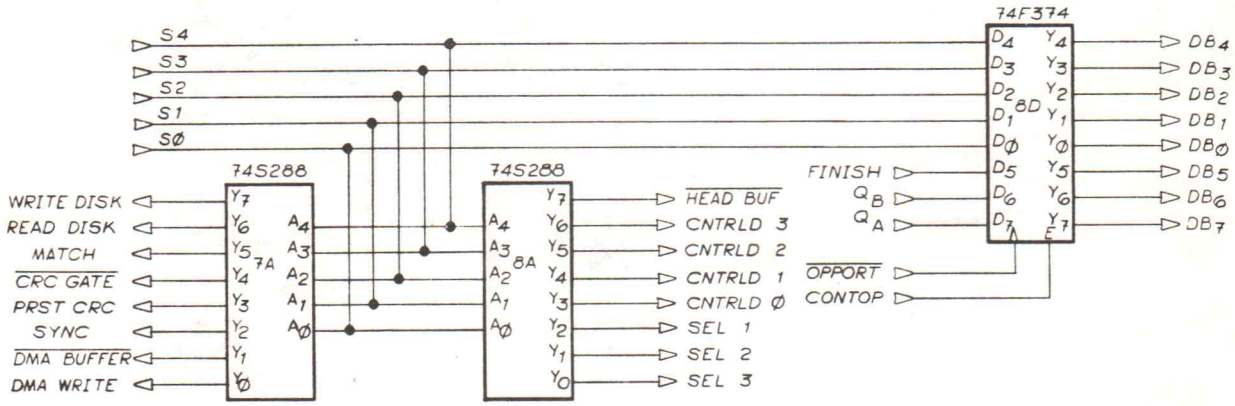


FIGURE III - 7A

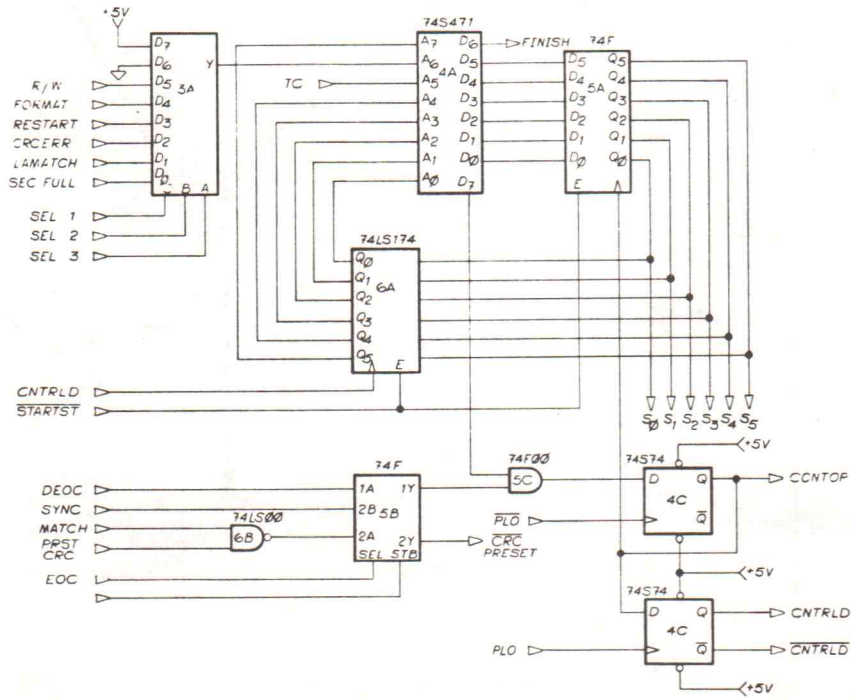


FIGURE III - 7B

STATE MACHINE CIRCUITRY

The outputs of the two decode PROMs provide the control signals necessary for the supervision of the disk transfer. The level of each of the control signals is determined by the five bit state code which is present on the inputs to the PROMs. The control outputs, and their functions are discussed fully in heading 3-3 below.

The hex latch IC-6A is used to gate the five bit identification code of the current state back to the input of the control PROM. The control PROM uses the state code of the current state, the control variable currently selected by IC-3A, and TC, the output of the presetable byte counter IC-8B, to determine what the next state should be.

The lower three output bits of decode PROM IC-8A (SEL 1 - SEL 3) select the output of the control variable multiplexer, IC-3A. These lines select one of the six control variables. The state diagram in Figure III - 6 lists the control variable used to select between two possible subsequent states at each decision point. The control variables are listed below, with their definitions.

TC: TC is the output of the timeout counter. It is used to count the number of bytes in the current state. The value loaded into the counter is given in the state diagram, and is preceded by "C=" for each state.

R/W: R/W is bit DØ of CODEPORT and selects either a read or write operation. This input is ignored if the FORMAT input (below) is true.

FORMAT: FORMAT is bit Dl of CODEPORT and is used by the operating system to select a Format operation.

RESTART: RESTART is used to start the state machine.

CRCERR: CRCERR is the output of the CRC (Cyclical Redundancy Check) chip IC-16D. When this input is high, it indicates to the state machine that the CRC chip has detected a CRC error in the current ID or DATA field.

LAMATCH: LAMATCH is the output of the disk data matching circuit IC-12B and IC-12C. It is used to find the sync bytes and is used to verify that the correct sector has been found.

SECTOR FULL: SECTOR FULL indicates that the sector transfer is complete. The signal is generated by the carry output of the DMA address counter formed by IC-7B and IC-9B.

3-3 State Machine Control Signal Outputs

The outputs of the two 8 bit decode PROMs (ICs 7A and 8A, see Figure 7A) provide the control signals necessary to supervise the data transfer between the disk and buffer RAM. These signals, and their definitions are listed below.

WRITE DISK: WRITE DISK indicates that the disk is being written to, either during a WRITE or FORMAT Operation. This signal is inverted by IC-14A to provide the /WRITE GATE signal to the drive. In addition, it configures the parallel-to-serial converter, IC-15D, to take bytes off of the controller's local data bus and convert them into a serial bit stream.

READ DISK: READ DISK indicates that the disk is being read from, either during an ID field read during a READ or WRITE operation, or a read from the DATA field during a READ operation. This signal controls the /READ GATE signal from IC-14A. In addition, it configures the parallel-to-serial converter, IC-15D, to take the serial bit stream and convert it into bytes which are placed on the controller's data bus.

/DISKOP: /DISKOP is generated by IC-15C and indicates that a disk transfer operation is in progress. This signal controls the multiplexers on the address and control lines of the buffer RAM.

MATCH: MATCH is used to divide the local data bus into two sections by disabling bus transceiver IC-13D (via IC-14C which generates TO RAM and /BUFSEL). Other signals involved in this process are /HEAD BUF, READ DISK, DISKOP. This enables the general purpose matcher IC-12B and IC-12C used to detect Sync bytes in the ID and DATA fields as well as to verify the ID field contents. Figure III - 8 below illustrates the bus divider and byte matcher.

CRC GATE: CRC GATE is used to gate the CRC bits generated by IC-16D into the serial data stream at the end of each ID and DATA field when they are written (see heading 6 below).

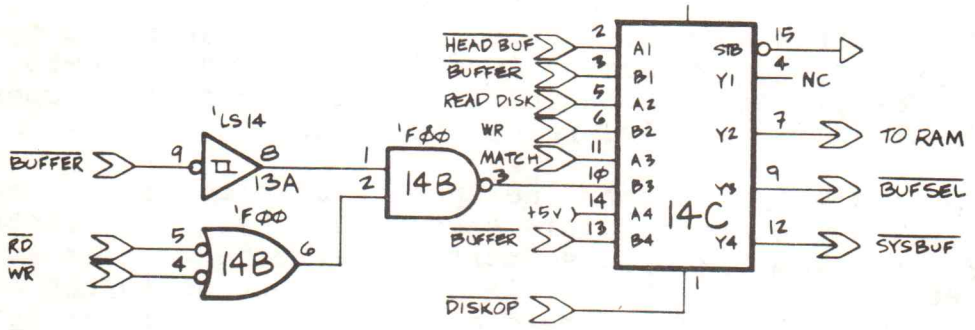
/PRST CRC: /PRST CRC clears the CRC generater/checker, IC-16D.

SYNC: SYNC is generated by the state machine as a synchronizing signal used to set up the byte sync counter, IC-1A, shown in Figure III - 8 below.

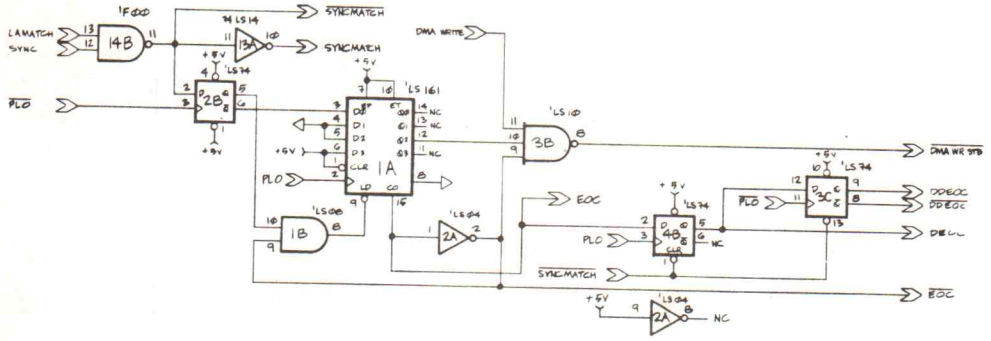
DMA WRITE: DMA WRITE gates the /DMA WR STB generated by the byte sync counter. The /DMA WR STB provides the write signal required to write the bytes from the local data bus to the RAM buffer during Read operations.

/HEAD BUF: /HEAD BUF and its complement controls the buffer RAM address multiplexer. This signal is used to set the RAM address lines A6 - A9 to Ø, so that the state machine can compare the ID field from the disk with the ID field stored in the buffer by the operating system.

CNTRLDØ - CNTRLD3: These four signals are used to preset the byte counter, IC-8B (see Figure III - 9) to the proper value so that the terminal count (TC) will occur after the correct number of bytes.



DATA BUS DIVIDER DIRECTION SIGNAL GENERATION



BYTE SYNC COUNTER

FIGURE III - 8

SUPPORTING STATE MACHINE LOGIC

4 DMA ADDRESS GENERATION

During the disk transfer, the buffer RAM performs two functions. During the ID read or write process, the ID field is read from the lower 64 bytes of the buffer. If a FORMAT operation is selected, the bytes are written to the disk, otherwise the bytes are compared with the bytes being read from the disk in order to verify that the proper sector is being accessed. During a DATA read or write, the upper 512 bytes of the buffer RAM are accessed in sequence.

Both of these functions require the rapid generation of sequential address values. This function is performed by a 10 bit binary counter comprised of IC-8B, IC-7B, and IC-9B. The counter may be preset by both the state machine and the operating system. Figure III - 9 illustrates the logic.

The operating system sets the upper four bits of the address counter to accommodate multiple sector lengths. The controller currently supports 512 byte sectors, therefore counter is currently preset to 200H. This selects the upper 512 bytes as the buffer. During the ID field read and write the lower 32 bytes of the RAM must be read. The HEAD BUF signal allows the state machine to clear the upper 4 bits by deselecting the upper nibble multiplexer, IC-9C. In addition, IC-8C and IC-8B allow the lower 6 bits to be preset to properly read the ID field.

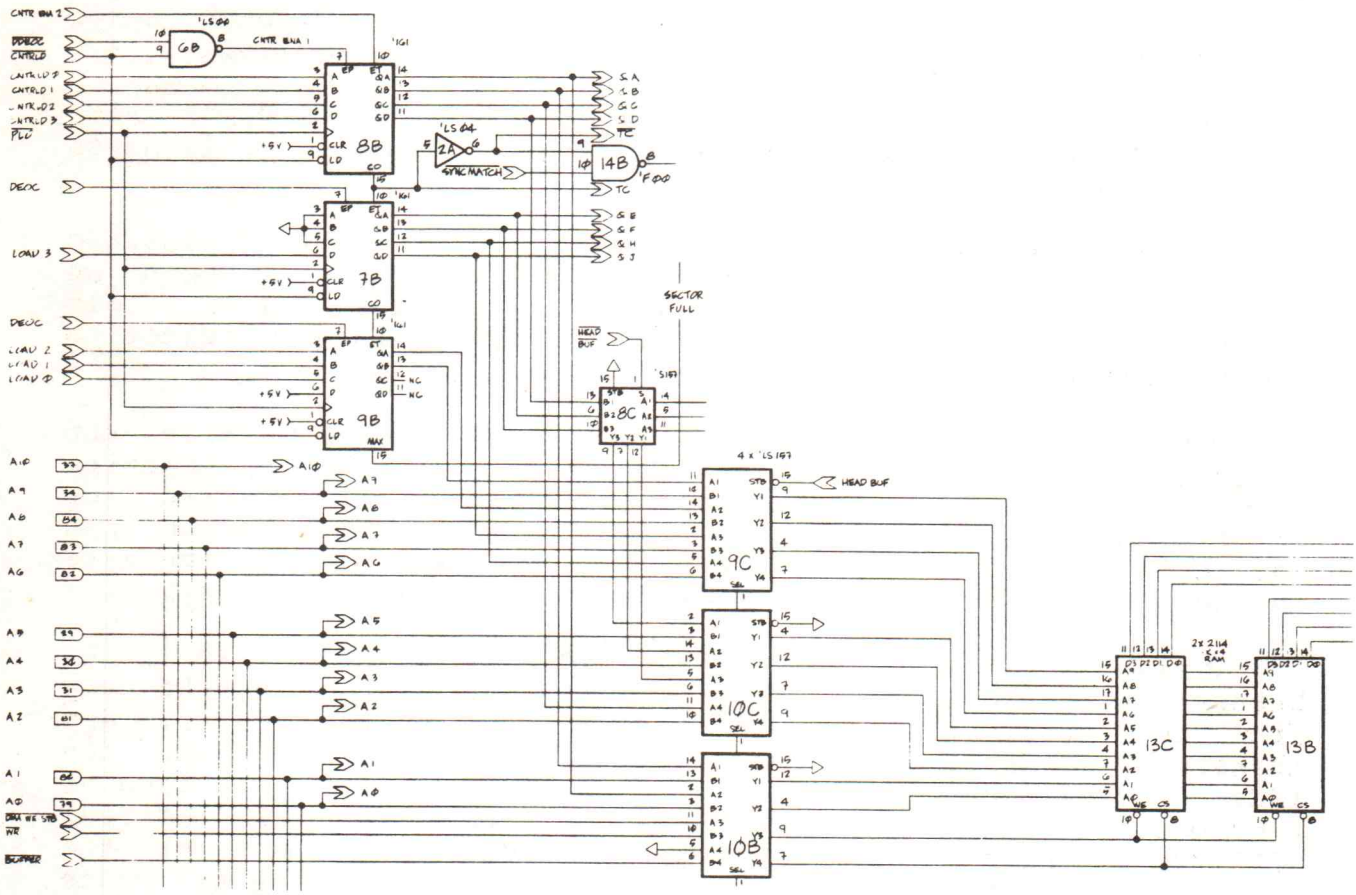


FIGURE III - 9

DMA ADDRESS GENERATION

5 ID MATCH COMPARITOR

Each sector has an ID field which contains the track, head, and sector numbers pertaining to that sector. The purpose of the ID field is to allow the controller to verify that a seek error has not occurred in the mechanical positioning mechanism.

The Micromation controller verifies the ID field of each sector when it performs a read or write operation. The ID match circuitry is detailed in Figure III - 10.

The host processor must place a copy of the expected ID field into the buffer prior to instructing the controller to begin an operation. This copy is then compared with the actual ID field as it is being read to determine if a match exists, indicating the sector has been successfully found.

The ID field match comparitor consists of IC-13D, IC-12B, and IC-12C. At the beginning of the ID field read, the state machine sets the address counter to the buffer RAM to the starting address, as described in section 3.4, DMA Address Generation. As each byte is read from the disk by IC-15D, the corresponding byte in the buffer RAM is addressed by the DMA address circuitry.

IC-13D is disabled by the state machine, creating two local busses. The byte which is read from the buffer RAM, and the byte from the disk, placed on the second local bus by IC-15D, are therefore separated. The exclusive OR gates of IC-12B and IC-12C, compare the two bytes on the two local busses. As long as they match, the output of the open collector XOR gates (LAMATCH) will remain high. If a discrepency is detected in any of the bytes, the LAMATCH line will be pulled low, informing the state machine that the ID field read in from the disk does not match the ID field read in from the disk.

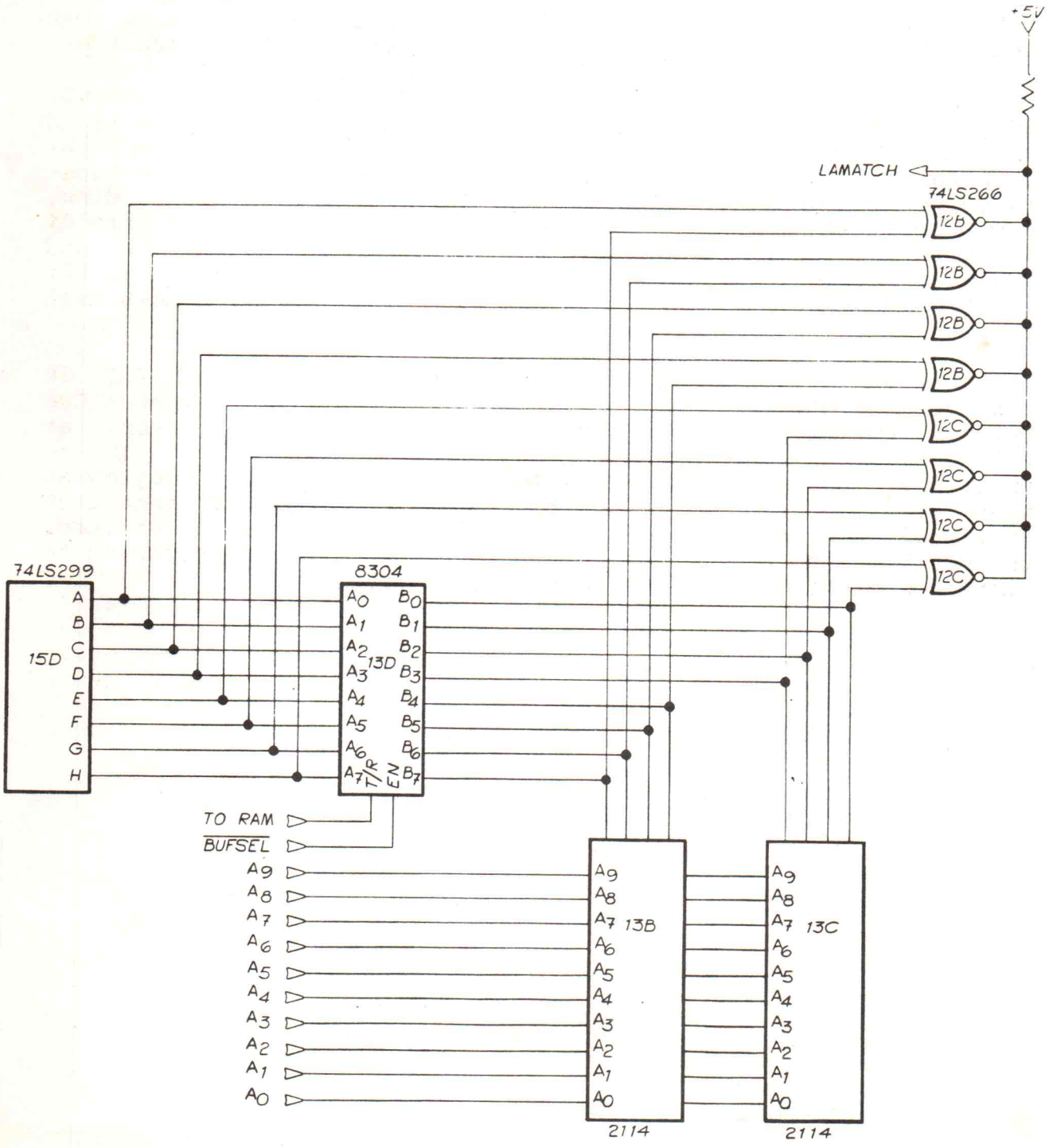


FIGURE III - 10

ID MATCH CIRCUITRY

6 CRC GENERATION AND VERIFICATION

Both the Data and ID fields contain 2 CRC bytes (16 bits) which allow the controller to verify that the data has been read correctly from the disk. The CRC bytes are appended to the ID field during FORMAT operations and to the data field during both FORMAT and WRITE operations. The bytes are checked during READ and WRITE operations. Figure III - 11 illustrates the circuitry.

The actual CRC bytes are generated and checked by IC-16D. When the controller is writing to the disk, both during ID field and Data field writes, IC-16D monitors the output of the parallel-to-serial converter, IC-15D. The CRC bytes are generated by IC-16D based on the data bits being written to the disk. When the state machine is finished writing the ID or Data field, it brings the /CRCGATE line low. This signal causes IC-6C and IC-16C to write the output of the CRC generator (IC-16D, pin 12) to the disk, instead of the output of the parallel-to-serial converter, IC-15D.

During the reading of the ID and Data fields, the CRC IC monitors the data coming from the disk. The CRC IC computes CRC bytes, as it would during a disk write operation. However, at the end of the data, the state machine signals the CRC IC to enter the check mode. The CRC IC then compares the CRC bytes as they are read in from the disk, with the CRC bytes generated internally during the data read. If a discrepency is detected, the CRCERR line is driven high by the CRC checker, indicating to the state machine that a CRC error was detected.

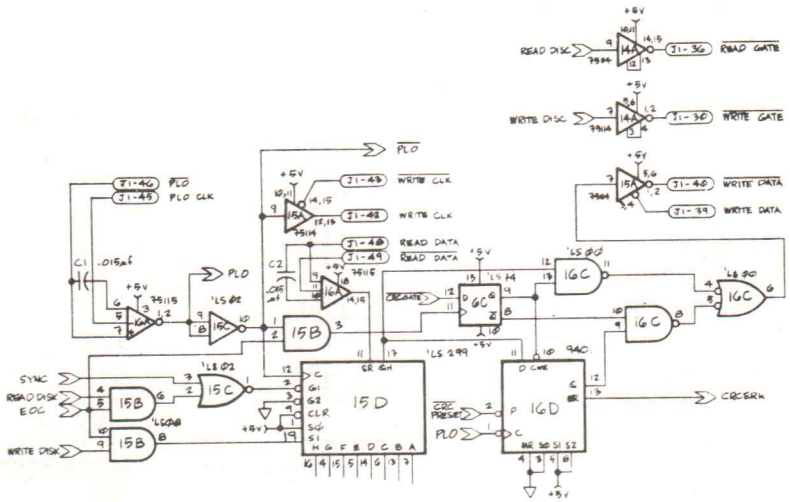


FIGURE III - 11

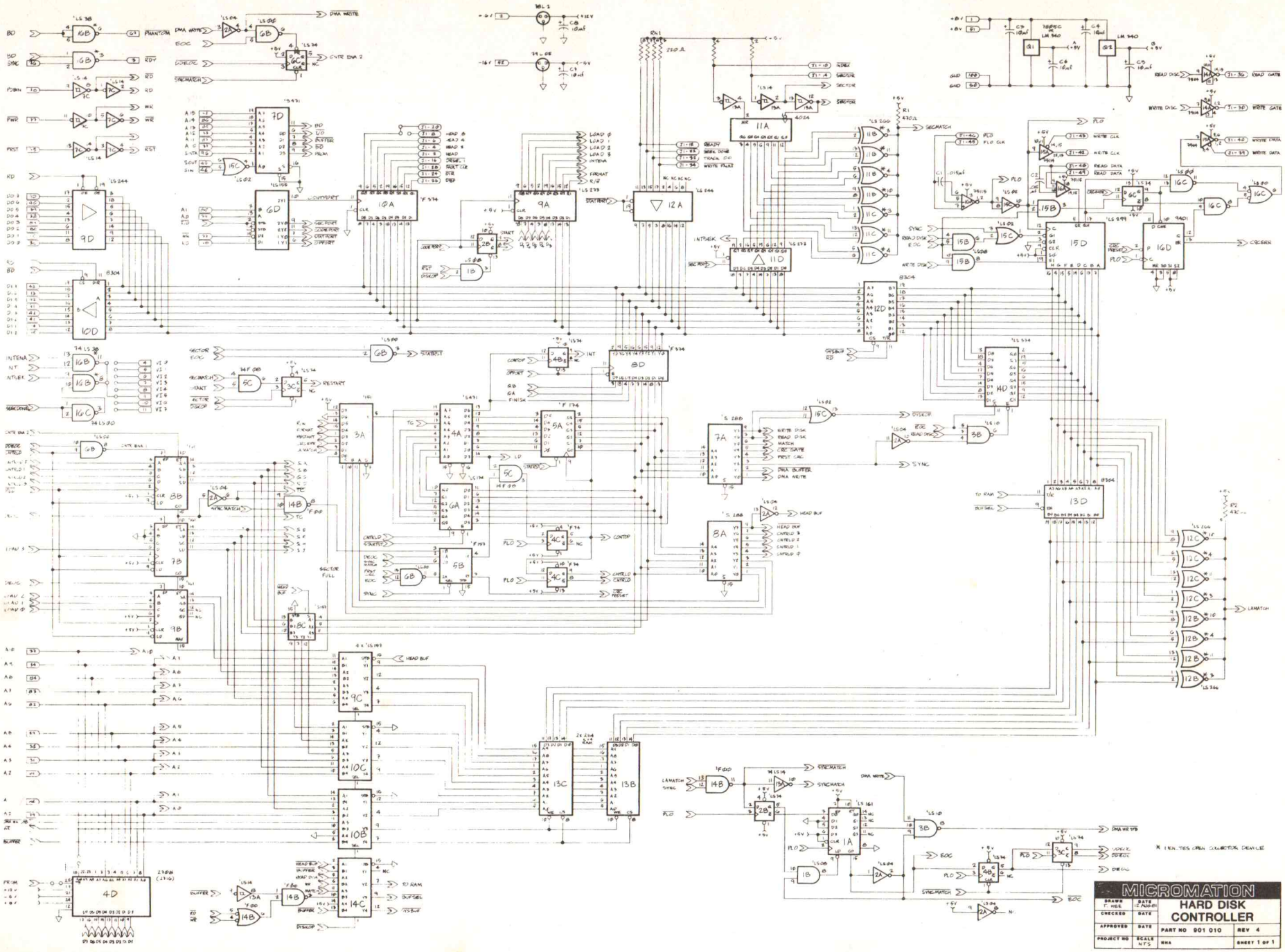
CRC CHECKING CIRCUITRY

APPENDIX A

REVISION LOG

Manual Number	Name
DØ1 Ø4Ø	Hard Disk Controller Theory of Operation

Revision Number	Date	Notes
1	12/79	Preliminary version
2	3/8Ø	Preliminary updated for new software
3	9/8Ø	Preliminary updated for M/NET system
4	11/81	Completed revised with extended descriptions of circuit logic


MICROMATION
HARD DISK CONTROLLER
PART NO 901 010
REV 4
SHEET 1 OF 1
DRAWN T. HEE
DATE 12 NOV 81
CHECKED
APPROVED
PROJECT NO
SCALE NTS
RMA
DMA WRITE
PHANTOM
RDY
RD
WR
RST
SYNCMATCH
SECTOR
INDEX
WRITE GATE
READ GATE
WRITE DATA
READ DATA
WRITE CLK
READ CLK
PLO
SYNC
WRITE DISK
READ DISK
MATCH
DISKOP
SECTOR FULL
LAMATCH
TO RAM
BUFSEL
CRCERR
* TEN-TIES OPEN COLLECTOR DEVICE