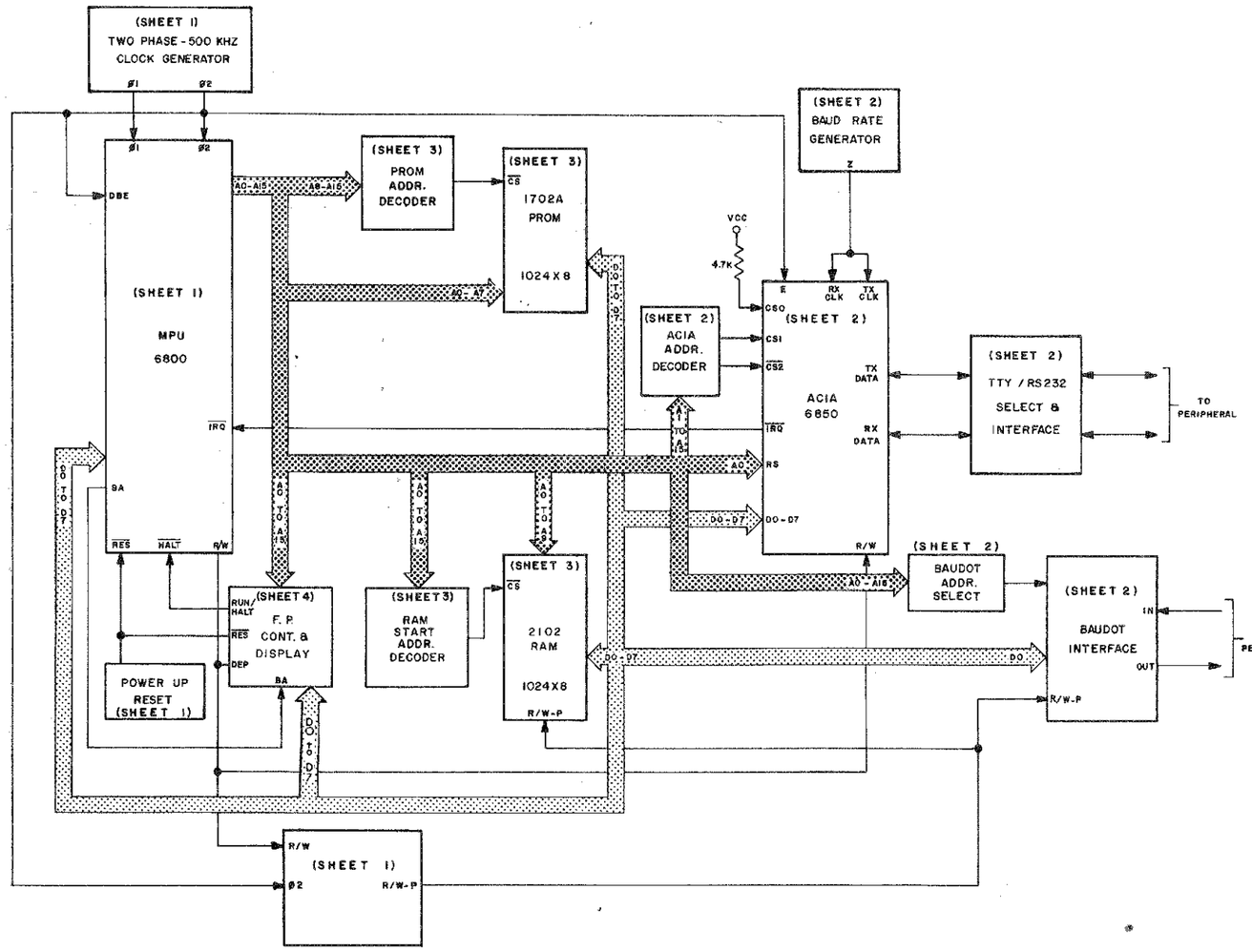
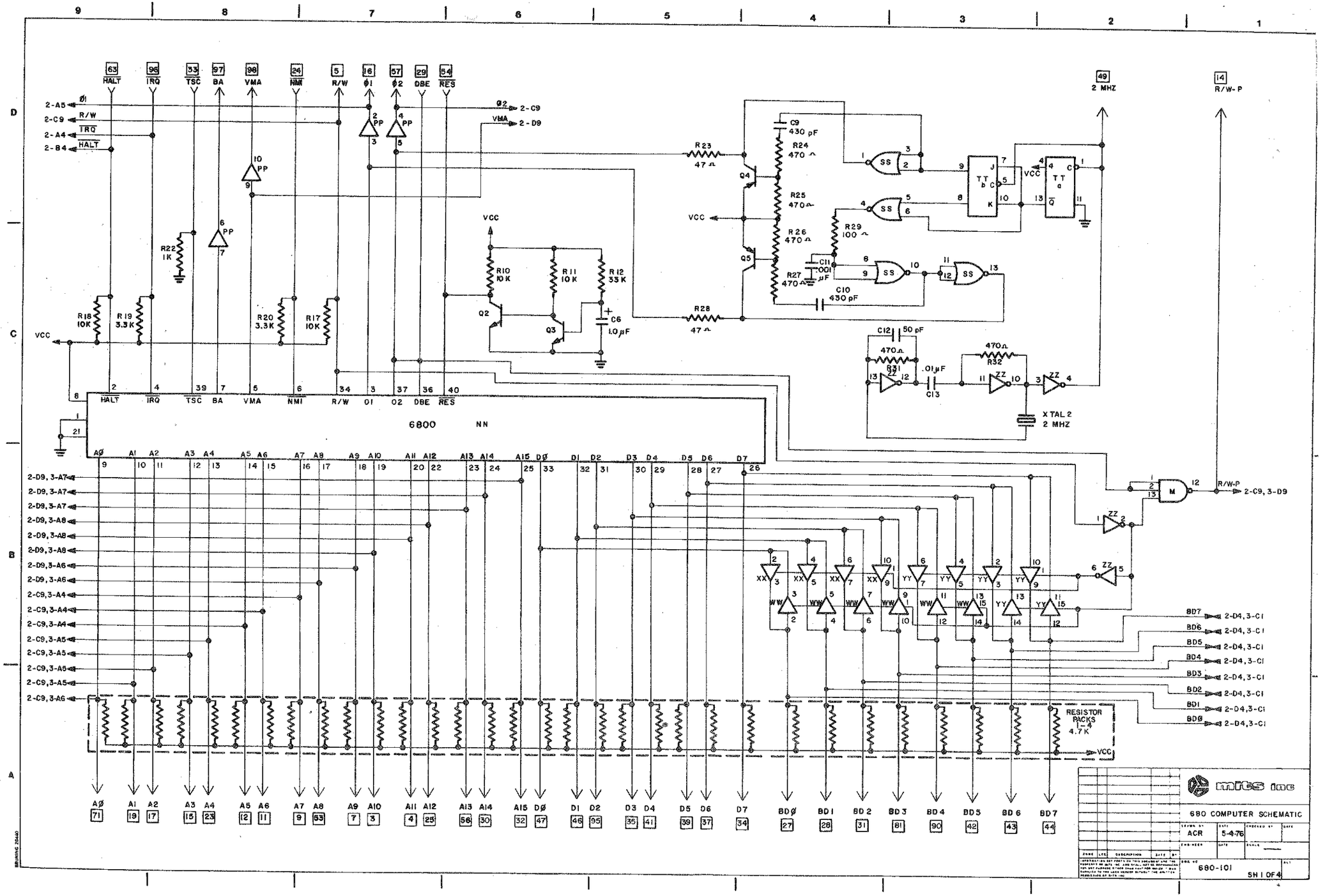
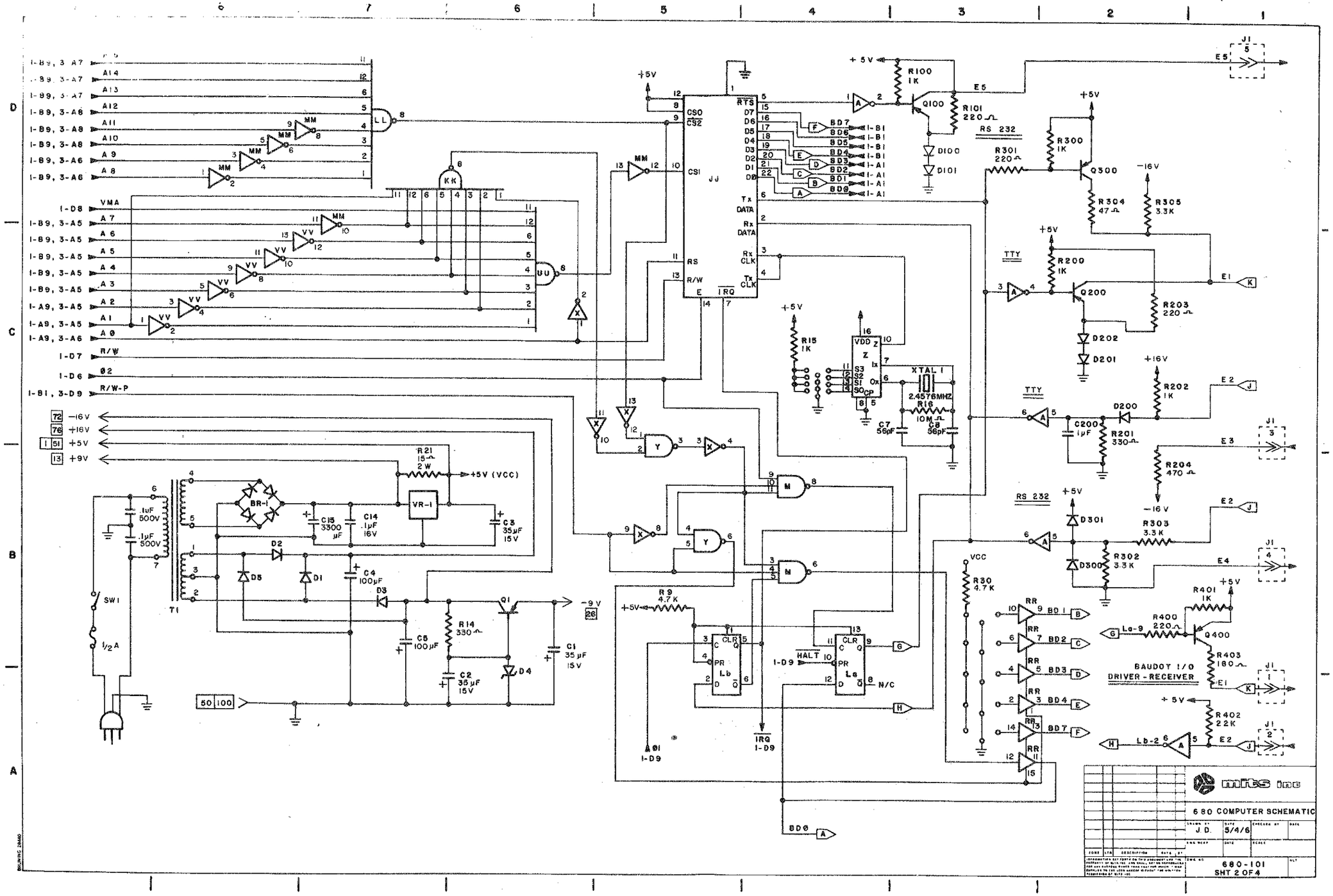


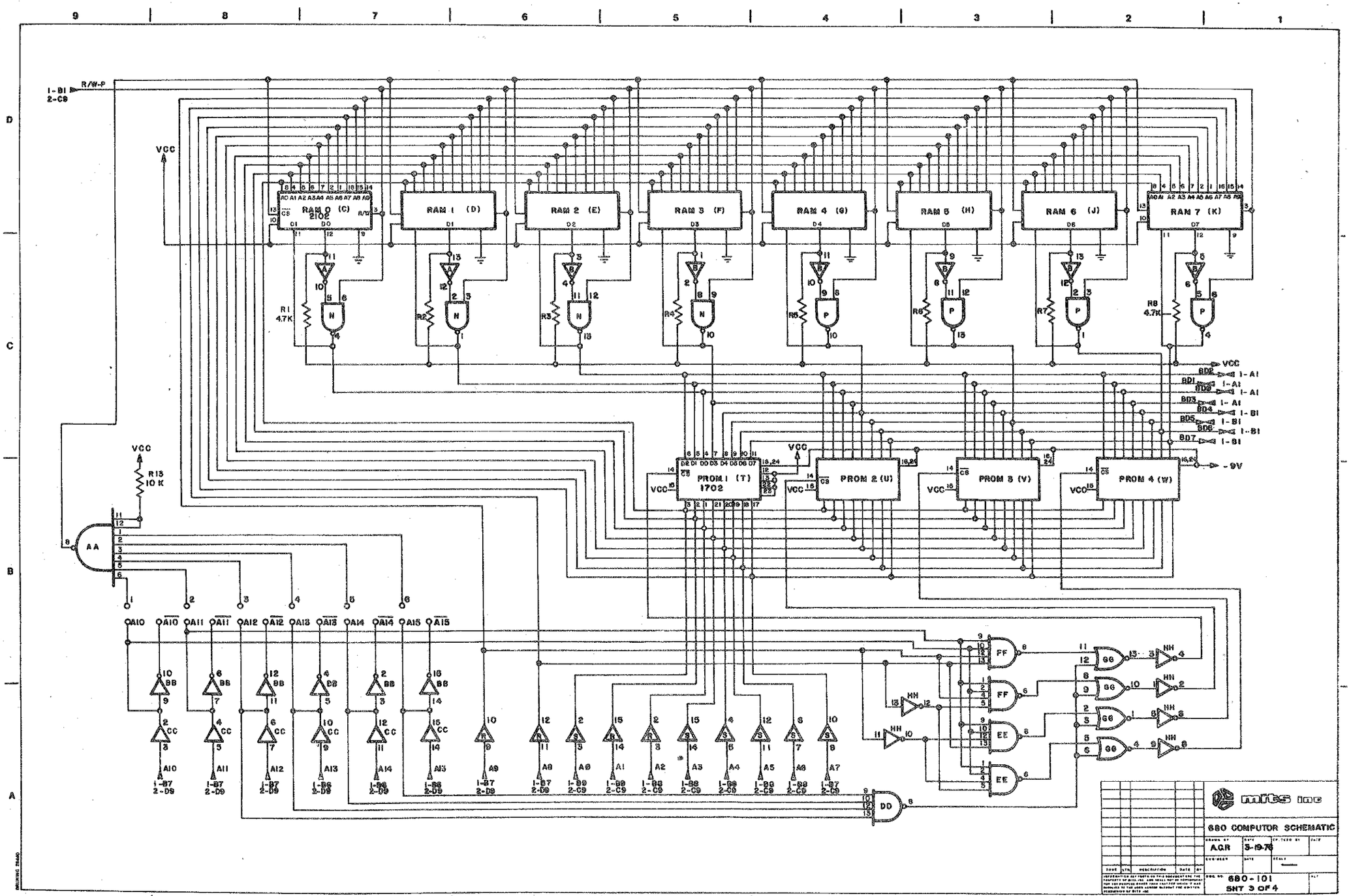
680b SYSTEM DIAGRAM

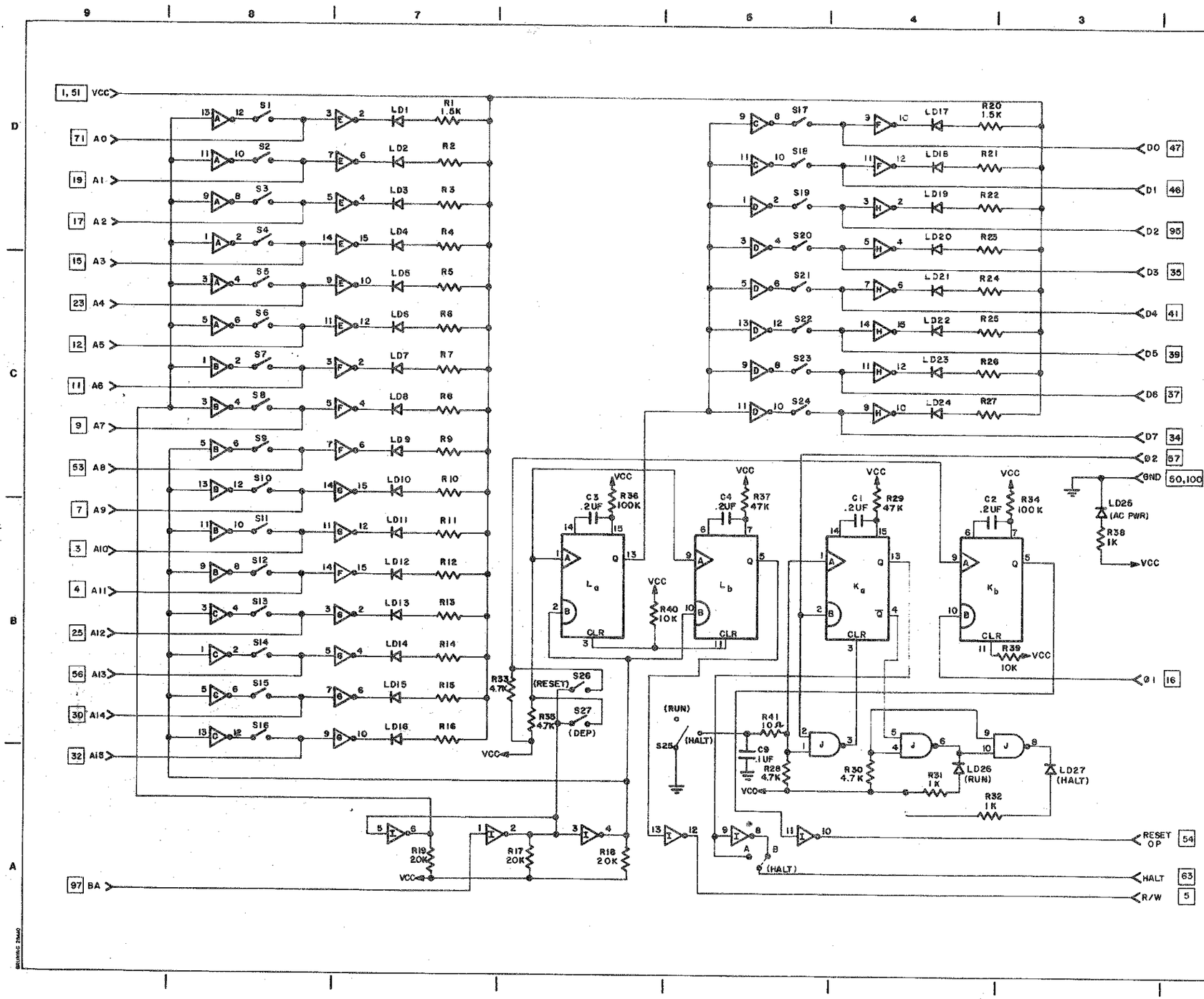
KEY FOR 680b SYSTEM DIAGRAM

MPU	Microprocessing Unit
F.P. CONT. & DISPLAY	Front Panel Control & Display
ACIA	Asynchronous Communication Interface Adapter
DBE	Data Bus Enable
BA	Bus Available
$\overline{RES}$	Reset
$\overline{HALT}$	Halt
R/W	Read - Write
R/W-P	Read - Write Prime
DEP	Deposit
A0 - A15	Address Zero to Address Fifteen
D0 - D7	Data Zero to Data Seven
$\overline{CS}$	Chip Select
$\overline{IRQ}$	Interrupt Request
E	Enable
RS	Register Select
Rx	Receive
Tx	Transmit
CLK	Clock


9 8 7 6 5 4 3 2 1
D C B A
63 HALT
96 IRQ
33 TSC
97 BA
98 VMA
24 NMI
5 R/W
16 Ø1
57 Ø2
29 DBE
54 RES
2-A5 Ø1
2-C9 R/W
2-A4 IRQ
2-B4 HALT
Ø2 2-C9
VMA 2-D9
49 2 MHZ
14 R/W-P
R22 1K
R18 10K
R19 3.3K
R20 3.3K
R17 10K
R10 10K
R11 10K
R12 33K
C6 1.0µF
R23 47Ω
R24 470Ω
R25 470Ω
R26 470Ω
R27 470Ω
R28 47Ω
R29 100Ω
C9 430 pF
C10 430 pF
C11 .001 µF
C12 50 pF
C13 .01µF
470Ω R31
470Ω R32
XTAL 2 2 MHZ
6800 NN
2-D9, 3-A7
2-D9, 3-A8
2-C9, 3-A4
2-C9, 3-A5
2-C9, 3-A6
R/W-P 2-C9, 3-D9
BD7 2-D4, 3-C1
BD6 2-D4, 3-C1
BD5 2-D4, 3-C1
BD4 2-D4, 3-C1
BD3 2-D4, 3-C1
BD2 2-D4, 3-C1
BD1 2-D4, 3-C1
BDØ 2-D4, 3-C1
RESISTOR PACKS 4.7K
VCC
AØ A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 DØ D1 D2 D3 D4 D5 D6 D7
BDØ BD1 BD2 BD3 BD4 BD5 BD6 BD7
mtes inc
6800 COMPUTER SCHEMATIC
DRAWN BY ACR
DATE 5-4-76
CHECKED BY
DATE
ENG. HEAD
DATE
SCALE
SIZE C
680-101
SHEET 1 OF 4


I-B9, 3-A7 A15
I-B9, 3-A7 A14
I-B9, 3-A7 A13
I-B9, 3-A6 A12
I-B9, 3-A6 A11
I-B9, 3-A8 A10
I-B9, 3-A8 A9
I-B9, 3-A6 A8
I-D8 VMA
I-B9, 3-A5 A7
I-B9, 3-A5 A6
I-B9, 3-A5 A5
I-B9, 3-A5 A4
I-B9, 3-A5 A3
I-A9, 3-A5 A2
I-A9, 3-A5 A1
I-A9, 3-A6 A0
I-D7 R/W
I-D6 Ø2
I-B1, 3-D9 R/W-P
72 -16V
76 +16V
1 51 +5V
13 +9V
+5V
+5V (VCC)
-16V
+16V
-9V
R21 15Ω 2W
BR-1
VR-1
C15 3300 µF
C14 .1µF 16V
C3 35µF 15V
C4 100µF
C5 100µF
C2 35µF 15V
C1 35µF 15V
.1uF 500V
.1µF 500V
SW1
1/2A
T1
D1
D2
D3
D4
D5
R14 330Ω
Q1
CSO CS2
CSI
RS
R/W
E
IRQ
RTS
D7
D6
D5
D4
D3
D2
D1
D0
Tx DATA
Rx DATA
Rx CLK
Tx CLK
R100 1K
R101 220Ω
Q100
D100
D101
RS 232
R300 1K
R301 220Ω
Q300
R304 47Ω
R305 3.3K
TTY
R200 1K
Q200
R203 220Ω
D202
D201
R202 1K
D200
C200 1µF
R201 330Ω
R204 470Ω
R303 3.3K
R302 3.3K
D301
D300
R401 1K
R400 220Ω
Q400
R403 180Ω
R402 22K
BAUDOT I/O DRIVER - RECEIVER
R15 1K
R16 10M
C7 56pF
C8 56pF
XTAL I 2.4576MHZ
VDD
S3 S2 S1 SO
CP
Ix Ox
R9 4.7K
R30 4.7K
HALT I-D9
IRQ I-D9
Ø1 I-D9
N/C
BD0 A
BD1 B
BD2 C
BD3 D
BD4 E
BD7 F
E1 E2 E3 E4 E5
J1 3 J1 4 J1 1 J1 2
mits inc
680 COMPUTER SCHEMATIC
J.D. 5/4/6
680-101 SHT 2 OF 4


1-BI
2-CS
R/W-P
VCC
RAM 0 (C) 2102
RAM 1 (D)
RAM 2 (E)
RAM 3 (F)
RAM 4 (G)
RAM 5 (H)
RAM 6 (J)
RAM 7 (K)
R1 4.7K
R8 4.7K
R13 10 K
PROM 1 (T) 1702
PROM 2 (U)
PROM 3 (V)
PROM 4 (W)
- 9V
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
AA
DD
FF
GG
HH
EE
mits inc
680 COMPUTOR SCHEMATIC
DRWN BY A.G.R
DATE 3-19-76
DWG NO. 680-101
SHT 3 OF 4



REF	TYPE	VCC	GND
A,B,C,D,I	74LS05	14	7
H/13, E/13 F/13, G/13	4009 OR 4049	16	8
J/11, 12, 13	74L00	14	7
K/11, 12 L/3,4,11,12	74L123	16	8

mits inc

680 DISPLAY SCHEMATIC

DRAWN BY	DATE	CHECKED BY	DATE
A.C.R.	3-22-76		
ENGINEER	DATE	SCALE	—

680-100 SHT 4 OF 4

(SHEET 4 OF 4)