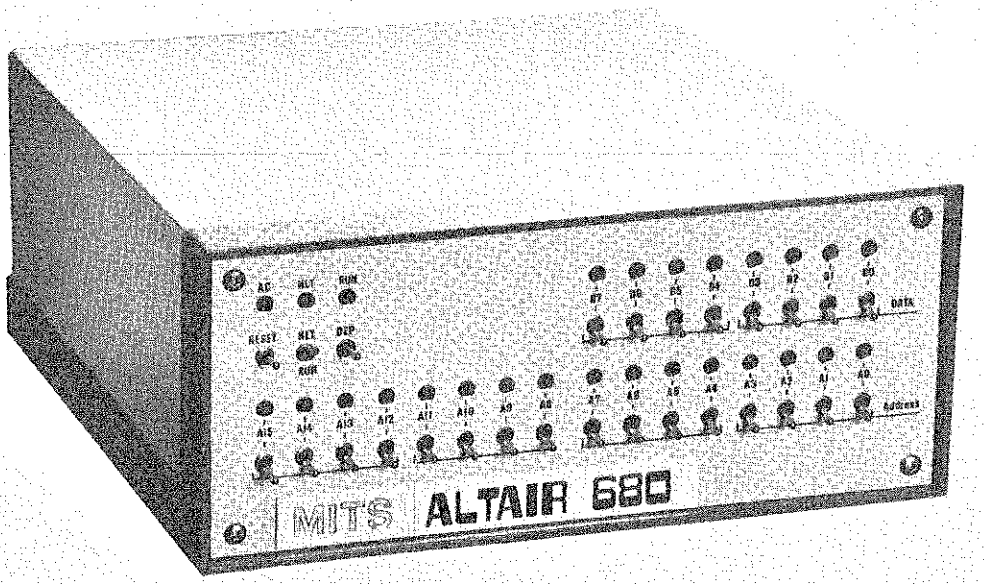
operator's manual



ALTAIR 680

Operator's Manual

altair™ 680b

Table of Contents

MITS, Inc. ©1976
2450 Alamo S.E.
Albuquerque, N.M. 87106

I. USER DEFINED FUNCTIONS

There are three areas on the Altair 680b main printed circuit board that must be wired according to user-defined specifications. These three areas are:

A. Baud Rate Generator

B. RAM Starting Address Selection

C. Hardware Programmable Bits

If you have not yet wired the board for these user-defined functions, or if you wish to change any of the functions, read the instructions given in this section. All jumper wiring must be complete before you begin operating the 680b.

A. Baud Rate Generator

If a terminal is to be used with the 680b, the baud rate must be set on the main PC board to coincide with the baud rate of the terminal.

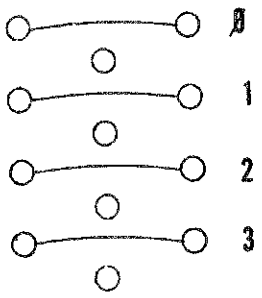
Refer to the main PC board. Moving to the left from IC Z, you will find: 1) a column of four holes labeled 0 through 3; 2) a column of four holes (not labeled) representing the ground (LOW) plane; 3) a column of four holes (not labeled) representing the +5 volt (HIGH) plane.

The baud rate for the 680b computer is user selectable according to the jumper connections placed across these holes. The configurations of the jumper wires for the various baud rates are listed in the chart on the next page.

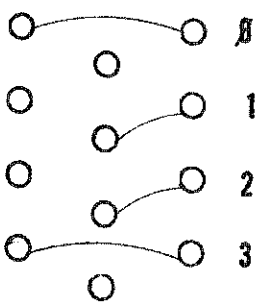
0	1	2	3	OUTPUT RATE Z(pin 10)
L	H	L	L	50 Baud
H	H	L	L	75 Baud
L	L	H	L	134.5 Baud
H	L	H	L	200 Baud
L	H	H	L	600 Baud
H	H	H	L	2400 Baud
L	L	L	H	9600 Baud
H	L	L	H	4800 Baud
L	H	L	H	1800 Baud
H	H	L	H	1200 Baud
L	L	H	H	2400 Baud
H	L	H	H	300 Baud
L	H	H	H	150 Baud
H	H	H	H	110 Baud

TRUTH TABLE FOR
RATE SELECT INPUTS

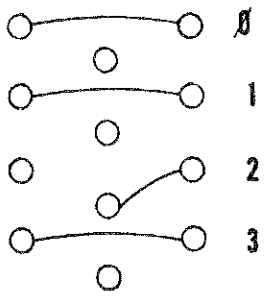
Examples are shown below of the jumper wire configurations for 110 baud and 1200 baud.



110 Baud



4800 Baud



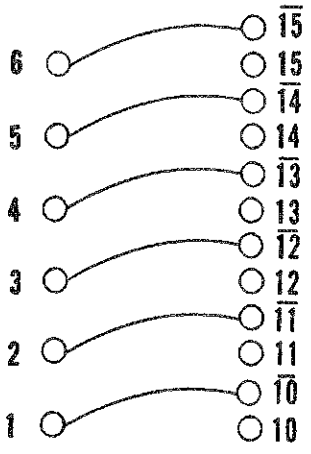
1200 Baud

B. RAM Starting Address Selection

The Altair 680b comes equipped with 1K of Random Access Memory (RAM). The starting address for this block of memory is determined by the configuration of the jumper wires across pads 1 through 6 and 10 through $\overline{15}$ (between ICs AA and BB on the main PC board).

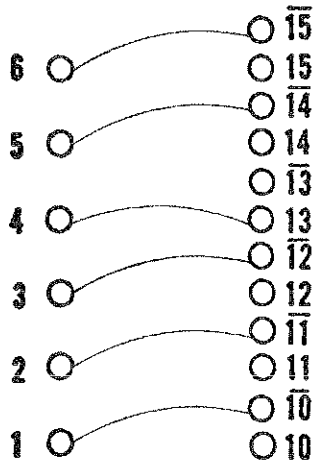
Address locations A_0 through A_9 are needed to properly address every location in 1K of RAM. 1K of memory is equal to 1024_{10} bits (or 400_{16} bits). In order to place the 1K block of RAM at a particular starting address, it is necessary to NAND either address lines A_{10} to A_{15} or their complement. This causes the CHIP SELECT ($\overline{CS}$) inputs to the RAMs to be pulled to their proper logic level (i.e. zero) when they are addressed. For example, if starting address 0000 is desired for the RAM, then it would be highly undesirable for the RAM to be selected at address 2000_{16} also. If this were done, each location in the RAM would have two addresses. To prevent this from occurring, when the RAM is to be located at 0000, A_{10} to A_{15} are inverted before being NANDed to derive the $\overline{CS}$ signal. Thus, if any location is addressed higher than the addresses included in the 1K block, there will be no $\overline{CS}$ and, therefore, no false addressing.

To see this in terms of "ones and zeros," refer to schematic 3-B7,8 of the Theory of Operation manual. It can be seen that integrated circuit C is for standard memory address line buffering, and integrated circuit BB is a hex inverter. If starting address zero is chosen, then A_0 through A_9 will be used for addressing all of the locations within this 1K block. Whenever these locations are addressed, A_{10} through A_{15} will be zeros; therefore it is necessary to invert them before they are ANDed and INVERTED by integrated circuit AA. It is absolutely necessary to have all "ones" on the inputs of IC AA in order to have the "zero" output necessary to affect RAM chip selection ($\overline{CS}$). To accomplish this inversion of A_{10} to A_{15}, jumpers 1 through 6 on the main PC board are tied to their corresponding inverted outputs, i.e. $\overline{10}$, $\overline{11}$, $\overline{12}$, $\overline{13}$, $\overline{14}$, $\overline{15}$.



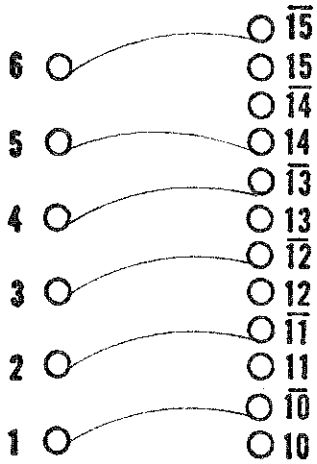
Jumper Wire Configuration for RAM Starting Address 0000

If an 8K RAM board is used with the system and it is desirable to have the original 1K RAM block begin at 8K (hexadecimal address 2000), then it is necessary to configure the jumpers such that the inputs to AA are at a logic level one whenever the 1K RAM block is addressed at 2000 . This means that A_{13} is high and A_{10} through A_{15} (except A_{13}) are low. Since A_{13} is already high, it does not need to be inverted before being fed to integrated circuit AA. Therefore, jumpers 1, 2, 3, 5, and 6 are connected to pads $\overline{10}$, $\overline{11}$, $\overline{12}$, $\overline{14}$, and $\overline{15}$, respectively; and jumper 4 is connected to pad 13. Since A_{13} is not inverted, the 1K RAM block will begin to be selected when address location 2000_{16} is addressed.

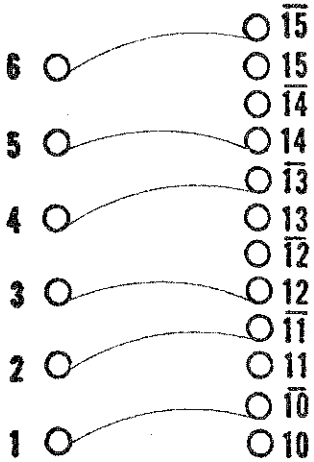


Jumper Wire Configuration for
RAM Starting Address 2000

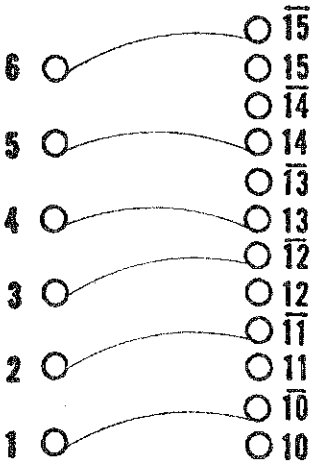
The following diagrams will illustrate the correct jumper wire configurations for RAM starting addresses 4000 (16K), 5000 (20K), 6000 (24K) and 8000 (32K).



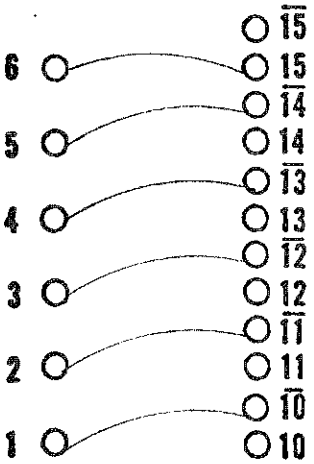
Location 4000 (16K)



Location 5000 (20K)



Location 6000 (24K)



Location 8000 (32K)

C. Hardware Programmable Bits

Refer to the main PC board. Moving to the left from IC WW, you will find: 1) a column of five holes labeled 1 through 5; 2) a column of five holes (not labeled) representing the ground (LOW) plane; 3) a column of five holes (not labeled) representing the +5 volt (HIGH) plane.

The following three conditions are to be hardware programmed by placing jumper connections across these holes:

1. Baudot Interface Bit

   Jumper hole #1 HIGH if a Baudot interface is to be used.
   Jumper hole #1 LOW if no Baudot interface is to be used.

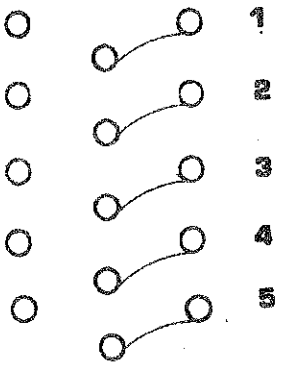
2. Number of Stop Bits Bit

   Jumper hole #2 HIGH for 1 stop bit.
   Jumper hole #2 LOW for 2 stop bits.

3. Terminal/No Terminal Bit

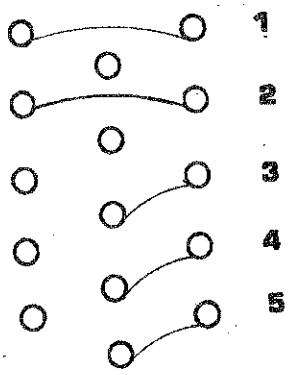
   Jumper hole #5 HIGH if no terminal is to be interfaced (i.e. programming to be done via the front panel).
   Jumper hole #5 LOW if a terminal is to be interfaced (i.e. programming to be done via Teletype, CRT terminal, etc.).

The remaining two holes (#3 and #4) are reserved for future system expansion and are not used at this time. They should be jumpered to the LOW plane to insure proper noise immunity on the bus. Two examples of wiring the hardware programmable bits are shown below.



Programmed for:

1. no Baudot
2. 2 stop bits
3. terminal



Programmed for:

1. Baudot
2. 1 stop bit
3. terminal

II. INPUT/OUTPUT CONFIGURATIONS

In the upper left-hand corner of the Main PC Board, a portion of the foil pattern has been boxed off and labeled "I/O."

The components in this box may be configured in one of three different ways, depending on the interface level desired.

A. ASR33/KSR33 Teletype Interface (20 ma current loop)

B. Standard RS-232 Interface

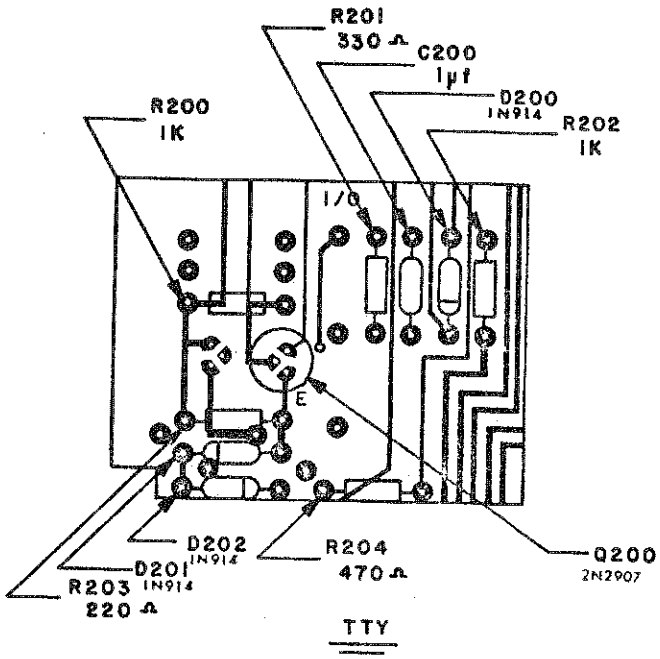
C. Baudot Interface Driver

The component configuration for each of the three interface levels is diagrammed below. The correct part numbers and values appear on the diagrams.

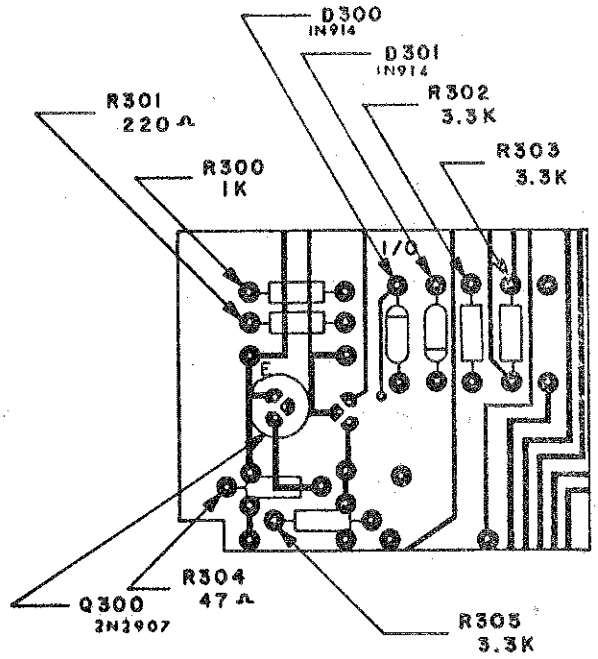
Install these components onto the "I/O" section of the Main PC Board according to the interface level you are planning to use.

A. ASR33/KSR33 Teletype Interface

(20 ma current loop)

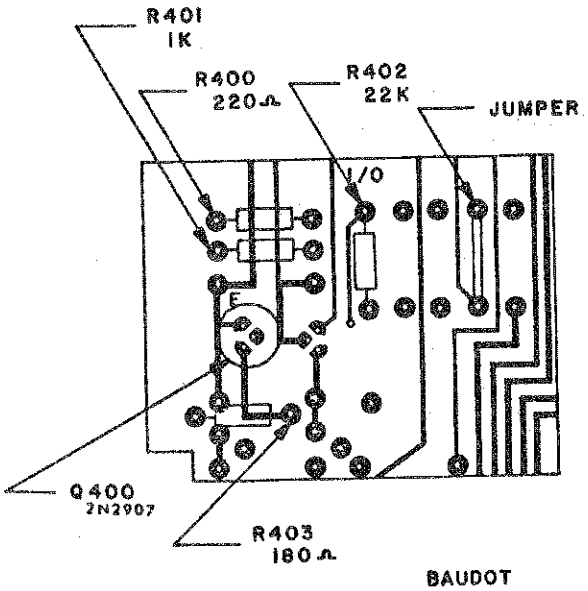


B. Standard RS-232 Interface



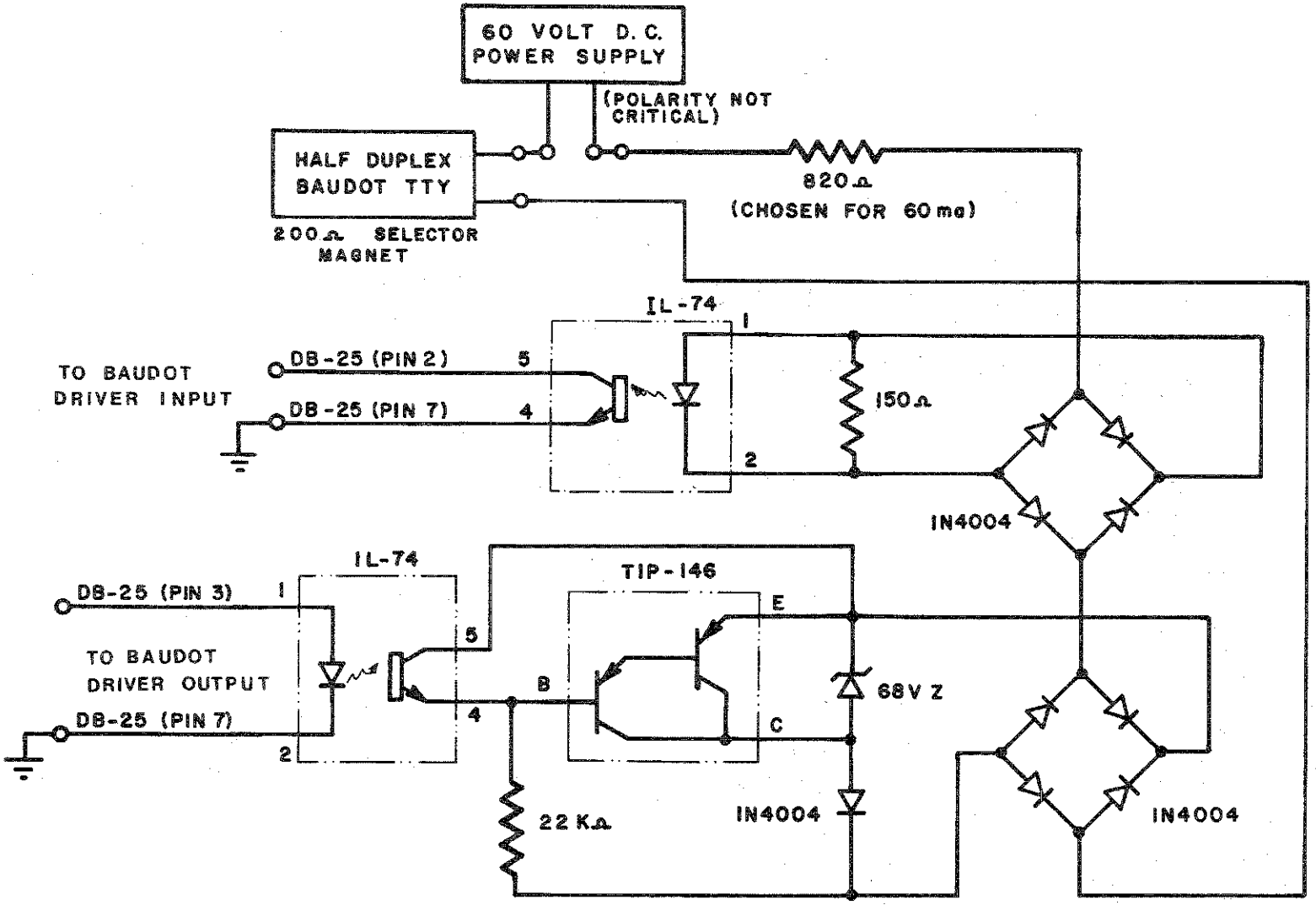
RS 232

C. Baudot Interface Driver*



BAUDOT

*This component configuration alone does not provide a Baudot level interface for the 680b. It is also necessary to include a level converting and isolation circuit (either a read relay or an optical isolation circuit will suffice). A suggested isolation circuit is shown on the following page.



SUGGESTED BAUDOT INTERFACE CIRCUITRY

The 80-volt Darlington transistor (TIP-146) may be obtained from a Texas Instruments, Inc. distributor. The IL-74 Opto-Isolator is available from a Litronix, Inc. distributor. If a substitution is made for the IL-74, it must have a minimum current transfer ratio of 12.5%.

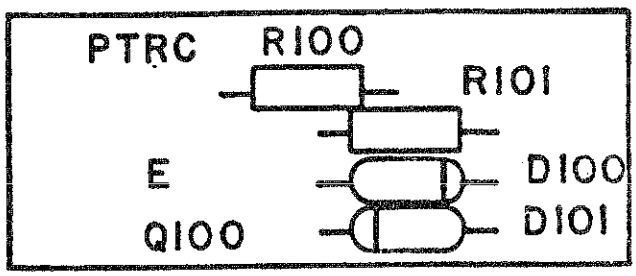
III. PAPER TAPE READER CONTROL

In the upper left-hand corner of the Main PC Board there is a block of components labeled "PTRC" (Paper Tape Reader Control).

These components are to be installed only if the Altair 680b is interfaced to a Teletype that is equipped with a Call/ Control Unit (controllable reader).

The part numbers for the components are listed in the chart below.

Silk Screen Designation	Part Number
R100	1K ohm brown-black-red
R101	220 ohm red-red-brown
D100 & D101	IN914
Q100	2N2907



If you are not using a controllable reader, it is not necessary to mount these components onto the board.

IV. OPERATION OF FRONT PANEL DISPLAY SWITCHES

"Power On" is indicated by the LED labelled "AC" at the top left corner of the front panel. When the machine is in the HALT mode, it is possible to address and deposit within specific memory locations. Both the ADDRESS and DATA lights are configured in a hexadecimal format so that it takes four hexadecimal figures to address any location and two hexadecimal figures to deposit one byte of data within a particular location.

Address locations are indicated by LEDs A_0 through A_{15}, while data within specific locations is indicated by LEDs D_0 through D_7. When either a DATA or ADDRESS switch is in the down position, a zero will be displayed by the respective LED (i.e. the LED will be off); when in the up position, a one will be displayed (i.e. the LED will be on).

When in the HALT mode, the unit is continuously addressing whatever location is defined by the ADDRESS switches. To address a different location, merely change the ADDRESS switches to indicate that location. The chosen address will be displayed on the ADDRESS LEDs. The contents of that address will be displayed on the DATA LEDs.

To change the contents of the displayed location, position the DATA switches to reflect the new data, and acutate the DEPOSIT switch (upper left corner of front panel). The newly deposited data will appear on the DATA LEDs.

Before attempting to run a program, the RESET switch must be actuated to insure proper initialization of the MPU and peripheral interfaces.

V. POWER-UP, ADDRESS and DATA DEPOSIT SEQUENCE*

1. Be sure the RUN-HALT switch is in HALT mode.

2. Turn on rear panel POWER switch.

3. Actuate the RESET switch.

4. Display the desired address location by setting the ADDRESS switches.

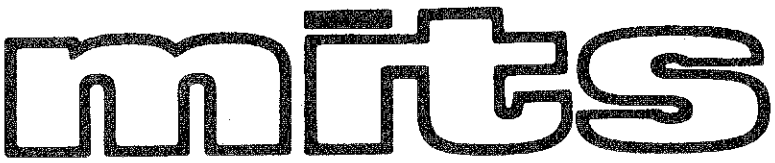
5. Position the DATA switches to reflect the desired entry data.

6. Actuate the DEPOSIT switch.

7. Repeat steps 4 through 6 until all data is completely entered.

8. When the front panel is being used as the system I/O device, the NO TERMINAL BIT should have been set. This assures that the MPU Program Counter will begin at location zero when the 680b is switched into the RUN mode.

*NOTE: If a terminal is being used with the 680b, please refer to the System Monitor manual for power-up sequence.



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