altair 680b

PROCESS CONTROL INTERFACE DOCUMENTATION

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SECTION I
INTRODUCTION

1-1. SCOPE AND ARRANGEMENT

The 680b-Process Control Interface Board documentation is divided into five major sections:

I. Introduction
II. Theory of Operation
III. User Information
IV. Troubleshooting
V. Assembly

Section I contains the scope and arrangement of the manual and a brief description of the board and its capabilities.

Section II contains the information needed to understand the operation of the board at a technical level. It covers the logic circuits, the input and output devices (optical isolators and relays, respectively) and the input and output functions of the board.

Section III contains the general information necessary to set up and initialize the board from both hardware and software standpoints. Two detailed applications and several software programs are included along with a list of various uses.

Section IV contains general troubleshooting information and various tables to aid in locating and correcting most malfunctions that may be encountered.

Section V contains the step-by-step instructions needed to assemble the 680b-PCI board, including detailed diagrams and silkscreens.

1-2. DESCRIPTION

The 680b-Process Control Interface board allows interfacing with the real world of relays, switches, motors, fans, contacters, alarms, solenoids, heaters, etc.

The output section of the board consists of eight SPST relays, each capable of switching 120 VAC at 1 amp. The input section consists of eight opto-isolators which can be configured by the user to accept a wide range of voltages. The 680b-PCI contains four more opto-isolated signal lines which are configured as two pairs of handshake lines; one pair associated with the input section and one with the output section. Each pair consists of one input line and one output line, both optically isolated. All of the lines are completely isolated and balanced for use in environments with high levels of electrical noise.

680b PCI
SECTION II
THEORY OF OPERATION

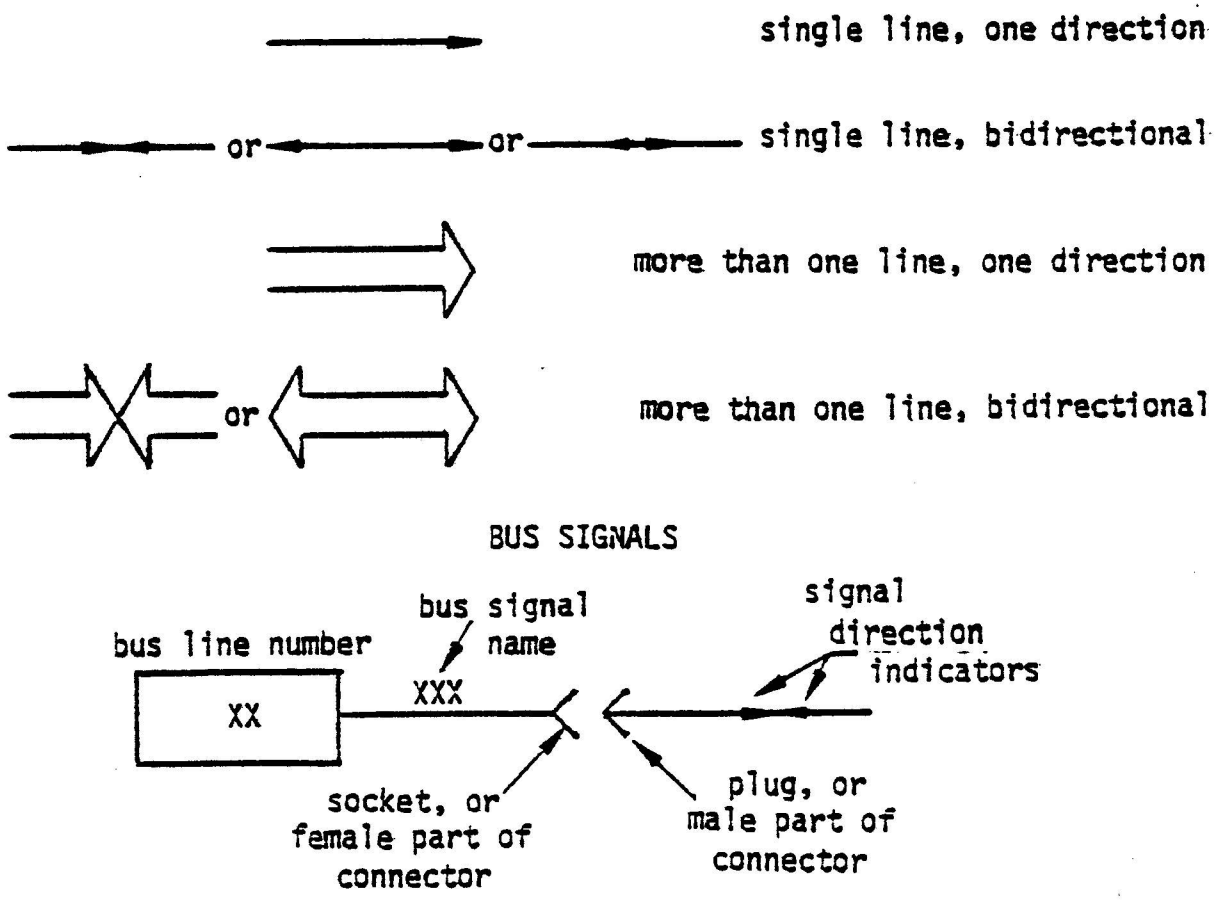
2-1. GENERAL CONTENTS

Section II contains technical data to aid in understanding the 680b-PCI's circuit operation. Contained in this section is information on schematic referencing, including a chart showing signal and bus line designations; information on logic circuits containing a chart with truth tables and a description of each logic circuit and its Boolean Algebra equivalent; a circuit description section explaining support logic; and a description of the board's input and output circuits.

2-2. SCHEMATIC REFERENCING

A detailed schematic of the 680b-PCI (Figure 2-7) is provided to aid in determining signal direction. Table 2-A shows how signal direction is indicated on signal lines and how to interpret the signal bus designations.

Table 2-A. Signal Direction and Bus Signals

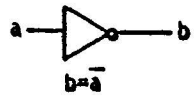
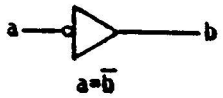
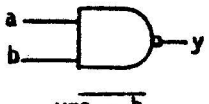
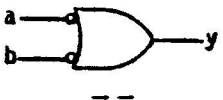
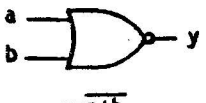
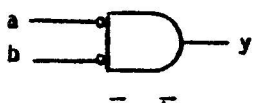


2-3. LOGIC CIRCUITS

The Logic Circuits shown in the 680b-PCI illustrations are presented in Table 2-B. This table contains the functional name, symbolic representation and a brief description of each logic circuit.

The active state of the inputs and outputs of the logic circuit is graphically displayed by the presence or absence of small circles. A small circle at an input to a logic circuit indicates the input is an active LOW; i.e. a LOW will enable the input. A small circle at the output of a logic circuit indicates the output is an active LOW; i.e. the output is LOW in the actuated state. Conversely, the absence of a small circle indicates that the input or output is active HIGH.

Table 2-B
Logic Circuits

Name	Normal	Equivalent	Description
Inverter or Buffer			An inverter is a gate whose output is the inverse of its input. a b 0 1 1 0
NAND gate			The NAND gate gives a LOW output when all of its inputs are HIGH. As the truth table will show, it is the equivalent of an OR gate with all of its inputs inverted. a b y 0 0 1 0 1 1 1 0 1 1 1 0
NOR gate			The NOR gate gives a LOW output when any of its inputs are HIGH. It is equivalent to an AND gate with all of its inputs inverted. a b y 0 0 1 0 1 0 1 0 0 1 1 0

1=HIGH
0=LOW

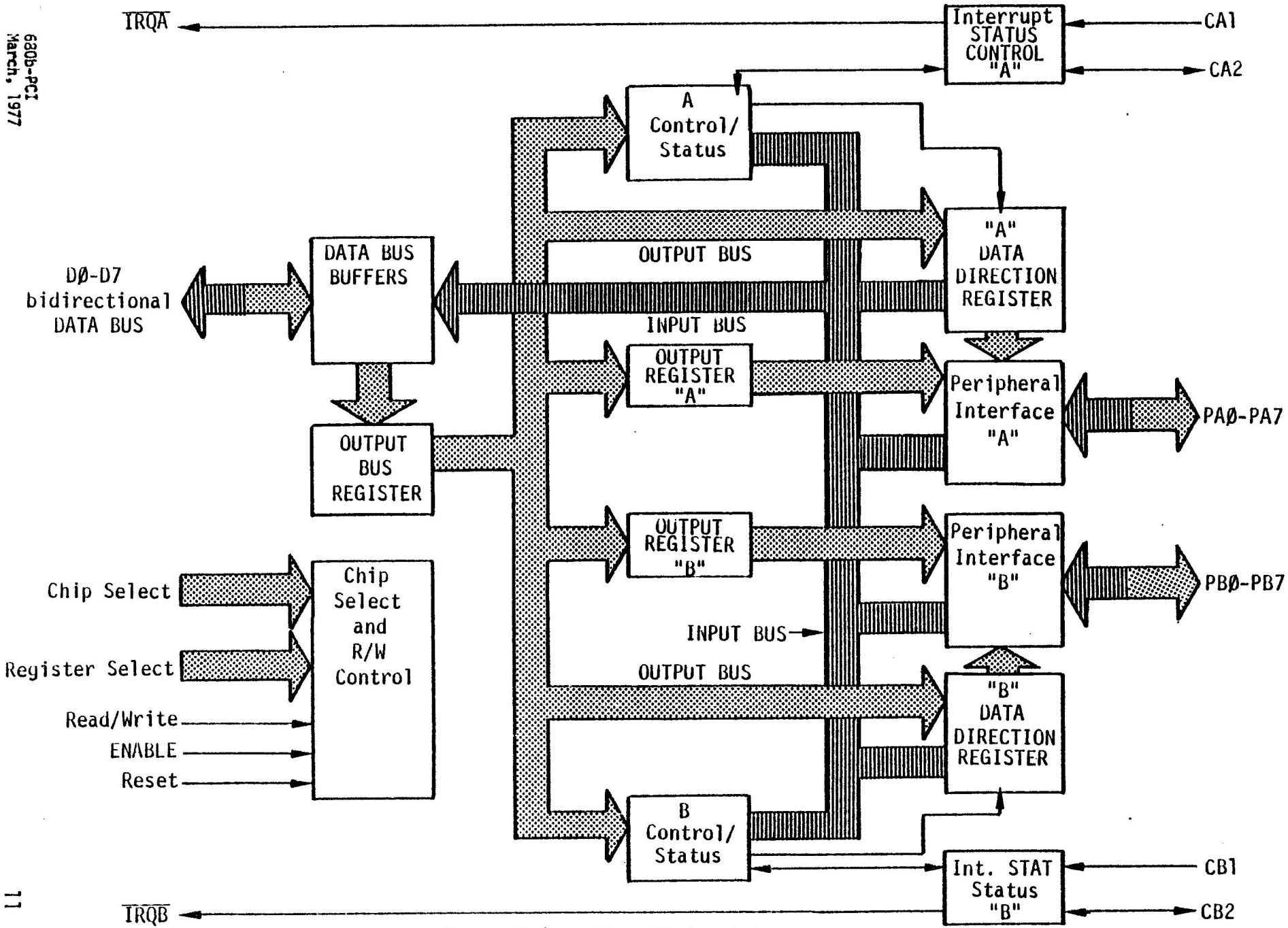


Figure 2-2. 6820 PIA Block Diagram

The 6820 utilizes four addresses. (Refer to Table 2-C, Register Selection.) The first address, or base address, selects Control/Status Register A. The second address (base address + 1) selects the Data Direction Register or the Data Channel Registers* themselves. The Control/Status Register determines which of these registers will be used. The next address (base address + 2) selects Control/Status Register B, and the last address (base address + 3) selects Data Direction Register B or Data Channel Register B.

The only timing signal going into the 6820 is the ENABLE (E pulse). The Ø2 (phase two clock) line is tied directly to the ENABLE signal. All data is transferred from one register to the other when the ENABLE signal is valid.

2-6. Support Logic

A. Addressing

The 680b-PCI board contains 64 possible locations that may be selected in increments of four. Refer to the addressing logic diagram, Figure 2-3. The address lines enter the board from the bus through an edge connector (shown by two interlocking arrows). The next (solid) arrow on the line indicates signal direction on the board.

*The Data Channel Register used for inputs is shown on the 6820 PIA Block Diagram as the Peripheral Interface (A or B). The Data Channel Register used for outputs is shown as the Output Data Channel Register. The Peripheral Interface is regarded as a Data Channel Register only during inputs, and the Output Data Channel Register is regarded as a Data Channel Register during outputs.

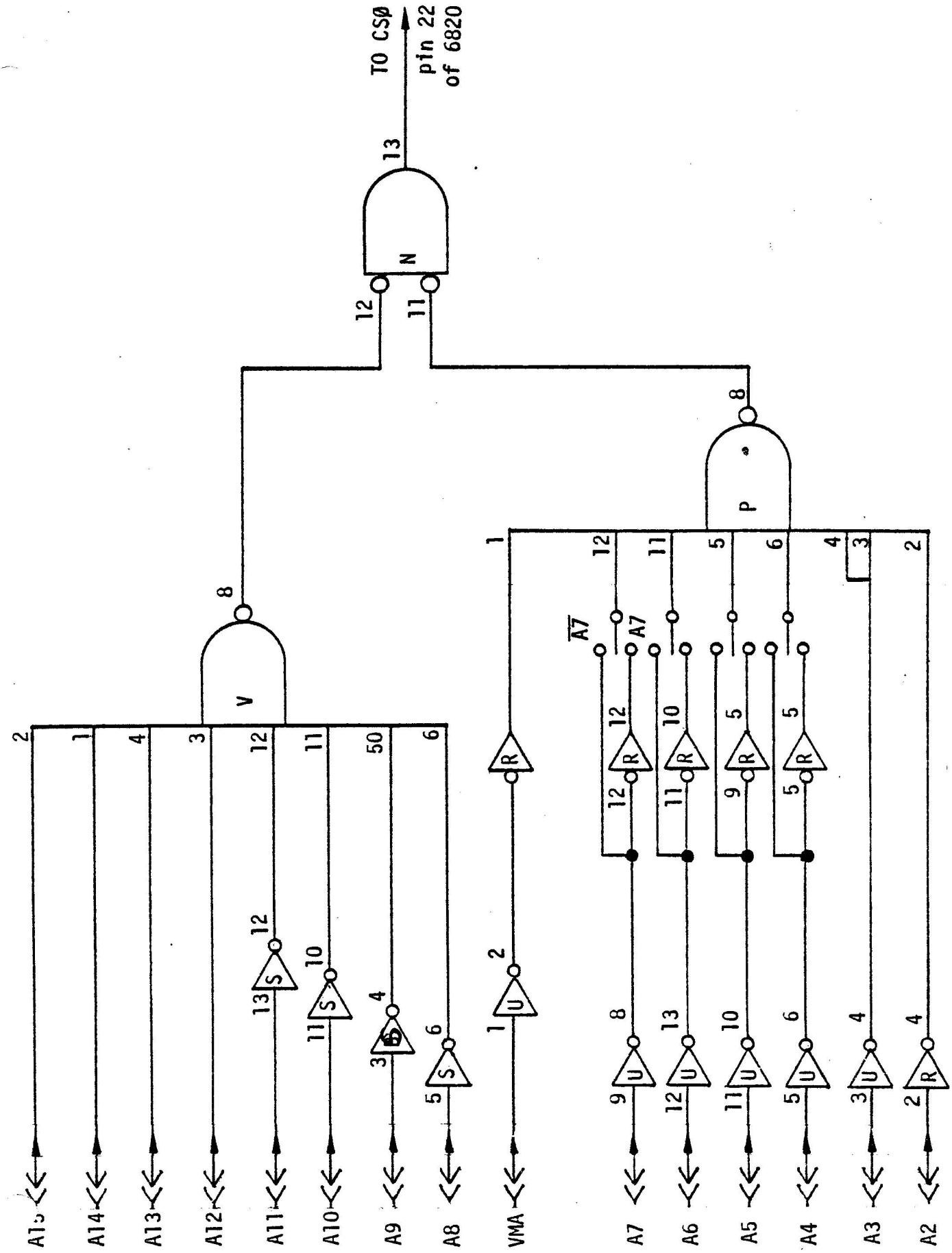


Figure 2-3. Addressing Logic Diagram

Refer to the schematic, Figure 2-7. Address lines A15 through A12 enter the board in a HIGH logic state and are tied directly to input pins 2 (zone A8), 1, 4 and 3 (zone A7) of NAND gate V. The next four address lines (A11 through A8) enter the board in a LOW logic state. Each is inverted at IC S, input pins 13, 11 (zone A7), 3 and 5 (zone A6), respectively, producing a HIGH logic signal at output pins 12, 10, 4 and 6.

After entering NAND gate V (zone A7), all eight signals produce a LOW output at pin 8, thus tying a LOW signal at input pin 12 of IC N (zone B5).

The Valid Memory Address (VMA) line comes onto the board from the 680b in a HIGH logic state. It goes to IC U (zone A6) and is inverted at output pin 2. The inverted signal goes to IC R (zone A6) and is inverted again at output pin 2. This signal enters input pin 1 of NAND gate P (zone B5).

Address selection of the board is accomplished by Switch 1 (SW1). All four address lines (A4, A5, A6 and A7) operate in the same manner. They are inverted and brought to four separate address switches. Because these lines are identical in operation, only one line (A7) is described here.

A7 comes onto the board from bus line 9 and enters inverter U at input pin 9 (zone A6). The signal is inverted at output pin 8 of IC U and is tied to the $\overline{A7}$ pole of SW1 (zone B6). The signal is also tied to inverter R (zone B6) at input pin 13 which brings it back to its original polarity at pin 12. The output at pin 12 is then sent to the A7 pole of SW1 (zone B6), thus making both the address line and its inversion available at SW1.

Address lines A3 and A2 are inverted HIGH at inverters U (output pin 4, zone A5) and R (output pin 4, zone A5). These HIGH signals go directly to input pins 4, 3 (which is tied to pin 4) and 2 of NAND gate P (zone B5).

CHIP SELECT ZERO (CSØ) occurs only when all of the inputs to ICs V (zone A7) and P (zone B5) are HIGH, thus producing LOW signals at IC N (zone B5), input pins 12 and 11. These two LOW inputs at IC N produce a HIGH output at pin 13. This means that the address lines (A7 through A4) selected at SW1 must be HIGH at the bus. If any inverted address lines ($\overline{A7}$ through $\overline{A4}$) have been selected at SW1, they must be LOW at the bus so that after inversion they will appear HIGH at all eight inputs of IC P (zone B5). For example, to strap the board at beginning location F010, $\overline{A7}$, $\overline{A6}$, $\overline{A5}$ and A4 should be selected at SW1.

Address lines AØ and A1 also come in from the bus. AØ is inverted at output pin 12 of IC T (zone A4) and goes to Register Select Ø (RSØ, pin 36 of the 6820), where it selects between the Control/Status Register (when AØ is LOW and RSØ is HIGH) and the Data Channel Register or the Data Direction Registers (when AØ is HIGH and RSØ is LOW). This is in keeping with the Altair™ standard of even order addresses for control/status and odd order addresses for data. A1 is inverted at output pin 2 of IC T (zone A4) and again at output pin 4 of IC T (zone A4) and goes to RS1 (pin 35 of the 6820) where it selects either Section A (when A1 and RS1 are LOW) or Section B (when A1 and RS1 are HIGH). Section A, the input channel, reads from the opto-isolators; Section B, the output channel, controls the relays.

Table 2-C

READ/WRITE, DATA BUS, ENABLE, RESET and $\overline{IRQ}$						
Base Address	$\overline{A0}$	$\overline{A1}$	C/S	Section	RSØ	$\overline{RS1}$
BA + 1	AØ		D-DDR	A	$\overline{RSØ}$	
BA + 2	$\overline{A0}$	A1	C/S	Section	RSØ	RS1
BA + 3	AØ		D-DDR	B	$\overline{RSØ}$	

A1=RS1

A0=$\overline{RSØ}$

B. READ/WRITE, DATA BUS, ENABLE, RESET and $\overline{IRQ}$

The READ/WRITE line comes off the bus at line 5 and is inverted at pin 8 of IC T (zone A4). It is inverted again at pin 10 of IC T (zone A4) and tied to pin 21 of the 6820 (zone B4). The R/W line controls the direction of data flow on the bidirectional data lines. In the Read mode data is received on the data bus from the opto-isolators. In the Write mode data is transmitted from the data bus into Section B in order to operate the relays.

The Ø2 (phase two clock, 500 KHz) line is tied directly to the ENABLE (E) signal of the 6820 (pin 25, zone B5). The E pulse is the only timing signal supplied to the 6820. All of the 6820's internal signals are clocked by the leading and trailing edge of the E pulse.

$\overline{IRQ}$ (pins 37 and 28 of the 6820) is also tied directly to the bus at line 96 (zone A3).

The RESET line ($\overline{RST}$, pin 34 of the 6820, zone B6) is an active LOW signal and is activated when the system is turned on. When power is first applied, transistor Q12 (zone B7) is turned on. Q12 holds the RESET line LOW until C4 can obtain enough charge to turn on transistor Q11, which turns Q12 off. This ends the RESET operation by pulling the RESET line HIGH.

2-7. Relay Outputs

Refer to Figure 2-4. The line labelled "FROM 6820" is a B Section output line (PBØ through PB7) which drives the base of a switching (or driving) transistor through a limiting resistor. When this transistor conducts, the current is allowed to flow through the relay coil, thus energizing the relay. The diode and resistor (in series across the coil) act as a suppression circuit for the inductive transient that is generated when the transistor is turned off and the coil is deenergized.

Increased relay contact life and lower electrical noise are two of the benefits of relay suppression. Because the suppression scheme is different for each type of load and power supply, this suppression should be supplied by the user. Various methods of suppression are covered in detail in Section III, Paragraph 3-4.

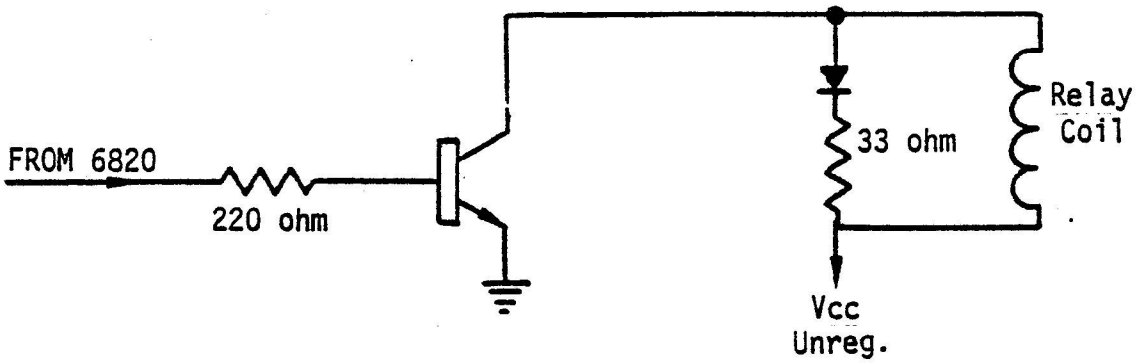


Figure 2-4. Relay Outputs

2-8. Opto-Isolators

Refer to Figure 2-5. An opto-isolator consists of an LED (or other light source) optically coupled to a photo-transistor (or other detecting device). The purpose of the opto-isolator is to maintain a high degree of electrical isolation between input and output while transmitting data. While this function can be carried out with other devices (such as relays, isolation transformers or blocking capacitors), the opto-isolator can be used with high switching speed, low cost and easy interfacing with other semi-conductor circuitry. The opto-isolators used here are the LED/photo transistor type. The operation of the circuit is as follows:

A. Inputs

The input to the LED is a network consisting of a diode, a resistor and a capacitor. LEDs are very sensitive to damage by reverse biasing. The diode provides protection against this type of damage. The resistor is used to limit current through the LED, and the capacitor (in conjunction with the diode) acts as a debouncing circuit. When current flows through the LED, the transistor conducts. When the photo transistor is conducting, the junction of the collector of the transistor, the pullup resistor and the line labelled "TO 6820" is essentially grounded, producing a logic LOW. When the transistor

is not conducting, the pullup resistor pulls the junction HIGH, producing a logic HIGH signal. (Further details on input network selection are given in Section III, Paragraph 3-5.) Handshake lines CA1 and CB1 are identical in operation to the other opto-isolated inputs.

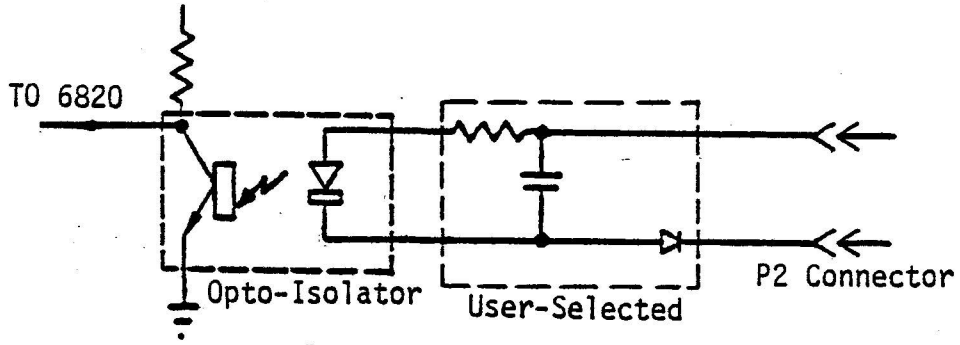


Figure 2-5. Opto-Isolator Inputs.

B. Outputs

There are two opto-isolated outputs (CA2 and CB2) that are also handshake lines. Refer to Figure 2-6. The line labelled "FROM 6820" is an output line that goes through two inverters so that both the inverted and non-inverted signals are available at the jumper, thus allowing selection of either HIGH or LOW active signals. These are applied to the base of a transistor through a current limiting resistor. When the transistor is conducting, it carries current through the LED in series with a current limiting resistor. When the LED conducts, it emits light that falls on the photo transistor. This produces a conducting output to the two handshake lines going out to the connector, CA2 and CB2.

These lines can be configured in two ways. If a resistor is connected from the collector line to a positive voltage and if the emitter line is grounded, the collector line then becomes a signal line. Thus, when the LED and the photo-transistor are conducting, a logic LOW is produced.

When neither the LED nor the photo-transistor are conducting, a logic HIGH is produced. If the collector is connected to a positive voltage and a resistor is connected between the emitter and ground, the emitter lead then becomes an output that produces a HIGH logic signal when the transistor is conducting or a LOW logic signal when it is not conducting.

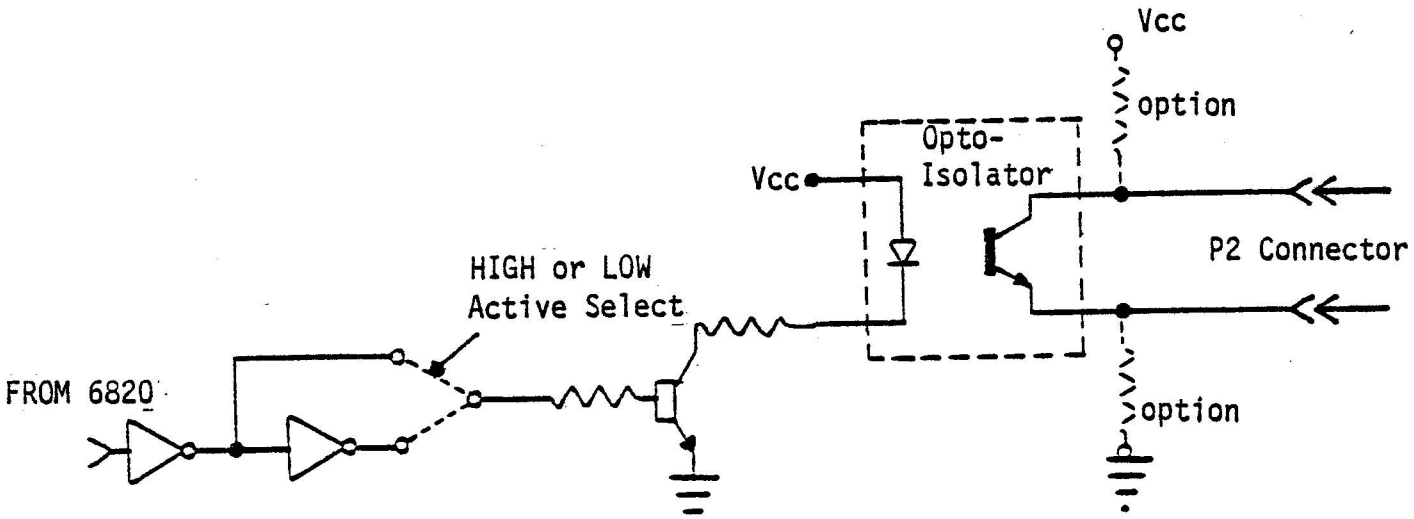


Figure 2-6. Opto-Isolator Outputs.

2-4. CIRCUITRY

Paragraphs 2-5 through 2-8 describe the circuitry of the 680b-PCI board. Included in this section is an overall block diagram (Figure 2-1) and several smaller diagrams detailing individual circuit areas. Schematic zone references are also provided for use with these diagrams.

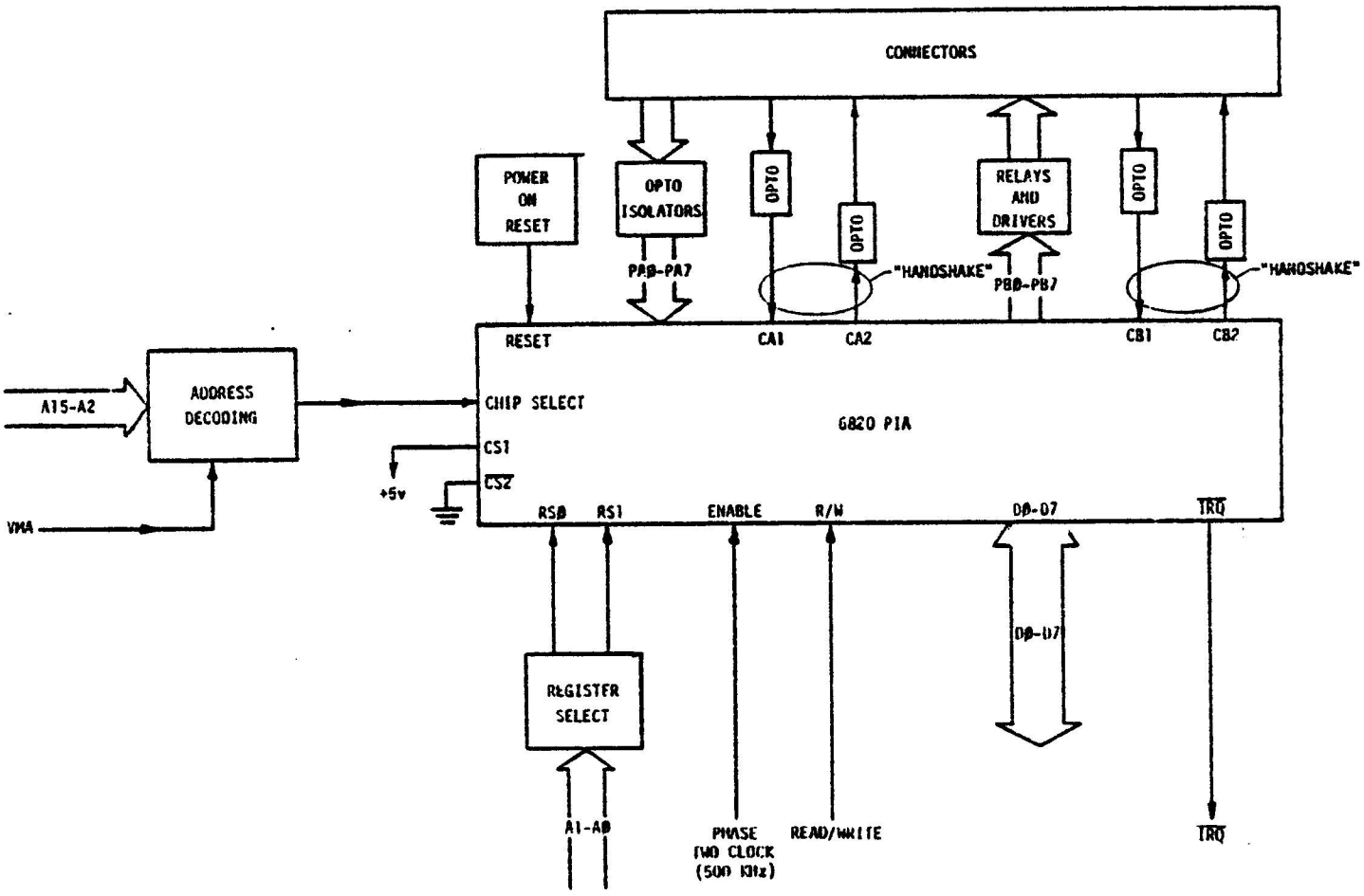


Figure 2-1. 680b-PCI Block Diagram

2-5. 6820 PIA

Refer to Figure 2-2. The 6820 Peripheral Interface Adapter (PIA) contains all the circuitry necessary to implement and control the eight incoming data lines (PAØ-PA7) from the opto-isolators, the eight outgoing data lines (PBØ-PB7) which control the relays and the two sets of bidirectional handshake lines. Handshake lines CA1 and CA2 are used with Section A, and lines CB1 and CB2 are used with Section B. The lines connecting the 6820 to the rest of the system consist of eight bidirectional data lines (DØ-D7), one interrupt request line ($\overline{IRQ}$), lines to do chip select (CSØ, CS1 and $\overline{CS2}$) and register select (RS1 and RSØ) within the chip, lines to control read and write states (R/W), a line to enable the chip (E) and a line to reset the chip (RST).

The 6820 has a large number of software controllable functions. For instance, the PA and PB lines can be enabled as either inputs or outputs by software, and many of the functions of the control lines can be changed or controlled through software. The configuration of the peripheral interface (how the data lines are set up with their inputs or outputs) is under the control of the Data Direction Register. In the initialization process, it is necessary to do an output to the Data Direction Register in order to tell the PIA which lines to set up as inputs and which to set up as outputs. The relationship of control lines CA1 and CA2 to the interrupt request line ($\overline{IRQ}$) is controlled by Control/Status Register A. The relationship of control lines CB1 and CB2 to $\overline{IRQ}$ is controlled by Control/Status Register B.

Figure 2-7. 680b-PCI Schematic

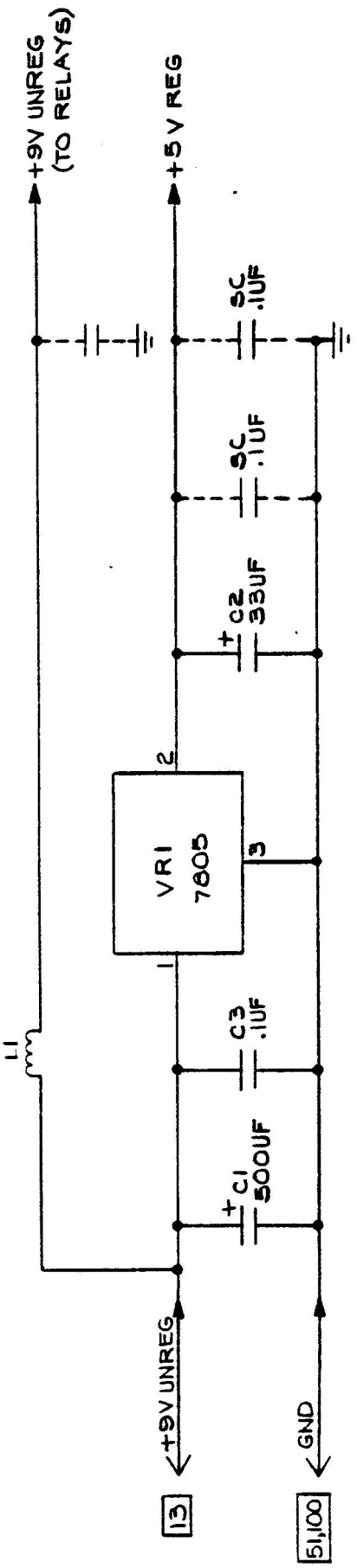


Figure 2-8. Power Supply Schematic

680b PCI
SECTION III
USER INFORMATION

3-1. INTRODUCTION

Section III is designed to help the user set up and initialize the 680b-Process Control Interface board for his own individual needs. Contained in this section are: information and charts on hardware set-up procedures, relay contact life, opto-isolator inputs and outputs, software initialization, applications software including sample programs and several suggested applications.

3-2. HARDWARE SET-UP

The first step in the hardware set-up procedure is to determine the number of relays needed, the amount of current each relay must conduct, the amount of voltage each relay must carry, and the manner in which the on-board relays will connect to the external circuitry.

When an amount of current and voltage has been determined, check the Relay Life Chart (Figure 3-3, page 33) to make sure that particular combination will yield an acceptable relay life. For example, 120 VAC at 1 amp resistive (power factor = 1) yields a life of approximately 500,000 operations. If the resulting life of the chosen combination is unacceptable, the relay on the board may be used to drive a contacter or a larger relay.

3-3. Cable Connections

When connecting the voltage and current to the board to be switched, the connections should be made (25-pin DB to P1) according to Table 3-A. Use #24 (or larger) wire with insulation sufficient to withstand the anticipated maximum voltage that will be encountered. The wire must also be able to withstand any abrasion, oil or weather exposure that may be expected during normal use.

CAUTION

When hazardous voltages and currents are to be used, be sure to check the local electrical codes for your area. All lines having such voltages should be fused.

Table 3-A. Cable Connections

P2 to 25-pin DB				P1 to 25-pin DB			
PA0	6 5	7+ 6-		PB0	2 1	2 Gray 1 Black	
PA1	1 2	2+ 3-		PB1	4 3	4 Violet 3 Black	
PA2	7 8	8+ 9-		PB2	6 5	6 Blue 5 Black	
PA3	9 10	10+ 11-		PB3	8 7	8 Green 7 Black	
PA4	11 12	12+ 13-		PB4	10 9	10 Yellow 9 Black	
PA5	24 23	14+ 15-		PB5	13 12	13 Orange 12 Black	
PA6	16 15	22+ 23-		PB6	15 14	15 Red 14 Black	
PA7	18 17	20+ 21-		PB7	17 16	17 Brown 16 Black	
CA1	14 13	24+ 25-		CB1	21 20	21 Gray (Anode) 20 Black (Cathode)	
CA2	22 (Coll) 21 (Emit)	16 (Coll) 17 (Emit)		CB2	19 (Coll) 18 (Emit)	19 White (Coll) 18 Black (Emit)	

Note: Pin 11 of the P1 connector should be keyed.

Figure 3-1 illustrates the general connection for the relay section of the board.

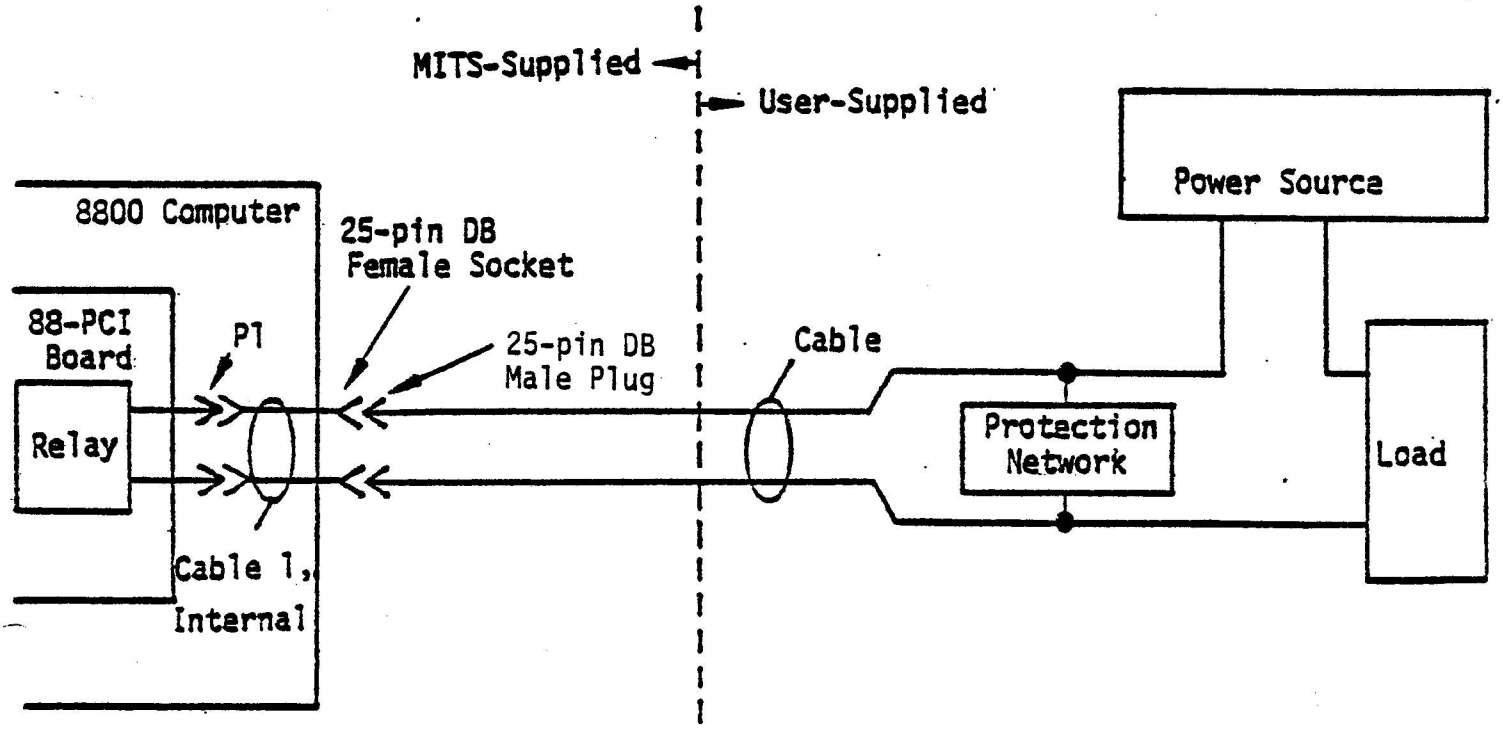


Figure 3-1. General Relay Connections

3-4. Relay Contact Protection and Suppression

There are two important advantages to relay protection. First, relay life can be doubled, or tripled in some cases, by protecting the relays from arcing when the contacts open and close. During normal use, unprotected relays may become pitted because of this arcing. Second, electromagnetic and radio frequency interference that can cause erratic circuit performance can be reduced through arc suppression.

Protection networks and their interconnections should be assembled in a suitable chassis. (Note: Network assembly can be made within the chassis of an existing piece of equipment.) The protection networks should be located as close to the relays as possible in order to minimize the inductive effects of long lines.

A resistor and a capacitor used in series across the contacts is one means of protection for the contacts used in DC circuits. Refer to Figure 3-2a. Component values should be selected to suppress arcing, but they should not affect load performance. The best way to select these values is through empirical testing. The capacitance should be large enough for worst-case conditions and the resistance large enough to limit capacitor charge/discharge. If the resistance is too small, the contacts will weld shut; but if the resistance is too large, the purpose of the capacitor may be defeated. The formula shown below provides a nominal starting value.

$C=I^2/10$, where:
C=Capacitance in microfarads
I=Current in amps

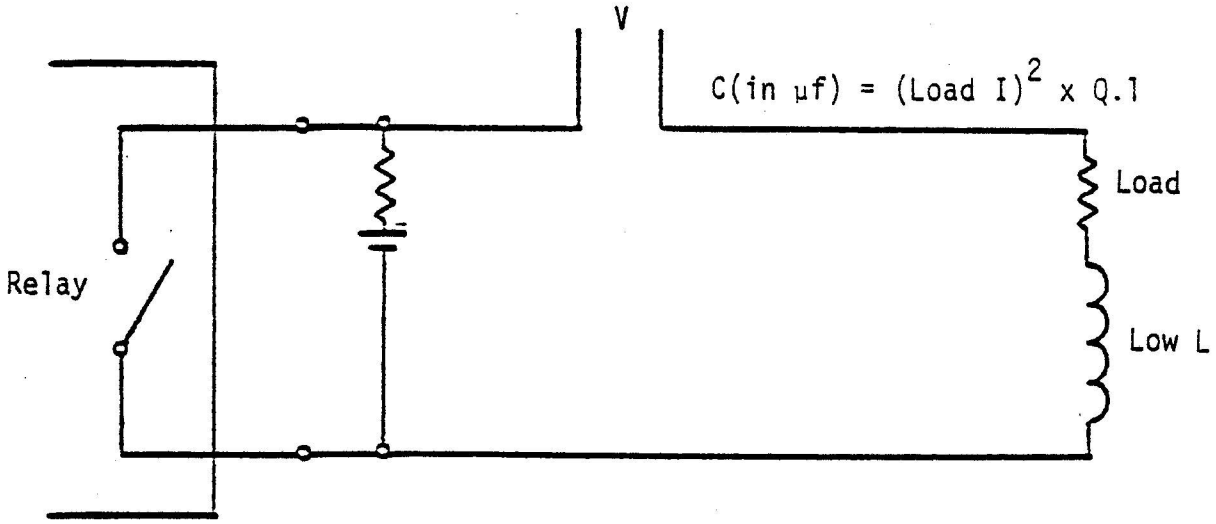


Figure 3-2-a. Relay Contact Protection for DC Loads (Resistor and Capacitor Circuit)

The protection circuit shown in Figure 3-2b is another method used with DC loads. When separation occurs, it gives a near-zero voltage drop across the contacts (even on highly inductive loads). The values of the capacitor and the diode are selected so that at the instant of separation, the peak voltage to which the capacitor charges will not cause breakdown of the diode, the contact gap or the capacitor itself.

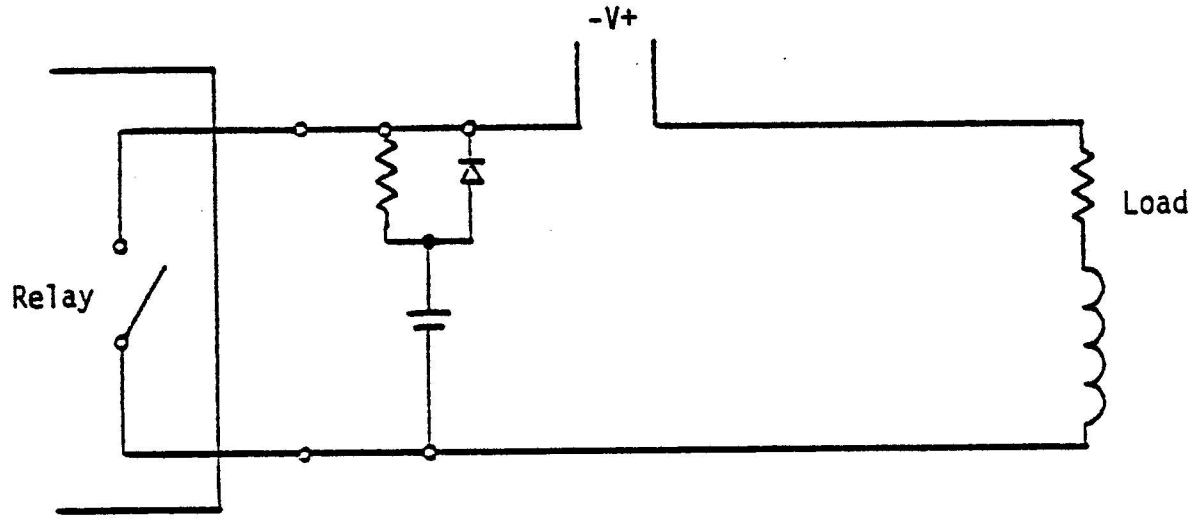


Figure 3-2-b. Relay Contact Protection for DC Loads (Capacitor and Diode Circuit)

In AC loads, after contact separation, an alternating current arc is extinguished when current passes through zero. Therefore, contact protection for AC loads (particularly resistive loads) is not as critical as for DC loads. An arc can last no longer than 8.3 milliseconds on a 60 Hz line since the current reversal occurs 120 times per second. Thus, the higher the frequency, the shorter the duration of the arc.

Figure 3-2c illustrates a contact protection circuit for an AC inductive load. This network allows the arc to extinguish naturally by making an inductive load appear resistive to the contacts.

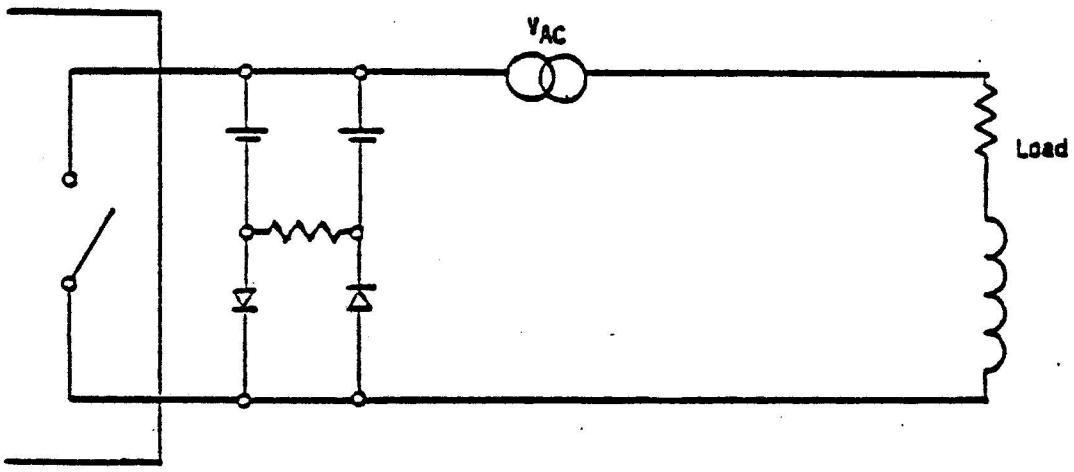


Figure 3-2c. Relay Contact Protection for AC Inductive Loads

Figure 3-3 shows the expected life of relay contacts vs. load current for various voltages and power factors.

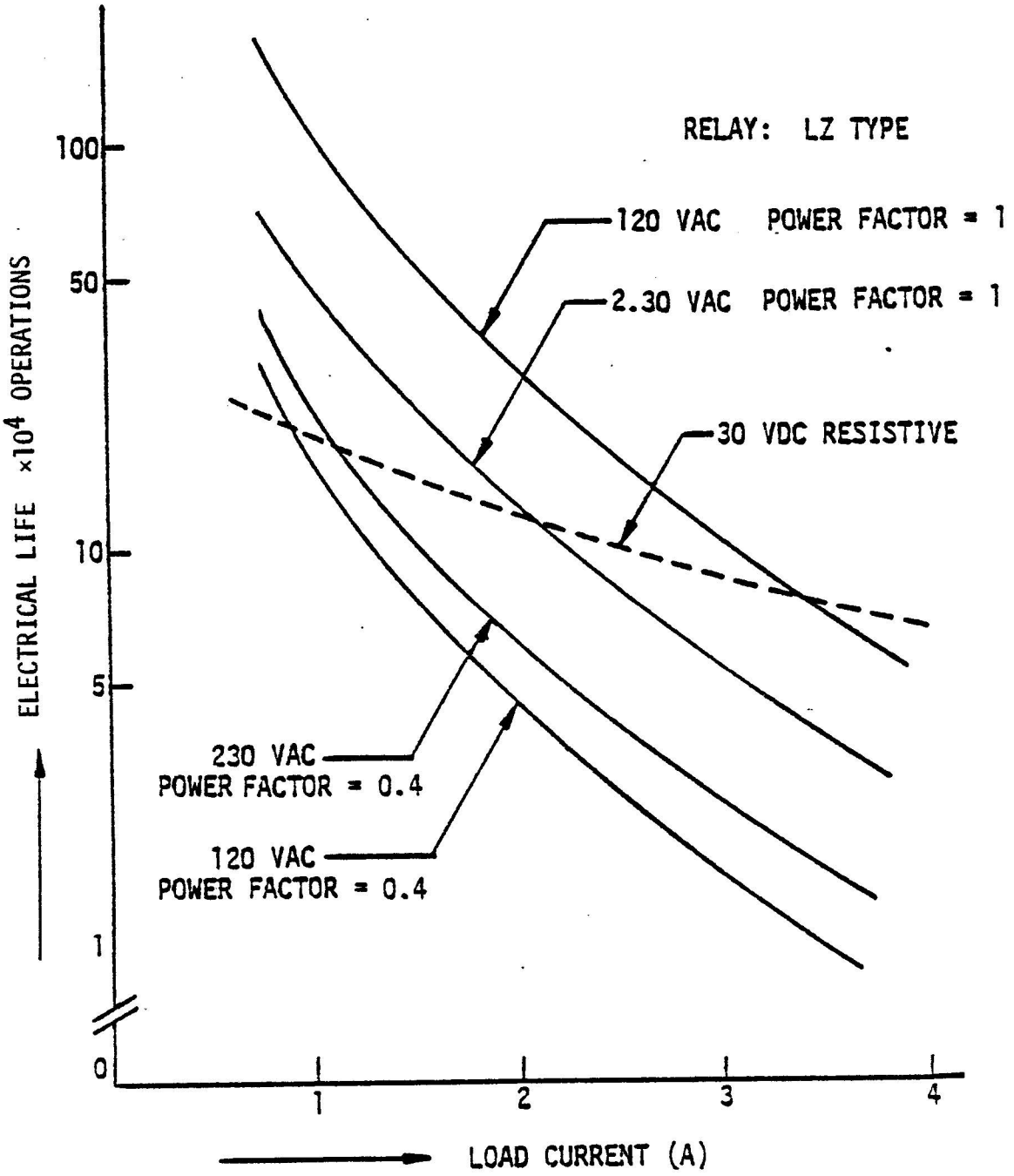


Figure 3-3. Relay Contact Life

3-5. Opto-Isolator Input Connections

Connecting the opto-isolator inputs is fairly simple. The main considerations are:

a) the amount of voltage applied to the inputs

b) the length of switching time and propagation delays of the opto-isolators

c) how to transmit the signals to the board

A simplified general connection scheme is shown in Figure 3-4.

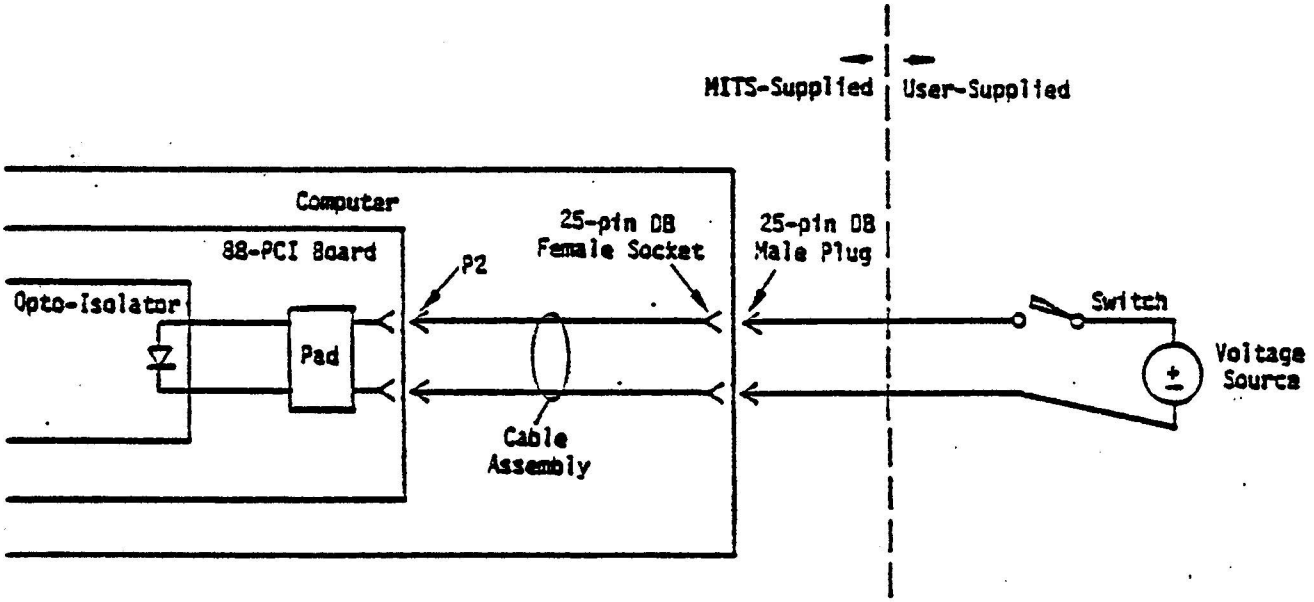


Figure 3-4. Opto-Isolator General Connections

Use the following calculations to determine the active and non-active ranges of the forward current in the LED (I_{LED}). Refer to Figure 3-5.

The Process Control Interface board contains pads to provide a circuit which adapts the inputs to a wide range of voltages and pulse widths. A diagram of this circuit is shown in Figure 3-5. A description of the Altair-supplied circuit configuration is given on page 38.

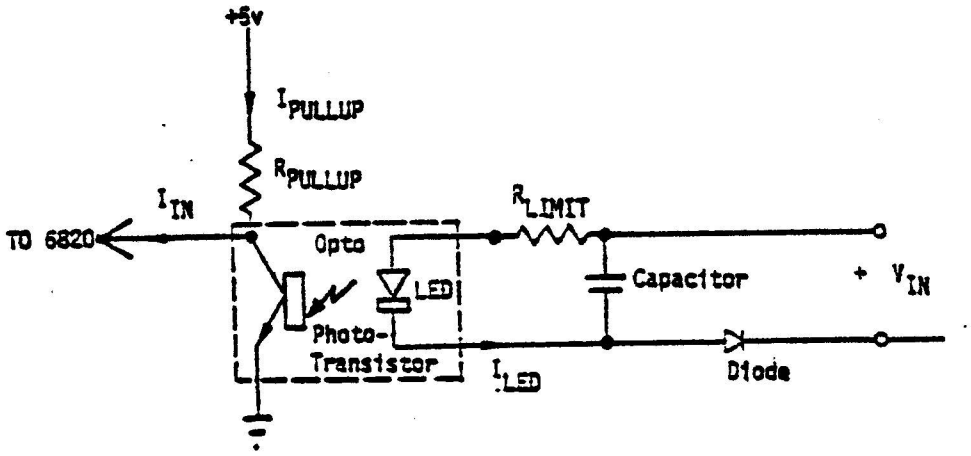


Figure 3-5. Input Voltage Adaptor Circuit

For CA1 and CB1:

Input leakage is 2.5 microamps (max). Since this amount is negligible, the input current to the 6820 (I_{IN}) is virtually 0. Therefore, the current through the pullup resistor (I_{PULLUP}) is equal to I_C, where I_C is the collector current in the photo transistor of the opto-isolator. Input high voltage (V_{IH}) is 2.0 volts (min) which makes the voltage across the R_{PULLUP} equal to V_{cc} (+5v) - V_{IH} (+2.0) = 3 volts.

$$I_{PULLUP}\ (max) = I_C\ (max) = \frac{3\ volts}{2.2K\ ohms}\ (R_{PULLUP}) = 1.36\ milliamps\ (max)$$

With current transfer ratio (CTR) = 35%, I_{LED} = 3.90 milliamps (max). Therefore, the maximum input current through the LED (I_{LED}) allowable for a logic HIGH at the CA1 or CB1 input to the 6820 is 3.9 milliamps.

Input low voltage (V_{IL}) is 0.8v (max). Therefore, the minimum voltage across the $R_{PULLUP} = V_{cc} - V_{IL} = 5.0 - 0.8 = 4.2v$.

$$I_{PULLUP}\ (min) = I_C\ (min) = \frac{4.2v}{2.2K\ ohm} = 1.91\ milliamps\ (min)$$

With CTR = 35%, I_{LED} = 5.45 milliamps (min)

Thus, for a logic LOW at the CA1 or CB1 input to the 6820, the minimum input current through the LED (I_{LED}) is 5.45 milliamps.

For inputs PAØ-PA7:

Input HIGH current (I_{IH}) = -100 microamps (min)

Input LOW current (I_{IL}) = -1.6 milliamps (max)

Input HIGH voltage (V_{IH}) = 2.0 (min)

Input LOW voltage (V_{IL}) = 0.8 (max)

For a logic HIGH at the 6820:

$$I_{PULLUP}\ (max) = \frac{V_{cc} - V_{IH}}{R_{PULLUP}} = 1.36\ milliamps\ (max)$$

$$I_C = I_{PULLUP} - I_{IH} = 1.36 - (-.1) = 1.46\ milliamps\ (max)$$

$$I_{LED}\ (max) = I_C/CTR = \frac{1.46}{35} = 4.17\ milliamps\ (max)$$

For a logic LOW at the 6820:

$$I_{PULLUP}\ (min) = \frac{V_{cc} - V_{IL}}{R_{PULLUP}} = \frac{5.0 - 0.8}{2.2K\ ohms} = 1.91\ milliamps\ (min)$$

$$I_C = I_{PULLUP} - I_{IL} = 1.91 - (-1.6) = 3.51\ milliamps\ (min)$$

$$I_{LED}\ (min) = I_C/CTR = \frac{3.51}{.35} = 10.03\ milliamps\ (min)$$

The active and inactive LED currents are shown in Table 3-B.

Table 3-B

Active and Inactive LED Currents

	For CA1, CB1			For PAØ-PA7		
All in mA	Min.	Nominal	Max.	Min.	Nominal	Max.
I_{LED} for input LOW	5.45	10	100	10.03	15	10
I_{LED} for input HIGH	-0.1μA	0	3.90	-0.1μA	0	4.1

When the input voltage to the network (V_{IN}) is a pulse less than 20 microseconds, the switching time of the opto-isolator may be too slow to react to it. To add flexibility to the inputs so that short pulses can be detected, pads are provided to form a pulse stretching capacitor (C) as shown in Figure 3-6.

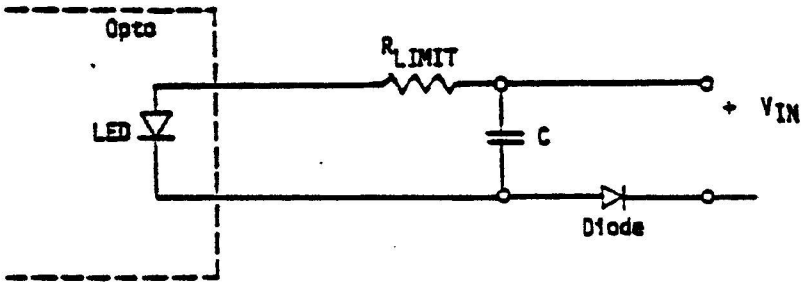


Figure 3-6. Pulse Stretching Capacitor

With a short pulse condition, the values of R_{LIMIT} and C for the user's own pulse height, width and shape can best be determined by empirical testing and by the capacitive drive capability of the input signal. The capacitor will be charged to the maximum input voltage (V_{IN}) less the forward voltage of the diode (V_D, which is approximately 0.7 volts). When the input voltage returns LOW, use the formula shown in Figure 3-7 to find the LED current.

$$I_{LED} = \frac{Vc - 1.3}{R} \; e \; (-t/RC)$$

t=time in seconds
Vc=Initial Cap. Voltage
R=R limit
C=Capacitor Size
e=2.71828

Figure 3-7. LED Current Formula

Because the LED in the opto-isolator has a maximum reverse current of 0.1 microamps or 100 nanoamps, the diode should be chosen for LOW reverse current leakage (I_R).

The opto-isolator inputs supplied are set up in an STD TTL interface as shown in Figure 3-8.

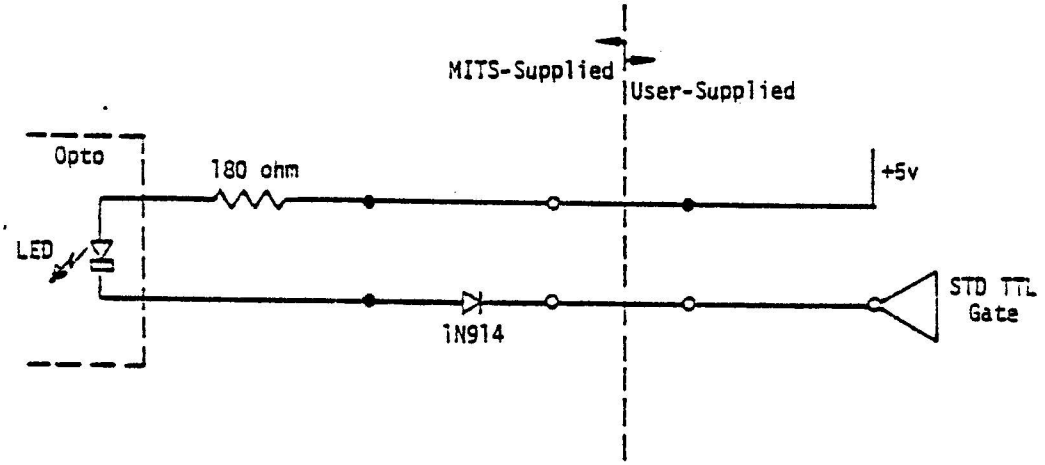


Figure 3-8. STD TTL Interface

In this form, the output of the TTL gates will sink approximately 15 milliamps in the LOW state and approximately 5-10 microamps in the HIGH state. Each of these currents is well within the limits shown in Table 3-B.

Table 3-C identifies the names of the individual components in each circuit shown as the general case in Figure 3-9. The two optically isolated outputs (ICAA and ICR) coupled to CA2 and CB2, respectively, are configured as follows.

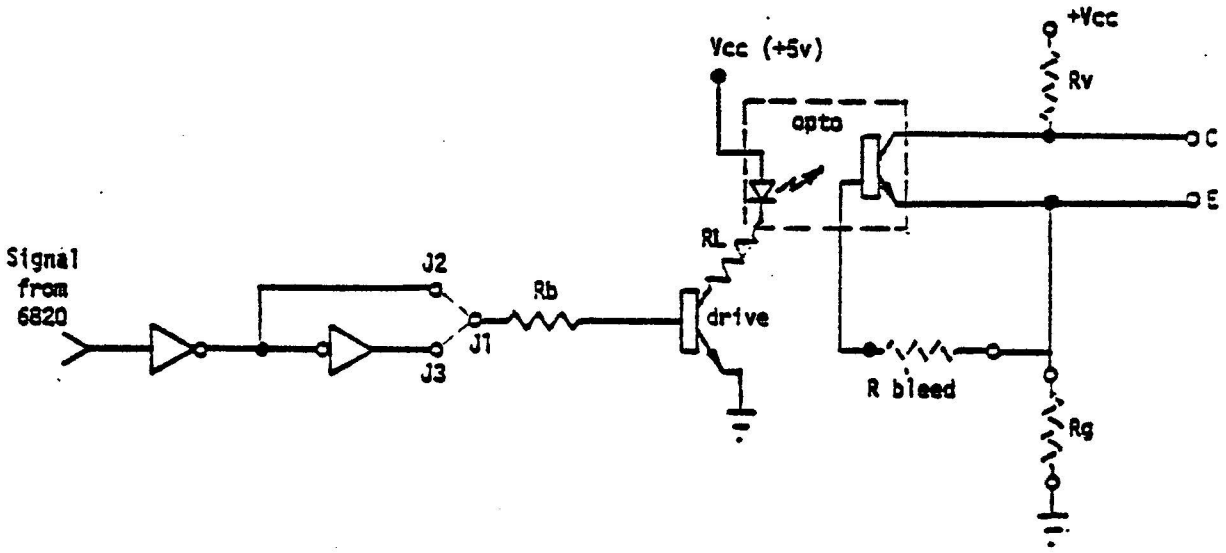


Figure 3-9. R_{bleed} Circuit :

Table 3-C

Opto-Isolator Output Configurations									
Signal	Jumper Pads			Components					
	J1	J2	J3	R_B	R_L	R_V	R_{bleed}	R_G
CA2	JA	JC	JB	R_{44}	R_{43}	R_{41}	R_{49}	R_{42}
CB2	JD	JF	JE	R_1	R_2	R_5	R_3	R_6

By connecting a jumper from J1 to J2 or J3, the user can select the operation that will cause the photo transistor in the opto-isolator to conduct when CA2 or CB2 is active (HIGH or LOW). If J1 is tied to J2, either control lines CA2 or CB2 will be active LOW; if J1 is tied to J3, either CA2 or CB2 will be active HIGH.

When a logic HIGH appears at the base of the drive transistor through R_B, approximately 36 milliamps flow through the LED. Thus, with a CTR of 35%, the photo transistor can conduct approximately 12.6 milliamps in this HIGH state. The maximum voltage which should be applied to the photo transistor (BV_{CEO}) is 20v, collector to emitter.

The user should be sure not to exceed the maximum dissipation limits of the opto-isolator which is a total of 200 milliwatts (LED + photo transistor). When the LED is conducting 36 milliamps, it is dissipating approximately 47 milliwatts. Therefore, dissipation in the transistor should be limited to about 150 milliwatts (max).

3-6. Opto-Isolator Outputs

The speed with which an opto-isolator responds to a signal (bandwidth) depends almost entirely on the sensor. For example, switching time is a function of the transistor base storage time and the output-circuit time constant. For better sensitivity, these parameters are traded off. The larger the collector base junction, the more sensitive the photo transistor. This results in longer storage time and slower switching time.

One problem often encountered when applying opto-isolators is minimizing switching time while using practical values of load resistance. (Time is directly proportional to R_L and C_{ob}, where R_L = Load Resistance and C_{ob} = Open Circuit Base Capacitance.) In most photo transistors, relatively long time constants occur in the output circuit because the typical value of C_{ob} is approximately 25 pico-farads. This time will be proportional to β where β is the photo transistor's current gain. For example, for a 500 ohm load a photo transistor with a typical minimum β value of 100 and a C_{ob} of 25 picofarads yields a time constant of (500) (25 x 10 - 12) (100) = 1.25 microseconds. Switching time is 5 time constants of 6.25 microseconds.

This corresponds to a bandwidth of only 130 KHz. When using load resistance values greater than 1K ohm, signals of no more than 500 KHz are executable with conventional opto-isolators.

The solution to the problem of long time constants is to provide an external path for removal of the stored charge. This can be accomplished by adding a base-to-emitter bleed resistor (R_{bleed} in Figure 3-9) that will reduce both sensitivity and Current Transfer Ratio (CTR) and will decrease the photo transistor's switching time. The limiting condition is zero ohms of bleed resistance. This shorts the base to emitter of the photo transistor, thus converting the device to a photo diode. It is at this point that the highest possible speed and the lowest sensitivity occur.

A resistor is not supplied for R bleed because current switching ability associated with infinite resistance is desirable and switching speed is adequate for most applications. If higher speed is needed, it can be achieved by experimenting with various values for R bleed. However, this will reduce the CTR considerably, and provisions in the external circuitry may have to be made to compensate for the lower switched current in the photo transistor.

Pads are provided for R_V and R_G (see Figure 3-9) which may be used to implement signals referenced to the computer's V_{cc} and GND. It is advisable to use these pads only where short cable runs are used and where isolation is unimportant. Generally, the supply and ground for the signals should be implemented in an external isolated chassis. Several examples of external output connections are shown below in Figures 3-10a through 3-10d.

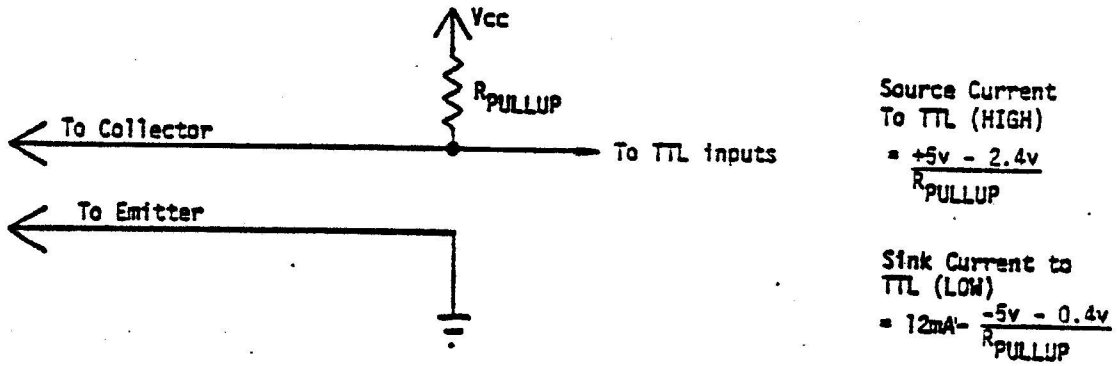


Figure 3-10a. External Output Connections

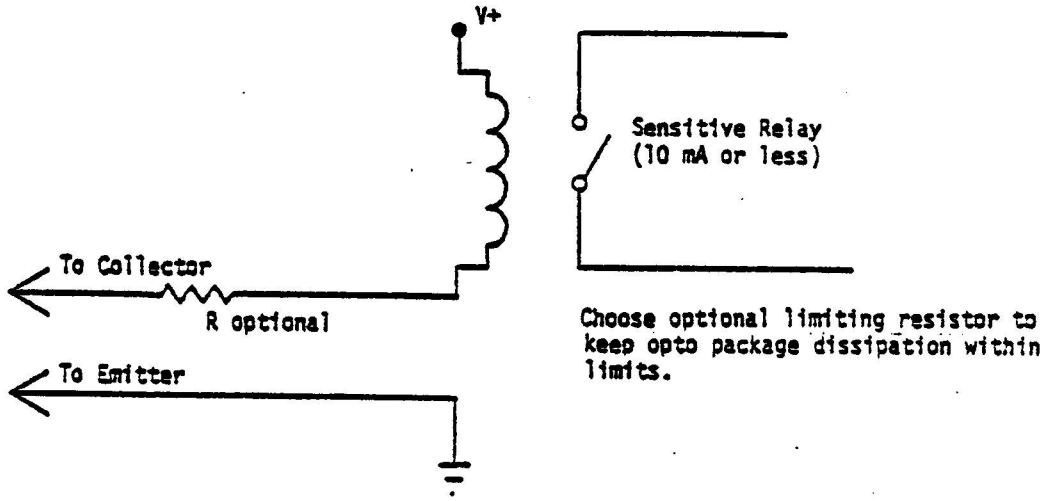


Figure 3-10b. External Output Connections

For more source current:

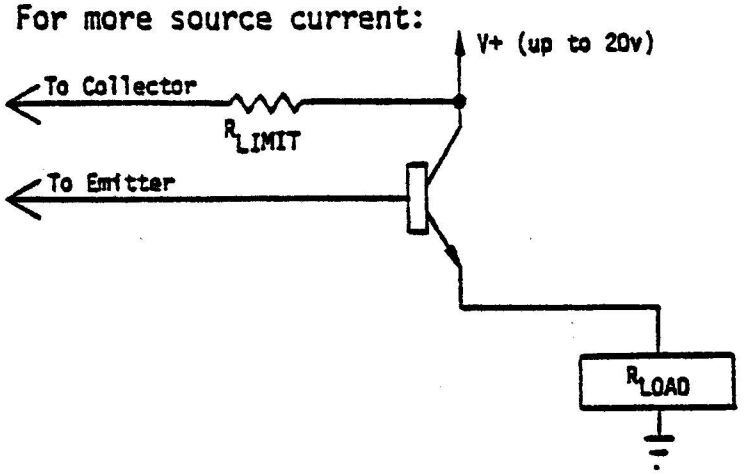


Figure 3-10c.
External Output Connections

For more sink current:

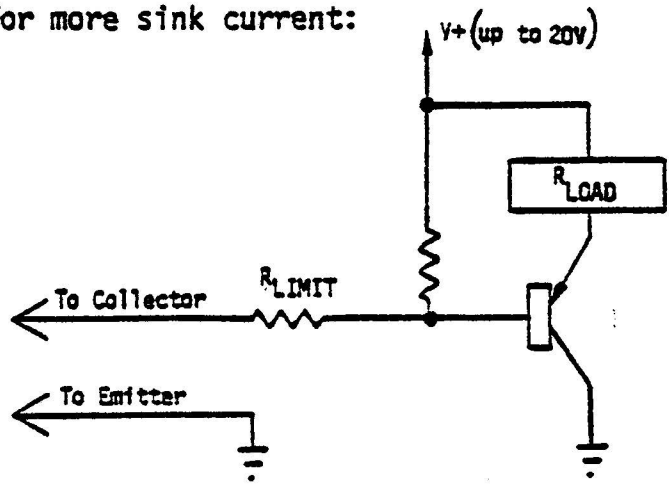


Figure 3-10d.
External Output Connections

3-7. SOFTWARE INITIALIZATION

Before the Process Control Interface board can be utilized, the 6820 PIA's Data Direction Registers and Control/Status Registers must be initialized. Refer to the Internal Register Addressing Diagram, Table 3-D. The two Data Direction Registers tell the PIA whether to set up its lines as inputs or outputs. The two Control/Status Registers control the functions of the CA1, CB1, CA2 and CB2 signal lines.

Table 3-D. Internal Register Addressing

Address Lines				Control Register Bit		Register Selected
RS0	A0	RS1	A1	CRA-2	CRB-2	
1	0	0	0	X	X	Control/Status Register (Section A)
0	1	0	0	0	X	Data Direction Register (Section A)
0	1	0	0	1	X	Data Channel Register (Section A)
1	0	1	1	X	X	Control/Status Register (Section B)
0	1	1	1	X	0	Data Direction Register (Section B)
0	1	1	1	X	1	Data Channel Register (Section B)

The Control/Status Registers also determine whether to write to the Data Register or the Data Direction Register. When writing to the Data Direction Register, it is necessary to set Bit 2 of the Control/Status Register to 0. The A Section Data Direction Register is enabled by writing 0's into the base address ("A" Control/Status Register). The B Section Data Direction Register is enabled by writing zeros into the base address + 2 ("B" Control/Status Register).

Refer to Table 3-D. With Bit 2 of the Control/Status Registers set at 0, the next time the user writes to the Data Channels (base address + 1 and base address + 3), he would be writing into the Data Direction Registers. Section A is connected to the opto-isolator inputs and Section B is connected to the Relays (outputs).

Therefore, to initialize Section A as an input section, 0's should be written into the Data Direction Register (at base address + 1). To initialize Section B as an output section, 1's should be written into the Data Direction Register (at base address + 3). (See example initializations in the Software Application Section, Paragraph 3-8.)

When the Data Direction Registers of Sections A and B have been initialized, the Control/Status Registers may be set up for their final operating form. Bit 2 of the Control/Status Registers must be set at 1. This will move the addressing from the Data Direction Registers to the Data Channel Registers.

Refer to Tables 3-E.1 through 3-E.4 for information on the various options of the control lines and their interaction with the Interrupt Request line, the Status Bit and the Control/Status Register.

Table 3-E.1. Control Line Options

Bit #	7	6	5 4 3	2	1 0
C/S Section A	IRQA 1 flag	IRQA 2 flag	CA2 Control	DDR-A Access	CA1 Control
C/S Section B	IRQB 1 flag	IRQB 1 flag	CB2 Control	DDR-B Access	CB1 Control

Table 3-E.2. Control Line Options

C/S Bit 1	C/S Bit 2	CA1 or CB1	Intr. flag C/S Bit 7	MPU $\overline{IRQ}$
0	0	↓ active	Set HIGH	disabled
0	1	↓ active	Set HIGH	Goes LOW when C/S bit 7 goes HIGH
1	0	↑ active	Set HIGH	Disabled
1	1	↑ active	Set HIGH	Goes LOW when C/S bit 2 goes HIGH
↓ = from HIGH to LOW signal transition				1=Logic HIGH
↑ = from LOW to HIGH signal transition				0=Logic LOW
Section A: C/S bit 7 (Int. flag) is Reset (LOW) by a read of A Section Data Channel Register.				
Section B: C/S bit 7 (Int. flag) is Reset (LOW) by a read of B Section Data Channel Register.				

Table 3-E.3. Control Line Options

CB2:				
C/S Bit 5	C/S Bit 4	C/S Bit 3	Cleared	Set
1	0	0	Low on ↑ of first E pulse after write of B Data Channel Register after C/S bit 7 is reset by a read of B Data Channel Register	HIGH when Int. flag (C/S bit 7) is SET
1	0	1	LOW on ↑ of first E pulse after a write of B Section Data Channel Register	HIGH on ↑ of next E pulse.
1	1	0	Always LOW when bit 3 LOW	
1	1	1		Always HIGH when bit 3 is HIGH
CA2 and CB2 differ slightly in function.				

Table 3-E.4. Control Line Options

For CA2:				
C/S Bit 5	C/S Bit 4	C/S Bit 3		
1	0	0	LOW on ↓ of E pulse after read of "A" Data Channel Register	HIGH when Int. flag (C/S bit 7) is set
1	0	1	LOW on ↓ of E pulse after read of "A" Data Channel Register	HIGH on ↓ of first E pulse which occurs while device is deselected
1	1	0	Same as CB2	
1	1	1		Same as CB2

3-8. APPLICATIONS SOFTWARE

Note: Throughout the Applications Software section, the 680b-PCI board is assumed to be addressed at base address location F010 (hexadecimal). For further addressing, see the Address Selection chart, Table 3-F.

Base address = F010 (hex)-Opto-Isolator Input Control/Status

Base address + 1 = F011 (hex)-Opto-Isolator in Data and Data Direction Register

Base address + 2 = F012 (hex)-Relay Control/Status

Base address + 3 = F013 (hex)-Relay Control Data and Data Direction Register

Table 3-F. Address Selection

	SW1 Switch Position			
Address	1	2	3	4
F010-13	down	up	up	up
F020-23	up	down	up	up
F030-33	down	down	up	up
F040-43	up	up	down	up
F050-53	down	up	down	up
F060-63	up	down	down	up
F070-73	down	down	down	up
F080-83	up	up	up	down
F090-93	down	up	up	down
F0A0-A3	up	down	up	down
F0B0-B3	down	down	up	down
F0C0-C3	up	up	down	down
F0D0-D3	down	up	down	down
F0E0-E3	up	down	down	down
F0F0-F3	down	down	down	down

Instructions: SW1 contains four separate switches that are labelled on the package. Table 3-F shows the proper setting for each switch to obtain the desired address location.

Up=switch is positioned closest to the back panel

Down=switch is positioned away from the back panel

The following programs are sample initialization programs for the 680b-PCI in Machine Language. The Index mode of addressing is used.

Program 3-I. Machine Language Initialization

Address	Hex	Mnemonic	Description
0000	CE	LDX	Set address F010
0001	F0	F0	in the Index Register
0002	10	10	
0003	4F	CLRA	Set all zeros in Accumulator A
0004	A7	STA A	Zero Control/Status Register location
0005	00	address	F010 of Section A (making bit 2=0, giving address to Data Direction Register).
0006	A7	STA A	Set all 0's in Data Direction Register at location F011,
0007	01	Address	making PA lines inputs
0008	A7	STA A	Zero Control/Status Register Location F012 of Section B. (Making Bit 2=0,
0009	02	address	accessing Data Direction Register of Section B).
000A	43	COM A	Set all ones in Accumulator
000B	A7	STA A	Write ones in Data Direction Register of Section B (location F013)
000C	03	address	Make PB lines outputs
000D	86	LDA A	Set bit pattern in Accumulator A
000E	24	bit pattern 00100100	
000F	A7	STA A	Store Bit Pattern in C/S Register A, Section A
0010	00	Address	Location F010
0011	A7	STA A	Store Bit Pattern in C/S
0012	02	Address	of Section B, location F012

Refer to Tables 3-E.1 through 3-E.4. The control lines in the preceeding program are set up as follows:

CA1 and CB1 = active LOW transition, $\overline{IRQ}$ disabled

CA2 = HIGH when CA1 is active, goes LOW on LOW transition of E pulse after a read of the "A" Data Channel Register.

CB2 = Set HIGH when Interrupt flag bit 7 of the B Section C/S Register is set (Bit 7 is set HIGH when CB1 is active). After bit 7 is reset by a read of the "B" Data Channel Register, CB2 goes LOW on HIGH transition of E pulse after a write of the "B" Data Channel Register.

Several examples of input/output software are listed in the following programs. These programs are used to input data through the opto-isolators and to output data to control the relays. The Index mode of addressing is used.

Program 3-II. Input

Address	Contents	Mnemonic	Description
N	A6	LDA A	Entering the contents of the opto-
N+1	01	address	isolator inputs into Accumulator A
N+2	84	AND A	Logical AND Accumulator A with
N+3	XX	data	immediate data (Mask for bits of
N+4	27 or	BEQ	interest) Conditional jump or
N+4	26	BNE	subroutine call
N+5	XX	*Relative Address	

Program 3-III. Output (to turn on a specific bit without affecting others)

Address	Contents	Mnemonics	Description
N	86	LDA A	Read the output Register for exist-
N+1	03	address	ing condition
N+2	8A	ORI	or Accumulator A with bits of data to
N+3	XX	data	turn on (to turn on bit 0, data would be 01)
N+4	A7	STA A	output the new
N+5	03	address	control word

Program 3-IV. Output (to turn off a specific relay without affecting others)

Address	Contents	Mnemonics	Description
N	A6	LDA A	Read existing output Register
N+1	03	address.	
N+2	84	AND A	And with complement of bits to be
N+3	data		turned off (to turn off bit 0, data
N+4	A7		is FE) Output new control
N+5	03		word

Program 3-V. (When you know the state you want the relays in, the output is simple)

Address	Contents	Mnemonics	Description
N	86	LDA A	Load on and off bit pattern into
N+1	XX	data	Accumulator A
N+2	A7	STA A	output to relay control
N+3	03	address	channel

3-9. HARDWARE APPLICATIONS

The 680b-PCI board can be used in almost any instance in which the computer must control large amounts of power. The relays can directly control up to 120 watts, and with external contacters and solenoids added, the amount of power that can be controlled is essentially unlimited. Contained in the following paragraphs are a list of possible applications and detailed descriptions of two specific applications.

> NOTE
>
> Before actually beginning a project, it may be necessary to review the Hardware Set-Up procedure, paragraphs 3-2 through 3-6.

3-10. Applications Ideas

The applications listed below are just a few of the many areas in which the 680b-PCI may be utilized. Hopefully, these applications will stimulate new ideas; and any interesting concepts developed by users will be welcomed in the MITS Technical Publications Department. Original and imaginative ideas will be published in Computer Notes or as an "Application Note."

1. Household:

Input	Output
a. thermostats	e. heater/cooler
b. alarm sensors	f. alarms
c. clock	g. coffee
d. manual switches, remote control transducers	h. stereo

2. Ham Radio:

Input	Output
a. signal strength comparator	c. antenna rotater
b. end of tape sensor	d. recording equipment
	e. power switch for transmitters

3. Test Control:

Input	Output
a. thermostats	d. heaters/coolers
b. remote logic input	e. power supplies
c. comparators	f. load switching

4. Agriculture:

Input	Output
a. flow meters	f. pumps
b. pressure sensors	g. solenoid valves
c. automatic material weighing	h. conveyor motors
d. position switches	i. hopper control
e. thermostats	j. distribution control

5. Chemical Process Control:

Input	Output
a. ph meters	e. agitator motors
b. thermostats	f. pumps
c. viscosity testers	g. valves (solenoid)
d. flow meters	h. hopper control
	i. heaters

6. Industrial Process Control:

Input	Output
a. strain gauges	g. tool motor power
b. limit switches	h. tool position motors
c. pressure transducer	i. valves (solenoid)
d. thermostats	j. heaters
e. position sensor	k. rejector solenoid
f. miscellaneous tester outputs	l. solenoid operated stampers

3-11. Specific Application Descriptions

The following paragraphs describe two specific applications (lawn sprinkler control and solar tracking) in detail.

A. Lawn Sprinkler Control

There are several factors to be considered with this application. Naturally, the most important is the amount of moisture in the ground. Moisture can be measured by installing a humidistat in the lawn. Another consideration is the amount of water absorption compared to the level of evaporation. This data will help determine the most effective time to do the watering. A measurement of wind speed may be used as a simple parameter for this purpose. An elementary "go/no-go" device can be set up which will inhibit watering if wind speed exceeds a set limit.

Temperature and relative humidity also have an effect on evaporation. These two parameters may be sensed directly. However, in any given 24-hour period, optimum temperature and humidity usually occur at night. With this in mind, a photo cell may be implemented to tell the computer whether it is day or night.

When the lawn is too dry to wait for optimum watering conditions, a more complex humidistat or a second humidistat with a different setting may be installed to signal this condition.

If it is necessary to water different areas of the lawn separately, additional humidistats and solenoid valves may be installed in each area.

If your city charges premium water prices during heavy usage hours, an input from a clock can tell the computer when the lower rates are in effect.

If there is an irrigation system as well as a normal water system in your area, a float switch may be installed in the irrigation ditch. This will enable the computer to sense the presence of water. The irrigation water can then be pumped from the ditch to water the lawn.

B. Solar Tracking

In recent years the use of solar tracking mechanisms has become well-recognized for such uses as solar boilers for heating, solar boilers (fed to small turbines) for electrical generation, solar cooking ovens and many scientific uses.

Several questions to consider when designing a solar tracker control system are:

1) How will the tracker know if it is on target?
2) If it is not on target, how will it know which way to go?
3) How will it know how far to go?
4) Will it search endlessly at night, or will it track the moon?

One means of resolving these problems is to construct a solar collector and solar sensor in a common chassis with parallel center focal axes, as shown in Figure 3-11.

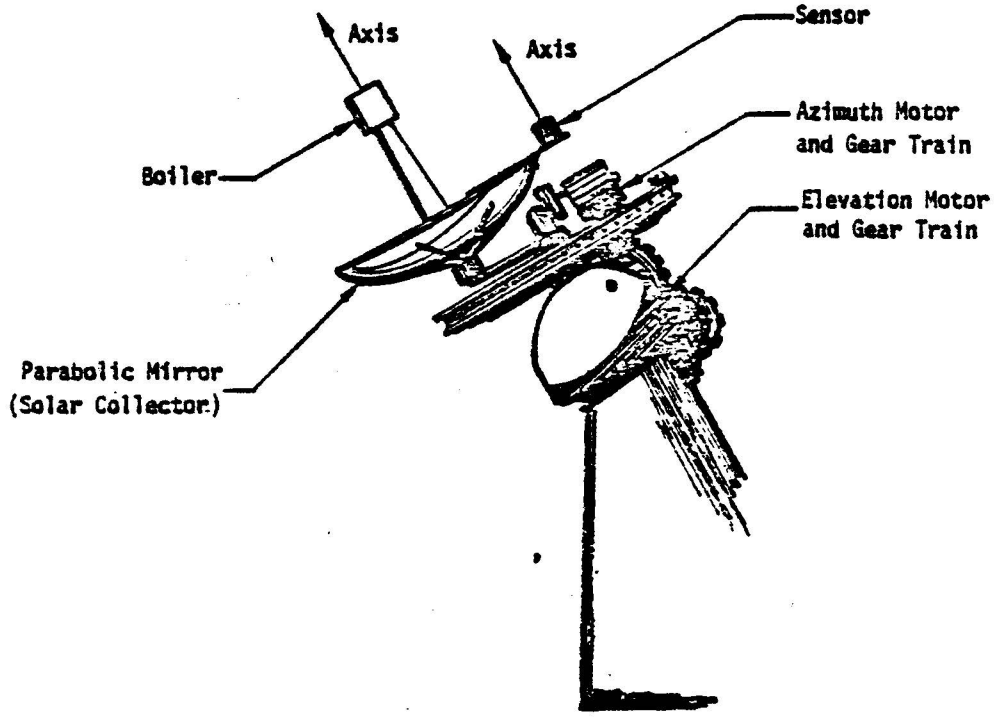


Figure 3-11. Solar Collector and Sensor

Refer to Figure 3-12. The sensor is aligned so that it can detect an offset in rotation. Thus, when the sun is not on the sensor's focal axis, light will fall on one of the photo transistors. The geometry of the sensor can be adjusted for the degree of tracking accuracy desired. Two sensors are required; one for the elevation axis and one for the azimuth. Infrared type photo transistors should be used since they are the most discrimating, i.e. they will not track the moon, clouds, etc.

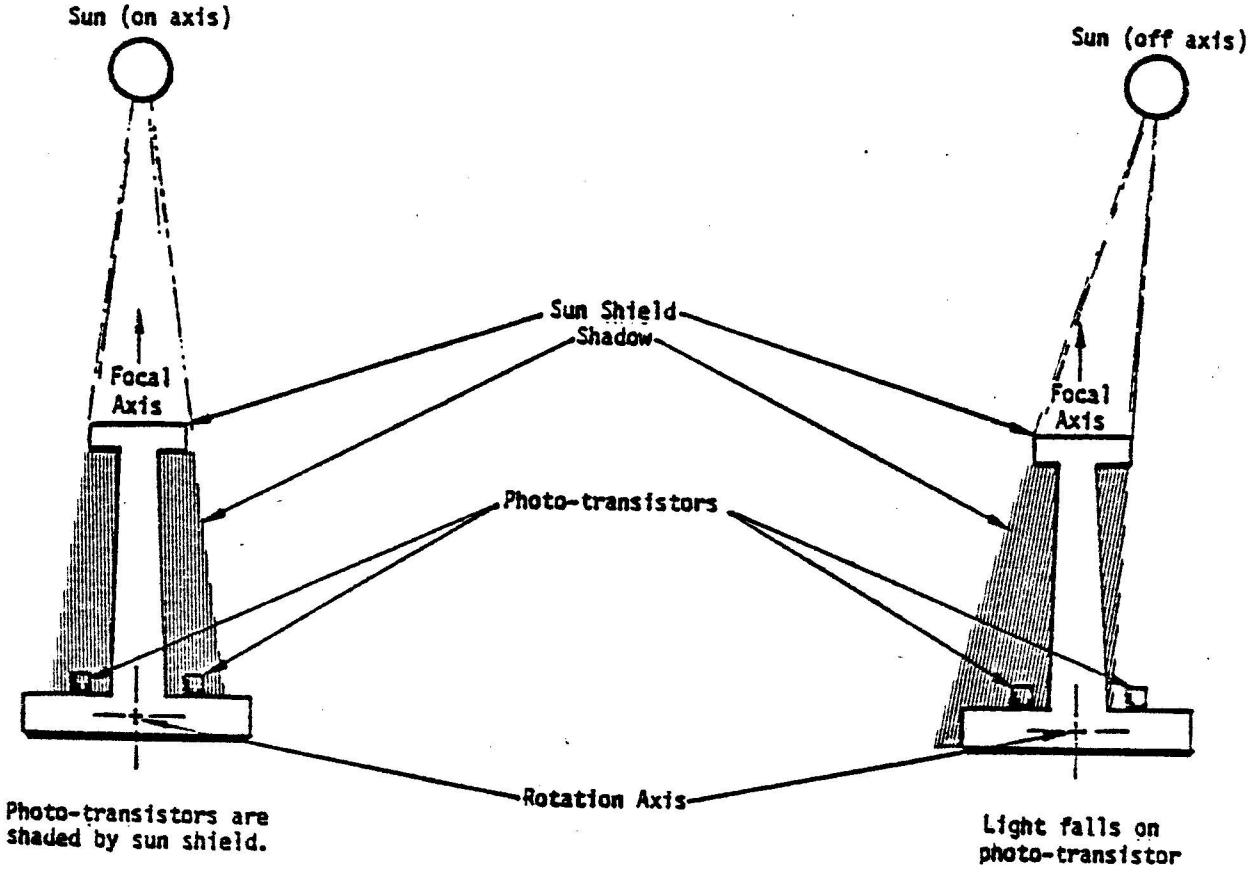


Figure 3-12. Solar Sensor Diagram

The circuit shown in Figure 3-13 can be used to connect the sensors to the 680b-PCI. Four such circuits should be used to provide the four inputs to the board (above, below, right and left). All are LOW active at the PIA. The software should scan the inputs periodically and adjust the position until all the signals are extinguished. The adjustment may use four relay outputs; two for the elevation motor (up, down) and two for the azimuth motor (right, left).

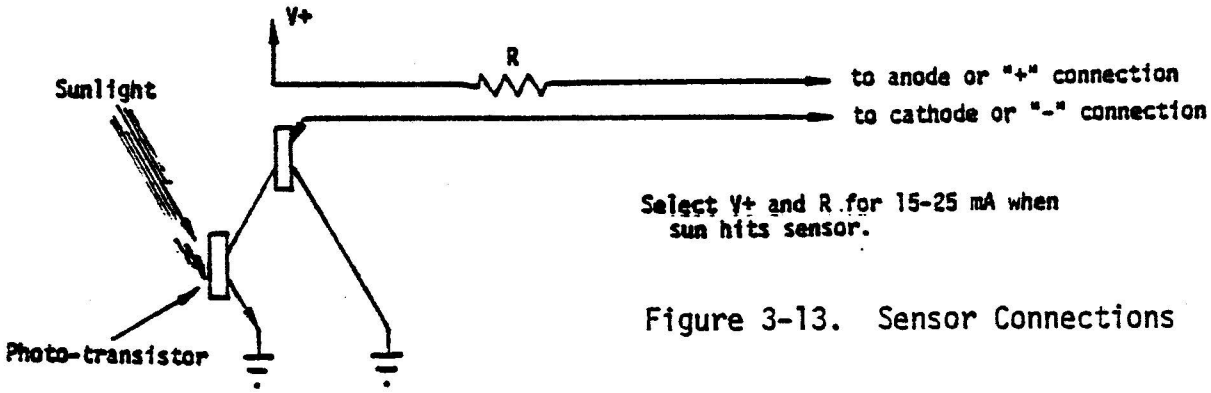


Figure 3-13. Sensor Connections

A general sun sensor which measures the amount of sunlight is another possible input. This sensor enables the computer to sense whether or not there is sufficient light to track. The sensor can also be used to signal the computer during damaging weather conditions (wind, hail, etc., since the sky is usually dark). In this case, the computer will cause the elevation motor to turn the collector face down. The sensor should be placed where it can sense the sun at any time of day.

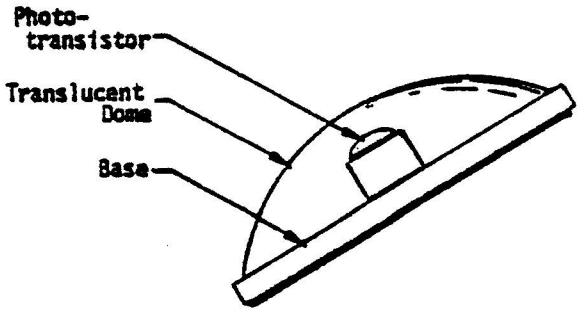


Figure 3-14. General Sun Sensor

680b PCI
SECTION IV
TROUBLESHOOTING

4-1. INTRODUCTION

Section IV is designed to aid the user in pinpointing trouble areas and correcting any problems that may be encountered with the 680b-Process Control Interface board. Contained in this section are: a preliminary check to make sure the board is properly assembled, a power supply check (Table 4-A), an Address Decoding Circuit and RESET check (Table 4-B), a Relay Output check (Table 4-C) along with a test program, and an Opto-Isolator check (Table 4-D).

These troubleshooting procedures are intended only as a guide. They contain basic instructions that should help in locating and correcting most malfunctions. However, if the problem(s) encountered cannot be rectified, send the board to the MITS Repair Department or your local Altair dealer.

Before beginning these troubleshooting procedures, it will be helpful to have a clear understanding of the board's operation; refer to the Theory of Operation section, paragraphs 2-3 through 2-8.

4-2. PRELIMINARY CHECK

The first step in troubleshooting is to carefully examine the board for solder shorts, open lands, or misplaced components. Each 680b-PCI board is carefully assembled and tested at the MITS factory, and problems of this kind should not occur. However, to avoid long hours of troubleshooting, a preliminary check should always be made since improper handling can cause broken leads, lost parts or foreign articles to be lodged on the board.

4-3. POWER SUPPLY VOLTAGE CHECK

The next step in troubleshooting is the power supply voltage check. A defective power supply can cause problems on every part of the board. Refer to Table 4-A for proper voltages. If the voltages check out but the board is still inoperative, double check your program. If the program is correct, proceed to Table 4-B. If only one or two inputs or outputs appear to be defective, refer to the Relay Test Program on page 65 and Table 4-C for outputs and to Table 4-D for inputs.

Table 4-A
Power Supply Voltage Check

Step	Instructions	If Correct	If Incorrect
1	Check the output pin (far right pin) of the Voltage Regulator.	It should read +5v. Proceed to Step 3.	If +5v is not read, proceed to Step 2.
2	Check the input pin (far left pin) of the Voltage Regulator.	It should read +9v unreg. If so, replace the Voltage Regulator.	Possible problem on the 680b Main Board. Refer to the 680b Manual, Section II, page 7.
3	Check the Vcc pins on each of the ICs (pin 14 of the 14-pin ICs) for proper voltages.	If correct, proceed to Table 4-B.	If incorrect, check the Vcc line for opens and correct as necessary.

4-4. ADDRESS DECODING AND RESET CHECK

The 680b-PCI board must have a unique address. When this address is on the bus, the board must be able to distinguish it from any other. If this distinction is not made, problems will occur. Table 4-B will aid in locating and correcting these problems.

Table 4-B

Address Decoding Circuit and RESET Check

Note: This check should be made while the 680b is in the Halt mode. VMA (at pin 1 of IC N) must be tied HIGH with clip leads.

Step	Instructions	If Correct	If Incorrect
1	Check pin 34 of IC W.	It should be HIGH. If correct, proceed to Step 2.	Check the collector of Q11. It should be LOW. If LOW, replace Q12. If HIGH, Q11 is probably defective and should be replaced. Proceed to Step 2.
2	Assuming the board is addressed at F010 (SW1 switches are positioned as follows: $\overline{A7}$, $\overline{A6}$, $\overline{A5}$ and A4), and the address switches are positioned accordingly, check the CSØ line (pin 22 of IC W).	It should be HIGH. If correct, proceed to Step 6.	Check pins 12 and 11 of NOR gate N. If they are LOW, replace IC N. If pin 12 is HIGH, proceed to Step 3. If pin 11 is HIGH, proceed to Step 4.
3	Check the input pins of IC V.	All the input pins of IC V must be HIGH to produce the desired LOW at output pin 8. If all input pins are HIGH, replace IC V.	Address lines A15 through A12 are tied to pins 2, 1, 4 and 3, respectively. If one pin is LOW, the problem may be in the bus. Address lines A11 through A8 are tied to input pins 12, 11, 5 and 6, respectively, through inverter S. If one of these input pins is LOW, the problem may be a defective S inverter or a corresponding address line on the bus.

Table 4-B, continued.

Step	Instructions	If Correct	If Incorrect
4	Check the input pins of IC P.	If the address is selected properly, all the inputs of IC P should be HIGH. If all the inputs are HIGH and the output is HIGH also, IC P should be replaced.	If pin 1 of IC P is LOW, one of the inverters is defective or VMA was not tied HIGH. If one or more of pins 12, 11, 5 or 6 are LOW, check the position of SW1. If the board is addressed at F010, address line A7 on the bus is LOW. Pin 8 of IC U should be HIGH (if not, replace IC U). The operation of A6 and A5 is the same as A7. Since SW1 is selected for F010 and is positioned in the A4 side of the switch, pin 6 of IC P should be HIGH. If it is LOW, check pin 6 of IC U. If it is LOW, replace IC R. If pin 6 is HIGH, IC U is probably defective and should be replaced.
5	Check pins 4 and 2 of IC P.	Both pins should be HIGH. Proceed to Step 6.	If pins 4 or 2 are LOW, check the switch setting. If correct, replace IC P.
6	While toggling address switch A1, check pin 35 of the 6820.	Pin 35 should be HIGH when the A1 switch is in the up position, and LOW when A1 is in the down position. If correct, proceed to Step 7.	If pin 35 does not change, IC T is probably defective and should be replaced.
7	While toggling address switch AØ, check pin 36 of the 6820.	Pin 36 should be LOW when the AØ switch is in the up position, and HIGH when AØ is in the down position. If correct, proceed to Step 8.	If pin 35 does not change, IC T is probably defective and should be replaced.

Table 4-B, continued.

Step	Instructions	If Correct	If Incorrect
8	While actuating the DEPOSIT switch, check pin 21 of the 6820.	A LOW going pulse approximately 2.5 msec. wide should be produced. If so, proceed to Table 4-C.	If there is no pulse, IC T may be defective and should be replaced.

4-5. RELAY OUTPUT CHECK

To test the relay outputs, enter the following program using the System Monitor's M and N command. The A Section Data lines of the 6820 are used as inputs; the B Section Data lines are used as outputs. The program will energize the relays. When the relays close, a click will be heard, followed by a short pause and another click when the relays open. Also, an ohmmeter should be tied across each relay contact on the P2 connector. The meter will deflect as the contacts open and close. If the meter fails to deflect, proceed to Table 4-C.

Program 4-I. Relay Output Test Program

```
.M 0000 CE
.N 0001 F0  Set address F010 in Index Register
.N 0002 10
.N 0003 4F  Clear Accumulator A
.N 0004 A7  Access DDR of
.N 0005 00  Section A
.N 0006 A7  Store all zeros
.N 0007 01  in Section A DDR, Section A = input
.N 0008 A7
.N 0009 02  Access DDR of Section B
.N 000A 43  Complement ACC.A
.N 000B A7  Store all ones in B Section
.N 000C 03  for outputs
.N 000D 86
.N 000E 04  Access Data Channel
.N 000F A7  Register of Section B
.N 0010 02
.N 0011 4F  Clear ACC.A
.N 0012 43  Compt. ACC.A
.N 0013 B7  Store All
.N 0014 F0  ones at output channel
.N 0015 13  of Section B (energize relays)
.N 0016 8D  Branch to Subroutine
.N 0017 09  at location 0021
.N 0018 4F  Store all zeros at
.N 0019 B7  output channel of Section B
.N 001A F0  to deenergize
```

(continued)

Program 4-I, continued.

```
.N 001B 13  Relays
.N 001C 8D  Branch to Subroutine
.N 001D 03  at location 0021
.N 001E 7E  JMP to
.N 001F 00  location
.N 0020 11  0011
.N 0021 FE
.N 0022 FF
.N 0023 FF
.N 0024 09
.N 0025 26  Subroutine
.N 0026 FD  for time
.N 0027 39  delay
```

Table 4-C

Relay Output Check

Note: If the contacts did not cause the ohmmeter to deflect, proceed with the following table while continuing to run the program.			
Step	Instructions	If Correct	If Incorrect
1	Check the collector of the transistor associated with the inoperative relay.	The collector of the transistor should measure approximately +9v when the transistor is off (relay de-energized) and 0v when the transistor is on (relay energized). If correct, the relay may be defective or a bad connection may exist.	If correct, proceed to Step 2.
2	Check the base of the transistor.	A signal from approximately 0v to +2v should be seen. If the reading is correct, the transistor is probably defective and should be replaced.	If correct, the PIA may be defective and should be replaced.

4-6. 6820 INPUT CHECK

To test the 6820's input lines and control lines, refer to Table 4-D.

Table 4-D

Opto-Isolator Check

Step	Instructions	If Correct	If Incorrect
1	Tie the cathode pin of the diode to ground of the defective data line. While tying the connector side of the associated resistor (R23-R30) of the input line to +5v, check pin 5 of the opto-isolator. (This is assuming that R23-R30 are 180 ohm 1/2W resistors, and the signal applied is Vcc.)	Signal is normally HIGH until Vcc is applied at the input resistor. It will then go LOW.	The opto-isolator is probably defective and should be replaced. If the problem still exists, proceed to Step 2.
2	Check pin 1 of the opto-isolator while tying the connector side of the input resistor to +5v.	It should read approximately +2v.	If +5v is read, the line associated with the diode is probably defective
3	Since the CA1-CB1 control lines are identical to the PA data input lines, use steps 1 and 2 (above) to check both lines with their associated components.		
4	If there is a suspected problem with the CA2 or CB2 control lines, check the jumper for active HIGH or LOW signals. If R41 and R5 are used, the collector of the associated opto-isolator transistor is the signal line (pin 5). If R42 and R6 are	CA2 and its associated components are used in this troubleshooting step. This same step also applies to CB2. If R41 is jumpered for an active HIGH signal (JA tied to JB), the signal at pin 22 of connector P2 should be LOW.	If the signal is HIGH, the photo transistor is not conducting. Proceed to Step 5.

Table 4-D, continued.

Step	Instructions	If Correct	If Incorrect
	used instead of R41 and R5, the signal line is the emitter of the opto-isolators (pin 4). Tie pin 3 or pin 9 of IC X HIGH, depending on which control is defective.		
5	Check pin 2 of the IL-74(L).	It should read approximately +3.8v. If the reading is correct, the opto-isolator is probably defective and should be replaced.	If the reading is incorrect, proceed to Step 6.
6	Check the base of Q10.	It should read approximately 0v. If the reading is correct, Q10 is probably defective and should be replaced.	Proceed to Step 7.
7	Check pin 8 of IC X.	If LOW, the 6820 CA2 control line is not operating properly and the 6820 should be replaced.	If pin 9 is HIGH, IC X is defective and should be replaced.

680b PCI
SECTION V
ASSEMBLY

5-1. INTRODUCTION

Section V contains complete step-by-step instructions for component installation and mounting of the 680b-PCI board. Two organizational aids are provided throughout the instructions: 1) Boxed off parts identification lists to check off each component as it is installed and 2) reproductions of the board's silkscreen showing previously installed components, components being installed and components yet to be installed (see Figure 5-1).

Before beginning the assembly procedure, carefully read the enclosed "MITS Kits Assembly Hints" booklet. It contains helpful suggestions and several important warnings. Failure to heed these warnings could cause you to void your warranty.

Check the contents of your kit against the parts list (Appendix A) to make sure you have all the required parts. As you construct the board, read each step carefully and follow the instructions in the order in which they are presented. Always complete each step before going on to the next.

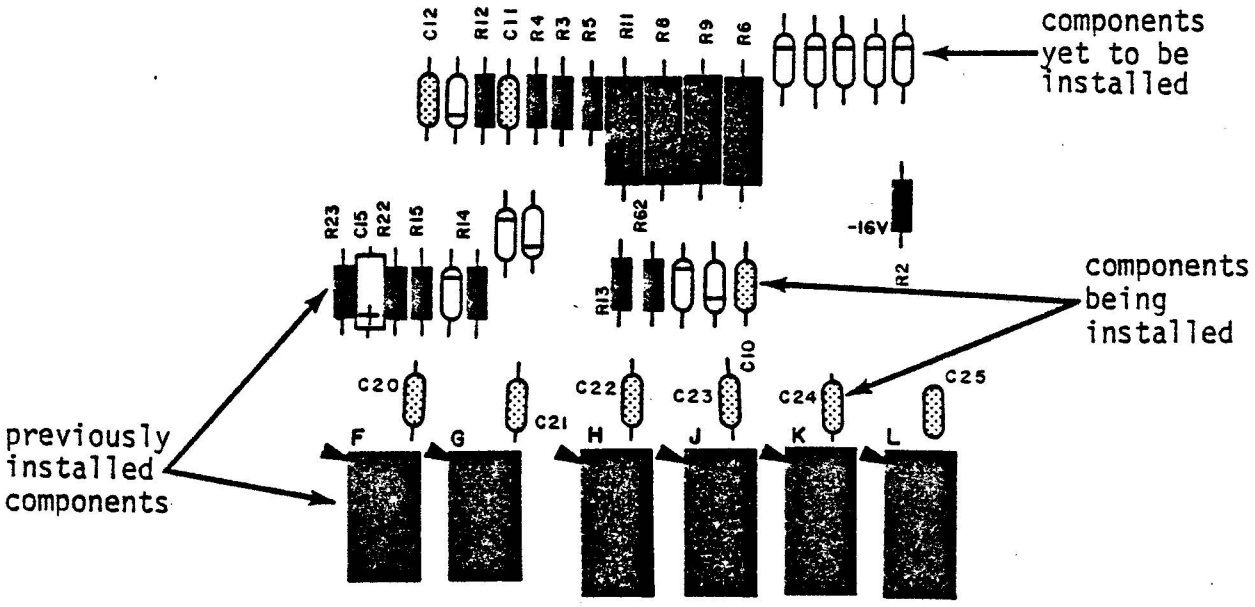
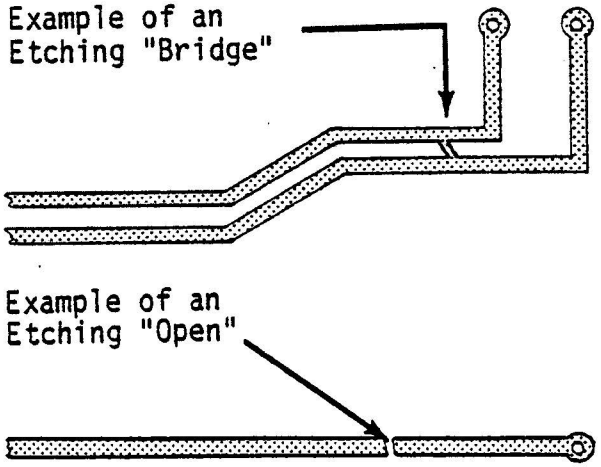


Figure 5-1. Typical Silkscreen

5-2. VISUAL INSPECTION

It is recommended that a visual inspection of the PC Board(s) in your kit be made before beginning the assembly procedures.

Look for etching "bridges" or etching "opens" in the printed circuit lands, as shown in the drawings below:



This could also appear as a "hairline" cut.

A thorough visual inspection will eliminate one possibility for errors, should the board not operate properly after it is assembled. Troubleshooting efforts may then be concentrated elsewhere.

5-3. COMPONENT INSTALLATION INSTRUCTIONS

Pages 77 through 83 describe the proper procedures for installing various types of components in your kit.

Read these instructions over very carefully and refer back to them whenever necessary. Failure to properly install components may cause permanent damage to the component or the rest of the unit; it will definitely void your warranty.

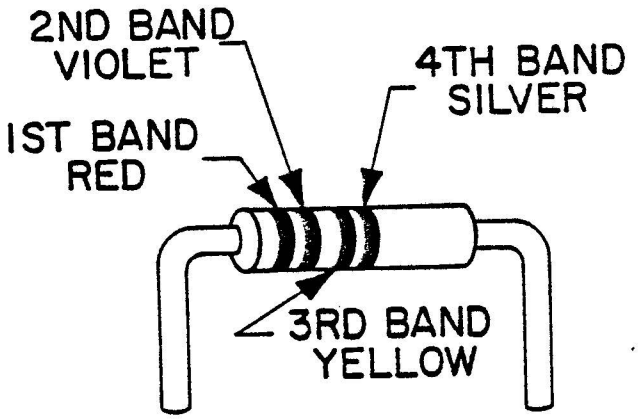
More specific instructions, or procedures of a less general nature, will be included within the assembly text itself.

Under no circumstances should you proceed with an assembly step without fully understanding the procedures involved. A little patience at this stage will save a great deal of time and potential "headaches" later.

5-4. Resistor Installation

Resistors have four (or possibly five) color-coded bands as represented in the chart below. The fourth band is gold or silver and indicates the tolerance. NOTE: In assembling a MITS kit, you need only be concerned with the three bands of color to the one side of the gold or silver (tolerance) band. These three bands denote the resistor's value in ohms. The first two bands correspond to the first two digits of the resistor's value and the third band represents a multiplier.

For example: a resistor with red, violet, yellow and silver bands has a value of 270,000 ohms and a tolerance of 10%. By looking at the chart below, you see that red is 2 and violet 7. By multiplying 27 by the yellow multiplier band (10,000), you find you have a 270,000 ohm (270K) resistor. The silver band denotes the 10% tolerance. Use this process to choose the correct resistor called for in the manual.



RESISTOR COLOR CODES		
COLOR	BANDS 1&2	3rd BAND (Multiplier)
Black	0	1
Brown	1	10^2
Red	2	10^3
Orange	3	10^4
Yellow	4	10^5
Green	5	10^6
Blue	6	10^7
Violet	7	10^8
Gray	8	10^9
White	9	

Use the following procedure to install the resistors onto the boards. Make sure the colored bands on each resistor match the colors called for in the list of Resistor Values and Color Codes given in the assembly instructions.

1. Using needle-nose pliers, bend the leads of the resistor at right angles to match their respective holes on the PC board.

2. Install the resistor into the correct holes on the silk-screened side of the PC board.

3. Holding the resistor in place with one hand, turn the board over and bend the two leads slightly outward.

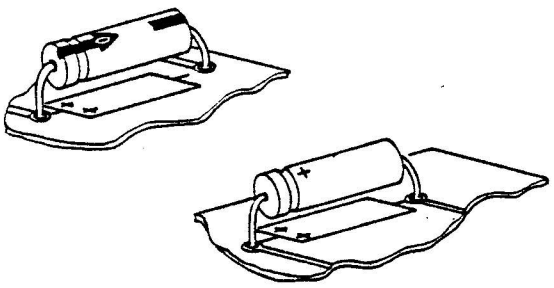
4. Solder the leads to the foil pattern on the back side of the board; then clip off any excess lead lengths.

5-5. Capacitor Installation Instructions

A. Electrolytic Capacitors

Polarity must be noted on electrolytic capacitors before they are installed.

The electrolytic capacitors contained in your kit may have one or possibly two of three types of polarity markings. To determine the correct orientation, look for the following.



ELECTROLYTIC CAPACITOR

One type will have plus (+) signs on the positive end; another will have a band or a groove around the positive side in addition to the plus signs. The third type will have an arrow on it; in the tip of the arrow there will be a negative (-) sign. The capacitor must be oriented so the arrow points to the negative side.

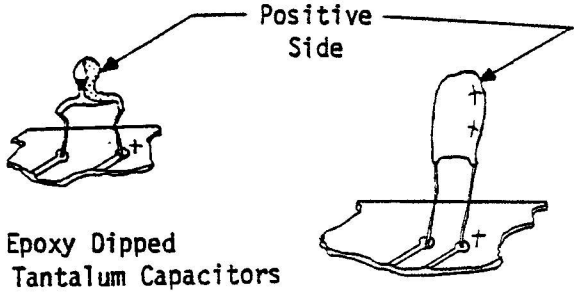
Install the electrolytic capacitors using the following procedure. Make sure you have the correct capacitor value before installing each one.

1. Bend the two leads of the capacitor at right angles to conform to their respective holes on the board. Insert the capacitor into the holes on the silk-screened side of the board, aligning the positive side with the "+" signs printed on the board.
2. Holding the capacitor in place, turn the board over and bend the two leads slightly outward. Solder the leads to the foil (bottom) side of the board and, clip off any excess lead lengths.

B. Epoxy Dipped Tantalum, Epoxy Dipped Ceramic, and Ceramic Disk Capacitors

Polarity must be noted on epoxy dipped tantalum capacitors before they are installed.

There are two types of epoxy dipped tantalum capacitors contained in you your kit. The first type is blue on the positive side. The second type is marked with "+" signs on the positive side. Both types of epoxy dipped tantalum capacitors are shown in the drawings below.



Epoxy Dipped Tantalum Capacitors

The epoxy dipped ceramic capacitors and the ceramic disk capacitors are non-polarized.

These two types of capacitors are shown in the drawings below.

Epoxy Dipped Ceramic Capacitor

Ceramic Disk Capacitor

Install these 4 types of capacitors using the following procedure. Make sure you have the correct capacitor value before installing each one.

1. Bend the two capacitor leads to conform to their respective holes on the board.
2. Insert the capacitor into the correct holes from the silk-screened side of the board. Holding the capacitor in place, turn the board over and bend the two leads slightly outward.
3. Solder the two leads to the foil (bottom) side of the board and, clip off any excess lead lengths.

5-6. Diode Installation

NOTE: Diodes are marked with a band on one end indicating the cathode end. Each diode must be installed so that the end with the band is oriented towards the band printed on the PC board. Failure to orient the diodes correctly may result in permanent damage to your unit.

DIODE

Use the following procedure to install diodes onto the board. Refer to the list of Diode Part Numbers included for each board to make sure you install the correct diode each time.

1. Bend the leads of the diode at right angles to match their respective holes on the board.

2. Insert the diode into the correct holes on the silk screen, making sure the cathode end is properly oriented. Turn the board over and bend the leads slightly outward.

3. Solder the two leads to the foil pattern on the back side of the board; then clip off any excess lead lengths.

5-7. Transistor Installation

To install transistors, use the following instructions.

NOTE: Always check the part number of each transistor before you install it. (See listing of Transistor Part Numbers for each board.) Some transistors look identical but differ in electrical characteristics, according to part number. If you have received substitute part numbers for the transistors in your kit, check the Transistor Identification Chart which follows these instructions to be sure you make the correct substitutions.

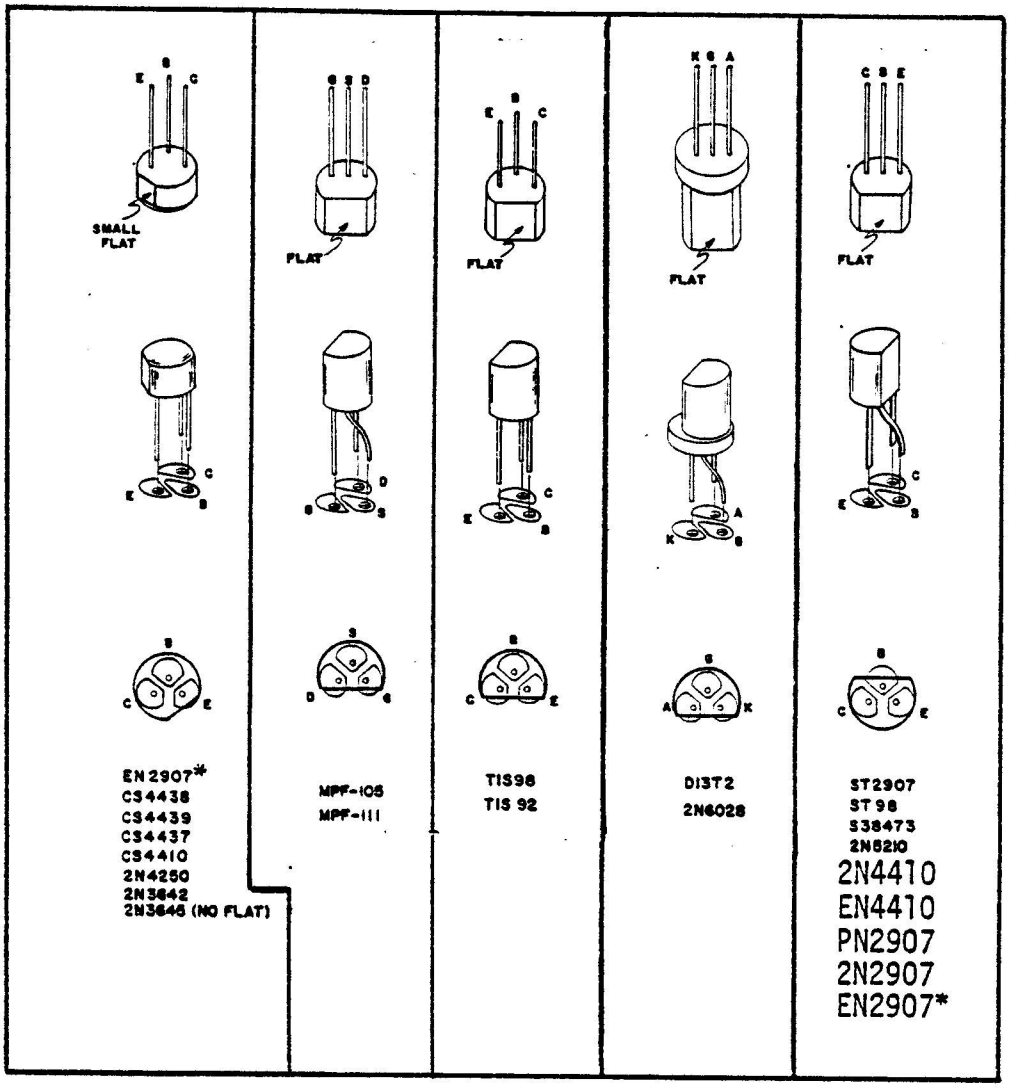
NOTE: Always make sure the transistor is oriented so that the emitter lead is installed in the hole on the PC board labeled with an "E". To determine which lead is the emitter lead, refer to the Transistor Identification Chart.

1. After the correct transistor has been selected and the leads have been properly oriented, insert the transistor into the holes on the silk-screened side of the board.

2. Holding the transistor in place, turn the board over and bend the three leads slightly outward.

3. Solder the leads to the foil pattern on the back side of the board; then clip off any excess lead lenghts.

TRANSISTOR IDENTIFICATION CHART



IN THE ILLUSTRATION ABOVE THE OUTLINE OF EACH TYPE OF TRANSISTOR IS SHOWN OVER THE PADS ON THE CIRCUIT BOARD WITH THE CORRECT DESIGNATION FOR EACH OF THE THREE LEADS. USE THIS INFORMATION TOGETHER WITH THE INFORMATION IN THE ASSEMBLY MANUAL FOR THE CORRECT ORIENTATION OF THE TRANSISTORS AS YOU INSTALL THEM.

THE FOLLOWING IS A LIST OF POSSIBLE SUBSTITUTIONS: IF ANY OTHERS ARE USED YOU WILL RISK DAMAGING YOUR UNIT:

2N4410 = EN4410 = CS4410 = CS4437, CS4438, TIS98, ST98, S38473 (NPN)

EN2907 = 2N2907 = PN2907 = ST2907, CS4439 (PNP)

WHEN MAKING SUBSTITUTIONS, REFER TO THE ILLUSTRATION TO DETERMINE THE CORRECT ORIENTATION FOR THE THREE LEADS.

*Configuration of the leads on EN2907 may vary.

5-8. IC Installation

All ICs must be oriented so that the notched end is toward the end with the arrowhead printed on the PC board. Pin 1 of the IC should correspond with the pad marked with the arrowhead. If the IC does not have a notch on one end, refer to the IC Identification Chart to identify Pin 1.

To prepare ICs for installation:
All ICs are damaged easily and should be handled carefully -- especially static-sensitive MOS ICs. Always try to hold the IC by the ends, touching the pins as little as possible. When you remove the IC from its holder, CAREFULLY straighten any bent pins using needle-nose pliers. All pins should be evenly spaced and should be aligned in a straight line, perpendicular to the body of the IC itself.

A. Installing ICs without sockets:

1. Orient the IC so that Pin 1 coincides with the arrowhead on the PC board.

2. Align the pins on one side of the IC so that just the tips are inserted into the proper holes on the board.

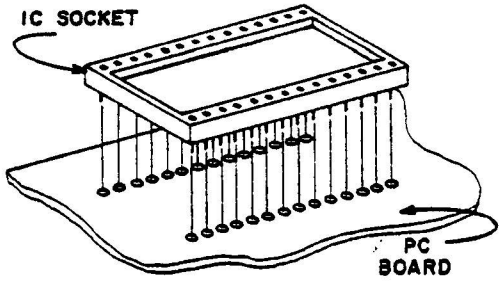
3. Lower the other side of the IC into place. If the pins don't go into their holes right away, rock the IC back, exerting a little inward pressure, and try again. Be patient. The tip of a small screwdriver may be used to help guide the pins into place. When the tips of all the pins have been started into their holes, push the IC into the board the rest of the way. Tape the IC to the board with a piece of masking tape.

4. Turn the board over and solder each pin to the foil pattern on the back side of the board. Be sure to solder each pin and be careful not to leave any solder bridges. Remove the masking tape.

WARNING:
Make sure none of the pins have been pushed underneath the IC during insertion.

B. Installing ICs with sockets:

1. Referring to the drawing below, set the IC socket into the designated holes on the board and secure it with a piece of masking tape.



2. Turn the board over and solder each pin to the foil pattern on the back side of the board. Be sure to solder each pin and be careful not to leave any solder bridges. Remove the masking tape.

3. Orient the IC over the socket so that Pin 1 coincides with the arrowhead on the PC board.

4. Align the pins on one side of the socket so that just the tips are inserted into the holes.

5. Lower the other side of the IC into place. If the pins don't go into their holes right away, rock the IC back, exerting a little inward pressure, and try again. Be patient. When the tips of all the pins have been started into their holes, push the IC into the socket the rest of the way.

MOS IC SPECIAL HANDLING PRECAUTIONS

There are several MOS integrated circuits contained in this kit. These IC's are very sensitive to static electricity and transient voltages. In order to prevent damaging these components, read over the following precautions and adhere to them as closely as possible. FAILURE TO DO SO MAY RESULT IN PERMANENT DAMAGE TO THE IC.

1) All equipment (soldering iron, tools, solder, etc.) should be at the same potential as the PC board, the assembler, the work surface and the IC itself along with its container. This can be accomplished by continuous physical contact with the work surface, the components, and everything else involved in the operation.

2) When handling the IC, develop the habit of first touching the conductive container in which it is stored before touching the IC itself.

3) If the IC has to be moved from one container to another, touch both containers before doing so.

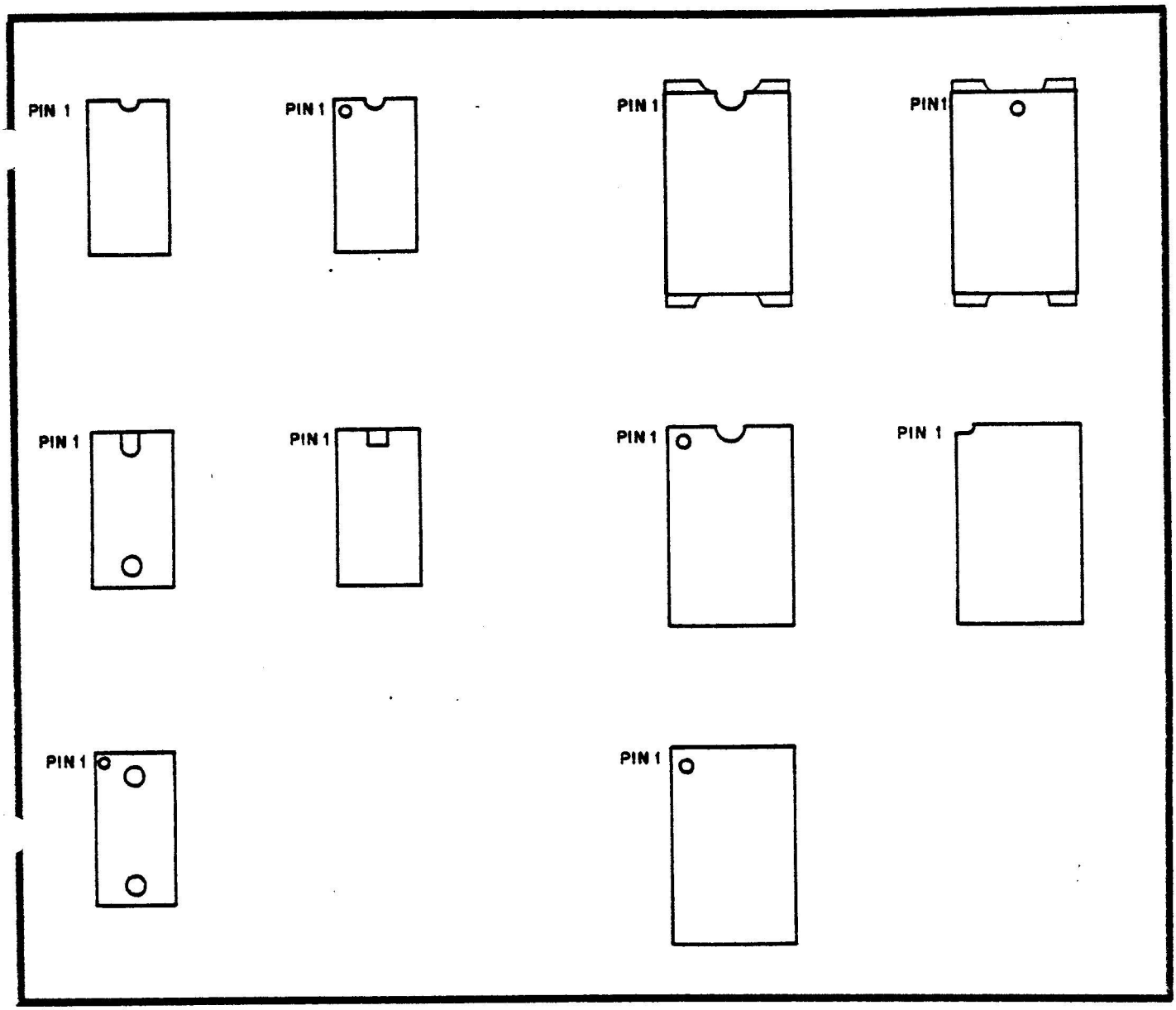
4) Do not wear clothing which will build up static charges. Preferably wear clothing made of cotton rather than wool or synthetic fibers.

5) Always touch the PC board before touching the IC to the board. Try to maintain this contact as much as possible while installing the IC.

6) Handle the IC by the edges. Avoid touching the pins themselves as much as possible.

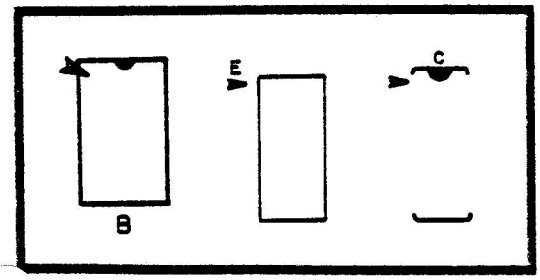
7) Dry air moving over plastic can build up considerable static charges. Avoid placing the IC near any such area or object.

8) In general, never touch anything to the IC that you have not touched first while touching both it and the IC itself.



INTEGRATED CIRCUITS (ICs) CAN COME WITH ANY ONE OF, OR A COMBINATION OF, SEVERAL DIFFERENT MARKINGS. THESE MARKINGS ARE VERY IMPORTANT IN DETERMINING THE CORRECT ORIENTATION FOR THE ICs WHEN THEY ARE PLACED ON THE PRINTED CIRCUIT BOARDS. REFER TO THE ABOVE DRAWING TO LOCATE PIN 1 OF THE ICs, THEN USE THIS INFORMATION IN CONJUNCTION WITH THE INFORMATION BELOW TO PROPERLY ORIENT EACH IC FOR INSTALLATION.

WARNING: INCORRECTLY ORIENTED IC's MAY CAUSE PERMANENT DAMAGE!



THE DRAWING ON THE LEFT INDICATES VARIOUS METHODS USED TO SHOW THE POSITION OF ICs ON THE PRINTED CIRCUIT BOARDS. THESE ARE SILK-SCREENED DIRECTLY ON THE BOARD. THE ARROWHEAD INDICATES THE POSITION FOR PIN 1 WHEN THE IC IS INSTALLED.

5-9. IC Socket and IC Installation

Install the following nine integrated circuits with sockets (Bag 2) according to the IC Installation Instructions, Section B, given on page 81.

Silkscreen Designation	IC Part Number	Socket Size
( ) N	74LS02	14-pin
( ) P, V	74LS30	14-pin
( ) R, S, T, U, X	74LS04	14-pin
( ) W	6820	40-pin

5-10. Opto-Isolator Socket and Opto-Isolator Installation

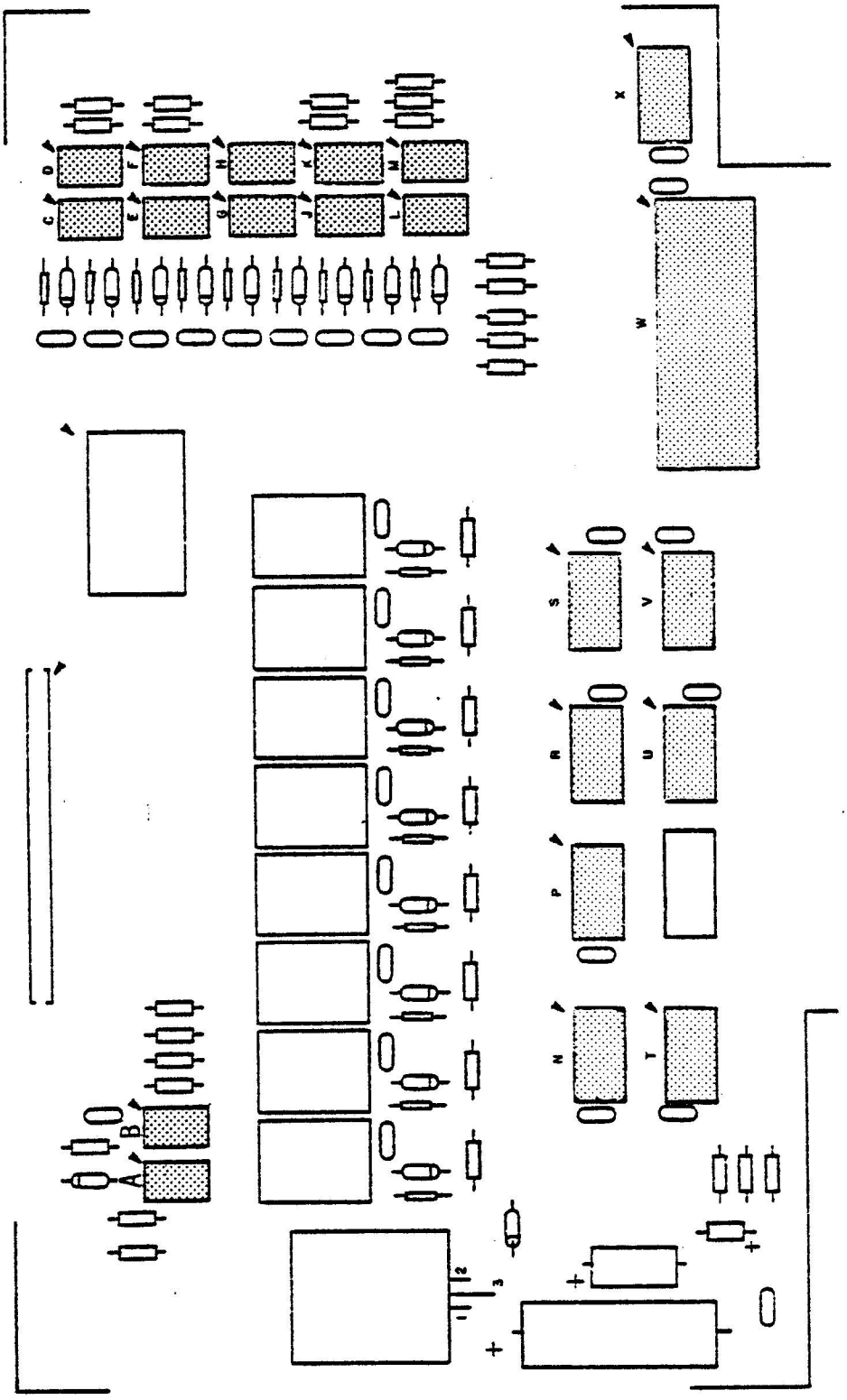
Install opto-isolators A through M with sockets (Bag 2) according to the following instructions.

1. Lower the socket into the designated holes on the silkscreened (top) side of the board and secure in place with a piece of masking tape.

2. Solder each pin to the foil pattern on the back of the board. Do not leave any solder bridges. Remove the tape.

3. Each opto-isolator is marked with a raised circle at pin 1. Orient the opto-isolator over the socket so that pin 1 coincides with the arrowhead shown on the silkscreen (Figure 5-2). Carefully insert one side of the opto-isolator into the socket. Lower the other side into place and push in all the way.

Opto-Isolator	Part Number
( ) A through M	IL-74



5-2. IC and Opto-Isolator Installation

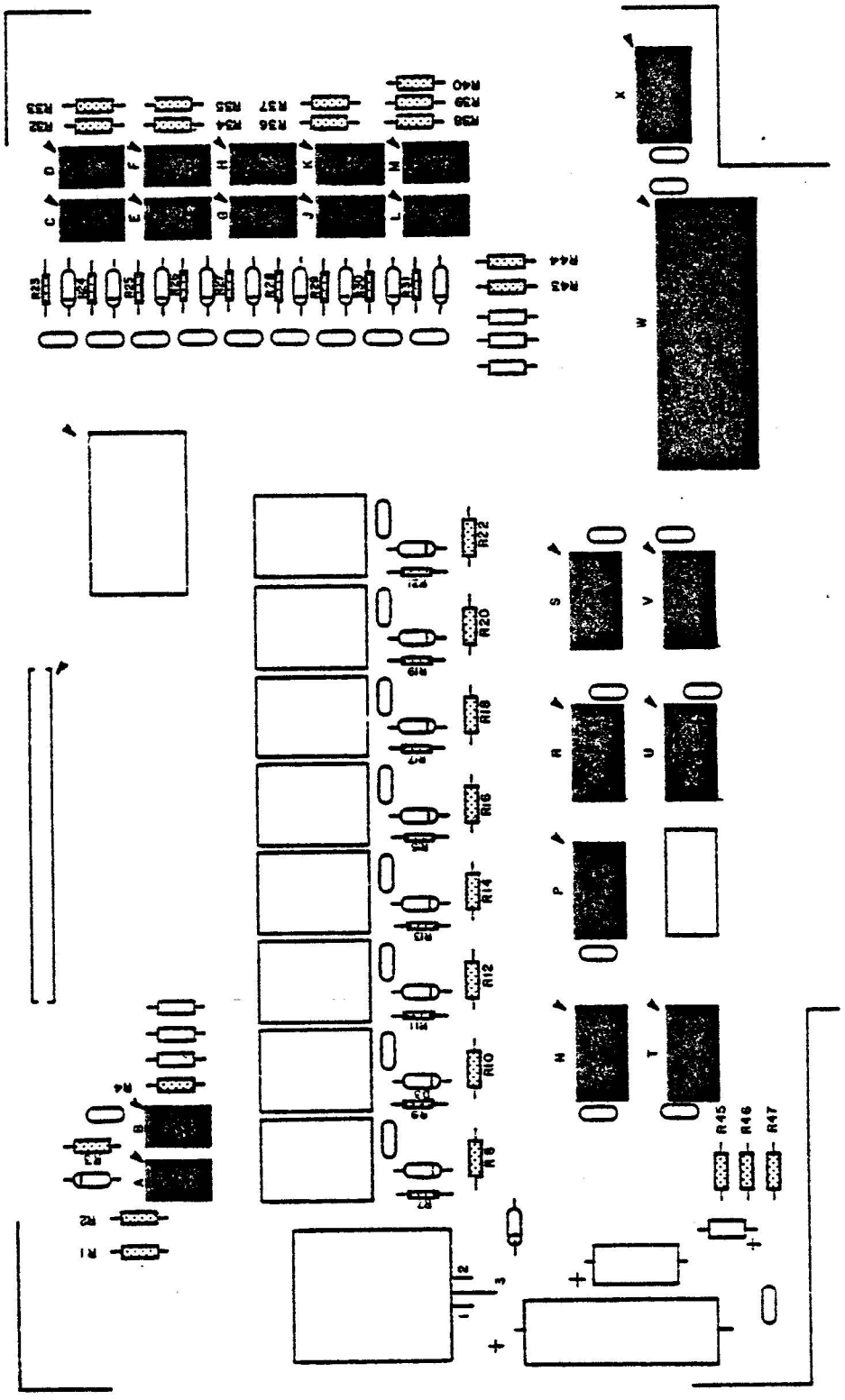
5-11. Resistor Installation

There are 43 MITS-supplied resistors (Bag 4) to be installed on the board, although the silk-screen shows a total of 49. These extra six resistors are optional and should be supplied by the user. Install the resistors according to the Resistor Installation Instructions on page 77.

> NOTE
> Save any excess leads for use in Paragraphs 5-18 and 5-22.

The following chart shows the values and color-codes of the MITS-supplied resistors.

Silkscreen Designation	Value	Color Code
( ) R1, R44	470 ohm	yellow, violet, brown
( ) R2, R43	100 ohm	brown, black, brown
( ) R3, R23, R24, R25, R26, R27, R28, R29, R30, R31	180 ohm	brown, gray, brown
( ) R4, R32, R33, R34, R35, R36, R37, R38, R39, R40	2.2K ohm	red, red, red
( ) R7, R9, R11, R13, R15, R17, R19, R21	33 ohm	orange, orange, black
( ) R8, R10, R12, R14, R16, R18, R20, R22	220 ohm	red, red, brown
( ) R45, R46	10K ohm	brown, black, orange
( ) R47	33K ohm	orange, orange, orange



5-3. Resistor Installation

5-12. Suppressor Capacitor Installation

There are 17 suppressor capacitors (Bag 3) to be installed which are used for noise suppression. They have no individual component designations, but are shown on the silkscreen as small oval shapes. Install all 17 capacitors according to the Ceramic Disk Capacitor Installation Instructions on page 78.

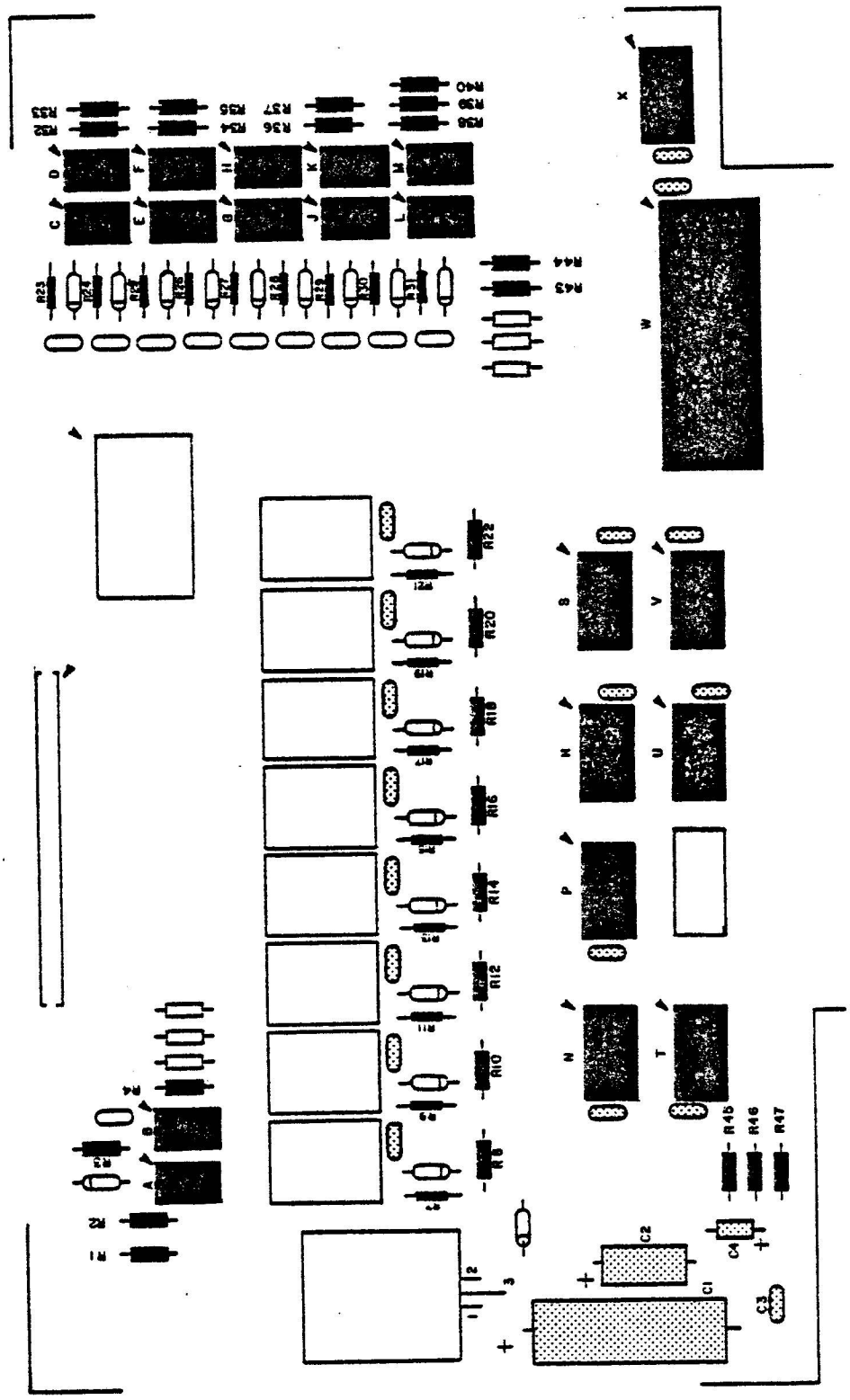
Suppressor Capacitors	Value
( ) 17 suppressor capacitors	.1 µf, 12v or 16v

5-13. Capacitor Installation

There are three types of capacitors to be installed on the 680b-PCI board. C1 and C2 (Bag 3) are electrolytic capacitors and should be installed according to the Capacitor Installation Instructions, Section A, on page 78. C3 (Bag 3) is a ceramic disk capacitor, and C4 (Bag 3) is an epoxy dipped tantalum capacitor. To install C3 and C4, refer to the Capacitor Installation Instructions, Section B, on page 78.

> NOTE
>
> To insure proper polarity C1, C2 and C4 must be oriented as shown in the instructions on page 78. C3 is non-polarized.

Capacitor	Value
( ) C1	500 µf, 25v
( ) C2	33 µf, 16v
( ) C3	.1 µf, 50v
( ) C4	10 µf, 16v



5-4. Suppressor Capacitor and Capacitor Installation

5-14. Transistor Installation

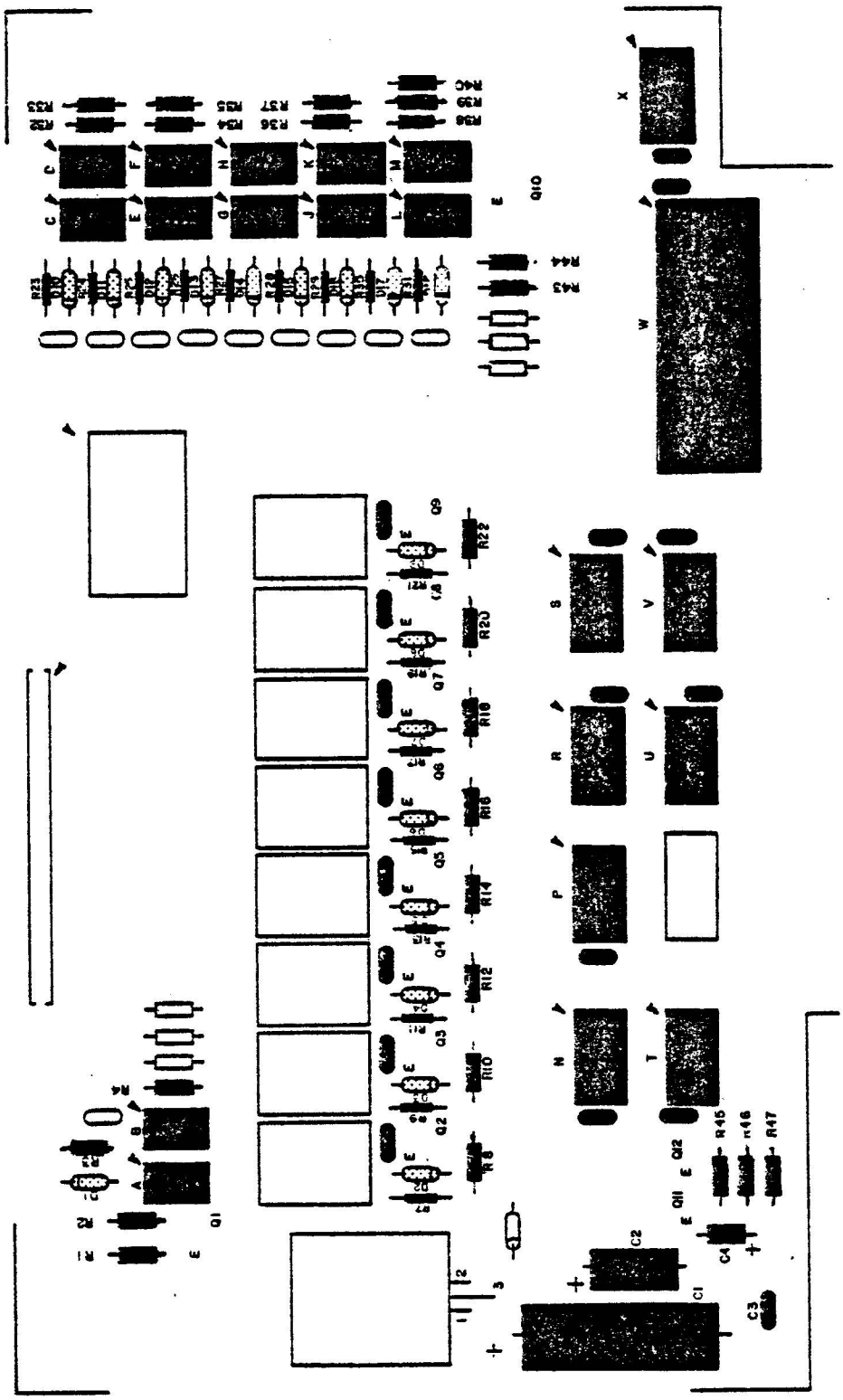
Install transistors Q1 through Q12 (Bag 2) according to the Transistor Installation Instructions on page 79.

Transistor	Part Number
( ) Q1 through Q12	2N4410

5-15. Diode Installation

Install diodes D1 through D18 (Bag 2) according to the Diode Installation Instructions on page 79.

Diode	Part Number
( ) D2 through D9	1N4004
( ) D1, D10 through D18	1N914



5-5. Transistor and Diode Installation

5-16. Voltage Regulator Installation

Install VR1 with heat sink (Bag 1) according to the following instructions.

1. Set the regulator in place on the silkscreened side of the board, aligning the leads with their designated holes.

2. Use needle-nose pliers to bend each of the three leads at a right angle to conform to its proper hole on the board.

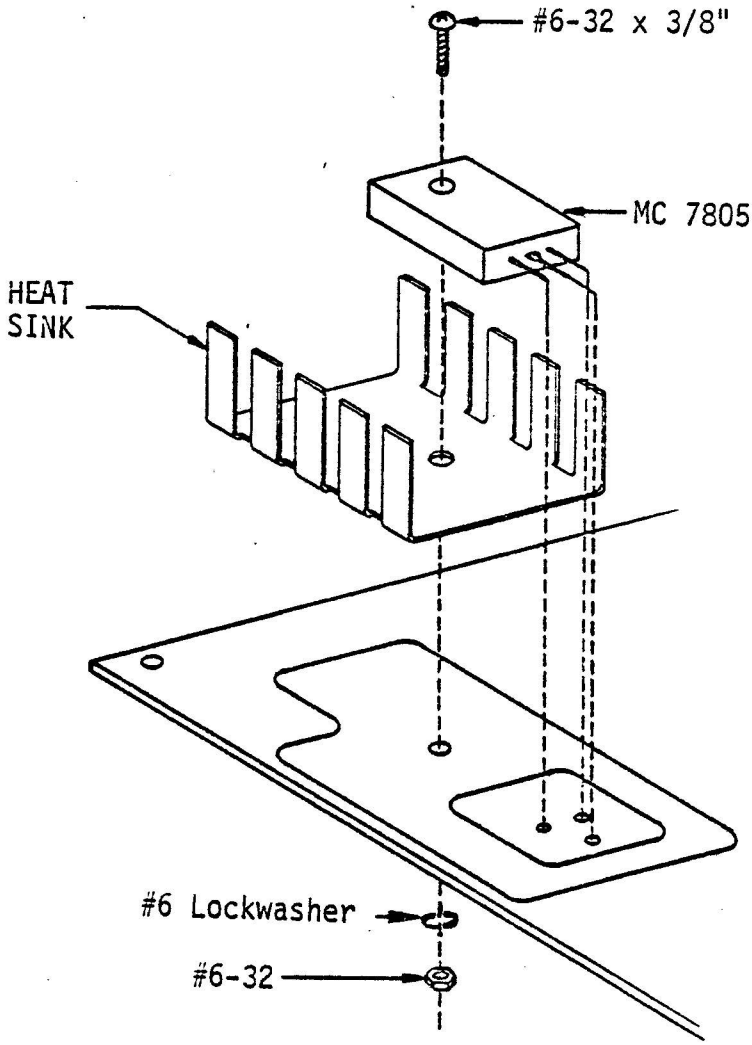
> NOTE
>
> Use heat sink grease when installing this component. Apply the grease to all metal surfaces which come in contact with each other.

3. Referring to Figures 5-6 and 5-7, set the regulator and heat sink in place on the silkscreened side of the board. Secure them in place with a #6-32 x 3/8" screw, a #6-32 nut and a #6 lockwasher.

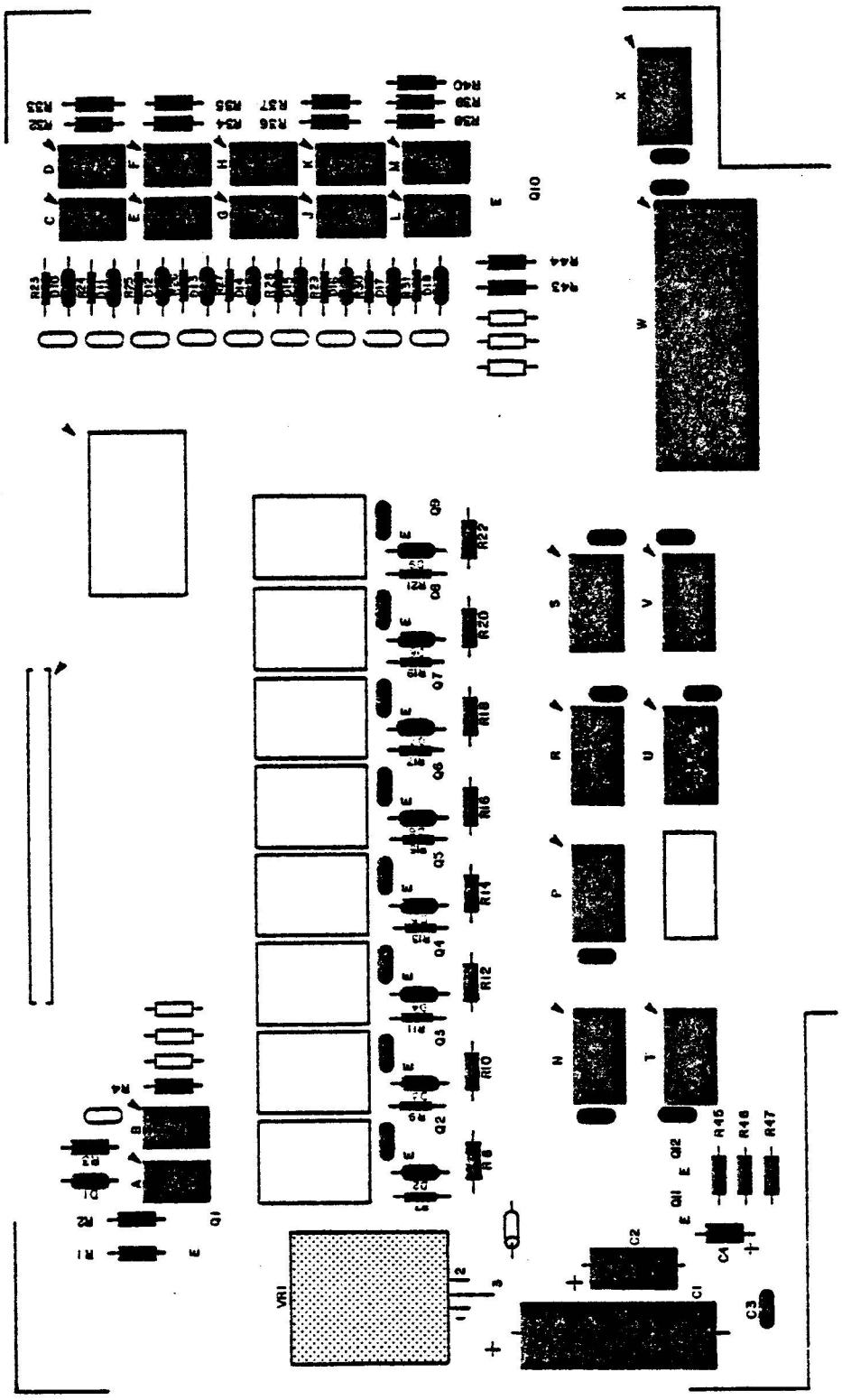
4. Solder the three leads to the foil pattern on the back of the board. Be sure not to leave any solder bridges.

5. Clip off any excess lead lengths.

Voltage Regulator	Part Number
( ) VR1	MC 7805



5-6. Voltage Regulator Orientation



5-7. Voltage Regulator Installation

5-17. Switch Installation

Install the 16-pin dip switch, SW1 (Bag 6), according to the following instructions.

1. Remove SW1 from its holder and straighten any bent pins with needle-nose pliers.

2. Orient the switch so that the numbers 1,2,3,4 line up directly under SW1 as shown in Figure 5-8.

3. Start the pins on one side of the switch into their respective holes on the silkscreened side of the board. Do not push the pins in all the way. If you have difficulty inserting the pins into the holes, guide them with the tip of a small screwdriver.

4. Start the pins on the other side of the switch into their holes in the same manner. When all 16 pins have been started, push the switch into place by gently rocking it back and forth until it rests as close as possible to the board. Secure in place with a piece of masking tape.

5. Solder each pin to the foil pattern on the back of the board. Be careful not to leave any solder bridges and clip off any excess lead lengths.

Switch	Part Number
( ) SW1	206-124

5-18. Ferrite Bead Installation

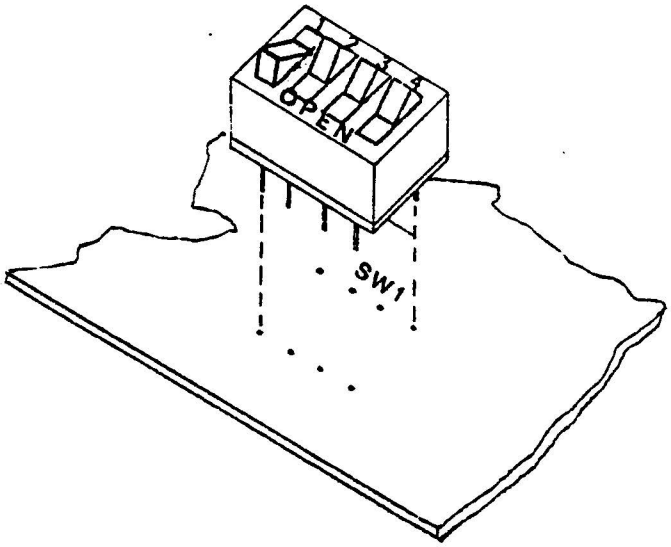
Install one ferrite bead, L1 (Bag 6), on the board according to the following instructions.

1. Using a resistor lead saved from Paragraph 5-11, cut a one-inch lead length.

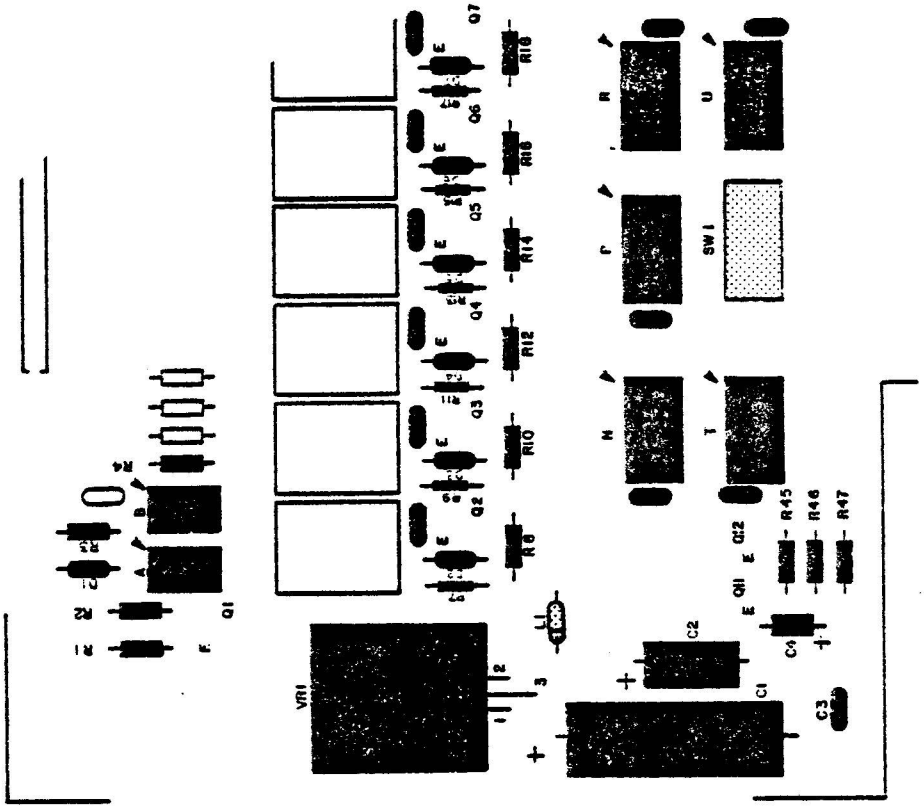
2. Insert the lead through the bead and bend the ends of the lead to conform to the designated holes on the board.

3. Insert the lead into the silkscreened side of the board and solder to the foil pattern on the back of the board. Be sure not to leave any solder bridges and clip off any excess lead lengths.

( ) 1 ferrite bead, L1



5-8. Switch Orientation



5-9. Switch and Ferrite Bead Installation

5-19. Relay Installation

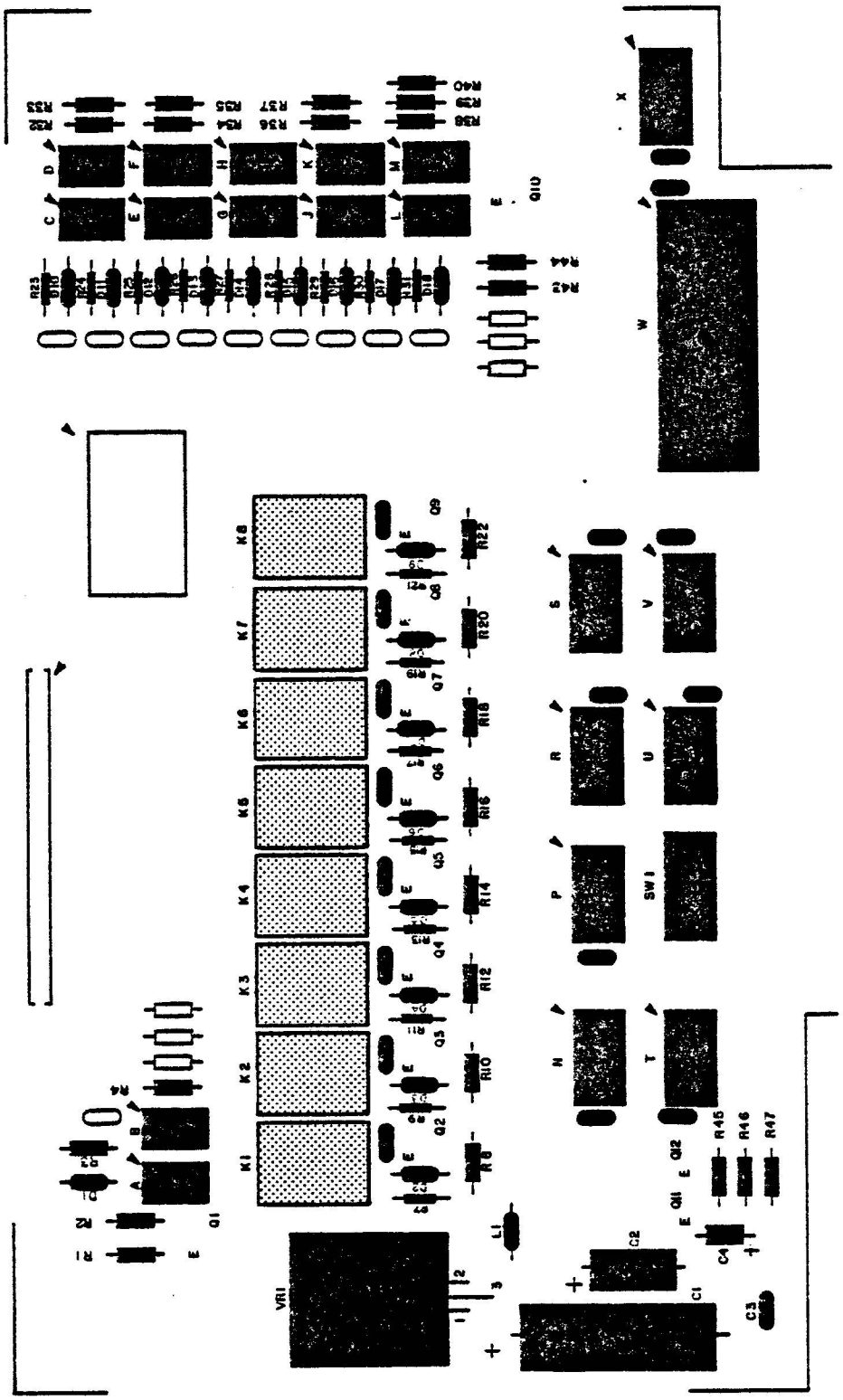
Install relays K1 through K8 (Bag 6) according to the following instructions.

1. Set the relay in place on the silkscreened side of the board, aligning the leads with their designated holes.

2. Use needle-nose pliers to bend each lead at a right angle to conform to its proper hole on the board.

3. Solder the leads to the foil pattern on the back of the board. Be sure not to leave any solder bridges and clip off any excess lead lengths.

Relay	Part Number
( ) K1 through K8	LZ9



5-10. Relay Installation

5-20. Male Connector Installation

Install one 25-pin male connector, P1 (Bag 6), according to the following instructions.

1. With the bent pins pointing toward the bottom of the board, orient the connector so that pin 1 is aligned with the arrow on the silkscreen as shown in Figure 5-11.

2. Insert the short pins into their designated holes on the silkscreened side of the board.

3. Solder each pin to the foil pattern on the back of the board. Be sure not to leave any solder bridges, and clip off any excess lead lengths.

( ) 1 male connector, P1

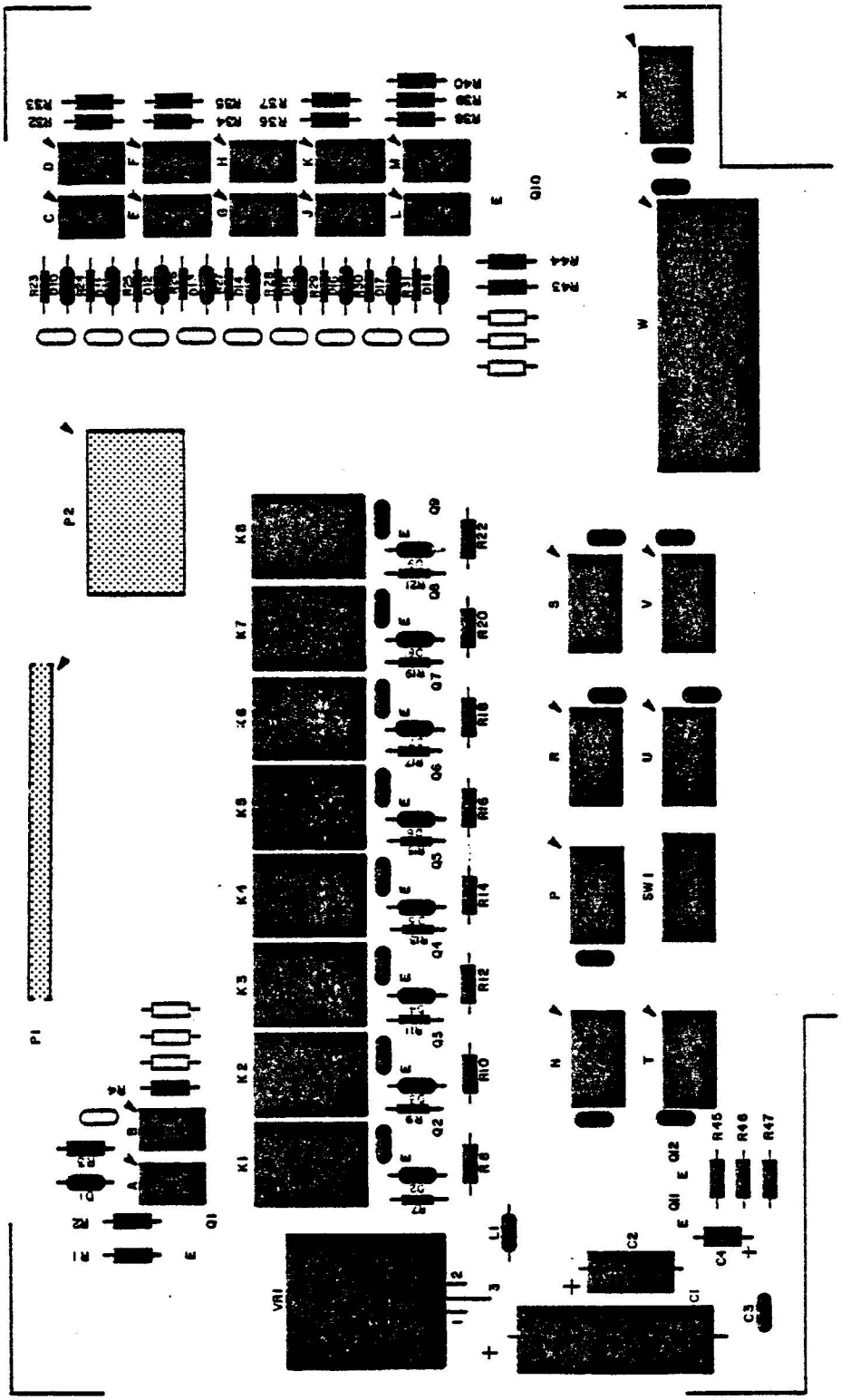
5-21. Female Connector Installation

Install one 24-pin female socket, P2 (Bag 6), according to the following instructions.

1. Insert P2 into the designated holes on the silkscreened side of the board. Secure with a piece of masking tape.

2. Solder each pin to the foil pattern on the back of the board. Be sure not to leave any solder bridges and clip off any excess lead lengths.

( ) 1 female connector, P2

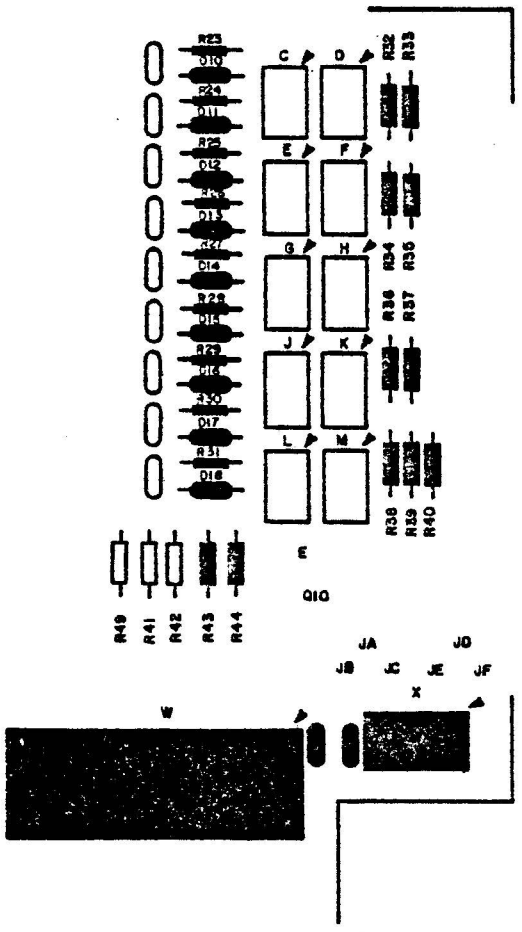


5-11. Male and Female Connector Installation

5-22. Optional Jumper Connections

There are four optional jumper wires that may be installed on the 680b-PCI board. Use the resistor leads saved from Paragraph 5-11 to cut 1-inch lengths, and jumper the pads as shown in the following chart.

Control Line	Jumper
( ) For CA2 HIGH	JA to JB
( ) For CA2 LOW	JA to JC
( ) For CB2 HIGH	JD to JE
( ) For CB2 LOW	JD to JF



5-12. Optional Jumper Connections

5-23. BOARD INSTALLATION

Before installing the 680b-PCI board, check the board for solder shorts, open lands or missing components. Make sure the 680b-MB Expander Card is correctly installed according to the instructions enclosed with the card. The 680b-PCI board is connected to the expander card with a 100-pin edge connector, and is installed horizontally above the 680b Main Board with two threaded standoffs. Install the 680b-PCI board according to the following instructions.

5-24. Installation of 100-Pin Edge Connector Onto Expander Card

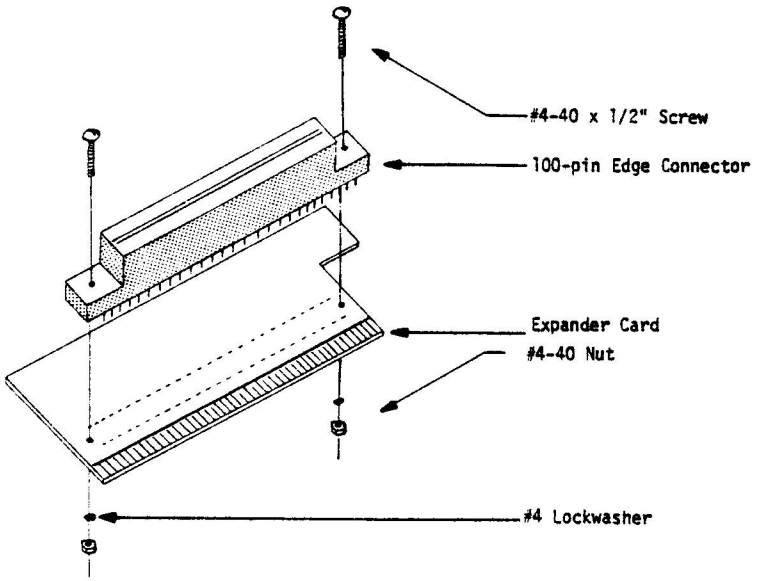
1. Remove the Expander Card from the socket on the 680b Main Board.

2. Orient the 100-pin edge connector (Bag 6) over the two rows of holes at the lowest unused position on the Expander Card.

3. Insert the connector pins into their respective holes. It may be necessary to guide the pins with the tip of a small screwdriver. Insure that the 100-pin connector is tight against the board and that all 100 pins are in their respective holes.

4. Secure the connector to the card with two #4-40 x 1/2" screws and two #4-40 nuts (Bag 5).

5. Solder each pin to the foil pattern on the back of the board. Be sure not to leave any solder bridges.



5-13. Installation of 100-Pin Edge Connector Onto Expander Card

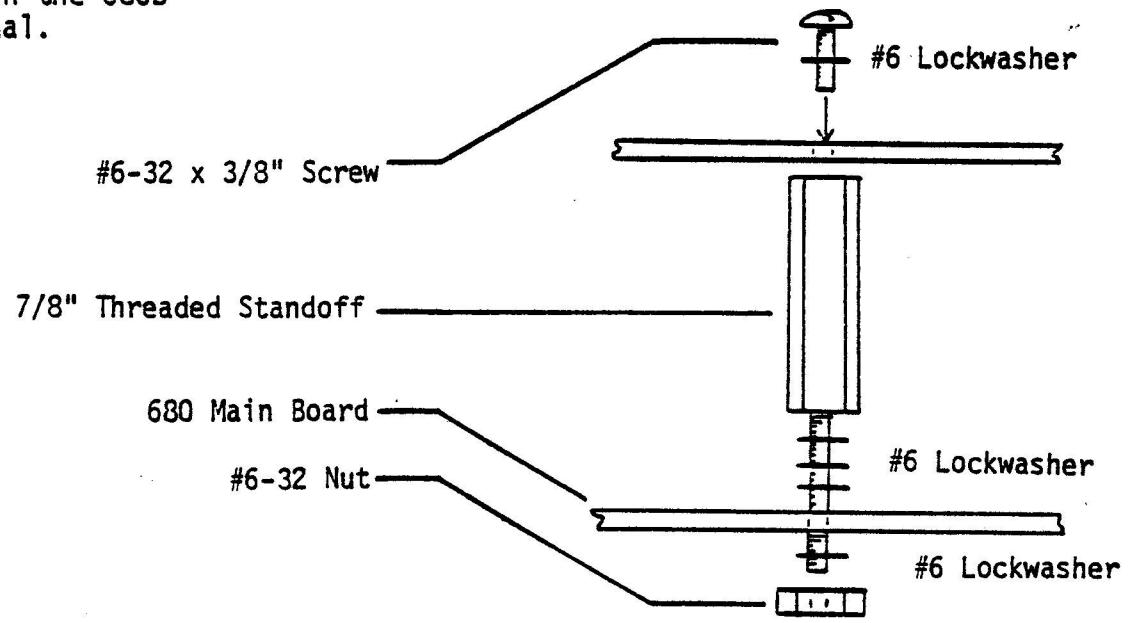
5-25. Installation of Threaded Standoffs Onto 680b Main Board

> NOTE
>
> If this board is not being installed in the lowest position on the Expander Card, proceed to Paragraph 5-26.

1. Carefully remove the 680b Main Board from the case. Referring to Figure 5-14, insert a #6-32 x 7/8" threaded standoff (Bag 5) with three #6 lockwashers (Bag 5) in the mounting holes provided on each side of the Main Board.

2. Secure each standoff by placing a #6 lockwasher and a #6-32 nut on the bottom of the board.

3. Properly replace the 680b Main Board in the case as shown on pages 69-70 in the 680b Assembly Manual.



5-14. Installation of Threaded Standoffs Onto 680b Main Board

5-26. 680b Process Control Interface Final Installation

1. Replace the Expander Card in its socket on the 680b Main Board.

2. Insert the card stab connector of the 680b-PCI board (silk-screened side up) into the 100-pin edge connector on the Expander Card.

3. Secure the board in place by inserting a #6-32 x 3/8" screw and a #6 lockwasher (Bag 5) into the top of each threaded standoff, as shown in Figure 5-15, page 104.

5-27. Installation of More Than One Board

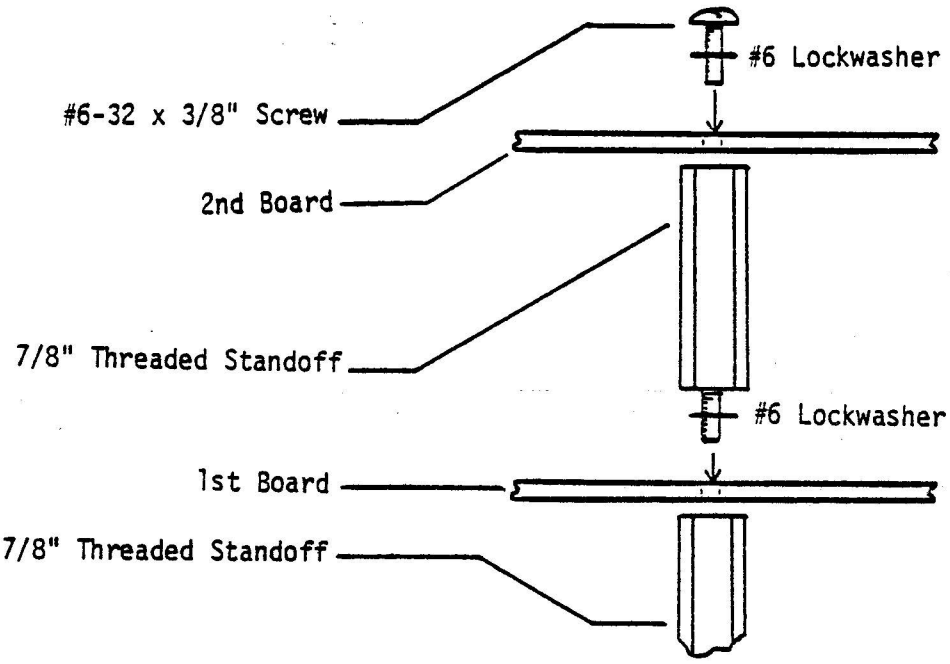
1. If this board is being installed in the second or third position above the 680b Main Board, follow the same procedure for installation of the 100-pin edge connector onto the Expander Card (Paragraph 5-23).

2. After installation of the 100-pin connector has been completed, reinstall the Expander Card and the lower board(s) into the 680b Main Board.

3. Replace the #6-32 x 3/8" screws and #6 lockwashers that previously secured the lower board with two #6-32 x 7/8" threaded standoffs and two #6 lockwashers (Bag 5).

4. Insert the card stab connector of the 680b-PCI board (silk-screened side up) into the 100-pin edge connector.

5. Secure the 680b-PCI board in place by inserting a #6-32 x 3/8" screw and a #6 lockwasher (Bag 5) into the top of each threaded standoff.



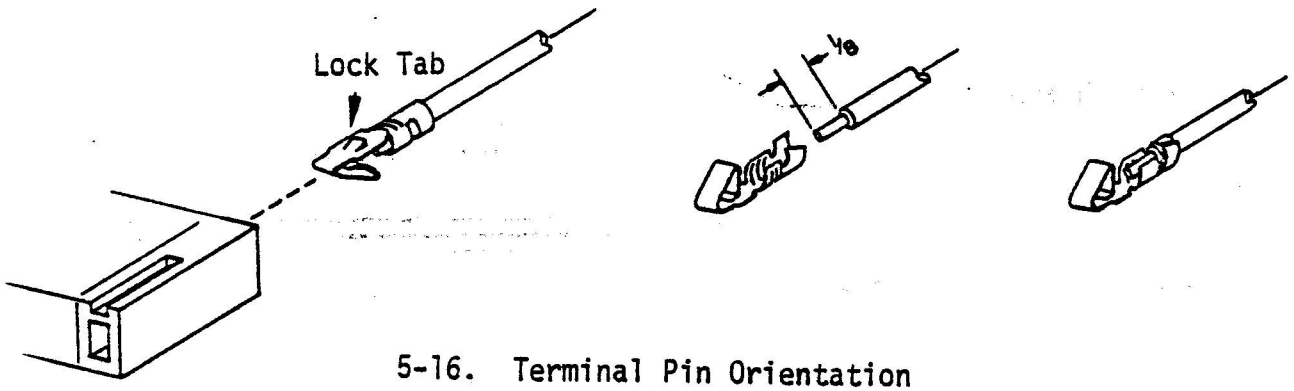
5-15. Installation of More Than One Board

5-28. Cable Assembly

An 18-paired twisted flat cable assembly is supplied for the relay outputs. A flat cable assembly is supplied for the opto-isolator inputs of the PIA. Install each cable according to the following procedure.

A. 18-Paired Twisted Flat Cable Assembly

1. Refer to Table 3-A, page 28, for proper wire connections.
2. Strip two inches of the clear plastic covering off the cable.
3. Strip 1/8" of insulation off each wire.
4. Crimp a miniature terminal pin (Bag 6) onto each wire and solder along the edges to insure a good connection.
5. Insert the plastic key (part number 101791, Bag 5) into pin 11 of the 25-pin connector.
6. Referring to Table 3-A, insert each of the 20 wires into its designated socket of the 25-pin connector. Make sure the terminal pin lock-tabs are facing up as shown in Figure 5-16.
7. The other end of the cable must be connected to a 24-pin connector. Strip 1/4" of insulation off each wire.
8. Referring to Table 3-A, insert the wires into the metal sockets and solder in place.



5-16. Terminal Pin Orientation

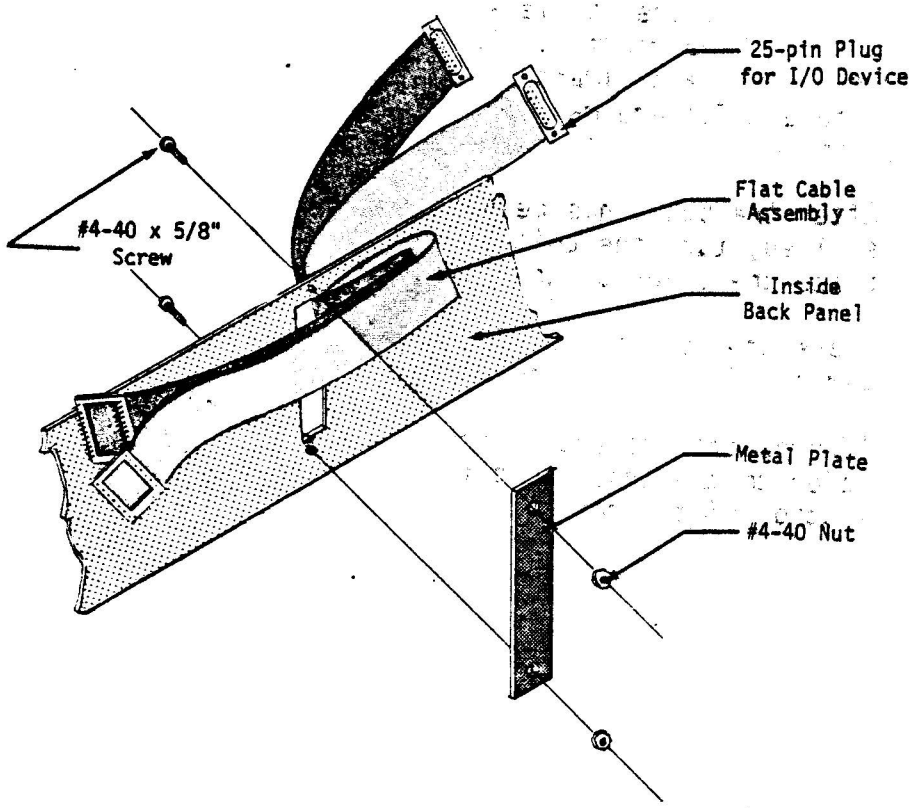
5-29. Cable Assembly Installation

Connect each cable according to the following instructions.

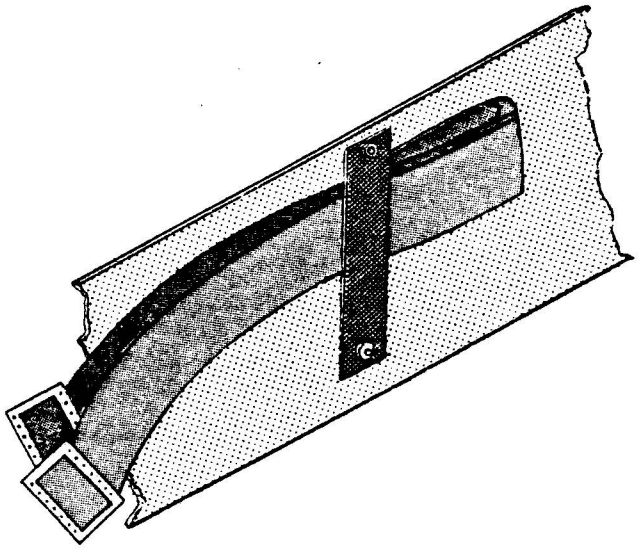
1. Remove the two #4-40 x 3/8" screws and the metal plate from the 680b back panel slot.

2. Insert the cables through the slot as shown in Figure 5-17, and plug into the appropriate board socket. The 25-pin connector on the 18-paired twisted flat cable plugs into male connector P1. The 25-pin plug on the flat cable connects to female connector, P2.

3. With the cable sockets properly inserted, fold the excess flat cable once against the back panel slot. Secure the cables as shown in Figure 5-18 with the metal plate supplied with the 680b back panel and two #4-40 x 5/8" screws (Bag 5) supplied with the 680b-PCI board.



5-17. Cable Assembly Insertion



5-18. Final Cable Assembly Installation

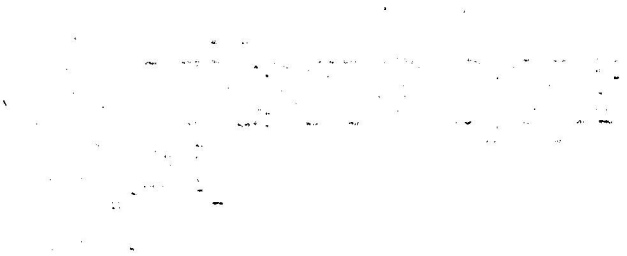
5-30. "Burn-In" Procedure

When assembly of the board has been completed, we recommend that a "burn-in" procedure (at least 48 hours long) be performed. Possible malfunctions due to improper assembly or component failure may occur at this time.

1. After the board has been installed, turn the unit on and place the cover on the computer.

2. Leave the computer on for a period of 48 to 100 hours.

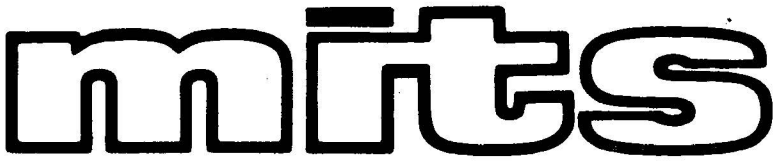
3. If problems are encountered, refer to the troubleshooting section of the manual.



appendix A
parts list

Bag	Quantity	Component	MITS Part Number
1	1	6820 Integrated Circuit	101097
	5	74LS04 Integrated Circuit	101042
	1	74LS02 Integrated Circuit	101136
	2	74LS30 Integrated Circuit	101135
	1	7805 Voltage Regulator	101074
2	12	IL-74 Opto-Isolator	100730
	12	2N-4410 Transistor	102806
	10	IN-914 Diode	100705
	8	IN-4004 Diode	100718
	2	DB-25M Male Connector	102111
	1	Printed Circuit Board	100214
	1	20" 18-Pair Twisted Flat Cable	103066
3	17	.1mf 12v Capacitor	100348
	1	33mf 16v Capacitor	100326
	1	500mf 25v Capacitor	100310
	1	.1mf 50v Capacitor	100312
	1	10mf 16v Tantalum Capacitor	100394
4	10	2.2K ohm, 1/2W Resistor	101945
	2	100 ohm, 1/2W Resistor	101924
	2	470 ohm, 1/2W Resistor	101927
	8	220 ohm, 1/2W Resistor	101925
	2	10K ohm, 1/2W Resistor	101932
	8	33 ohm, 1/2W Resistor	101921
	1	33K ohm, 1/2W Resistor	102053
	10	180 ohm, 1/2W Resistor	101998

Bag	Quantity	Component	MITS Part Number
5	1	Large Heat Sink	101870
	3	#6-32 x 3/8" Screw	100925
	3	#6-32 Nut	100933
	11	#6 Lockwasher	100942
	2	#4-40 x 1/2" Screw	100938
	2	#4-40 Nut	100932
	2	#4 Lockwasher	100941
	2	#4-40 x 5/8" Screw	100904
	1	DB-25 Female Connector	102112
	3	DB-25 Case Cover (8253)	101739
	2	7/8" Threaded Standoff	101666
	1	Polarizing Key	101791
6	1	Dip Switch	102321
	1	Ferrite Bead	101876
	25	Small Terminal Pin	101723
	1	25-pin Female Molex Connector	101882
	1	25-pin Male Molex Connector	101883
	1	40-pin Socket	102106
	1	24-pin Socket	102105
	14	14-pin Socket	102102
	1	Cable Assembly	103036
	8	LZ9 Relay	101653
	1	Edge Connector	101864



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