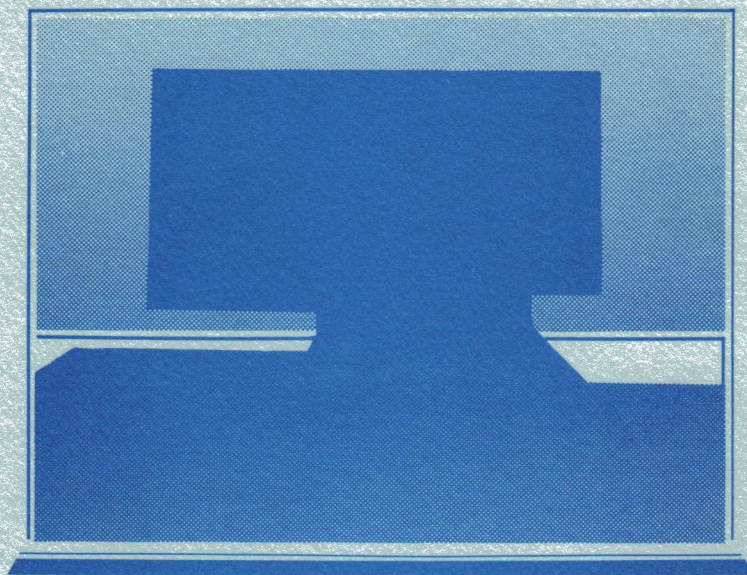


altair™ 680b-BSM

16K Static Memory Board



Documentation

ALTAIR 680b-BSM
16K Static Memory Board

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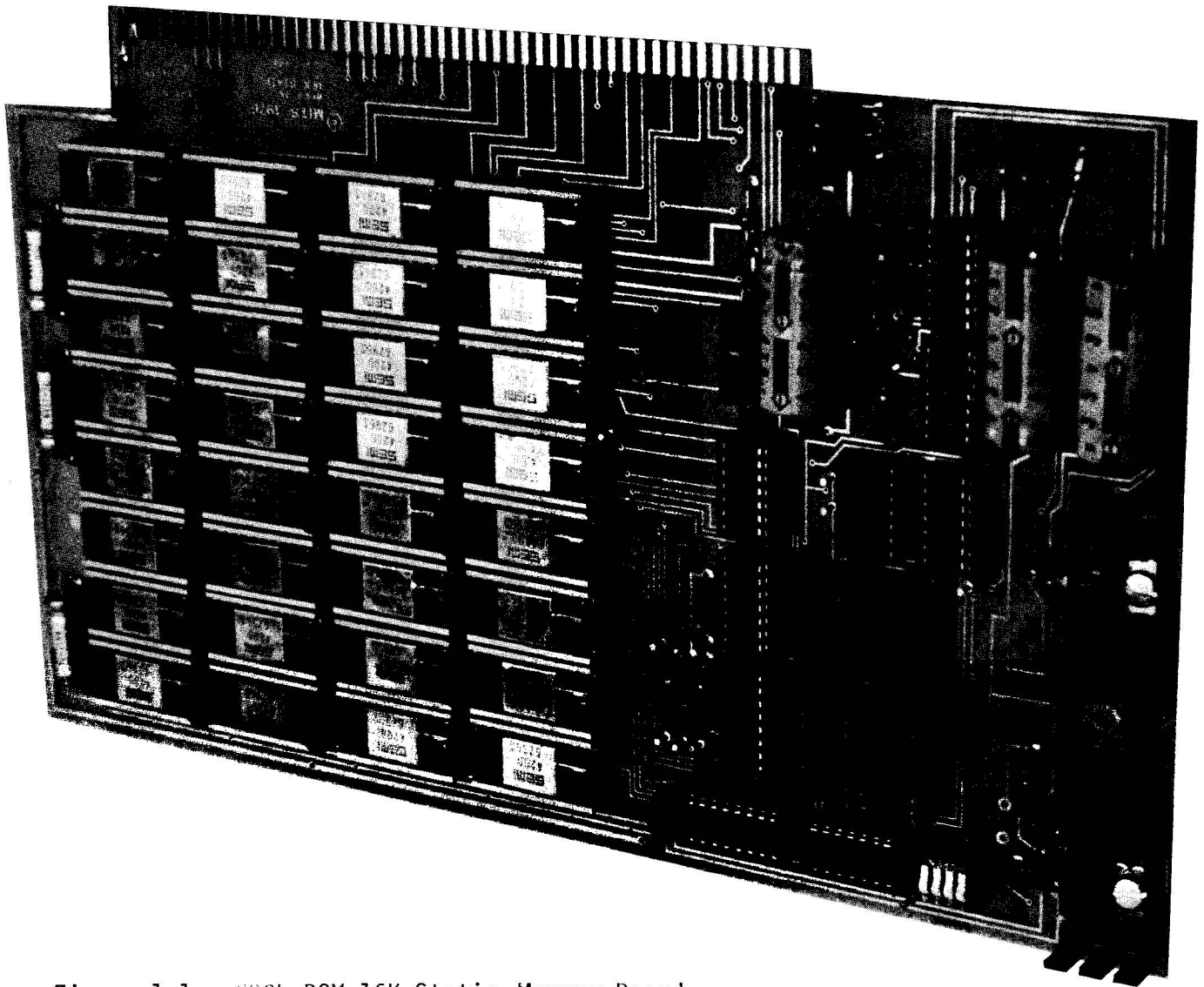


Figure 1-1. 680b-BSM 16K Static Memory Board

SECTION I

INTRODUCTION

1-1. SCOPE

The Altair 680b-BSM documentation provides a general description of the Altair 680b-BSM 16K Static Memory Board and its detailed theory and assembly instructions. The board is only compatible with the MITS Altair 680b computer.

1-2. ARRANGEMENT

This manual contains three sections as follows.

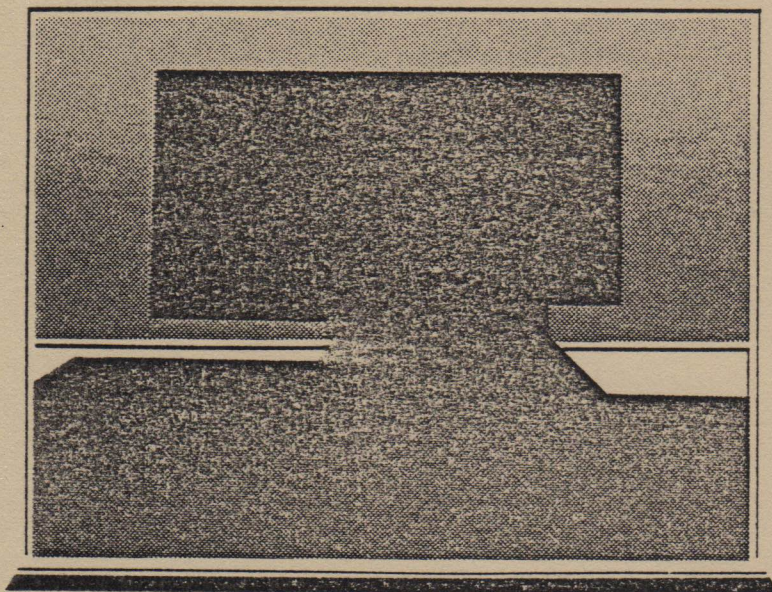
1. Section I: General Description
2. Section II: Theory of Operation
3. Section III: Assembly Instructions

1-3. DESCRIPTION

The Altair 680b-BSM 16K Static Memory Board has a minimal power consumption of 5 watts or 38 micro watts per bit. This allows operation of two 16K cards without adding a second transformer. It also has a fast access time with a maximum of 215 nanoseconds. A DIP switch is used for address selection and test points have been installed at important signal outputs for ease of checkout and troubleshooting. There are sockets for all ICs, providing easy installation and removal.

altair 680b-BSM

SECTION II



Theory of Operation
and
Troubleshooting

2-1. GENERAL

This section describes the operation of the 680b-BSM 16K Static Memory Board (16K Static). It contains an outline of the logic symbols used in the 16K static schematics, detailed theory of operation, and troubleshooting information.

2-2. LOGIC CIRCUITS

The logic circuits used in the 16K Static drawings are presented as a tabular listing in Table 2-1. The table is constructed to present the functional name, symbolic representation, and brief description of each logic circuit. Where applicable, a truth table is provided to aid in understanding the circuit operation. Although Table 2-1 does not include every logic circuit used in the drawings, all unmentioned circuits (and their symbolic representations) are variations of the circuits presented and their functional descriptions are fundamentally the same. The active state of the inputs and outputs of the logic circuits is graphically displayed by small circles. A small circle at an input to a logic circuit indicates that the input is an active LOW; that is, a LOW signal will enable the input. A small circle at the output of a logic circuit indicates that the output is an active LOW; that is, the output is LOW in the actuated state. Conversely, the absence of a small circle indicates that the input or output is an active HIGH.

2-3. SCHEMATIC REFERENCING

The detailed schematics of the 16K Static are provided to aid in determining signal direction and tracing. A solid arrow (→) on the signal line indicates direction, and the tracing of the signal through the schematics is referenced as it leaves the page. The reference is shown as a number - letter number (e.g. 2-A3), indicating sheet 2 and zone A3. The reference may be shown alone or in a bracket. If the reference is bracketed, the signal is going to another schematic which is referenced outside the bracket. If the reference is shown alone, the signal is going to another page of the multisheet schematic.

Table 2-1. Symbol Definitions



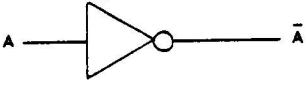
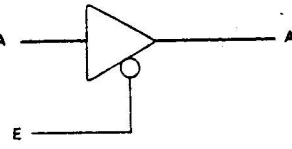
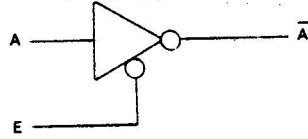
NAME	LOGIC SYMBOL	DESCRIPTION
NAND gate	 $Y = \overline{AB \dots N}$	<p>The NAND gate performs one of the basic logic functions.</p> <p>All of the inputs have to be enabled (HIGH) to produce the desired (LOW) output.</p>
NOR gate	 $Y = \overline{A + B \dots +N}$	<p>The NOR gate performs one of the basic logic functions.</p> <p>Any of the inputs need be enabled (HIGH) to produce the desired (LOW) output.</p>
Inverter		<p>The inverter is an amplifier whose output is the opposite state of the input.</p>
Non-Inverting Bus Driver		<p>The non-inverting bus driver is an amplifier whose output is the same state as the input. Data is enabled through the device by applying a (LOW) signal to the E input.</p>
Inverting Bus Driver		<p>The inverting bus driver is an amplifier whose output is the opposite state of the input. Data is enabled through the driver by applying a (LOW) signal to the E input.</p>

Table 2-1. Symbol Definitions

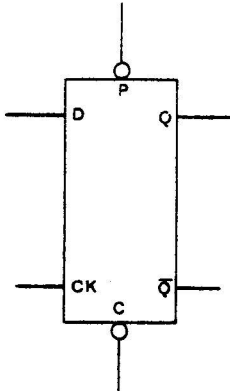
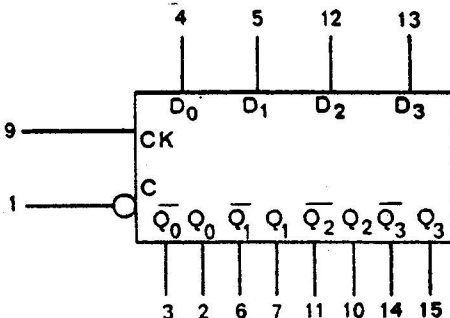
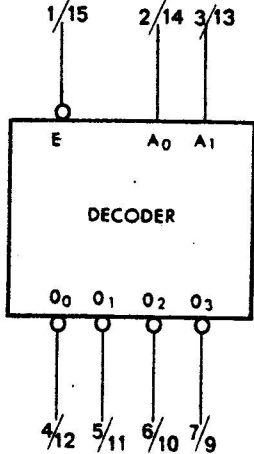
NAME	LOGIC SYMBOL	DESCRIPTION																																																																					
<p>Edge triggered D type flip-flop</p>	 <p>TRUTH TABLE</p> <table border="1" data-bbox="544 745 779 976"> <thead> <tr> <th>T_n</th> <th colspan="2">T_{n+1}</th> </tr> <tr> <th>D</th> <th>Q</th> <th>\bar{Q}</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>H</td> </tr> <tr> <td>H</td> <td>H</td> <td>L</td> </tr> </tbody> </table>	T_n	T_{n+1}		D	Q	\bar{Q}	L	L	H	H	H	L	<p>Applying a LOW signal to the preset input (P) sets the flip-flop with output Q HIGH and output \bar{Q} LOW. Applying a LOW signal to the clear input (C) resets the flip-flop with Q LOW and \bar{Q} HIGH. This method of setting and re-setting the flip-flop is independent of the clock (asynchronous). If a signal is applied to the D input, the flip-flop Q output is directly affected on the positive edge of the clock (cf. truth table)</p>																																																									
T_n	T_{n+1}																																																																						
D	Q	\bar{Q}																																																																					
L	L	H																																																																					
H	H	L																																																																					
<p>QUAD D flip-flop</p>		<p>The information on the D inputs is stored during the positive edge of the clock (CK). The clear (C) input, when LOW, resets all flip-flops independent of the clock or D inputs.</p>																																																																					
<p>4200 Random Access Memory (RAM) IC chip</p>	<table border="1" data-bbox="535 1386 787 2047"> <thead> <tr> <th>PIN</th> <th>SYMBOL</th> <th>FUNCTION</th> </tr> </thead> <tbody> <tr><td>1</td><td>V_{SX}</td><td>Supply Voltage (-5V)</td></tr> <tr><td>2</td><td>A₉</td><td>Address Input</td></tr> <tr><td>3</td><td>A₁₀</td><td>Address Input</td></tr> <tr><td>4</td><td>A₁₁</td><td>Address Input</td></tr> <tr><td>5</td><td>N/C</td><td></td></tr> <tr><td>6</td><td>D₁</td><td>Data In</td></tr> <tr><td>7</td><td>\bar{D}_0</td><td>Data Out</td></tr> <tr><td>8</td><td>A₀</td><td>Address Input</td></tr> <tr><td>9</td><td>A₁</td><td>Address Input</td></tr> <tr><td>10</td><td>A₂</td><td>Address Input</td></tr> <tr><td>11</td><td>V_{RF}</td><td>Supply Voltage (5V)</td></tr> <tr><td>12</td><td>\bar{R}/\bar{W}</td><td>Read/Write Input</td></tr> <tr><td>13</td><td>A₃</td><td>Address Input</td></tr> <tr><td>14</td><td>A₄</td><td>Address Input</td></tr> <tr><td>15</td><td>A₅</td><td>Address Input</td></tr> <tr><td>16</td><td>N/C</td><td></td></tr> <tr><td>17</td><td>\bar{CS}</td><td>Chip Select</td></tr> <tr><td>18</td><td>V_{DD}</td><td>Supply Voltage (12V)</td></tr> <tr><td>19</td><td>A₆</td><td>Address Input</td></tr> <tr><td>20</td><td>A₇</td><td>Address Input</td></tr> <tr><td>21</td><td>A₈</td><td>Address Input</td></tr> <tr><td>22</td><td>GND</td><td>Ground</td></tr> </tbody> </table>	PIN	SYMBOL	FUNCTION	1	V _{SX}	Supply Voltage (-5V)	2	A ₉	Address Input	3	A ₁₀	Address Input	4	A ₁₁	Address Input	5	N/C		6	D ₁	Data In	7	\bar{D}_0	Data Out	8	A ₀	Address Input	9	A ₁	Address Input	10	A ₂	Address Input	11	V _{RF}	Supply Voltage (5V)	12	\bar{R}/\bar{W}	Read/Write Input	13	A ₃	Address Input	14	A ₄	Address Input	15	A ₅	Address Input	16	N/C		17	\bar{CS}	Chip Select	18	V _{DD}	Supply Voltage (12V)	19	A ₆	Address Input	20	A ₇	Address Input	21	A ₈	Address Input	22	GND	Ground	<p>The chip select controls the operation of the memory. When chip select input is HIGH, power is supplied only to the memory elements. Other internal circuits are in the off state until the chip select input is pulled LOW enabling the memory. The output stage is enabled on the negative going edge of the chip select.</p>
PIN	SYMBOL	FUNCTION																																																																					
1	V _{SX}	Supply Voltage (-5V)																																																																					
2	A ₉	Address Input																																																																					
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20	A ₇	Address Input																																																																					
21	A ₈	Address Input																																																																					
22	GND	Ground																																																																					

Table 2-1. Symbol Definition

NAME	LOGIC SYMBOL	DESCRIPTION
DUAL 1 of 4 Decoder		Applying a LOW to the enable (E) input allows the decoder to decode the A0 and A1 input information (truth table).

TRUTH TABLE

INPUTS			OUTPUTS			
\bar{E}	A_0	A_1	\bar{O}_0	\bar{O}_1	\bar{O}_2	\bar{O}_3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

2-4. 16K STATIC BLOCK DIAGRAM (Figure 2-1)

The Central Processing Unit (CPU) controls the interpretation and execution of software instructions, and the 16K Static memory stores the software information to be used by the CPU. Sixteen ADDRESS LINES (A0-A15) condition the 16K Static Memory for data transfer. Data is transferred between the CPU and memory on eight bi-directional DATA LINES (D0-D7). Four control lines are required to allow the data transfer to occur. The READ/WRITE line controls the transfer of data to and from memory. The READ/WRITE-PRIME line enables Write Chip Select during a write cycle. The 2MHz and $\phi 2$ (500kHz) clocks are used to synchronize memory operations.

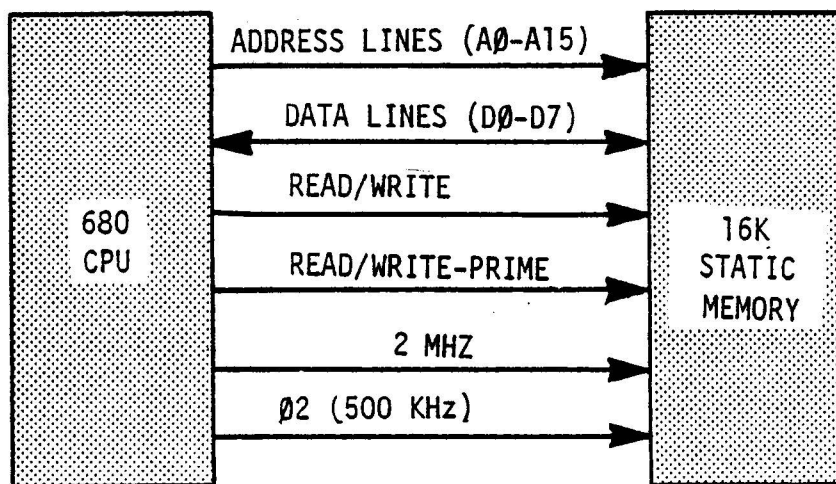


Figure 2-1. 16K Static Block Diagram

2-5. MEMORY ADDRESSING (Figure 2-4)

The memory addressing operation is necessary in any CPU-to-16K Static memory data transfer. The CPU selects a specific address in the 16K Static memory by the use of sixteen parallel address lines. The address lines contain binary information which represents a specific 16K Static memory address. Once the address information is present and stable, data is transferred to or from the memory address. Therefore, it is necessary to understand the 16K Static memory address decoding before discussing any data transfer operations.

The 16K Static memory is addressed by sixteen parallel lines, A0-A15 (sheets 1 and 2, zone D8). The A12-A15 (sheet 1, zone D8) bits of the address are the most significant bits (MSBs). These bits determine which memory board and which 4K section (\overline{CSA} - \overline{CSD} , zone D2) is to be addressed. Three combinations of binary numbers (00, 01, and 10) can be presented on the A14 and A15 (zone C7) bits to select the first, second, or third memory board. A 00 combination at A14 and A15 would be inverted by L (zone C7) and H (zone C6), presenting HIGHS to the A0 and A1 inputs of the one-of-four decoder C (zone C6). A constant LOW from inverter N (zone C6) to pin 15 enables C to decode a LOW at one of three output positions (S1, S2, or S3), as described in Table 2-2. When switch SW1 (zone C5) is positioned to 1 (Table 2-3), the S3 output is enabled for memory board one selection (0-15K), enabling one-of-four decoder C (zone C5).

Table 2-2. Operation of One-Of-Four Decoder

A0	A1	Produce LOW at	Enable Memory Board
1	1	S3	1
0	1	S2	2
1	0	S1	3

NOTE: Switch position 4 is not used on the 16K Static Board due to PROM and I/O addresses reserved in HIGH memory.

Table 2-3. Operation of Switch

4-Position Switch Configuration*				Memory Location	Address
1	2	3	4		
ON	Off	Off	Off	0 - 15K	0000-3FFF
Off	ON	Off	Off	16 - 31K	4000-7FFF
Off	Off	ON	Off	32 - 47K	8000-BFFF

*For each 16K static memory board, turn only one switch ON at a time.

The one-of-four decoder decodes any four binary combinations from address bits A12 and A13 (zone D7). The address bits are inverted by L (zone D7) and H (zone D6) to C, which decodes (in the manner described for A14 and A15) a LOW at outputs S0, S1, S2, or S3. This decoding determines which 4K area of memory on the selected board is being addressed. The A0-A11 bits (sheet 2, zone D8) determine the exact memory location in the 4K addressed area.

2-6. CLOCK SYNCHRONIZATION (Figures 2-2 and 2-4)

The $\phi 2$ (500KHz) and the 2MHz clocks are combined to generate a synchronized 1MHz signal used to control a Read or Write operation. The $\phi 2$ clock, after a 100 nanosecond propagation delay, goes LOW and is inverted HIGH by N pin 4 (sheet 1, zone B7) and LOW at N pin 6 (zone A6). This presents LOWs to K pin 1 and J pin 6. The HIGH at N, pin 4 is delayed 150 nanoseconds by the RC time constant of R9 and C5 (zone A6), leaving J pin 6 LOW. J pin 4 is enabled HIGH and inverted by J (zone B4), resetting flip-flop M (zone B6). With flip-flop M reset, the Q output is LOW, and the \bar{Q} output is HIGH. The reset condition remains until the 2MHz clock (zone B7) goes LOW at the bus and is inverted to a HIGH by N, setting flip-flop M (zone B6) for a 1MHz output at Q and \bar{Q} . The LOW at \bar{Q} is present at K pin 5 (zone A4). The HIGH at Q, after a 150 nanosecond delay by the RC time constant of R8 and C4 (zone B5), is inverted LOW by N pin 10 (zone B4) to the input of gate K pin 3 (zone A4). If a read or write signal is present from the CPU, gate K pin 12 or gate K pin 6 is enabled for a 400 nanosecond Read or Write operation.

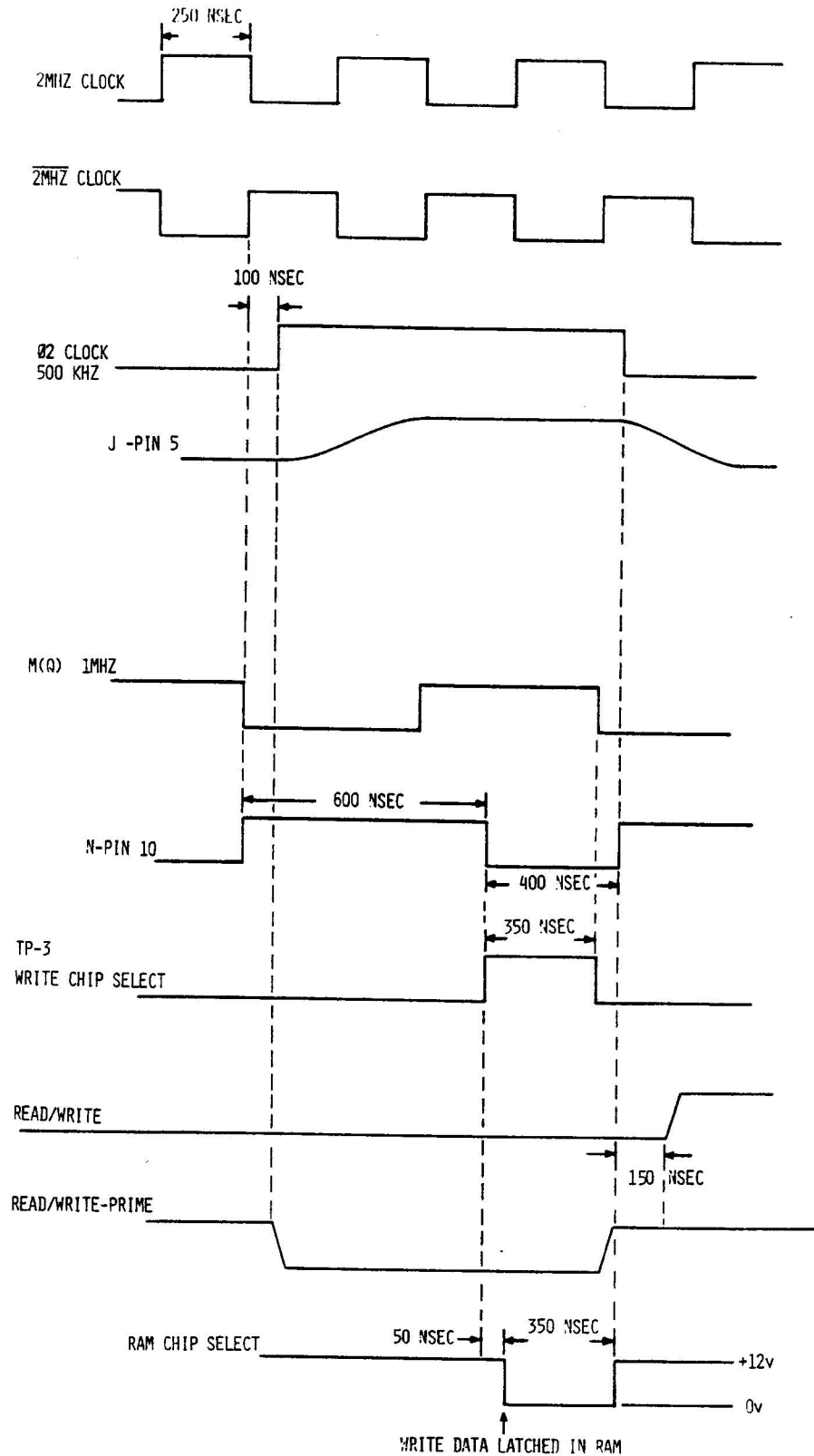


Figure 2-2. Write Cycle Timing Diagram

2-7. WRITING DATA INTO MEMORY (Figure 2-2 and 2-4)

Once address information is present, data can be transferred between the CPU and memory. Data is transferred to a specific address in memory over eight bi-directional data lines when a Read/Write instruction is generated on the control lines by the CPU. A Write instruction is generated when data is to be transferred and stored in an addressed memory location. Writing data in memory requires a LOW on the READ/WRITE and READ/WRITE-PRIME lines (sheet 1, zone A8). The LOW is inverted HIGH by N to pin 2 of NOR gate K and pin 8 of NOR gate J (zone A4), while simultaneously enabling the READ/WRITE driver F (sheet 2, zone A3) for a write operation. When the READ/WRITE-PRIME line is LOW and the 1MHz clock pulse is present, NOR gate K pin 4 (zone A4) is enabled, producing a LOW at pin 8 of NOR gate K (sheet 1, zone A3). This enables one of the D gates (zone D4), which is selected by one-of-four decoder C (zone D5), to determine a specific 4K area on the memory board. Data is transferred into the addressed memory location through data lines BD0-BD7 (sheet 2, zone C8) and inverting bus drivers L and H (zone C8).

2-8. READING DATA FROM MEMORY (Figure 2-3 and 2-4)

Reading data from memory is similar to a write operation. When data stored in a specific address is to be read, it is transferred between memory and the CPU over the same bi-directional data lines as the write operation. A HIGH on the READ/WRITE line (sheet 1, zone A7) is inverted LOW by N (zone A6) and applied to gate K, pin 2; gate J, pin 8 (zone A4); and gate F (sheet 2, zone A3) to enable the memory for a read operation. When the LOW 1MHz clock pulse is present, K pin 12 (sheet 1, zone A4) is HIGH, enabling Quad latches B and E (sheet 2, zone B5), and one of the D gates (sheet 1, zone D4) to determine the specific 4K area on the memory board. The data at Da-Dd is transferred to Qa-Qd while the clock is HIGH, but will not appear on data lines BD0-BD7 (sheet 2, zone C8) until the eight non-inverting data drivers, F and G (zone B6), are enabled. Gate J (sheet 1, zone A4) is enabled HIGH by the LOWs present at pins 8 and 9. The HIGH is inverted LOW by J (zone A3), enabling the non-inverting data drivers.

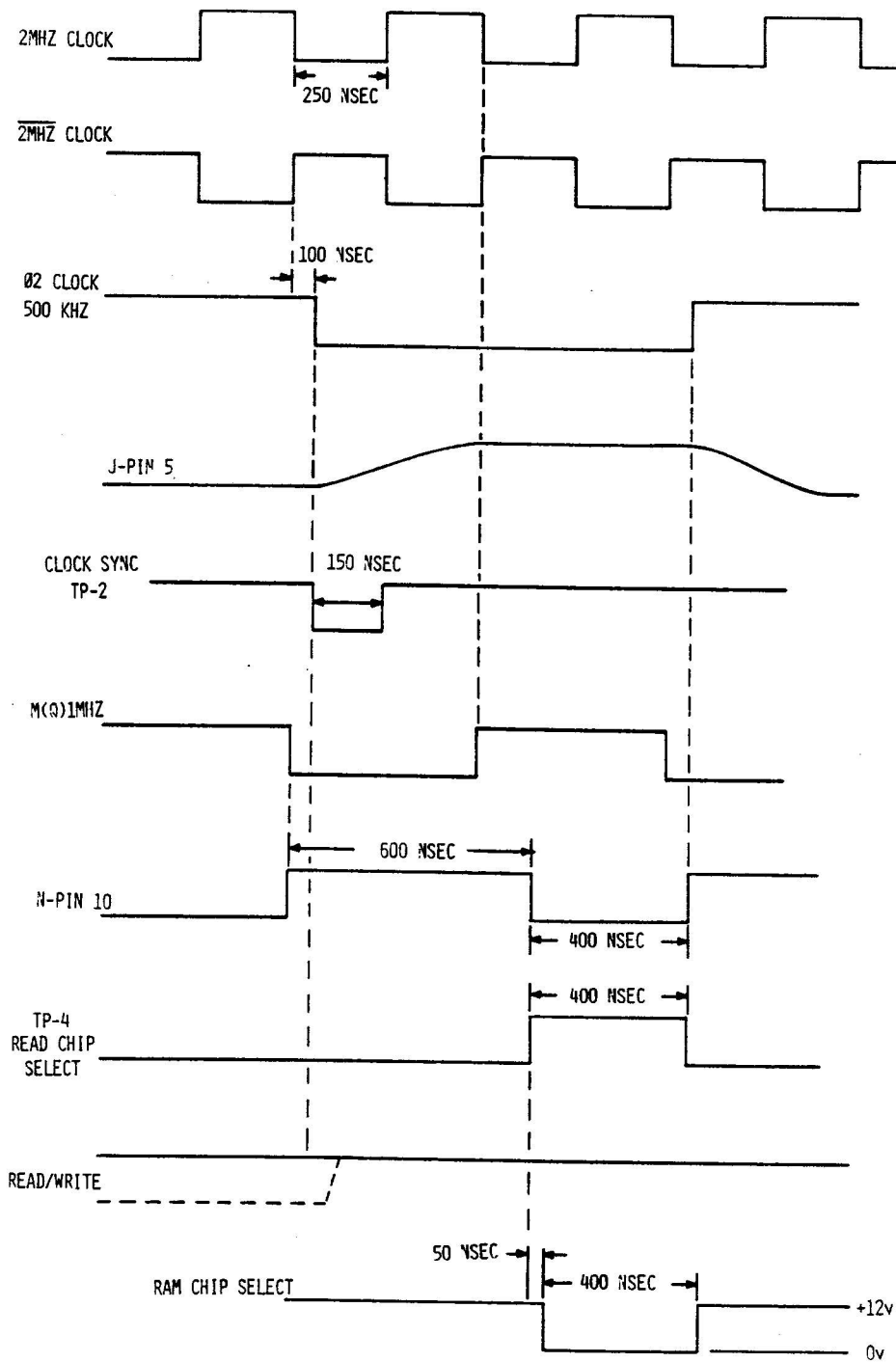


Figure 2-3. Read Cycle Timing Diagram

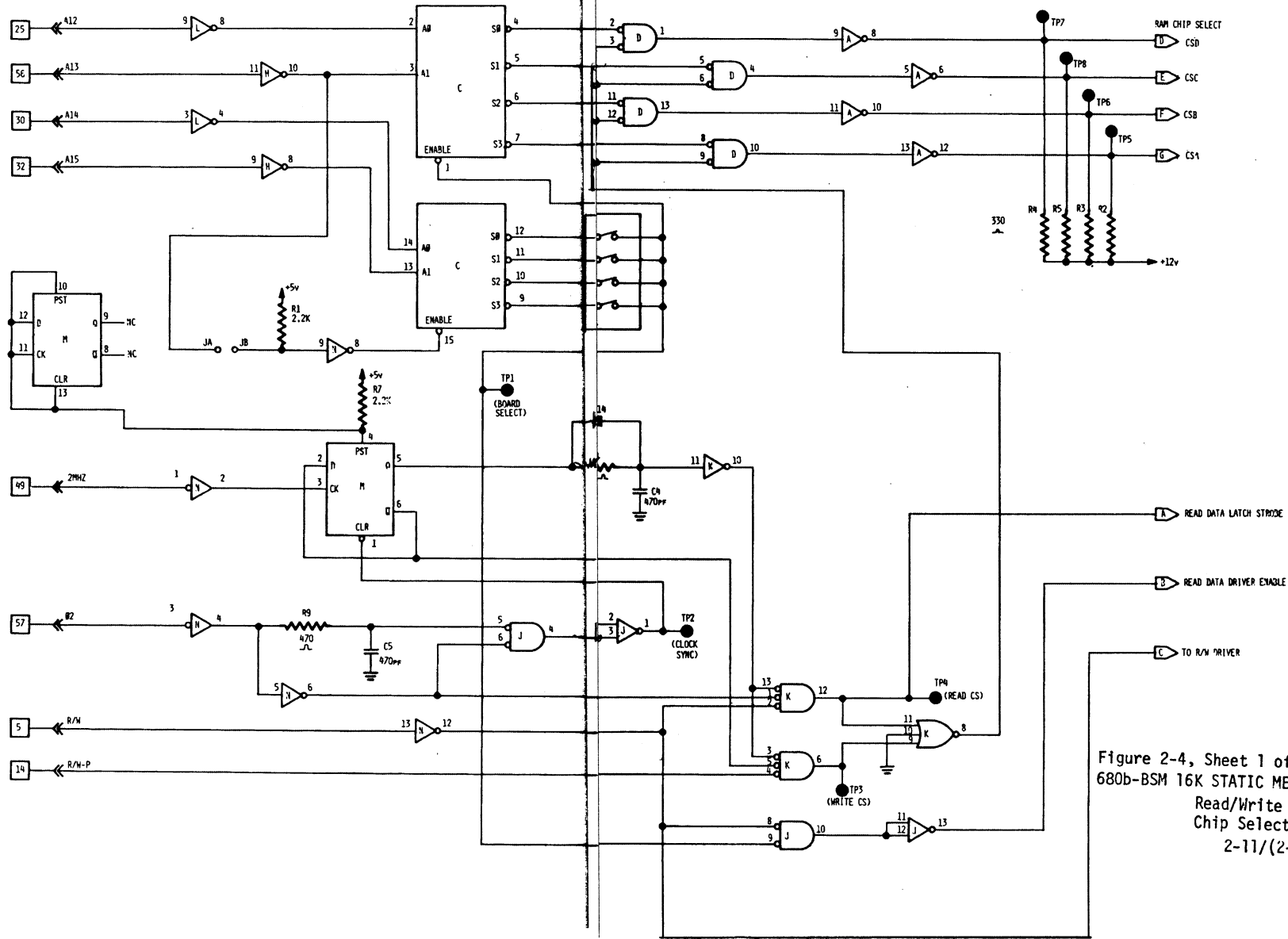


Figure 2-4, Sheet 1 of 2
 680b-BSM 16K STATIC MEMORY BOARD
 Read/Write Timing and
 Chip Select Circuits
 2-11/(2-12 Blank)

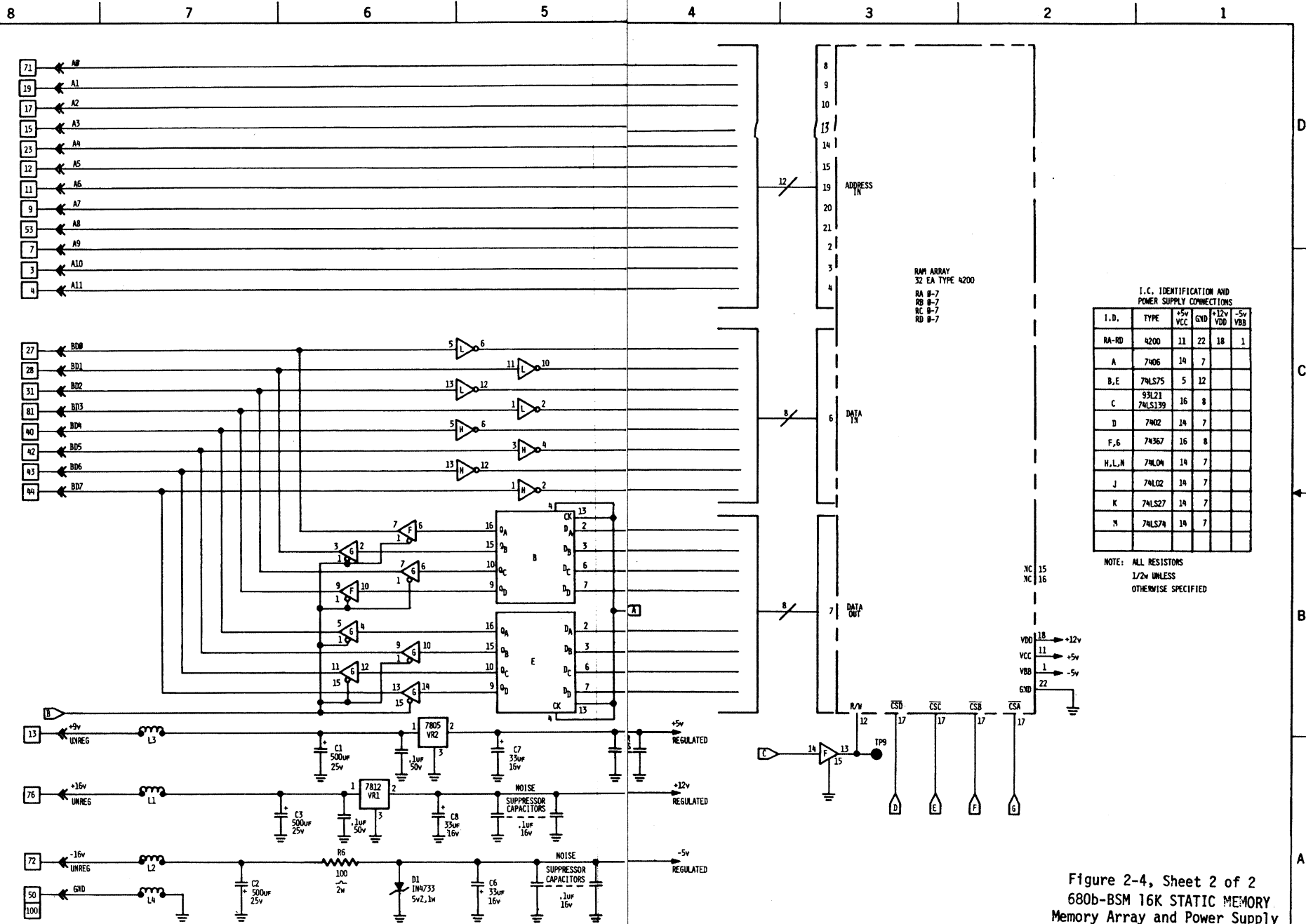


Figure 2-4, Sheet 2 of 2
680b-BSM 16K STATIC MEMORY
Memory Array and Power Supply

2-9. INTRODUCTION TO TROUBLESHOOTING

This section is designed to aid in locating a failure that could be encountered after the 16K static memory is assembled and installed. It contains a visual inspection check list, a preliminary check to make sure the board is functioning properly, troubleshooting tables to find component failures or assembly errors, and a memory test program designed to examine all locations in memory.

2-10. VISUAL INSPECTION CHECK LIST

Before an assembled board is installed, it should be checked for possible problems due to improper assembly.

1. Check for solder bridges.
2. Check for cold solder connections.
3. Examine electrolytic capacitors for proper polarity.
4. Examine diodes for proper polarity.
5. Be sure the correct color code has been observed on all resistors.
6. Check all IC chips for proper pin placement and good socket connections.

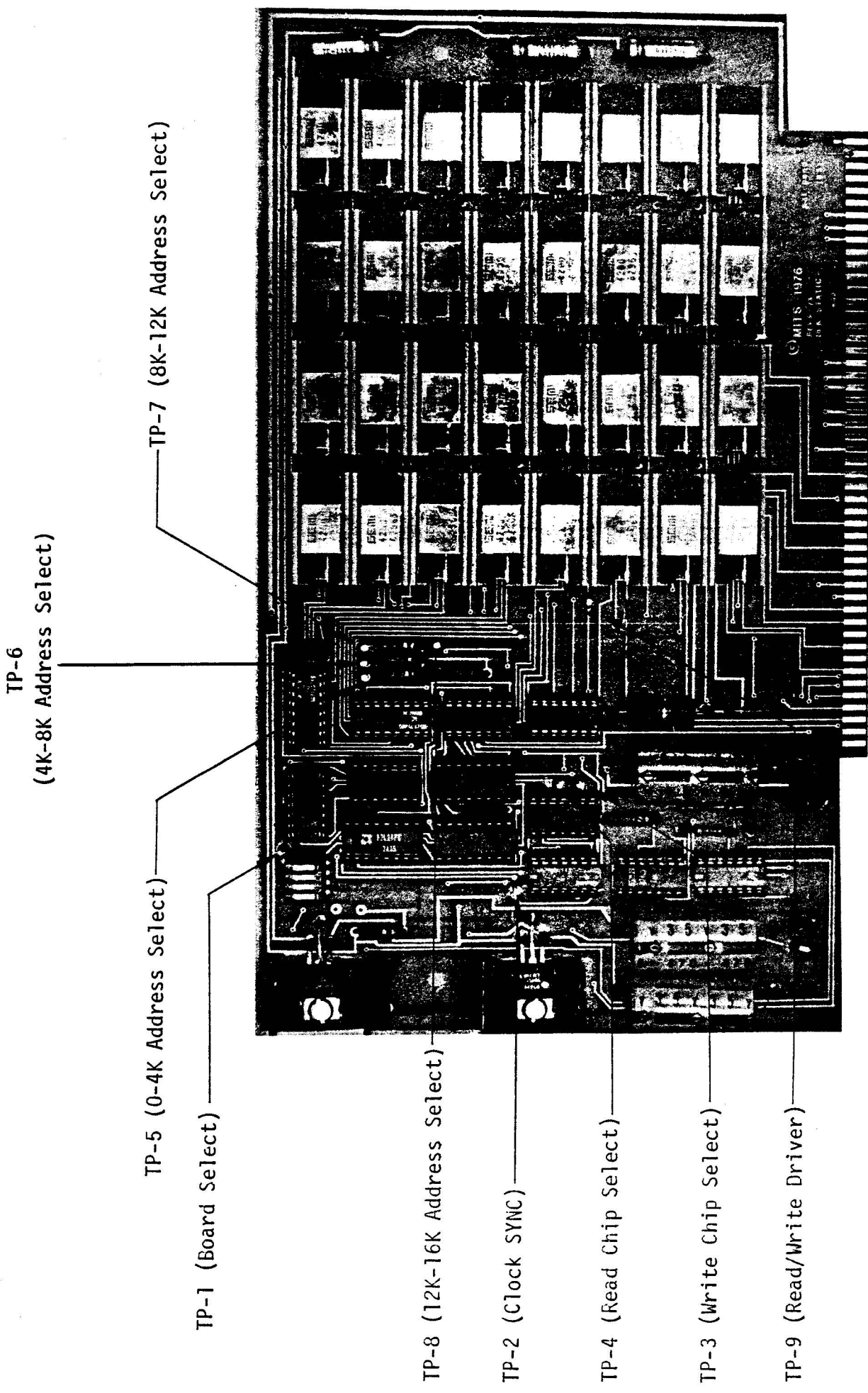
2-11. PRELIMINARY CHECK

After visual inspection has been completed and the 16K board has been installed, the address lines and data lines should be checked for shorts or opens. Be sure that the internal 1K of memory is wired above the 16K address and that all the preliminary checks are done while the computer is in the Halt mode. Initially, each address switch on the front panel should be in the down position and then switched to the up position individually while watching for the respective LED to come on. After all the address switches are HIGH, return them individually to the LOW position while watching for the respective LED to go off. If one LED fails to come on or go off, or if more than one LED comes on or goes off at the same time, there are possible problems on the 16K static board. The board should be removed from the circuit and

A resistance check should be made on the bus pins corresponding to the address lines showing the incorrect indications. If the resistance reading indicates an apparent short or open in the circuit, trace the land from the bus until the problem is isolated. Data lines are checked in much the same manner. All HIGHS are deposited into memory individually; then all LOWs are deposited while watching each respective LED. If any problems are detected, follow the above procedure.

2-12. TROUBLESHOOTING TABLES FOR 16K STATIC MEMORY BOARD

The following tables are designed under the assumption that there is only one failure on a board at any given time. In using the tables, refer to Figure 2-5 for test point locations, and Figures 2-6 through 2-9 for proper scope settings. The schematic diagram (Figure 2-4) is also included.



TP-6

(4K-8K Address Select)

TP-7 (8K-12K Address Select)

TP-5 (0-4K Address Select)

TP-1 (Board Select)

TP-8 (12K-16K Address Select)

TP-2 (Clock SYNC)

TP-4 (Read Chip Select)

TP-3 (Write Chip Select)

TP-9 (Read/Write Driver)

Figure 2-5. 16K Static Test Point Locations

TP-2
1 V/CM
500 NS/CM

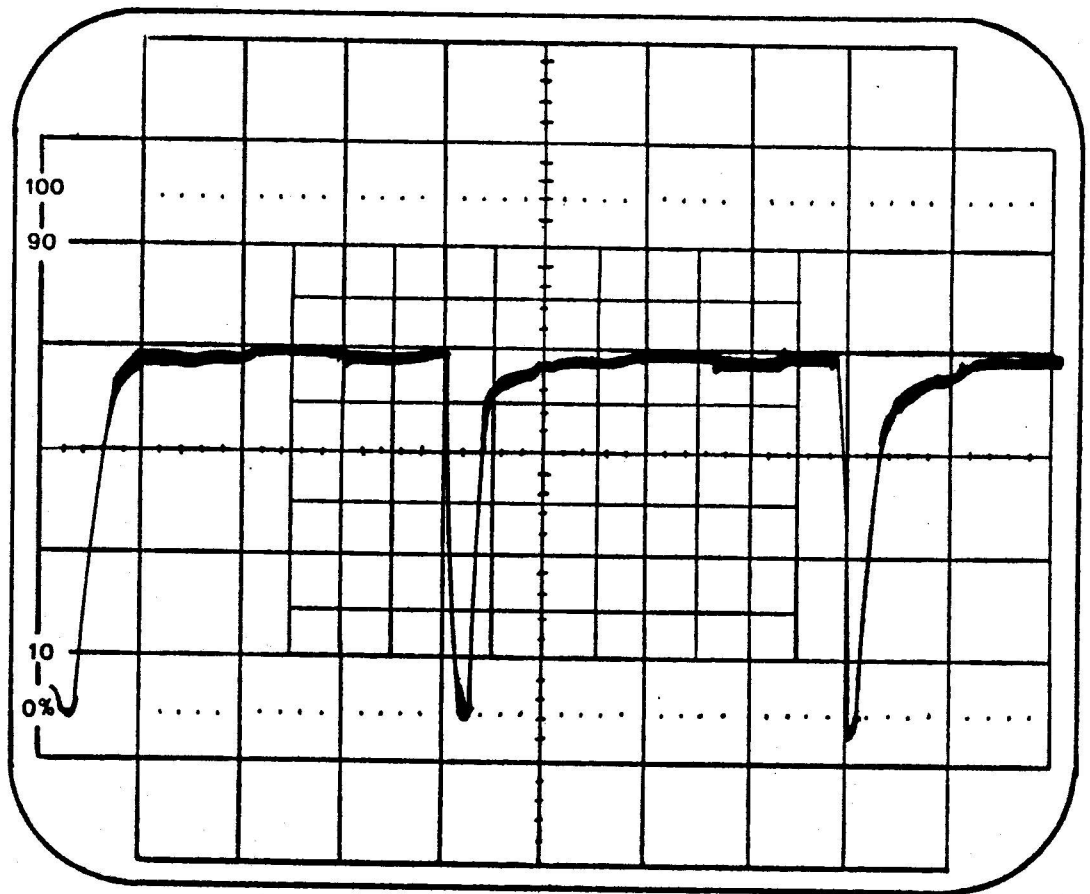


Figure 2-6. Test Point 2 (Clock SYNC) Waveform

TP-3
2 V/CM
100 NS/CM

TP-5
TP-6
TP-7
TP-8
5 V/CM
100 NS/CM

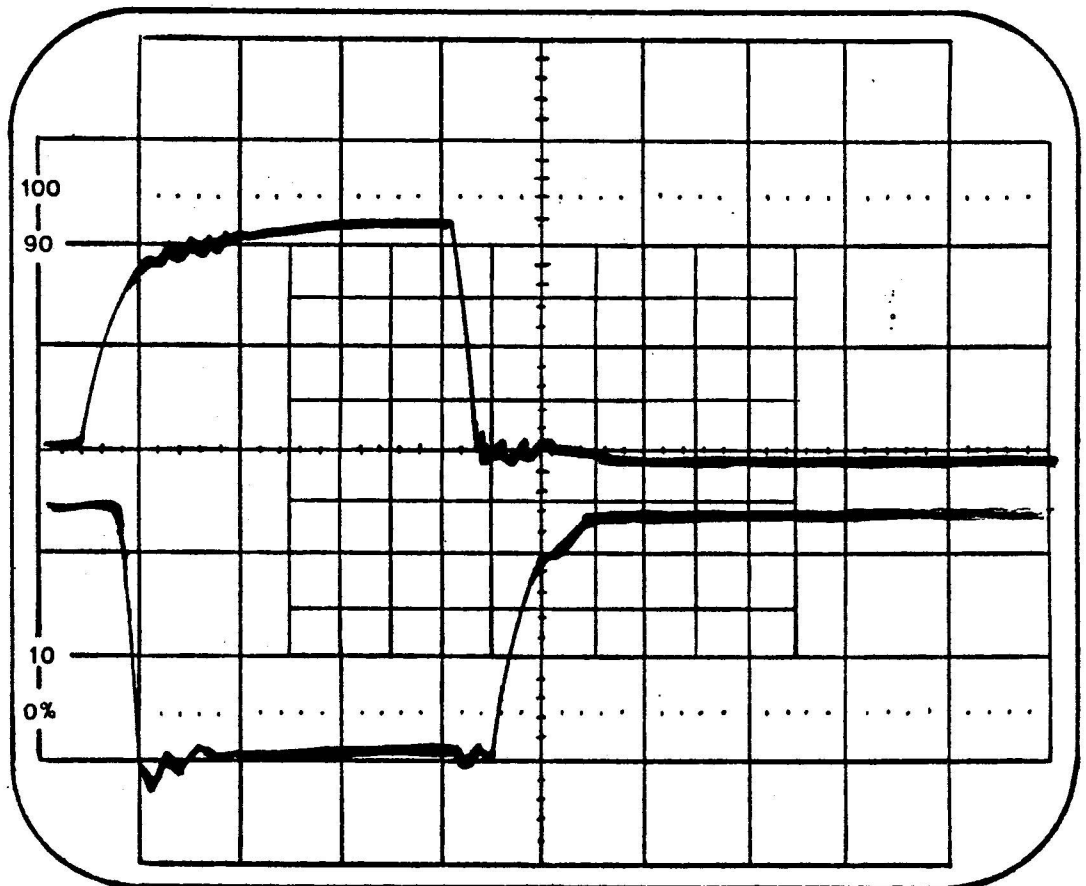


Figure 2-7. Test Point 3 (Write Chip Select) and Test Points 5, 6, 7, and 8 (Address Select) Waveforms

TP-4
2 V/CM
100 NS/CM

TP-5
TP-6
TP-7
TP-8
5 V/CM
100 NS/CM

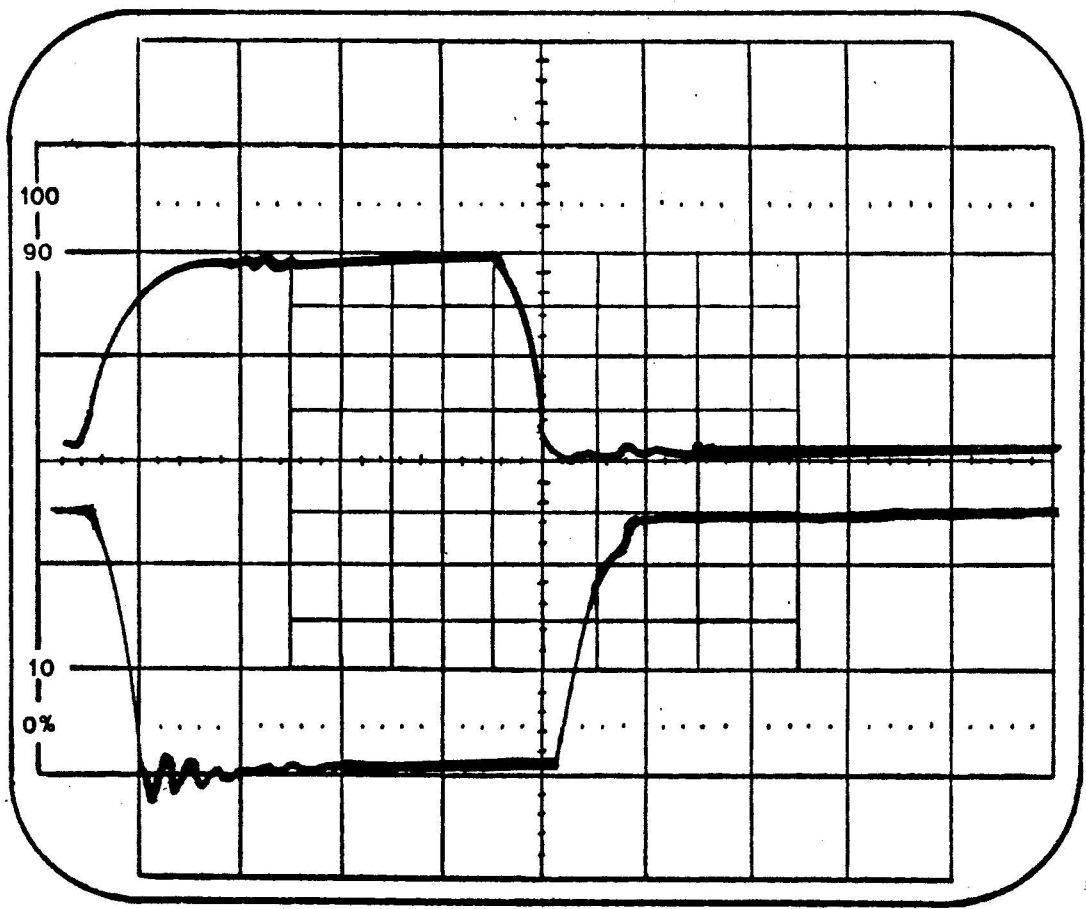


Figure 2-8. Test Point 4 (Read Chip Select) and Test Points 5, 6, 7, and 8 (Address Select) Waveforms

TP-9
2 V/CM
1 μ S/CM

ϕ 2 Clock
2 V/CM
1 μ S/CM

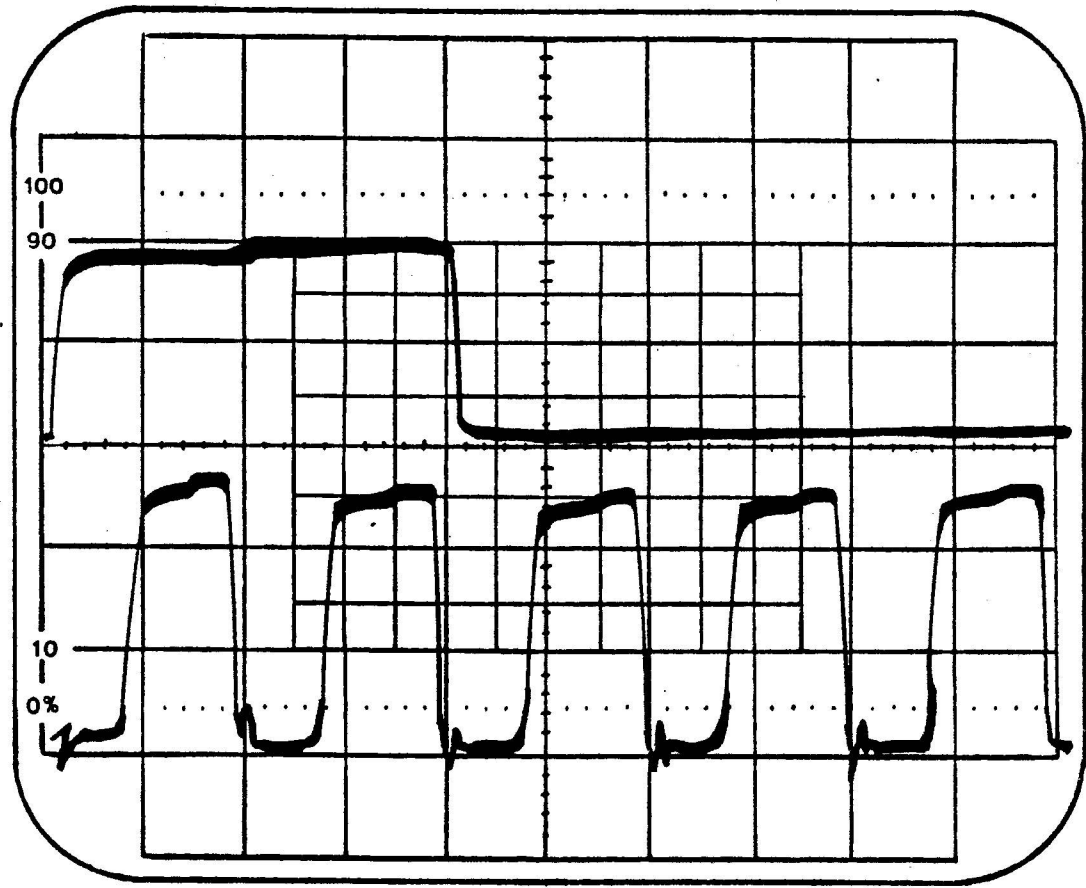


Figure 2-9. Test Point 9 (Read/ Write Driver) and ϕ 2 Clock Waveforms

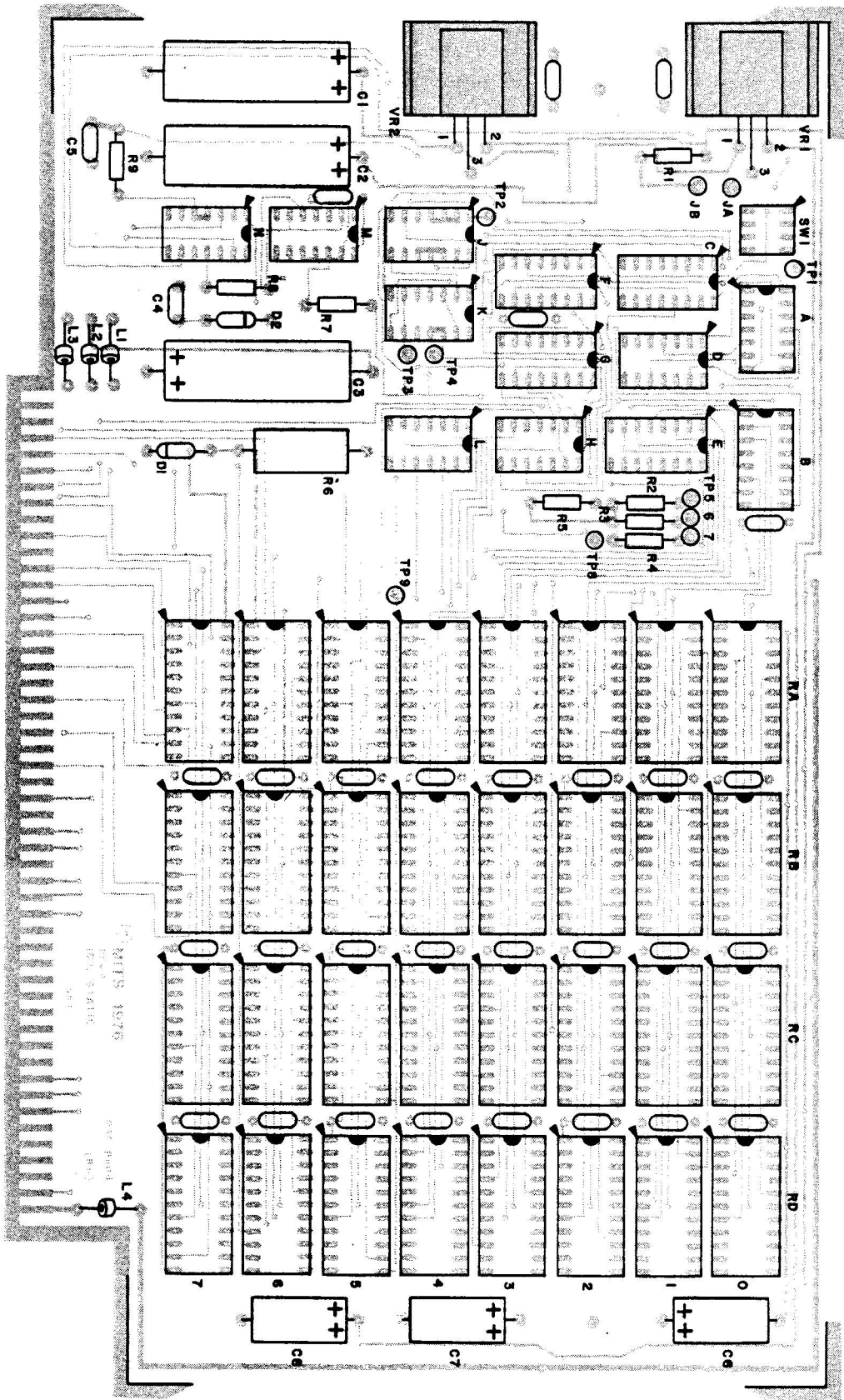


Figure 2-10. 680b-BSM 16K Static Memory Board (Top View)

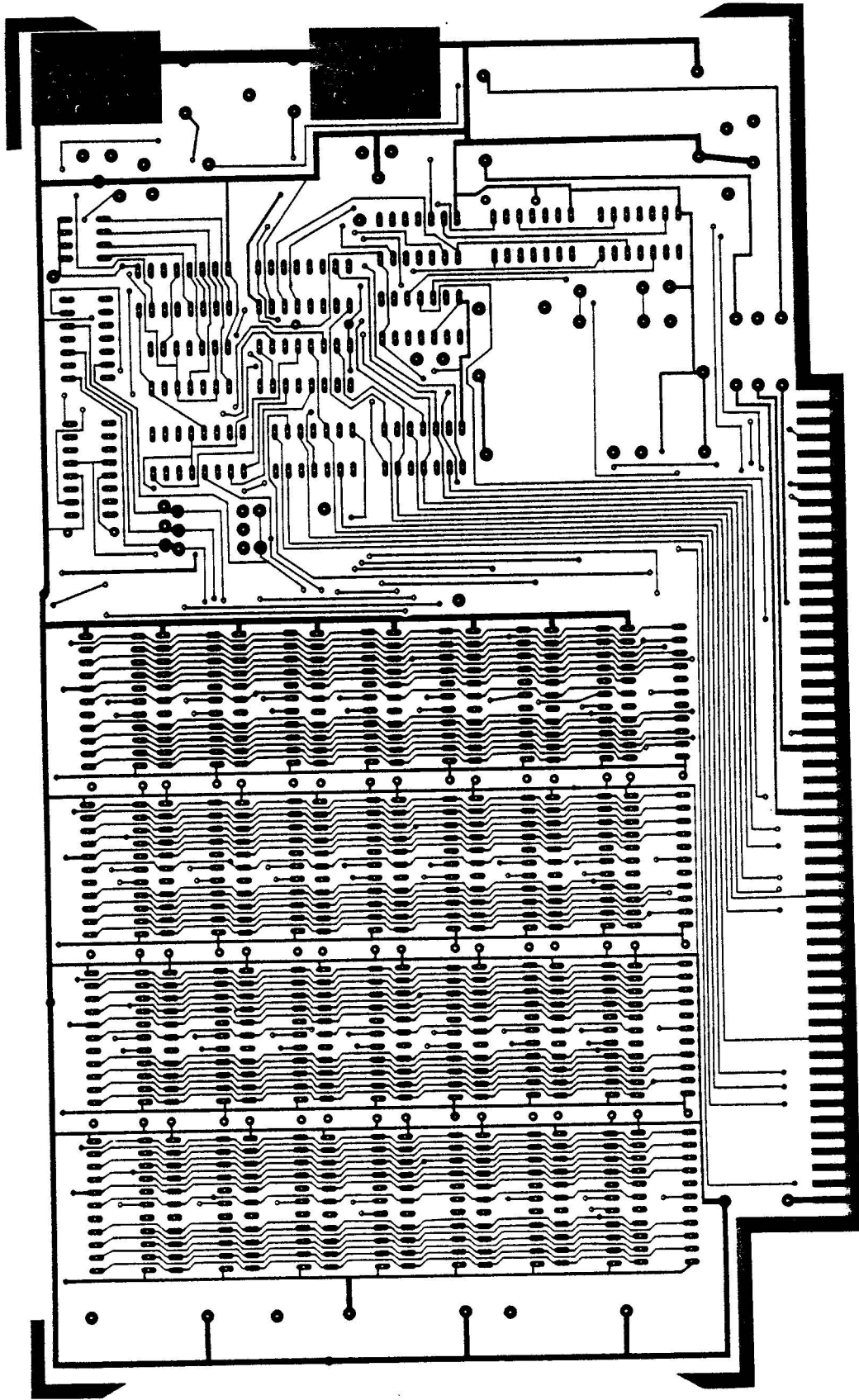


Figure 2-11. 680b-BSM 16K Static Memory Board (Bottom View)

Make sure the computer is in the Halt mode (front panel switch to HLT) and all address switches are down before starting troubleshooting. Be sure the correct board select switch (SW-1) is closed (up) for the board being examined and that the other three switches are open (down). In making measurements, a good ground is the negative end of capacitor C1 or C2 (Figure 2-10). Allow for a 10% error on all waveforms (Figures 2-6 through 2-9) to compensate for different component tolerance and scope calibrations. Before replacing chips or components, check carefully for solder shorts and broken or improper etching of lands. If a signal is missing, and there appears to be no continuity between the main board and the 16K board, be sure to check the solder connections of the 100 pin connectors on the expander card (680-MB) and the associated lands.

Sometimes it is difficult to recognize which table should be used to locate a problem on the 16K board. The power supply check (Table 2-4) should be completed before referring to any of the other tables when a failure is detected. This is to insure that proper voltage levels are being supplied to the various IC chips. Sometimes it is difficult to determine if a write operation is being executed. In this case, refer to Table 2-8 (step 1), and check to see if a write operation is present. If a write operation is present, proceed with the table; if not, refer to the table indicated. Most problems can be readily detected by observing the front panel LEDs and depositing and reading data.

Power Supply Check (Table 2-4)

STEP	SETTINGS AND INSTRUCTIONS	NORMAL INDICATIONS	IF CORRECT	IF INCORRECT INDICATION
1	Check +9V UNREG at bus pin 13, +16 UNREG at bus pin 76, and -16V UNREG at bus pin 72.	Should be about +9V; +16V and -16V respectively.	Proceed to Step 2.	Problem probably with input transformer. (Refer to 680 Manual.)
2	Check for regulated +5V at positive side of C7 (Figure 2-10).	Should be a constant +5V with a +5% tolerance.	Proceed to Step 3.	Check VR2 or check for shorted capacitor.
3	Check for regulated +12V at positive side of C8 (Figure 2-10).	Should be a constant +12V with a +5% tolerance.	Proceed to Step 4.	Check VR1 or check for shorted capacitor.
4	Check for a regulated -5V at the negative side of C6 (Figure 2-10).	Should be a constant -5V with a +5% tolerance.	End of Power Supply Check.	Check R6, Diode D1 or check for shorted capacitor.

16K Static Memory Will Not Read or Write (Table 2-5)

STEP	SETTINGS AND INSTRUCTIONS	NORMAL INDICATION	IF CORRECT	IF INCORRECT INDICATION
1	Position the A0-A15 switches on the front panel to up (HIGH). Monitor pins 71, 19, 17, 15, 23, 12, 11, 9, 53, 7, 3, 4, 27, 28, 31, 81, 40, 42, 43, and 44 on the bus.	Should go LOW and HIGH as respective address switch is toggled.	Proceed to Step 2.	The problem is probably in the CPU. (Refer to 680 Manual.)
2	Position the A0-A15 switches on the front panel down (LOW). Monitor Read Chip Select at TP4 (sheet 1, zone A3). Monitor Write Chip Select at TP3 (zone A3) while positioning DEP switch on front panel to DEP, and then release. (DEP switch only required for test at TP3.)	Should look like waveform in Figures 2-6 and 2-7.	Proceed to Step 3.	Proceed to Step 13.
3	Check NOR gate K (zone A3) pin 8.	Check pulse, if present.	Proceed to Step 4.	Probably bad and should be replaced
4	Check R/W Driver F at TP9 (sheet 2, zone A3) with Front Panel in RUN mode (Running Monitor).	Should look like waveform in Figure 2-8.	Proceed to Step 5.	Probably bad and should be replaced
5	Monitor TP1 (sheet 1, zone B4) and position on the front panel switches A14 and A15 for the board being examined:	TP1 will be LOW.	Proceed to Step 8.	Proceed to Step 6.
	A14 A15 Decoder Board Switch Position			
	0 0 S3 1 1 1			
	1 0 S2 2 2 2			
	0 1 S1 3 3 3			

16K Static Memory Will Not Read or Write (Table 2-5) - Continued

STEP	SETTINGS AND INSTRUCTIONS	NORMAL INDICATION	IF CORRECT	IF INCORRECT INDICATION
6	Check inverters L pin 4 (zone C7), H pin 8 (zone C6) and N pin 8 (zone C6).	Inverter N8 will be LOW, enabling decoder C (zone C6) L pin 4, and H pin 8 will be A14 and A15 inverted. Output will be LOW.	Proceed to Step 7	Probably bad and should be replaced
7	Check decoder C (zone C6) for LOW at correct output corresponding to board being checked (see table of step 5).		SW-1 probably bad or not set properly.	Decoder C probably bad and should be replaced.
8	Monitor TP2 (zone B4).	Should look like waveform in Figure 2-5.	Proceed to Step 13.	Proceed to Step 9.
9	Monitor Ø2 clock at the bus, pin 57 (zone B8).	Should be 500KHZ square wave.	Proceed to Step 10.	Possible problems with CPU. (Refer to 680 Manual.)
10	Check inverter N pin 4 (zone B7).	Should see Ø2 Clock.	Proceed to Step 11.	Probably bad inverter and should be replaced.
11	Check inverter N pin 6 (zone A6).	Should see Ø2 Clock.	Proceed to Step 12.	Probably bad and should be replaced.

16K Static Memory Will Not Read or Write (Table 2-5) - Continued

STEP	SETTINGS AND INSTRUCTIONS	NORMAL INDICATION	IF CORRECT	IF INCORRECT INDICATION
12	Check gate J pin 4 (zone B5).	Should see 150 ns. positive pulse every 2 microseconds (inverted signal of Figure 2-5).	Inverter J (zone B4) could be bad.	J (zone B5) probably bad and should be re-placed.
13	Monitor 2MHz Clock at bus pin 49 (zone B8).	A 2MHz square wave is present.	Proceed to Step 14.	Probably CPU problem. (Refer to 680 Manual.)
14	Check inverter N pin 2 (zone B7).	2MHz clock should be present.	Proceed to Step 15.	Probably bad and should be re-placed.
15	Check flip-flop M pin 5 (zone B6).	1MHz square wave is present.	Proceed to Step 16.	Flip-flop should probably be re-placed.
16	Check inverter N pin 10 (zone B4).	1MHz clock should be HIGH for 600 ns and LOW for 400 ns.	Proceed to Step 17.	If 1MHz signal present, check components in delay circuit. If signal is not there, N is probably bad and should be re-placed.

16K Static Memory Will Not Read or Write (Table 2-5) - Continued

STEP	SETTINGS AND INSTRUCTIONS	NORMAL INDICATION	IF CORRECT	IF INCORRECT INDICATION
17	Check inverter N pin 12 (zone A6). Toggle DEP switch on front panel to DEP and release.	Should be normally LOW pulsing HIGH when switch is pressed.	Check gates K (zone A4). Probably bad and should be replaced.	Inverter probably bad and should be replaced.

4K of 16K Static Memory Will Not Read or Write (Table 2-6)

STEP	SETTINGS AND INSTRUCTIONS	NORMAL INDICATION	IF CORRECT	IF INCORRECT INDICATION															
1	Position the A12 and A13 switches on the front panel as follows and monitor test points for each setting:	Should look like waveform in Figure 2-6 or 2-7.	Check pin 17 of RAMs, to insure that the proper column is being selected. Check address pins at RAM, or if possible, bad chip or chips can be located with a memory check (Table 2-9).	Proceed to Step 2.															
	<table border="1"> <thead> <tr> <th>A12</th> <th>A13</th> <th>Test Point</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>TP5</td> </tr> <tr> <td>1</td> <td>0</td> <td>TP6</td> </tr> <tr> <td>0</td> <td>1</td> <td>TP8</td> </tr> <tr> <td>1</td> <td>1</td> <td>TP7</td> </tr> </tbody> </table>	A12	A13	Test Point	0	0	TP5	1	0	TP6	0	1	TP8	1	1	TP7			
A12	A13	Test Point																	
0	0	TP5																	
1	0	TP6																	
0	1	TP8																	
1	1	TP7																	
2	Check inverters L pin 8 (zone D7) and H pin 10 (zone D6) for each of the four binary settings for A12 and A13.	L pin 4 and H pin 8 should be the inverse of A12 and A13.	Proceed to Step 3.	Probably bad and should be replaced															
3	Check decoder C (zone D7) for a LOW at correct output corresponding front panel settings of A12 and A13 as follows:	Output should be LOW; all others HIGH.	Proceed to Step 4.	Probably bad and should be replaced															
	<table border="1"> <thead> <tr> <th>A12</th> <th>A13</th> <th>Decoder</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>S3</td> </tr> <tr> <td>1</td> <td>0</td> <td>S2</td> </tr> <tr> <td>0</td> <td>1</td> <td>S1</td> </tr> <tr> <td>1</td> <td>1</td> <td>S0</td> </tr> </tbody> </table>	A12	A13	Decoder	0	0	S3	1	0	S2	0	1	S1	1	1	S0			
A12	A13	Decoder																	
0	0	S3																	
1	0	S2																	
0	1	S1																	
1	1	S0																	

4K of 16K Static Memory Will Not Read or Write (Table 2-6) - Continued

STEP	SETTINGS AND INSTRUCTIONS	NORMAL INDICATION	IF CORRECT	IF INCORRECT INDICATION
4	Check outputs of gates D, pins 1, 4, 13, or 10 (zone D4), for each front panel setting for A12 and A13. Monitor each gate, corresponding to the correct decoder output. (Refer to table in Step 3.)	Output should be HIGH.	Inverters A (zone D3) are probably bad.	Probably bad and should be replaced.

Unable to Write But Can Read Data (Table 2-7)

STEP	SETTINGS AND INSTRUCTIONS	NORMAL INDICATION	IF CORRECT	IF INCORRECT INDICATIONS
1	Check R/W and R/W-P line at data bus pins 5 and 14 (sheet 1, zone A8). Position DEP switch on front panel to DEP, and then release.	Normally HIGH signal will go LOW when switch is depressed.	Proceed to Step 2.	Probably problem with CPU. (Refer to 680 Manual.)
2	Check inverter N (zone A6). Position DEP switch.	Normally should be LOW going HIGH when switch is pressed.	Check K pin 6 (zone A3). Possibly bad and should be replaced.	Check inverter N. Possibly bad and should be replaced.

Unable to Read But Can Write Data (Table 2-8)

STEP	SETTINGS AND INSTRUCTIONS	NORMAL INDICATION	IF CORRECT	IF INCORRECT INDICATION
1	To be sure the CPU is able to write into memory, check outputs of L pins 2, 6, 10, and 12 (sheet 2, zone C5) and H pins 6, 12, 4, and 2 (sheet 2, zone C5). Toggle DEP switch on front panel to DEP, and then release.	Correct data should be present during deposit.	Proceed to Step 2.	Probably defective inverter or data line.
2	Check output of F pin 13 (R/W Driver, zone A3). Toggle DEP switch on front panel to DEP and then release.	Should be LOW going pulse when switch is toggled.	Proceed to Step 3.	Refer to Table 2-5.
3	Monitor TP4 (sheet 1, zone A3).	See Figure 2-7 for waveform.	Proceed to Step 5.	Proceed to Step 4.
4	Check inverter N pin 12 (zone A6).	Should invert HIGH when READ/WRITE line is LOW; and LOW when R/W line is HIGH.	Proceed to Step 5.	Possible problems and should be replaced.
5	Check Data Latch B and E (sheet 2, zone B5).	When clocked HIGH at (A), data at DA-DD should be latched to QA-QD.	Proceed to Step 6.	Latch is probably bad and should be replaced.
6	Check inverter J pin 10 (sheet 1, zone A4).	HIGH at J pin 10 should be LOW during a read cycle.	Proceed to Step 7.	Inverter probably bad and should be replaced.
7	Check inverter J pin 13 (zone A3).	LOW during read cycle.	Data Drivers F and G (sheet 2, zone B6) should be replaced.	Probably bad and possible bad.

2-13. MEMORY TEST

The memory test program (Paragraph 2-17) will test each location on the 680b-BSM 16K Static Memory Board for proper operation. The program operates by entering all 256 combinations of 8 bits into each memory location and checking to see if each combination has been stored properly. The test will print out the address of any "bad" memory locations.

2-14. Preparation for Loading the Memory Test Program

This test assumes that the first 100 memory locations of memory are good. If your 680b has been operating the monitor satisfactorily, the 1K of RAM on the 680b main board is probably good.

- A) If you are testing your first 16K board, leave the 1K of RAM strapped at address 0. Set the 4 position switch on the 680b-BSM 16K board to position #2 "on". See table 2-9 for the first and last memory address to be tested for the different settings of the address switch.
- B) If you are testing a second or third 16K board and using your first 16K board at the lowest 16K location (selector switch 1 "on"), be sure the 680b internal 1K memory is addressed above the highest addressed 16K board.

Table 2-9. 680b-BSM First/Last Address Locations

<u>SWITCH SETTING</u>	<u>FIRST LOCATION TO TEST</u>	<u>LAST LOCATION TO TEST</u>
SW1 ON (2, 3, 4 OFF)	0100	3FFF
SW2 ON (1, 3, 4, OFF)	4000	7FFF
SW3 ON (1, 2, 4 OFF)	8000	BFFF

- C) To avoid a malfunction during the memory test, take the following precautions:
 1. Do not test locations 0000 to 00FF, as the memory test and Monitor reside in these locations.
 2. Do not test areas where there is no memory. All locations tested with no memory will be printed out as bad locations.

2-15. Loading and Running the Memory Test Program

- A. Use the Monitor's M & N commands to enter the memory test program starting at location 0000.
- B. Use the Monitor's J command to start execution at 0000.
- C. A space and question mark will be printed on the terminal.
- D. Enter the address of the first memory location to be tested (refer to Table 2-9).
NOTE: Do not attempt to test locations 0-100, as the memory test and Monitor use these locations.
- E. A space and question mark will be printed on the terminal.
- F. Enter the address of the last memory location to be tested (refer to Table 2-9).
- G. Upon entry of the last location to be tested, the memory test will go into operation automatically.
- H. On each pass through the specified memory locations, the addresses of any "bad" locations will be printed.
- I. At the end of each pass, a "P" will be printed on the terminal.
- J. The program may be halted at any time by typing any character on the terminal. Control will then return to the Monitor. Switching front panel switches HALT, RESET, and RUN will also return control to the Monitor.

2-16. Interpreting the Output

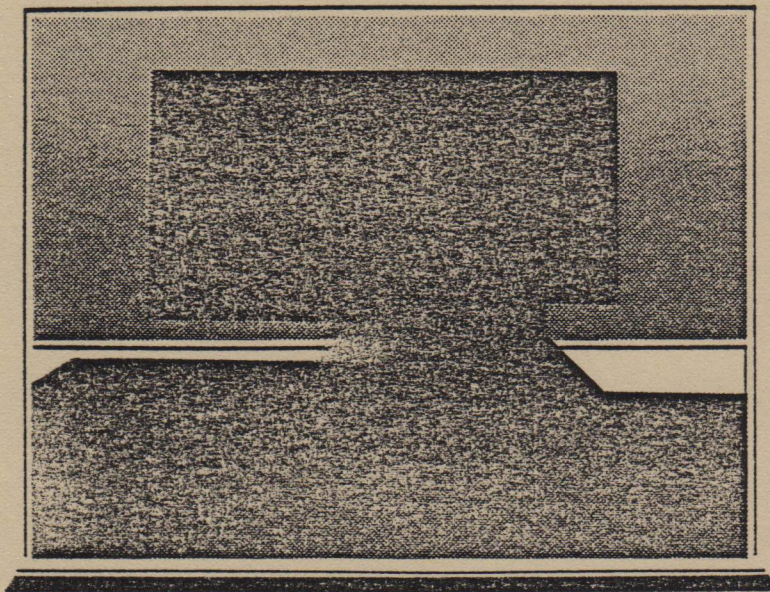
- A. If there are random individual bad locations, the problem is probably bad memory cells. This can be verified by examining the suspect location in the HALT mode and depositing all 1's or all 0's and checking for a bad bit. The defective RAM may then be easily isolated and replaced. Please attach a piece of masking tape indicating the address of the defective memory cell on any returned 4200 type RAMs.
- B. If there are long continuous groups of bad locations that show a certain pattern, try to determine what relationship the pattern has to the addressing of the RAMs, or which bit(s) are not being written or read correctly. This type of output indicates a defective data line, address problem, or bad socket connection on the RAM. Isolation of these problems is discussed earlier in the Troubleshooting section.

2-17. Memory Test Program Listing

Address	Contents	Address	Contents
0000	8D	0027	6D (6C for Baudot Monitor)
0001	41	0028	20
0002	DF	0029	03
0003	4D	002A	4C
0004	8D	002B	26
0005	3D	002C	DF
0006	08	002D	08
0007	DF	002E	9C
0008	4F	002F	4F
0009	DE	0030	26
000A	4D	0031	D9
000B	4F	0032	8D
000C	BD	0033	06
000D	FF	0034	C6
000E	24	0035	50
000F	24	0036	8D
0010	03	0037	08
0011	7E	0038	20
0012	FF	0039	CF
0013	D8 (CC for Baudot Monitor)	003A	C6
0014	A7	003B	0D
0015	00	003C	8D
0016	A1	003D	02
0017	00	003E	C6
0018	27	003F	0A
0019	10	0040	7E
001A	8D	0041	FF
001B	1E	0042	81
001C	DF	0043	BD
001D	51	0044	FF
001E	96	0045	82 (7F for Baudot Monitor)
001F	51	0046	C6
0020	BD	0047	3F
0021	FF	0048	8D
0022	6D (6C for Baudot Monitor)	0049	F6
0023	96	004A	7E
0024	52	004B	FF
0025	BD	004C	62 (61 for Baudot Monitor)
0026	FF		

altair 680b-BSM

SECTION III



Assembly

SECTION III

ASSEMBLY

3-1. GENERAL

This section contains all the information needed for the circuit construction of the Altair 680b-BSM 16K Static Memory Board. It consists of helpful assembly hints and detailed instructions of component installation on the 680b 16K Static Memory Board.

3-2. ASSEMBLY HINTS

Before beginning the construction of your unit, it is important that you read the "MITS Kits Assembly Hints" booklet included with your kit. Pay particular attention to the section on soldering because most problems occur as the result of poor soldering. It is essential that you use the correct type of soldering iron. A 25-30 watt iron with a chisel tip (such as an Ungar 776 with a 7155 tip) is recommended in the assembly hints booklet.

NOTE

Some important warnings are also included in the hints booklet. Read them carefully before you begin work on your unit -- failure to heed these warnings could cause you to void your warranty.

Check the contents of your kit against the appendix in this manual (Parts List) to make sure you have all the required components, hardware, and parts. The components are in plastic envelopes; do not open them until you need the components for an assembly step. You will need the tools called for in the "Kits Assembly Hints" booklet.

As you construct your kit, follow the instructions in the order they are presented in the assembly manual. Always complete each section before going on to the next. Two organizational aids are provided throughout the manual to assist you: 1) Boxed off parts identification lists, with spaces provided to check off the components as they are installed; 2) reproductions of the silkscreens showing previously installed components, components being installed, and components yet to be installed (Figure 3-1).

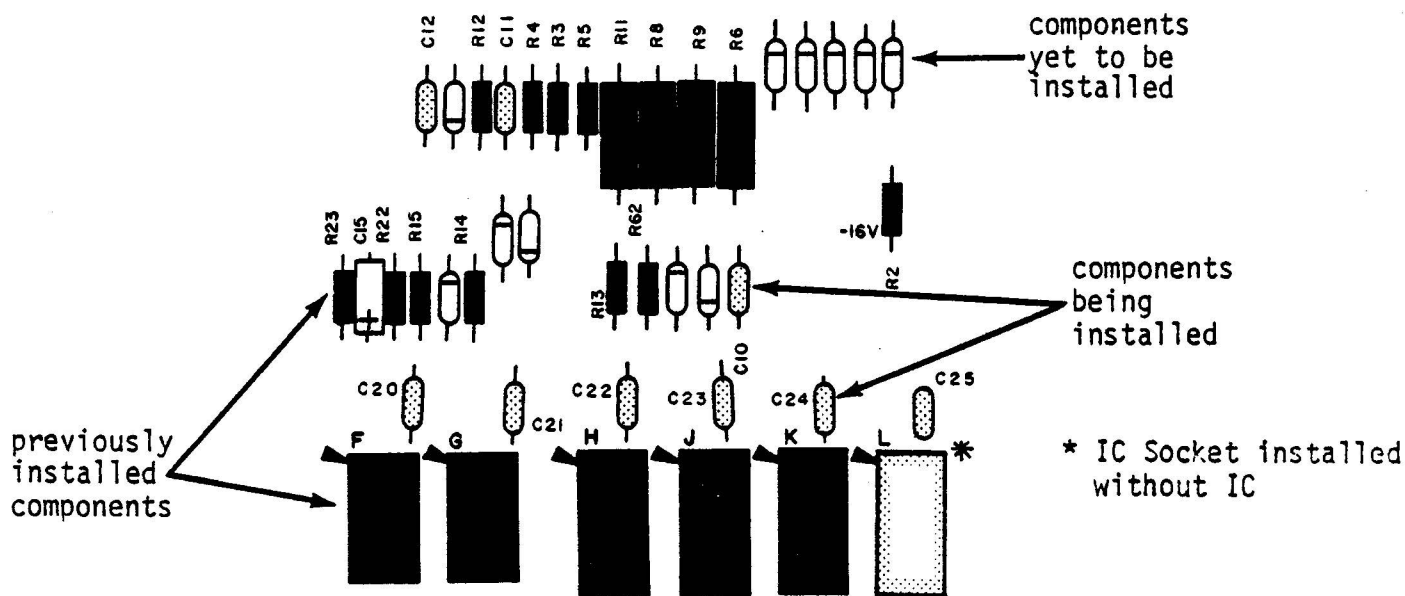


Figure 3-1. Typical Silkscreen

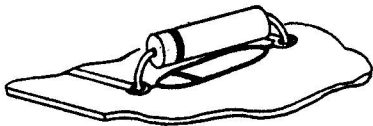
3-3. COMPONENT INSTALLATION INSTRUCTIONS

The following component installation instructions describe the proper procedures for installing various types of components in your kit. Read these instructions over very carefully and refer back to them whenever necessary. Failure to properly install components may cause permanent damage to the component or the rest of the unit; it will definitely void your warranty. More specific instructions, or procedures of a less general nature, will be included within the assembly text itself.

Under no circumstances should you proceed with an assembly step without fully understanding the procedures involved. A little patience at this stage will save a great deal of time and potential "headaches" later.

3-4. DIODE INSTALLATION INSTRUCTIONS

NOTE: Diodes are marked with a band on one end indicating the cathode end. Each diode must be installed so that the end with the band is oriented towards the band printed on the PC board. Failure to orient the diodes correctly may result in permanent damage to your unit.



DIODE

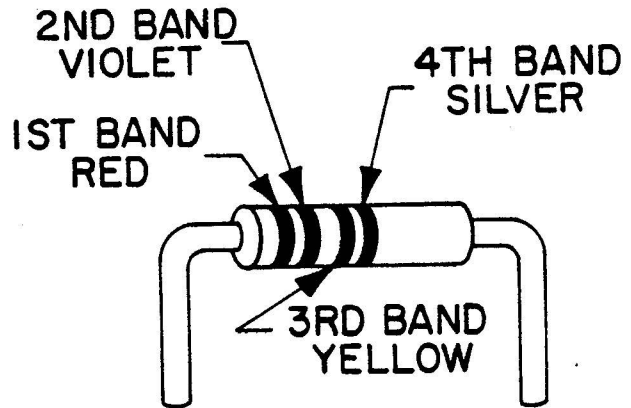
1. Bend the leads of the diode at right angles to match their respective holes on the board.
2. Insert the diode into the correct holes on the silk screen, making sure the cathode end is properly oriented. Turn the board over and bend the leads slightly outward.
3. Solder the two leads to the foil pattern on the back side of the board; then clip off any excess lead lengths.

Use the following procedure to install diodes onto the board. Refer to the list of Diode Part Numbers included for each board to make sure you install the correct diode each time.

3-5. RESISTOR INSTALLATION INSTRUCTIONS

Resistors have four (or possibly five) color-coded bands as represented in the chart below. The fourth band is gold or silver and indicates the tolerance. NOTE: In assembling a MITS kit, you need only be concerned with the three bands of color to the one side of the gold or silver (tolerance) band. These three bands denote the resistor's value in ohms. The first two bands correspond to the first two digits of the resistor's value and the third band represents a multiplier.

For example: a resistor with red, violet, yellow and silver bands has a value of 270,000 ohms and a tolerance of 10%. By looking at the chart below, you see that red is 2 and violet 7. By multiplying 27 by the yellow multiplier band (10,000), you find you have a 270,000 ohm (270K) resistor. The silver band denotes the 10% tolerance. Use this process to choose the correct resistor called for in the manual.



RESISTOR COLOR CODES		
COLOR	BANDS 1&2	3rd BAND (Multiplier)
Black	0	1
Brown	1	10 ²
Red	2	10 ³
Orange	3	10 ⁴
Yellow	4	10 ⁵
Green	5	10 ⁶
Blue	6	10 ⁷
Violet	7	10 ⁸
Gray	8	10 ⁹
White	9	10 ⁹

Use the following procedure to install the resistors onto the boards. Make sure the colored bands on each resistor match the colors called for in the list of Resistor Values and Color Codes given in the assembly instructions.

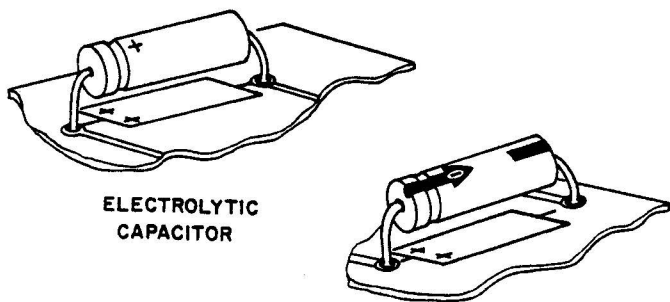
1. Using needle-nose pliers, bend the leads of the resistor at right angles to match their respective holes on the PC board.
2. Install the resistor into the correct holes on the silk-screened side of the PC board.
3. Holding the resistor in place with one hand, turn the board over and bend the two leads slightly outward.
4. Solder the leads to the foil pattern on the back side of the board; the clip off any excess lead lengths.

3-6. CAPACITOR INSTALLATION INSTRUCTIONS

A. Electrolytic and Tantalum Capacitors

Polarity must be noted on electrolytic capacitors and tantalum capacitors before they are installed.

The electrolytic capacitors contained in your kit may have one or possibly two of three types of polarity markings. To determine the correct orientation, look for the following.



One type will have plus (+) signs on the positive end; another will have a band or a groove around the positive side in addition to the plus signs. The third type will have an arrow on it; in the tip of the arrow there is a negative (-) sign and the capacitor must be oriented so the arrow points to the negative polarity side.

The tantalum capacitor is metallic in appearance and smaller than the electrolytic capacitors. Its positive end has a plus sign on it or a red dot.

Install the electrolytic capacitors and tantalum capacitors using the following procedure. Make sure you have the correct capacitor value each time.

1. Bend the two leads of the capacitor at right angles to match their respective holes on the board. Insert the capacitor into the holes on the silk-screened side of the board. Be sure to align the positive polarity side with the "+" signs printed on the board.
2. Holding the capacitor in place, turn the board over and bend the two leads slightly outward. Solder the leads to the foil pattern and clip off any excess lead lengths.

B. Ceramic Disk Capacitors

Install the ceramic disk capacitors using the following procedure. Make sure you have the correct capacitor value each time.

1. Straighten the two capacitor leads as necessary to fit their respective holes on the PC board.
2. Insert the capacitor into the correct holes from the silk-screened side of the board. Push the capacitor down until the ceramic insulation almost touches the foil pattern.
3. Holding the capacitor in place, turn the board over and bend the two leads slightly outward.
4. Solder the two leads to the foil pattern on the back side of the board; then clip off any excess lead lengths.

3-7. IC INSTALLATION INSTRUCTIONS

All ICs must be oriented so that the notched end is toward the end with the arrowhead printed on the PC board. Pin 1 of the IC should correspond with the pad marked with the arrowhead. If the IC does not have a notch on one end, refer to the IC Identification Chart to identify Pin 1.

To prepare ICs for installation:

All ICs are damaged easily and should be handled carefully -- especially static-sensitive MOS ICs. Always try to hold the IC by the ends, touching the pins as little as possible. When you remove the IC from its holder, **CAREFULLY** straighten any bent pins using needle-nose pliers. All pins should be evenly spaced and should be aligned in a straight line, perpendicular to the body of the IC itself.

A. Installing ICs without sockets:

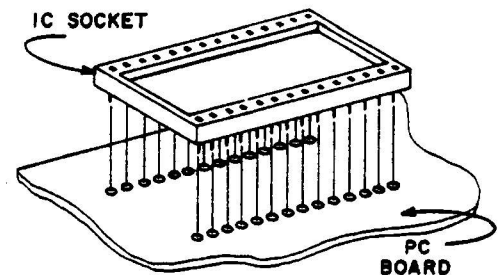
1. Orient the IC so that Pin 1 coincides with the arrowhead on the PC board.
2. Align the pins on one side of the IC so that just the tips are inserted into the proper holes on the board.
3. Lower the other side of the IC into place. If the pins don't go into their holes right away, rock the IC back, exerting a little inward pressure, and try again. Be patient. The tip of a small screwdriver may be used to help guide the pins into place. When the tips of all the pins have been started into their holes, push the IC into the board the rest of the way. Tape the IC to the board with a piece of masking tape.
4. Turn the board over and solder each pin to the foil pattern on the back side of the board. Be sure to solder each pin and be careful not to leave any solder bridges. Remove the masking tape.

WARNING:

Make sure none of the pins have been pushed underneath the IC during insertion.

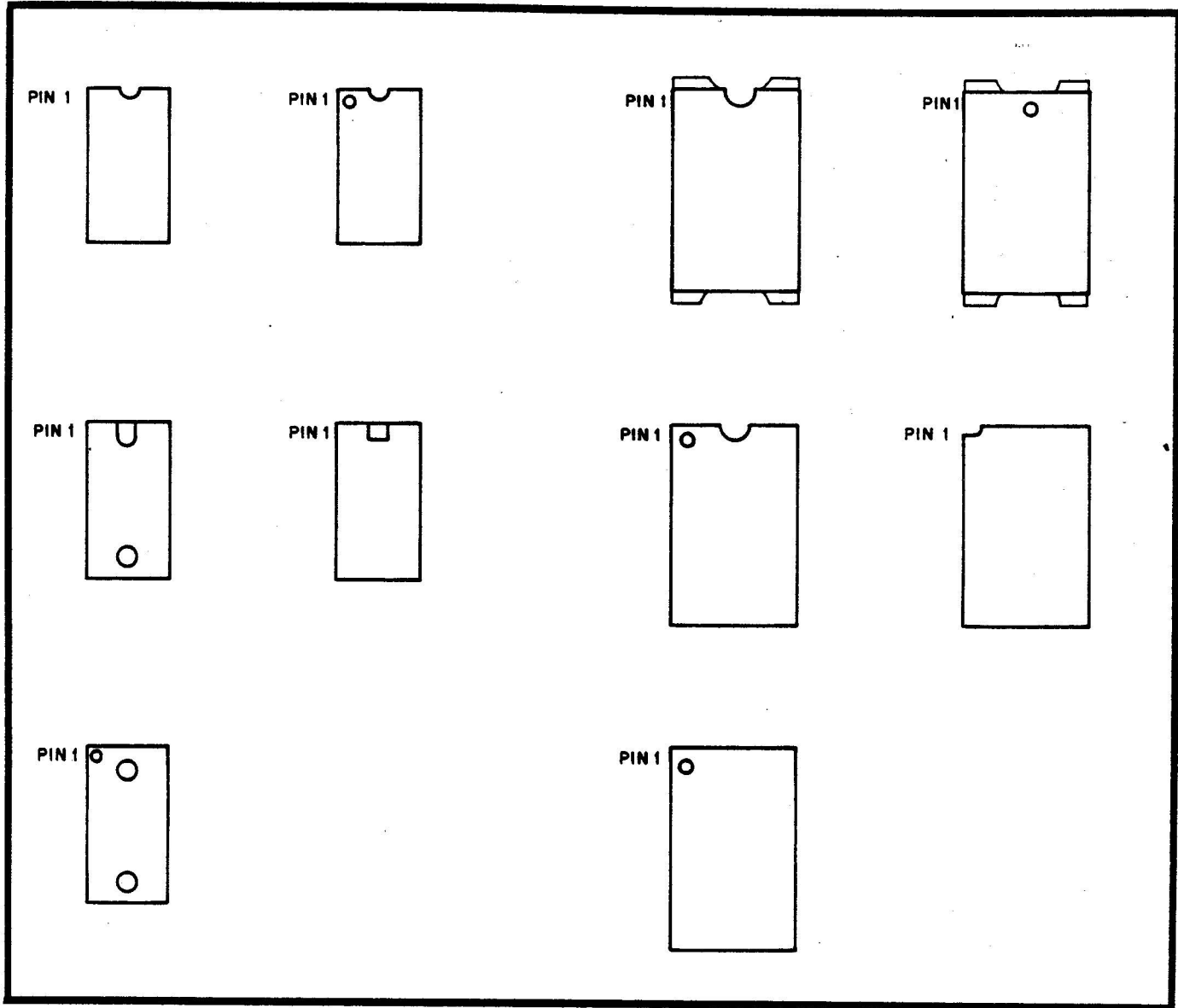
B. Installing ICs with sockets:

1. Referring to the drawing below, set the IC socket into the designated holes on the board and secure it with a piece of masking tape.



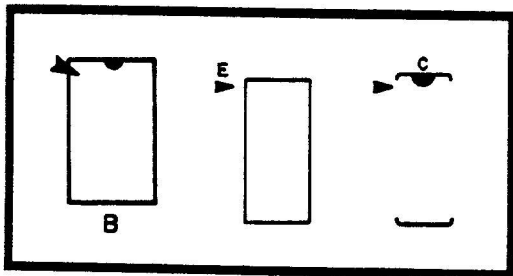
2. Turn the board over and solder each pin to the foil pattern on the back side of the board. Be sure to solder each pin and be careful not to leave any solder bridges. Remove the masking tape.
3. Orient the IC over the socket so that Pin 1 coincides with the arrowhead on the PC board.
4. Align the pins on one side of the socket so that just the tips are inserted into the holes.
5. Lower the other side of the IC into place. If the pins don't go into their holes right away, rock the IC back, exerting a little inward pressure, and try again. Be patient. When the tips of all the pins have been started into their holes, push the IC into the socket the rest of the way.

3-8. IC IDENTIFICATION CHART



INTEGRATED CIRCUITS (IC's) CAN COME WITH ANY ONE OF, OR A COMBINATION OF, SEVERAL DIFFERENT MARKINGS. THESE MARKINGS ARE VERY IMPORTANT IN DETERMINING THE CORRECT ORIENTATION FOR THE IC's WHEN THEY ARE PLACED ON THE PRINTED CIRCUIT BOARDS. REFER TO THE ABOVE DRAWING TO LOCATE PIN 1 OF THE IC's, THEN USE THIS INFORMATION IN CONJUNCTION WITH THE INFORMATION BELOW TO PROPERLY ORIENT EACH IC FOR INSTALLATION.

WARNING: INCORRECTLY ORIENTED IC's MAY CAUSE PERMANENT DAMAGE!



THE DRAWING ON THE LEFT INDICATES VARIOUS METHODS USED TO SHOW THE POSITION OF IC's ON THE PRINTED CIRCUIT BOARDS. THESE ARE SILK-SCREENED DIRECTLY ON THE BOARD. THE ARROWHEAD INDICATES THE POSITION FOR PIN 1 WHEN THE IC IS INSTALLED.

3-9. MOS IC SPECIAL HANDLING INSTRUCTIONS

There are several MOS integrated circuits contained in this kit. These IC's are very sensitive to static electricity and transient voltages. In order to prevent damaging these components, read over the following precautions and adhere to them as closely as possible. FAILURE TO DO SO MAY RESULT IN PERMANENT DAMAGE TO THE IC.

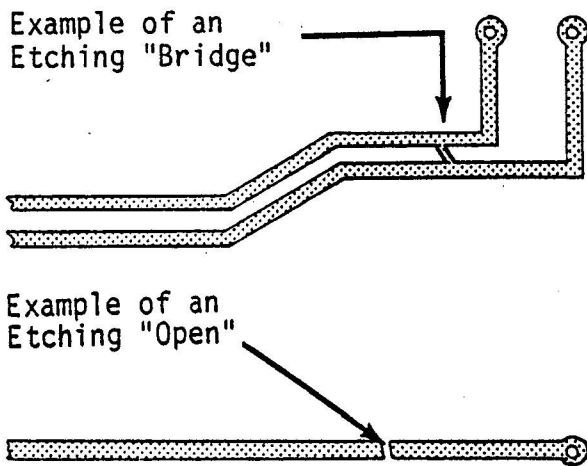
- 1) All equipment (soldering iron, tools, solder, etc.) should be at the same potential as the PC board, the assembler, the work surface and the IC itself along with its container. This can be accomplished by continuous physical contact with the work surface, the components, and everything else involved in the operation.
- 2) When handling the IC, develop the habit of first touching the conductive container in which it is stored before touching the IC itself.
- 3) If the IC has to be moved from one container to another, touch both containers before doing so.
- 4) Do not wear clothing which will build up static charges. Preferably wear clothing made of cotton rather than wool or synthetic fibers.
- 5) Always touch the PC board before touching the IC to the board. Try to maintain this contact as much as possible while installing the IC.
- 6) Handle the IC by the edges. Avoid touching the pins themselves as much as possible.
- 7) Dry air moving over plastic can result in the development of a significant static charge. Avoid placing the IC near any such area or object.
- 8) In general, never touch anything to the IC that you have not touched first while touching both it and the IC itself.

3-10. 680b-BSM 16K STATIC MEMORY BOARD ASSEMBLY

After reviewing the theory of operation, the component installation instructions, and the Assembly Hints Manual, construct the 16K Static Memory Board according to the following instructions.

It is recommended that a visual inspection of the PC Board(s) in your kit be made before beginning the assembly procedures.

Look for etching "bridges" or etching "opens" in the printed circuit lands, as shown in the drawings below:



This could also appear as a "hairline" cut.

A thorough visual inspection will eliminate one possibility for errors, should the board not operate properly after it is assembled. Troubleshooting efforts may then be concentrated elsewhere.

3-11. TERMINAL TEST POINT INSTALLATION (Figure 3-2)

Install the nine test points, TP1 through TP9 (Bag 6), on the 16K Static Memory Board according to the following instructions.

1. Insert the pin through the silk-screened (top) side of the board and solder it in place on the silk-screened (top) side.
2. Turn the board over and solder the pin on the foil (bottom) side of the board.
3. Return the board to the silk-screened (top) side of the board and resolder the pin, straightening it if necessary.

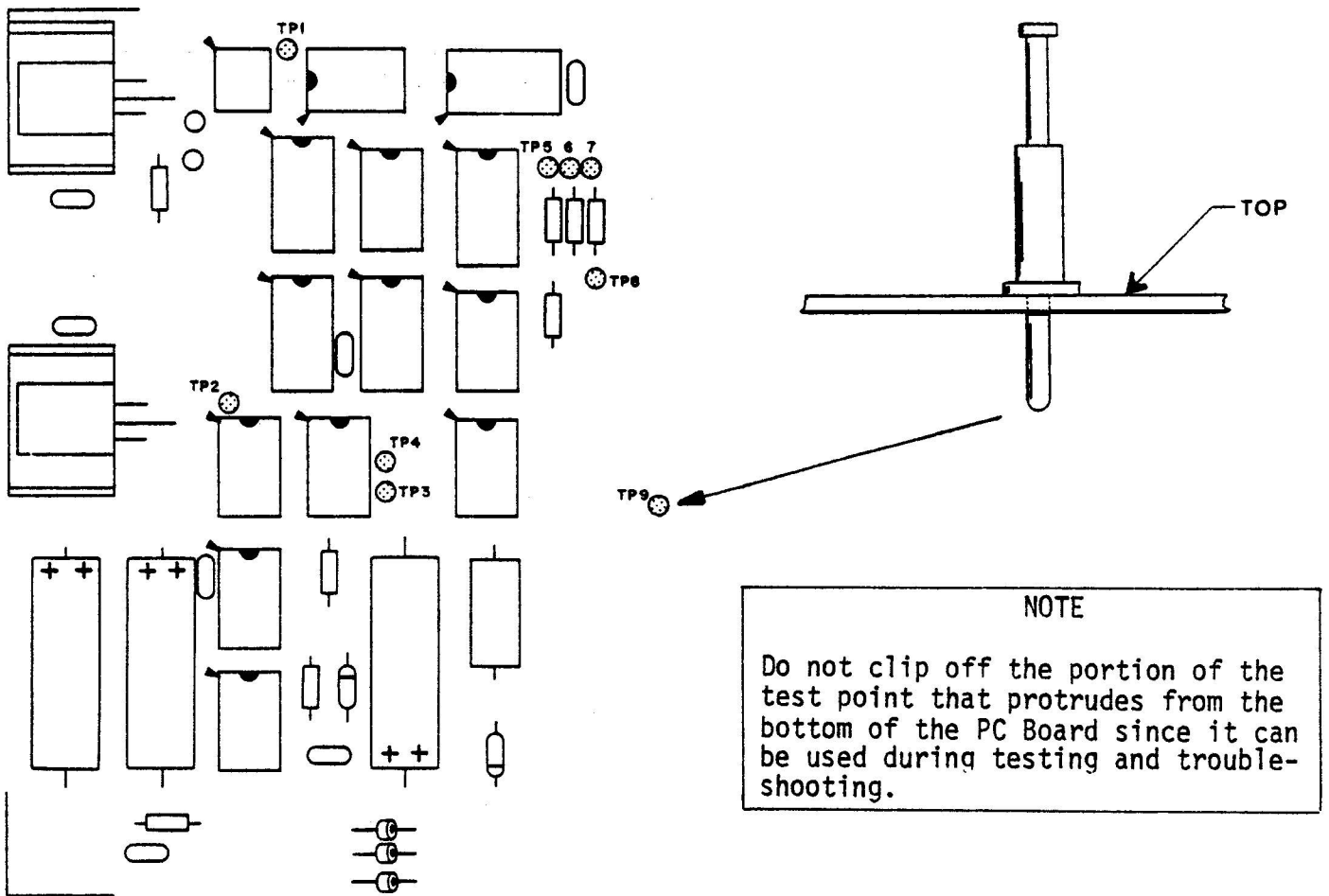


Figure 3-2. Terminal Test Point Installation

3-12. DIODE INSTALLATION (Figure 3-3)

Install the two diodes, D1 and D2 (Bag 5), on the 16K Static Memory Board according to the Diode Installation Instructions on page 3-4.

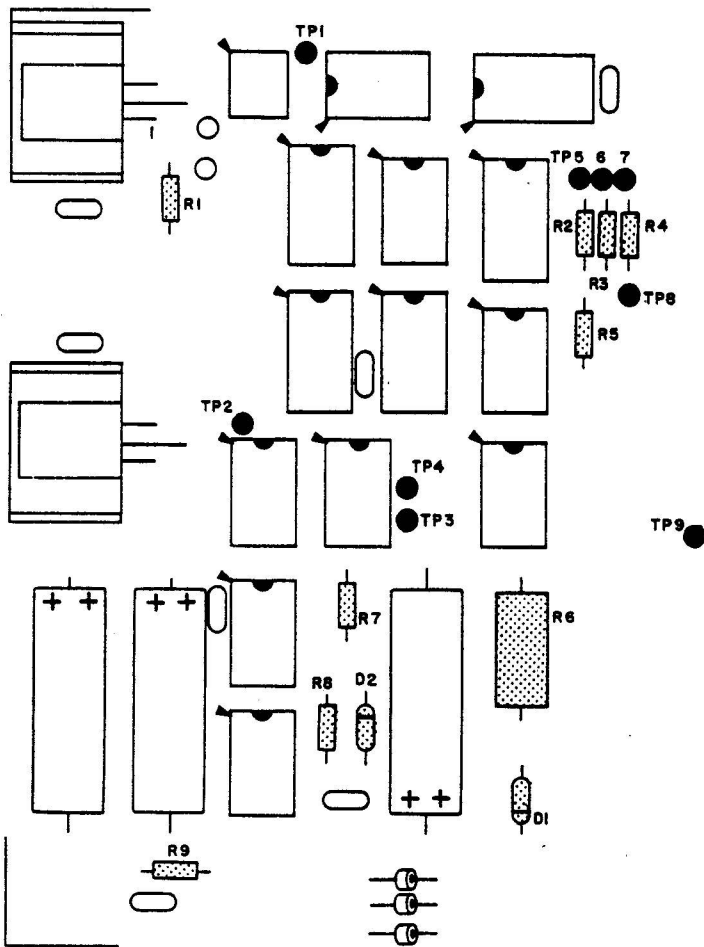
Diode	Part Number
() D1	IN4733, 5.1v Zener
() D2	IN914 or IN4148

3-13. RESISTOR INSTALLATION (Figure 3-3)

Install the following nine resistors, R1 through R9 (Bag 5), on the 16K Static Memory Board according to the Resistor Installation Instructions on page 3-5.

NOTE

Save excess resistor leads for use in the Ferrite Bead Installation, paragraph 3-14.



Resistor Values

- | | |
|--------------------|--|
| () R1, R7 | 2.2K ohm, 1/2w
(red, red, red) |
| () R2, R3, R4, R5 | 330 ohm, 1/2w
(orange, orange, brown) |
| () R6 | 100 ohm, 2w
(brown, black, brown) |
| () R8, R9 | 470 ohm, 1/2w
(yellow, purple, brown) |

Figure 3-3. Diode and Resistor Installation

3-14. FERRITE BEAD INSTALLATION (Figure 3-4)

Install the four ferrite beads, L1 through L4 (Bag 6), on the 16K Static Memory Board according to the following instructions.

1. Using excess resistor leads, cut four 1-inch lead lengths.
2. Insert the lead through the bead and bend the ends so they conform to the designated holes on the 16K Static Memory Board.
3. Insert the leads into the silk-screened (top) side of the board and solder to the foil (bottom) side of the board, being careful not to leave any solder bridges.
4. Clip off any excess lead lengths.

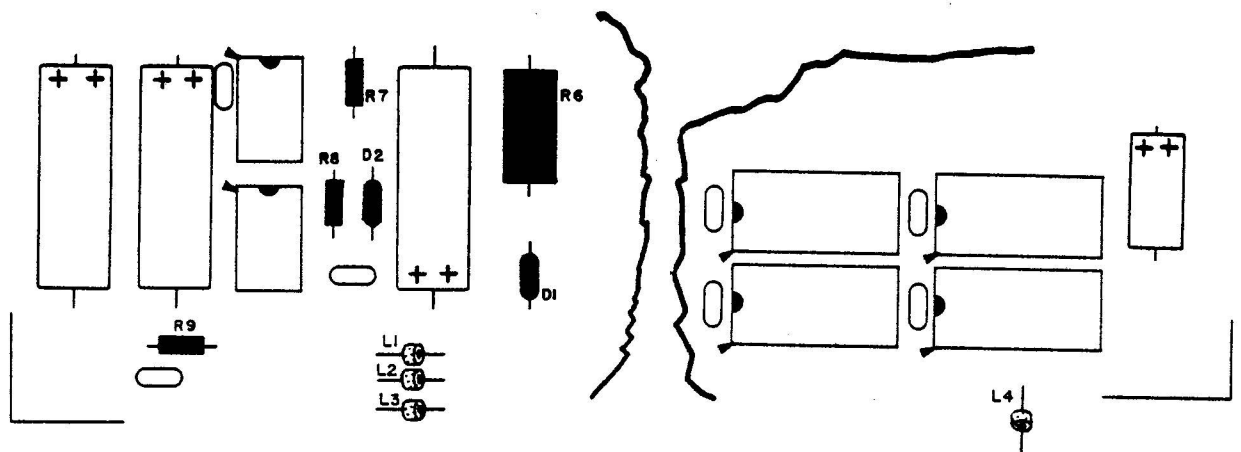


Figure 3-4. Ferrite Bead Installation

3-15. VOLTAGE REGULATOR INSTALLATION (Figure 3-5)

Install the voltage regulators, VR1 and VR2 with heat sinks (Bag 2), on the 16K Static Memory Board according to the following instructions.

1. Set the regulator in place on the silk-screened (top) side of the board, aligning the leads with their designated holes.
2. Use needle-nose pliers to bend each of the three leads at a right angle to conform to its proper hole on the board.

3. Referring to Figure 3-5, set the regulator and heat sink in place on the silk-screened (top) side of the board and secure them with a #6-32 x 3/8" screw and 6-32 nut.
4. Solder the three leads to the foil (bottom) side of the board, being careful not to leave any solder bridges.
5. Clip off any excess lead lengths.

Voltage Regulator	Part Number
() VR1	7812
() VR2	7805

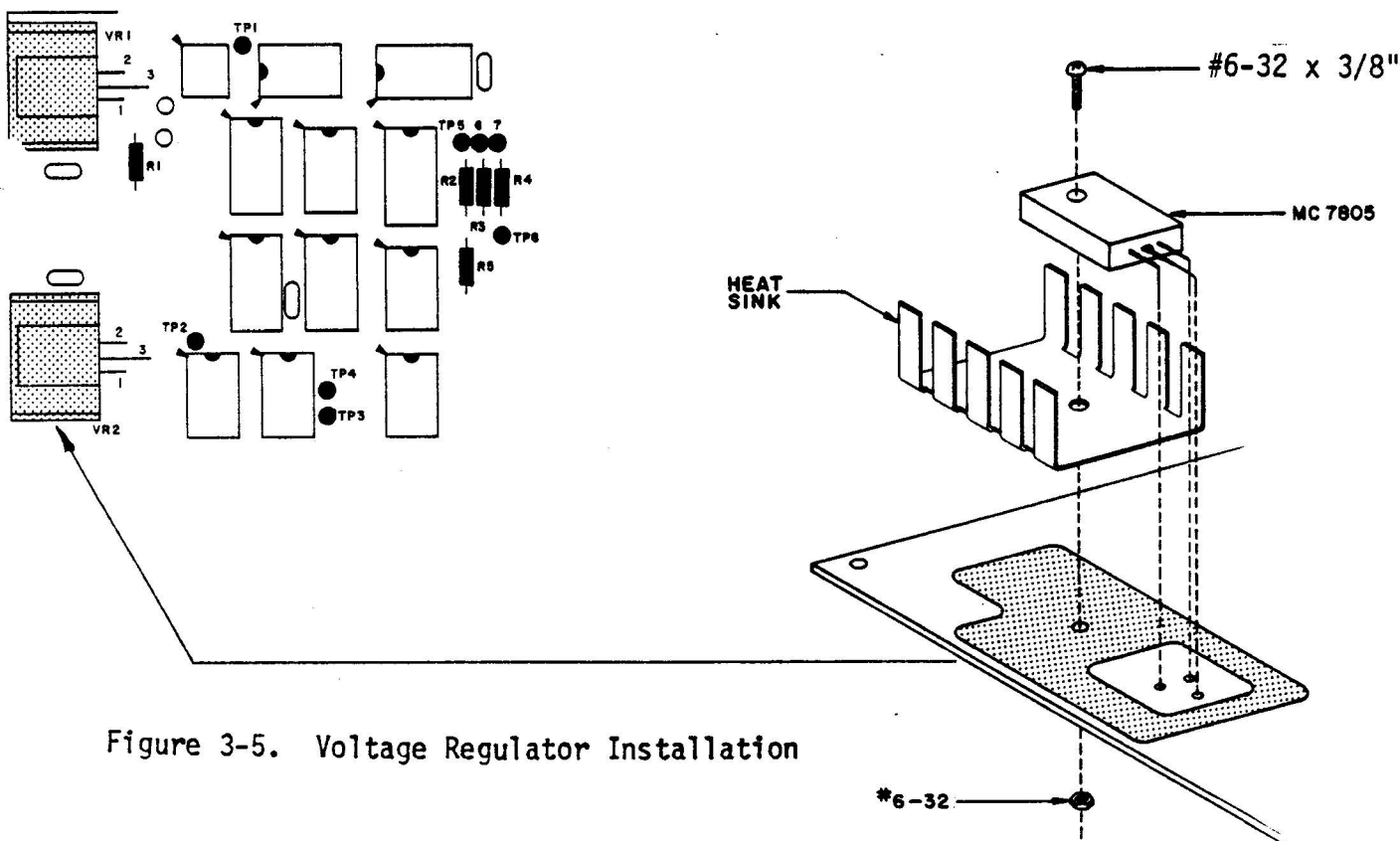


Figure 3-5. Voltage Regulator Installation

3-16. CAPACITOR INSTALLATION (Figure 3-6)

3-17. IC SOCKET INSTALLATION (Figure 3-6)

Install the four ceramic disk and six electrolytic capacitors (Bag 4) on the 16K Static Memory Board according to the Capacitor Installation Instructions on page 3-6.

Install the following forty-five IC sockets (Bags 7 and 8) according to the Integrated Circuit Instructions, Section B, on page 3-7.

Capacitor Values	
() C4,C5	470pf, 500-1Kv ceramic disk
() two capacitors between VR1 and VR2	.1uf, 50v ceramic disk
() C6,C7,C8	33uf or 35uf, 16-35v electrolytic
() C1,C2,C3	470-500uf, 25-35v electrolytic

CAUTION

Insure that solder bridges are not formed.

Socket	Size
() R-A, 0-7	22-pin
() R-B, 0-7	22-pin
() R-C, 0-7	22-pin
() R-D, 0-7	22-pin
() B,C,E,F,G	16-pin
() A,D,H,L,K,J,M,N	14-pin

* IC Socket installed without IC

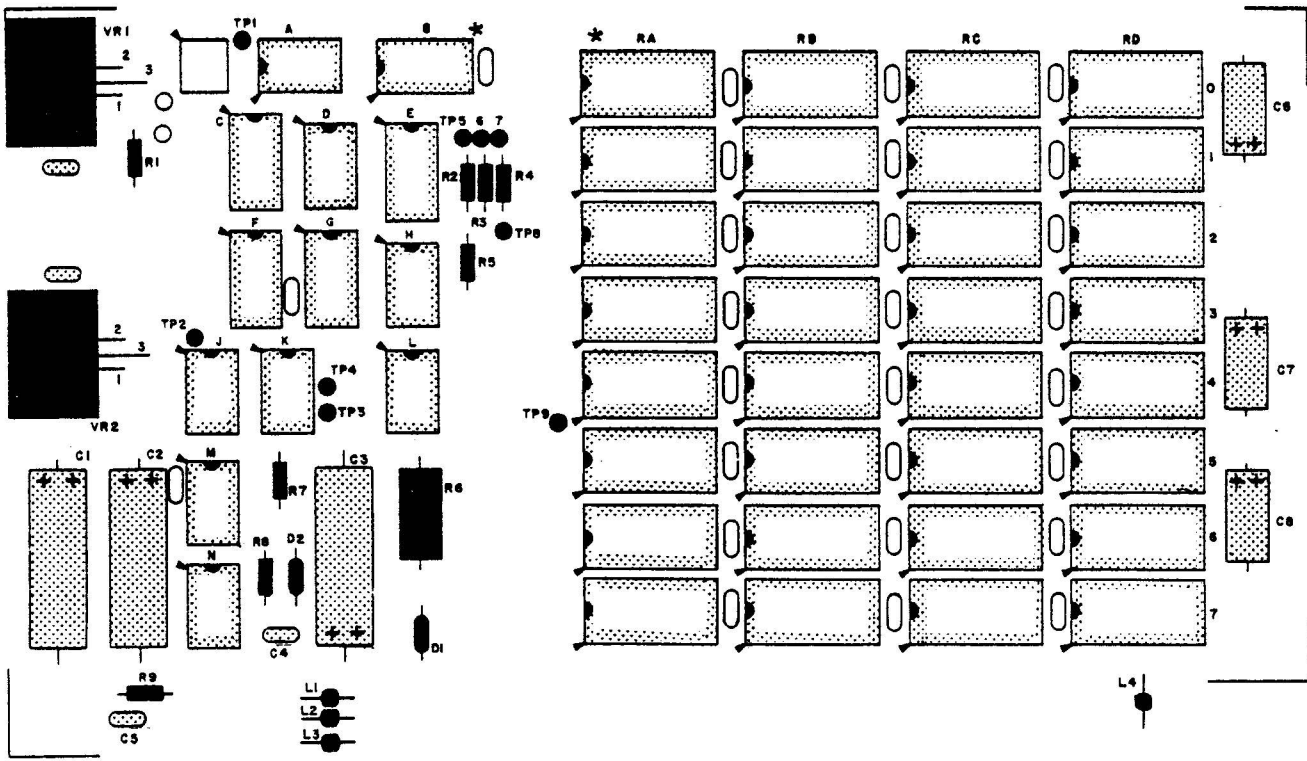


Figure 3-6. Capacitor and IC Socket Installation

3-18. SUPPRESSOR CAPACITOR INSTALLATION
(Figure 3-7)

Install the twenty-seven suppressor capacitors (Bag 3) on the 16K Static Memory Board according to the Capacitor Installation Instructions, Section B, on page 3-6. All of these capacitors are ceramic disk and are marked only by an outline on the silkscreen.

Suppressor Capacitor Values

() 27 suppressor capacitors .1mf, 16v

IC	Part Number
() A	7406
() B,E	74LS75
() C	74LS139 or 93L21
() D	7402 or 74LS02 or 9L02
() F,G	74367 or 8097
() H,L,N	74L04 or 9L04
() J	74L02 or 74LS02 or 9L02
() K	74LS27
() M	74LS74

3-19. IC INSTALLATION (Figure 3-7)

Install the following thirteen integrated circuits (Bag 2) on the 16K Static Memory Board according to the Integrated Circuit Installation Instructions, Section B, on page 3-7.

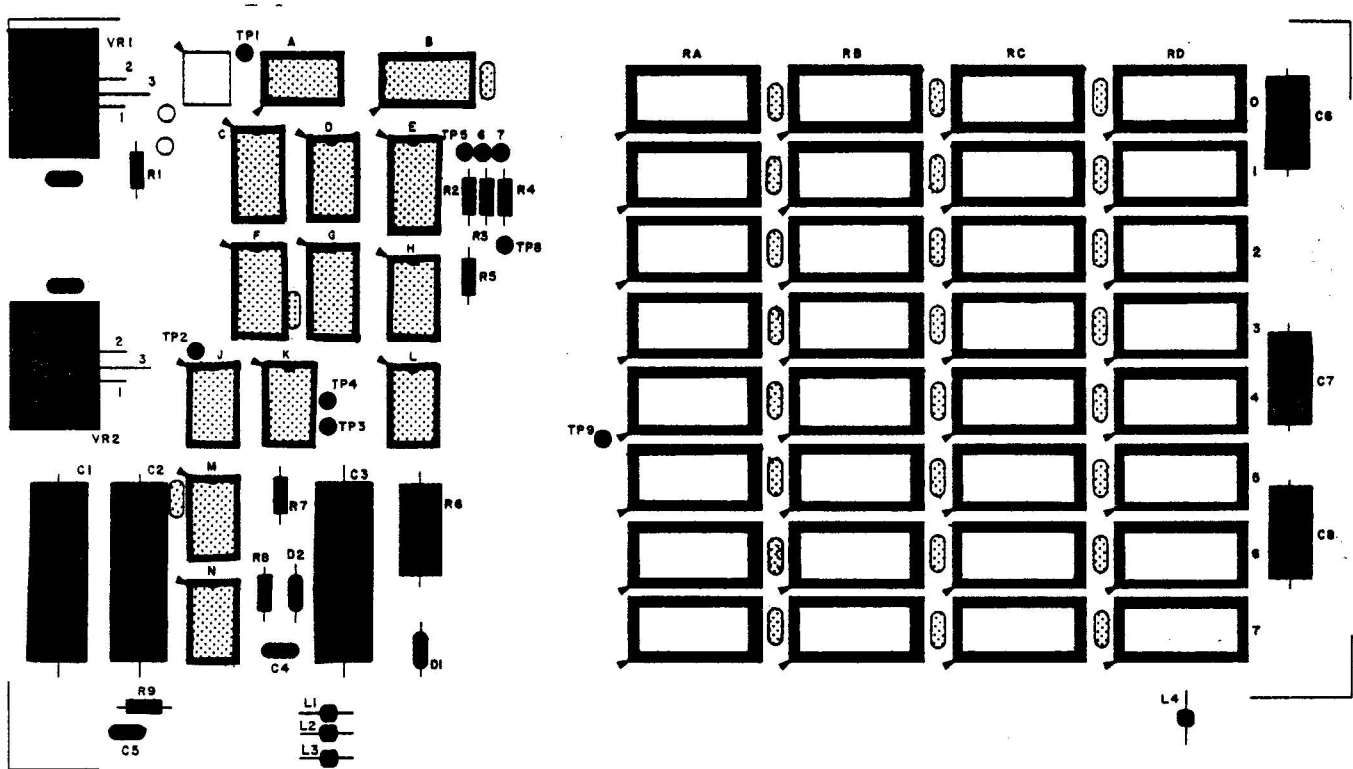


Figure 3-7. Suppressor Capacitor and IC Installation

3-20. ADDRESS SWITCH INSTALLATION (Figure 3-8)

Install the 4-position address switch (Bag 8) on the 16K Static Memory Board according to the following instructions.

1. Remove the 8-pin switch from its holder and straighten any bent pins with needle-nose pliers.
2. Orient the switch so that the numbers 1,2,3,4 line up directly under SW1 as shown in Figure 3-8.
3. Start the pins on one side of the switch into their respective holes on the silk-screened side (top) of the board. DO NOT PUSH THE PINS IN ALL THE WAY. If you have difficulty getting the pins into the holes, use the tip of a small screwdriver to guide them.
4. Start the pins on the other side of the switch into their holes in the same manner and when all the pins have been started, set the switch into place by gently rocking it back and forth until it rests as close to the board as possible.
5. After you are certain that the switch is straight, tape it in place with a piece of masking tape.
6. Turn the board over and solder EACH pin to the foil (bottom) side of the board, being careful not to leave any solder bridges.

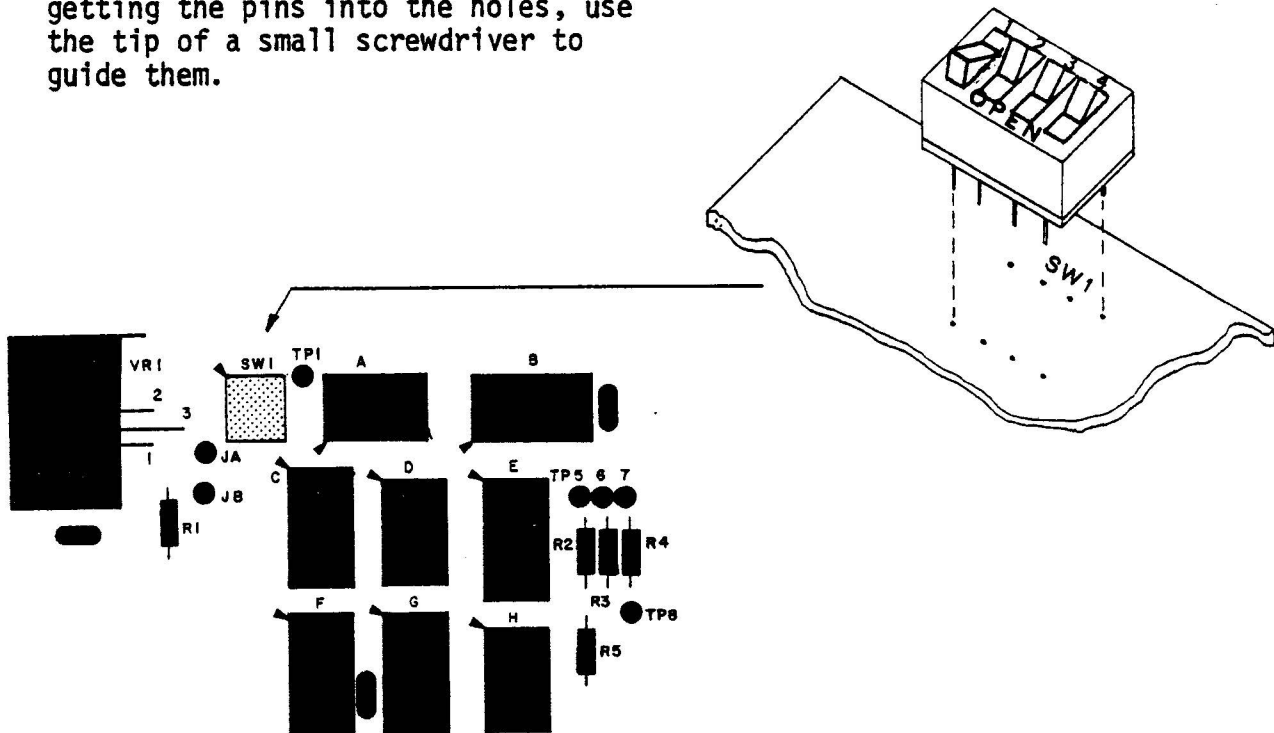


Figure 3-8. Address Switch Installation

3-21. ADDRESS SWITCH SETTING

1. The maximum memory using the 680b-BSM is 49K or three 16K Boards plus the 1K of good internal memory. Always wire the jumpers to the 680b internal 1K memory above the highest 16K board used. Consult your 680b Operators Manual, page 5, for wiring the jumpers to the 1K memory.
2. The configuration of the four-position switch determines the board selection. Only one of the four switches is used to select a particular board. The following chart indicates which switch to place in the "ON" position for the memory location desired. The positioning of the boards on the expander card does not matter as long as each board has a different configuration.

NOTE

A switch pressed toward 1,2,3 or 4 is considered to be ON. A switch pressed toward OPEN is considered to be OFF.

4-Position Switch Configuration*				Memory Location
1	2	3	4	
ON	Off	Off	Off	0 - 15K
Off	ON	Off	Off	16 - 31K
Off	Off	ON	Off	32 - 47K

*For each 16K static Memory Board, use only one switch ON at a time.

3-22. RAM INSTALLATION (Figure 3-9)

Install the thirty-two RAM ICs (Bag 1) on the 16K Static Memory Board according to the Integrated Circuit Instructions, Section B, on page 3-7. Refer to page 3-9 for special handling instructions of the RAMs. Failure to carefully follow these instructions may result in permanent damage to the static-sensitive ICs.

IC	Part Number	Socket Size
() R-A, 0-7	4200	22-pin
() R-B, 0-7		
() R-C, 0-7		
() R-D, 0-7		

NOTE

It is also recommended that a piece of aluminum foil be placed along the card stab connector when installing the ICs so that the pins of the RAMs are at the same potential. This will reduce the possibility of static damage to the RAMs during assembly.

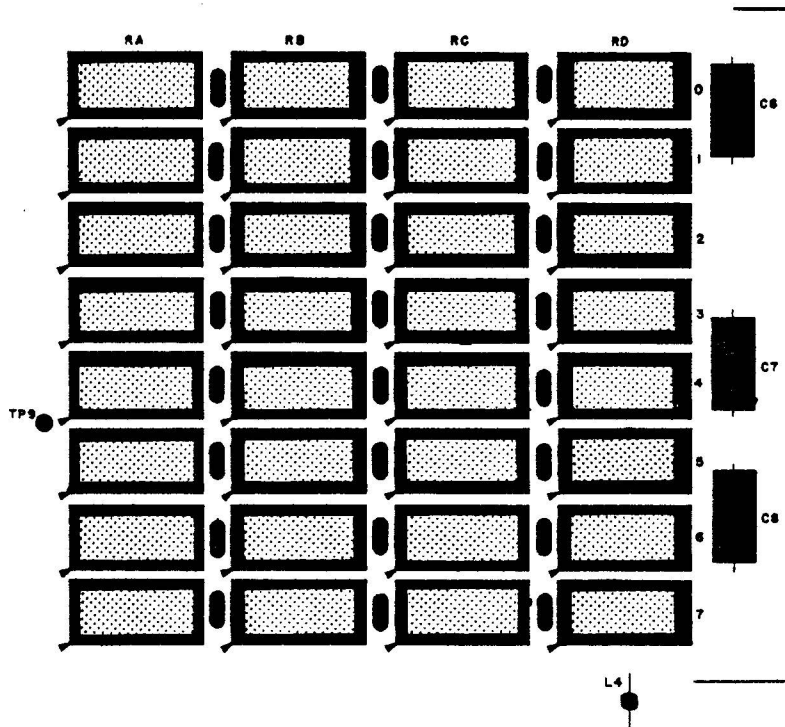


Figure 3-9. RAM Installation

3-23. JUMPER CONNECTION POINTS JA - JB

Points JA and JB will be utilized for future options to be announced.

3-24. 16K STATIC MEMORY BOARD INSTALLATION

Before installing the completely assembled 680b-BSM 16K Static Memory Board (Figure 3-10), refer to Section 2, paragraph 2-10, and perform the visual checks. Make sure the 680-MB Expander Card is correctly installed according to the instructions enclosed with the card. The 16K Static Memory Board is connected to the expander card by means of a 100-pin edge connector and is installed horizontally above the 680b Main Board with two threaded standoffs. Install the completely assembled 16K Static Memory Board according to the following instructions.

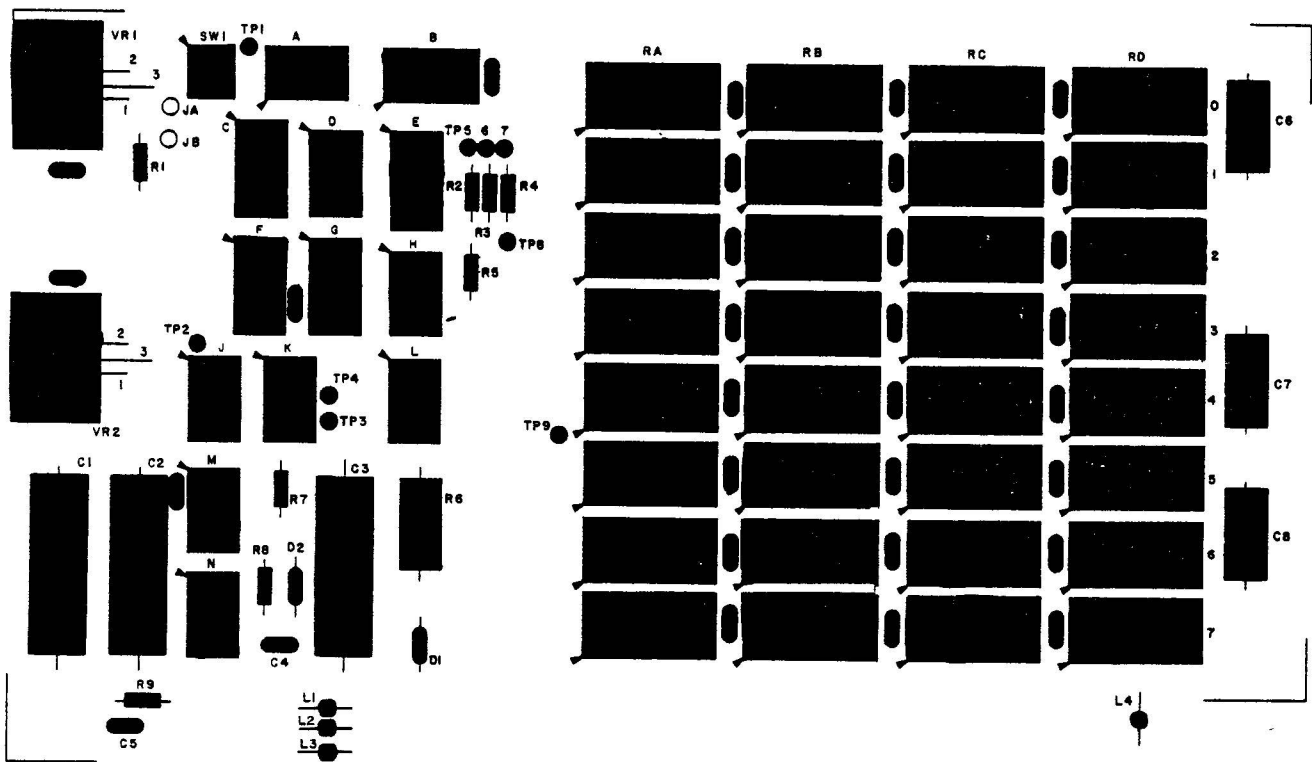


Figure 3-10. Completely Assembled 16K Static Memory Board

A. Installation of 100-pin Edge Connector onto Expander Card (Figure 3-11)

1. Remove the expander card from the socket on the 680b Main Board.
2. Orient the 100-pin edge connector (Bag 8) over the two rows of holes at the lowest unused position on the expander card silkscreen.
3. Insert the connector pins into their respective holes. It may be necessary to guide some of the pins with the tip of a small screwdriver.

NOTE

Insure that the 100-pin connector is tight against the board and that all 100 pins are in their respective holes.

4. Secure the connector to the board with two 4-40 x 1/2" screws and two 4-40 nuts (Bag 6).
5. Solder each pin to the foil (bottom) side of the board.

CAUTION

Insure that solder bridges are not formed.

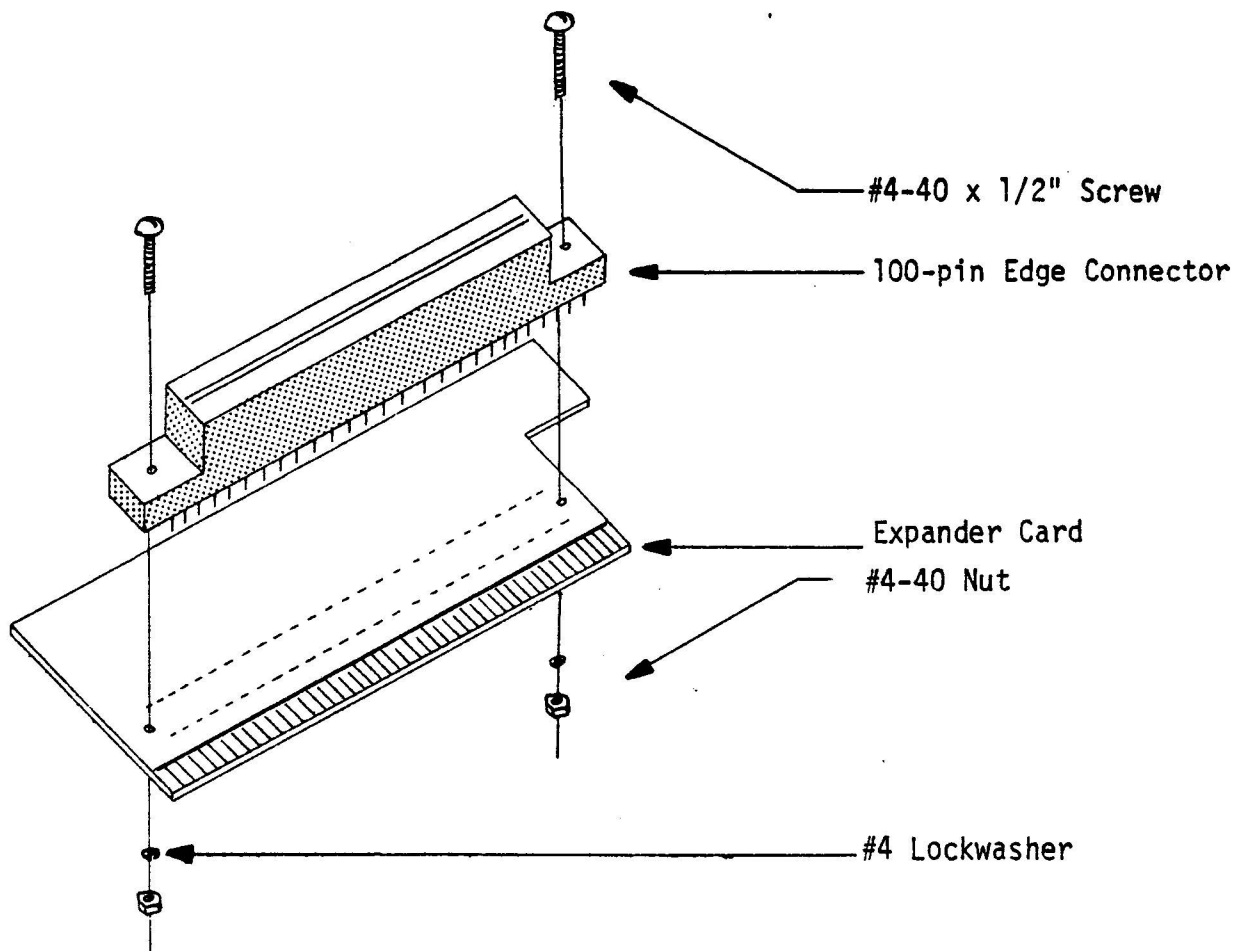


Figure 3-11. Installation of 100-pin Edge Connector onto Expander Card

B. Installation of Threaded Standoffs onto 680b Main Board (Figure 3-12)

NOTE

For installation of a second or third added board, skip "B" and "C" and go to "D".

1. Carefully remove the 680b Main Board from the case.
2. Referring to Figure 3-12, insert a 6-32 x 7/8" threaded standoff with three #6 lockwashers (Bag 6) in the mounting hole provided on each side of the main board.
3. Secure each standoff from the foil (bottom) side of the board with a #6 lockwasher and a 6-32 nut.
4. Properly replace the main board in the case as shown on pages 69-70 in the 680b Manual.

C. Final Installation of the 16K Static Memory Board

1. Replace the expander card into its socket on the 680b Main Board.
2. Insert the card stab connector of the 16K Static Memory Board (silkscreen side up) into the 100-pin edge connector on the expander card.
3. Before securing the 16K Static Memory Board, refer to Section 2, paragraph 2-11, and perform an operational check to insure that the board is operating properly.
4. Secure the board in place by inserting a 6-32 x 3/8" screw with a #6 lockwasher into the top of each of the threaded standoffs as shown in Figure 3-12.

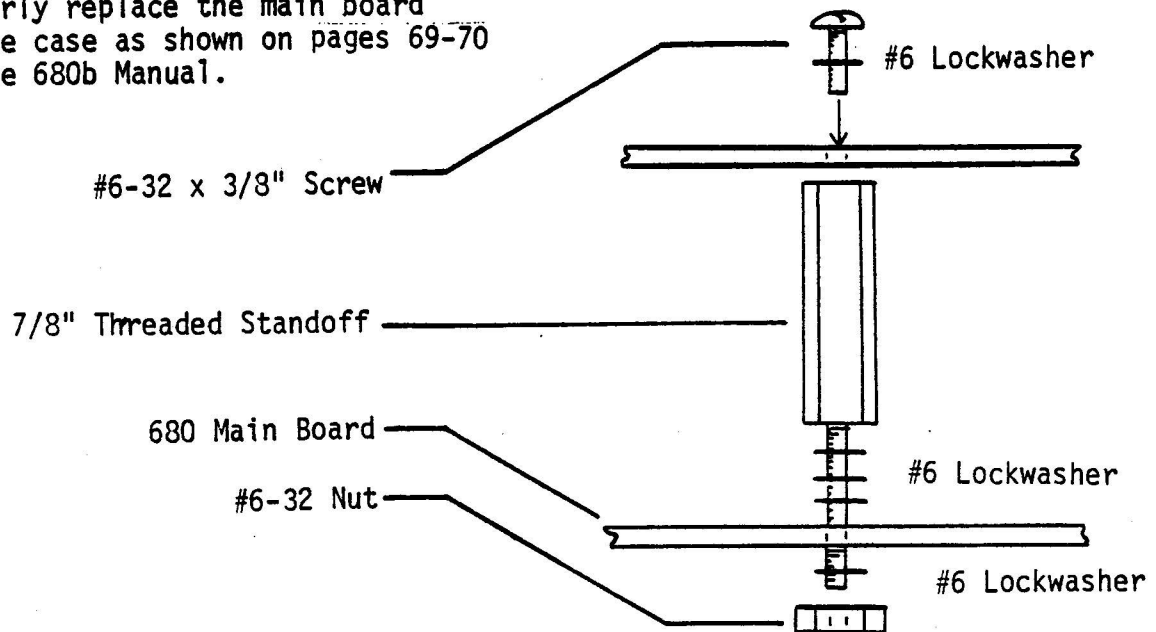


Figure 3-12. Installation of Threaded Standoffs onto 680b Main Board

D. Installation of More Than One Board
(Figure 3-13)

1. If a second or third board is installed, follow the same procedure for installation of the 100-pin edge connector onto the expander card(A).
2. After installation of the 100-pin connector, reinstall the expander card and original card into the 680b Main Board.

3. Replace both 6-32 x 3/8" screws and #6 lockwashers that previously held the lower board with a 6-32 x 7/8" threaded standoff and a #6 lockwasher.
4. Insert the card stab connector of the new board (silkscreen side up) into the 100-pin edge connector.
5. Secure the new board in place with a 6-32 x 3/8" screw and a #6 lockwasher into the top of each of the threaded standoffs.

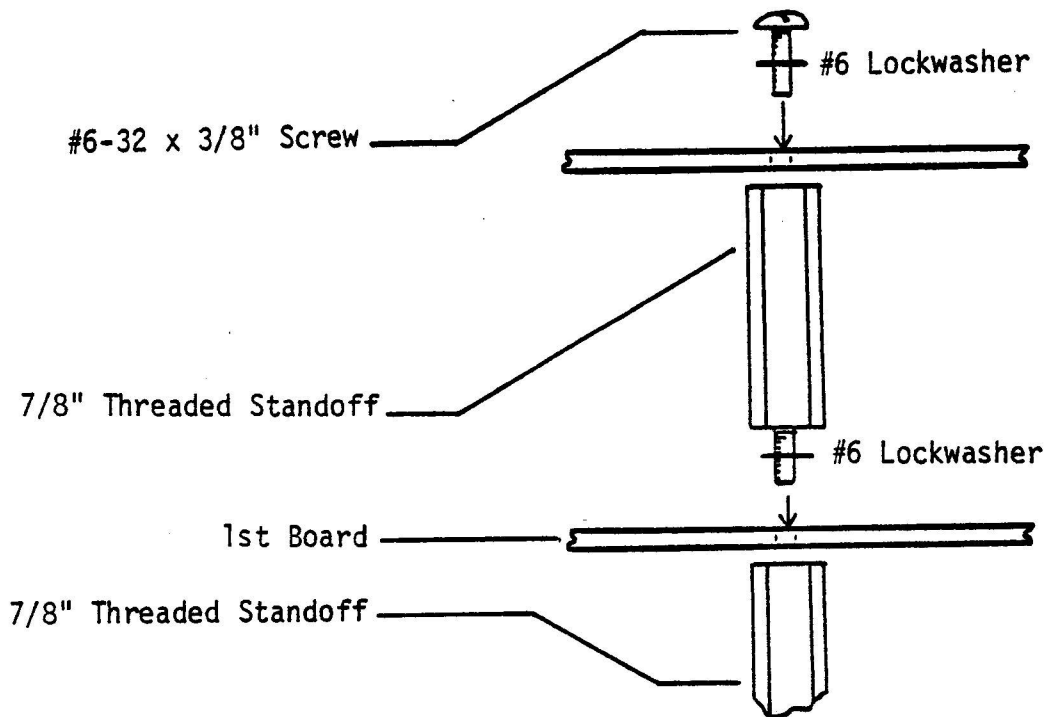


Figure 3-13. Installation of More Than One Board

appendix A

parts list

Bag	Quantity	Component	MITS Stock Number
1	32	4200 RAM Integrated Circuit	101137
2	1	7402 Integrated Circuit	101021
	1	74L02(or 9L02) Integrated Circuit	101072
	1	7406 Integrated Circuit	101054
	3	74L04(or 9L04) Integrated Circuit	101073
	1	74LS27 Integrated Circuit	101103
	1	74LS74 Integrated Circuit	101088
	2	74LS75 Integrated Circuit	101117
	1	74L139(or 93L21) Integrated Circuit	101138
	2	74367(or 8097) Integrated Circuit	101040
	1	7805 Voltage Regulator	101074
	1	7812 Voltage Regulator	101085
3	27	.1uf,16v Suppressor Capacitor	100327
4	2	470pf, 500-1Kv Capacitor	100316
	2	.1uf, 50v Capacitor	100312
	3	33uf, 16v Capacitor	100326
	3	500uf, 25v Capacitor	100318
5	1	100 ohm, 2w Resistor	102009
	4	330 1/2w Resistor	101926
	2	470 ohm 1/2w Resistor	101927
	2	2.2K 1/2w Resistor	101945
	1	IN4733 5v Zener Diode	100721
	1	IN914/IN4148 Diode	100705



6	4	6-32 x 3/8" Screw	100925
	4	6-32 Nut	100933
	12	#6 Lockwasher	100942
	2	6-32 x 7/8" Threaded Standoff	101666
	9	Terminal (Test Point)	101663
	4	Ferrite Bead	101876
	2	Heat Sink(small)	101667
	2	4-40 x 1/2" Screw	100903
	2	4-40 Nut	100932
	2	#4 Lockwasher	100941
7	32	22-Pin Socket	102108
8	1	Dip Switch	102348
	5	16-Pin Socket	102103
	8	14-Pin Socket	102102
	1	100-Pin Edge Connector	101864
MISC:	1	P.C. Board	100203
	1	680b-BSM 16K Static Memory Board Documentation	101576

mits

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