

ROUTINE TO UTILIZE RAM TEST - 3 (FC00)

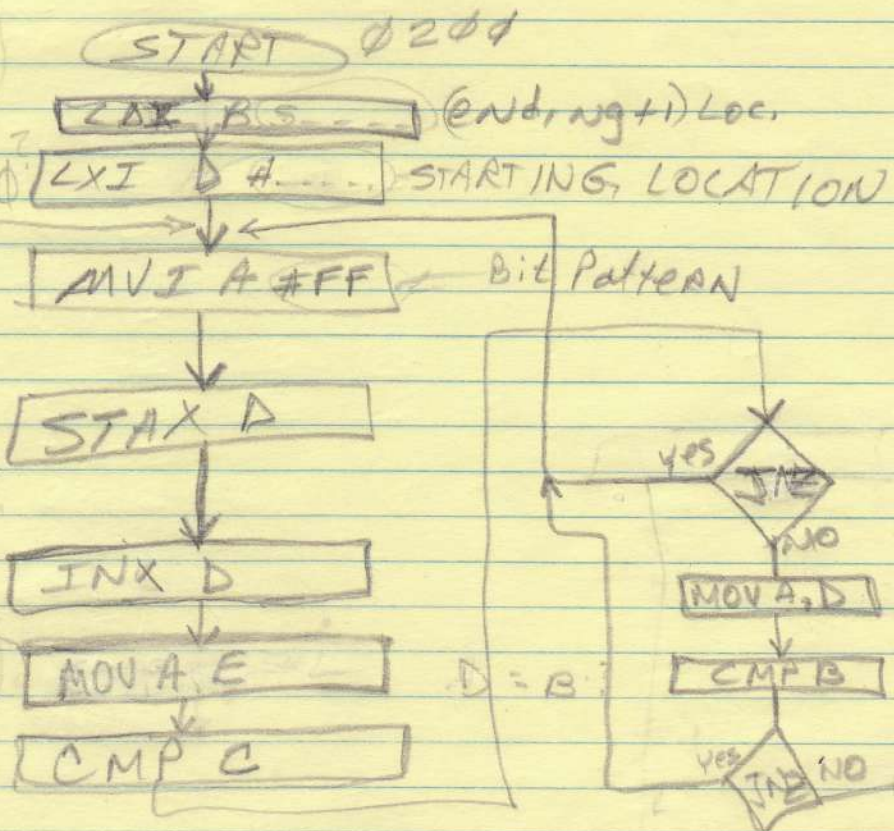


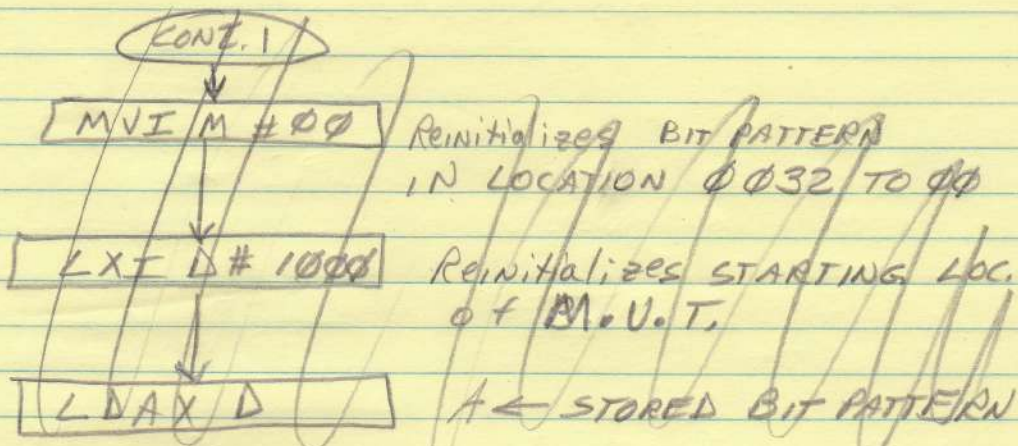
0000	31	FF	01	LXI SP, #01FF
0003	CD	00	FC	call, FC00
0006	76			HLT
0007	00	00		INIT Bcd.
0009	00	10		START CO.
000B	20			END+1 LOC
000C	00			B.P.

10 Subtraction ROUTINE
DE - BC = HL

ROUTINE STORE BLOCK OF BIT PATTERN

A₃ = H
 A₄ = L
 MIN LOW = C
 MIN HI = B
 SUB LOW = E
 SUB HI = D
 DE - BC = 0
 MOV A, E
 CMA
 ADI, #01
 MOV L, A
 MOV A, D
 CMA
 ACI, #00
 MOV H, A
 MOV A, L
 ADD C
 MOV L, A
 MOV A, H
 MOV B, A
 ADC B, A
 MOV H, A





CODING of ROUTINE : STORE BLOCK WITH BIT PATTERN

ADDR	CODE	LABEL	MNEMONIC	COMMENT
0200	01 00 01		LXI B #0100 (ending +1) Loc.	
0203	11 CD 00		LXI D A000 START	
0206	3E FF	STORE	MVI A #FF BIT PATTERN	
0208	12		STAX D STORE	
0209	13		INX D Next Loc.	
020A	7B		MOV A, E	} DE = Bx?
020B	89		CMP C	
020C	C2 06 02		JNZ STORE	
020F	7A		MOV A, D	
0210	B8		CMP B	
0211	C2 06 02		JNZ STORE	
0214	76		HLT Done	

01

MEMORY MAP - ALTAIR 8800

0000	4K RAM	Passed RAM test-2 4K RAM Bd. #1 MITS 88-SK4
0FFF		
1000	4K RAM	Passed RAM test-2 4K RAM Bd #2 MITS 88-SK4
1FFF		
2000	4K RAM	Passed RAM test-2 4K RAM Bd #3 MITS 88-SK4
2FFF		
3000	4K RAM	Passed RAM test-2 4K RAM - Bd. Godbout
3FFF		
4000	1K RAM	Passed RAM test-2 1K RAM Bd. MITS - STATIC Rev. 0
43FF		
4400		
	Presently not used	
	40K BYTES	
		10111001
		EA-1 EB-3 EC-3 FD-1 FE-1 FF-1
DFFF		
E000	PROGRAMMING. PROG. resides IN E000 - E117	BYTESAVE 8K EPROM 2708 WITH PROGRAMMER
	8K EPROM	
FFFF		

E000
FC00

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2-28-81

4K RAM TEST-1

Note: This
Doesn't
TEST
FOR
PATTERN
SENSITIVITY

40 IN M0031 } all
4 00 IN M0030 } MEMORY
CHECKS
OTHERWISE,
Locat'ion of
Bad MEMORY
cell will be
there:
0030 = L BYTE
0031 = H BYTE

```

LXI H #0030  HL = 0030
MVI M #00   M0030 = 00
INX H       HL = 0031
MVI M #40   M0031 = 40
LDI D #1000 DE = 1000
  
```

```

MVI A #88   A = 88
STAX D      MDE = 88
INX D       DE = DE + 1
MVI A #20   A = 20
CMP D       Z↑ if D = 20
              (highest addr. has been stored)
JNZ        All MEMORY STORED
  
```

25 INSTRUCTIONS

```

MVI B #88   B = 88 (MASK)
LXI D #1000 DE = 1000 (STARTING LOC.)
  
```

```

LDAX D      A ← MDE
INX D       DE = DE + 1
CMP B       Z↑ if MEMORY IS NOT 88
JNZ        Restore Addr. HL ← DE
              HL → 0030+31
              XCHG → SHLD → HALT
NO. MEMORY cell checks OKAY
MVI A #20   A = 20
CMP D       Z↑ if D = 20 (highest addr. has
              BEEN READ AND VERIFIED)
JNZ        HALT
  
```

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2-28-81

4K RAM TEST-1

(4000 means all good)
BAD MEMORY CELL LOC.
IN 0030 (L) and
0031 (H)

ADDR	OP CODE			MNEMONIC	COMMENTS
0000	21	30	00	LXI H #0030	HL = 0030
0003	36	FF		MVI M #FF	00 → 0030
0005	23			INX H	HL = 0031
0006	36	FF		MVI M #FF	40 → 0031
0008	11	00	10	LDI D #1000	DE = 1000 ← START OF M.V.T.
000B	3E	88		MVI A #88	88 → A TEST PATTERN
000D	12			STAX D	A → M _{DE} implement
000E	13			INX D	DE = DE + 1 Next LOC
000F	3E	20		MVI A #20	A = 20
0011	BA			CMP D	Z1-TEST for end of STORE
0012	C2	0B	00	JNZ	TO STORE NEXT LOC.
0015	06	88		MVI B #88	ALL DATA STORED, INIT MASK
0017	11	00	10	LXI D #1000	re-initialize MEMORY START LOC.
001A	1A			LDAX D	fetch MEMORY TO VERIFY
001B	13			INX D	NEXT LOC. set UP
001C	B8			CMP B	TEST MEMORY retention
001D	C2	Z1	00	JNZ	JMP TO BAD Mem. cell ROUTINE
0020	3E	20		MVI A #20	MASK = 20
0022	BA			CMP D	Z1-TEST for end of READ
0023	C2	1A	00	JNZ	TO READ NEXT LOC.
0026	76			HLT	DONE - ALL MEMORY GOOD
0027	1B			DCX D	RESTORE BAD cell addr.
0028	EB			XCHG	set up addr. in HL
0029	22	30	00	SHLD	STORE ADDR IN 0030 & 0031
002C	76			HLT	DONE - BAD CELL
002D	00	00	00	NOP	NOT USED
0030					LOC. of L BYTE of Bad cell
0031					LOC. of H BYTE of Bad cell
					(FFFF IN LOC. 0030 & 31 indicate all MEMORY GOOD)

256 RAM TEST-1

BAD MEMORY CELL LOC.
STORED IN 0030 (L)
AND 0031 (H). FFFF
MEANS ALL MEMORY GOOD

ADDR	OP	CODE	MNEMONIC	COMMENTS
0000	21	30 00	LXI H # 0030	HL = 0030
0003	36	FF	MVI M # FF	00 → 0030
0005	23		INX H	HL = 0031
0006	36	FF	MVI M # FF	40 → 0031
0008	11	00 01	LDI D # 0100	DE = START LOC OF M.U.T.
000B	3E	88	MVI A # 88	A = TEST DATA BYTE
000D	12		STAX D	A → MDE (IMPLEMENT WRITE)
000E	13		INXD	INC. TO NEXT LOCATION
000F	3E	02	MVI A # 02	MEMORY END + MASK (STARTS)
0011	BA		CMP D	Z↑ - TEST FOR END OF WRITE
0012	C2	0B 00	JNZ	
0015	06	88	MVI B # 88	ALL DATA STORED, INIT. PATTERN MASK
0017	11	00 01	LXI D # 0100	reinit. START LOC OF M.U.T.
001A	1A		LDAX D	fetch MEMORY TO VERIFY
001B	13		INXD	INC TO NEXT LOCATION
001C	B8		CMP B	TEST MEMORY RETENTION
001D	C2	27 00	JNZ	Go to Bad MEMORY cell ROUTINE
0020	3E	02	MVI A # 02	MEMORY END + 1 MASK
0022	BA		CMP D	Z↑ - TEST FOR END OF READ
0023	C2	1A 00	JNZ	Go to Read next Loc.
0026	76		HLT	DONE - ALL MEMORY good
0027	1B		DCXD	Restore BAD cell addre.
0028	EB		XCHG	set up addr. in HL
0029	22	30 00	SHLD	STORE ADDR IN 0030 & 0031
002C	76		HLT	DONE - BAD cell Identified
002D	00	00 00	NOP	NOT USED
0030				Loc. of L BYTE of BAD cell
0031				Loc. of H BYTE of BAD cell (FFFF, in loc's indicate all MEMORY good)

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 2-28-81
 uses - HL, DE, EC, A
 M 0007-000C

PUSH PSW
 PUSH #
 PUSH D
 PUSH B

- STORES BAD cell Loc. IN 0007(L) and 0008(H).
 - PICKS UP STARTING Loc. OF M.U.T. AT 0009(L) and 000A(H).
 - PICKS UP (ENDING + 1) ADDR. IN 000B(H). THIS PROG. TESTS MEMORY IN 256 BYTE BLOCKS ONLY.
 - B.P. IN 000C

RAM TEST.3
 TO BE IN EPROM FC00x

```

LXI H # 0007
MVI M, # FF
INX H
MVI M, # FF
  
```

INITIALIZES 0007 AND 0008 TO FF

```

LHLD 0009
  
```

HL = STARTING LOC.

```

XCHG
  
```

LOADS D.E. WITH STARTING ADDRESS

```

LXI B, # 000B
  
```

LOC. OF M.U.T.

```

LXI H # 000C
  
```

HL = 0005

```

MVI M, # 00
  
```

INITIALIZES B.P. IN 0004 TO 00

sets BE to loc. of end+1 addr.

```

MOV A, M
  
```

A = CURRENT B.P.

```

STAX D
  
```

STORES B.P. IN M.U.T.

```

LDAX D
  
```

READS BACK B.P. IN M.U.T.

```

CMP M
  
```

checks for correct retention

SNZ

Yes

HL = Bad Cell Loc

```

XCHG
  
```

```

SHLD
  
```

J to Ret. ROUTINE

No

```

INR M
  
```

goes to 0007(L) and 0008(H) next B.P.

```

INR A
  
```

puts current B.P. in Acc.

```

CPI # 00
  
```

checks to see if all 256 BIT PATTERNS have been stored and verified for the current loc. of M.U.T.

SNZ

Yes

No (all have been checked)

(B.P. has turned over 00)

```

INX D
  
```

```

LDAX B
  
```

A = END+1 LOC. (H)

```

CMP D
  
```

SNZ

Yes

No (Yes they have all been tested)

J to Ret. ROUTINE

Ret. ROUTINE

```

POP B
  
```

```

POP D
  
```

```

POP H
  
```

```

POP PSW
  
```

```

RET
  
```

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3-1-81

Tests for bit pattern
sensitivity & retention

RAM TEST 3

- STORES BAD CELL LOC. OF
M.U.T. IN 0009(L) and
0008(H).
- PICKS UP START. LOC. OF
M.U.T. AT 0009(L) and
000A(H).

- OFFENDING B.P.
IN 000C

- PICKS UP (END+1)
LOC. OF M.U.T. AT
000B(H). THIS PROG.
TEST MEM. IN 256 BYTE BLOCKS ONLY

Addr.	OP CODE	LABEL	MNEMONIC	COMMENTS
FC00	F5		PUSH PSW	} SAVES REG. THAT ARE USED ON STACK
FC01	E5		PUSH H	
FC02	D5		PUSH D	
FC03	C5		PUSH B	
FC04	00		NOP	
FC05	21 07 00		LXI H #0007	} INITIALIZES 0007 AND 0008 TO FF
FC08	36 FF		MVI M, #FF	
FC0A	23		INX H	
FC0B	36 FF		MVI M, #FF	
FC0D	00		NOP	
FC0E	2A 09 00		LHLD 0009	HL = STARTING ADDR.
FC11	EB		XCHG	DE = START. LOC. OF M.U.T.
FC12	01 0B 00		LXI B, #000B	BE = LOC. OF (END+1) ADDR.
FC15	21 0C 00		LXI H, #000C	HL = LOCATION OF B.P.
FC18	36 00		MVI M #00	INIT. B.P. IN 000C TO 00
FC1A	00		NOP	
FC1B	7E	STORE	MOVA, M	A = CURRENT B.P.
FC1C	12		STAX D	STORES B.P. IN M.U.T.
FC1D	1A		LDAX D	READS BACK B.P. IN M.U.T.
FC1E	BE		CMP M	CHECKS FOR CORRECT RETENTION
FC1F	C2 32 FC		JNZ ERROR	J if there was an error
FC22	34		INRM	INC. TO NEXT B.P.
FC23	3C		INRA	PUTS UPDATED B.P. IN A
FC24	FE 00		CMP I #00	ALL 256 B.P.'S VERIFIED FOR ^{this} LOC.
FC26	C2 1B FC		JNZ STORE	J if all have not
FC29	13		INXD	INC TO NEXT LOC. OF M.U.T.
FC2A	0A		LDAX B	A = (END+1) LOC. (H) OF M.U.T.
FC2B	BA		CMP D	ALL LOC'S TESTED
FC2C	C2 1B FC		JNZ STORE	J if all have not
FC2F	C3 36 FC		JMP RETURN	if they have, then J to ret.
FC32	EB	ERROR	XCHG	HL = BAD CELL LOCATION
FC33	22 07 00		SHLD #0007	STORES BAD LOC. IN 0007(L) & 0008(H)
FC36	C1	RETURN	POP B	} RESTORES REGISTERS USED
FC37	D1		POP D	
FC38	E1		POP H	
FC39	F1		POP PSW	
FC3A	C9		RET	
FC3B	00		NOP	
FC3C	76		HLT	RETURNS