Altair 88-MDS

Minidisk Documentation
Preliminary

Change Sheet
8800 Minidisk Documentation Preliminary

The following changes should be made in this document:

Page	Change	Date
Controller Board #1 Schematic, Sheet 1 of 3	ICA2 (zone C2) from 74L02 to 74LS02 R5 (zone B3) from 15K to 7.32K, 1% R12 (zone A5) from 33K to 14.7K, 1%	4/20/78
Controller Board #1 Schematic, Sheet 2 of 3	ICA2 (zone D5) from 74L02 to 74LS02 ICA4 (zone B4) from 74L10 to 74LS10 ICG2 (zone D4) from 74L00 to 74LS00	4/20/78

Erratum, December, 1977

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( ) E1, E2 -- 14-pin -- 74L00

CHANGE TO:

( ) E1, E3 -- 14-pin -- 74L00

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3. Reliability Specifications of Minidisk Drive:
   a) Error Rates
      - Soft (recoverable) errors -- 1 per 10^8 bits READ
      - Hard (unrecoverable) errors -- 1 per 10^{11} bits READ
   b) MTBF -- 8000 Hrs. (25% motor run time)
   c) Service Life -- 5 years
   d) Media Life -- 3.0 x 10^6 Passes/Track
4. Power Requirements:
   a) Minidisk Drive Cabinet
      - Standby -- 25 watts, typical
      - Operating -- 35 watts, typical   } 110V or 220V, 60HZ or 50HZ
5. Physical Specifications:
   a) Size: 5" high
             11" wide
             11" deep
   b) Weight: 10 lbs.

1-3. OPTIONS/ACCESSORIES

A. Software:

Altair Minidisk Extended BASIC supplied with 88-MDS. Software on a Write Protected Minidiskette virtually identical to Altair Disk Extended BASIC in operation and features. Manual includes Bootstrap Listing and Read/Write Driver Code.

B. MDBL PROM:

Minidisk Bootstrap Loader on a Programmable Read Only Memory IC to be used with the 88-PMC PROM Memory Card at highest 256-byte block address.

C. DRWT PROM:

Floppy and Minidisk Read/Write Test PROM has the fundamental diagnostic tests for checking hardware operation. To be used with the 88-PMC at 3rd highest 256 byte block address.

D. Miscellaneous:

Minidiskette - Blank, Hard Sectored Diskette, MITS Part Number 102501

Minidisk Drive Service Manual, MITS Part Number 101597

Alignment Diskette (to be used with service manual), MITS Part Number 102502

Altair Minidisk System Operators and Theory Manual, MITS Part Number 101571

Section I
Introduction

1-1. MITS ALTAIR MINIDISK SYSTEM DESCRIPTION

The Altair Minidisk System, used for mass storage of data for the Altair 8800 computer, has a capacity of 71,680 bytes (formatted) per Minidisk with a worst case access time of less than three seconds. A typical system using an Altair computer and Minidisk consists of an Altair 8800 Mainframe, CPU, 32K of memory, I/O Interface, a set of Minidisk Controller Cards and two Minidisk Drives.

The software most commonly used with the Altair Minidisk is Altair Minidisk BASIC, which resides in the lower 24K of memory. Altair Minidisk BASIC includes the standard features of BASIC, plus many extra functions that increase programming power significantly. The Software Driver for the Minidisk Read/Write functions is based on the Hard Sectoring technique, simplifying controller design.

The Altair computer interacts with the Minidisk Drives through two Minidisk Controller Cards that plug into the Altair bus. All Control, Status and Data I/O for the Minidisk System are handled through three I/O ports dedicated to the Minidisk Controller. To insure maximum life of the Drive Motor, a timer in the Controller turns the system off if the Minidisk is not accessed for six seconds.

Inside the Minidisk Drive cabinet is the Power Supply Drive, Line Buffers and Addressing Circuitry, allowing implementation of up to four Drives. The Drive Address is switch selectable, and the selected address is displayed on the front panel for easy identification. WRITE PROTECT is a standard feature in all Altair Minidisk Drives.

1-2. SPECIFICATIONS

A. 88-MDS Altair Minidisk System

The Altair Minidisk System contains a set of two Controller Boards and associated Interconnect Cables and one Minidisk Drive (88-MDDR). The Controller can control one to four Minidisk Drives. The Minidisk Drive case contains the Power Supply, Buffer and Address electronics. Included with the Minidisk Drive are interconnect cable and one blank Minidiskette.

B. 88-MDS Controller Specifications

   1) Number of slots required in 8800 bus - 2

   2) Number of ICs

      - TTL Logic -- 57

      - CMOS -- 1

      - Voltage Regulators - 2

   3) I/O Addresses (Octal) - 010, 011, 012

   4) Data Transfer Rate - 1 byte every 64μs.

   5) Data Format - Hard Sectored (16 sectors)

   6) Interrupt System - Interrupt at beginning of Sector (Optional - not used for Minidisk BASIC)

   7) Power Requirements - 1.4A @ 8V

C. 88-MDDR Drive Specifications

   1. Performance Specifications:

      a) Data Capacity - Hard Sectored Format

         - Per Minidiskette -- 71,680 Data Bytes

         - Per Track -- 2,048 Data Bytes

         - Per Sector -- 128 Data Bytes

      b) Data Transfer Rate - 125,000 Bits Per Second

      c) Access Time

         - Disk Enable to READ or WRITE (Function of motor start-up time) -- 1 sec. (min)

         - Track to Track -- 50 ms.

         - Average Access Time (including motor start-up time) -- 1.85 sec.

         - Worst Case Access Time -- 2.9 sec.

         - Worst Case Latency -- 200 ms.

   2. Functional Specifications:

      a) Rotational Speed -- 300 rpm (200 ms/rev.)

      b) Track Density -- 48 Tracks per inch

      c) Number of Tracks -- 35

      d) Number of Sectors -- 16

      e) Time Per Sector -- 12.5 ms.

Section II
System Installation

2-1. MINIDISK DRIVE INSPECTION AND DRIVE ADDRESS SELECTION

A. Inspection

After unpacking the Minidisk Drive and before the unit is plugged in, take the case top and back panel off by removing the two bottom corner screws on the back panel. Slide the case top back about 1 inch and tilt it away from the chassis, leaving the wiring connected. Remove the Drive PC board from its mounting clips (if still attached) and observe the stepper cam disk with the spiral groove in it. Check the cam follower stylus attached to the head assembly and be sure the stylus is seated in the groove. The cam disk may be manually rotated to check the follower tracking. Re-install the Drive PC board in the mounting clips, making sure the interconnect wiring does not interfere with the mechanism.

B. Drive Address Selection

The Drive Address may be set to one of four addresses by switch SW-1 mounted on the Buffer PC board. Positions 1 and 2 of SW-1 select the addressing circuit and positions 3 and 4 select the address displayed on the front panel. Table 2-A lists the address switch positions.

Table 2-A. Drive Address Selection

Address	1	2	3	4
0	down	down	down	down
1	up	down	up	down
2	down	up	down	up
3	up	up	up	up

After setting the desired address, check the wiring to insure there is no interference with the mechanism or installation of the case top. Re-install the Drive case top and attach with the two screws removed in the previous section.

2-2. INSTALLING THE CONTROLLER

The Minidisk Controller boards are installed in the Altair 8800 chassis with the interconnect cable attached. The following section describes the procedure for installing the PC boards and connectors:

A. Parts Required
    1. Disk Board #1 (Horizontal and vertical rows of ICs).
    2. Minidisk Board #2 (50-pin connector on right edge of card)
    3. Interconnect cable (50-pin socket on one end, PC board and connector on the other end)
    4. 26-pin bulkhead connector (pins on both sides)
    5. 2 each #4-40 x 1/2 inch screw, #4-40 nut, and #4 lockwasher (for mounting item "d" in chassis back panel)

B. Installation of 26-pin Bulkhead Connector

With the Altair 8800 computer unplugged from the power outlet and the top cover removed, install the 26-pin bulkhead connector on the outside of the Altair back panel using the #4-40 hardware supplied. If the connector shell does not fit in the small rectangular holes in the back panel, split the connector shell in half. Mount the half shell with the pins attached on the outside of the computer back panel and the unprotected pins should point towards the inside of the computer. The other half shell is not used.

Be sure to mount the connector with the colored marker indicating pin 1 on the top left side of the shell as viewed from the rear of the Altair computer, matching up with the cable it connects to.

C. PC Board and Cable Installation

Take the end of the interconnect cable with the small circuit board attached and connect it to the 10 and 20 pin right angle connector on Disk Board #1. The small PC board should be oriented so that the flat cable connector is on the top (component) side of the board, and the angled corner is at the lower right corner. Disk Board #1 may be placed in the bus, leaving one space to the right for Minidisk Board #2. Place Board #1 in a position where there is minimum interference with the connector PC board.

Install the 50-pin socket connector to the matching 50-pin connector on Minidisk Board #2, noting the colored markers or small triangles indicating pin 1. Plug Minidisk Board #2 into the Altair bus to the right of Board #1, making sure there is no interference with the cables.

Connect the end of the cable with the 26-pin socket to the bulkhead connector, noting that the two blank pins are #25 and #26, and the colored marker or small triangle indicates pin 1.

This completes installation of the Minidisk Controller.

2-3. CONNECTING THE MINIDISK DRIVE

The Minidisk Drive is connected to the Altair 8800 by a 26 conductor cable containing 26-pin sockets on both ends. The end of the connector with the colored marker, small triangle or wire with dark blue stripe indicates the pin 1 end and should be aligned with the marked end of the bulkhead connector on the Altair chassis. The other end of the cable connects to either one of the bulkhead connectors on the Drive back panel. Pin 1 of the connector on the Drive back panel is indicated by the colored marker and should always be the top end. When connecting Drives together, either back panel connector may be used, being sure that pins 1 of the connectors are oriented the same way. The cable for the 88-MDS is approximately 6 feet long. It should be used for interconnecting the Altair computer to the Drives. The cable supplied with the 88-MDDR Drive is approximately 1 1/2 feet long and is intended for Drive to Drive connection. The interconnect cables should be kept away from power wires and excess cable rolled up and held with a rubber band.

Note that the use of the bulkhead connectors reverses the orientation of wires in the interconnect cable so that the top wire (blue stripes) is connected to pin 2 and the second wire is connected to pin 1, etc. Since there are bulkhead connectors on each end of the interconnect cable, there are two sets of reversals, thereby connecting 1 to 1, 2 to 2, etc.

Section III
Using the
Minidisk System

3-1. GENERAL INSTRUCTIONS

A. Minidisk Drive

The power switch is located on the back panel near the middle of the top edge. The up position is ON as indicated by the POWER indicator on the front panel; the down position is OFF.

The fuse is located near the middle of the bottom edge of the back panel and is a 1 amp, 3 AG slow blow fuse for 110v operation. For 220v applications use a 1/2 amp, 3 AG slow blow fuse.

Unless otherwise specified, the Drive Power Supply will be wired for 105 - 130V, 50/60HZ operation. The Drive Power Supply may be rewired for 210 - 260V, 50/60HZ operation if required (consult Figure 4-16).

WRITE PROTECT is a standard feature of the Altair Minidisk Drive. An unprotected Minidiskette has a notch on one side that allows a switch to close, enabling the Write Circuit when selected. To WRITE PROTECT the Minidiskette, apply a piece of tape around the edge of the Minidiskette and over the notch. This prevents enabling of the Write Circuit by blocking the switch closure. The WRITE PROTECT indicator will illuminate only when the Drive is enabled.

When inserting the Minidiskette into the Drive, open the door on the Drive front panel by lifting up on the square tab. Insert the Minidiskette with the label side up (towards the open door tab). The oval slot in the jacket is inverted first. A mechanical interlock prevents the door from closing if the Minidiskette is improperly inserted.

There is an indicator on the front panel of the Drive. When the Drive is enabled, this indicator will illuminate, indicating that data transfers are taking place. When this light is on, do not attempt to open the Minidisk Drive door because data on the Minidiskette may be lost.

B. Minidiskette

The Minidiskette used in the 88-MDS is Hard Sectored with 16 Sector holes and one Index hole. Mindiskettes are available from MITS (part number 102501) or may be purchased from your local Altair dealer.

The Altair Minidisk BASIC Diskette supplied with the unit is WRITE PROTECTED and is used only for loading Altair Minidisk BASIC. For saving programs or data on a blank Minidiskette, it must first be initialized (see section 3-5, System Operation with Minidisk BASIC).

There are several handling precautions for the Minidiskette. The procedures are as follows:

1. Return the Minidiskette to the storage envelope when not in use. Do not leave it in the Drive.

2. Keep the Minidiskette away from magnetic fields including flourescent lamps, power transformers, or materials such as steel that may become magnetized.

3. Use only a felt tip pen to write on the jacket. Do not use a ball point pen or pencil.

4. Keep Minidiskette free from particulate matter such as dust and cigarette ashes.

5. Keep Minidiskette away from sunlight or heat.

6. Do not touch the Minidiskette surface or attempt to clean it (the inside of the Minidiskette jacket has self-cleaning properties).

C. <u>Controller Boards</u>

The I/O address for the Minidisk Controller is the same as the Floppy Disk Controller (88-DCDD). Thus, the Minidisk and Floppy Disk Systems should not be used in the same Altair computer simultaneously.

Minidisk Controller Board #2 has a timer circuit that turns off the Minidisk system 6.4 seconds after the last Minidisk access to minimize wear on the Drive. The timer circuit uses the Sector pulses from the Drive as the time base and requires the 16 Sector (Hard Sectored) Minidiskette for proper operation.

3-2. LOADING MINIDISK BASIC

To use Minidisk BASIC, a WRITE PROTECTED Minidisk BASIC Diskette, a bootstrap loader which is available in several different forms, and an Altair 8800 computer with a minimum 24K of memory is required. The various methods and options for loading Minidisk BASIC are listed below. The Drive must be addressed to 0 and a Minidisk BASIC Diskette must be in the Drive before loading is started. If errors occur during loading, see section 3-3.

A. Loading Options

1. MDBL PROM (used with 88-PMC)

The MDBL PROM allows loading of Minidisk BASIC by examining its starting location (highest 256 byte block 177400_8), selecting the desired I/O device by setting the sense switches and pressing the RUN switch on the Altair 8800 front panel. Altair Minidisk BASIC will then load and respond with the initialization dialog (see section 3-5 for initialization dialog explanation). Table 3-A contains the I/O Sense Switch settings for the MDBL PROM.

Table 3-A. Sense Switch Settings

Sense switches (switches A8 through A15) must be set before tape or cassette loading begins. The settings depend on the terminal and input interface boards in use. The low order (rightmost) four switches determine the loading I/O board and the high order four switches determine the terminal I/O board setting. In the table below the setting is given for each I/O board option. The setting is also an octal number which signifies the switch positions. The Terminal Switch and Load Switch columns show the switches that are raised for each of the load and terminal device options.

Device	Sense Switch Setting	Terminal Switches	Load Switches	Channels
2SIO (2 stop bits)	Ø	none	none	2Ø, 21
2SIO (1 stop bit)	1	A12	A8	2Ø, 21
SIO	2	A13	A9	Ø, 1
ACR	3	A13, A12	A9, A8	6, 7
4PIO	4	A14	A10	4Ø, 41, 42, 43
PIO	5	A14, A12	A1Ø, A8	4, 5
HSR	6	A14, A13	A1Ø, A9	46, 47
non-standard terminal	14			
no terminal	15			

Example 1:
Input from audio cassette through ACR and CRT terminal through 2SIO with 1 stop bit.

Switch	15	14	13	12	11	1Ø	9	8
Position	Ø	Ø	Ø	1	Ø	Ø	1	1

Example 2:
Input from high speed paper tape reader, terminal through SIO.

Switch	15	14	13	12	11	1Ø	9	8
Position	Ø	Ø	1	Ø	Ø	1	1	Ø

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2. Minidisk Boot Loader on Audio Cassette Tape (used with 88-ACR)

   a) Using the MBL PROM (use with 88-PMC)

      (1) Examine Address Location 177400_8. 177000

      (2) Set sense switches for the 88-ACR according to Table 3-A.

      (3) With the tape in the recorder and the recorder connected, start tape in PLAY mode.

      (4) Wait 10 seconds and press RUN switch on the Altair computer front panel.

      (5) The initialization dialog is printed when BASIC is loaded (see section 3-5).

   b) Toggling In Loader Program

      (1) Load the following program in the computer:

          Loading from cassette

Octal Address	Octal Data
000	041
001	302
002	077
003	061
004	022
005	000
006	333
007	006
010	017
011	330
012	333
013	007
014	275
015	310
016	055
017	167
020	300
021	351
022	003
023	000

(2) Examine address 000.

(3) Set sense switches (refer to Table 3-A).

(4) With tape in recorder and the recorder connected, start tape in PLAY mode.

(5) Wait 10 seconds and press RUN switch on the Altair computer front panel.

(6) The initialization dialog is printed when BASIC is loaded (see section 3-5).

3. Using the Paper Tape Minidisk Boot Loader

a) With the MBL PROM (use with 88-PMC)

(1) Examine address 000.

(2) Set Sense Switches for the input interface board in use (refer to Table 3-A in this section).

(3) Start paper tape on leader.

(4) Press RUN switch on the Altair computer front panel.

(5) BASIC will load and then respond with the initialization dialog (see section 3-5).

b) Toggling in the Boot Loader Program

> **NOTE**
>
> It is assumed that the 2SIO interface board is used. However, if another interface board is used, the loader programs may be found on pages 96 through 99 of the Altair BASIC Reference Manual (version 4.0).

(1) Load the following program in the computer:

Loading with the 2SIO board

Octal Address	Octal
000	076
001	003
002	323
003	020
004	076
005	021 (=2 stop bits, 025=1 stop bit)
006	323
007	020
010	041
011	302
012	077
013	061
014	032
015	000
016	333
017	020
020	017
021	320
022	333
023	021
024	275
025	310
026	055
027	167

(2) Examine address 000.

(3) Set sense switches according to Table 3-A in this section.

(4) Start paper tape on leader.

(5) Press RUN switch on Altair computer front panel.

(6) The initialization dialog is printed when BASIC is loaded (see section 3-5).

A. Error Codes

    1. Error Detection

        The checksum loader turns on the Interrupt Enable light on the front panel when a loading error occurs. The ASCII Code of the error letter is stored in location 0. In addition, the error letter is sent to all the terminal channels. The error letters are as follows:

        C   checksum error. Bad tape data. Indicates a defective Minidiskette (hard error) or alignment problems.

        M   memory error. Data will not store properly. Indicates a defective or nonexistent memory location. The address or the bad memory location is stored in locations 1 and 2.

        O   overlay error. An attempt was made to load data on top of the loader.

        I   invalid load device. Invalid setting on the sense switches.

    2. Miscellaneous Difficulties

        Check the obvious sources of trouble first. The following is a list of potential problems:

        - interconnect cables improperly oriented or not connected
        - PC boards not plugged in properly (to check, remove and plug in all boards in bus)
        - Drive address incorrect (must be Drive 0 for loading BASIC)
        - wrong Minidiskette
        - not enough memory (needs 24K minimum)
        - I/O or memory boards incorrectly addressed
        - power not on or unit not plugged in
        - wrong PROM being used. If using MDBL, see listing in section 3-4.
        - defective Diskettes or tapes. To verify, use a known good copy.
        - sense switches incorrectly set

3-4. MDBL PROM LISTING

Program 3-I is a listing of the MDBL PROM program:

Program 3-I. MDBL PROM Listing

Address	Code	Address	Code	Address	Code
177400	041	177454	061	177530	020
177401	023	177455	161	177531	365
177402	377	177456	115	177532	325
177403	021	177457	257	177533	305
177404	000	177460	323	177534	325
177405	114	177461	010	177535	021
177406	016	177462	333	177536	206
177407	343	177463	010	177537	200
177410	176	177464	346	177540	041
177411	022	177465	010	177541	343
177412	043	177466	302	177542	114
177413	023	177467	034	177543	333
177414	015	177470	114	177544	011
177415	302	177471	076	177545	037
177416	010	177472	004	177546	332
177417	377	177473	323	177547	120
177420	303	177474	011	177550	114
177421	000	177475	303	177551	346
177422	114	177476	070	177552	037
177423	363	177477	114	177553	270
177424	257	177500	333	177554	302
177425	323	177501	010	177555	120
177426	042	177502	346	177556	114
177427	057	177503	002	177557	333
177430	323	177504	302	177560	010
177431	043	177505	055	177561	267
177432	076	177506	114	177562	372
177433	054	177507	076	177563	134
177434	323	177510	002	177564	114
177435	042	177511	323	177565	333
177436	076	177512	011	177566	012
177437	003	177513	333	177567	167
177440	323	177514	010	177570	043
177441	020	177515	346	177571	035
177442	333	177516	100	177572	302
177443	377	177517	302	177573	134
177444	346	177520	055	177574	114
177445	020	177521	114	177575	341
177446	017	177522	021	177576	021
177447	017	177523	000	177577	346
177450	306	177524	000	177600	114
177451	020	177525	006	177601	001
177452	323	177526	000	177602	200
177453	020	177527	076	177603	000

Address	Code	Address	Code	Address	Code
177604	032	177672	346	177760	172
177605	167	177673	002	177761	274
177606	276	177674	302	177762	300
177607	302	177675	245	177763	173
177610	303	177676	114	177764	275
177611	114	177677	076	177765	311
177612	200	177700	001	177766	000
177613	107	177701	323	177767	000
177614	023	177702	011	177770	000
177615	043	177703	303	177771	000
177616	015	177704	102	177772	000
177617	302	177705	114	177773	000
177620	161	177706	076	177774	000
177621	114	177707	200	177775	000
177622	032	177710	323	177776	000
177623	376	177711	010	177777	000
177624	377	177712	303		
177625	302	177713	000		
177626	210	177714	000		
177627	114	177715	321		
177630	023	177716	361		
177631	032	177717	075		
177632	270	177720	302		
177633	301	177721	106		
177634	353	177722	114		
177635	302	177723	076		
177636	272	177724	103		
177637	114	177725	001		
177640	361	177726	076		
177641	361	177727	115		
177642	052	177730	373		
177643	344	177731	062		
177644	114	177732	000		
177645	315	177733	000		
177646	335	177734	042		
177647	114	177735	001		
177650	322	177736	000		
177651	263	177737	107		
177652	114	177740	076		
177653	004	177741	200		
177654	004	177742	323		
177655	170	177743	010		
177656	376	177744	170		
177657	020	177745	323		
177660	332	177746	001		
177661	104	177747	323		
177662	114	177750	021		
177663	006	177751	323		
177664	001	177752	005		
177665	312	177753	323		
177666	104	177754	043		
177667	114	177755	303		
177670	333	177756	322		
177671	010	177757	114		

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3-5. **System Operation With Minidisk BASIC**

    A. Initialization Dialog. After BASIC has been loaded correctly, the following question is printed on the terminal:

    MEMORY SIZE?

The user replies to this question with a number specifying the total amount of memory to be used by the BASIC system and BASIC programs. This number is followed by a carriage return. Typing the return without specifying a number causes the system to use all of the memory available in the system.

    After the return, BASIC asks:

    LINE PRINTER?

Three responses are acceptable. Typing Q means the Q70 printer is in use. C specifies the C700 and 0 specifies the LP80. If no printer is connected to the system, any of the letters may be typed. The letter is followed by a return.

    BASIC now asks

    HIGHEST DISK NUMBER?

to which the user responds with the number of the last Minidisk drive in the system. If there is one Minidisk drive in the system, the highest disk number is 0. If there are two drives, the number is 1.

    Since BASIC must allocate a certain amount of memory for each disk file in use, BASIC now asks:

    HOW MANY FILES?

The user responds with the number of disk files (either random access or sequential) that are to be open at one time. Finally, BASIC asks

    HOW MANY RANDOM FILES?

which allows the user to specify the number of random access files to be open at one time. Note that the answer to this question may not be greater than the number specified in the HOW MANY FILES? question.

    When the initialization dialog is completed, BASIC prints

    XXXXXX BYTES FREE

    ALTAIR BASIC REV. 4.1

    [DISK EXTENDED VERSION]

    COPYRIGHT 1977 BY MITS, INC.

    OK

Minidisk BASIC is now ready for use.

B. Using PIP and STARTREK. Because the BASIC code takes up so much diskette space, it is supplied on a "write protected" diskette. This means that no programs or data may be saved on the BASIC diskette.

In addition to BASIC, the BASIC diskette includes two programs, PIP and STARTREK, which are available to users. Before they can be run, the BASIC diskette must be mounted (see section D). Since the BASIC diskette is write protected, mounting it causes a DISK I/O ERROR, but the reading process is not affected.

The desired program may now be read from the disk and loaded into memory. To do this, type the following command:

LOAD "<program name>", <disk number>

where <program name> is the name of the desired program and <disk number> is the number of the disk drive into which the BASIC disk was inserted (usually zero).

To avoid inadvertant damage to the BASIC disk, type the following command:

UNLOAD <disk number>

where <disk number> is the drive number that appeared in the LOAD command above.

Now the BASIC diskette may be removed and another diskette inserted into the drive and mounted. The program may be saved on the new diskette by typing the following command:

SAVE "<program name>", <disk number>

where <disk number> is the number of the disk drive into which the new diskette was inserted.

Subsequent to saving the program, it may be run by typing the following command:

RUN "<program name>", <disk number>

where <disk number> is the number of the disk drive into which the diskette bearing the program was inserted.

```
                           CAUTION
  Do not attempt to write programs or data onto the BASIC
  diskette.  This can result in FILE LINK ERRORS that can make
  the BASIC diskette unusable.  Before writing anything on disk,
  unload and remove the BASIC diskette.
```

C. Initializing New Diskettes. If the diskette has never been used, it must be initialized before it can be used. This is done by typing the following command:

DSKINI <disk number>

where <disk number> is the number of the disk drive on which the blank diskette is loaded. The DSKINI command marks all the sectors on the diskette as being empty. BASIC reads these marks to determine sector boundaries.

```
+-----------------------------------------------------------+
|                        CAUTION                            |
| Only new, blank diskettes need to be initialized.  Using  |
| DSKINI on a diskette that contains files destroys all the |
| files.  DSKINI should, therefore, be used with extreme cau-|
| tion.  The DSKINI process takes about 2 minutes per diskette.|
| When it is finished, BASIC prints OK.                     |
+-----------------------------------------------------------+
```

D. Mounting Diskettes. To ready a diskette for reading or writing, type the following command:

MOUNT <disk number>

Omitting the disk number causes all disks in the system to be mounted. After a few seconds, BASIC prints

OK

to indicate that the disk is ready for use.

Before removing a mounted disk from a drive, type the following command

UNLOAD <disk number>

Omitting the disk number unloads all mounted disks.

3-6. ASSEMBLY CODE TO READ AND WRITE A SECTOR

Program 3-II is provided to help users write assembly language subroutines to read and write data on the Minidisk. It is assumed that the Disk being used has already been enabled and positioned to the correct track.

Program 3-II. Assembly Code To Read And Write A Sector

```
; CALL WITH NUMBER OF DATA BYTES TO WRITE IN [A]
; AND POINTER TO DATA BUFFER IN [H,L]
; ALL REGS DESTROYED.
DSKO:   MOV   C,A         ; SAVE # OF BYTES IN C
        MVI   A,136       ; CALCULATE NUMBER OF ZEROS TO WRITE
        SUB   C           ; SUBTRACT THE NUMBER OF DATA BYTES
        MOV   B,A         ; NUMBER OF ZEROS+1
        CALL  SECGET      ; LATENCY
        MVI   A,128       ; ENABLE WRITE WITHOUT SPECIAL CURRENT
        OUT   9
;
; CALL WITH [B]=NUMBER OF ZEROS [C]=NUMBER OF DATA BYTES
; AND [H,L] POINTING AT OUTPUT DATA
;
OHLDSK: MVI   D,1         ; SETUP A MASK (READY TO WRITE)
        MVI   A,128       ; HIGH BIT (D7) ALWAYS ON IN FIRST BYTE
        ORA   M           ; OR ON DATA BYTE
        MOV   E,A         ; SAVE FOR LATER
        INX   H           ; INCREMENT BUFFER POINTER
NOTYTD: IN    8           ; GET WRITE DATA READY STATUS
        ANA   D           ; TEST STATUS BIT
        JNZ   NOTYTD      ; NOT READY TO WRITE, WAIT
        ADD   E           ; ADD BYTE WE WANT TO SEND TO ZERO
        OUT   10          : SEND THE BYTE
```

```
            MOV     E,M             ; GET NEXT DATA BYTE
            INX     H               ; MOVE BUFFER POINTER AHEAD AGAIN
            DCR     C               ; DECREMENT COUNT OF CHARS TO SEND
            JNZ     NOTYTD          ; STILL MORE CHARS, DO THEM.
ZRLOP:      IN      8               ; GET READY TO WRITE
            ANA     D               ; IS IT READY
            JNZ     ZRLOP           ; IF NOT, LOOP
            OUT     10              ; KEEP SENDING FINAL BYTE
            DCR     B               ; DECREMENT COUNT OF BYTES TO SEND
            JNZ     ZRLOP           ; KEEP WAITING
            EI                      ; RE-ENABLE INTERRUPTS
            MVI     A,8             ; UNLOAD HEAD
            OUT     9               ; SEND COMMAND
            RET                     ; DONE
; DISK INPUT ROUTINE.  ENTER WITH POINTER
; OF 137 BYTE BUFFER IN [H,L].  ALL REGS DESTROYED.
DSKI:       CALL    SECGET          ; POINT TO RIGHT SECTOR
            MVI     C,137           ; GET # OF CHARS TO READ
READOK:     IN      8               ; GET DISK STATUS
            ORA     A               ; READY TO READ BYTE
            JM      READOK
            IN      10              ; READ THE STUFF
            MOV     M,A             ; SAVE IN BUFFER
            INX     H               ; BUMP DESTINATION POINTER
            DCR     C               ; LESS CHARS
            JNZ     READOK          ; IF CHARS STILL LEFT, LOOP BACK
```

```
RETDO:  EI                      ; RE-ENABLE INTERRUPTS
        MVI   A,8               ; UNLOAD HEAD
        OUT   9                 ; SEND COMMAND
        RET
SECGET: DI                      ; DISABLE INTERRUPTS
SECLP2: IN    9                 ; GET SECTOR INFO
        RAR                     ; FIX UP SECTOR #
        JC    SECLP2            ; IF NOT, KEEP WAITING
        ANI   15                ; GET SECTOR #
        CMP   E                 ; IS IT THE ONE WE WANTED
        JNZ   SECLP2            ; TRY TO FIND IT
        RET
```

3-7. MACHINE LANGUAGE OPERATION

A. Controller I/O Requirements

To communicate with the 88-MDS Controller at the machine language level, the following I/O information is provided. The Minidisk Controller uses three I/O Channels in the Altair computer. Three 8-bit Channels go into the Controller for controlling and writing of data, and three 8-bit Channels for reading the Controller Status, the Sector Count (rotational position of the Minidiskette) and the Read Data. The following is a listing of the Channels and a description of their functions.

1. I/O Address for the Minidisk Controller

Octal Address	Mode	Description
010	Output from CPU	Enables one of four Drives
010	Input to CPU	Indicates status of Drives and Controller
011	Output from CPU	Controls Drive operation
011	Input to CPU	Indicates Sector position of Diskette
012	Output from CPU	Write Data
012	Input to CPU	Read Data

2. Definitions of I/O Functions as listed above.

   a) Output from CPU to Minidisk Controller address 010:

Bit	Function
D0 D1	Enables one of four Minidisk Drives. The Read/ Write Head is loaded when the Drive is enabled.
D2-D6	Not used
D7	Set to zero if enabling Drives. When set to 1, Minidisk system is turned off.

```
                            NOTES
(1) When changing from one Drive address to another, turn the
    system off (output a 377 to Channel Ø1Ø), and then enable the
    desired Drive
(2) Never issue a Head Step command prior to changing Drive addresses
    or turning off a Drive.  If you must step the head, check the
    MH status bit for a logic Ø before changing or turning off the
    Drive.
(3) If the Drive selected is not connected or its power is off, the
    Controller will automatically turn off.
(4) Drive addresses are selected as follows:
       Drive Address        DØ       D1
            0               0        0
            1               1        0
            2               0        1
            3               1        1
```

b) An input to CPU from Minidisk Controller Address Ø1Ø gives
   the Disk System status when a Drive is enabled.

   When a bit is True, it is a logic Ø, when False, the bit is
   a logic 1. Also, all status bits are logic 1 when there is
   not a Minidiskette in the Drive. The status bits are des-
   cribed as follows:

   DØ = $\overline{ENWD}$ - Enter New Write Data when True, requests
                   that a byte of data be output to the Write
                   Data Channel (Ø12). Occurs during the
                   Write mode every 64µs. $\overline{ENWD}$ is reset upon
                   receipt of the output data byte.

   D1 = $\overline{MH}$ - Move Head when True, indicates that head
                   stepping is allowed. Goes False for 50ms.
                   after the step command, indicating the head
                   may not be stepped. Also False during
                   Write mode.

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D2 = $\overline{\text{HS}}$ - Head Status when True, indicates the head is properly loaded and motor speed is stable. Goes True one second after Disk Enable, goes False for 50ms following a command. When False, it prevents the Sector information from being read. This bit is not normally used since Read/Write software tests the Sector Channel just before Reading or Writing. Note that the head is always loaded when the Drive is enabled.

D3 - Not used, always = 0 when Drive is enabled.

D4 - Not used, always = 0 when Drive is enabled.

D5 - $\overline{\text{INTE}}$, reflects the Interrupt Enable status of the CPU. True when equal to 0, indicating CPU interrupts are enabled.

D6 - $\overline{\text{TRACK }\emptyset}$, when True, indicates that the Drive R/W head is positioned at the outermost track. This status bit should be used for zeroing the software track counter.

D7 - $\overline{\text{NRDA}}$, New Read Data Available when True indicates the Read Circuit has a byte of data ready to be input from the Read Data Channel ($\emptyset$12). $\overline{\text{NRDA}}$ occurs every 64μs. when reading data and is reset each time a byte of Read Data is input from Channel $\emptyset$12.

c) An output from the CPU to Minidisk Controller Address $\emptyset$11 controls the Minidisk Drive functions.

A logic 1 represents a True signal and controls the Drive functions as follows:

D$\emptyset$ = STEP IN - steps the Drive R/W head in one position to a higher numbered track. The $\overline{\text{MH}}$ status should be checked before issuing a step command. STEP IN also resets the 6.4 second Disk Disable Timer and causes $\overline{\text{MH}}$ and Sector information to go False for 50ms. Software is responsible for keeping the track position.

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D1 = STEP OUT - Steps the Drive R/W head out one position
to a lower numbered track. The MH status should be
checked before issuing a step command. STEP OUT also
resets the 6.4 second Disk Disable Timer and causes
$\overline{MH}$ and Sector information to go False for 50ms. Soft-
ware is responsible for keeping the track position.

D2 = TIMER RESET - Resets the 6.4 second Disk Disable
Timer. This command should be issued before every
Read or Write operation to insure that the 88-MDS
continues to be enabled.

D3 = Not used.

D4 = INTERRUPT ENABLE - Enables interrupts to occur at the
beginning of each Sector. Stays enabled until turned
off by Interrupt Disable or the Controller turned
off (see section 3-8 for more information).

D5 = INTERRUPT DISABLE - Disables the Controllers interrupt
circuit. Interrupts are also disabled when the Controller
is turned off.

D6 = Not used.

D7 = WRITE ENABLE - turns the Controller and Drive Write
Circuits on. WRITE ENABLE is reset at the end of
each Sector. The WRITE ENABLE sequence should be
performed as follows:

  a. Minidisk Drive selected with head positioned at
     desired track.

  b. Desired Sector is searched for (see next section,
     part d, for Sector information).

  c. Desired Sector is found and WRITE ENABLE command
     is issued.

  d. Zeros are automatically written for the first 1ms
     of the Sector.

  e. 1ms after beginning of Sector, $\overline{ENWD}$ goes True,
     requesting first byte of Write Data.

f. Most significant bit (D7) of first byte written must be a logic 1 (sync bit). The sync bit is used for Read synchronization. The MSB (D7) is written first. The first byte is referred to as the sync byte.

g. $\overline{ENWD}$ goes True every 64μs and is reset after a Write Data byte is output to Channel Ø12.

h. The maximum number of bytes that are written is 137, including the sync byte.

i. The last or 138th byte written must be all zeros (000). This pattern will be written to the end of the Sector. $\overline{ENWD}$ may be ignored from this point on.

j. At the end of the Sector the Write Circuit automatically turns off.

The WRITE ENABLE sequence is now completed. For more information on the software required for reading and writing data, see the Read/Write Test program in section 5-4 (Program 5-I).

d) Sector Position

An Input to the CPU from Minidisk Controller address Ø11 gives the Sector position of the Minidiskette in the selected Minidisk Drive.

Sector position is determined by the rotational position of the Minidiskette. The 88-MDS uses a 16 Sector Minidiskette which has 16 Sector holes and one Index hole. These holes are sensed optically and cause pulses to be sent to the Minidisk Controller. The Controller has a counter that is cleared when the Index hole is detected and then counts the Sectors 0 through 15. Reading and writing of data must start at the beginning of the Sector to insure there is no loss of data. To be certain the Read/Write operations start at the beginning of a Sector, the first Sector position bit goes True only during the first 30μs of a Sector. The next four Sector position bits give the actual Sector count. Table 3-B describes the Sector position bits.

$D\emptyset = \overline{ST}$ - Sector True = $\emptyset$ when True. It is True during
the first 30μs of a Sector. When reading or
writing data, this is the only time the Sector
position may be checked against the desired Sector
position.

The following bits reflect the actual Sector count:

Table 3-B. Sector Position Bits

Sector Count									
	0	1	2	3	4	13	14	15	
D1	0	1	0	1	0	1	0	1	
D2	0	0	1	1	0	0	1	1	
D3	0	0	0	0	1	1	1	1	
D4	0	0	0	0	0	1	1	1	
D5 = Always $\emptyset$									
D6 = Not used = 1									
D7 = Not used = 1									

NOTE

The Sector position channel will be disabled (all "1"s) for
1 second after the Drive is enabled, and 50 ms after a step
command is issued.

When reading a Sector, the Read Circuit is disabled during
the first 500μs to insure valid detection of the sync byte.
When writing a Sector, the Write Circuit should be enabled
as near to the Sector True detection as possible. When
enabled, the Write Circuit will automatically write zeros
for the first 1ms of the Sector.

e) Write Data

An output from the CPU to Minidisk Controller address $\emptyset12$
writes data to the Controller Write Circuit.

Write Data should be output to the Controller only after
detection of the $\overline{ENWD}$ status bit going True. $\overline{ENWD}$ is reset
upon the Controllers receipt of the output data byte.

Write Data is written on the Minidiskette most significant
bit first in MFM format.

f) Read Data

An input to the CPU from Minidisk Controller Address Ø12
reads data from the Controller Read Circuit.

When the Minidisk Drive is enabled, the Controller is normally
in the Read mode unless the Write Circuit is enabled. Data
bytes may be read upon detection of the $\overline{\text{NRDA}}$ status bit going
True. $\overline{\text{NRDA}}$ is reset when the byte of data is read on
Channel Ø12.

Read Data is read from the Minidisk Drive most significant
bit first in MFM format.

3-8. USING INTERRUPTS ON THE ALTAIR MINIDISK SYSTEM

Although the Interrupt Circuit of the Minidisk Controller is an
extremely useful feature, not many users take advantage of it since it
is not utilized in Altair Minidisk BASIC. The primary functions of the
interrupt procedures are to save CPU time in systems that are supporting
Minidisks and other operations simultaneously. Minidisk interrupts are
caused by detection of a Sector pulse when interrupts are enabled.

The most obvious use of the Sector interrupts would be performing
a Sector search for Disk I/O. The Minidisk Controller would interrupt
the Altair computer at the beginning of every Sector, or every 12.5ms.
Only a few microseconds would be used in identifying the Sector count,
and the Altair computer could be performing other tasks until the
required Sector was found.

Another use for the interrupts is for Disk system timing. Instead
of checking Move Head status every time the Disk head is stepped, the
timing can be controlled by Sector interrupts. This is done by enabling
interrupts and issuing the desired step command after the first inter-
rupt is received. Since interrupts occur every 12.5ms , four interrupts
are counted (50ms) and the next step command is issued. This process
may be used to step the Disk head any number of tracks. Check for
TRACK Ø status before issuing the step command.

To utilize Sector interrupts, on Minidisk Controller Board 1, the SR1 jumper must be connected to the desired interrupt pad. If single level interrupts are implemented, use the INT (or PINT) pad. If Vectored Interrupts are implemented, use the highest level priority, VI∅.

To enable interrupts, the 8080 CPU must have its interrupts enabled. Also if Vectored Interrupts are utilized, consult the 88-VI/RTC manual. Then, the Minidisk Controller must have its interrupts enabled. CPU Interrupts must be re-enabled after every interrupt is serviced if more interrupts are required.

Section IV
Theory of Operation

4-1. GENERAL

This section contains information needed to understand the operation of the MITS Altair Minidisk System (88-MDS). It contains a description of the logic symbols used in the Minidisk schematics and a detailed theory of operation.
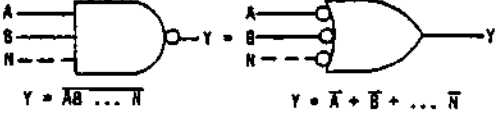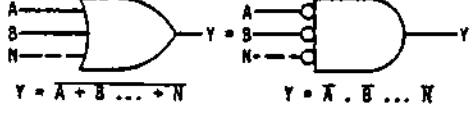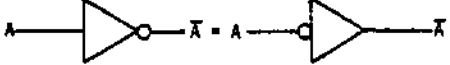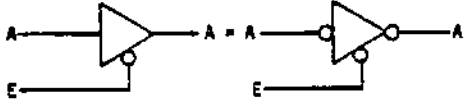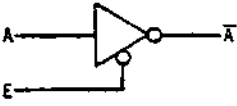
4-2. LOGIC CIRCUITS

The logic circuits used in the schematics are presented as a tabular listing in Table 4-A. The table is constructed to present the functional name, symbolic representation and a brief description of each logic circuit. Truth tables are provided to aid in understanding circuit operation where applicable. The active state of the inputs and outputs of the logic circuits is graphically displayed by small circles. A small circle at an input to a logic circuit indicates that the input is an active LOW; that is, a LOW signal will enable the input. A small circle at the output of a logic circuit indicates that the output is an active LOW; that is, the output is LOW in the actuated state. A bar over the signal description also indicates an active LOW. Conversely, the absence of a small circle on the input or output, or a bar over the signal description indicates an active HIGH.

4-3. SCHEMATIC REFERENCING

The detailed schematics are provided to aid in determining signal direction and tracing. A solid arrow (➤) on the signal line indicates direction, and the tracing of the signal through the schematics is referenced as it leaves the page. The reference is shown as a number - letter number (e.g. 2-A3), indicating Sheet 2 and schematic Zone A3.

Table 4-A.   Symbol Definitions

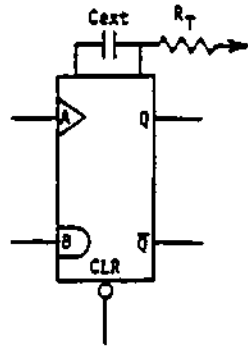| Name/Logic Symbol	Description
AND gate A ─┐ B ─┤ [AND gate symbol] ─ Y N ─┘	All the inputs have to be enabled HIGH to produce the desired HIGH output. The output is LOW if any of the inputs are LOW.
NAND gate [NAND gate symbol] Y = $\overline{AB\ldots N}$ [OR gate symbol] Y = $\overline{A} + \overline{B} + \ldots \overline{N}$	All of the inputs have to be enabled HIGH to produce the desired LOW output. The output is HIGH if any of the inputs are LOW.
NOR gate [NOR gate symbol] Y = $\overline{A + B \ldots + N}$ [AND gate symbol] Y = $\overline{A} \cdot \overline{B} \ldots \overline{N}$	Any of the inputs need to be enabled HIGH to produce the desired LOW output. The output is HIGH if all of the inputs are LOW.
Inverter A ─[inverter]─ $\overline{A}$ = A ─[inverter]─ $\overline{A}$	The inverter is a device whose output is the opposite state of the input.
Non-Inverting Bus Driver A ─[bus driver]─ A = A ─[bus driver]─ A E ─┘ E ─┘	When enabled, the non-inverting bus driver is a device whose output is the same state as the input. Data is enabled through the device by applying a LOW signal to the E input. The output "floats" or goes to a high impedance state when the non-inverting bus driver is not enabled.
Inverting Bus Driver A ─[bus driver]─ $\overline{A}$ E ─┘	The inverting bus driver is a device whose output is the opposite state of the input when enabled. Data is enabled through the driver by applying a LOW signal to the E input. The output "floats" or goes to a high impedance state when the non-inverting bus driver is not enabled.

Retriggerable Monostable Multivibrator (74123)	The multivibrator is essentially a pulse generator whose pulse width may be varied by changing the value at two external components. Output pulse $= .32\ R_T\ C_{ext}\ \left(1+\dfrac{.7}{R_T}\right)$ R_T is in K ohms. C_{ext} is in pf. Output pulse is in nsec. Before an output pulse is terminated, the output of a retriggerable multivibrator may be triggered again, allowing output pulses of long duration.
Quad D Latch (74L75)	When the clock is HIGH, information present at data inputs $(D_A\text{-}D_D)$ is transferred to the $Q_A\text{-}Q_D$ outputs. Data is latched on the falling edge of the clock pulse. The data is inverted when the $\overline{Q}$ outputs are used.
Dual J-K Master-Slave Flip-Flop (74L73 or 74LS73)	When inputs are conditioned with J HIGH and K LOW and the flip-flop is clocked at C, the Q output either goes or remains HIGH, but cannot go LOW. If J and K are both HIGH, the Q outputs will toggle. Applying a LOW signal to the clear (CLR) input resets the flip-flop with Q LOW and $\overline{Q}$ HIGH. Clocking occurs on a HIGH to LOW transition at the clock (C) input.
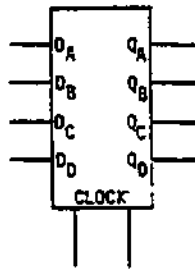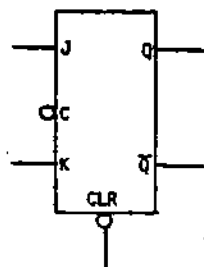
4-Bit Binary Counter (7493)	Output Q_A must be externally connected to the B_{IN} input. The count pulses are applied to the A_{IN} input. At the Q_A, Q_B, Q_C and Q_D outputs the 4-bit ripple through counter performs simultaneous frequency divisions of 2, 4, 8 and 16. When RO1 and RO2 are both HIGH, the Q outputs are reset LOW. Clocking occurs on a HIGH to LOW transition at the clock input.
8-Bit Parallel-Out, Serial-In Shift Register (74164)	Clocking occurs on a LOW to HIGH transition of the clock input, shifting the data over one position. A LOW at either or both inputs inhibits entry of new data and resets the flip-flop LOW on the following clock pulse. When both inputs are HIGH, the A output is HIGH.
Edge Triggered D Type Flip-Flop (74L74)	Applying a LOW signal to the clear input (CLR) resets the flip-flop with Q LOW and $\overline{Q}$ HIGH. If a signal is applied to the D input, the Q and $\overline{Q}$ outputs are directly affected on the positive edge of the clock pulse. (Q output follows D input)
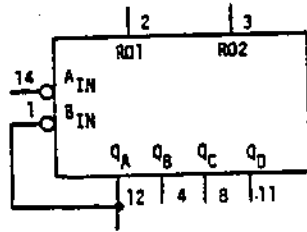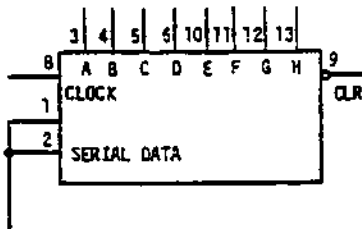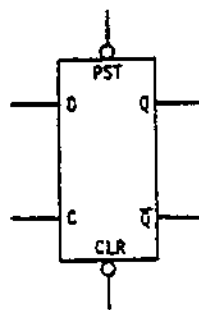
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Synchronous 4-Bit Counter (74L161 or 93L16) [diagram of counter block with inputs A B C D, EP, ET, CLOCK and outputs LOAD, RC, A_OUT B_OUT C_OUT, CLR]	The synchronous 4-bit counter is used as a Divide by Eight Presettable counter with internal carry (RC). When all outputs (A_{OUT}, B_{OUT} and C_{OUT}) are clocked HIGH, RC is HIGH. Data is transferred to the outputs when LOAD is LOW and a clock pulse is received. Clocking occurs on the rising edge of the clock pulse.
8-Bit Parallel-In, Serial-Out Shift Register (74166) [diagram of shift register block with Serial Data Out, CLOCK, CLOCK INHIB inputs and CLR, SER/Ø PAR outputs, Parallel Data In 0 1 2 3 4 5 6 7]	When HIGH, the SER/ØPAR input enables the serial data input; when LOW, the parallel data inputs are enabled. During parallel loading (Ø-7), serial data flow (SERIAL DATA OUT) is inhibited. When clock inhibit (CLOCK INHIB) is held HIGH, clocking is inhibited. Clocking is accomplished on a LOW to HIGH level of the clock, shifting data over one position towards the serial data output.
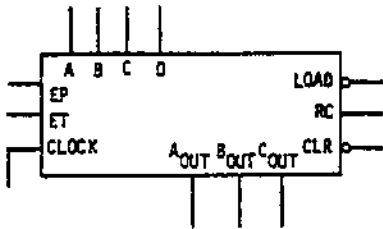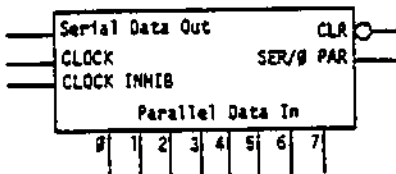
4-4. MINIDISK SYSTEM BLOCK DIAGRAM

The 88-MDS system consists of three major sections:

1. The Altair 8800 computer and the appropriate hardware and software for operating the Disk System which is typically 32K of memory and Minidisk Extended BASIC.

2. Two Controller boards which interface the Altair 8800 computer to the Disk Drive (see Disk Controller Theory of Operation, beginning with paragraph 4-5).

3. The Disk Drive cabinet which contains the Minidisk Drive plus the line drivers and receivers necessary for interconnection to the Controller and additional Disk Drives.

MINIDISK SYSTEM BLOCK DIAGRAM
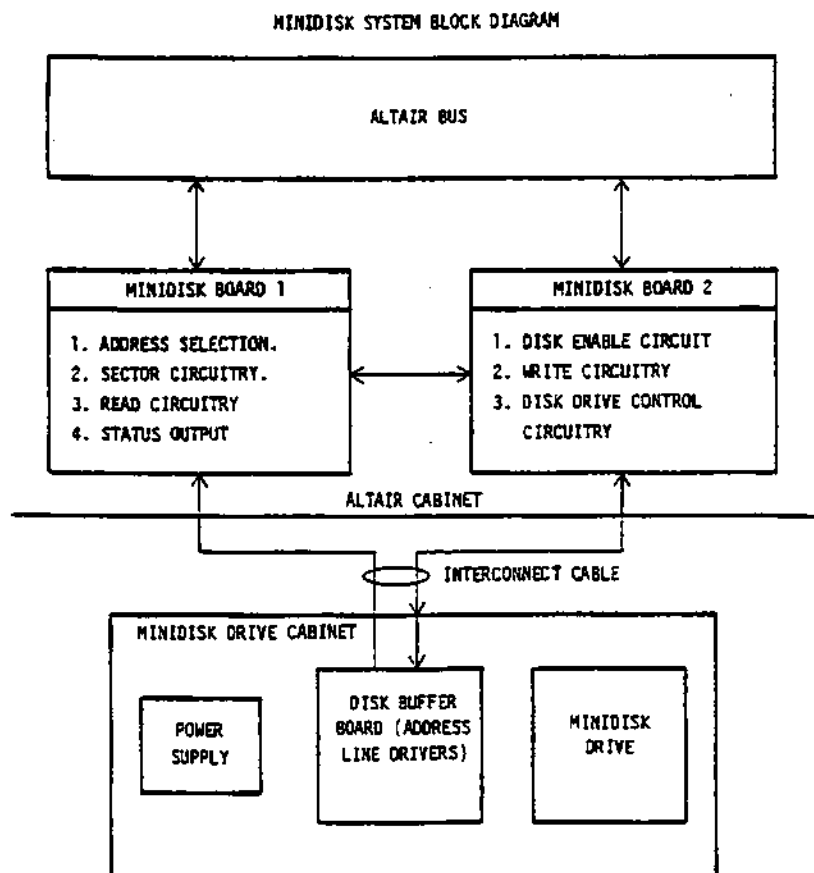
Figure 4-1. Minidisk System Block Diagram

4-5. GENERAL SYSTEM OPERATION

In order to begin Disk operation, the computer must select and enable the Disk Drive and Controller. The desired Drive address ($\emptyset\emptyset\emptyset$ to $\emptyset\emptyset4_8$) is output on I/O Channel $\emptyset1\emptyset_8$. When the Drive is enabled, the head is automatically loaded and the motor starts. TRACK $\emptyset$ is found by stepping the head out to the outermost track (Output-Channel $\emptyset11_8$, Bit D1 = 1) and testing the Status (Input-Channel $\emptyset1\emptyset_8$, Bit D6 = 0).

After the appropriate reference for TRACK $\emptyset$ is found, the Altair computer steps the head in (Output-Channel $\emptyset11_8$, Bit D$\emptyset$ = 1) to the desired track. Software determines which track the Disk head is on, once TRACK $\emptyset$ has been found.

The correct Sector is located by performing an input from the Sector Channel (Input-Channel $\emptyset11_8$) and comparing the desired Sector number with the Sector count from the Controller circuit. After the Disk reaches the correct rotational position or Sector, the Altair computer performs either a Read Data function (Input-Channel $\emptyset12_8$, D$\emptyset$-D7) or enters a Write Data mode. In the Write mode, the Write Circuits must be enabled (Output-Channel $\emptyset11_8$, D7 = 1). A few hundred micro-second delay elapses before Write Data is requested, after which a new byte of Write Data is requested every 32 microseconds.

When the computer has finished accessing the Disk, Disk Control is cleared (Output-Channel $\emptyset1\emptyset_8$, D$\emptyset$ through D7 = 1 or 377_8). Clearing Disk Control disables the Drive and causes all Disk functions to cease. Turning the Disk Drive power off, or disconnecting the cable also clears Disk Control.

When changing access from one Drive to another, Disk Control must be cleared (Output-Channel $\emptyset1\emptyset_8$, 377_8) before enabling the new Disk. This is to insure the Controller circuits are reset before accessing a new Drive.

4-6. MINIDISK CONTROLLER BLOCK DIAGRAM

The Minidisk Controller Address Select Circuit accepts input and output (I/O) instructions from the Altair computer on I/O Channels 010_8, 011_8 and 012_8. The Altair I/O ADDRESS LINES (8 lines) select one of the three I/O Channels and Altair I/O Status lines (4 lines) determine whether an input or output instruction is required. An I/O instruction to any channel results in a LOW going 500nsec. pulse (refer to Figure 4-2) on the respective enable line from the address select circuit (Board 1).
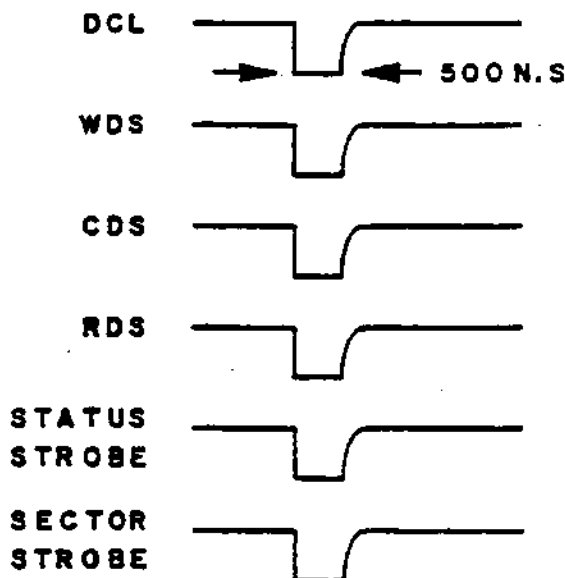
Figure 4-2. I/O Channel Timing

The three Output functions associated with Minidisk Board 2 are:

1. Output on Channel 010_8: DISK CONTROL LATCH (DCL) selects Disk address and enables Controller.

2. Output on Channel 011_8: CONTROL DISK (CD) controls Disk Drive functions such as STEP IN or OUT, WRITE ENABLE, etc.

3. Output on Channel 012_8: WRITE DATA STROBE (WDS) strobes WRITE DATA bytes into write data latch during Disk Write mode. WDS also resets ENWD (Enter New Write Data) Status bit until next byte is requested.

The three Input functions associated with Minidisk Board 1 are:

1. Input on Channel 010_8: Places Disk status information on the Altair Data Bus. Status information includes: HEAD STATUS (HS); OK TO MOVE HEAD (MH); ENTER NEW WRITE DATA (ENWD); NEW READ DATA AVAILABLE (NRDA).

2. Input on Channel 011_8: Places the Disk Sector count on the Altair Data Bus. As the Disk rotates, the Sector count is incremented every 12.5ms , and is reset to 0 upon detection of the Index hole once every rotation (200ms).

3. Input on Channel 012_8: Places Disk READ DATA on the Altair Data Bus. This input instruction resets the NRDA Status bit.
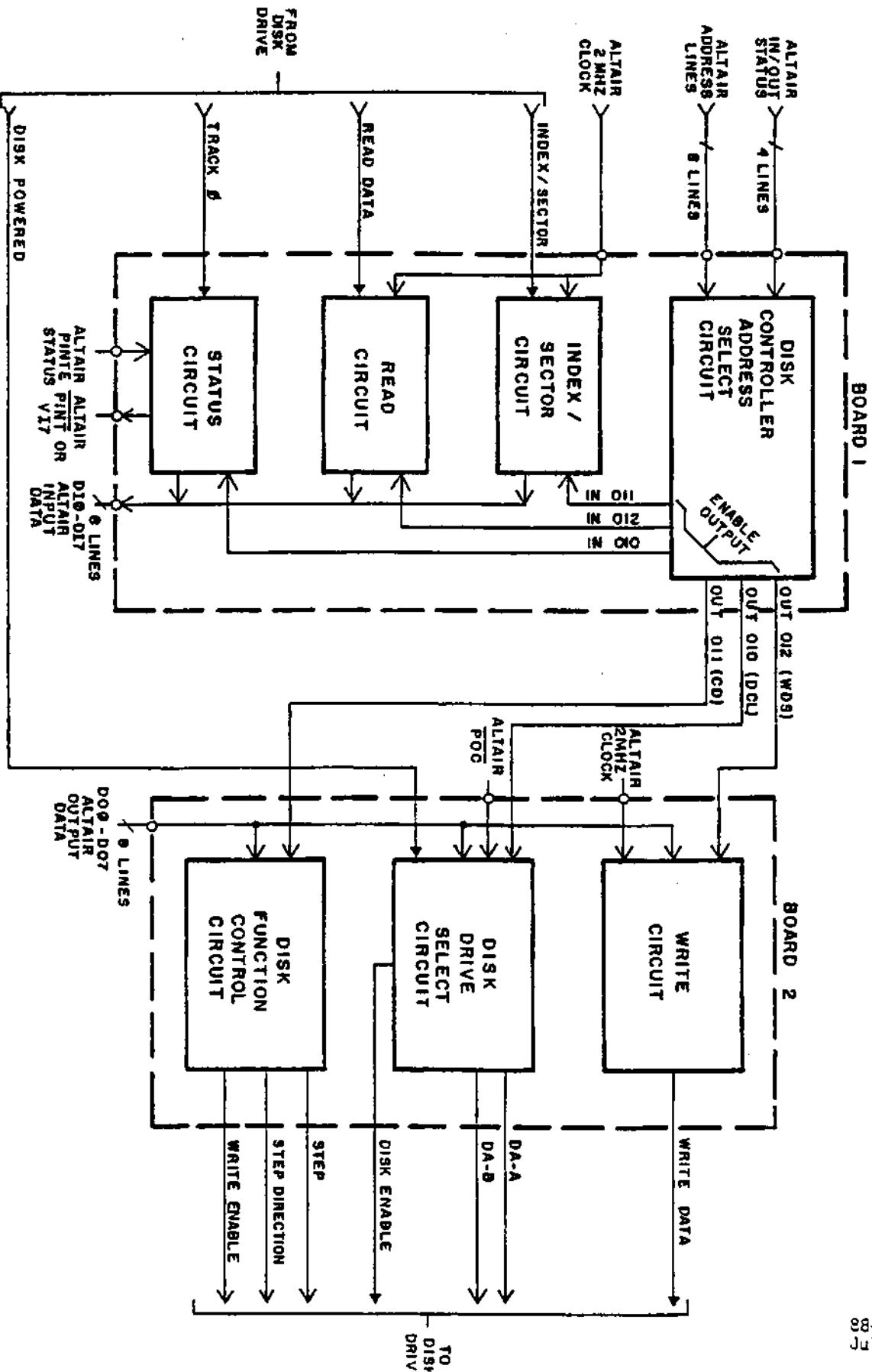
Figure 4-3. Disk Controller Block Diagram (Sheet 1, External Connections and Address Select)

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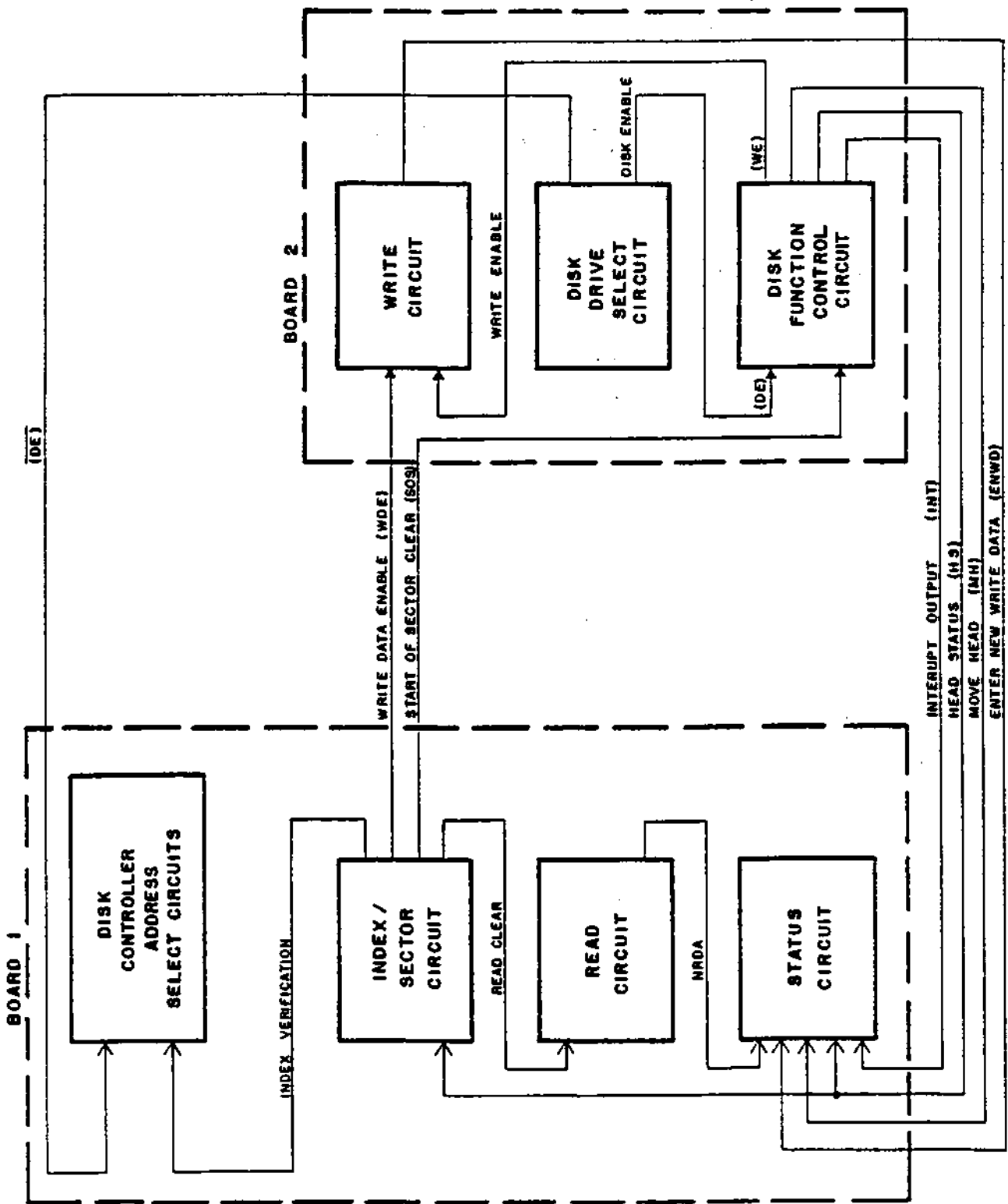
Figure 4-4. Disk Controller Block Diagram (Sheet 2, Internal Connections)

Upon an Output to Channel 010_8, the DISK CONTROL LATCH (DCL), Disk Drive Select Circuits are enabled with DA-A and DA-B, selecting one of four possible Minidisk Drives. The DISK POWERED line enables the Disk Drive Select Circuit when the Drive selected is properly connected and powered. When the Minidisk Drive is selected and enabled, the DISK ENABLE (DE) signal is presented to the Disk Function Control Circuit where DE enables the Status information.

The Disk Function Control Circuits, when selected, load the head on the Disk (HEAD LOAD), step the head out (STEP OUT), step the head in (STEP IN) and enable the Write Circuit (WRITE ENABLE). Control Circuits also produce INTERRUPT OUTPUT, MOVE HEAD or HEAD STATUS signals which are transferred to the Disk Status Circuits. Control signals, Disk address information and WRITE DATA are transferred from the Altair computer to Controller Board 2 by eight Output Data Lines (D00-D07).

WRITE DATA is transferred to the Write Circuit upon an output to Channel 012_8, the WRITE DATA STROBE (WDS). The rate of serial WRITE DATA to the Disk is controlled by dividing the Altair 2MHz Clock. ENTER NEW WRITE DATA (ENWD) is the Status signal generated by the Write Circuit when new WRITE DATA is requested.

When INDEX and SECTOR pulses are received by the Index/Sector Circuit, the INDEX pulse is detected, Sector count (beginning with Sector 0) may begin. The Index/Sector Circuit is synchronized by the Altair 2MHz Clock, and upon an Output to Channel 011_8, the Sector count is presented. The Index/Sector Circuit also provides a START OF SECTOR CLEAR (SOS) signal to the Disk Function Control Circuit, a WRITE DATA ENABLE (WDE) signal to the Write Circuit and the READ CLEAR signal to the Read Circuit. INDEX VERIFICATION and a True (LOW) condition on HEAD STATUS must be present before the Address Select Circuits can enable the Sector information from Channel 011_8.

When READ DATA is present from the Disk Drive and transferred to the Altair Data Bus, the Read Circuit is enabled by addressing Input Channel 012_8. The Read Circuit provides the NRDA (NEW READ DATA AVAILABLE) Status signal when READ DATA is detected.

The Status Circuit provides information on the state of the Controller and Disk Drive. A desired track is found by referencing TRACK $\emptyset$ (the outermost track). TRACK $\emptyset$, NRDA and the other Status signals are enabled by addressing Input Channel $\emptyset1\emptyset_8$. Input data is transferred from the Index/Sector Circuit, Read Circuit or Status Circuit to the Altair computer by eight Input Data Lines (DIO-DI7).

4-7. <u>ADDRESS SELECT CIRCUIT</u>

The Address Control Circuit (Figure 4-14, Sheet 1) accepts I/O instructions from the Altair computer on Channels $\emptyset1\emptyset_8$, $\emptyset11_8$ and $\emptyset12_8$.

To enable any of the strobe gates A3, A4 or A5, F5 pin 8 (zone D7) must be enabled LOW. F5 pin 8 is LOW when address lines A15-A8 (zones C8 and D8) equal $\emptyset1X_8$. (X represents a User Selectable condition for A8-A10). A15-A12 is LOW, inverted HIGH at G5 pins 2, 4, 6 and 8 (zone D8) and appear HIGH at F5. With All HIGH, F5 pin 8 goes LOW and is inverted HIGH to A5 pin 1 (zone D6). Address lines A10-A8, when equal to $XX\emptyset_8$, $XX1_8$ or $XX2_8$ (XX represents a User Selectable condition for address lines A11-A15 described above), enable one of the AND gates B4 pins 6, 8 or 12 (zone C6). When A8, A9 and A10 are all LOW, B4 pin 6 is enabled, allowing an Input or Output on Channel $\emptyset1\emptyset_8$. When A9 is HIGH and A10 and A8 are LOW, B4 pin 12 is enabled, allowing an Input or Output on Channel $\emptyset12_8$. When A8 is HIGH and A10 and A9 are LOW, B4 pin 8 is enabled, allowing an Input or Output on Channel $\emptyset11_8$. AND gates B4 determine the I/O Channel to be addressed since only one gate is enabled at a time. A specific output instruction is then selected if SOUT is HIGH and PWR is LOW (zone D8), and the specific input instruction is recognized when SINP and PDBIN are HIGH (zone D8). When the Disk is enabled, the Disk Enable line (DE, zone D8) goes HIGH, enabling the INPUT STATUS STROBE (Channel $\emptyset1\emptyset_8$) and allowing the Index Verification Flip-Flop, B3 (zone C3) to be clocked.

4-8. INDEX/SECTOR CIRCUIT (011_8 - Input)

As the Minidiskette rotates in the Drive, an optoelectronic sensor detects the 16 Sector holes and the Index hole on the Diskette. The Sector holes generate a 4.4ms pulse every 12.5ms. (Refer to Figure 4-5 for timing diagram relating to Index/Sector Circuits). The Index hole, located halfway between Sector holes 15 and 0, generates a 4.4ms pulse every revolution (200.0ms.).

The Index or Sector pulse (IND) appears LOW and is inverted HIGH to E5 pin 2 (Figure 4-14, Sheet 1, zone C6). E5 pin 3 is enabled LOW until E3 pin 13 (zone C6) is clocked. The 2MHz Clock (zone B8) goes LOW at pin 49 of the bus and is inverted by J3 pin 8, clocking the Sector Pulse Compressor Flip-Flop, E3 pin 13 (zone C6). The output pulse width (500ns $\pm$ 250ns) of E5 pin 3 (zone C6) is dependent on the propagation time of the flip-flop and the delay time of the RC time constant of R7 and C30. After being inverted, E5 pin 3 appears HIGH at the Index Window Gate, A4 pin 11 (zone C5). A4 separates the Index pulse from the Sector pulses. A2 pin 10 is enabled HIGH when E5 pin 3 goes LOW. Sector Pulse One Shot, E1 pin 13 (zone C4), goes HIGH for 300μs which triggers Index Window One Shot, E1 pin 5 (zone C4), HIGH for 9.6ms. A4 pin 8 (zone C5) is only enabled when the Index pulse enables E5 pin 3 since E1 pin 4 (zone C4) and E1 pin 5 are HIGH at A4 pins 9 and 10 during this time. The 300μs LOW going pulse at E1 pin 4 also toggles the 4 Bit Sector Counter, G4 pin 14 (zone A3).

E1 pin 5 is HIGH, leaving A2 pin 8 (zone C5) HIGH when the Index pulse appears at A2 pin 9. As a result, A2 pin 10 is not enabled when the Index pulse appears, allowing only Sector pulses to trigger E1 pin 13 (zone C4). In addition to enabling E1 at pin 10 (zone C4), the HIGH 300μs pulse at E1 pin 13 is also present at E2 pin 10 (zone B6). E2 pin 8 is enabled LOW when E1 pin 13 is HIGH, since E3 pin 8 (zone B6) is in a reset condition (E3 pin 8 HIGH). The 2MHz Clock enables the Sector Pulse One Shot Compressor, F2 pin 9 (zone B7) HIGH, and on the

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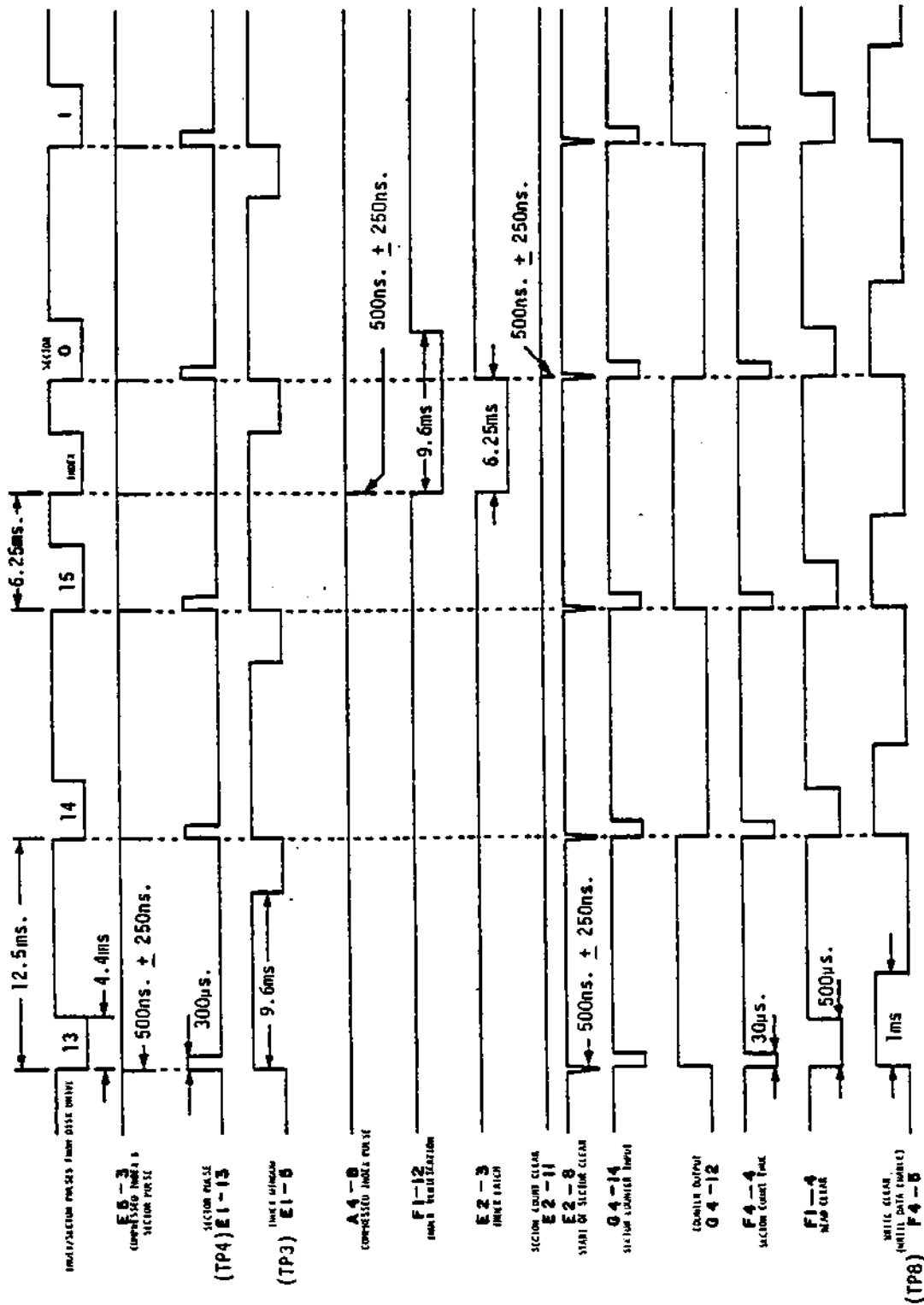
Figure 4-5. Index/Sector Timing

falling edge enables E3 pin 8 LOW. When E3 pin 8 goes LOW, E2 pin 8 is disabled. When E2 pin 8 is disabled HIGH, the Sector Count True One Shot, F4 pin 4 (zone A7), toggles LOW for 30μs. If it is the first Sector pulse after the Index pulse, the Index Latch, E2 pins 3 and 6 (zone A5) is reset, forcing E2 pin 3 HIGH. The LOW at E2 pin 8 also appears on board 2 (Figure 4-15, Sheet 1, zone A8) as the START OF SECTOR CLEAR (SOS) signal, which clears the Write Circuit at the end of a Write mode.

After a valid Index pulse has been detected, A4 pin 8 (Figure 4-14, Sheet 1, zone B5) is enabled LOW, setting the Index Latch with E2 pin 3 LOW. When E2 pin 3 is LOW, the Index Latch Pulse Compressor, F3 pin 13 (zone B5), is cleared. A4 pin 8 also triggers F1 pin 12 (zone B3) LOW for 9.6ms. After 6.25ms , the Index Latch is reset by a Sector pulse, leaving E2 pin 3 HIGH. E2 pin 11 (zone B5) is enabled LOW until the Index Latch Pulse Compressor Flip-Flop, F3 pin 13, is clocked by the 2MHz Clock pulse. The 500ns. ($\pm$250ns) output pulse at E2 pin 11 is dependent on the propagation time of F3 pin 13 and the delay time of the RC time constant of R8 and C20. A2 pin 1 (zone C3) is HIGH for 500ns ($\pm$250ns) if F1 pin 12 (zone B3) has been triggered LOW. This clocks B3 pin 8 (zone C3) LOW if B3 pin 7, the HEAD STATUS (HS) signal, is HIGH. HEAD STATUS should go HIGH 50ms. after the head is loaded on the Disk. A LOW at B3 pin 8 indicates that the correct Index pulse has been detected. The Index Latch, in allowing E2 pin 11 to be enabled, also resets the 4 Bit Sector Counter, G4, at pins 2 and 3 (zone A3), and the 5th Bit Sector Count Flip-Flop, F3 pin 6 (zone B4). Since this occurs on the first Sector pulse after the Index pulse, a correct Sector count is guaranteed every revolution. INPUT SECTOR STROBE (Channel 011_8) is enabled when A2 pin 4 (zone C2) goes HIGH. This occurs only when the Index Verification Flip-Flop is set (B3 pin 8 LOW) and the HEAD STATUS signal is LOW, indicating that the head is properly loaded for reading and writing. Drivers H5 pins 9, 11, 5, 7, 3 and 13 (zone B2) are then enabled when A3 pin 8 (zone B3) goes LOW. The Sector count is then transferred to the bus. The correct Sector is located by comparing the desired Sector number with the Sector count from this Index/Sector Circuit. Software also checks DIO to see if it is the beginning of the Sector.

When the Sector Count True One Shot, F4 pin 4 (zone A7), is triggered LOW for 30μs , Write Clear One Shot, F4 pin 5 (zone A5), goes HIGH for 1ms. F4 pin 5 is a timer that prevents Write Data (other than 0's) from begin written during the first 1ms. of a Sector by inhibiting the request for Write Data. When F4 pin 5 goes LOW, J3 pin 10 (zone A2) goes HIGH, enabling the Write Circuit to request Write Data. F1 pin 4 (zone B4) is also triggered by the Sector Count True One Shot, F4. F1 pin 4 is a timer that turns off the Read Circuit at the beginning of every Sector by going LOW for 500μs. This prevents the reading of false data at the beginning of a Sector, and insures proper synchronization with the Read Clock for detection of the sync bit.

4-9. READ CIRCUIT ($\emptyset12_8$ - INPUT)

Composit Read Clock and Data consisting of LOW going 1μs. pulses is received from the Disk Drive at Read Data Mask Gate, E5 pin 4 (Figure 4-14, Sheet 2, zone B6). The Read Clock pulse occurs every 8μs ($\pm$1μs), and the Read Data pulse occurs 4μs later if it is a logic 1 (refer to Figure 4-6). When a clock pulse is received, E5 pin 6 is enabled HIGH, triggering Read Clock One Shot, A1 pin 4 (zone B6), LOW for 2μs. This LOW is present at the Read Data Window Gate, A4 pin 13 (zone B4). A1 pin 13 is HIGH for 2μs , triggering the Read Data Window Gate, A1 pin 5 (zone B4), HIGH and A1 pin 12 LOW for 6.1μs. A1 pin 4 returns HIGH after 2μs., leaving A4 pin 13 and the Read Data Bit Latch, G2 pin 9 (zone B3) HIGH. If a logic 1 data bit is received at E5 pin 4, it is inverted HIGH by E4 pin 2 (zone B4), allowing A4 pin 12 (zone B4) to go LOW. This sets the Read Data Bit Latch, G2 pin 6 (zone B3) HIGH, indicating a logic 1 data bit has been received. After 6.1μs, A1 pin 12 (zone B4) returns HIGH and clocks the Read Data Serial to Parallel Shift Register, G1 pin 8 (zone C4). Serial Data at G2 pin 6 (zone B3) is then transferred to G1 pins 1 and 2. The Read Data Bit Latch is reset when A1 pin 4 (zone B6) receives the next clock pulse from the Disk Drive and returns LOW. If a logic $\emptyset$ data bit is received at E5 pin 4 (zone B6), the Read Data Bit Latch remains reset (G2 pin 6 LOW) and a logic $\emptyset$ is clocked into the Divide By Eight Counter, B1 (zone D6).
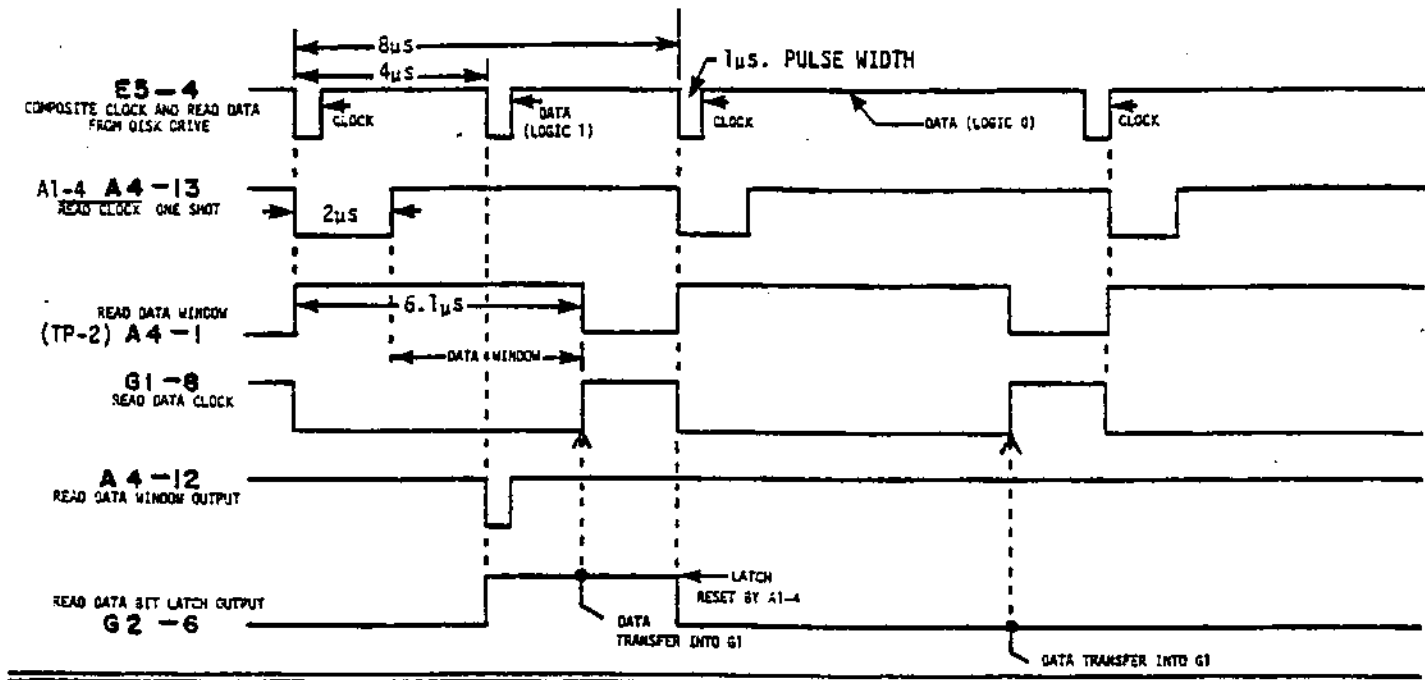
Figure 4-6. Read Circuit Timing

The sync bit is the first logic 1 data bit detected after the
500μs READ CLEAR pulse at the beginning of every Sector. B1 is held
in a LOAD condition (does not count) until the sync bit is detected.
Since Write Data is not enabled for 1ms from the beginning of a Sector,
Read Data will not be available during that time. The Devide by Eight
Presettable Counter, B1 (refer to Figure 4-7), counts eight read clocks
and toggles on the trailing edge of the $\overline{Q}$ output at A1 pin 12 (zone B4).
A2 pin 11 (zone D5) goes HIGH every 64μs. on the leading edge of the
clock pulse at B1 pin 2. G1 pin 13 (zone C4) goes HIGH seven read data
clocks after the sync bit has been detected and clocks the Sync Bit
Detector Flip-Flop, B2 pin 8 (zone C7) LOW. B1 pin 15 returns LOW
after 8μs., allowing A2 pin 13 (zone D5) to go HIGH. This enables G2
pin 3 (zone D4) LOW for 500ns. (+250ns) until the Read Latch Pulse
Compressor Flip-Flop, F2 pin 1 (zone D7), is clocked. The output pulse
width is dependent on the propagation time of the flip-flop and the
delay time of the RC time constant of R21 and C29. When the Read Latch
Pulse Compressor Flip-Flop, F2 pin 13, is clocked by the 2MHz Clock
pulse at F2 pin 1, F2 pin 13 is enabled LOW, disabling G2 pin 3 (zone
D4). When G2 pin 3 is enabled LOW and inverted by J3 pin 6 and J3

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pin 4 (zone D3), data present at G1 outputs A through H is transferred to the D_A through D_D inputs of Read Data Latches, G3 (zone D3) and H1 (zone C3). The HIGH at J3 pin 6 also clocks the New Read Data Available Flip-Flop, B3 pin 13 (zone C6) LOW, enabling the New Read Data Available (NRDA) Status signal at H2 pin 14 (zone B2). As G2 pin 3 returns HIGH, the clock inputs of latches G3 and H1 go LOW and latch the data present at the D_A through D_D inputs to the Q_A through Q_D outputs. When an input is done on Channel 012_8 (INPUT READ DATA STROBE), line drivers H4 pins 9, 3, 5 and 7 (zone D2) and H3 pins 5, 7, 3 and 9 (zone C2) allow data at outputs Q_A through Q_D to be transferred to the Altair Data Bus.
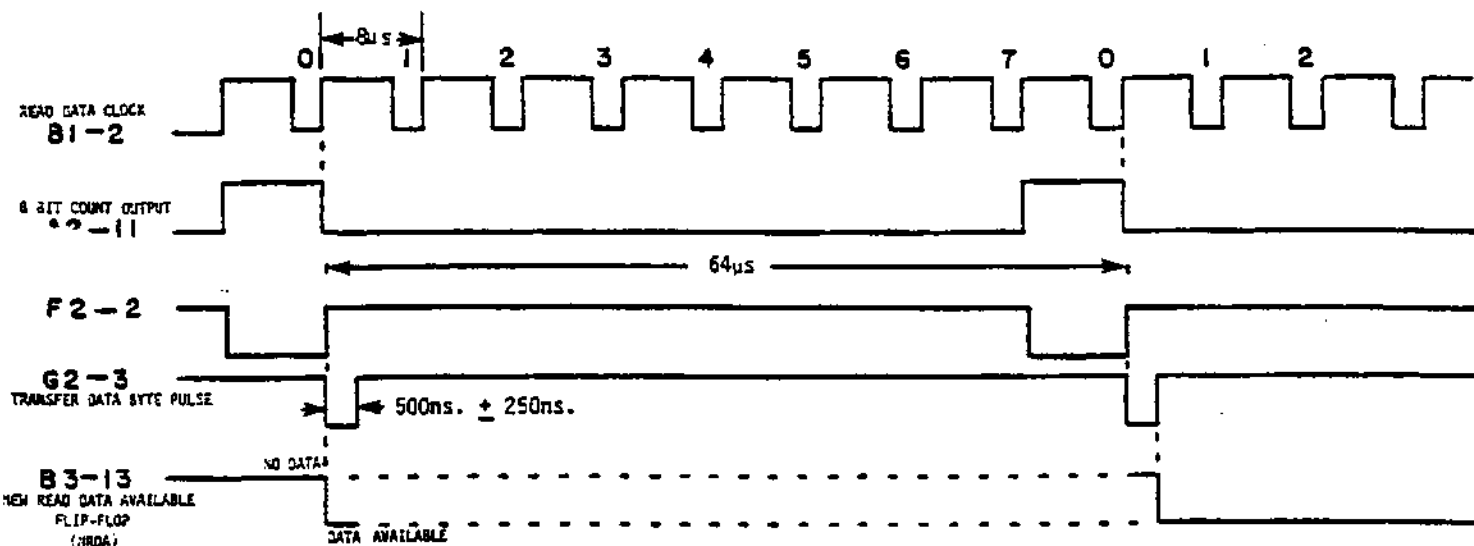
Figure 4-7. Read Timing

At the beginning of every Sector, the Read Clear One Shot, F1 pin 4 (Figure 4-14, Sheet 1, zone B4), goes LOW for 500µs clearing the Divide By Eight Presettable Counter, B1; the Sync Bit Detector Flip-Flop, B2; and the Read Data Serial to Parallel Shift Register, G1. When INPUT READ DATA STROBE goes LOW, the New Read Data Available Flip-Flop, B3, is cleared.

4-10. STATUS CIRCUIT (010_8 - INPUT

When an input is done on Channel 010_8, Disk Status information
(Figure 4-14, Sheet 2, zone B2) is transferred to the Altair Data Bus.
Status signals include HEAT STATUS (HS), MOVE HEAD (MH), INTERRUPT
STATUS (INT STATUS), ENTER NEW WRITE DATA (ENWD), NEW READ DATA AVAIL-
ABLE (NRDA), and TRACK 0 (TRK 0). Track 0 is generated by the Disk
Drive unit and indicated when the head is on the outermost track. When
the INPUT STATUS STROBE is enabled LOW at A3 pin 6 (Figure 4-14, Sheet
1, zone C3), line drivers H3 pins 13 and 11 (Figure 4-14, Sheet 2, zone
C2) and H2 pins 5, 11, 9, 7, 3 and 13 (zone B2) are enabled, allowing
Status information to the Altair Data Bus.

4-11. DISK ENABLE CIRCUIT (010_8 - OUT)

When the DISK CONTROL LATCH STROBE (Channel 010_8 - OUT) is
enabled LOW for 500ns. (Figure 3-21, Sheet 1, zone C8) and inverted HIGH
at G2 pin 12 (zone C5), the Disk Address Latch, J3, and Disk Enable
Flip-Flop, A2 (zone C5), are clocked (refer to Figure 4-8). Data Out
Bus lines D$0$0-D$0$1 transfer the Disk address information through inver-
ters G4 pins 2, 3 and 4 to the Disk Address Latch, J3 pins 2 and 3.
As the clock goes HIGH at J3 pins 13 and 4, data is latched into the
D_A and D_B inputs, and as the clock returns LOW, data present at the D_A
and D_B inputs is transferred to the $\overline{Q}_A$ and $\overline{Q}_B$ outputs. The address
information then enables one of four possible Disk Drives through line
drivers K3 pins 5 and 7 (zone C2). The Disk Enable Flip-Flop, A2 pin 8
(zone C5), is clocked LOW, providing the DISK ENABLE signal through
line driver K3 pin 3 (zone C2) and the DISK ENABLE signal to B4 pin 1
(zone A7). A2 pin 8 also triggers the Disk Enable Timer, B3 pin 1
(zone C4) and the Drive Motor On Delay One Shot, B1 pin 1. The Drive
Motor Delay Flip-Flop, B1 pin 4 triggers LOW for 1 second when the Disk
Enable Flip-Flop is toggled LOW. E1 pin 8 (zone B4) is enabled HIGH
and the Disk Disable Flip-Flop (explained in Paragraph 4-15) is reset.
The Drive Motor On Delay Flip-Flop allows the Disk Drive Motor time to
stabilize. B3 pin 13 is enabled HIGH for 3µs. 50 to 200ns. after the
Disk Drive is enabled, the DISK POWERED line goes LOW at the Disk Reset
One Shot, B3 pin 11 (zone C4). This prevents the Disk Reset One Shot
from being triggered by the Disk Enable Timer.
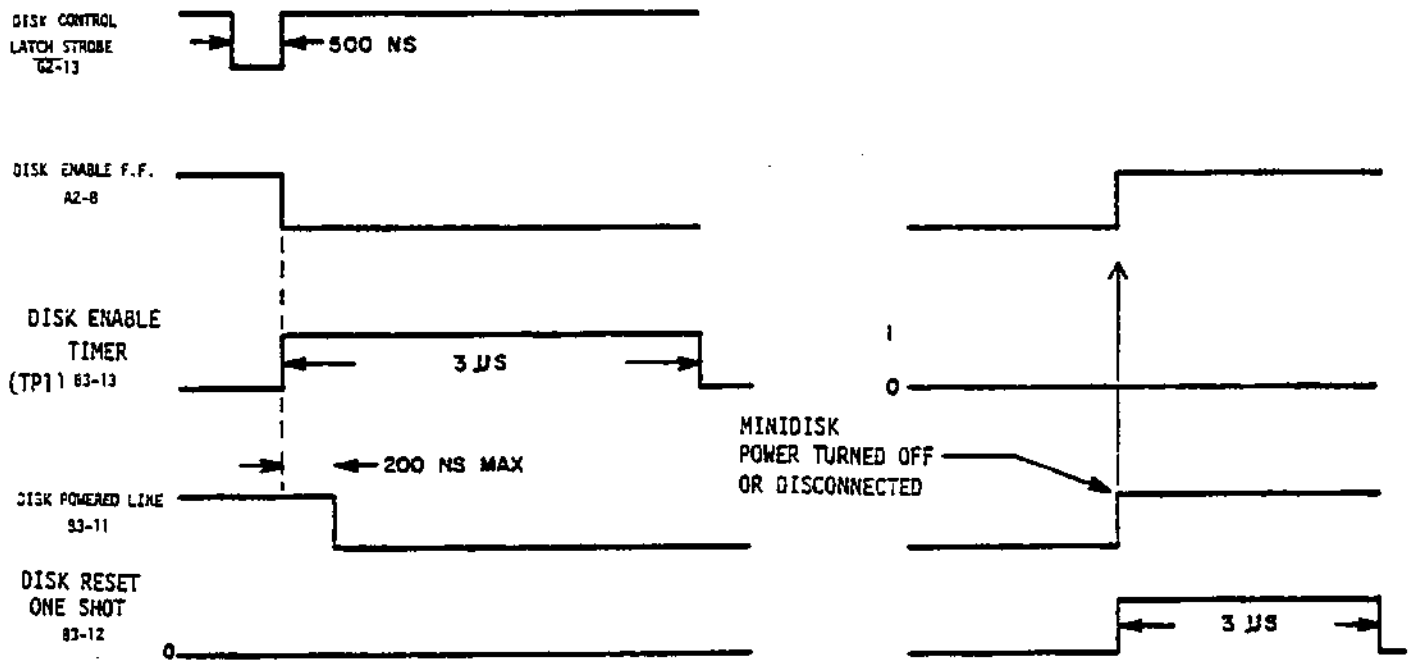
Figure 4-8. Disk Enable Timing With Valid Disk Address (board 2, sheet 1)

If a Disk is not connected, there is no power, the DISK POWER line stays HIGH at B3 pin 11 (zone C4), allowing B3 pin 9 to be triggered. B3 pin 12 is triggered LOW for 3µs , enabling E1 pin 11 HIGH (refer to Figure 4-9). This leaves F3 pin 13 (zone C5) LOW and the Disk Enable Flip-Flop, A2, is cleared. A2 is also cleared when POC (POWER ON CLEAR) is LOW or by the DISK CONTROL LATCH when Data line D07 is HIGH. This allows F3 pin 13 LOW, clearing A2 pin 6. When D07 (zone C8) is HIGH, it is inverted LOW by H4 pin 8 (zone C7), leaving F3 pin 8 (zone C6) LOW. When the DISK CONTROL LATCH goes LOW, F3 pin 10 is enabled HIGH. This leaves F3 pin 13 LOW, and the Disk Enable Flip-Flop is cleared.

DISK CONTROL
LATCH STROBE
G2-13 — 500 NS

DISK ENABLE F.F.
A2-8

DISK ENABLE
ONE SHOT
(TP1) A3-13 — 3 US

DISK POWERED LINE
B3-11

DISK DISABLE
ONE SHOT
B3-12 — 3 US
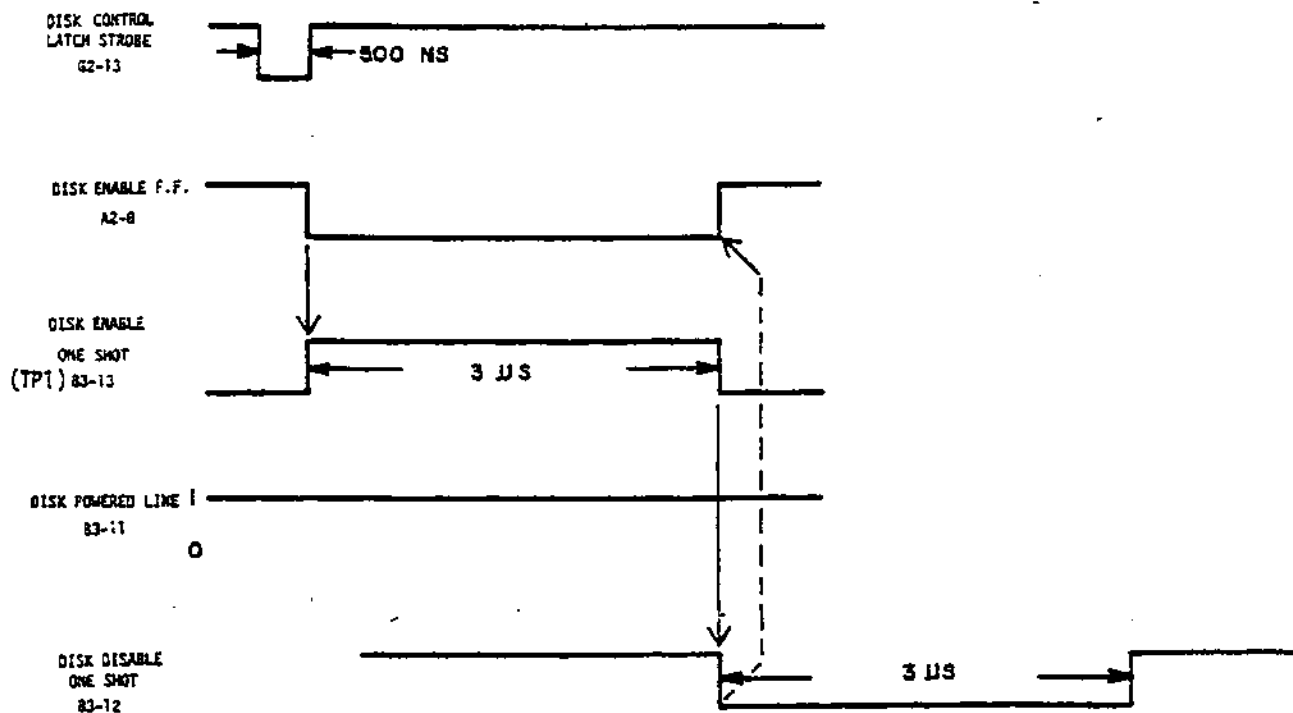
Figure 4-9. Disk Enable Timing With Invalid Disk Selection (board 2, sheet 1)

4-12. WRITE CIRCUIT (012_8 - OUT)

Software detects Sector True status, and the desired Sector is located. An output to Channel 011_8 (CONTROL DISK STROBE), with data line D07 inverted LOW, enables J1 pin 10 (Figure 4-15, Sheet 1, zone A7) HIGH. This toggles the Write Enable Flip-Flop, E2 pin 9 (zone A5), HIGH for 12.5ms. The HIGH at E2 pin 9 is present at E3 pin 1 (zone D7) and provides the (WRTEW) Write Enable signal to the Drive. When E2 pin 9 goes LOW, the Counters and Shift Registers H2, A3 and A4 are cleared.

The WRITE DATA ENABLE signal (refer to Figure 4-10) is generated when the Sector Count True One Shot, F4 pin 4 (Figure 4-14, Sheet 1, zone A7), is enabled LOW for 30µs , triggering the Write Clear One Shot, F4 pin 5 (zone A5), HIGH for 1ms. The HIGH at F4 pin 5 is inverted LOW at J3 pin 10 (zone A2) and presented to New Write Data Request Flip-Flop, J4 pin 2 (Figure 4-15, Sheet 1, zone D2). The 1ms. delay inhibits the ENTER NEW WRITE DATA request at the beginning of a Sector. After 1ms , J4 pin 2 goes HIGH. J4 pin 6 is toggled LOW by the next pulse from the Write Byte Counter, A4 (zone D3). J4 pin 6

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goes LOW every 64μs. The LOW pulse width of the ENTER NEW WRITE DATA
Status pulse depends on software, and each pulse is cleared upon an
output to WRT (WRITE) DATA STROBE (Channel 012_8).
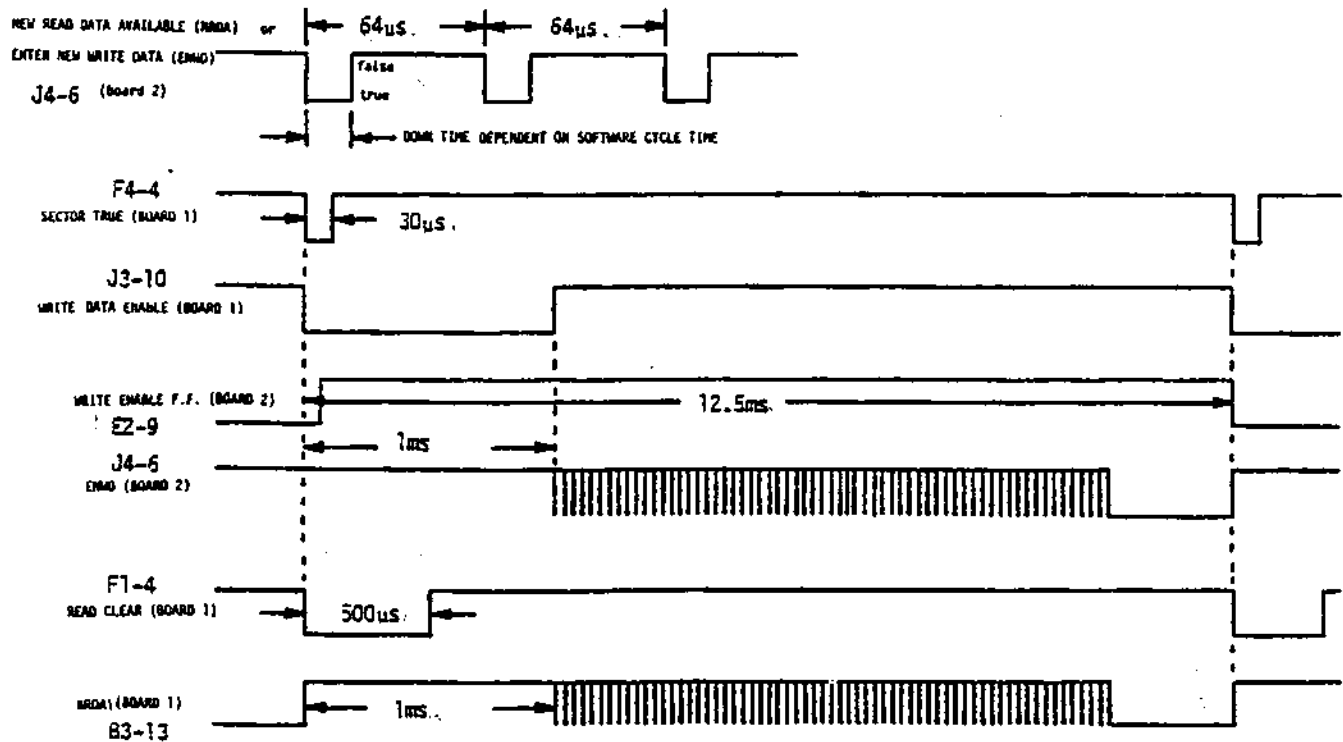
Figure 4-10. Minidisk Read/Write Timing

The Parallel to Serial Write Data Shift Register (zone D6) must
not be clocked during the 1ms. delay at J4 pin 2. Clocking is inhibited
when CLOCK INHIB (Clock Inhibit), H2 pin 6 (zone D6), is HIGH. Since
WRT ENABLE at E3 pin 1 (zone D8) is initially LOW and WRT (Write) DATA
STROBE at E3 pin 5 (zone D7) is initially HIGH, E3 pin 3 (zone D7) is
HIGH. Logic 0 bits are written to the Disk Drive during the first 1ms.
because H2 is not clocked, and output pin 13 which is cleared by a LOW
on the WRT ENABLE line before the Write Circuit was enabled, is at logic
0. When J4 pin 6 (zone D2) is enabled LOW, software detects ENTER NEW
WRITE DATA Status True and outputs the first byte to Channel 012_8,

enabling WRT DATA STROBE LOW. The first D7 bit written, the sync bit, must be logic 1. When WRT DATA STROBE is LOW at E3 pin 5 and E3 pin 1 is HIGH, E3 pin 3 is enabled LOW. CLOCK INHIB is then LOW, allowing H2 to shift data when clocked at pin 7.

In addition to allowing H2 to be clocked, WRT DATA STROBE also strobes data into Write Data Latches H3 and G3 (zone C6). Data present on Altair Data Out Bus, DØ0 through DØ7, is inverted by G4 pins 2, 4, 6, 10 and 12 and H4 pins 8 and 10, and transferred to the Disk Drive Control Signal Decoders (zone B6) and to the D_A through D_D inputs of Write Data Latches, H3 and G3 (zone C6). When H3 and G3 go HIGH at pin 13, data is latched into the D_A through D_D inputs. WRT DATA STROBE (Channel $\emptyset12_8$ - OUT) goes LOW for 500ns , is inverted HIGH by G2 pin 8 and G2 pin 10, and clocks H3 and G3. Data present at D_A through D_D is transferred to $\overline{Q}_A$ through $\overline{Q}_D$ when the clock at pin 13 goes LOW. Data is then available at PARALLEL DATA IN of Parallel To Serial Write Data Shift Register, H2 (zone D6). The Write Byte Counter, A4 (zone D3), counts eight 1μs. clock pulses from the Write Clock + Data Window Generator, A3 pin 15 (zone D4), to the Parallel To Serial Write Data Shift Register, H2 pin 15 (refer to Figure 3-11). On the eighth count, A4 pin 15 will go HIGH for 8μs. This HIGH is inverted LOW by B4 pin 12 (zone C3) to H2 pin 15 and enables the PARALLEL DATA INPUTS (Ø through 7). On the next H2 pin 7 clock pulse, data present at $\overline{Q}_A$ through $\overline{Q}_D$ of the Write Data Latches is synchronously loaded into the Shift Register.

In addition to clocking the Write Byte Counter, A4 pin 2, the Write Clock + Data Window Generator, when HIGH at A3 pin 15, provides the write clock pulse to F4 pin 12 (zone D2). A_{OUT}, B_{OUT} and C_{OUT} (zone D5) are gated together to provide the Write Data Window at E4 pin 6 (zone D3).

The Write Clock + Data Window Generator, A3, is enabled by the 1MHz Clock pulse (zone D8) at A3 pin 2. The 1MHz clock is derived by dividing the 2MHz Clock by 2 at J4 pin 9 (zone A4). In addition to clocking A3 pin 2, the 1MHz Clock is also present at F3 pin 3 (zone D6). On the eighth 1MHz Clock pulse, occurring every 8μs., A3 pin 15 (RC) is HIGH for 1μs and, after being inverted LOW by B4 pin 6 (zone D4), is present at F3 pin 2. When the 1MHz Clock pulse goes LOW at F3 pin 3, F3 pin 1 is enabled HIGH, clocking H2 pin 7. When H2 pin 15 (SHIFT/$\overline{LD}$) is HIGH, WRITE DATA is shifted serially out on H2 pin 12 (SERIAL DATA OUT). If a logic 1 is being written, the HIGH at H2 pin 13 is inverted by B4 pin 10 (zone D4) and Serial Write Data appears LOW to F4 pin 3 (zone D3). When A_{OUT} and B_{OUT} are HIGH, and C_{OUT} is inverted HIGH by G2 pin 6 (zone D4), E4 pin 6 (zone D3) is enabled LOW. F4 pin 1 (zone D3) is enabled HIGH, insuring F4 pin 13 is LOW (refer to Figure 4-11 and 4-12), and the Disk WRT DATA (Write Data) input is enabled through line driver K3 pin 9 (zone D2). The Write Data Windows (zone D3) are developed halfway between the write clocks which are generated every 8μs.

The Write Clock + Data Window Generator, A3, the Write Byte Counter, A4, and the Parallel To Serial Write Data Shift Register, H2, are cleared when WRT ENABLE (generated at E2 pin 9, zone A5) is LOW.
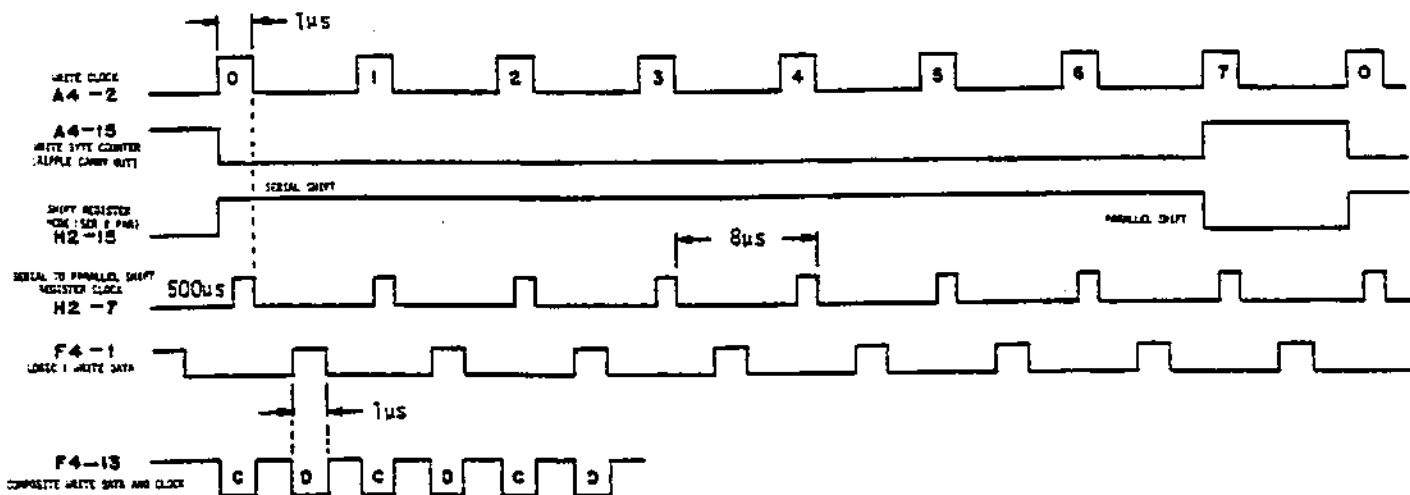
Figure 4-11. Write Circuit Timing
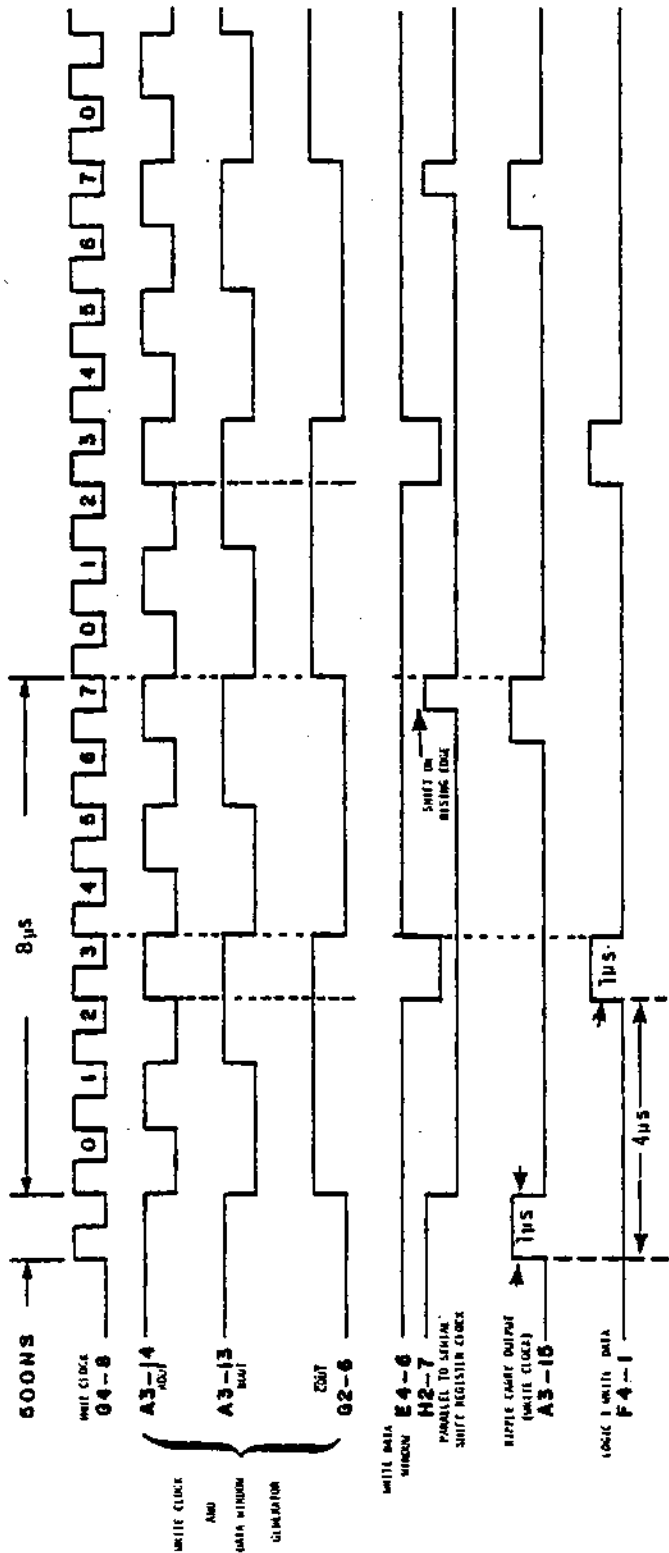
Figure 4-12. Write Timing

4-13. DISK FUNCTION CONTROL CIRCUIT (011_8 - OUT)

Channel 011_8 - OUT controls Disk operations when both Disk Drive and Controller are enabled. Data line D$0$0 through D$0$7 (Figure 4-15, Sheet 1, zone C8) transfer the control information from the Altair Data Out Bus to the Disk Drive unit. HIGH signals on the Data lines are inverted by G4 and H4 (zone C7) and appear as D$0$0 through D$0$7 at Control Signal Decoding Gates H1 and J1 (zone B7). Before the decoding gates can be enabled, the CONTROL DISK STROBE (011_8 - OUT) line (zone A8) must be enabled LOW (500ns. pulse). Refer to Figure 4-13 for timing diagrams relating to Disk Control functions discussed in Paragraphs 4-14 through 4-19.
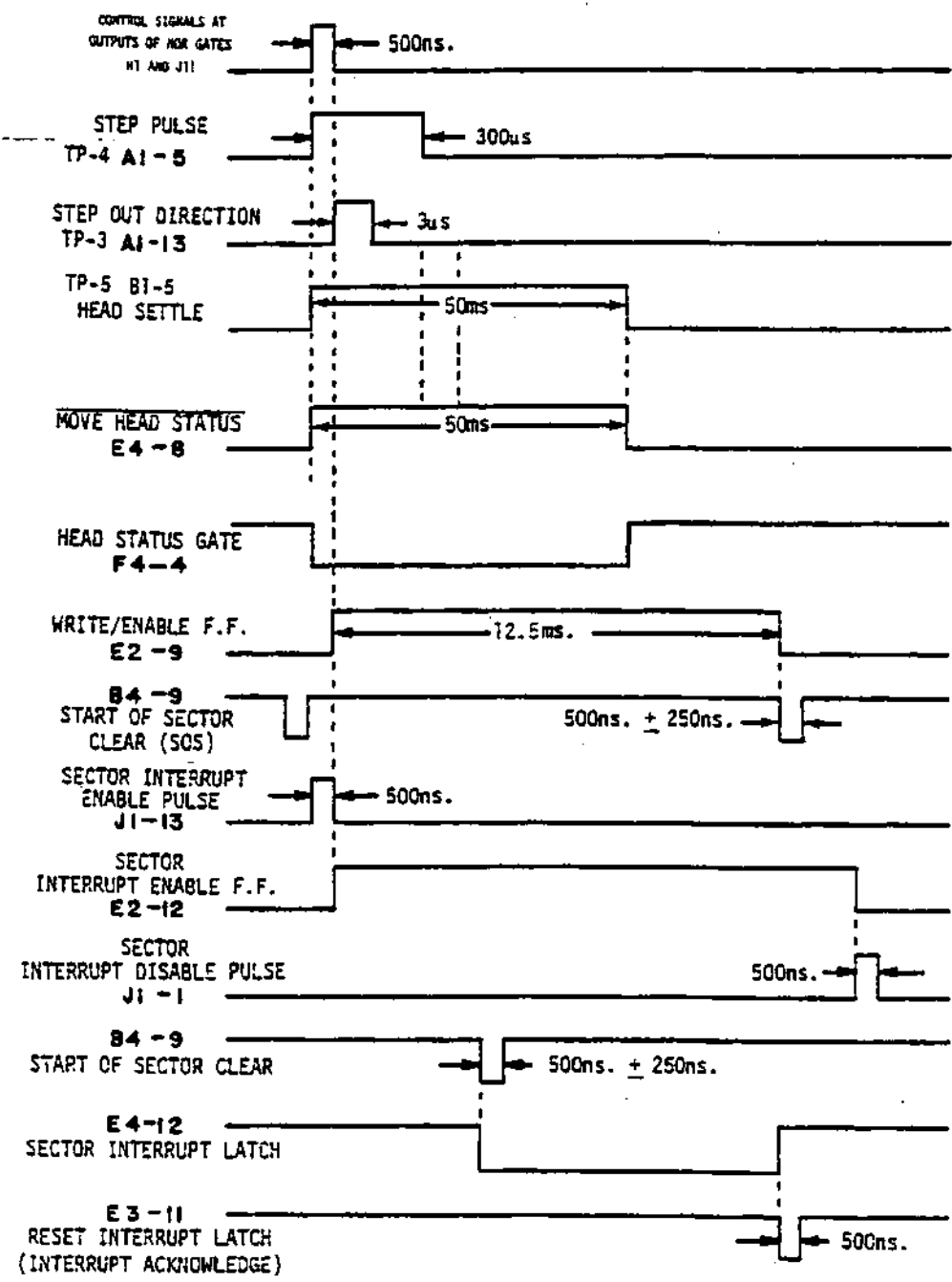
Figure 4-13. Disk Function Control Timing

4-14. Head Stepping

During an output to Channel 011_8, Control Disk Strobe (zone A8) pulses LOW, causing H1 pin 12 (zone B7) to pulse LOW. If DØ0 is HIGH, it appears LOW at H1 pin 11, causing H1 pin 13 to pulse HIGH. On the trailing edge of this pulse, A2 pin 1 (zone C4) is clocked, causing A2 pin 12 to go HIGH. This HIGH is inverted at J2 pin 5 (zone B2), causing a LOW on the STEP DIRECTION line indicating a STEP IN direction. H1 pin 13 is also connected to F1 pin 2 (zone B6), causing a LOW pulse on F1 pin 1 when either input pulses HIGH. The LOW going pulse at F1 pin 1 triggers the Step Pulse One Shot at A1 pin 9 (zone B5) which gives a .3ms positive pulse at A1 pin 5. This pulse is inverted at J2 pin 3 (zone B2), causing a LOW going Step Pulse. When the STEP DIRECTION line is LOW, the trailing edge of the .3ms Step Pulse causes the Minidisk head to be moved in one track (to higher numbered tracks) towards the center of the Minidiskette.

If DØ1 is HIGH when outputting to Channel 011_8, LOWs appear at H1 pins 8 and 9 (zone B7), causing a HIGH pulse at H1 pin 10. The trailing edge of this signal triggers A1 pin 1 (zone B4), causing a 3us. pulse at A1 pin 4 clearing A2 pin 2. With A2 pin 12 LOW, the STEP DIRECTION line goes HIGH, indicating the STEP OUT direction. The HIGH going pulse at H1 pin 10 also causes F1 pin 1 to pulse LOW, resulting in a Step Pulse as described in the preceding paragraph. When the STEP DIRECTION line is HIGH, the trailing edge of the .3ms Step Pulse causes the Minidisk head to move out one track towards the outer edge (lower numbered tracks). Note that if DØ0 and DØ1 are both HIGH during an output to Channel 011_8, the STEP OUT direction will always be selected due to the clearing action on the Step Direction Flip-Flop, A2.

4-15. Disk Disable Timer

F1 pin 1 is normally HIGH and goes LOW when a step command is received. This enables A1 pin 5 HIGH for 300μs and B1 pin 12 LOW for 50ms (explained in Section 4-16). The pulse at F1 pin 1 is also present at E4 pin 10. After being inverted by J2 pin 3 (zone B1), the HIGH at the Step Pulse One Shot, A1 pin 5, provides the STEP PULSE signal to the Disk Drive. The HIGH at A1 pin 5 is also present at F1 pin 5, enabling F1 pin 4 LOW. This allows E1 pin 8 (zone B4) to go HIGH which resets the Disk Disable Timer, B2, keeping the system enabled. The Disk Disable timer turns the system off after 6.4 seconds if there is no head movement or the Timer is not reset by software. The Timer is clocked every 12.5ms by the START OF SECTOR CLR pulse, occurring at the beginning of each Sector.

When DØ2 is HIGH at bus pin 88 (zone C8) and an output is done to Control Disk Strobe, H1 pin 4 is enabled HIGH, allowing F1 pin 4 LOW. E1 pin 8 is then allowed HIGH and the Disk Disable Timer is reset. This command should be issued before every Read or Write operation to insure the 88-MDS continues to be enabled.

4-16. Move Head Status

If a step command is received, F1 pin 1 goes LOW and B1 pin 9 (zone B3) is triggered LOW, causing B1 pin 12 (zone B3) to go LOW for 40ms. While B1 pin 12 is LOW, E4 pin 8 (zone B2) remains HIGH, indicating that the head is being stepped. The Head Settle One Shot holds E4 pin 8 HIGH, allowing time for the head to settle before the Move Head Status True (LOW) signal is generated. The Move Head signal is also False (HIGH) during the Write mode as E2 pin 8 (zone A5) is enabled LOW, having gate E4 disabled (E4 pin 8 HIGH).

4-17. Head Status

Although the head is loaded when the Drive is enabled, a one
second delay is required for the motor speed to stabilize when the Drive
is first enabled. B1 pin 1 is triggered by A2 pin 8 (zone C5) going LOW
when a Drive is enabled, causing a one second LOW pulse at E1 pin 9.
E1 pin 8 (zone B4) goes HIGH and F4 pin 4 is enabled LOW. Inverted at
B5 pin 8 (board 1, sheet 2, zone B2) the HIGH (False) Head Status signal
is generated. Head Status (HS) also goes False (HIGH) for 50ms. during
a step command when E4 pin 8 is held HIGH, enabling F4 pin 4 (zone B4)
LOW. When the signal is inverted on board 1, $\overline{\text{Head Status}}$ is False
(HIGH). When $\overline{\text{Head Status}}$ is False (HIGH) on board 1, Sector information
is inhibited and no reading or writing of data is permitted. When
$\overline{\text{Head Status}}$ is LOW, reading or writing of data is allowed.

4-18. Enable Interrupts

When $\overline{\text{D}\emptyset 4}$ goes LOW, J1 pin 13 (zone B7) is enabled for 500ns ,
applying a clock pulse to Interrupt Enable Flip-Flop, E2 (zone B3). E2
pin 12 is enabled HIGH and present at Interrupt Latch, E4. E4 pin 12
(zone A3) is normally HIGH in a Reset condition. E3 pin 11 (zone A3),
is normally HIGH and applied to E4 pin 1 when an interrupt is acknow-
ledged by the computer's Central Processing Unit (CPU). When START OF
SECTOR CLR (zone A8) goes LOW for 500ns. (+250ns) at the beginning of
each Sector, E4 pin 12 is latched LOW providing the Disk Drive INTERRUPT
signal. When PDBIN and SINTA (zone A8) go HIGH for 500ns. and 1.5µs ,
respectively, E3 pin 11 goes LOW and E4 pin 12 is reset HIGH.

Flip-Flop E2 pin 12 is cleared LOW when J1 pin 1 (zone A6) goes
HIGH for 500ns. E1 pin 6 (zone A6) is HIGH and inverted LOW at H4 pin
2 (zone A5), clearing Flip-Flop E2. Software must enable interrupts
in the CPU and have an appropriate service routine in memory to enable
the INTERRUPT signal.

MINI DISK CONTROLLER BOARD TIMING

CONTROLLER BOARD #1

TP	PULSE WIDTH	NAME	
1	2.0µS ($\frac{1.6}{2.4}$)	READ CLOCK	
2	6.1µS ($\frac{5.9}{6.3}$)	READ DATA WINDOW	
3	9.6MS ($\frac{7.6}{11.6}$)	INDEX WINDOW	
4	300µS ($\frac{150}{600}$)	SECTOR PULSE	
5	500µS ($\frac{400}{600}$)	READ CLEAR	
6	9.6MS ($\frac{7.6}{11.6}$)	INDEX VERIFY	
7	30µS ($\frac{20}{40}$)	SECTOR COUNT	
8	1.0MS ($\frac{0.9}{1.2}$)	WRITE CLEAR	

CONTROLLER BOARD #2

TP	PULSE WIDTH	NAME	
1	3µS ($\frac{1.5}{4.5}$)	DISK ENABLE	
2	3µS ($\frac{1.5}{4.5}$)	DISK RESET	
3	3µS ($\frac{1.5}{4.5}$)	STEP OUT	
4	.3MS ($\frac{200µS}{400µS}$)	STEP	
5	50MS ($\frac{45}{75}$)	HEAD SETTLE	
6	1 SEC ($\frac{0.9}{1.5}$)	DRIVE MOTOR ON DELAY	
7	NOT USED	——	
8	NOT USED	——	

Shep

Pulse Width Formulae for One-Shots

For 74123, ~~74L~~ 74L123

$$\text{Pulse Width} = K \, RC \left(1 + \frac{.7}{R}\right)$$

Where K = .28 FOR 74123
K = .33 FOR 74L123
K = .25 FOR 74123 WITH DIODE
K = .29 FOR 74L123 WITH DIODE

For Approximation, Use Pulse Width = .3RC

For 74221, 74LS221

$$\text{Pulse Width} = (L_N 2) RC \quad \text{or}$$
$$.7 RC$$

Shep

Section V
Minidisk System
Preliminary Checkout

5-1. DISK ENABLE TEST

The following program is used to check the primary functions of the Altair Minidisk System. Since it is a static test, it does not check actual data transfers or the Read/Write circuitry. It is useful to identify the possible areas of malfunction as a first step of trouble-shooting.

Since the Disk Disable Timer will turn the system off 6 seconds after it is enabled, the timer should be disconnected for this test. This is done by removing IC B2 on Minidisk Board #2 (4020), bending pin 10 up and placing B2 back in its socket with no connection to pin 10. After the necessary tests are completed, it is important that B2 pin 10 is returned to its proper connection.

When using this test program, use Drive address 0 and be sure there is a Minidiskette in the Drive.

Single step the following program:

Test #	Address		Instruction
1	000,000	076	MVI A
	1	000	Drive Address 0
	2	323	Output to:
	3	010	Disk Enable Channel
2	4	333	Input from:
	5	011	Sector Count Channel
3	6	333	Input from:
	7	010	Status Channel

Test #1

Examine address 000,000, and single step five times. The Minidisk Drive should now be enabled with the motor on and the head loaded. Failure to enable the Drive at this point could be the result of defective Disk Board #1 addressing circuitry, the Disk Enable circuitry on Minidisk Board #2, interconnect cable or the Minidisk Drive itself.

Test #2

After enabling the Minidisk Drive in Test 1, single step two more times. The Altair 8800 front panel Data lights should display the Sector Position Register as follows:

D0 - ON all the time

D1 - ON all the time (flashing very fast)

D2 - Flashing very fast

D3 - Flashing fast

D4 - Flashing slowest

D5 - OFF all the time

D6 - ON all the time

D7 - ON all the time

Improper display of lights indicates problems on Disk Board #1 in the Index/Sector circuit. If all the lights stay on, the trouble is either in the Disk Board #1 Addressing circuit or in the Minidisk Drive.

Test #3

With the Minidisk Drive still enabled, single step the program three times. The Minidisk System Status should now appear on the Altair 8800 Data lights as follows:

D0 - ON (ENWD = Indicates Write Circuit is Not Requesting Data)

D1 - OFF (MH = OK To Step The Head)

D2 - OFF (HS = Head Properly Loaded)

D3 - OFF = No Function

D4 - OFF = No Function

D5 - ON if "INTE" On Front Panel Off

D6 - Indicates Track 0 = OFF if at TRK 0

D7 - ON Flickering (NRDA Indicates Read Circuit is Detecting Data)

If the lights do not appear normal, the circuit associated with the questionable light may be defective. If all lights are on, the trouble is probably in the Address Circuit on Disk Board #1.

5-2. ALTAIR MINIDISK CONTROLLER TIMING TEST POINTS

The Minidisk Controller PC cards are equipped with test points on the key timing circuits. Below are listed the test points, their associated circuit function and the positive pulse width for normal operation. These test points may be observed when running the Disk Read/ Write Test Program (see Paragraph 5-4).

<u>1</u>   <u>5K BOARD #1</u>

TP-1   Read Clock Mask - 1.6 to 2.4µs. Occurs every 8µs when
(CI A1-13) Drive enabled and not writing. Used to separate Read
            Clock from Read Data.

TP-2   Read Data Window - 5.9 to 6.3µs. Occurs every 8µs when
(IC A1-5)   Drive enabled and not writing. The most critical time
            constant, nominally 6.1µs. Used to separate Read Clock
            from Read Data.

TP-3   Index Pulse Window - 8.0 - 11.2ms. Occurs every 12.5ms
(IC E1-5)   when Drive is enabled. Used to separate Index pulses from
            Sector pulses.

TP-4   Sector Pulse Mask - 150 - 600µs. Occurs every 12.5ms
(IC E1-13) when Drive is enabled. Used to separate Index pulses from
            Sector pulses.

TP-5   Read Clear - 400 - 600µs. Occurs every 12.5ms when Drive
(IC F1-13) is enabled. Used to clear Read Circuit at beginning of
            Sector.

TP-6   Index Pulse Verification - 8.0 - 11.2ms. Occurs every 200
(IC F1-5)   ms when Drive is enabled. Used to insure proper detection
            of Index pulse when Drive first enabled.

TP-7   Sector True - 20 - 40 s. Occurs every 12.5ms when Drive
(IC F4-13) is enabled. Used to indicate beginning of Sector.

TP-8   Write Data Enable - 900 - 1200µs. Occurs every 12.5ms
(IC F4-5)   when Drive is enabled. Used to keep Write Registers
            cleared during start of Write operation so that zeros are
            written during first portion of Sector (preamble).

<u>MINIDISK BOARD #2</u>

TP-1   Disk Enable Timer - 1.5 - 4.5µs. Occurs when Disk is
(ICB3-13)   enabled. Used to insure proper enabling of Drive.

TP-2   Disk Reset - 1.5 - 4.5us. Occurs when Disk is disabled.
(IC B3-5)   Used to insure proper reset of Controller.

TP-3   Step Out Direction - 1.5 - 4.5µs. Occurs when step out
(IC A1-13) movement desired. Used to clear Step Direction Flip-Flop

READ: The Read Data is stored in memory, starting at address 001,236$_8$ and consists of the data written by the Write Program.

OUTPUT: After the Read Program, the data is output to a terminal (Teletype, CRT, etc.). The output program is set to output on Channel 1. To obtain a useful output pattern, change the sense switches until a desirable pattern is printed. The characters printed will consist of all printable ASCII characters in reversed order (as in 987654321 and ZYXWVU . . .). This pattern repeats itself and is easily observed for errors.

Program 5-I. Minidisk Read/Write/Output Test Program

TAG	MNEMONIC	ADDRESS	OCTAL CODE	EXPLANATION
	MVI(A)	000,000	076	
		1	000	Disk drive address
	OUT	2	323	
		3	010	Disk controller enable channel
LDHD	MVI(A)	4	076	
		5	004	Reset Timer Bit
	OUT	6	323	
		7	011	Disk function control channel
WRTLP	IN	10	333	Input # of bytes to be written
		11	377	Sense switch
	MOV(C)←(A)	12	117	Store in "C" reg.
	MVI(D)	13	026	Store in "D" reg.
		14	377	First write byte
	MVI(B)	15	006	Store in "B" reg.
		16	001	"ENWD" status mask
WSECT	IN	17	333	Write sector test
		20	011	Sector position channel
	CPI	21	376	
		22	300	$\emptyset$ sector
	JNZ	23	302	Jump if not start of $\emptyset$ sect.
		24	017	to "WSECT"
		25	000	
	MVI(A)	26	076	
		27	200	Write enable bit
		30	323	
		31	011	Disk function control channel
FBYT		32	333	First byte test
		33	010	Disk status channel
	ANA(A)/(B)	34	240	Test for "ENWD" status
	JNZ	35	302	Jump if "ENWD" false (=1)
		36	032	to "FBYT"
		37	000	
	MOV(A)(D)	40	172	Move 377 into accum.
	OUT	41	323	Output first byte
		42	012	Disk data channel
INDAT	IN	43	333	Start of write data sequence
		44	010	Disk status channel
	ANA	45	240	Test for "ENWD" status
	JNZ	46	302	Jump if "ENWD" false (=1)
		47	043	to "WDAT"
		50	000	
	MOV(A)←(C)	51	171	Move "DATA" byte to accum.
	OUT	52	323	
		53	012	Disk data channel
	DCR(C)	54	015	Decrement "DATA" byte
	JNZ	55	302	Jump if data byte = $\emptyset$
		56	043	to "WDAT", write another byte
		57	000	
	...	60	333	Start of zero byte

TAG	MNEMONIC	ADDRESS	OCTAL CODE	EXPLANATION
		.61	010	Output sequence
	ANA(A)←(B)	62	240	Test "ENWD" (last byte written)
	JNZ	63	302	Jump if "ENWD" false
		64	060 ⎤	To WZT
		65	000 ⎦	
	XRA(A)(A)	66	257	Zeros accumulator
	OUT	67	323	Output zero byte
		70	012	Disk data channel (end of write, start of read)
	LXI	71	041	Load H+L reg. with:
		72	236 ⎤	Starting addr. to store read data
		73	001 ⎦	
	MVI(B)	74	006	Store in "B" reg.
		75	200	"NRDA" mask
	NOP	76	000	
	NOP	77	000	
RSECT	IN	100	333	Read sector test
		101	011	Sector position channel
	CPI	102	376	
		103	300	Ø sector
	JNZ	104	302	Jump if not start of Ø sect.
		105	100	to "RSECT"
		106	000	
RDTST	IN	107	333	Start of "NRDA" test
		110	010	Disk status channel
	ANA(A)/(B)	111	240	Test for "NRDA" status
	JNZ	112	302	Jump if "NRDA" false (=1)
		113	107 ⎤	to "RDTST"
		114	000 ⎦	
	IN	115	333	Input read data
		116	012	Disk data channel
	MOV(M)←(A)	117	167	Store data in memory (H+L)
	INR(L)	120	054	Increment L reg. (mem addr)
	JNZ	121	302	Jump if L reg. ≠ 0
		122	107 ⎤	to RDTST
		123	000 ⎦	
	MOV(A)←(D)	124	172	Move 377 byte to accum.
	OUT	125	323	Disenable disk by output logic 1 on
		126	010	D7 to disk enable chan. (end of read, start of output)
	LXI(H+L)	127	041	Load H+L with:
		130	236 ⎤	Starting addr of data stored by read program
		131	001 ⎦	

TAG	MNEMONIC	ADDRESS	OCTAL CODE	EXPLANATION
*INIT	MVI(A)	000,132	076	
		133	003	
	OUT	134	323	
		135	020	Initialize 2SIO Port 20/21
	MVI(A)	136	076	
		137	021	
	OUT	140	323	
		141	020	
OTST	IN	142	333	Test Output Channel for Busy
		143	020	Status Channel
	ANI	144	346	And immediate
		145	002	Mask for bit D1
	JZ	146	312	Jump if D1 = 0 (busy)
		147	142	
		150	000	To "OTST"
	MOV(A)◄(M)	151	176	Move data PROM mem to Accum
	OUT	152	323	Output data
		153	021	To I/O port
	INR(L)	154	054	Increment L register
	JNZ	155	302	If L ≠ 0, output another
				byte, jump
		156	142	
		157	000	To "OTST"
	MVI(A)	160	076	
		161	000	Enable Disk
		162	323	
		163	010	
		164	303	Jump
**		165	004	
**000,166			000	To "LDHD"

*If using the old SIOA board, replace instructions from 000,132 with the following program.

**For R/W-step loop, change Data at (000,165) to 037; Data at (000,166) to 001.

TAG	MNEMONIC	ADDRESS	OCTAL CODE	EXPLANATION
OTST	IN	132	333	Test output device for busy
		133	000	Status chan. of terminal
	RLC	134	007	Test bit $\emptyset$. rotate into carry
	JC	135	332	Jump if carry (bit $\emptyset$ = 1)
		136	132	to "OTST"
		137	000	
	MOV(A)←(M)	140	176	Move data from mcm(H+L)
	OUT	141	323	Output data
		142	001	Data channel for term
	INR(L)	143	054	Increment L register
	JNZ	144	302	Jump if L reg ≠ 0, output another byte
		145	132	to "OTST"
		146	000	
	MVI(A)	147	076	
		150	000	Enable disk
	OUT	151	323	
		152	010	
	JMP	153	303	
NOTE		†154	004	To "LDHD"
		†155	000	
		156		
		157		

†For R/W-step loop, change Data at 000,154 to 037; Data at 000,155 to 001.

Read/Write/Output Program Flow Chart

START

(000,000)
ENABLE DISK #
AND LOAD HEAD

(000,010)
INITIALIZE REGISTERS:
REG B = "ENWD" MASK
REG C = NUMBER OF BYTES TO BE WRITTEN
REG D = FIRST BYTE WRITTEN (377)

(000,017)
BEGINNING OF SECTOR #? — NO / YES

(000,026)
TURN WRITE CIRCUIT ON

(000,032)
IS ENWD TRUE? — NO / YES

(000,040)
WRITE FIRST BYTE (377)

(000,043)
IS ENWD TRUE? — NO / YES

(000,051)
WRITE DATA BYTE FROM "C" REGISTER

(000,054)
DECREMENT C REGISTER

(000,055)
IS "C" REG = 0 ? — NO / YES

(000,060)
IS ENWD TRUE ?

#'S WRITTEN FOR REMAINDER OF SECTOR

(000,064)
WRITE 000

(000,071)
INITIALIZE REGISTERS
H - L REG = STARTING ADDRESS FOR STORING READ DATA IN MEMORY

B REG = "NRDA" MASK

(000,100)
BEGINNING OF SECTOR # ? — NO / YES

(000,107)
IS NRDA TRUE ? — NO / YES

(000,115)
INPUT READ DATA AND STORE IN MEMORY (ADDRESS SPECIFIED BY H - L)

(000,120)
INCREMENT L REGISTER

(000,121)
DOES L REGISTER = 0 — NO / YES

(000,124)
DISENABLE DISK DRIVE AND CONTROLLER

WRITE PROGRAM

READ PROGRAM

TO OUTPUT PROGRAM

TO OUTPUT PROGRAM

(000,127)
INITIALIZE H - L REGISTER WITH STARTING ADDRESS OF READ DATA STORED IN MEMORY

(000,132)
IS OUTPUT DEVICE READY TO RECEIVE DATA ? — NO / YES

(000,140)
OUTPUT DATA FROM MEMORY ADDR. AS SPECIFIED BY H - L REG

(000,143)
INCREMENT L REGISTER

(000,143)
IS L REGISTER = 0 — NO / YES

(000,147)
ENABLE DISK #

OUTPUT PROGRAM

FOR R/W - STEP LOOP

FOR R/W LOOP ONLY

(000,153)

JUMP TO STEP PROGRAM

JUMP TO WRITE PROGRAM

TO STEP PROGRAM

TO WRITE PROG.

82

88-MDS
July, 1973

5-5. Stepping Program

This program steps the Disk head out 34 times to TRACK 0 and then in 34 times to track 34, continuously repeating with the computer in the Run mode. This program is useful for testing the Disk Enable, MH status, TRACK 0 status, and stepping functions of the Disk. To loop with the Read/Write Program, see next section.

Drive Address

For Stepping Program, Disk Drive address of 000 is used. To change Disk Drive tested, the address is contained in location 001,001. For the Read/Write Test, the Drive address is in location 000,001 and 000,150 .

5-6. Looping With Stepping Program

To check the Read/Write and step functions simultaneously, the two programs may be run together by changing the following:

1) Data in locations 000,154 and 000,155 to 037,001 as indicated

2) Data in location 001,034 to 303 as indicated

Begin the program at 001,000, the start of the Stepping Program. The Disk head will step out to Track 0.

The head will then load and a Write/Read will occur. The head will then unload and output will take place. After output, the head will step in once, starting the Write/Read sequence again. After this repeats 34 times, the head is stepped out to TRACK 0, and it begins again.**

NOTE**: 1) For Read/Write program, Disk Drive address of 000 is used. To change Disk Drive tested, the address is contained in location 000,001 and 000,150.

2) Output device addresses are in locations 000,133 status and 000,141 data.

Program 5-II. Minidisk Stepping Program

TAG	MNEMONIC	ADDRESS	OCTAL CODE	EXPLANATION
STEP	MVI(A)	001,000	076	
		1	000	Disk drive addr 0
	OUT	2	323	Output (data-000) to
		3	010	Disk CTRL enable channel
NOS	MVI(E)	4	036	Initialize E register
		5	043	=35 (number of steps + 1)
SOUT	IN	6	333	Test "MH" status bit (move head)
		7	010	Disk status channel
	ANI	10	346	Test
		11	002	D1 mask
	JNZ	12	302	Jump if "MH" false (D1=1)
		13	006	To "SOUT"
		14	001	
	MVI(A)	15	076	
		16	002	Bit D1=1 (step out)
	OUT	17	323	Output (data 002) to
		20	011	Disk function control channel
	DCR(E)	21	035	Decrement step counter (E. reg.)
	JNZ	22	302	Jump if E reg ≠ 0
		23	006	to "SOUT"
		24	001	
TZ	IN	25	333	Test for track 0 status
		26	010	Disk status channel
	ANI	27	346	Test
		30	100	D6 mask
	JNZ	31	302	Jump if track 0 false (D6=1)
		32	025	to "TZ"
		33	001	
LOOP	NOP	*34	000	
	NOP	35	000	
	NOP	36	000	
SIN	IN	37	333	Test "MH" status bit (move head)
		40	010	Disk status channel
	ANI	41	346	Test
		42	002	D1 mask
	JNZ	43	302	Jump if "MH" false (D1=1)
		44	037	to "SIN"
		45	001	
	MVI(A)	46	076	
		47	001	Bit D0 = 1
	OUT	50	323	Output (Data 001) to
		51	011	Disk function control channel

TAG	MNEMONIC	ADDRESS	OCTAL CODE	EXPLANATION
	INR(E)	52	034	Add 1 to "E" register
	MVI(A)	53	076	
		54	042	34 steps
	CMP(A)/(E)	55	273	Compare "E" reg. to 34
	JNZ	56	302	Jump if "E" reg. ≠ 34
		57	034	To "Loop"
		60	001	to "Loop"
	JMP	61	303	Jump if "E" reg. = 34
		62	004	to "NOS"
		63	001	
		64		
		65		
		66		
		67		

*--Change to 303 for Step + R/W loop

MINIDISK STEPPING PROGRAM FLOWCHART

START (001,000)

ENABLE DISK
INITIALIZE "E" REGISTER WITH # OF
STEPS - 1

(001,006)
IS
"TH" STATUS
TRUE
?
NO / YES

(001,015)
STEP HEAD OUT
1 TIME

(001,021) DECREMENT
"E" REGISTER

(001,022)
IS
"E" REG
= 0
?
NO / YES

(001,025)
IS
TRACK 0
STATUS
TRUE
?
NO / YES

FOR
STEP
ONLY

(001,034)
JUMP
TO R/W PROGRAM

FOR RW/STEP LOOP

TO STEP IN
PROGRAM

[STEP OUT PROGRAM]

FROM STEP OUT PROG. OR
OUTPUT PROG.

(001,037)
IS
"TH" STATUS
TRUE
?
NO / YES

(001,046)
STEP HEAD IN
1 TIME

(001,052) INCREMENT "E"
REGISTER
(STEP COUNTER)

(001,053)
IS
E REG
= 34
?
NO / YES

(001,061)
JUMP TO BEGINNING OF
STEP OUT PROGRAM

[STEP IN PROGRAM]

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88-MDS
July, 1977

appendix A
parts list

88-MDDR Minidisk Disk Drive Parts List

Quantity	Component	MITS Part Number
1	7402 Integrated Circuit	101021
1	7406 Integrated Circuit	101054
1	7410 Integrated Circuit	101024
1	74367 Integrated Circuit	101040
1	7805 Voltage Regulator	101074
1	7812 Voltage Regulator	101085
2	.01μf 1KV	100305
2	.1uf 16V Disk Capacitors	100327
2	.1uf 50V Disk Capacitors	100312
2	35μf 50V or (35V @ 33uf) capacitors	100311
1	1000μf 25V Elect. Capacitors	100365
2	2200μf 25V Elect. Capacitors	100375
8	680 ohm 1/2W Resistors	102099
4	1K ohm 1/2W Resistors	101928
4	180 ohm 1/2W	101998
3	IN4004 Diode	100718
4	RL21 LED	100702
1	680 Style Cabinet, modified	100553
1	Minidisk Dress Panel	100554
1	Shugart SA-400 Drive	101606
1	Transformer	102612
1	SPST Toggle Switch	102366
1	Fuse Holder	101813
1	1A SB Fuse	101777
1	Power Cord	101742
1	5 Lug Terminal Strip	101713
1	10-Pin Socket Housing	101636
14	Socket Pins	101640
1	10-Pin Plug Housing	101635

Quantity	Component	MITS Part Number
8	Plug Pins	101639
4	Connector Shorting Strips	101641
1	4-Pin Socket AMP #1-480-424-0	101604
1	5-Pin Molex Socket	101873
4	Molex KK-156 Socket Pins	101769
2	2' #20 Orange Wire	103063
1	6' #20 Black Wire	103062
2	26-Pin Bulkhead Conn	101608
7'	26 Cond Flat Cable	103094
1	26-Pin Solder Conn	102505
1	Diskette (Blank)	102501
4	26 Pin Socket Conn	102506
12"	34 Cond Flat Cable	103095
1	34 Cond Solder Conn	102511
1	34-Pin Edge Conn	102512
1	Minidisk Buffer PC Card	100224
3	14-Pin Socket	102102
1	16-Pin Socket	102103
2	Regulator Socket	102121
1	4 Position SPDT Dip Switch	102321
1	5 Pin Molex KK-156 P.C. Plug	101872
4	Large Rubber Feet	101752
1	Fan (Pee Wee)	101711
1	3/16 Cable Clamp	103023
1	Strain Relief	101719
1	Serial # Sticker	101833
2	Tye Wraps	103037
1"	1/8' Heatshrink Tubing	103068
2"	1/2" Heatshrink Tubing	103071
9"	Duct Tape 2" Wide	103059
1	SPST Switch	102366
2	5/8 x 6" Channel Minidisk Mtg Bracket	101619
1	3/4 x 1 1/2 Rect Tubing Minidisk Heatsink	101610

Quantity	Component	MITS Part Number
4	#6-32 x 1" Pan Head Screw	100919
18	#6-32 x 3/8" Pan Head Screw	100925
8	#6-32 Nut	100933
23	#6 Lockwasher	100942
4	#4-40 x 1/2 Pan Head Screw	100903
4	#4-40 Nut	100932
4	#4 Lockwasher	100941
3	#6 Flatwasher	100943
4	#6-32 x 1/2" Black Oxide Screw	100972

88-MDS Minidisk Controller Parts List

Quantity	Component	MITS Part Number
5	74LS00 Integrated Circuit	101069
6	74LS02 Integrated Circuit	101136
8	74LS04 Integrated Circuit	101042
3	74LS10 Integrated Circuit	101133
1	74LS11 Integrated Circuit	101089
1	74LS20 Integrated Circuit	101134
1	74LS30 Integrated Circuit	101135
6	74LS73 Integrated Circuit	101119
2	74LS74 Integrated Circuit	101088
5	74LS75 Integrated Circuit	101117
1	7493 Integrated Circuit	101030
7	74123 Integrated Circuit	101100
1	74164 Integrated Circuit	101091
4	74367 Integrated Circuit	101040
2	7805 Voltage Regulator	101074
3	93L16 Integrated Circuit	101093
1	74166 Integrated Circuit	101092
1	8T98 Integrated Circuit	101045
1	4020 Integrated Circuit	101164

Quantity	Component	MITS Part Number
4	220 ohm 1/2W Resistor	101925
4	330 ohm 1/2W Resistor	101926
3	470 ohm 1/2W. Resistor	101927
10	1K ohm 1/2W Resistor	101928
8	10K ohm 1/2W Resistor	101932
2	15K ohm 1/2W Resistor	102083
1	22K ohm 1/2W Resistor	101933
3	33K ohm 1/2W Resistor	102053
1	47K ohm 1/2W Resistor	101934
2	IN914 or IN4148 Diode	100705
2	Heatsink	101870
2	#6-32 Hex Nut	100933
2	#6 Lockwasher	100942
10	#6-32 x 3/8" Pan Head Screw	100925
4	Card Guides	101714
3	Ferrite Bead	101876
2	#4-40 x 1/2" Pan Head Screw	100903
2	#4-40 Nut	100932
2	#4 Lockwasher	100941
1	420pf 5% Mica Capacitor	100322
1	910pf 5% Mica Capacitor	100356
3	470pf 10% Disk Ceramic	100316
1	.01μf 16V Disk Ceramic Capacitor	100321
39	.1uf 12V Disk Ceramic Capacitor	100348
2	.1uf 100V 5% Mylar Capacitor	100339
2	.68uf 100V 5% Mylar Capacitor	100343
4	33μf 16V Electrolytic Capacitor	100326
3	.001μf Disk Ceramic Capacitor	100328
1	5μf 25V Electrol Capacitor	100323
1	100μf 15V Electrol Capacitor	100357

Quantity	Component	MITS Part Number
1	Controller #1 PC Board	100216
35	14-Pin Socket	102102
23	16-Pin Socket	102103
1	10-Pin 90° KK-100 Wafer	101798
1	20-Pin 90° KK-100 Wafer	101788
13	Test Point Terminal	101663
3	Ferrite Beads	101876
1	Mini Disk #2 PC Board	100222
1	50-Pin 90° PC Flat Cable Conn.	102503
1	26-Pin Chassis Header	101608
18"	50 Cond. Flat Cable, #28 Strdd	103093
1	50-Pin Socket Conn.	102504
1	26-Pin Solder Transition Conn	102505
1	26-Pin Socket Connector	102506
1	31-Pin Single Row Conn.	102507
1	Adapter PC Board (DCCA)	100223
1	Minidisk System Manual	101571
2	100-Pin Edge Connector	101864
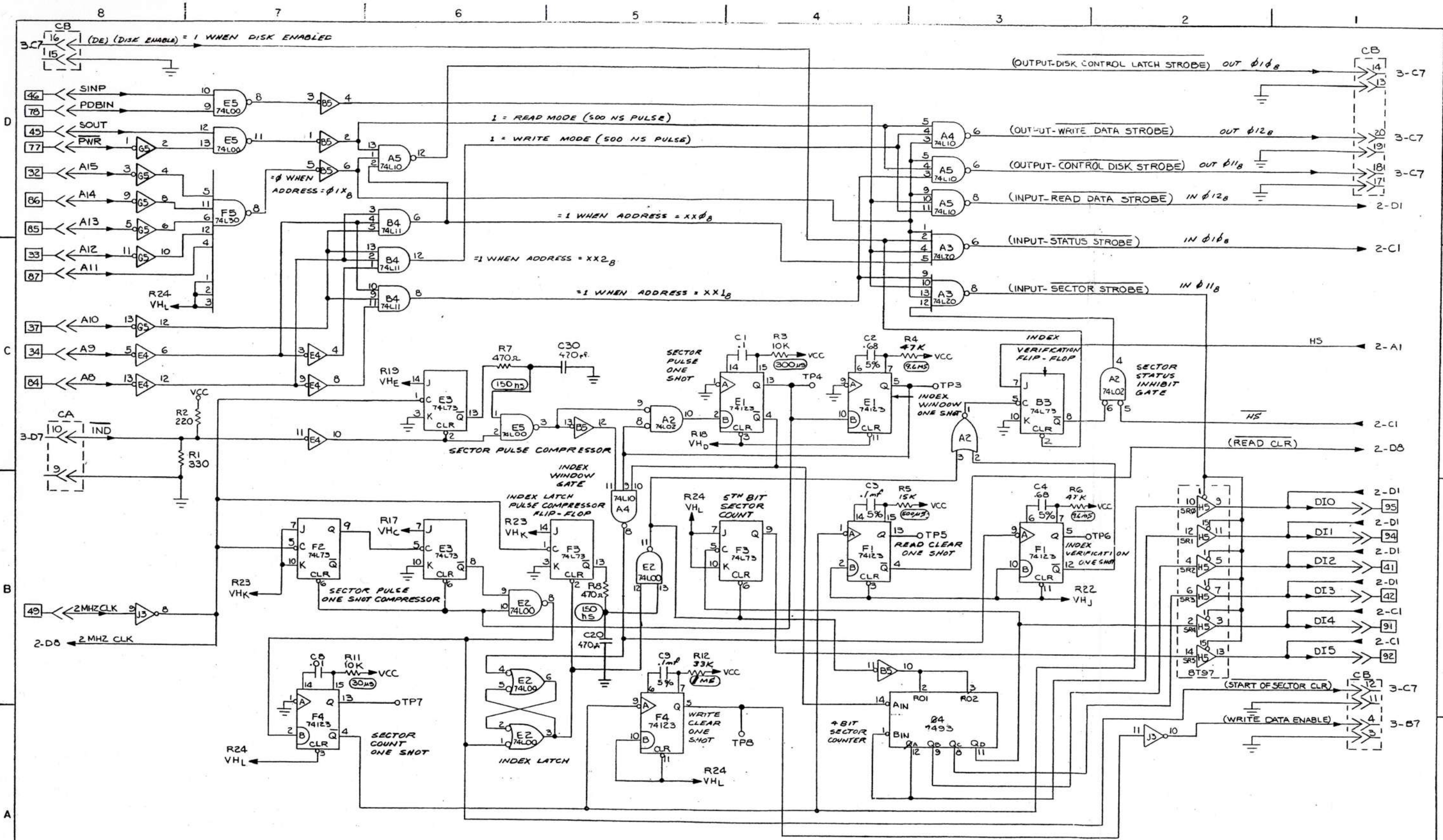
Figure 4-14.
Minidisk Controller Board #1   Sheet 1 of 3
Address/I-O Select and Sector Circuits
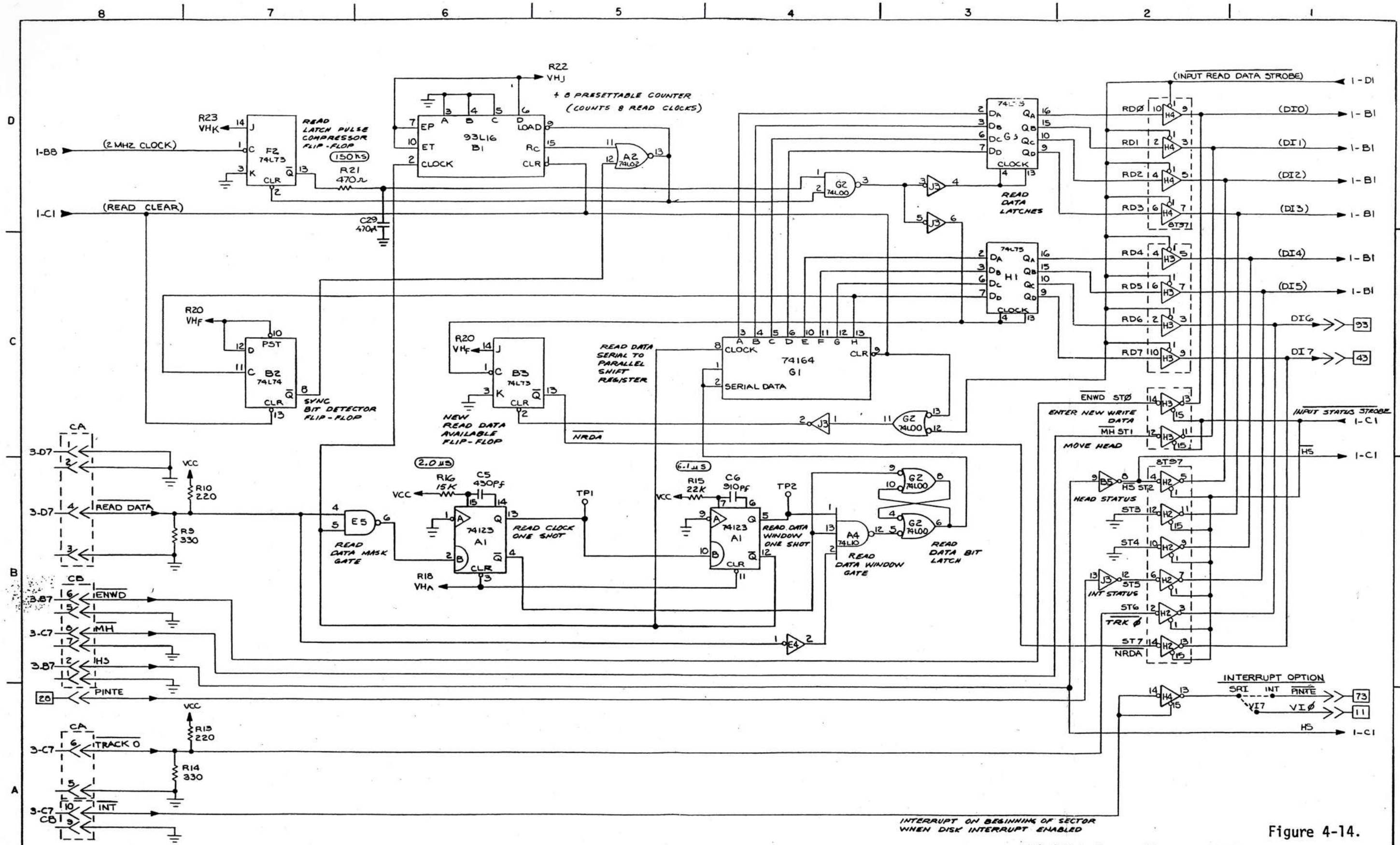
Figure 4-14.
Minidisk Controller Board #1   Sheet 2 of 3
Read Circuit and Status Output

POWER CONNECTIONS

IC	TYPE	VCC	GRD	SUBSTITUES
B5,E4,G5,J3	74L04	14	7	74LS04
E2,E5,G2	74L00	14	7	74LS00
B4	74L11	14	7	74LS11
A4,A5	74L10	14	7	74LS10
A3	74L20	14	7	74LS20
F5	74L30	14	7	74LS30
A2	74L02	14	7	74LS02
H2,H3,H4,H5,F6	8T97	16	8	74367
B3,E3,F2,F3,A1	74L73	4	11	74LS73
E1,F1,F4	74123	16	8	—
G4	7493	5	10	74LS93
B1	93L16	16	8	74LS161
B2	74L74	14	7	74LS74
G3,H1	74L75	5	12	74LS75
G1	74164	14	7	74LS164
K1	7805	2	3	—

NOTE:
1) ALL DIODES IN9M4 UNLESS SPECIFIED.
2) ALL RESISTORS IN OHMS, 1/2 WATT UNLESS OTHERWISE SPECIFIED.
3) ALL CAPACITORS ARE µF UNLESS NOTED.
4) (280µS) - NORMAL TIME CONSTANT.

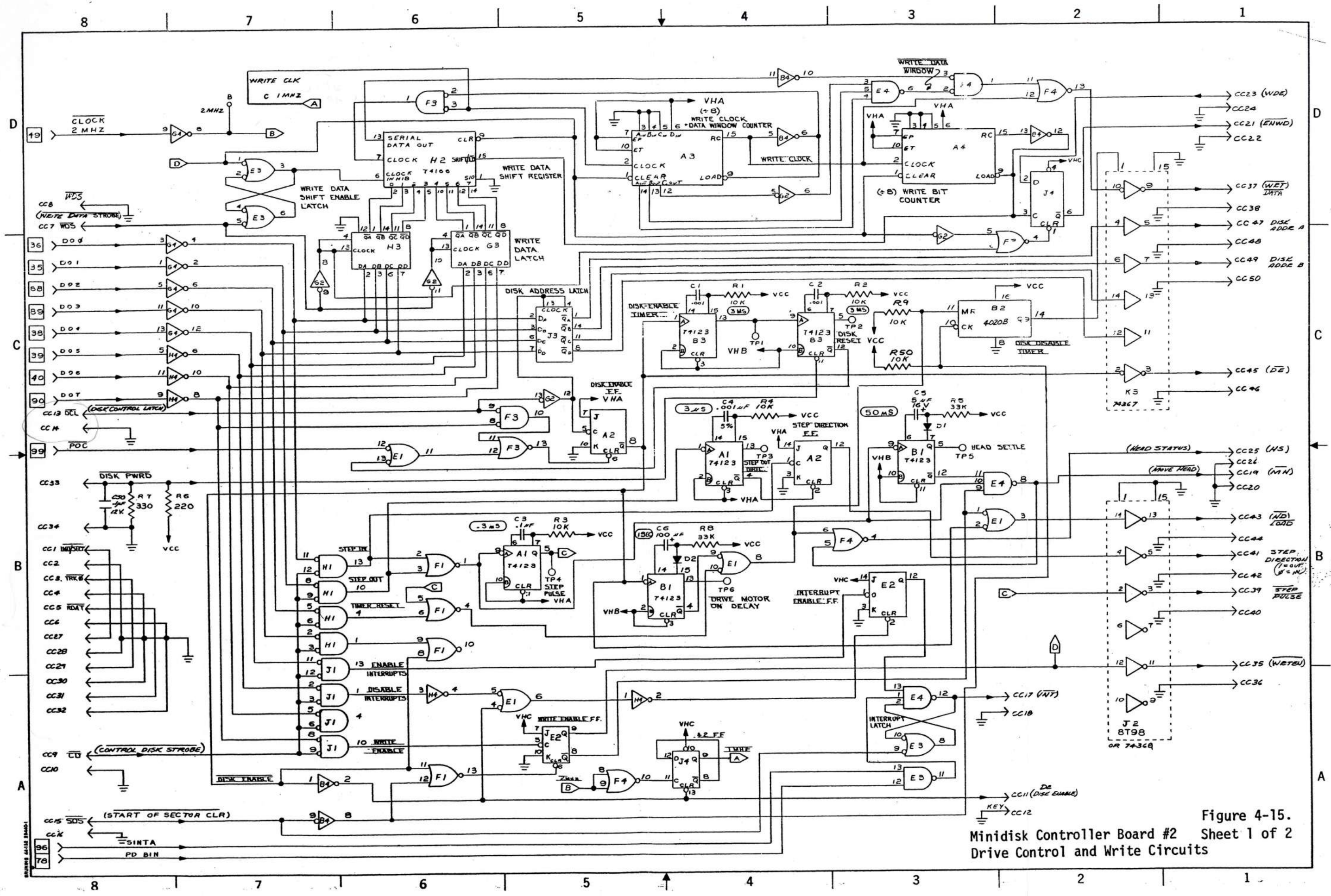Figure 4-14.
Minidisk Controller Board #1   Sheet 3 of 3

Figure 4-15.
Minidisk Controller Board #2   Sheet 1 of 2
Drive Control and Write Circuits

MINI-DISK CONTROLLER BOARD #2 INTERCONNECTIONS

POWER CONNECTIONS				
REF	TYPE	VCC	GRD	SUBSTITUTIONS
F,LF3,F4,HI,JI	74L02	14	7	74LS02
EI, E3	74L00	14	7	74LS00
B4,G2,G1,H4	74L04	14	7	74LS04
J2	8T98	16	8	74LS36B
E4	24L10	14	7	74LS10
H2	74166	16	8	74LS166
G3,H3,J3	74L75	5	12	74LS75
A3,A4	93L16	16	8	74LS161
J4	74L74	14	7	74LS74
A2,E2	74L73	4	11	74LS73
AI,BI,B3	74123	16	8	
K3	8T97	16	8	74367
LI	7805	2	3	
B2	4020B	16	8	

NOTES:
1) ALL RESISTORS 1/2 W UNLESS SPECIFIED
2) ALL CAPACITORS IN UF
3) ALL DIODES IN914
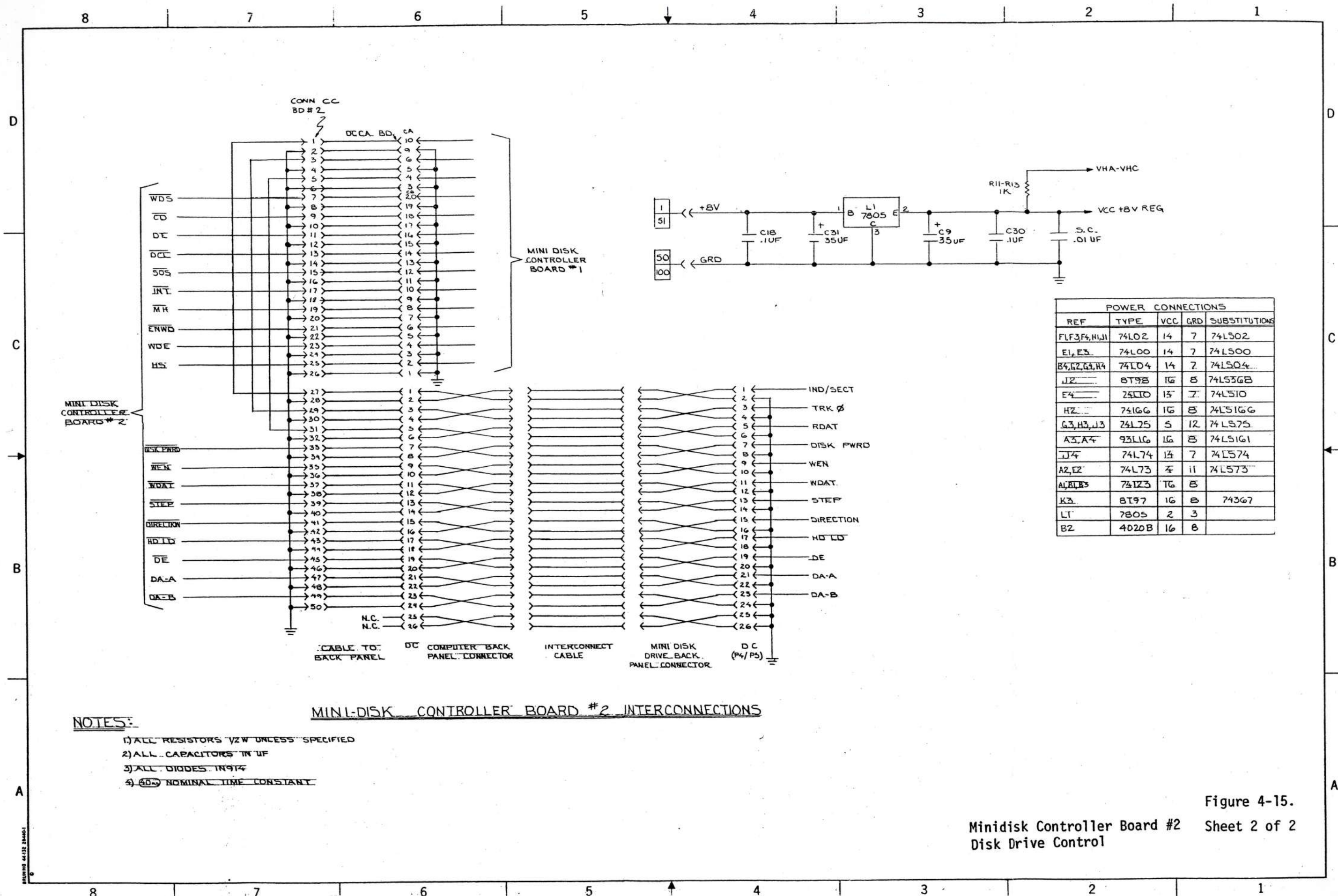4) 40ns NOMINAL TIME CONSTANT
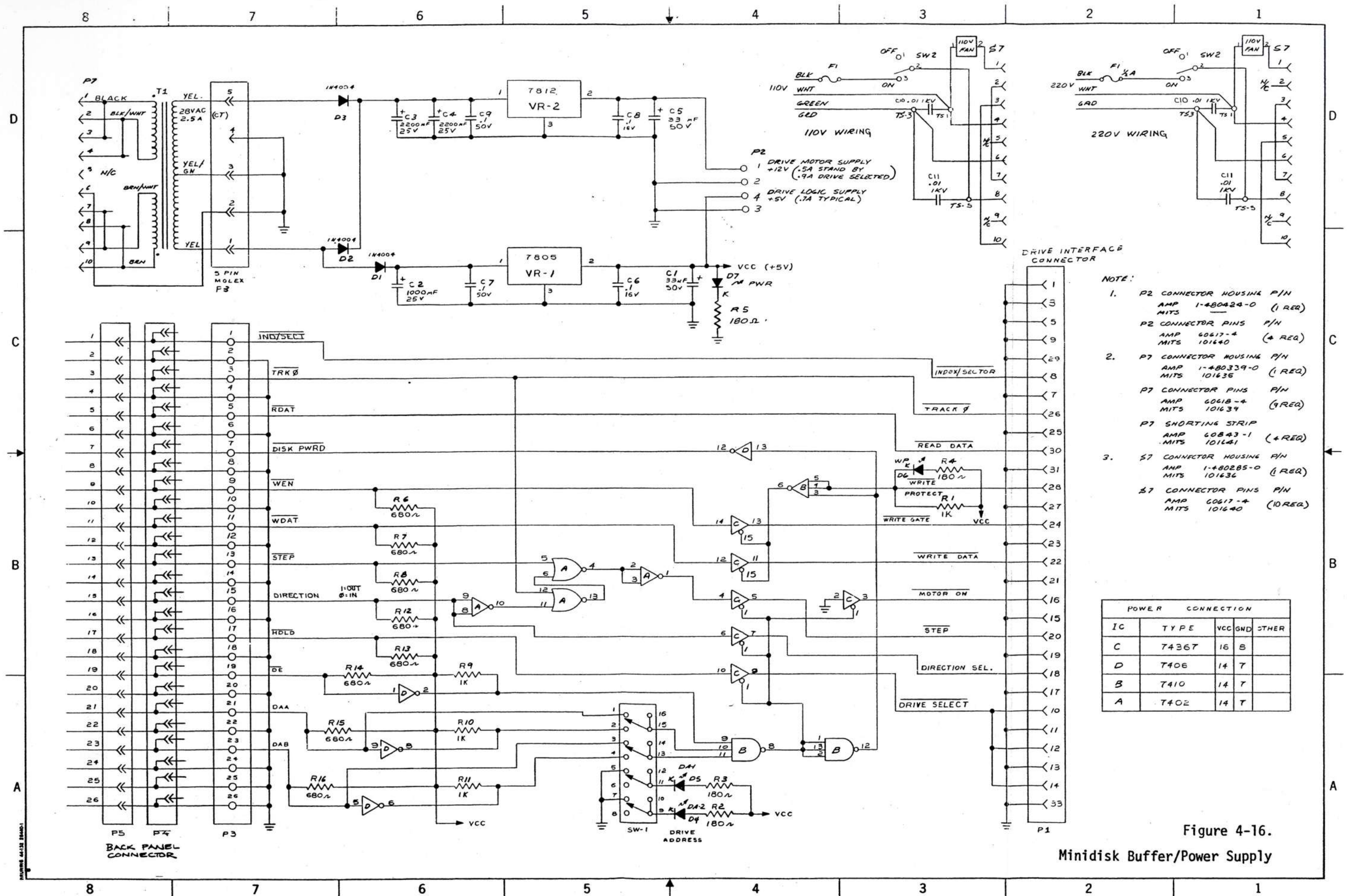
Figure 4-15.

Minidisk Controller Board #2   Sheet 2 of 2
Disk Drive Control

Figure 4-16.

Minidisk Buffer/Power Supply