8800b-sm & -dm
DOCUMENTATION

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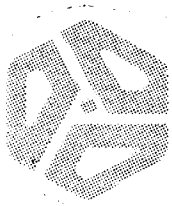

mits

a subsidiary of **Pertec Computer Corporation**
2450 Alamo S.E. /Albuquerque, New Mexico 87106

248067A

NOTICE

Marketing Headquarters

Pertec Computer Corporation
Microsystems Division
20630 Nordhoff Street
Chatsworth, CA 91311
Phone (213) 998-1800
TWX (910) 494-2788

International Marketing Headquarters

Pertec Computer Corporation
Business Systems Division
17112 Armstrong Avenue
Irvine, CA 92714, USA
Phone (714) 540-8340
TWX (910) 595-1912

CHANGE RECORD

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8800b-sm-& -dm
DOCUMENTATION
PART I
INTRODUCTION AND OPERATORS GUIDE

1. Introduction

1-1. Introduction to this Manual

The 8800b-sm and -dm are integrated computer systems that include the Altair 8800b Turnkey microcomputer along with either one (-sm) or two (dm) Altair Minidisk mass storage units.

The 8800b Turnkey computer includes the system power supply, the Central Processing Unit (CPU) with the 8080A microprocessor and a Turnkey Module board. The Turnkey Module is a multi-function board that includes 1K bytes of random access memory (RAM), provisions for up to 1K bytes of read only memory (PROM) (including the Minidisk Boot Loader PROM) and a serial input/output port (SIO) for connecting the computer to a terminal. Part II of this documentation package documents the 8800b Turnkey computer. Section 1 is a description of the components of the Turnkey computer, and Section 2 is a brief summary of its theory of operation. Section 3 is an advanced operation manual which details procedures for expanding and modifying the standard system. Section 4 is a brief guide to troubleshooting the electronics of the computer.

The Minidisk mass storage subsystem consists of one or two Minidiskk drives, a drive controller and an interface card for connecting the disk system to the computer. These are all described in Part III of this documentation package. Section 1 is a listing of the specifications of the Minidisk subsystem. Section 2 is a summary of the theory of operation and Section 3 is a description of procedures for initial checkout and fault diagnosis.

The Appendices include a description of the Altair bus, instructions for converting the power supply for use with 230 volts AC, a listing of the Minidisk Boot Loader PROM and aids for programming the Minidisk system in machine language.

Finally, the Intel 8080A Microcomputer System User's Manual details the structure, timing and instruction set of the 8080A microprocessor. It also gives technical information about some of the CPU's auxiliary circuits.

1-2. Introduction to the Standard System

The standard 8800b-sm or -dm system consists of the 8800b-sm or -dm computer and either a Teletype™ or Cathode Ray Tube (CRT) terminal. This section shows how to assemble such a system from its components and how to load and run BASIC on the assembled system.

A. Setting up the system. Carefully lift the computer unit from its packing case and place it on a hard, flat surface. Leave enough space on all sides so that the flow of cooling air is not impaired. Do not connect the power cord until the terminal has been installed.

Remove the protective tabs from the Minidisk drives following the directions printed on the tabs.

The computer is set at the factory to match the terminal shipped with it. Therefore, to install the terminal, it is only necessary to connect the computer and the terminal with the cable supplied with the terminal. The diagram below shows the 25 pin cable connectors and the matching connectors on the terminal and computer.

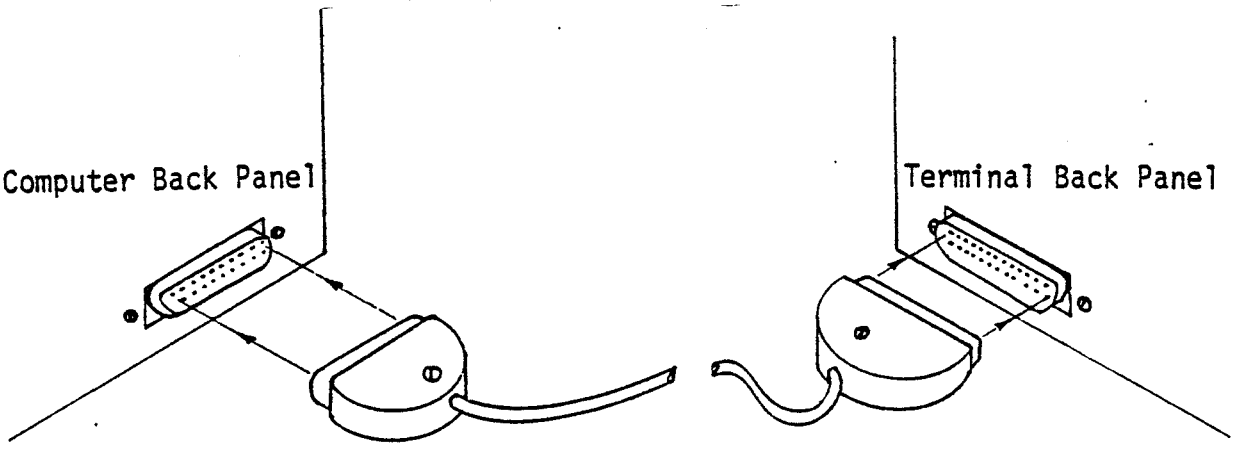


Figure 1-1. 25 Pin Cable Connectors

The power supply is protected by a 3 amp, slow-blow fuse mounted on the back panel of the computer. It should be replaced as necessary only by the same type of fuse. The power cord should be connected to a source of 115 volts, 50-60 Hz AC. (230 VAC operation is available as an option. See Appendix C).

After making sure the fuse is installed and the power cords for the terminal and computer are plugged in, insert the BASIC diskette into drive zero.

To do this, open disk drive zero by pulling out on the door tab (see Figure 1-2). Insert the edge of the diskette opposite the label into the drive with the label side toward the open tab. Push the diskette all the way into the drive and close the door tab.

Now, move the RUN/STOP switch on the front panel up to the RUN position and turn the power switch on. The power switch has three positions. At 12 o'clock, the unit is off and the key may be removed. At 3 o'clock, the power is on and the front panel switches are enabled. At 6 o'clock, the computer is on, but the front panel switches are disabled. In this position, the key may be removed.

With the power switch on, the Power indicator should light showing that the computer circuitry is receiving operating voltage from the power supply. If the Power indicator does not light, turn off the power switch and check the power cord and fuse.

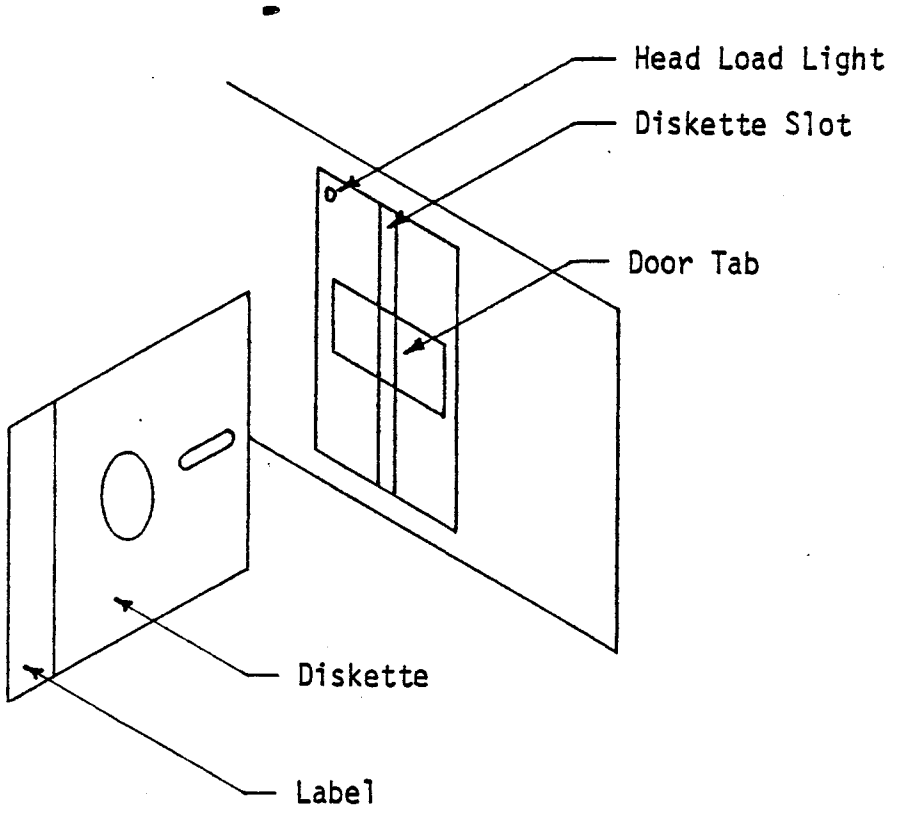


Figure 1-2 Inserting the Diskette

B. Initializing BASIC. When the power is turned on, BASIC is loaded into memory automatically. When it has been loaded, BASIC prints

MEMORY SIZE?

on the terminal to begin the initialization dialog. This question asks the operator to specify the amount of memory to be used by BASIC programs. Typing a number and carriage return reserves that number of bytes. Typing just a carriage return directs BASIC to use all available read/write memory. BASIC now prints

LINEPRINTER?

The operator types a letter and carriage return to indicate the type of printer in use as follows:

Letter		Printer
O	=	LP80
C	=	C700
Q	=	Q70

If no printer is connected, any of the letters may be typed. If the response is not O, C or Q, however, BASIC asks LINEPRINTER? again.

BASIC now asks

HIGHEST DISK NUMBER?

In a system with 1 disk, the highest number is 0. With 2 disks, the highest number is 1. Typing just a carriage return is equivalent to typing 0.

Now BASIC asks the number of disk data files (random access and sequential) to be open at one time:

HOW MANY DISK FILES?

The operator responds with the number of disk data files expected to be open at any one time. BASIC then prints

HOW MANY RANDOM FILES?

Here again, the operator responds with the number of random access files expected to be open at any one time.

Now BASIC is initialized and prints the following messages:

ALTAIR MINI-DISK BASIC
REVISION 4.1 JULY 1977
COPYRIGHT 1977 BY MITS, INC.

OK

BASIC is now ready for use.

At any time, BASIC may be reloaded simply by momentarily depressing the START switch.

C. Initializing New Diskettes. Because the BASIC code takes up so much diskette space, it is supplied on a "write protected" diskette. This means that no programs or data may be saved on the BASIC diskette.

In addition to BASIC, the BASIC diskette includes two programs, PIP and STARTREK, which are available to users. Before they can be run, the BASIC diskette must be mounted (see section D below). Since the BASIC diskette is write protected, mounting it causes a DISK I/O ERROR, but the reading process is not affected.

The desired program may now be read from the disk and loaded into memory. To do this, type the following command:

LOAD "<program name>",<disk number>

where <program name> is the name of the desired program and <disk number> is the number of the disk drive into which the BASIC disk was inserted (usually zero).

To avoid inadvertant damage to the BASIC disk, type the following command:

UNLOAD<disk number>

where<disk number>is the drive number that appeared in the LOAD command above.

Now the BASIC diskette may be removed and another diskette inserted into the drive and mounted.

The program may be saved on the new diskette by typing the following command:

SAVE "<program name>",<disk number>

where <disk number>is the number of the disk drive into which the new diskette was inserted.

Subsequent to saving the program, it may be run by typing the following command:

RUN "<program name>",<disk number>

where <disk number>is the number of the disk drive into which the diskette bearing the program was inserted.

CAUTION

Do not attempt to write programs or data onto the BASIC diskette. This can result in FILE LINK ERRORS that can make the BASIC diskette unusable. Before writing anything on disk, unload and remove the BASIC diskette.

If the diskette has never been used it must be initialized before it can be used. This is done by typing the following command:

DSKINI <disk number>

where disk number is the number of the disk drive on which the blank diskette is loaded. The DSKINI command marks all the sectors on the diskette as being empty. BASIC reads these marks to determine sector boundaries.

CAUTION

Only new, blank diskettes need to be initialized. Using DSKINI on a diskette that contains files destroys all the files. DISKINI should, therefore, be used with extreme caution. The DSKINI process takes about 2 minutes per diskette. When it is finished, BASIC prints OK.

D. Mounting Diskettes. To ready a diskette for reading or writing, type the following command:

MOUNT <disk number>

Omitting the disk number causes all disks in the system to be mounted. After a few seconds, BASIC prints

OK

to indicate that the disk is ready for use.

Before removing a mounted disk from a drive, type the following command

UNLOAD <disk number>

Omitting the disk number unloads all mounted disks.

E. Diskette Specifications and Care. The 8800T sm and dm use 5 1/4", hard-sectored diskettes. Diskettes are available from MITS (Part number 102501) or may be purchased from any Altair Computer Center.

The notch on the side of the diskette engages a switch in the drive which enables the write circuitry. Covering the notch with a piece of tape makes writing on the diskette impossible. The BASIC diskette is protected in this manner.

> CAUTION
>
> Unprotecting the BASIC diskette can cause destruction of the BASIC interpreter. DO NOT remove the BASIC diskette protection tab.

Several handling precautions will maximize the life and usefulness of diskettes and drives.

1. Return diskettes to their storage envelopes when they are not in use. Do not leave them in the drive.
2. Keep diskettes away from magnetic fields. Fields may be caused by fluorescent lights, transformers or large pieces of magnetizable materials.
3. Mark the diskette label only with felt tip pen. Do not use ball point pen or pencil.
4. Keep dust and other particulate matter away from diskettes.
5. Keep diskettes away from excessive sunlight and heat.
6. Never touch the diskette surface (through the head access window) or attempt to clean it.

F. Miscellaneous Information. Since the address of the Mini-Disk controller is the same as the standard size floppy disk controller (88-DCDD) the standard size disk drives may not be used in the 8800T-sm or-dm system.

A timing circuit in the Mini Disk Controller turns off the drive motor 6.4 seconds after the last access operation to minimize drive wear.

1-3. Using this Documentation Package

The remainder of the documentation in this package contains reference material for operating and maintaining the components of the system.

Three commonly encountered situations which require the use of this reference material are 1) expansion of the system memory, 2) adding or modifying input/output peripheral equipment and 3) adding special purpose PROM functions. The procedures for making these modifications are sketched below along with references to more detailed information. The references are either to the manuals or to the page numbers in this documentation package in which the information may be found.

> NOTE
>
> Before working on the inside of the computer case make sure the power is off and the power cord disconnected from the line.
>
> To remove the case cover, remove the two bolts in the upper corners of the back panel. Then slide the cover back and lift it off.
>
> To remove a card, pull straight up on both ends of the card. Carefully remove any cable connectors when the board is free.
>
> To insert a card, connect the necessary cables and position the board so the edge connector is down and the component side of the board is to the right as viewed from the front of the unit. Insert the card into the card guides and slide it straight down until it makes contact with the connector at the bottom of the slot. Apply firm, steady pressure to the upper edge of the card until the board seats in the connector. The top edge should be flush with the top of the card guides.

A. Expanding Memory. System memory expansion is accomplished by adding memory boards or replacing them with boards of higher capacity. Use the following procedure to make these changes:

1) Set the addresses of the new boards (memory board manual).
2) Insert the boards in the chassis (p.10).
3) Change the address of the RAM block on the Turnkey Module board, if necessary to avoid conflicts with the new memory addresses (p. 40).

B. Modification of Input/Output Arrangements. Input and output arrangements can be changed either by adding new peripheral devices (terminals, mass storage, printers, etc.) along with their associated interface boards or by changing the device connected to the Turnkey Module SIO port.

1) If a new interface board is being installed, set the port address, data transfer rate (or baud rate) and signal type (interface board manual).
2) Install all necessary cables and insert the board in the chassis (interface board manual and p. 10).
3) If the SIO port is to be connected to a different device or otherwise changed, set the desired address, data transfer rate and signal type (p. 42ff).
4) If the new device is to be the console terminal for BASIC or DOS, set the sense switch on the Turnkey module board to conform to the device (p. 41 and BASIC or DOS manual).

C. Adding Special PROM Functions. The Turnkey Module has sockets for up to four 256 byte PROM chips. These PROMs can be used to store any programs or data that must be permanently retained. Several pre-programmed PROMs are available for the 8800 series microcomputers including a Turnkey PROM Monitor and a multi-purpose bootstrap loader for loading programs from paper tape and cassette. In addition, user-written programs can be retained in PROM for use in dedicated applications. To install these PROM functions, use the following procedure:

1) Set the address of the Turnkey Module PROM block to the first location of the 1K byte block that includes the address of the new PROM (p. 40, PROM documentation).

2) Insert the new PROM in the proper socket on the Turnkey Module board. The first address of the first PROM socket is the address set in step 1. The first address of the second socket is the board address plus 256 and so on (p.40).

3) Set the starting address of the new program in the AUTO-START switches, if the program is to be executed automatically when the power is turned on or when the START switch is actuated. Note that the Turnkey Module is supplied with the Mini Disk Boot Loader PROM at the AUTO-START address to automatically load BASIC or DOS. Changing the PROM or AUTO-START addresses will disable this feature (p. 54).

NOTE

A Turnkey PROM Monitor is a good investment for an expanded system. The Monitor allows examination and modification of any memory location from the terminal. It lets the operator dump the contents of any range of memory locations and transfer control of the computer's execution to any address. Putting the Monitor at the AUTO-START address allows the Monitor to be entered at any time, simply by actuating the START switch. This provides a useful reset function for BASIC programs. If a programs hangs in an infinite loop or an impossible I/O function, reentering the Monitor with the START switch and jumping to location zero causes BASIC to print OK and await further instructions.

8800b-sm & -dm
DOCUMENTATION
PART II
8800b TURNKEY COMPUTER

SECTION 1
INTRODUCTION

1. INTRODUCTION

The Altair 8800b Turnkey computer is housed in a standard Altair system case and contains the following elements:

-Power supply and motherboard assembly
-CPU board with the 8080A microprocessor
-Turnkey Module with memory and I/O circuitry
-Front panel board

The heart of the computer is the Central Processing Unit (CPU) board (Figure 1-2) which holds the 8080A microprocessor and its associated circuitry. The 8080A performs all the logical and arithmetic computations for the system. It also supplies control and status signals for the other system components. Other circuitry on the CPU board provides clock signals and synchronization functions.

The Turnkey module (Figure 1-3) is a general support board for the Turnkey system which includes memory, I/O and AUTO-START control. The memory section has 1K bytes of random access memory (RAM) and positions for up to 1K bytes of read-only memory (ROM). Random access memory stores information that can be read, written or changed at will. RAM is volatile, however, and information is lost when power is interrupted. Programmable Read-only memory (PROM) is non-volatile. Information in PROM is always present whether the power is on or not. Thus, PROM can store programs and data which must be permanently retained. The computer cannot write information into PROM, however. A special PROM programmer must be used to do this, although factory-programmed PROMs are available for some widely used functions.

The serial Input/Output channel (SIO) connects the parallel data bus in the computer to serial input/output devices, such as Teletypes, CRT terminals, modems, etc. The SIO may be configured to accommodate a variety of terminal types and speeds to match virtually any serial I/O arrangement.

The AUTO-START feature is the key to the Altair 8800b Turnkey computer's ease of operation. When the computer's power is turned on or the START switch is actuated, the AUTO-START logic forces the computer to execute the instruction at a pre-selected address in PROM. The address could be the beginning of a series of instructions to load a program from an I/O device, the start of a monitor program or a dedicated application program.

Front Panel switches (Figure 1-4) include the power switch, which provides system security as well as turning the power on or off, and switches that start and stop execution of programs. Indicators on the Front Panel monitor the computer system's operation.

Power, data, addresses, status and control signals and miscellaneous pulses are carried by the system bus on the motherboard. The bus is fully parallel, meaning that all signals are available to all boards plugged into the motherboard's sockets. This allows for easy and quick system expansion. The motherboard can accommodate the CPU and Turnkey Module boards plus up to 16 additional boards.

The Power Supply provides all the power voltages required by the Altair 8800b Turnkey system components. The supply has enough capacity to allow expansion of the sytem by addition of as many I/O and memory boards as will fit in the system case.

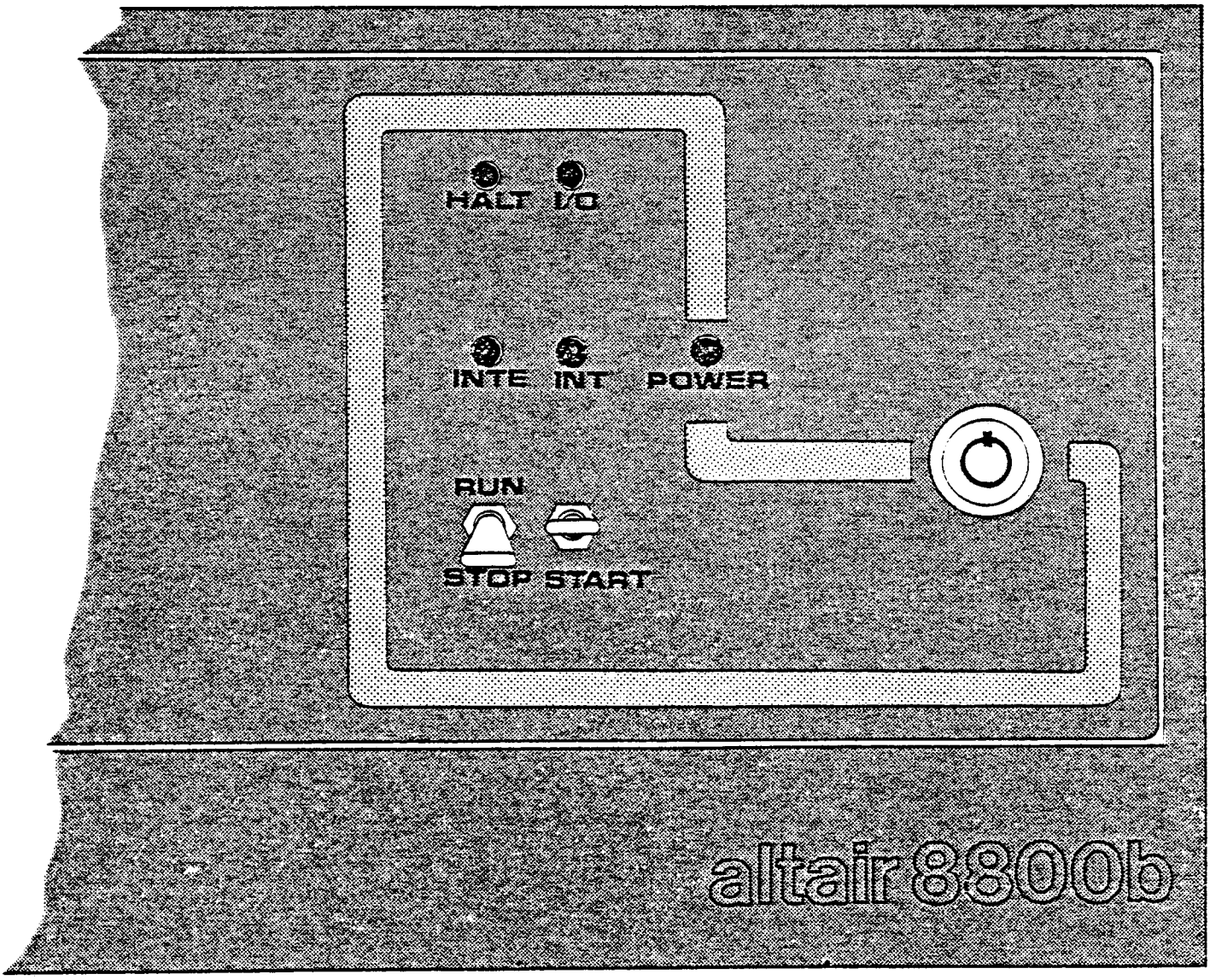


Figure 1-4
Front Panel Switches and Indicators

SECTION 2
THEORY OF OPERATION

2. THEORY OF OPERATION

2-1. General

A generalized block diagram of a computer system is shown in Figure 2-1. The Control, Processor, Memory and I/O are arranged so that instructions in Memory cause the Control to direct the Processor to access and manipulate Memory data. The Control also directs the Processor to arrange for Input and Output of data.

The system in the diagram is stored-program computer. Its actions are directed by instructions that are stored in memory. The computer has the ability to change the order in which its instruction are executed and to modify the instructions themselves. This accounts, in part, for the great flexibility of stored program computers.

As the diagram shows, the Control and Processor elements are the heart of the system. All the other elements of the system communicate with and are controlled by the Control and Processor. In many computers, including the Altair 8800b Turnkey computer, the Control and Processor elements are combined in one unit, the Central Processing Unit. Moreover, in the Turnkey system, some of the memory and I/O functions are combined into the Turnkey Module.

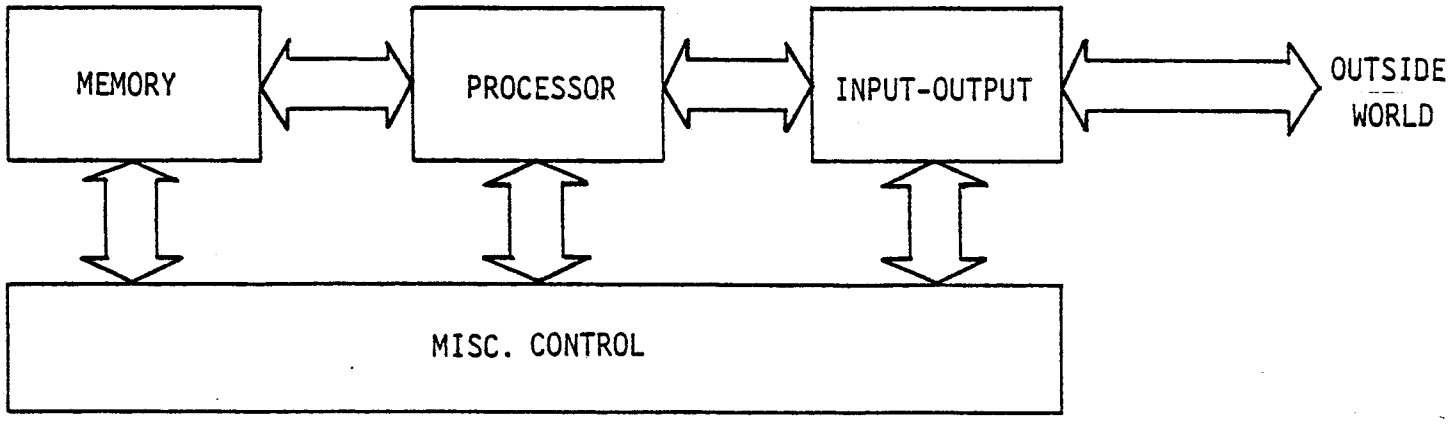


Figure 2-1
Typical Computer System
Block Diagram

Figure 2-2 is a diagram of the Altair 8800b Turnkey computer system showing how the functional parts are distributed among the physical units of the system.

One important feature of the Turnkey system's design is that it is based upon a bus. The Altair bus is a collection of conducting paths (lines) which distribute signals to all of the system's components. The pins of each board are connected directly to the corresponding pins of every other board. As a result, the system is easily expandable, since every board has access to all of the data, addresses, status and control information in the system.

The bus is located physically on a 100 conductor printed circuit motherboard. The printed circuit card edge connectors on the motherboard provide mechanical support for the system's circuit boards, as well as electrical connection to the bus.

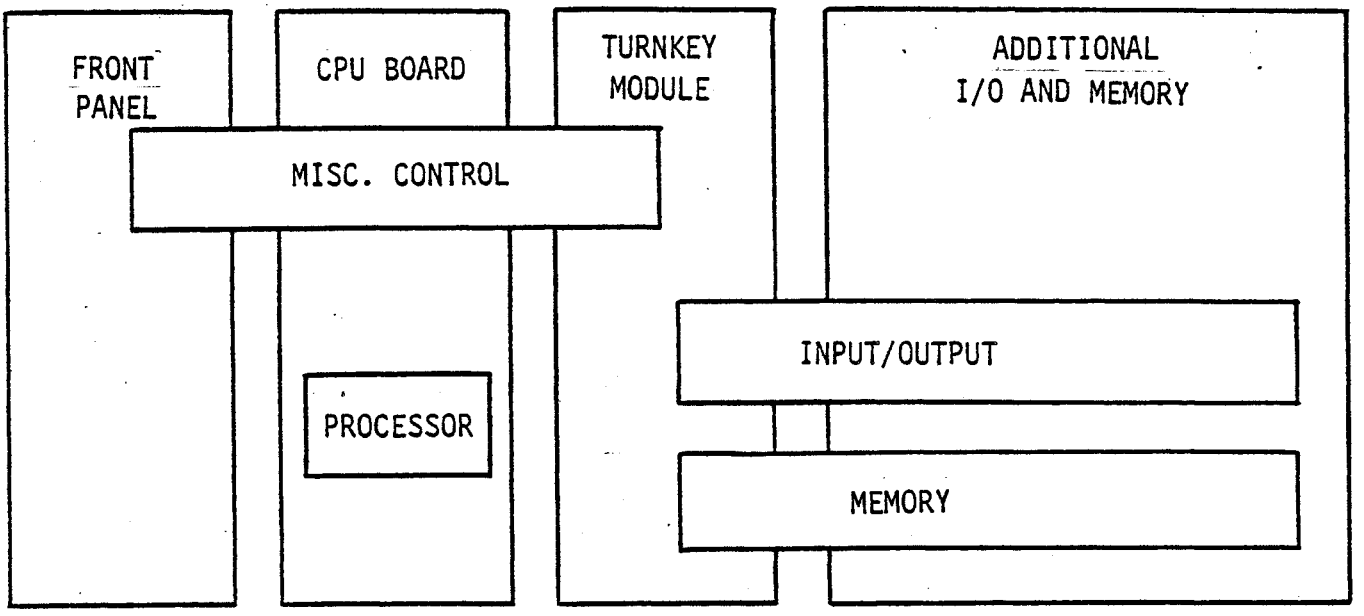


Figure 2-2
Altair 8800b Turnkey System
Function Distribution

The bus has 16 Address lines, 8 Data-In lines carrying data to the CPU, 8 Data-Out lines carrying data from the CPU and lines carrying pulses that indicate the status of the system and serve various control functions. A list of the conductors on the Altair system bus is in the Appendix.

The activity on the bus corresponds to six machine cycles; Memory Read and Write, I/O In and Out, Interrupt and Halt. The functions of the various bus lines depend on what cycle is currently in progress.

In a Memory cycle, the address of the memory location to be read or written is carried on the address bus. The Data-In bus carries data or instruction codes from memory to the CPU during a Memory Read. The Data-Out bus carries data from the CPU during a Memory Write. In an I/O cycle, the Address bus carries the address of the I/O port through which the data transfer is to take place. The port address is only eight bits long, so it is carried both in the high and low order bytes of the 16 bit Address bus. The Data-In bus carries information from the port to the CPU during an Input cycle. Similarly, the Data out bus carries information from the CPU to the port in an Output cycle.

The Interrupt cycle is provided so that peripheral devices can gain access to the bus. In the absence of interrupts, the CPU can be programmed to check its peripheral devices periodically and service them as they have information to transfer. An input device, for example, waits until the CPU signals that it is ready for input. This arrangement is simple, but it is often inefficient, since the CPU is required to poll the I/O devices whether or not there is information to be transferred.

In an interrupt driven system, on the other hand, the I/O device signals the CPU when it is ready to transfer data. This signal is called an Interrupt Request. If the CPU Interrupt Enable bit is set to 1, the CPU acknowledges the Interrupt Request. Otherwise, the request is ignored. In an Interrupt cycle, the CPU fetches an instruction which causes the computer to interrupt the execution of its current program and begin executing another program (called an interrupt service routine) at a special location in memory. The computer also stores the location of its current instruction so that it can return to the place where it left off when the interrupt service routine is completed. The interrupt scheme allows the computer to work on a program until a peripheral device has information to transfer. The CPU can then accept the information and take the necessary action without losing track of the program in progress.

A special machine cycle is provided for direct memory access. During the Hold state, the CPU is effectively disconnected from the bus. This allows a direct memory access device, if it is used, to take control of the bus and transfer information directly to and from memory. For more information on machine cycles, see the Intel 8080 machine cycles, see the Intel 8080 Microcomputer System User's Manual (abbreviated IMSUM), section 2, pp 3-11.

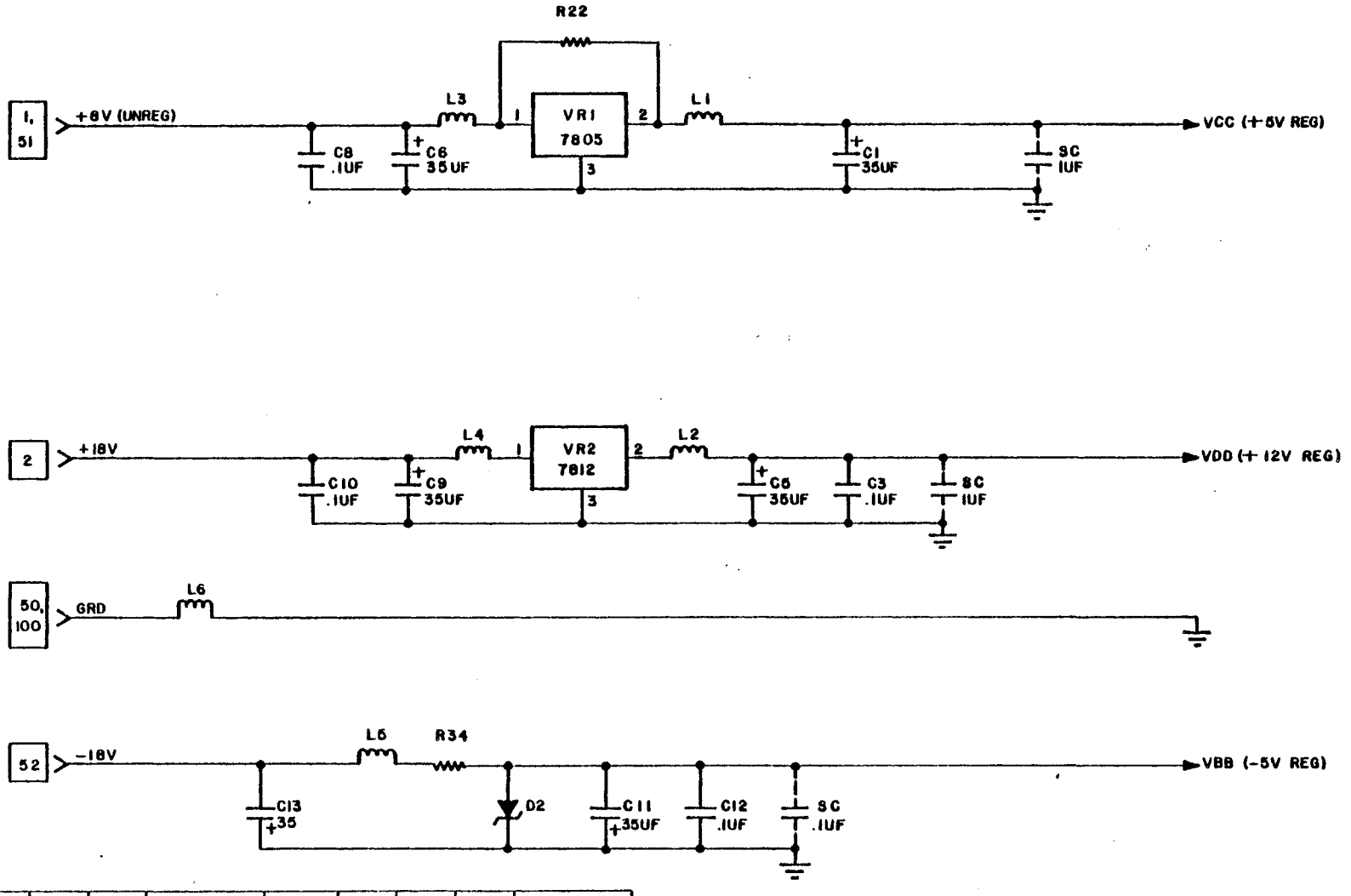
2-2. The CPU Board

NOTE

In the following descriptions, the names of signals appear in capital letters. Signal names which are barred ($\overline{\text{PRESET}}$, for example) are active LOW. That is, they are LOW (Ø volts) when activated and HIGH (+5 volts) otherwise. All other signals are active HIGH.

The address and data lines represent binary 1 as HIGH and binary Ø as LOW.

On the Turnkey module, the sense switches and the address switches for RAM, PROM and AUTO-START allow manual entry of data and addresses. The two states of each switch -on and off- correspond to the two states of a binary digit - 1 and 0. The bits represented by the sets of switches can, therefore, be treated by the computer in the same way as any other data or address bits. Moving a switch in the direction of the arrow next to each set of switches puts the switch in the 1 position.



REF DESIG	TYPE	VCC	GRD	OTHER	REF DESIG	TYPE	VCC	GRD	OTHER
					M	8080A	20	2	
G, B	74LS04	14	7		J, X, R, V, N, U, P	74368 OR 8T98	16	8	
C	74LS13 OR 74LS20	14	7		K	8212	24	12	
S, Y	74LS14	14	7		D, E	8216	16	8	
					F	8224	16	8	VDD = 9
P, W	74367	16	8		A	4009	1	8	VDD = 16

Figure 2-3b.
CPU Board Power Regulators

The CPU board contains the 8080A microprocessor, its timing and auxiliary control circuits. It also contains buffers and line drivers for the system bus. The heart of the CPU (and the whole computer system) is the 8080A microprocessor. All of the other circuitry on the board serves to support the microprocessor and connect it to the rest of the system.

A. The Microprocessor. The 8Ø8ØA is IC M on the schematic, Figure 2-3a. For a complete description of the internal organization and timing of the 8080A, see the IMSUM, Chapter 2.

B. Clock and Synchronization. The 8224 clock generator (IC F on the schematic) provides the two-phase, 2 MHz clock for the 8Ø8ØA at the required Ø and 12 volt levels. The master timing reference for the 8224 is an external 18 MHz crystal. The system timing frequency can be changed by replacing the crystal.

The clock generator also synchronizes the 8Ø8ØA's READY and RESET inputs and provides a status strobe signal ($\overline{\text{STSTB}}$) that is used to load the 8212 status latch. The READY signal is the logical product (AND) of bus signals XRDY, PRDY, XRDY2 and FRDY. Normally, only PRDY is used for memory synchronization; the others are set to logical 1 by pullup resistors. The bus signal $\overline{\text{PRESET}}$ is filtered, lengthened, shaped and synchronized by the 8224 to generate the RESET input for the 8Ø8ØA. The $\overline{\text{STSTB}}$ signal is generated as soon as the status information is available on the 8Ø8ØA data lines.

C. The Status Latch. At the beginning of each bus cycle, status information is presented momentarily on the 8Ø8ØA data lines. This information is stored in the 8212 latch so that the data lines may be used for other information later. The 8212 is IC K on the schematic. For a complete description of the status information and its timing, see page 2-6 of IMSUM. The 8212 is described on page 5-101 of the same manual.

D. Buffers.

1) Bus splitters. Information is communicated to and from the 8Ø8ØA through an eight-bit, bidirectional data bus. This bus is buffered by two 8216 bidirectional bus drivers to form a TTL compatible, bidirectional bus on the CPU board. The direction of the 8216's is controlled by PDBIN.

At the other end of the CPU bus are tri-state buffers that split the bidirectional data bus into Data-In and Data-Out busses which are brought out to the system bus. The buffers shown in zones B-3 and B-4 transfer data from the system Data-In bus to the bidirectional bus when both PDBIN and DIGI are HIGH. (DIGI is normally HIGH unless the bidirectional bus is being accessed through connector P3. When either PDBIN or DIGI are LOW, the buffers are put in a high impedance state and no information is transferred through them. Similarly, the buffers in zones C-2 and C-3 transfer data from the CPU bus to the Data-Out system bus when the signal $\overline{\text{DO DSBL}}$ is HIGH.

If no information is present on the Data-In bus, all eight lines are pulled HIGH by resistors on the CPU board. When a interrupt is acknowledged, this forces a RST 7 instruction onto the bus if the Vector Interrupt Board is not used.

2) Input buffers. All input lines to the CPU board are buffered by TTL circuitry. Unused lines are pulled HIGH by resistors which also allow any one of several boards to pull any input line LOW. A line is normally pulled LOW either by an open collector driver or a tri-state driver, with the condition that no more than one tri-state driver may be enabled at one time.

Examples of these input lines are $\overline{\text{PINT}}$ and PHOLD in zone D-8, the READY lines (PRDY, etc.) in zone A-7, PRESET in zone A-6, and the driver disable lines throughout the schematic.

3) Output buffers. All outputs from the CPU board are buffered to drive 30 standard TTL loads. The lines are collected into four groups, Address lines, Data Out lines, Status lines and a Control group made up of PWR, PDBIN, PWAIT, PSYNC, PHLDA and PINTE. Each group of lines may be disabled as a group by signals from the bus.

2-3. The Turnkey Module

The Turnkey Module contains 1024 bytes each of RAM and PROM, a serial I/O channel, AUTO-START logic, sense switch, the front panel board and logic and miscellaneous logic. The Turnkey Module schematic is shown in Figures 2-4 a, b and c.

A. RAM and PROM. The RAM and PROM memories and their control logic are shown in the schematic diagrams, Figures 2-4 a and c.

1) The incoming PROM address is compared with the starting PROM address by the NAND gate IC D. If the incoming address is in the 1K block selected for PROM, the output of IC D, active LOW, enables the PROM address decoder, IC Za, which selects one of the PROM ICs. Up to four PROM chips may be installed. The output of IC D is also combined with the output of the I/O address detector in a NOR gate, the output of which causes the CPU to execute a WAIT state and enables the data bus interface, IC's P and R. The selected PROM drives the bidirectional data bus and the interfaces P and R put the selected data on the Data-In system bus.

2) An address of a byte in RAM is detected by IC B. The output of IC B is active if a start sequence is not in progress and the current machine cycle is not an I/O cycle or an interrupt. Therefore, the only time a RAM address is detected is when the machine cycle is a memory cycle or a Halt cycle. The output of IC B enables the RAM ICs and the data bus interfaces P and R. The direction of the data bus is controlled by the MWRT pulse described in paragraph 2-3F. When RAM is selected, data at the address is put on the bidirectional bus. If the cycle is a memory read, the cycle is complete. If it is a write cycle, the direction of the data bus interfaces is momentarily reversed, overdriving the RAM output drivers. Pulsing the RAM write inputs then causes the data on the bus to be written in the addressed location.

B. AUTO-START. The AUTO-START logic causes the computer to jump to the address designated by the AUTO-START switches when the power is turned on or the START switch is actuated. Figure 2-5 shows the arrangement of the AUTO-START logic. The switches represent the variable byte in a JMP instruction. The JMP instruction is generated by a multiplexer, ICs M and N, which is controlled by flip-flops Ta, Sa and Sb. The flip-flops are cleared by PRESET, a bus signal derived from POC or generated by the START switch on the front panel. Subsequent PDBIN pulses cause the flip-flops to change from one state to the next as shown in the sequence diagram, Figure 2-6. The pulses generated by the flip-flops cause the multiplexer to choose one of three possible bytes; 3Ø3 octal, ØØØ octal or byte designated by the AUTO-START switches.

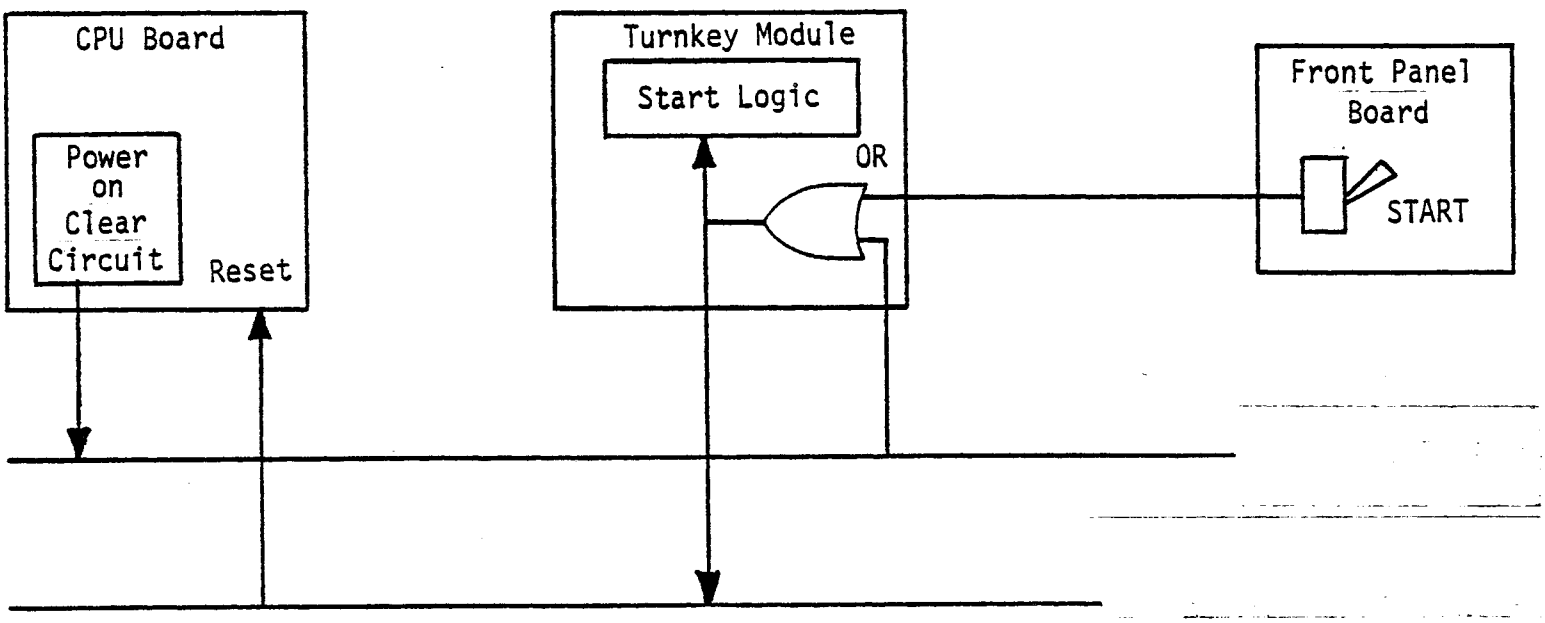


Figure 2-5
AUTO-START Block Diagram

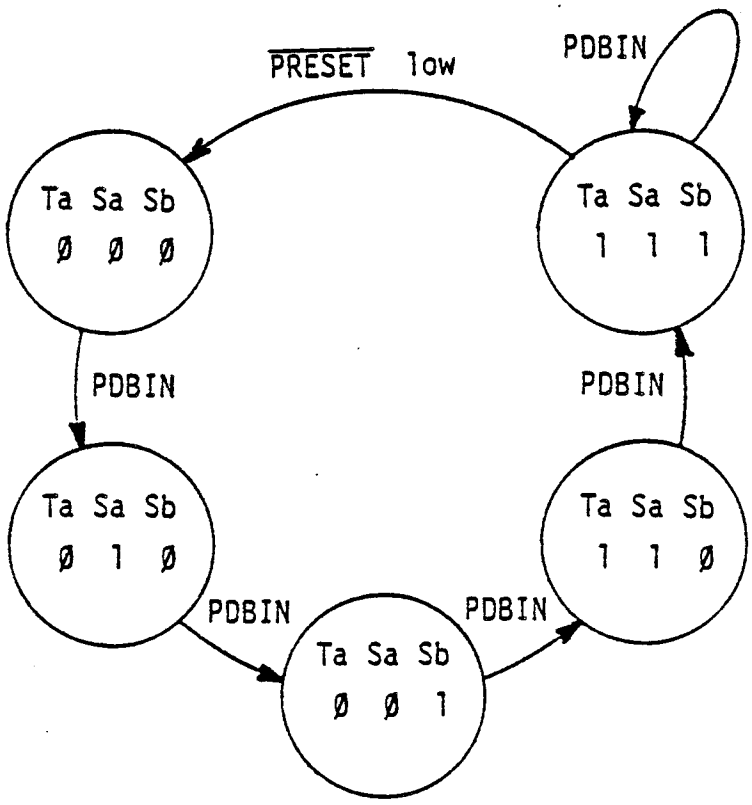


Figure 2-6
AUTO-START Logic
Control State Diagram

These bytes are placed on the bidirectional data bus in sequence and become the AUTO-START JMP instruction. Table 2-A shows the sequence of events in the AUTO-START procedure.

Table 2-A

Signal In	Control State	Function
PRESET	000	Mux. outputs enabled, Bus interface enabled, 303 octal put on bus.
PDBIN	010	000 put on bus.
PDBIN	001	Byte in address switches put on the bus.
PDBIN	110	First byte of PROM program
PDBIN	111	Next byte of PROM program
.	.	.
.	.	.
.	.	.

During the three bytes of the JUMP instruction, the HIGH Q output of flip-flop Ta is used to drive transistor Q2 to hold MEMR low and keep memory data off the bus. Once the JUMP instruction is complete, Q goes LOW and memory instructions can be fetched.

C. Sense Switches. The sense switch circuitry is shown in Figure 2-4 a and b. IC K (Figure 2-4a) detects I/O port address 255 decimal (377 octal), which is reserved for the sense switches. The output, active LOW, enables the tri-state buffers connected to the sense switches (Figure 2-4b) putting the bits represented by the switch positions on the bidirectional bus. IC K also enables the bus interface, so the sense switch bits are placed on the Data-In system bus.

D. Serial I/O Channel (SIO). The SIO schematic is shown in Figure 2-4b. The heart of the SIO is the 6850 Asychronous Communications Interface Adapter. The ACIA contains all the Status and Control registers discussed in section 3-2 and most of the timing and control circuitry. The bit rate is generated by a 34702 integrated circuit whose timing

reference is a 2.4576 MHz crystal. Jumpers are provided to set the output rate of the 34702 at 1, 16 or 64 times the required bit rate.

Input signals are received by RS232 receivers that may be made compatible with TTL or current loop signals by means of jumper-selected pullup resistors. TTL or RS232 outputs may be selected by jumpers or by internal cable wiring.

E. Front Panel. The front panel logic is contained on the Turnkey Module board. The indicators and switches are connected to the Turnkey Module by a cable and Molex connectors. The schematic diagram for the front panel circuitry is in Figure 2-4a.

The bus signals PHLTA, PINTE and $\overline{\text{PINT}}$ are buffered to drive the indicators HALT, INTE and INT, respectively. The I/O indicator is driven by the logical sum (OR) of the INP and OUT signals. The POWER indicator monitors the +5 volt supply on the Turnkey Module.

The bus signal PRDY is grounded when the RUN/STOP switch is in the STOP position. PRESET is grounded momentarily by the START switch which, in turn, initiates the AUTO-START sequence. Contact bounce is filtered out on the CPU board to generate a reset signal suitable for the CPU.

F. Miscellaneous Signals. Several miscellaneous signals are handled by the rest of the circuitry on the Turnkey Module. Some are optional and may be selected by jumpers.

1. MWRT is generated if the jumper from M1 to M2 is installed. In the full front panel version, MWRT is generated by the front panel logic and is used by memory boards of write functions.
2. PROT and UNPROT are used on the standard model of the Altair 8800b for memory protect and unprotect functions. As supplied, the Turnkey Module grounds PROT and pulses UNPROT with phase 2 of the clock to unprotect all memory as it is accessed. This feature may be disabled by removing the jumpers from 2 to UM and from G to PM.

3. AUX CLR is normally pulled HIGH by a resistor on the Turnkey Modlue, but insertion of optional jumpers as described in section 3-4b allows the signal to be used.

G. Power. All power used on the Turnkey Module and Front Panel boards comes from the +18 volt, -18 volt and +8 volt lines on the motherboard. The Turnkey Module's power regulator circuitry is shown in Figure 2-4a. The +5 volt supply is derived from the +8 volt line by an IC regulator. The +9 volt supply comes from the +18 volt line through a zener regulator and the -0 volt supply is derived by a transistor-zener regulator from the -18 volt line.

Figure 2-7 is the schematic for the power circuits in the 88ØØb case. The +18 and -18 volt supplies are pre-regulated. The +8 volt supply is not regulated, but it is adjusted by the taps on the secondary of the power transformer.

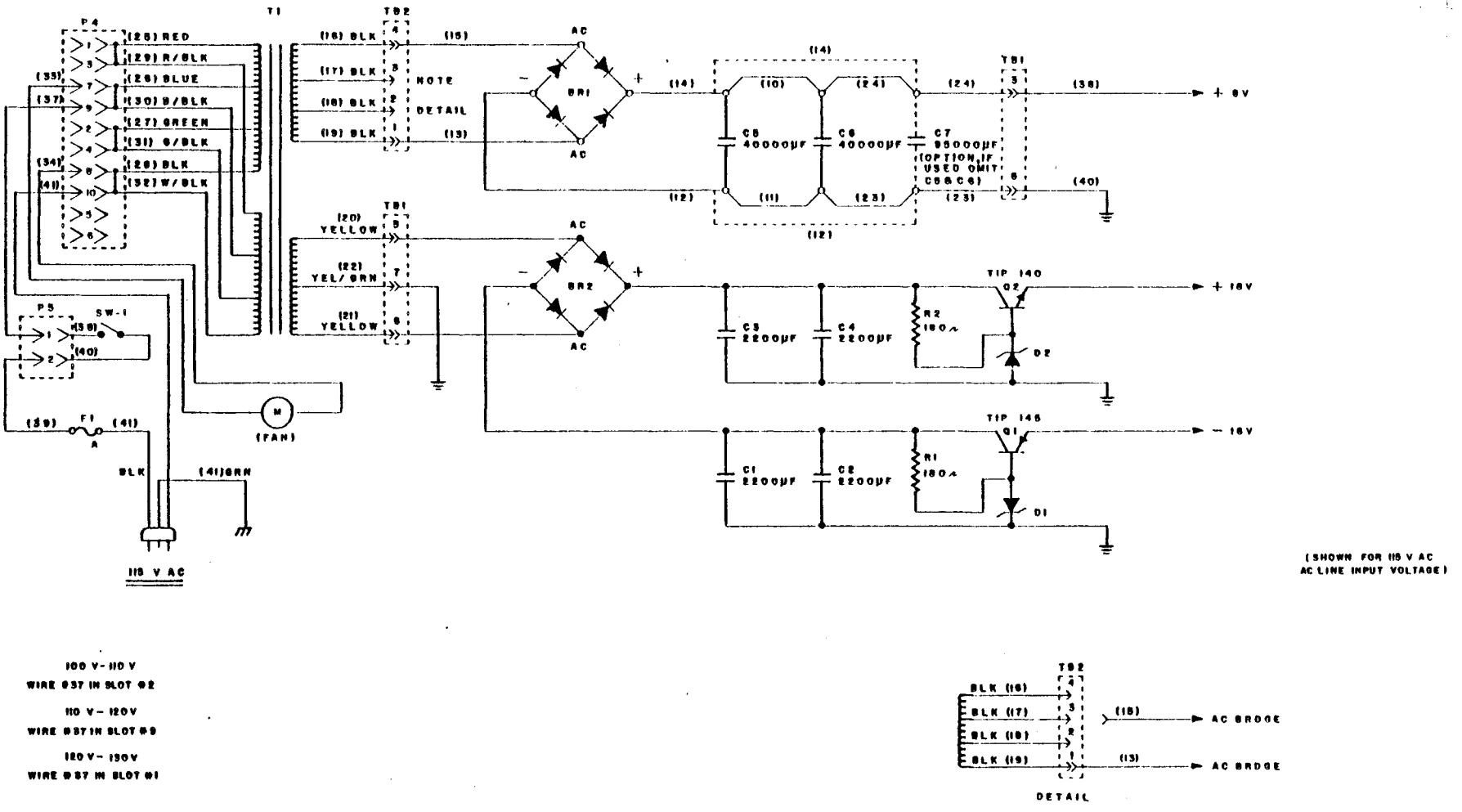


Figure 2-7
Power Supply Schematic

SECTION 3
ADVANCED OPERATIONS

3. ADVANCED OPERATION

3-1. The Front Panel

The Front Panel contains the functional switches and status indicators for controlling and monitoring the computer. A list of the switches and indicators along with their functions follows:

Power switch	Turns power on and off. Key-lock switch
POWER indicator	Indicates that power is on. Monitors the +5 volt supply on the Turnkey Module.
RUN/STOP switch	Causes the computer to run the program in memory when placed in the RUN position. Execution stops in the middle of the next machine cycle after the switch is moved to the STOP position. Moving the switch back to RUN continues execution at the point where it was stopped.
START switch	When actuated, stops execution. When released, starts execution at the START address selected by switches on the Turnkey Module. If the switch is actuated when the RUN/STOP switch is in the STOP position, the computer stops in the middle of the START sequence. Moving RUN/STOP to RUN continues the START sequence.
HALT indicator	Indicates that the computer is stopped either because a HALT instruction has been executed or because the PRESET line is LOW.
I/O indicator	Indicates data transfer to or from an I/O port.
INT indicator	Indicates that an interrupt is being requested.
INTE indicator	Indicates that the Interrupt Enable bit is set in the CPU and that the computer may be interrupted. When the INTE indicator is off, interrupt requests have no effect.

3-2. The Turnkey Module

A. Memory. The Turnkey Module contains 1K bytes each of RAM and PROM. The starting address of each 1K block is selected by 6 switches on the Turnkey Module board (Figure 3-1). In operation, the most significant 6 bits of the incoming address are compared with the settings of the switches. If they match, the remaining 1Ø bits are decoded to select the proper byte in that block.

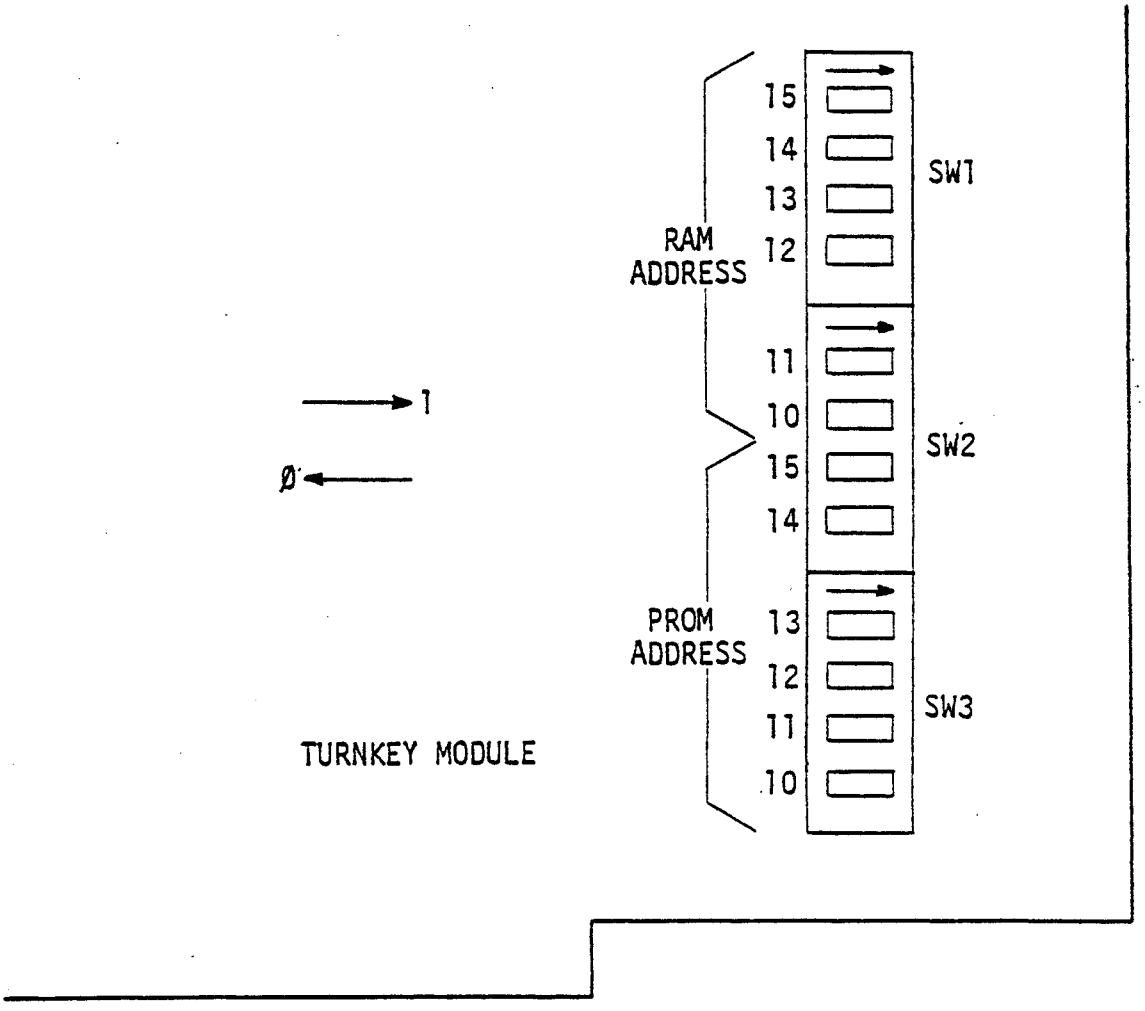


Figure 3-1
RAM and PROM Address Switches

To set the RAM and PROM address switches, first select the starting addresses for each block and convert them to binary. The starting addresses must be integral multiples of 1K (1024) so the low-order (rightmost) 10 bits of the addresses are zeros. The RAM and PROM addresses are zeros. The RAM and PROM addresses cannot be the same, nor may they overlap the addresses of any other memory in the system.

One starting address switch corresponds to each of the 6 high-order bits of the starting address (the most significant bit is bit 15). If the bit is one, the corresponding switch is moved in the direction of the arrow silkscreened on the board. If the bit is zero, the switch is moved in the opposite direction.

B. Sense Switches. There are eight sense switches on the Turnkey Module representing one byte of data. This byte may be read by program instructions and used as data or to select options in the program.

Sense switch settings are described in the documentation for the software products (such as Altair BASIC) that use the switches. Moving the Turnkey Module sense switches in the direction of the silk-screened arrow next to the switches is equivalent to moving a front panel switch up.

To allow use of the sense switches, there must be a jumper between points S and B on the Turnkey Module board as shown in Figure 3-2. If the Turnkey Module is being used in a standard model Altair 8800b computer, the front panel switches override the Turnkey Module sense switches. The sense switches may be read by the following instruction:

Assembly	IN 255
Machine (octal)	333 377

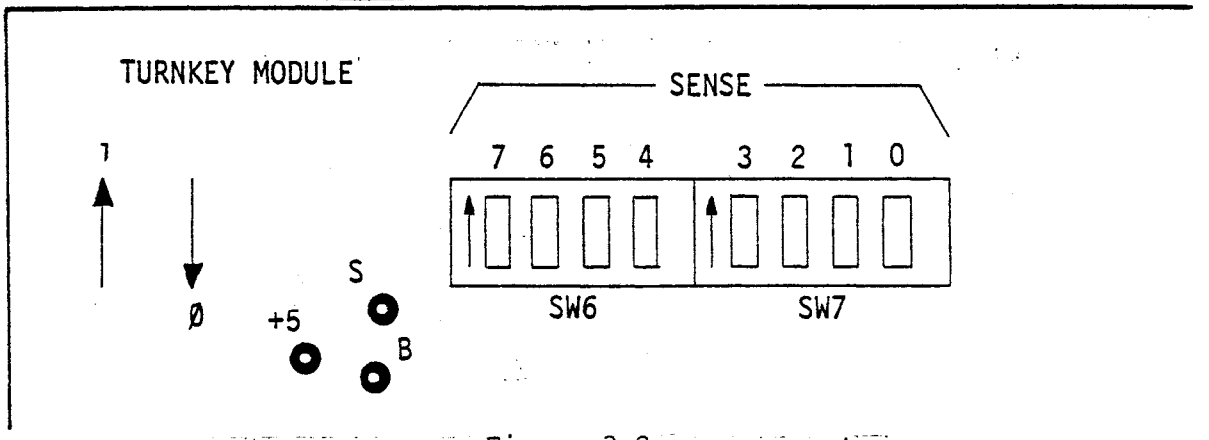


Figure 3-2
Sense Switches and Jumper Pads

C. SIO Section.

1) The Turnkey Module SIO channel appears to the CPU as two of the 256 possible I/O ports (see IMSUM, Section 3, pp. 8 -10). One of the ports is used for data transfer and the other for channel status and control information. Table 3-A is a summary description of the SIO ports.

The high-order seven bits of the I/O address are compared with the SIO address switch settings. If they match, the channel is enabled. The least significant bit selects the Data (bit zero=1) or Status/ Control (bit zero=0) port. To set the switches, convert the desired address to binary. Move each switch in the direction of the silk-screened arrow to represent one and in the opposite direction for zero. Switch 7 represents the most significant bit.

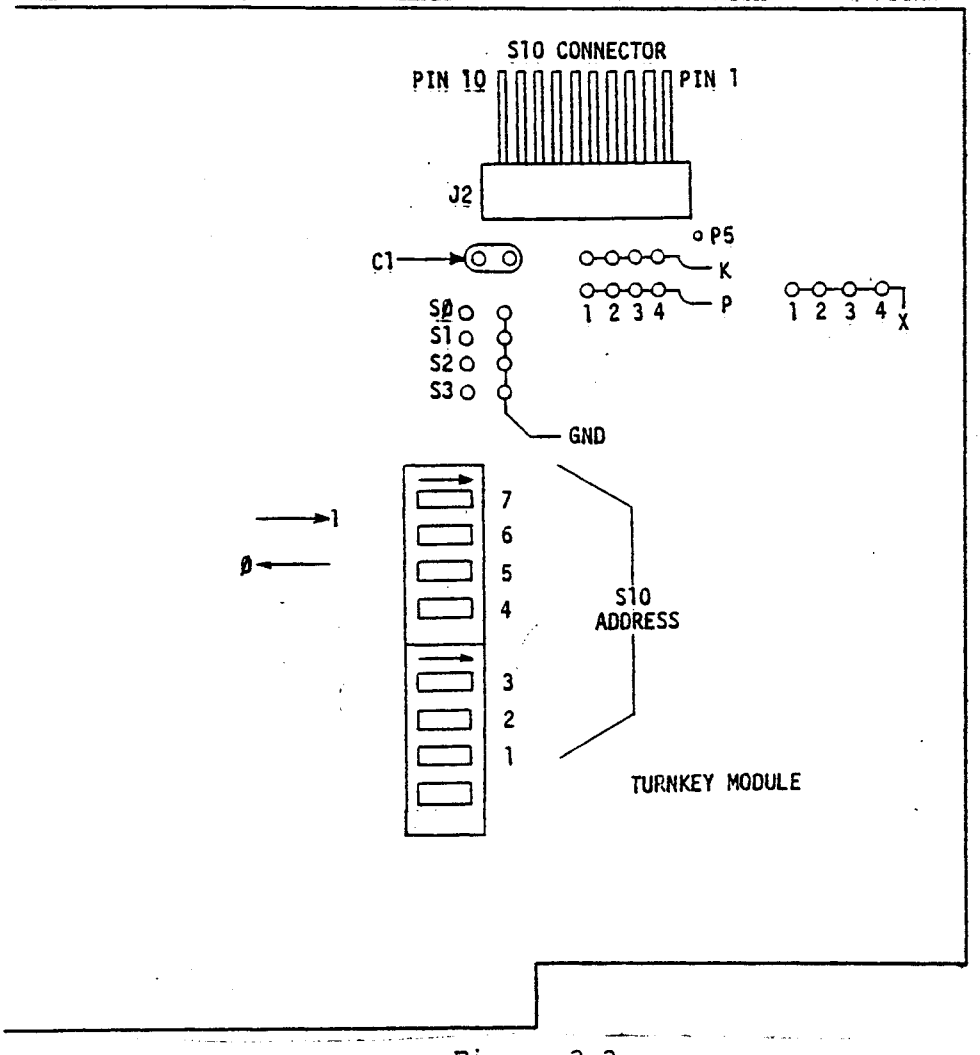


Figure 3-3
SIO Address Switches and Jumper Pads

Table 3-A

Address	Function when read during an Input Operation	Function when loaded during an Output Operation
S_7 S_6 S_5 S_4 S_3 S_2 S_1 1	Receive Data Buffer (Data is stripped of parity)	Transmit Data Buffer
S_7 S_6 S_5 S_4 S_3 S_2 S_1 0	Status	Control
S_1 through S_7 refer to the binary representation of the positions of the SIO address select switches		

2) The Status Register. When the Status/Control port is read during an input operation, the Status Register contains information on the status of the Transmit Data Register, the Receive Data Register and error logic, and the peripheral/modem status inputs. The function of each bit of the status register is given in the table below.

a. Receive Data Register Full (RDRF), Bit Ø. Receive Data Register Full indicates that received data has been transferred to the Receive Data Register. RDRF is cleared after the CPU reads the Receive Data Register or by a master reset. The cleared or empty state indicates that the contents of the Receive Data Register are not current. RDRF also indicates empty if Data Carrier Detect is LOW.

b. Transmit Data Register Empty (TDRE), Bit 1. The Transmit Data Register Empty bit set to 1 indicates that the Transmit Data Register contents have been transferred and that new data may be entered. A zero indicates that the register is full and that transmission of a new character has not begun since the last write data command.

c. $\overline{\text{Data Carrier Detect}}$ ($\overline{\text{DCD}}$), Bit 2. When the DCD input from a modem goes LOW to indicate that a carrier is not present, the $\overline{\text{Data Carrier Detect}}$ bit is set to 1. This setting causes an Interrupt Request to be generated if the Receive Interrupt Enable bit is set. After the DCD input returns HIGH, $\overline{\text{DCD}}$ remains one until it is reset, either by reading first the Status Register and then the Data Register, or by a master reset. If the DCD input remains LOW after the Status and Data Registers have been read or a master reset occurs, the $\overline{\text{DCD}}$ bit remains the inverse of the DCD input.

d. $\overline{\text{Clear-to-Send}}$ ($\overline{\text{CTS}}$), Bit 3. The $\overline{\text{Clear-to-Send}}$ bit is the inverse of the Clear-to-Send input from a modem. Thus, zero in $\overline{\text{CTS}}$ indicates that there is a Clear-to-Send from the modem. When the Clear-to-Send signal is LOW, the Transmit Data Register Empty bit is inhibited and the $\overline{\text{CTS}}$ status bit is set to one. Master reset does not affect the $\overline{\text{CTS}}$ bit.

e. Framing Error (FE), bit 4. A framing error occurs when the received character is improperly framed by a start and a stop bit. It is detected by the absence of the first stop bit. This indicates a synchronization error, faulty transmission or a break condition. The Framing Error flag, FE, is set during the receive data transfer time. Therefore, the error indicator is present throughout the time that the associated character is available.

f. Receiver Overrun (OVRN), bit 5. OVRN is an error flag that indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receive Data Register (RDR) before subsequent characters were received. The overrun condition begins at the midpoint of the last bit of the second character received without the RDR having been read. The OVRN bit is not set in the Status Register until the valid character prior to the overrun has been read. The RDRF bit remains set until OVRN is reset. The OVRN bit is reset when data is read from the Receive Data Register or by the master reset. Character synchronization is maintained during the overrun condition.

g. Parity Error (PE), bit 6. The Parity Error flag indicates that the number of ones in the character does not agree with the preselected parity. Odd parity is defined as the condition in which the total number of ones in the character is odd. Even parity means the number of ones is even. The parity error indication is present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

h. Interrupt Request (IRQ), bit 7. IRQ indicates the state of the IRQ signal. Any interrupt condition, with its applicable enable, is indicated in this status bit. Anytime the IRQ signal is LOW, the IRQ bit is one to indicate the interrupt or service request status. Section 2-2.C.4. shows how to jumper the IRQ signal to an interrupt line on the bus.

3) The Control Register. When the Status/Control port is loaded during an output operation, the Control Register contains information which controls the functions of the receiver and transmitter, interrupt enables and the Request-to-Send peripheral/modem control input. The Control Register bits and their functions are shown below.

a. Counter Divide Select, bits Ø and 1. The Counter Divide Select Bits determine the clock divide ratios used in both the transmitter and receiver sections of the SIO. Additionally, these bits are used to provide a master reset for SIO which clears the Status Register (except for external conditions on the CTS and DCD lines) and initializes both the receiver and transmitter. Master reset does not affect other Control Register bits. Note that after power-on or a power failure/restart, these bits must be set HIGH to

reset the SIO. After reset, the clock divide ratio may be selected. The counter select bits provide for the following clock divide ratios:

CR1	CRØ	Ratio
Ø	Ø	1 (synchronized)
Ø	1	16 (normal)
1	Ø	64 (slow)
1	1	master reset

Section 3-2.C.5. describes the use of these bits to select the baud rate.

b. Word Select, bits 2, 3 and 4. The Word Select Bits are used to specify word length, parity and the number of stop bits in each character. Word length, Parity Select, and Stop bit changes are not buffered and therefore become effective immediately. The encoding format is as follows:

CR4	CR3	CR2	Function
Ø	Ø	Ø	7 bits, even parity, 2 stop bits
Ø	Ø	1	7 bits, odd parity, 2 stop bits
Ø	1	Ø	7 bits, even parity, 1 stop bit
Ø	1	1	7 bits, odd parity, 1 stop bit
1	Ø	Ø	8 bits, two stop bits
1	Ø	1	8 bits, one stop bit
1	1	Ø	8 bits, even parity, one stop bit
1	1	1	8 bits, odd parity, one stop bit

c. Transmitter Control, bits 5 and 6. Two Transmitter Control Bits provide for control of the interrupt from the Transmit Data Register Empty condition, the Request-to-Send output, and the transmission of a break level (space). The setup of interrupt jumpers are shown in Section 3-2.C.4. The following coding is used:

CR6	CR5	Function
Ø	Ø	RTS = HIGH, Transmitting Interrupt disabled
Ø	1	RTS = HIGH, Transmitting Interrupt enabled
1	Ø	RTS = LOW, Transmitting Interrupt disabled
1	1	RTS = HIGH, transmits a break level on the transmit data output, Transmitting disabled.

d. Receive Interrupt Enable, bit 7. Receive Data Register Full, Overrun and Data Carrier Detect interrupt requests are enabled by a 1 in the Receive Interrupt Enable Bit. The setup of interrupt jumpers is shown in Section 3-2.C.4.

4) Interrupts. The SIO generates an interrupt signal that may be connected to an interrupt line on the bus by means of jumpers. The jumper pads are shown in Figure 3-4.

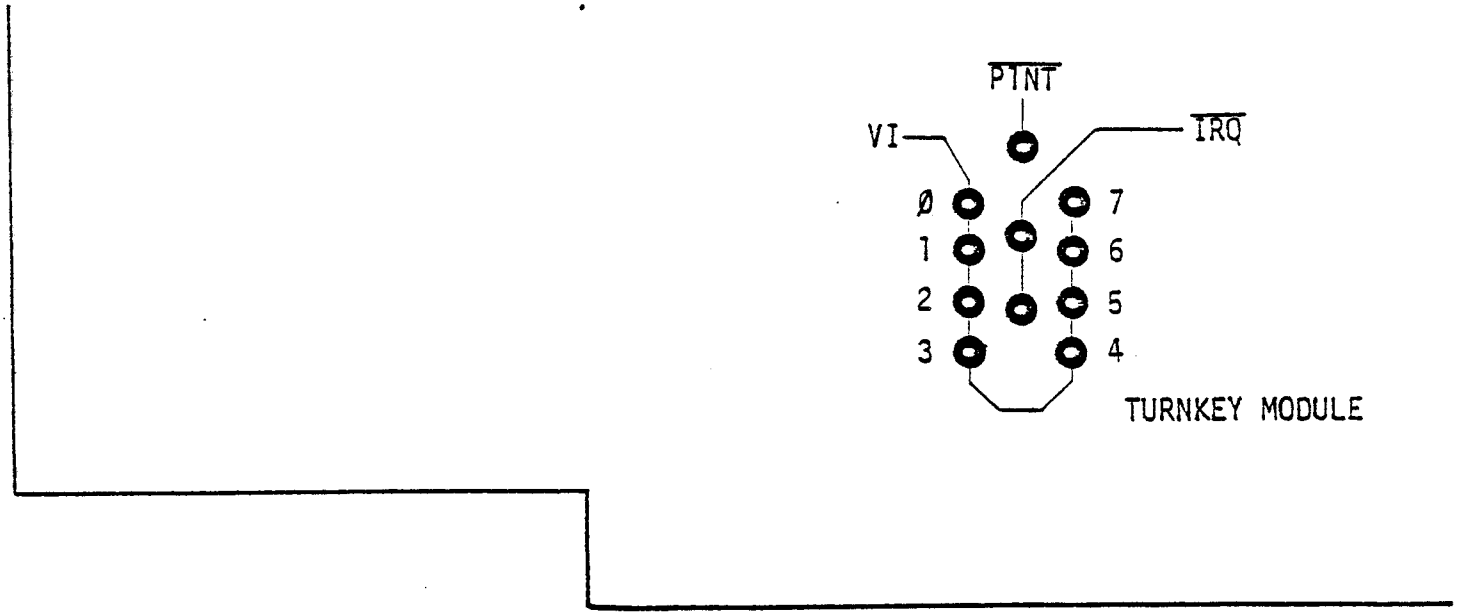


Figure 3-4
SIO Interrupt Jumper Pads

a. No jumper is installed if the SIO is not required to interrupt the CPU. Software can detect Status Register bits in this case and direct I/O operations without interrupts.

b. In systems not using the Vector Interrupt board, the signal IRQ may be connected to the $\overline{\text{PINT}}$ line. Then, if an SIO interrupt occurs, $\overline{\text{PINT}}$ will be pulled LOW until the condition that caused the interrupt no longer exists. If the Interrupt Enable bit in the CPU is set, then a RST 7 instruction is forced into the instruction sequence. Interrupt signals from other I/O circuits may also be connected to the $\overline{\text{PINT}}$ line if their outputs are effectively driven by open collector drivers. All Altair I/O boards currently manufactured and supported have open collector interrupt signal drivers. See the appropriate I/O board manual for more information.

c. In systems using the Vector Interrupt board, IRQ may be connected through a jumper to any pad marked VIØ through VI7. These represent the 8 interrupt priority levels. Interrupt signals from different boards may be connected to the same priority level if they are all driven by open collector drivers. See the Vector Interrupt board manual for further information.

5) Bit Rate Selection. In this section, 'bit rate' is defined as the maximum rate of level changes on the data signal line. Since the SIO is an asynchronous device, the bit rate determines the rate at which the bits within each character are received or sent, but not, in general, the average rate at which characters are handled.

The bit rate is selected by jumpers and by Control Register bits 1 and Ø. Table 3-B shows the resultant bit rate for every usable combination of jumpers and control bits. The jumpers SØ, S1, S2 and S3 are shown in Figure 3-3. If CRØ and CR1 are both zero and the external rate is not selected, then the SIO may only be used for transmission. Otherwise, the SIO may be used for both receiving and transmitting at the selected rate. If a rate above 3ØØ bits per second is selected, capacitor C1 should be removed.

If the external clock and the 1 counter are selected, then the data must be synchronized with the clock. The transmitted data line changes levels within one microsecond of the LOW to HIGH clock transition. Output jitter is about 5ØØ ns. The SIO will sample the receive data line within 1 microsecond after the HIGH to LOW clock transition.

Table 3-B

Data Transmission Rates						
Jumpers (X means installed)				CR0 = 1 CR1 = 0 (normal; 16 counter selected)	CR0 = 0 CR1 = 1 (slow; 64 counter selected)	CR0 = 0 CR1 = 0 (sychronous data; 1 counter selected)
S3	S2	S1	S0			
-	-	-	-	110	27.5	1760
-	-	-	X	150	37.5	2400
-	-	X	-	300	75	4800
-	-	X	X	2400	600	38400
-	X	-	-	1200	300	19200
-	X	-	X	1800	450	28800
-	X	X	-	4800	1200	76800
-	X	X	X	9600	2400	153600
X	-	-	-	2400	600	38400
X	-	-	X	600	150	9600
X	-	X	-	200	50	3200
X	-	X	X	134.5	33.375	2152
X	X	-	-	75	18.75	1200
X	X	-	X	50	12.5	800
X	X	X	-	External 16 rate	External 64 rate	External rate
X	X	X	X	(36,000 max)	(9000 max)	(400,000 max)

6) Signal Types. The SIO can be configured to interface with peripheral equipment using 20 mA loop, RS232C and TTL signals. These signal options are selected by jumpers and internal cable connections. Table 3-C shows the I/O signal types. The locations of the jumpers are shown in Figure 3-3. The cable runs from the I/O connector on the Turnkey Module to the rear panel. The rear panel connector is the industry standard 25-pin data communications connector.

Table 3-C

Signal Type	From	To	Notes
TTY Compatible	X1	X2	
	K4	P5	
	K3	P3	
	K2	P2	
RS232 Compatible	X3	X4	
	K3	P3	Put in only if DCD signal is not used.
	K2	P2	Put in only if CTS signal is not used
TTL Compatible (3.2 mA max load 16 mA min drive)	X2	X3	
	K4	P4	
	K3	P3	
	K2	P2	
	K1	P1	Not needed if external clock is not used.

Note: TTL inputs are two unit loads; input is actually "TTL compatible."

Table 3-D shows the connections of the internal cable.

D. Interfacing. This section describes interfacing of the SIO through the 25 pin rear panel connector to modems, RS 232 terminals or current loop terminals. The terminal's instruction book should be consulted for the proper choice of signal types.

Table 3-D

From Molex		To 25 Pin Connector		
Pin Number	Function	Female TTY Cable	Male RS232 Cable	Female TTL Cable
1	TTL RTS	6		4
2	TTY XMIT	3		
3	TTY REC	4		
4	All REC	5	2	2
5	DCD		8	8
6	CTS		5	5
7	XTERNAL CLOCK		15	15
8	GND	2	7	7
9	RS232 RTS		4	
10	RS232 + TTL XMIT		3	3

1) Connection to a modem is through a male to female extension cable. The board and internal cable are set up for RS-232 I/O.

2) To connect to a Teletype, first unplug the Teletype, then loosen the three thumb-screws in the back and remove the roll of paper, the Mode Switch knob and the face plate. Remove the four screws under the nameplate and the small screw on the reader cover. The cover can now be removed.

The interconnection between the computer's SIO and the Teletype is shown in Figure 3-5. Connection is made to terminal strip 1514111, which is at the right rear of the Teletype.

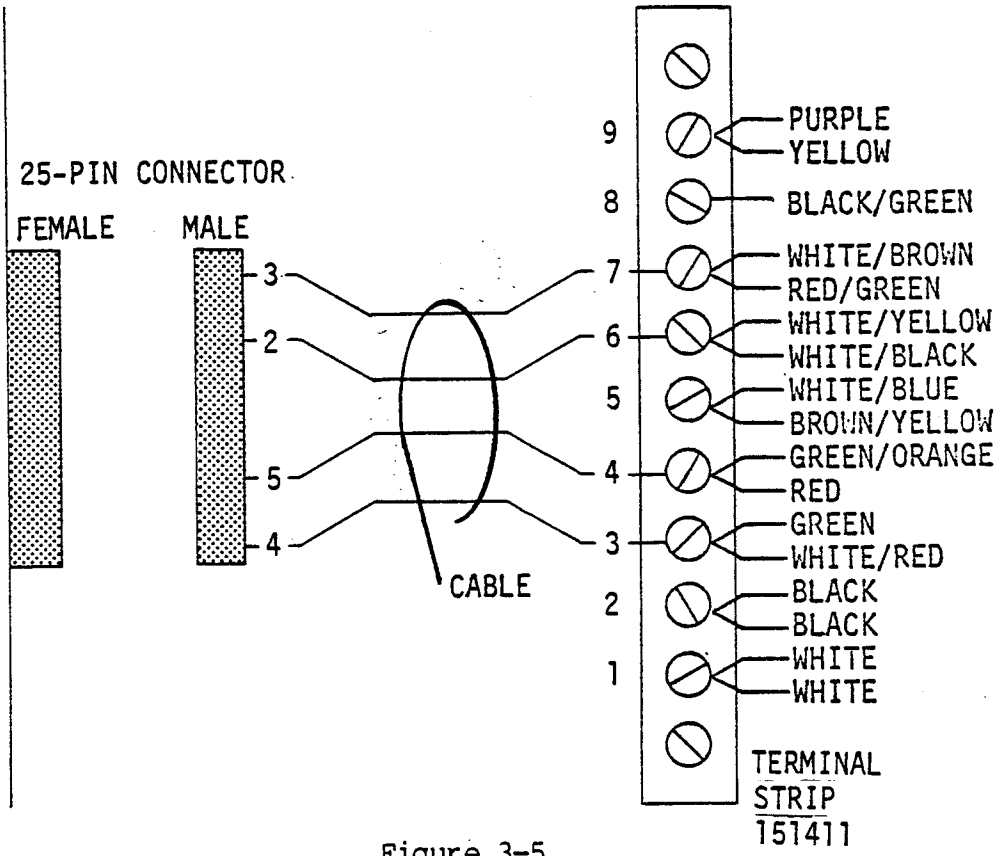


Figure 3-5
20mA Current Loop (TTY)
I/O Connections

While the cover is off, check that the Teletype is wired for 2ØmA, full duplex operation. The unit is set for full duplex if the Brown/Yellow wire is on terminal 5 and not on 3, and the White/Blue wire is on terminal 5 and not on 4 of terminal strip 1514111. The receiver current level is set to 2Ø mA if the Purple wire is connected to terminal 9 and not to 8. The correct connections are shown in Figure 3-5. The current source resistance for local mode should be connected as 145Ø ohms. This resistor is on the right hand side of the Teletype, halfway back.

After the connections and modifications are made, replace the cover, faceplate, knobs, paper roll and screws.

Be sure that the Turnkey Module and the internal cable have been set up for TTY I/O.

3) For RS-232 input/output, the cable is wired as shown in Figure 3-6. Note that the cable is symmetrical. The SIO of the Turnkey Module and the internal cable must be set up for RS-232 I/O.

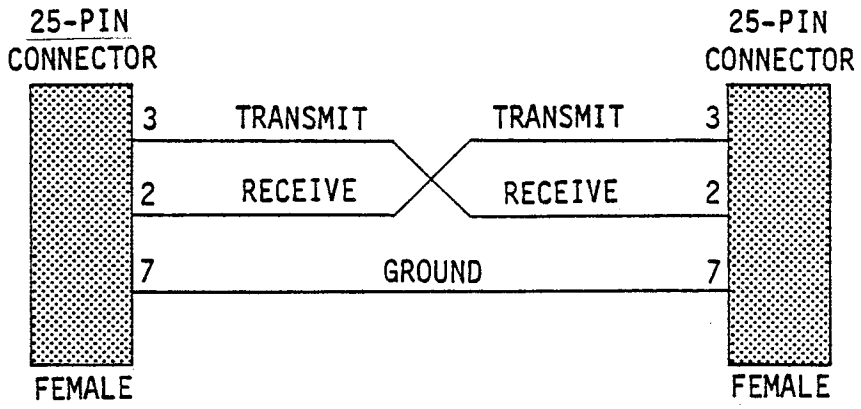


Figure 3-6
RS-232 I/O Connections

3-3. AUTO-START

When power is turned on, or when the START switch is released, the start sequence logic forces the CPU to begin executing instructions at an address selected by a set of switches on the Turnkey Module. The switches are shown in Figure 3-7.

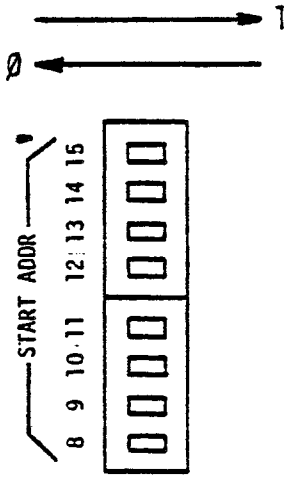


Figure 3-7
AUTO-START Address Switches

The AUTO-START switches are set in the same manner as the RAM and PROM address switches (see section 3-1). The AUTO-START address is the address of the first location of a routine in PROM. The address must be an integral multiple of 256, so the low order eight bits must be zeros. The eight AUTO-START switches correspond to the high-order eight bits of the AUTO-START address. Bit 8 is the least significant bit.

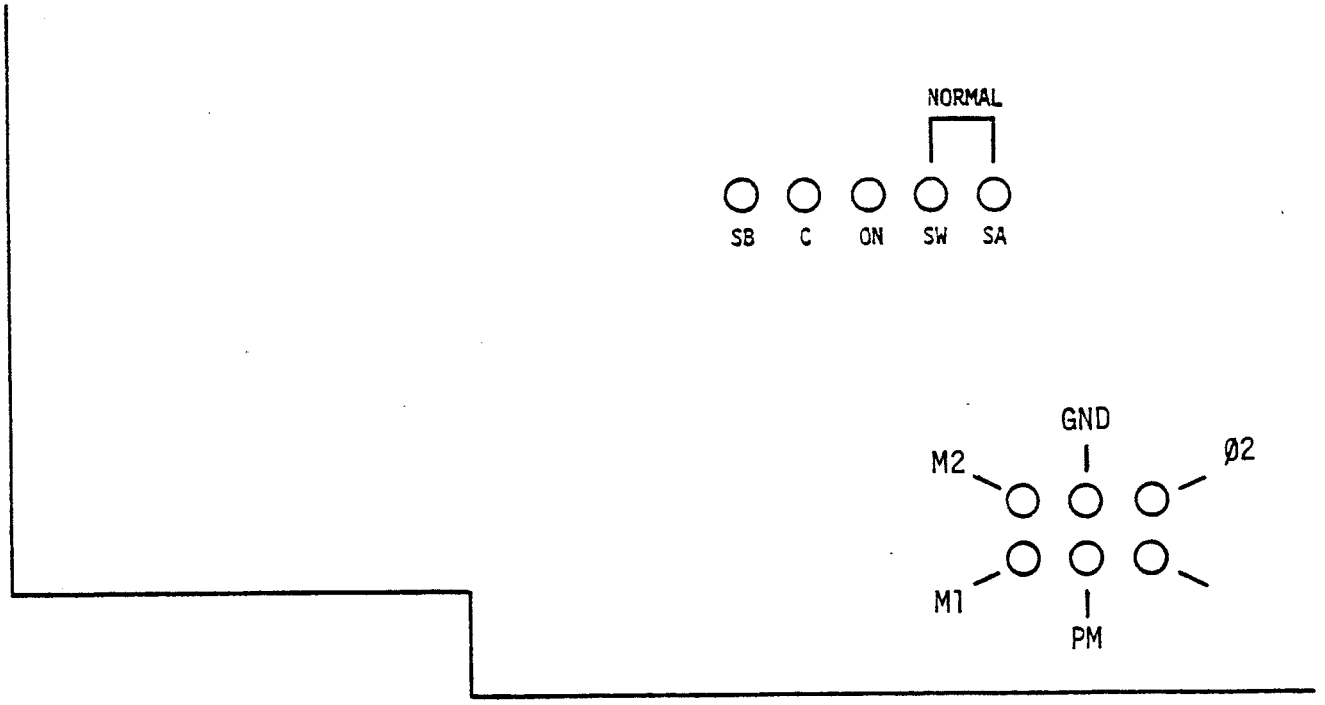
If the 88ØØb Turnkey Monitor PROM is installed, the AUTO-START address must be 176ØØ octal. Therefore, all the AUTO-START switches except switch 9 must be in the "1" position.

3-4. Miscellaneous Options

A. Use of Turnkey Module with Front Panel Model. The Turnkey Module may be used in the standard (full front panel) model of the Altair 88ØØb computer. To do this, the following jumpers must be removed from the Turnkey Module board:

M1 to M2
PM to GND
Ø2 to UM

Figure 3-8 shows these jumpers.



Section 3-8
Miscellaneous Option Jumper Pads

Table 3-E

Configuration	Jumpers	Cause	Effect
Normal	SA to SW	Power On	$\overline{\text{POC}}$ pulse
			START
		START switch	START
Alternate #1	SA to SW	Power On	$\overline{\text{POC}}$ pulse
	SB to C		START
			$\overline{\text{AUX CLR}}$ pulse
		START switch	START
			$\overline{\text{AUX CLR}}$ pulse
Alternate #2	ON to SW	Power On	$\overline{\text{POC}}$ pulse
			START
		START switch	$\overline{\text{POC}}$ pulse
			START
Alternate #3	ON to SW	Power On	$\overline{\text{POC}}$ pulse
	SB to C		START
			$\overline{\text{AUX CLR}}$ pulse
		START switch	$\overline{\text{POC}}$ pulse
			START
			$\overline{\text{AUX CLR}}$ pulse
Alternate #4	SA to SW	Power On	$\overline{\text{POC}}$ pulse
	ON to C		START
			$\overline{\text{AUX CLR}}$ pulse
		START switch	START

B. POC and AUX CLR options. As supplied, the computer generates the POC pulse when the power is turned on, but does not generate the AUX CLR pulse. This may be changed by jumpers between the pads marked C, ON, SA, SB and SW. These pads are shown in figure 3-8. Table 3-E shows the options available. The AUX CLR pulse is generated by a panel switch on the standard model of the 8800b computer and may be used by peripheral devices.

3-5. The Power Supply

A. Adjusting for differing loads. The +18 and -18 volt supplies are pre-regulated, but the +8 volt supply must be adjusted for differing loads by moving the tap on the power transformer secondary. The transformer secondary taps are shown in Figure 3-9. The correct secondary tap

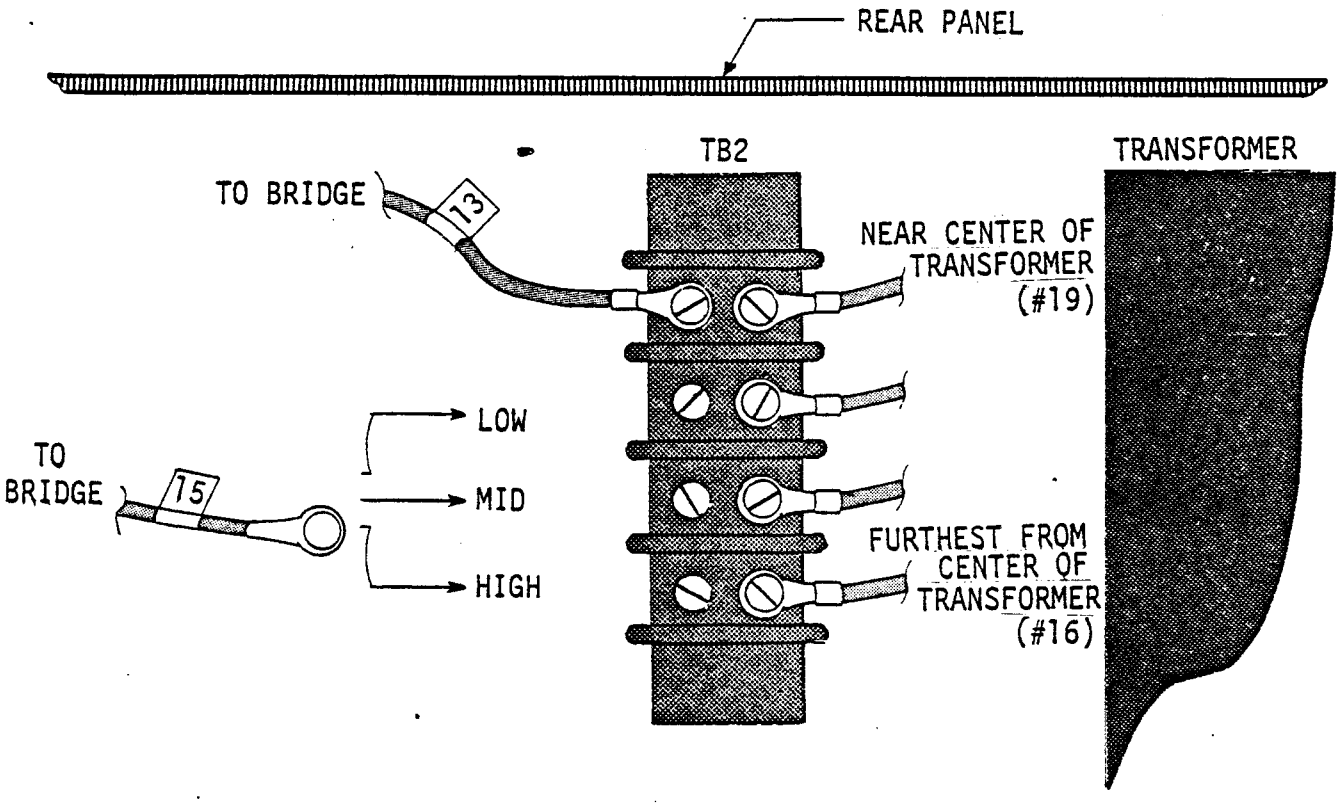


Figure 3-9
Power Transformer Secondary Taps

is determined experimentally. The procedure for adjusting the tap is as follows:

1. Disconnect the computer from its A.C. supply.
2. Connect wire 15 from the bridge rectifier to one of the secondary taps on the transformer as shown below:

Number of Boards in the Computer	Transformer Tap
Ø-6	low
7-12	middle
13-18	high

3. Connect the A.C. supply and measure the voltage between pins 1 and 5Ø on the motherboard.
4. If the measured voltage is greater than 9 volts, the next lower tap should be used if it is available. If the voltage is less than 7.5 volts, the next higher tap should be used. Be sure to disconnect the power cord before moving the transformer tap connection.

B. Power Supply capacity. The power supplies can power most systems that can be accommodated in the case. Only an unusually large system will tax the resources of the power supplies.

The A.C. line into the power supply is furnished with a 3 amp, slow-blow fuse. It should be replaced as necessary only with an identical fuse.

SECTION 4
TROUBLESHOOTING HINTS

4. TROUBLESHOOTING HINTS

4-1. Introduction

This section is not an extensive troubleshooting guide, but rather contains guidelines that can save the troubleshooter time. Knowledge of electronics and of the contents of Sections 2 and 3 of this manual is required for troubleshooting.

A. Equipment. An oscilloscope with 30 MHz or greater bandwidth is normally required to troubleshoot this unit. A voltage meter may be required in some measurements. In most cases, either a logic analyzer or a full panel version of the Altair 8800b computer is also needed. If the Turnkey Module is used with the front panel, remove jumpers as described in paragraph 3-9. To display both address lines and data lines on the logic analyzer, clock on the falling edge of IC W pin 8 on the Turnkey Module. To view data going to the Data Out bus as well as the Data In bus, make connections to the bi-direction bus on the CPU board.

B. Troubleshooting Optional Boards. Troubleshooting optional memory and I/O boards is covered in the manuals for those boards. The directions in these manuals often assume that a full front panel is used, presenting test loops to be executed in the single step mode. If a full front panel is not used, use a logic analyzer and a test program instead.

C. Trouble Follows Change. An error in system change, jumper installation, repair or board modification can cause trouble. If a system change has been made, be sure that all Turnkey Module jumpers are installed as shown in Section 3. If boards were added, be sure that the +8 volt bus has the correct voltage. Check that all boards and connectors are well seated and mated correctly. If the trouble follows jumper installation, repair or board modification, check for solder bridges and poor solder connections. If the trouble follows repair, check that the IC pins were inserted into the sockets properly.

4-2. Preliminary Considerations

A great deal of time can be saved by some preliminary checks.

A. First, check that all connectors and boards are well seated, that the unit is plugged in and that the fuse is not open.

B. Corner the problem by removing boards from the unit and by swapping boards with good ones, if possible. Use this method with caution; a board with a damaged bus driver may look OK when a good board is removed from the system, because the load is reduced. If a board fails catastrophically, several boards may be damaged along with cabling and power wiring. In this case, each board should be tested in another system.

C. Check for incorrect voltage and noise on the regulated voltages of every board plugged into the motherboard. The tolerances for the regulated voltages generated on the CPU board and the Turnkey Module are tabulated below.

Board	Voltage	Tolerance
CPU	+12	5%
	+5	5%
	-5	5%
Turnkey Module	+5	5%
	+9	10%
	-9	-1.Ø volt
		+Ø.5 volt

D. Check the clock on the CPU board. This may be monitored at IC J pin 3. The correct frequency is 2.Ø MHz.

4-3. CPU

The CPU board requires less troubleshooting than the circuits on the Turnkey Module. When troubleshooting the CPU, monitor TTL buffered signals rather than MOS driven signals as much as possible, to avoid loading the 8Ø8ØA IC. When monitoring the 8Ø8ØA outputs, use a low capacitance XIØ probe. See IMSUM (section 5, pp. 13-19, 163-166, 1-4) for nominal signals and timing measurements for the 8Ø8ØA, 8216 and 8224 ICs.

4-4. Turnkey Module

A. AUTO-START. AUTO-START should be one of the first functions tested if there are no other clues to the trouble. AUTO-START is tested with a front panel as shown in the table below. Depressing the RESET or STEP switch should produce the displays shown in the table.

Press Switch	Address Indicators	Data Indicators	Status Indicators
RESET	Ø	3Ø3	M1
STEP	1	ØØØ	none
STEP	2	setting of start address switches	none
STEP	start address	-----	M1,MEMR

If a logic analyzer is used instead of a front panel, depress the START switch on the Turnkey front panel and monitor at running speed.

B. PROM. If AUTO-START is operating properly and the computer still does not start, there may be a problem with the PROM circuitry. Most PROM problems can be found by stepping through the AUTO-START sequence and then through the program, monitoring key signals on the Turnkey Module. It should be possible to read every PROM location from the front panel. Problems may be masked when stepping through PROM, though, by the logic which generates WAIT states. The most common PROM problems are bent PROM IC pins, loss of -9 volts, bad PROM ICs, trouble in the wait state logic and incorrect address setting.

C. RAM. Correctly functioning RAM can be read from and written into from the front panel. The most common RAM problems are incorrect setting of the starting address switches and bad RAM ICs.

D. Sense Switches. Because software uses the sense switches to make decisions, trouble with the sense switches may look like trouble elsewhere. The front panel sense switches on the Altair 88ØØb computer override the sense switches on the Turnkey Module even if the logic on the Turnkey Module does not work correctly. So, if the trouble disappears when the front panel is used, check the sense switches as well as the logic that generates the MWRITE pulse.

E. Serial I/O Channel. Watch out, the trouble may not be here. A Teletype may run open if the SIO is not initialized because of trouble in the PROM circuitry, the logic for the sense switches, the AUTO-START logic or the CPU. Trouble with the sense switches may also cause the SIO channel to seem to be malfunctioning in other ways.

1) To check out the SIO, monitor a character echo loop, either by stepping through it using a front panel, by using a logic analyzer or, in a limited way, by using a different SIO channel to control a debug routine. As the status register is input, verify the correctness of each bit. Note that DCD should be Ø. Then, by examining the operation of the loop, decide if the problem is in the transmitter or the receiver.

2) The output of the baud rate generator can be checked at pin 1Ø of IC G. It should be a square wave with a frequency 16 times the selected baud rate. For verification on the oscilloscope, the periods for some popular baud rates are shown below:

Baud Rate	Clock Period
11Ø	568 µs
3ØØ	2Ø8 µs
12ØØ	52 µs

3) The most common sources of SIO problems are incorrect jumper installation, incorrect cabling, trouble in the wait state logic, damaged MOS ICs and catastrophic damage due to high voltages on the I/O lines.

8800b-sm & -dm
DOCUMENTATION
PART III
MINIDISK SYSTEM

SECTION 1
INTRODUCTION

1-1. MITS ALTAIR MINIDISK SYSTEM DESCRIPTION

The mass storage sub-sbystem for the 8800b-sm and -dm is a MITS Altair Minidisk system with a storage capacity of 71,680 bytes per minidiskette. The worst case access time for any byte of data is less than three seconds. The system consists of two controller boards that plug into the computer motherboard and the minidisk drive assimbly which includes the drives, power supply, buffers and addressing circuitry.

The Minidisk controller provides the interface between the Minidisk system and the computer. It communicates with the computer through three I/O ports which transmit all data, control and status signals. The controller uses a "hard sectorred" data format for simplicity. A built-in timer turns the drive motor off if the system has not been accessed for more than three seconds. This helps increase motor life.

The address of each drive is set by switch SW-1 on the drives buffer/address circuitry board. This board is physically attached to the drive by spring clips. The drive addresses are set at the factory (0 for a single drive, 0 and 1 for dual drives), but the addresses may be changed according to the following chart.

Drive Address	SW-1 Setting 1	2	3	4
0	off	off	off	off
1	on	off	on	off
2	off	on	off	on
3	on	on	on	on

1-2. SPECIFICATIONS

A. MITS Altair Minidisk System Summary

The Minisdisk system includes a set of two controller boards that plug into the computer motherboard and connect to the drives through cables. The controller boards are powered by the computer's DC power supplies. The drive assembly includes one or two drives, one buffer/address circuitry board for each drive and a power supply.

B. 88-MDS Controller Specifications

1) Number of slots required in 8800 bus - 2
2) Number of ICs
   - TTL Logic -- 57
   - CMOS -- 1
   - Voltage Regulators - 2
3) I/O Addresses (Octal) - Ø1Ø, Ø11, Ø12
4) Data Transfer Rate - 1 byte every 64µs.
5) Data Format - Hard Sectored (16 sectors)
6) Interrupt System - Interrupt at beginning of Sector (Optional - not used for Minidisk BASIC)
7) Power Requirements - 1.4A @ 8V

C. 88-MDDR Drive Specifications

1. Performance Specifications:
   a) Data Capacity - Hard Sectored Format
      - Per Minidiskette -- 71,680 Data Bytes
      - Per Track -- 2,048 Data Bytes
      - Per Sector -- 128 Data Bytes
   b) Data Transfer Rate - 125,000 Bits Per Second
   c) Access Time
      - Disk Enable to READ or WRITE (Function of motor start-up time) -- 1 sec. (min)
      - Track to Track -- 50 ms.
      - Average Access Time (including motor start-up time) -- 1.85 sec.
      - Worst Case Access Time -- 2.9 sec.
      - Worst Case Latency -- 200 ms.
2. Functional Specifications:
   a) Rotational Speed -- 300 rpm (200 ms/rev.)
   b) Track Density -- 48 Tracks per inch
   c) Number of Tracks -- 35
   d) Number of Sectors -- 16
   e) Time Per Sector -- 12.5 ms.

3. Reliability Specifications of Minidisk Drive:
   a) Error Rates
      - Soft (recoverable) errors -- 1 per 10^8 bits READ
      - Hard (unrecoverable) errors -- 1 per 10^{11} bits READ
   b) MTBF -- 8000 Hrs. (25% motor run time)
   c) Service Life -- 5 years
   d) Media Life -- 3.0×10^6 Passes/Track
4. Power Requirements:
   a) Minidisk Drive
      - Standby -- 25 watts, typical
      - Operating -- 35 watts, typical

      } 110V or 220V, 60HZ or 50HZ

SECTION 2
THEORY OF OPERATION

2-1. GENERAL

This section contains information needed to understand the operation of the MITS Altair Minidisk System (88-MDS). It contains a description of the logic symbols used in the Minidisk schematics and a detailed theory of operation.

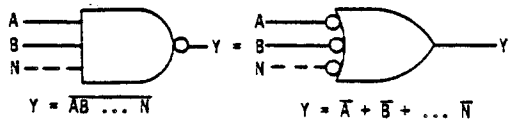
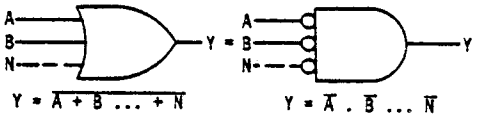
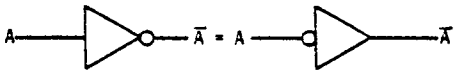
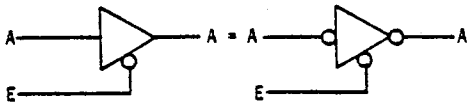
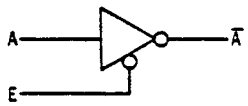
2-2. LOGIC CIRCUITS

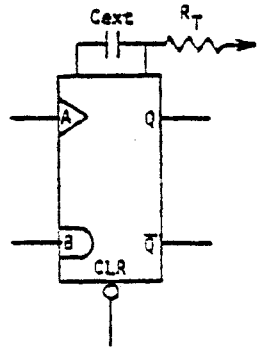
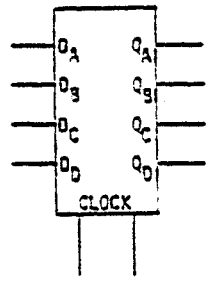
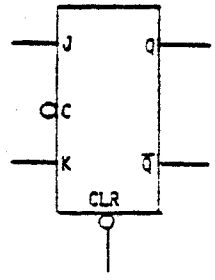
The logic circuits used in the schematics are presented as a tabular listing in Table 2-A. The table is constructed to present the functional name, symbolic representation and a brief description of each logic circuit. Truth tables are provided to aid in understanding circuit operation where applicable. The active state of the inputs and outputs of the logic circuits is graphically displayed by small circles. A small circle at an input to a logic circuit indicates that the input is an active LOW; that is, a LOW signal will enable the input. A small circle at the output of a logic circuit indicates that the output is an active LOW; that is, the output is LOW in the actuated state. A bar over the signal description also indicates an active LOW. Conversely, the absence of a small circle on the input or output, or a bar over the signal description indicates an active HIGH.

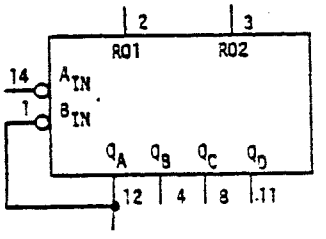
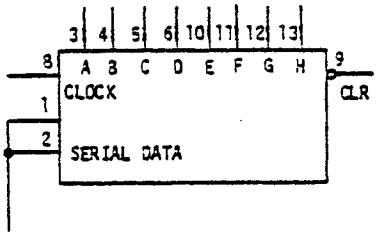
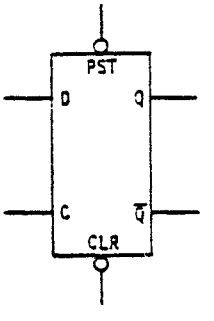
2-3. SCHEMATIC REFERENCING

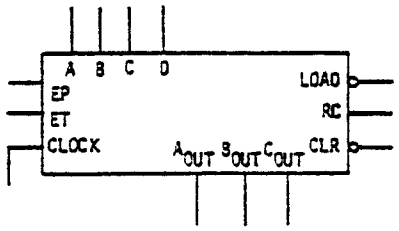
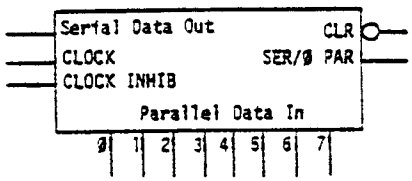
The detailed schematics are provided to aid in determining signal direction and tracing. A solid arrow (➙) on the signal line indicates direction, and the tracing of the signal through the schematics is referenced as it leaves the page. The reference is shown as a number - letter number (e.g. 2-A3), indicating Sheet 2 and schematic Zone A3.

Table 2-A. Symbol Definitions

Name/Logic Symbol	Description
AND gate 	All the inputs have to be enabled HIGH to produce the desired HIGH output. The output is LOW if any of the inputs are LOW.
NAND gate 	All of the inputs have to be enabled HIGH to produce the desired LOW output. The output is HIGH if any of the inputs are LOW.
NOR gate 	Any of the inputs need to be enabled HIGH to produce the desired LOW output. The output is HIGH if all of the inputs are LOW.
Inverter 	The inverter is a device whose output is the opposite state of the input.
Non-Inverting Bus Driver 	When enabled, the non-inverting bus driver is a device whose output is the same state as the input. Data is enabled through the device by applying a LOW signal to the E input. The output "floats" or goes to a high impedance state when the non-inverting bus driver is not enabled.
Inverting Bus Driver 	The inverting bus driver is a device whose output is the opposite state of the input when enabled. Data is enabled through the driver by applying a LOW signal to the E input. The output "floats" or goes to a high impedance state when the non-inverting bus driver is not enabled.

Retriggerable Monostable Multivibrator (74123) 	The multivibrator is essentially a pulse generator whose pulse width may be varied by changing the value at two external components. Output pulse = $.32\ R_T\ C_{ext}\ \left(1+\frac{.7}{R_T}\right)$ R_T is in K ohms. C_{ext} is in pf. Output pulse is in nsec. Before an output pulse is terminated, the output of a retriggerable multivibrator may be triggered again, allowing output pulses of long duration.
Quad D Latch (74L75) 	When the clock is HIGH, information present at data inputs (D_A-D_D) is transferred to the Q_A-Q_D outputs. Data is latched on the falling edge of the clock pulse. The data is inverted when the $\overline{Q}$ outputs are used.
Dual J-K Master-Slave Flip-Flop (74L73 or 74LS73) 	When inputs are conditioned with J HIGH and K LOW and the flip-flop is clocked at C, the Q output either goes or remains HIGH, but cannot go LOW. If J and K are both HIGH, the Q outputs will toggle. Applying a LOW signal to the clear (CLR) input resets the flip-flop with Q LOW and $\overline{Q}$ HIGH. Clocking occurs on a HIGH to LOW transition at the clock (C) input.

4-Bit Binary Counter (7493) 	Output Q_A must be externally connected to the B_{IN} input. The count pulses are applied to the A_{IN} input. At the Q_A, Q_B, Q_C and Q_D outputs the 4-bit ripple through counter performs simultaneous frequency divisions of 2, 4, 8 and 16. When R01 and R02 are both HIGH, the Q outputs are reset LOW. Clocking occurs on a HIGH to LOW transition at the clock input.
8-Bit Parallel-Out, Serial-In Shift Register (74164) 	Clocking occurs on a LOW to HIGH transition of the clock input, shifting the data over one position. A LOW at either or both inputs inhibits entry of new data and resets the flip-flop LOW on the following clock pulse. When both inputs are HIGH, the A output is HIGH.
Edge Triggered D Type Flip-Flop (74L74) 	Applying a LOW signal to the clear input (CLR) resets the flip-flop with Q LOW and $\overline{Q}$ HIGH. If a signal is applied to the D input, the Q and $\overline{Q}$ outputs are directly affected on the positive edge of the clock pulse. (Q output follows D input)

Synchronous 4-Bit Counter (74L161 or 93L16) 	The synchronous 4-bit counter is used as a Divide by Eight Preset-table counter with internal carry (RC). When all outputs (A_{OUT}, B_{OUT} and C_{OUT}) are clocked HIGH, RC is HIGH. Data is transferred to the outputs when LOAD is LOW and a clock pulse is received. Clocking occurs on the rising edge of the clock pulse.
8-Bit Parallel-In, Serial-Out Shift Register (74166) 	When HIGH, the SER/ØPAR input enables the serial data input; when LOW, the parallel data inputs are enabled. During parallel loading (Ø-7), serial data flow (SERIAL DATA OUT) is inhibited. When clock inhibit (CLOCK INHIB) is held HIGH, clocking is inhibited. Clocking is accomplished on a LOW to HIGH level of the clock, shifting data over one position towards the serial data output.

2-4. MINIDISK SYSTEM BLOCK DIAGRAM

The 88-MDS system consists of three major sections:

1. The Altair 8800 computer and the appropriate hardware and software for operating the Disk System which is typically 32K of memory and Minidisk Extended BASIC.
2. Two Controller boards which interface the Altair 8800 computer to the Disk Drive (see Disk Controller Theory of Operation, beginning with paragraph 2-5).
3. The Disk Drive assembly which contains the Minidisk drive plus the line drives and receivers necessary for interconnection to the Controller and additional Disk Drives.

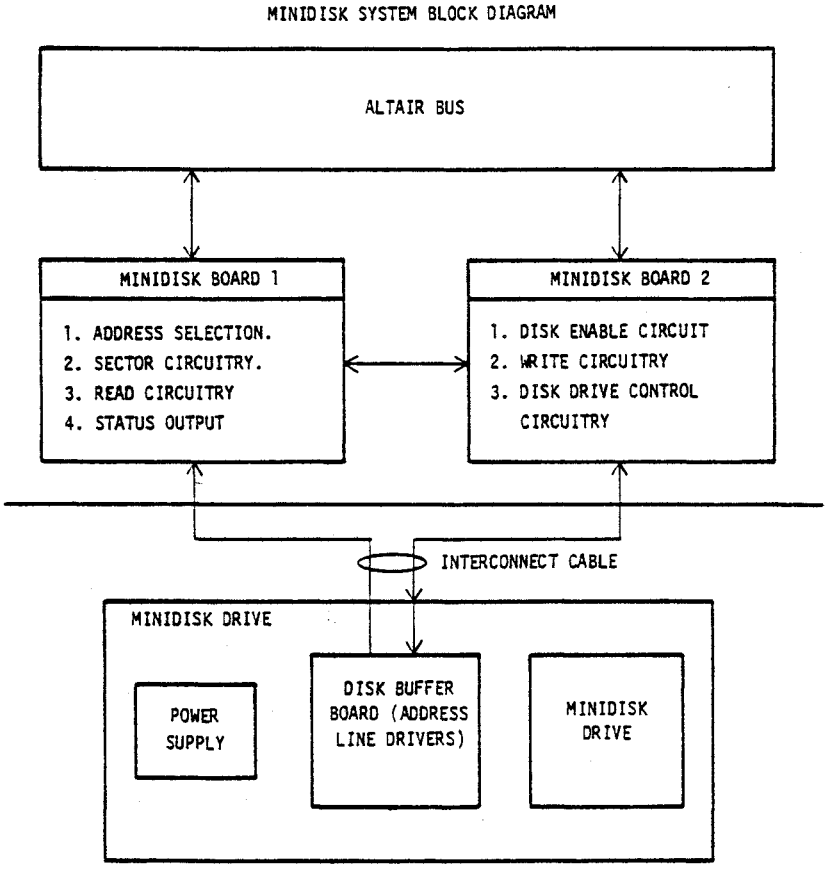


Figure 2-1. Minidisk System Block Diagram

2-5. GENERAL SYSTEM OPERATION

In order to begin Disk operation, the computer must select and enable the Disk Drive and Controller. The desired Drive address (ØØØ to $ØØ4_8$) is output on I/O Channel $Ø1Ø_8$. When the Drive is enabled, the head is automatically loaded and the motor starts. TRACK Ø is found by stepping the head out to the outermost track (Output-Channel $Ø11_8$, Bit D1 = 1) and testing the Status (Input-Channel $Ø1Ø_8$, Bit D6 = 0).

After the appropriate reference for TRACK Ø is found, the Altair computer steps the head in (Output-Channel $Ø11_8$, Bit DØ = 1) to the desired track. Software determines which track the Disk head is on, once TRACK Ø has been found.

The correct Sector is located by performing an input from the Sector Channel (Input-Channel $Ø11_8$) and comparing the desired Sector number with the Sector count from the Controller circuit. After the Disk reaches the correct rotational position or Sector, the Altair computer performs either a Read Data function (Input-Channel $Ø12_8$, DØ-D7) or enters a Write Data mode. In the Write mode, the Write Circuits must be enabled (Output-Channel $Ø11_8$, D7 = 1). A few hundred microsecond delay elapses before Write Data is requested, after which a new byte of Write Data is requested every 32 microseconds.

When the computer has finished accessing the Disk, Disk Control is cleared (Output-Channel $Ø1Ø_8$, DØ through D7 = 1 or 377_8). Clearing Disk Control disables the Drive and causes all Disk functions to cease. Turning the Disk Drive power off, or disconnecting the cable also clears Disk Control.

When changing access from one Drive to another, Disk Control must be cleared (Output-Channel $Ø1Ø_8$, 377_8) before enabling the new Disk. This is to insure the Controller circuits are reset before accessing a new Drive.

2-6. MINIDISK CONTROLLER BLOCK DIAGRAM

The Minidisk Controller Address Select Circuit accepts input and output (I/O) instructions from the Altair computer on I/O Channels $\emptyset 1\emptyset_8$, $\emptyset 11_8$ and $\emptyset 12_8$. The Altair I/O ADDRESS LINES (8 lines) select one of the three I/O Channels and Altair I/O Status lines (4 lines) determine whether an input or output instruction is required. An I/O instruction to any channel results in a LOW going 500nsec. pulse (refer to Figure 4-2) on the respective enable line from the address select circuit (Board 1).

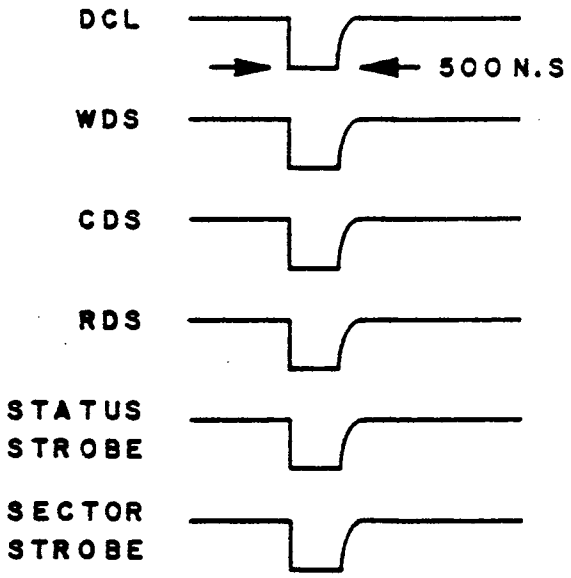


Figure 2-2. I/O Channel Timing

The three Output functions associated with Minidisk Board 2 are:

1. Output on Channel $\emptyset 1\emptyset_8$: DISK CONTROL LATCH (DCL) selects Disk address and enables Controller.
2. Output on Channel $\emptyset 11_8$: CONTROL DISK (CD) controls Disk Drive functions such as STEP IN or OUT, WRITE ENABLE, etc.
3. Output on Channel $\emptyset 12_8$: WRITE DATA STROBE (WDS) strobes WRITE DATA bytes into write data latch during Disk Write mode. WDS also resets ENWD (Enter New Write Data) Status bit until next byte is requested.

The three Input functions associated with Minidisk Board 1 are:

1. Input on Channel $\emptyset 1\emptyset_8$: Places Disk status information on the Altair Data Bus. Status information includes: HEAD STATUS (HS); OK TO MOVE HEAD (MH); ENTER NEW WRITE DATA (ENWD); NEW READ DATA AVAILABLE (NRDA).
2. Input on Channel $\emptyset 11_8$: Places the Disk Sector count on the Altair Data Bus. As the Disk rotates, the Sector count is incremented every 12.5ms , and is reset to 0 upon detection of the Index hole once every rotation (200ms).
3. Input on Channel $\emptyset 12_8$: Places Disk READ DATA on the Altair Data Bus. This input instruction resets the NRDA Status bit.

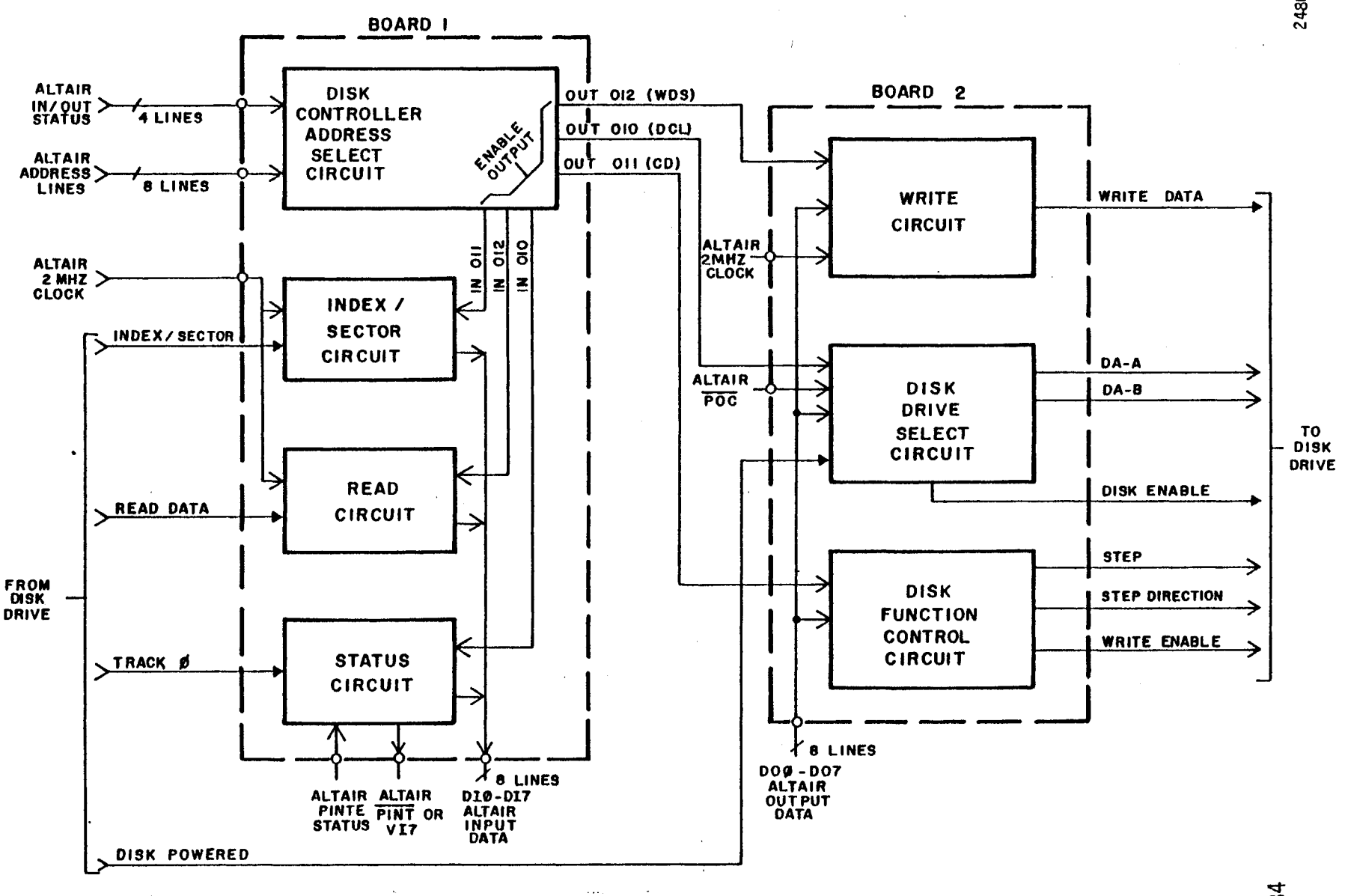


Figure 2-3. Disk Controller Block Diagram (Sheet 1, External Connections and Address Select)

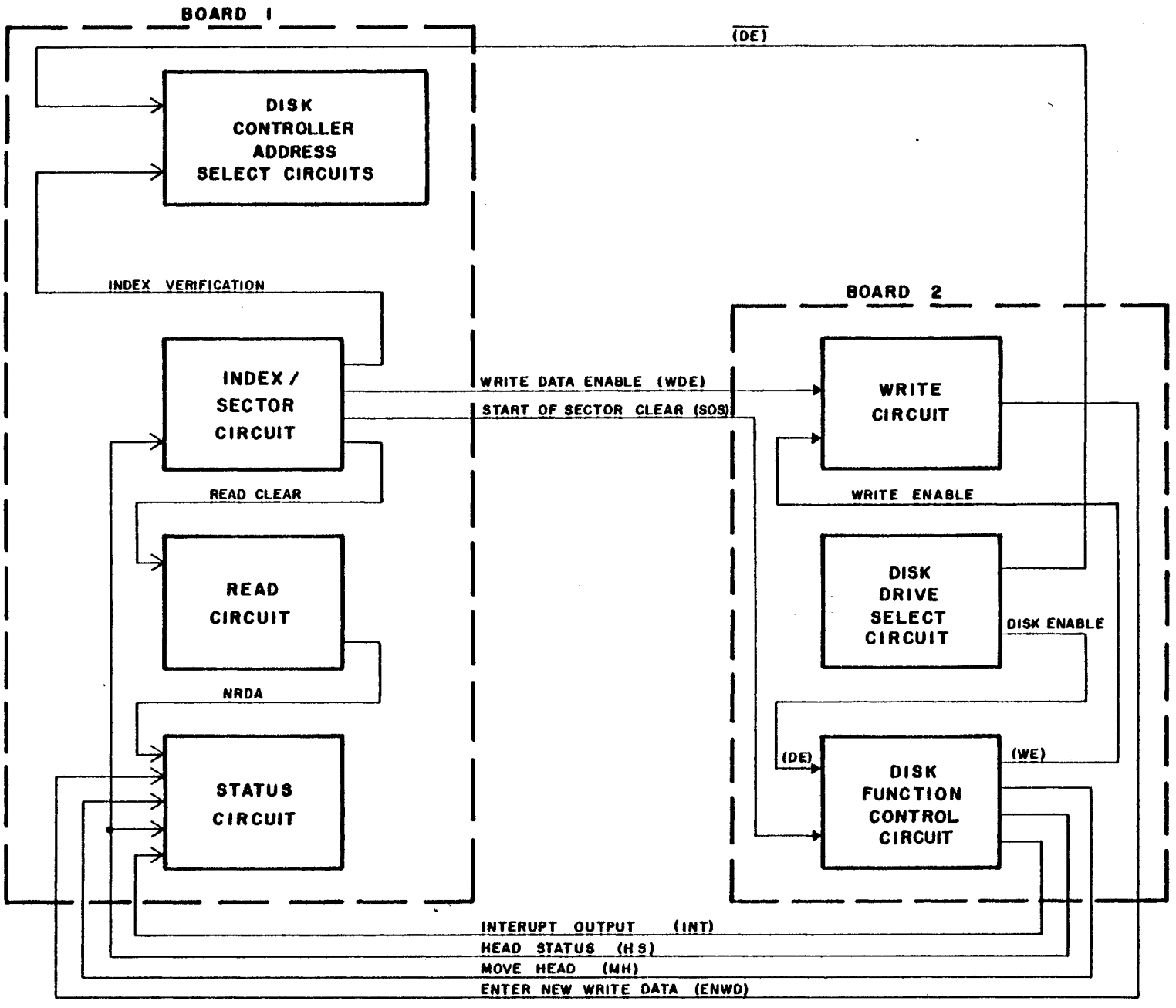


Figure 2-4. Disk Controller Block Diagram (Sheet 2, Internal Connections)

Upon an Output to Channel $\emptyset 1\emptyset_8$, the DISK CONTROL LATCH (DCL), Disk Drive Select Circuits are enabled with DA-A and DA-B, selecting one of four possible Minidisk Drives. The DISK POWERED line enables the Disk Drive Select Circuit when the Drive selected is properly connected and powered. When the Minidisk Drive is selected and enabled, the DISK ENABLE (DE) signal is presented to the Disk Function Control Circuit where DE enables the Status information.

The Disk Function Control Circuits, when selected, load the head on the Disk (HEAD LOAD), step the head out (STEP OUT), step the head in (STEP IN) and enable the Write Circuit (WRITE ENABLE). Control Circuits also produce INTERRUPT OUTPUT, MOVE HEAD or HEAD STATUS signals which are transferred to the Disk Status Circuits. Control signals, Disk address information and WRITE DATA are transferred from the Altair computer to Controller Board 2 by eight Output Data Lines (DØO-DØ7).

WRITE DATA is transferred to the Write Circuit upon an output to Channel $\emptyset 12_8$, the WRITE DATA STROBE (WDS). The rate of serial WRITE DATA to the Disk is controlled by dividing the Altair 2MHz Clock. ENTER NEW WRITE DATA (ENWD) is the Status signal generated by the Write Circuit when new WRITE DATA is requested.

When INDEX and SECTOR pulses are received by the Index/Sector Circuit, the INDEX pulse is detected, Sector count (beginning with Sector Ø) may begin. The Index/Sector Circuit is synchronized by the Altair 2MHz Clock, and upon an Output to Channel $\emptyset 11_8$, the Sector count is presented. The Index/Sector Circuit also provides a START OF SECTOR CLEAR (SOS) signal to the Disk Function Control Circuit, a WRITE DATA ENABLE (WDE) signal to the Write Circuit and the READ CLEAR signal to the Read Circuit. INDEX VERIFICATION and a True (LOW) condition on HEAD STATUS must be present before the Address Select Circuits can enable the Sector information from Channel $\emptyset 11_8$.

When READ DATA is present from the Disk Drive and transferred to the Altair Data Bus, the Read Circuit is enabled by addressing Input Channel $\emptyset 12_8$. The Read Circuit provides the NRDA (NEW READ DATA AVAILABLE) Status signal when READ DATA is detected.

The Status Circuit provides information on the state of the Controller and Disk Drive. A desired track is found by referencing TRACK Ø (the outermost track). TRACK Ø, NRDA and the other Status signals are enabled by addressing Input Channel $Ø1Ø_8$. Input data is transferred from the Index/Sector Circuit, Read Circuit or Status Circuit to the Altair computer by eight Input Data Lines (DIO-DI7).

2-7. ADDRESS SELECT CIRCUIT

The Address Control Circuit (Figure 2-14, Sheet 1) accepts I/O instructions from the Altair computer on Channels $Ø1Ø_8$, $Ø11_8$ and $Ø12_8$.

To enable any of the strobe gates A3, A4 or A5, F5 pin 8 (zone D7) must be enabled LOW. F5 pin 8 is LOW when address lines A15-A8 (zones C8 and D8) equal $Ø1X_8$. (X represents a User Selectable condition for A8-A10). A15-A12 is LOW, inverted HIGH at G5 pins 2, 4, 6 and 8 (zone D8) and appear HIGH at F5. With A11 HIGH, F5 pin 8 goes LOW and is inverted HIGH to A5 pin 1 (zone D6). Address lines A10-A8, when equal to $XXØ_8$, $XX1_8$ or $XX2_8$ (XX represents a User Selectable condition for address lines A11-A15 described above), enable one of the AND gates B4 pins 6, 8 or 12 (zone C6). When A8, A9 and A10 are all LOW, B4 pin 6 is enabled, allowing an Input or Output on Channel $Ø1Ø_8$. When A9 is HIGH and A10 and A8 are LOW, B4 pin 12 is enabled, allowing an Input or Output on Channel $Ø12_8$. When A8 is HIGH and A10 and A9 are LOW, B4 pin 8 is enabled, allowing an Input or Output on Channel $Ø11_8$. AND gates B4 determine the I/O Channel to be addressed since only one gate is enabled at a time. A specific output instruction is then selected if SOUT is HIGH and PWR is LOW (zone D8), and the specific input instruction is recognized when SINP and PDBIN are HIGH (zone D8). When the Disk is enabled, the Disk Enable line (DE, zone D8) goes HIGH, enabling the INPUT STATUS STROBE (Channel $Ø1Ø_8$) and allowing the Index Verification Flip-Flop, B3 (zone C3) to be clocked.

2-8. INDEX/SECTOR CIRCUIT ($Ø11_8$ - Input)

As the Minidiskette rotates in the Drive, an optoelectronic sensor detects the 16 Sector holes and the Index hole on the Diskette. The Sector holes generate a 4.4ms pulse every 12.5ms.. (Refer to Figure 4-5 for timing diagram relating to Index/Sector Circuits). The Index hole, located halfway between Sector holes 15 and Ø, generates a 4.4ms pulse every revolution (200.0ms.).

The Index or Sector pulse (IND) appears LOW and is inverted HIGH to E5 pin 2 (Figure 4-14, Sheet 1, zone C6). E5 pin 3 is enabled LOW until E3 pin 13 (zone C6) is clocked. The 2MHz Clock (zone B8) goes LOW at pin 49 of the bus and is inverted by J3 pin 8, clocking the Sector Pulse Compressor Flip-Flop, E3 pin 13 (zone C6). The output pulse width (500ns $\pm$ 250ns) of E5 pin 3 (zone C6) is dependent on the propagation time of the flip-flop and the delay time of the RC time constant of R7 and C30. After being inverted, E5 pin 3 appears HIGH at the Index Window Gate, A4 pin 11 (zone C5). A4 separates the Index pulse from the Sector pulses. A2 pin 10 is enabled HIGH when E5 pin 3 goes LOW. Sector Pulse One Shot, E1 pin 13 (zone C4), goes HIGH for 300µs which triggers Index Window One Shot, E1 pin 5 (zone C4), HIGH for 9.6ms. A4 pin 8 (zone C5) is only enabled when the Index pulse enables E5 pin 3 since E1 pin 4 (zone C4) and E1 pin 5 are HIGH at A4 pins 9 and 10 during this time. The 300µs LOW going pulse at E1 pin 4 also toggles the 4 Bit Sector Counter, G4 pin 14 (zone A3).

E1 pin 5 is HIGH, leaving A2 pin 8 (zone C5) HIGH when the Index pulse appears at A2 pin 9. As a result, A2 pin 10 is not enabled when the Index pulse appears, allowing only Sector pulses to trigger E1 pin 13 (zone C4). In addition to enabling E1 at pin 10 (zone C4), the HIGH 300µs pulse at E1 pin 13 is also present at E2 pin 10 (zone B6). E2 pin 8 is enabled LOW when E1 pin 13 is HIGH, since E3 pin 8 (zone B6) is in a reset condition (E3 pin 8 HIGH). The 2MHz Clock enables the Sector Pulse One Shot Compressor, F2 pin 9 (zone B7) HIGH, and on the

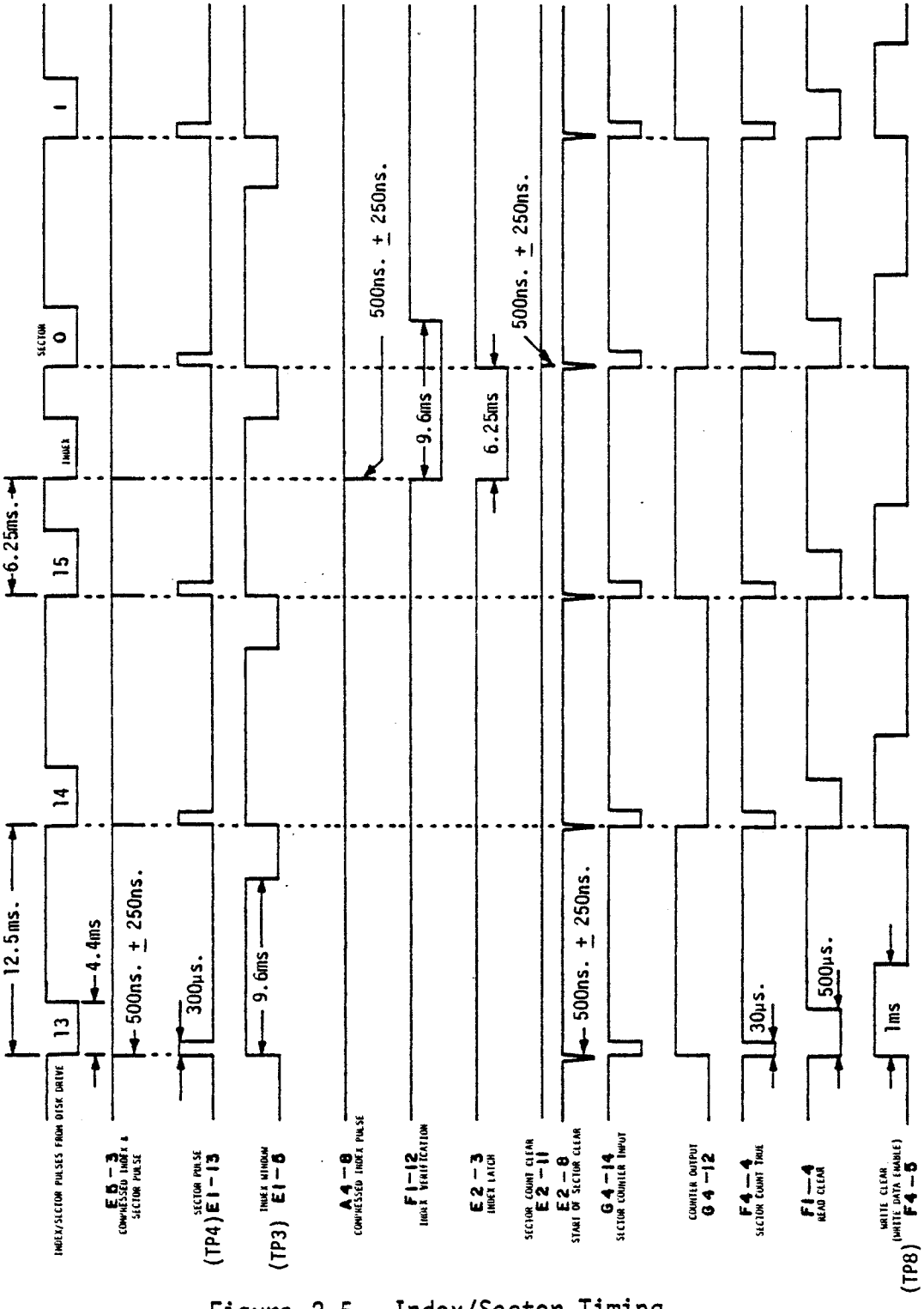


Figure 2-5. Index/Sector Timing

falling edge enables E3 pin 8 LOW. When E3 pin 8 goes LOW, E2 pin 8 is disabled. When E2 pin 8 is disabled HIGH, the Sector Count True One Shot, F4 pin 4 (zone A7), toggles LOW for 30µs. If it is the first Sector pulse after the Index pulse, the Index Latch, E2 pins 3 and 6 (zone A5) is reset, forcing E2 pin 3 HIGH. The LOW at E2 pin 8 also appears on board 2 (Figure 2-15, Sheet 1, zone A8) as the START OF SECTOR CLEAR (SOS) signal, which clears the Write Circuit at the end of a Write mode.

After a valid Index pulse has been detected, A4 pin 8 (Figure 2-14, Sheet 1, zone B5) is enabled LOW, setting the Index Latch with E2 pin 3 LOW. When E2 pin 3 is LOW, the Index Latch Pulse Compressor, F3 pin 13 (zone B5), is cleared. A4 pin 8 also triggers F1 pin 12 (zone B3) LOW for 9.6ms. After 6.25ms , the Index Latch is reset by a Sector pulse, leaving E2 pin 3 HIGH. E2 pin 11 (zone B5) is enabled LOW until the Index Latch Pulse Compressor Flip-Flop, F3 pin 13, is clocked by the 2MHz Clock pulse. The 500ns. (±250ns) output pulse at E2 pin 11 is dependent on the propagation time of F3 pin 13 and the delay time of the RC time constant of R8 and C20. A2 pin 1 (zone C3) is HIGH for 500ns (±250ns) if F1 pin 12 (zone B3) has been triggered LOW. This clocks B3 pin 8 (zone C3) LOW if B3 pin 7, the HEAD STATUS (HS) signal, is HIGH. HEAD STATUS should go HIGH 50ms. after the head is loaded on the Disk. A LOW at B3 pin 8 indicates that the correct Index pulse has been detected. The Index Latch, in allowing E2 pin 11 to be enabled, also resets the 4 Bit Sector Counter, G4, at pins 2 and 3 (zone A3), and the 5th Bit Sector Count Flip-Flop, F3 pin 6 (zone B4). Since this occurs on the first Sector pulse after the Index pulse, a correct Sector count is guaranteed every revolution. INPUT SECTOR STROBE (Channel $Ø11_8$) is enabled when A2 pin 4 (zone C2) goes HIGH. This occurs only when the Index Verification Flip-Flop is set (B3 pin 8 LOW) and the HEAD STATUS signal is LOW, indicating that the head is properly loaded for reading and writing. Drivers H5 pins 9, 11, 5, 7, 3 and 13 (zone B2) are then enabled when A3 pin 8 (zone B3) goes LOW. The Sector count is then transferred to the bus. The correct Sector is located by comparing the desired Sector number with the Sector count from this Index/Sector Circuit. Software also checks DIO to see if it is the beginning of the Sector.

When the Sector Count True One Shot, F4 pin 4 (zone A7), is triggered LOW for 30µs , Write Clear One Shot, F4 pin 5 (zone A5), goes HIGH for 1ms. F4 pin 5 is a timer that prevents Write Data (other than 0's) from begin written during the first 1ms. of a Sector by inhibiting the request for Write Data. When F4 pin 5 goes LOW, J3 pin 10 (zone A2) goes HIGH, enabling the Write Circuit to request Write Data. F1 pin 4 (zone B4) is also triggered by the Sector Count True One Shot, F4. F1 pin 4 is a timer that turns off the Read Circuit at the beginning of every Sector by going LOW for 500µs. This prevents the reading of false data at the beginning of a Sector, and insures proper synchronization with the Read Clock for detection of the sync bit.

2-9. READ CIRCUIT ($Ø12_8$ - INPUT)

Composite Read Clock and Data consisting of LOW going 1µs. pulses is received from the Disk Drive at Read Data Mask Gate, E5 pin 4 (Figure 2-14, Sheet 2, zone B6). The Read Clock pulse occurs every 8µs (±1µs), and the Read Data pulse occurs 4µs later if it is a logic 1 (refer to Figure 4-6). When a clock pulse is received, E5 pin 6 is enabled HIGH, triggering Read Clock One Shot, A1 pin 4 (zone B6), LOW for 2µs. This LOW is present at the Read Data Window Gate, A4 pin 13 (zone B4). A1 pin 13 is HIGH for 2µs , triggering the Read Data Window Gate, A1 pin 5 (zone B4), HIGH and A1 pin 12 LOW for 6.1µs. A1 pin 4 returns HIGH after 2µs., leaving A4 pin 13 and the Read Data Bit Latch, G2 pin 9 (zone B3) HIGH. If a logic 1 data bit is received at E5 pin 4, it is inverted HIGH by E4 pin 2 (zone B4), allowing A4 pin 12 (zone B4) to go LOW. This sets the Read Data Bit Latch, G2 pin 6 (zone B3) HIGH, indicating a logic 1 data bit has been received. After 6.1µs, A1 pin 12 (zone B4) returns HIGH and clocks the Read Data Serial to Parallel Shift Register, G1 pin 8 (zone C4). Serial Data at G2 pin 6 (zone B3) is then transferred to G1 pins 1 and 2. The Read Data Bit Latch is reset when A1 pin 4 (zone B6) receives the next clock pulse from the Disk Drive and returns LOW. If a logic Ø data bit is received at E5 pin 4 (zone B6), the Read Data Bit Latch remains reset (G2 pin 6 LOW) and a logic Ø is clocked into the Divide By Eight Counter, B1 (zone D6).

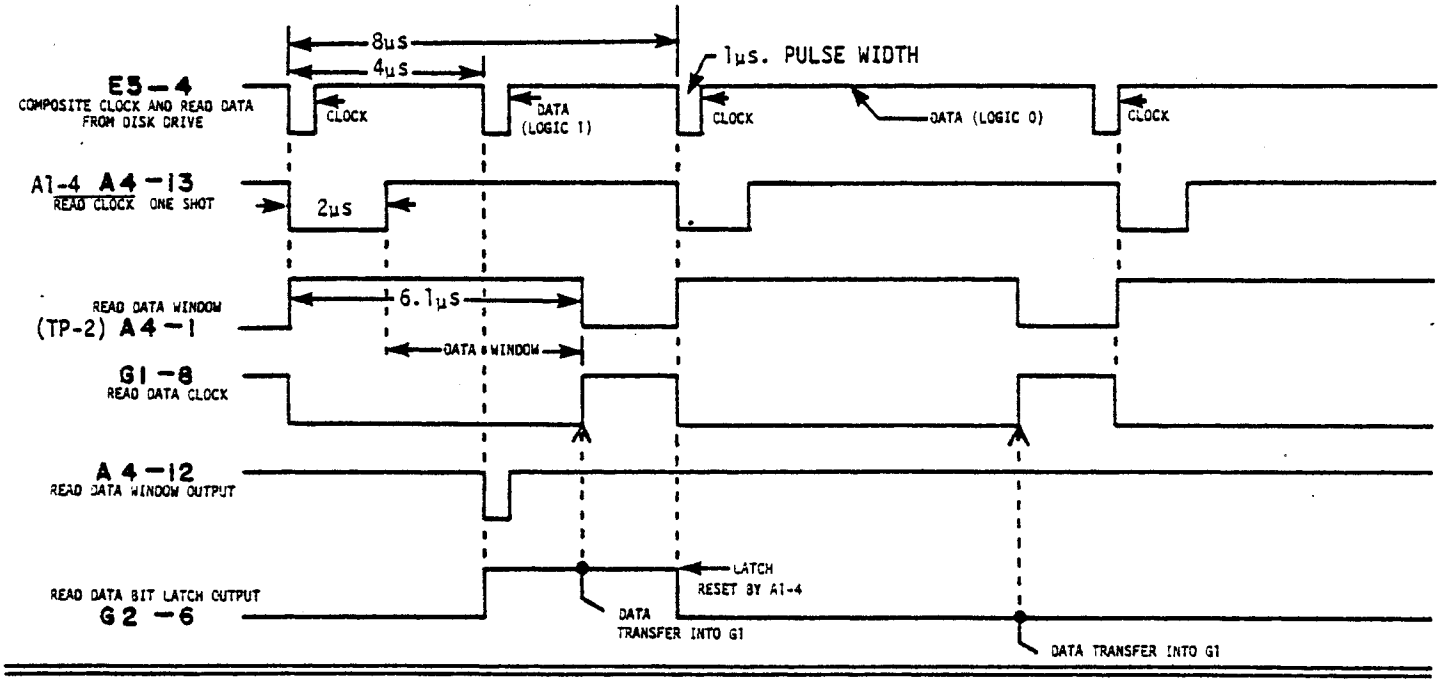


Figure 2-6. Read Circuit Timing

The sync bit is the first logic 1 data bit detected after the 500µs READ CLEAR pulse at the beginning of every Sector. B1 is held in a LOAD condition (does not count) until the sync bit is detected. Since Write Data is not enabled for 1ms from the beginning of a Sector, Read Data will not be available during that time. The Devide by Eight Presettable Counter, B1 (refer to Figure 2-7), counts eight read clocks and toggles on the trailing edge of the $\overline{Q}$ output at A1 pin 12 (zone B4). A2 pin 11 (zone D5) goes HIGH every 64µs. on the leading edge of the clock pulse at B1 pin 2. G1 pin 13 (zone C4) goes HIGH seven read data clocks after the sync bit has been detected and clocks the Sync Bit Detector Flip-Flop, B2 pin 8 (zone C7) LOW. B1 pin 15 returns LOW after 8µs., allowing A2 pin 13 (zone D5) to go HIGH. This enables G2 pin 3 (zone D4) LOW for 500ns. ($\pm$250ns) until the Read Latch Pulse Compressor Flip-Flop, F2 pin 1 (zone D7), is clocked. The output pulse width is dependent on the propagation time of the flip-flop and the delay time of the RC time constant of R21 and C29. When the Read Latch Pulse Compressor Flip-Flop, F2 pin 13, is clocked by the 2MHz Clock pulse at F2 pin 1, F2 pin 13 is enabled LOW, disabling G2 pin 3 (zone D4). When G2 pin 3 is enabled LOW and inverted by J3 pin 6 and J3

pin 4 (zone D3), data present at G1 outputs A through H is transferred to the D_A through D_D inputs of Read Data Latches, G3 (zone D3) and H1 (zone C3). The HIGH at J3 pin 6 also clocks the New Read Data Available Flip-Flop, B3 pin 13 (zone C6) LOW, enabling the New Read Data Available (NRDA) Status signal at H2 pin 14 (zone B2). As G2 pin 3 returns HIGH, the clock inputs of latches G3 and H1 go LOW and latch the data present at the D_A through D_D inputs to the Q_A through Q_D outputs. When an input is done on Channel $Ø12_8$ (INPUT READ DATA STROBE), line drivers H4 pins 9, 3, 5 and 7 (zone D2) and H3 pins 5, 7, 3 and 9 (zone C2) allow data at outputs Q_A through Q_D to be transferred to the Altair Data Bus.

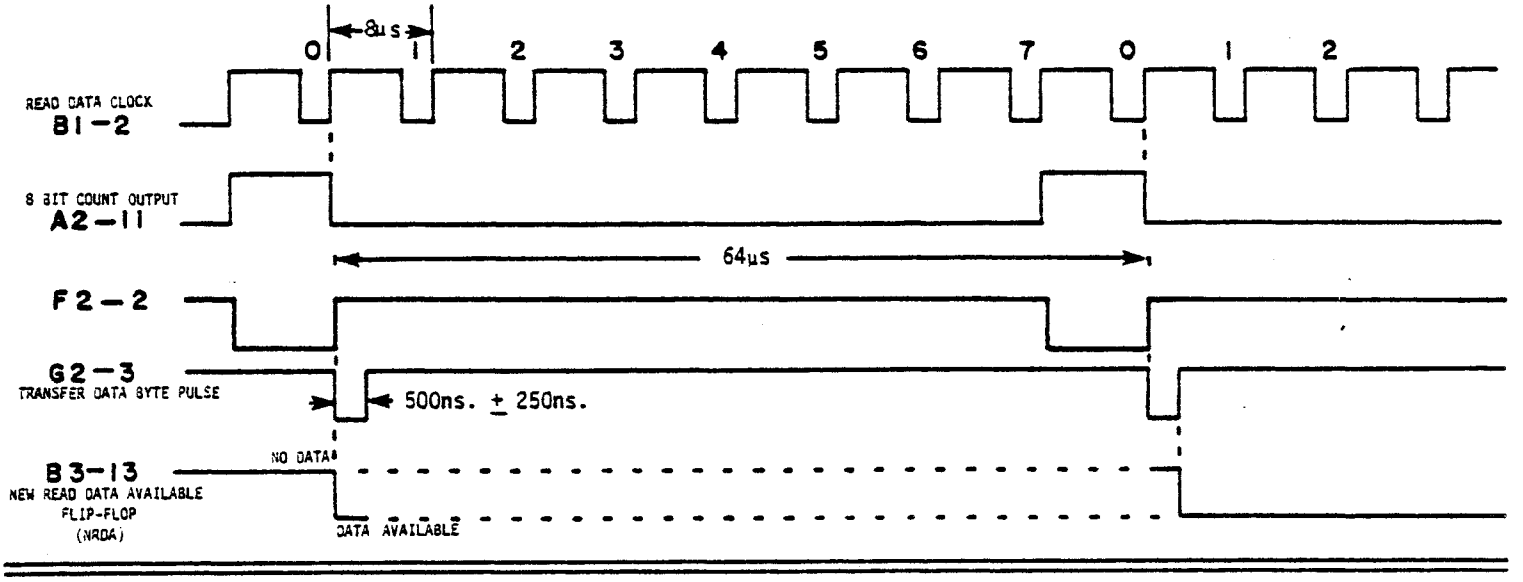


Figure 2-7. Read Timing

At the beginning of every Sector, the Read Clear One Shot, F1 pin 4 (Figure 2-14, Sheet 1, zone B4), goes LOW for 500µs clearing the Divide By Eight Presettable Counter, B1; the Sync Bit Detector Flip-Flop, B2; and the Read Data Serial to Parallel Shift Register, G1. When INPUT READ DATA STROBE goes LOW, the New Read Data Available Flip-Flop, B3, is cleared.

2-10. STATUS CIRCUIT ($\emptyset1\emptyset_8$ - INPUT

When an input is done on Channel $\emptyset1\emptyset_8$, Disk Status information (Figure 2-14, Sheet 2, zone B2) is transferred to the Altair Data Bus. Status signals include HEAD STATUS (HS), MOVE HEAD (MH), INTERRUPT STATUS (INT STATUS), ENTER NEW WRITE DATA (ENWD), NEW READ DATA AVAILABLE (NRDA), and TRACK Ø (TRK Ø). Track Ø is generated by the Disk Drive unit and indicated when the head is on the outermost track. When the INPUT STATUS STROBE is enabled LOW at A3 pin 6 (Figure 2-14, Sheet 1, zone C3), line drivers H3 pins 13 and 11 (Figure 2-14, Sheet 2, zone C2) and H2 pins 5, 11, 9, 7, 3 and 13 (zone B2) are enabled, allowing Status information to the Altair Data Bus.

2-11. DISK ENABLE CIRCUIT ($\emptyset1\emptyset_8$ - OUT)

When the DISK CONTROL LATCH STROBE (Channel $\emptyset1\emptyset_8$ - OUT) is enabled LOW for 500ns. (Figure 3-21, Sheet 1, zone C8) and inverted HIGH at G2 pin 12 (zone C5), the Disk Address Latch, J3, and Disk Enable Flip-Flop, A2 (zone C5), are clocked (refer to Figure 2-8). Data Out Bus lines DØ0-DØ1 transfer the Disk address information through inverters G4 pins 2, 3 and 4 to the Disk Address Latch, J3 pins 2 and 3. As the clock goes HIGH at J3 pins 13 and 4, data is latched into the D_A and D_B inputs, and as the clock returns LOW, data present at the D_A and D_B inputs is transferred to the $\overline{Q}_A$ and $\overline{Q}_B$ outputs. The address information then enables one of four possible Disk Drives through line drivers K3 pins 5 and 7 (zone C2). The Disk Enable Flip-Flop, A2 pin 8 (zone C5), is clocked LOW, providing the DISK ENABLE signal through line driver K3 pin 3 (zone C2) and the DISK ENABLE signal to B4 pin 1 (zone A7). A2 pin 8 also triggers the Disk Enable Timer, B3 pin 1 (zone C4) and the Drive Motor On Delay One Shot, B1 pin 1. The Drive Motor Delay Flip-Flop, B1 pin 4 triggers LOW for 1 second when the Disk Enable Flip-Flop is toggled LOW. E1 pin 8 (zone B4) is enabled HIGH and the Disk Disable Flip-Flop (explained in Paragraph 2-15) is reset. The Drive Motor On Delay Flip-Flop allows the Disk Drive Motor time to stabilize. B3 pin 13 is enabled HIGH for 3µs. 50 to 200ns. after the Disk Drive is enabled, the DISK POWERED line goes LOW at the Disk Reset One Shot, B3 pin 11 (zone C4). This prevents the Disk Reset One Shot from being triggered by the Disk Enable Timer.

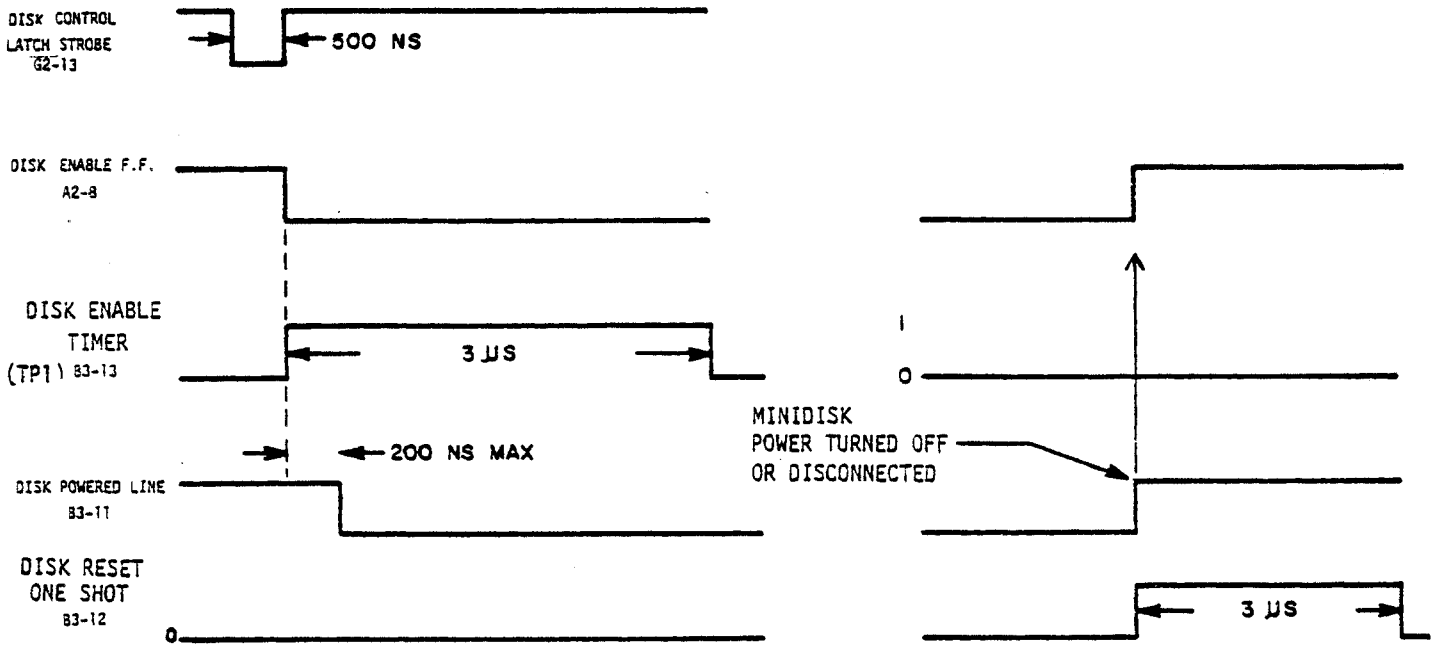


Figure 2-8, Disk Enable Timing With Valid Disk Address (board 2, sheet 1)

If a Disk is not connected, there is no power, the DISK POWER line stays HIGH at B3 pin 11 (zone C4), allowing B3 pin 9 to be triggered. B3 pin 12 is triggered LOW for 3µs , enabling E1 pin 11 HIGH (refer to Figure 4-9). This leaves F3 pin 13 (zone C5) LOW and the Disk Enable Flip-Flop, A2, is cleared. A2 is also cleared when POC (POWER ON CLEAR) is LOW or by the DISK CONTROL LATCH when Data line DØ7 is HIGH. This allows F3 pin 13 LOW, clearing A2 pin 6. When DØ7 (zone C8) is HIGH, it is inverted LOW by H4 pin 8 (zone C7), leaving F3 pin 8 (zone C6) LOW. When the DISK CONTROL LATCH goes LOW, F3 pin 10 is enabled HIGH. This leaves F3 pin 13 LOW, and the Disk Enable Flip-Flop is cleared.

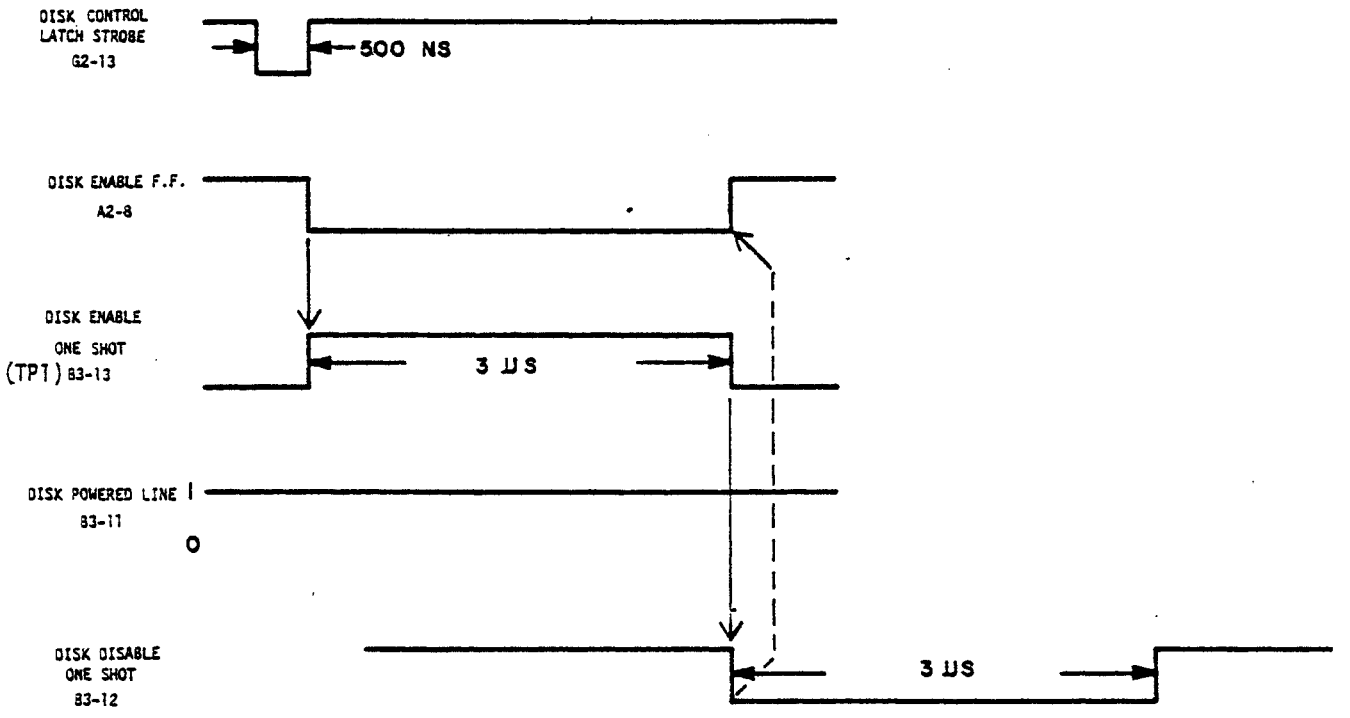


Figure 2-9. Disk Enable Timing With Invalid Disk Selection (board 2, sheet 1)

2-12. WRITE CIRCUIT (012_8 - OUT)

Software detects Sector True status, and the desired Sector is located. An output to Channel $\emptyset11_8$ (CONTROL DISK STROBE), with data line DØ7 inverted LOW, enables J1 pin 10 (Figure 4-15, Sheet 1, zone A7) HIGH. This toggles the Write Enable Flip-Flop, E2 pin 9 (zone A5), HIGH for 12.5ms. The HIGH at E2 pin 9 is present at E3 pin 1 (zone D7) and provides the (WRTEW) Write Enable signal to the Drive. When E2 pin 9 goes LOW, the Counters and Shift Registers H2, A3 and A4 are cleared.

The WRITE DATA ENABLE signal (refer to Figure 4-10) is generated when the Sector Count True One Shot, F4 pin 4 (Figure 4-14, Sheet 1, zone A7), is enabled LOW for 30µs , triggering the Write Clear One Shot, F4 pin 5 (zone A5), HIGH for 1ms. The HIGH at F4 pin 5 is inverted LOW at J3 pin 10 (zone A2) and presented to New Write Data Request Flip-Flop, J4 pin 2 (Figure 4-15, Sheet 1, zone D2). The 1ms. delay inhibits the ENTER NEW WRITE DATA request at the beginning of a Sector. After 1ms , J4 pin 2 goes HIGH. J4 pin 6 is toggled LOW by the next pulse from the Write Byte Counter, A4 (zone D3). J4 pin 6

goes LOW every 64μs. The LOW pulse width of the ENTER NEW WRITE DATA Status pulse depends on software, and each pulse is cleared upon an output to WRT (WRITE) DATA STROBE (Channel $\emptyset 12_8$).

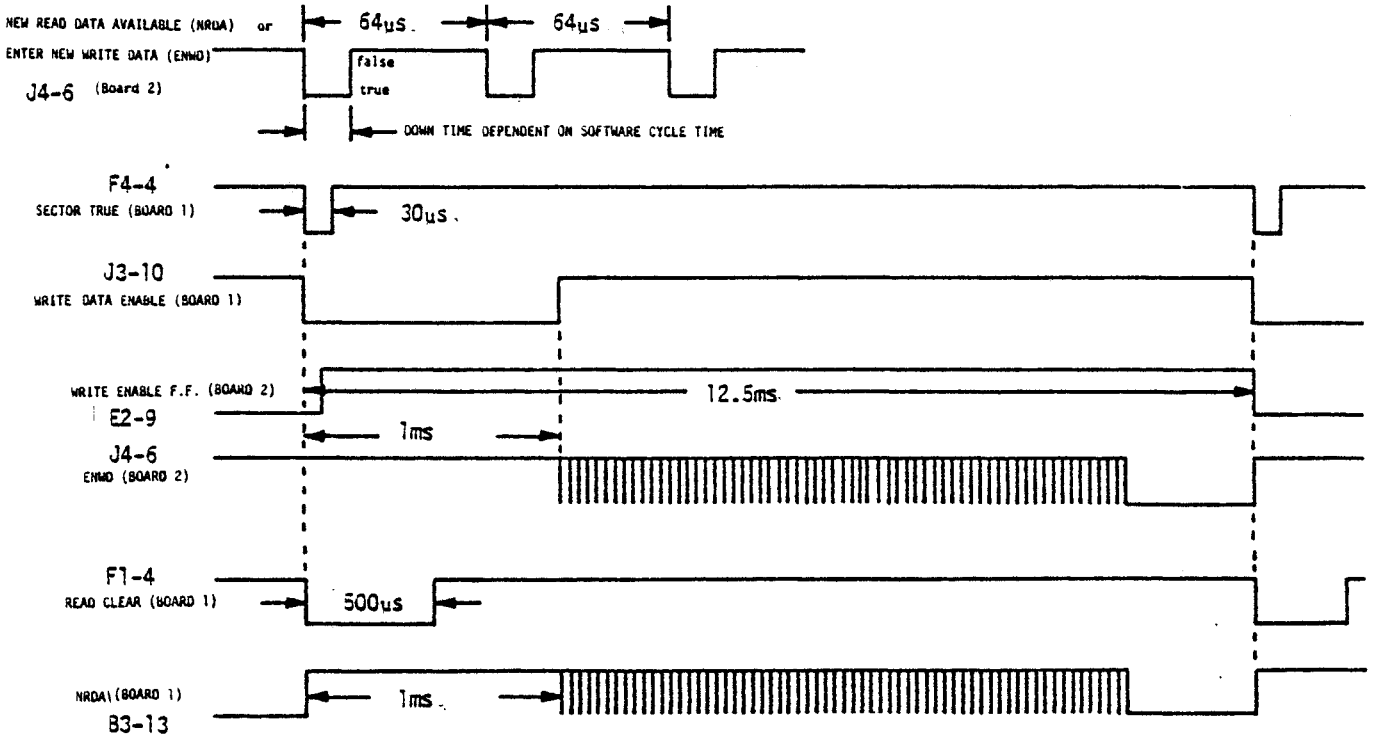


Figure 2-10. Minidisk Read/Write Timing

The Parallel to Serial Write Data Shift Register (zone D6) must not be clocked during the 1ms. delay at J4 pin 2. Clocking is inhibited when CLOCK INHIB (Clock Inhibit), H2 pin 6 (zone D6), is HIGH. Since WRT ENABLE at E3 pin 1 (zone D8) is initially LOW and WRT (Write) DATA STROBE at E3 pin 5 (zone D7) is initially HIGH, E3 pin 3 (zone D7) is HIGH. Logic Ø bits are written to the Disk Drive during the first 1ms. because H2 is not clocked, and output pin 13 which is cleared by a LOW on the WRT ENABLE line before the Write Circuit was enabled, is at logic Ø. When J4 pin 6 (zone D2) is enabled LOW, software detects ENTER NEW WRITE DATA Status True and outputs the first byte to Channel $\emptyset 12_8$,

enabling WRT DATA STROBE LOW. The first D7 bit written, the sync bit, must be logic 1. When WRT DATA STROBE is LOW at E3 pin 5 and E3 pin 1 is HIGH, E3 pin 3 is enabled LOW. CLOCK INHIB is then LOW, allowing H2 to shift data when clocked at pin 7.

In addition to allowing H2 to be clocked, WRT DATA STROBE also strobes data into Write Data Latches H3 and G3 (zone C6). Data present on Altair Data Out Bus, DØ0 through DØ7, is inverted by G4 pins 2, 4, 6, 10 and 12 and H4 pins 8 and 10, and transferred to the Disk Drive Control Signal Decoders (zone B6) and to the D_A through D_D inputs of Write Data Latches, H3 and G3 (zone C6). When H3 and G3 go HIGH at pin 13, data is latched into the D_A through D_D inputs. WRT DATA STROBE (Channel $Ø12_8$ - OUT) goes LOW for 500ns , is inverted HIGH by G2 pin 8 and G2 pin 10, and clocks H3 and G3. Data present at D_A through D_D is transferred to $\overline{Q}_A$ through $\overline{Q}_D$ when the clock at pin 13 goes LOW. Data is then available at PARALLEL DATA IN of Parallel To Serial Write Data Shift Register, H2 (zone D6). The Write Byte Counter, A4 (zone D3), counts eight 1µs. clock pulses from the Write Clock + Data Window Generator, A3 pin 15 (zone D4), to the Parallel To Serial Write Data Shift Register, H2 pin 15 (refer to Figure 3-11). On the eighth count, A4 pin 15 will go HIGH for 8µs. This HIGH is inverted LOW by B4 pin 12 (zone C3) to H2 pin 15 and enables the PARALLEL DATA INPUTS (Ø through 7). On the next H2 pin 7 clock pulse, data present at $\overline{Q}_A$ through $\overline{Q}_D$ of the Write Data Latches is synchronously loaded into the Shift Register.

In addition to clocking the Write Byte Counter, A4 pin 2, the Write Clock + Data Window Generator, when HIGH at A3 pin 15, provides the write clock pulse to F4 pin 12 (zone D2). A_{OUT}, B_{OUT} and C_{OUT} (zone D5) are gated together to provide the Write Data Window at E4 pin 6 (zone D3).

The Write Clock + Data Window Generator, A3, is enabled by the 1MHz Clock pulse (zone D8) at A3 pin 2. The 1MHz clock is derived by dividing the 2MHz Clock by 2 at J4 pin 9 (zone A4). In addition to clocking A3 pin 2, the 1MHz Clock is also present at F3 pin 3 (zone D6). On the eighth 1MHz Clock pulse, occurring every 8µs., A3 pin 15 (RC) is HIGH for 1µs and, after being inverted LOW by B4 pin 6 (zone D4), is present at F3 pin 2. When the 1MHz Clock pulse goes LOW at F3 pin 3, F3 pin 1 is enabled HIGH, clocking H2 pin 7. When H2 pin 15 (SHIFT/$\overline{LD}$) is HIGH, WRITE DATA is shifted serially out on H2 pin 12 (SERIAL DATA OUT). If a logic 1 is being written, the HIGH at H2 pin 13 is inverted by B4 pin 10 (zone D4) and Serial Write Data appears LOW to F4 pin 3 (zone D3). When A_{OUT} and B_{OUT} are HIGH, and C_{OUT} is inverted HIGH by G2 pin 6 (zone D4), E4 pin 6 (zone D3) is enabled LOW. F4 pin 1 (zone D3) is enabled HIGH, insuring F4 pin 13 is LOW (refer to Figure 4-11 and 4-12), and the Disk WRT DATA (Write Data) input is enabled through line driver K3 pin 9 (zone D2). The Write Data Windows (zone D3) are developed halfway between the write clocks which are generated every 8µs.

The Write Clock + Data Window Generator, A3, the Write Byte Counter, A4, and the Parallel To Serial Write Data Shift Register, H2, are cleared when WRT ENABLE (generated at E2 pin 9, zone A5) is LOW.

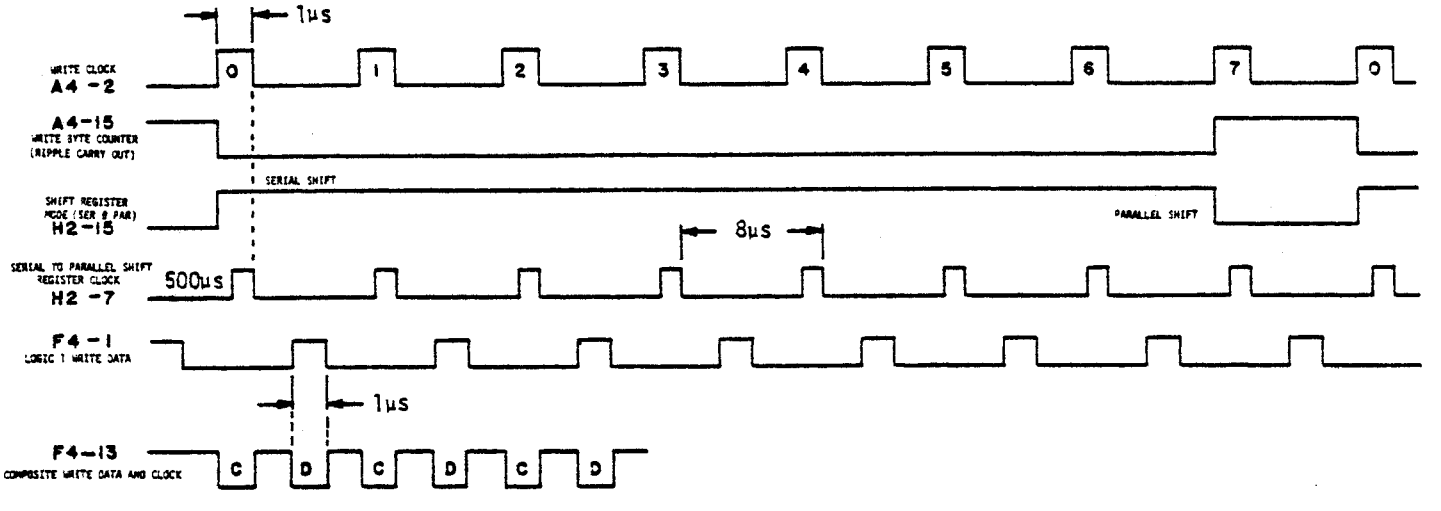


Figure 2-11. Write Circuit Timing

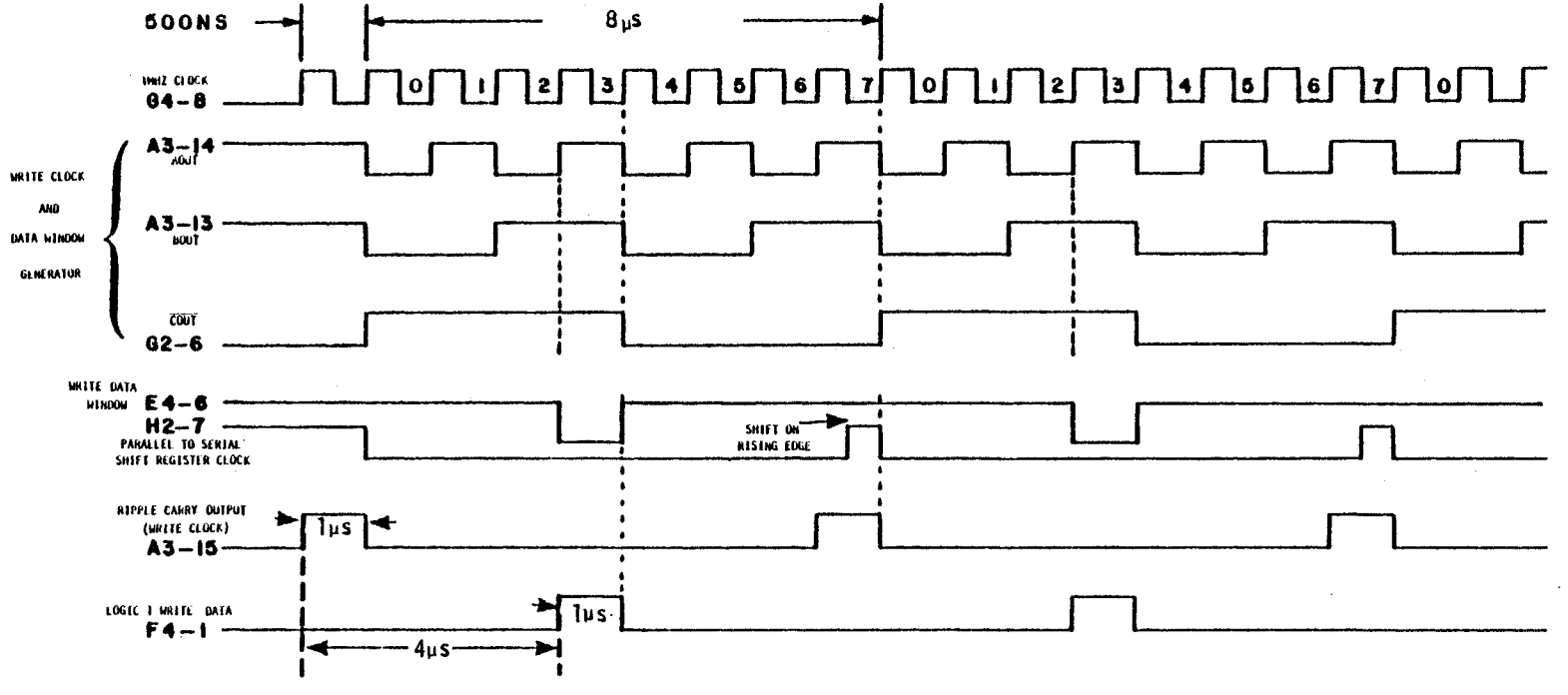


Figure 2-12. Write Timing

2-13. DISK FUNCTION CONTROL CIRCUIT ($Ø11_8$ - OUT)

Channel $Ø11_8$ - OUT controls Disk operations when both Disk Drive and Controller are enabled. Data line DØ0 through DØ7 (Figure 2-15, Sheet 1, zone C8) transfer the control information from the Altair Data Out Bus to the Disk Drive unit. HIGH signals on the Data lines are inverted by G4 and H4 (zone C7) and appear as DØ0 through DØ7 at Control Signal Decoding Gates H1 and J1 (zone B7). Before the decoding gates can be enabled, the CONTROL DISK STROBE ($Ø11_8$ - OUT) line (zone A8) must be enabled LOW (500ns. pulse). Refer to Figure 2-13 for timing diagrams relating to Disk Control functions discussed in Paragraphs 2-14 through 2-19.

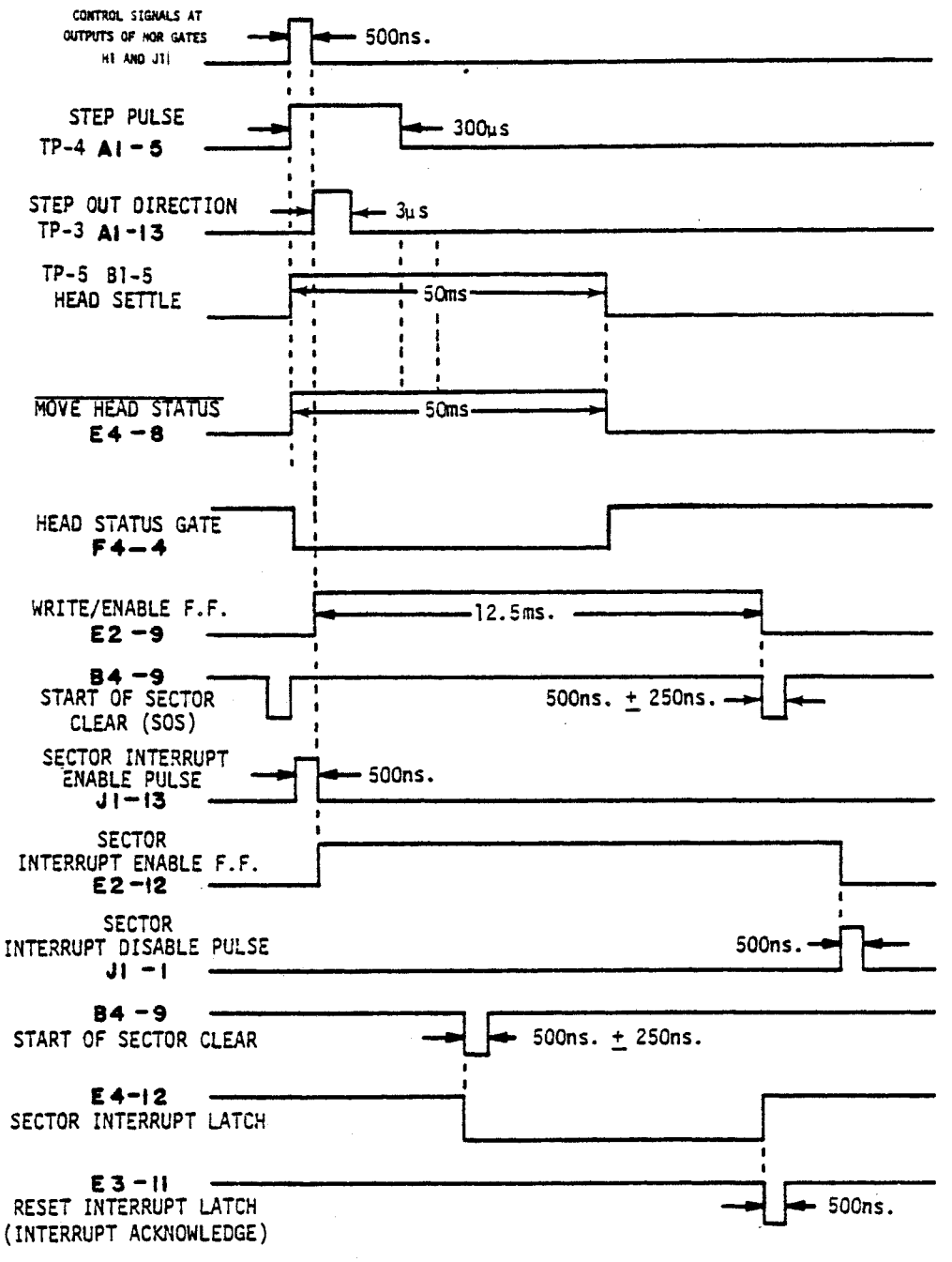


Figure 2-13. Disk Function Control Timing

2-14. Head Stepping

During an output to Channel $\emptyset 11_8$, Control Disk Strobe (zone A8) pulses LOW, causing H1 pin 12 (zone B7) to pulse LOW. If DØ0 is HIGH, it appears LOW at H1 pin 11, causing H1 pin 13 to pulse HIGH. On the trailing edge of this pulse, A2 pin 1 (zone C4) is clocked, causing A2 pin 12 to go HIGH. This HIGH is inverted at J2 pin 5 (zone B2), causing a LOW on the STEP DIRECTION line indicating a STEP IN direction. H1 pin 13 is also connected to F1 pin 2 (zone B6), causing a LOW pulse on F1 pin 1 when either input pulses HIGH. The LOW going pulse at F1 pin 1 triggers the Step Pulse One Shot at A1 pin 9 (zone B5) which gives a .3ms positive pulse at A1 pin 5. This pulse is inverted at J2 pin 3 (zone B2), causing a LOW going Step Pulse. When the STEP DIRECTION line is LOW, the trailing edge of the .3ms Step Pulse causes the Minidisk head to be moved in one track (to higher numbered tracks) towards the center of the Minidiskette.

If DØ1 is HIGH when outputting to Channel $\emptyset 11_8$, LOWs appear at H1 pins 8 and 9 (zone B7), causing a HIGH pulse at H1 pin 10. The trailing edge of this signal triggers A1 pin 1 (zone B4), causing a 3μs. pulse at A1 pin 4 clearing A2 pin 2. With A2 pin 12 LOW, the STEP DIRECTION line goes HIGH, indicating the STEP OUT direction. The HIGH going pulse at H1 pin 10 also causes F1 pin 1 to pulse LOW, resulting in a Step Pulse as described in the preceding paragraph. When the STEP DIRECTION line is HIGH, the trailing edge of the .3ms Step Pulse causes the Minidisk head to move out one track towards the outer edge (lower numbered tracks). Note that if DØ0 and DØ1 are both HIGH during an output to Channel $\emptyset 11_8$, the STEP OUT direction will always be selected due to the clearing action on the Step Direction Flip-Flop, A2.

2-15. Disk Disable Timer

F1 pin 1 is normally HIGH and goes LOW when a step command is received. This enables A1 pin 5 HIGH for 300µs and B1 pin 12 LOW for 50ms (explained in Section 2-16). The pulse at F1 pin 1 is also present at E4 pin 10. After being inverted by J2 pin 3 (zone B1), the HIGH at the Step Pulse One Shot, A1 pin 5, provides the STEP PULSE signal to the Disk Drive. The HIGH at A1 pin 5 is also present at F1 pin 5, enabling F1 pin 4 LOW. This allows E1 pin 8 (zone B4) to go HIGH which resets the Disk Disable Timer, B2, keeping the system enabled. The Disk Disable timer turns the system off after 6.4 seconds if there is no head movement or the Timer is not reset by software. The Timer is clocked every 12.5ms by the START OF SECTOR CLR pulse, occurring at the beginning of each Sector.

When DØ2 is HIGH at bus pin 88 (zone C8) and an output is done to Control Disk Strobe, H1 pin 4 is enabled HIGH, allowing F1 pin 4 LOW. E1 pin 8 is then allowed HIGH and the Disk Disable Timer is reset. This command should be issued before every Read or Write operation to insure the 88-MDS continues to be enabled.

2-16. Move Head Status

If a step command is received, F1 pin 1 goes LOW and B1 pin 9 (zone B3) is triggered LOW, causing B1 pin 12 (zone B3) to go LOW for 40ms. While B1 pin 12 is LOW, E4 pin 8 (zone B2) remains HIGH, indicating that the head is being stepped. The Head Settle One Shot holds E4 pin 8 HIGH, allowing time for the head to settle before the Move Head Status True (LOW) signal is generated. The Move Head signal is also False (HIGH) during the Write mode as E2 pin 8 (zone A5) is enabled LOW, having gate E4 disabled (E4 pin 8 HIGH).

2-17. Head Status

Although the head is loaded when the Drive is enabled, a one second delay is required for the motor speed to stabilize when the Drive is first enabled. B1 pin 1 is triggered by A2 pin 8 (zone C5) going LOW when a Drive is enabled, causing a one second LOW pulse at E1 pin 9. E1 pin 8 (zone B4) goes HIGH and F4 pin 4 is enabled LOW. Inverted at B5 pin 8 (board 1, sheet 2, zone B2) the HIGH (False) Head Status signal is generated. Head Status (HS) also goes False (HIGH) for 50ms. during a step command when E4 pin 8 is held HIGH, enabling F4 pin 4 (zone B4) LOW. When the signal is inverted on board 1, $\overline{\text{Head Status}}$ is False (HIGH). When $\overline{\text{Head Status}}$ is False (HIGH) on board 1, Sector information is inhibited and no reading or writing of data is permitted. When $\overline{\text{Head Status}}$ is LOW, reading or writing of data is allowed.

2-18. Enable Interrupts

When $\overline{\text{DØ4}}$ goes LOW, J1 pin 13 (zone B7) is enabled for 500ns , applying a clock pulse to Interrupt Enable Flip-Flop, E2 (zone B3). E2 pin 12 is enabled HIGH and present at Interrupt Latch, E4. E4 pin 12 (zone A3) is normally HIGH in a Reset condition. E3 pin 11 (zone A3), is normally HIGH and applied to E4 pin 1 when an interrupt is acknowledged by the computer's Central Processing Unit (CPU). When START OF SECTOR CLR (zone A8) goes LOW for 500ns. ($\pm$250ns) at the beginning of each Sector, E4 pin 12 is latched LOW providing the Disk Drive INTERRUPT signal. When PDBIN and SINTA (zone A8) go HIGH for 500ns. and 1.5µs , respectively, E3 pin 11 goes LOW and E4 pin 12 is reset HIGH.

Flip-Flop E2 pin 12 is cleared LOW when J1 pin 1 (zone A6) goes HIGH for 500ns. E1 pin 6 (zone A6) is HIGH and inverted LOW at H4 pin 2 (zone A5), clearing Flip-Flop E2. Software must enable interrupts in the CPU and have an appropriate service routine in memory to enable the INTERRUPT signal.

SECTION 3
PRELIMINARY CHECKOUT

3-1. DISK ENABLE TEST

The following program is used to check the primary functions of the Altair Minidisk System. Since it is a static test, it does not check actual data transfers or the Read/Write circuitry. It is useful to identify the possible areas of malfunction as a first step of trouble-shooting.

Since the Disk Disable Timer will turn the system off 6 seconds after it is enabled, the timer should be disconnected for this test. This is done by removing IC B2 on Minidisk Board #2 (4020), bending pin 10 up and placing B2 back in its socket with no connection to pin 10. After the necessary tests are completed, it is important that B2 pin 10 is returned to its proper connection.

When using this test program, use Drive address Ø and be sure there is a Minidiskette in the Drive.

Single step the following program:

Test #	Address		Instruction
1	000,000	076	MVI A
	1	000	Drive Address Ø
	2	323	Output to:
	3	010	Disk Enable Channel
2	4	333	Input from:
	5	011	Sector Count Channel
3	6	333	Input from:
	7	010	Status Channel

Test #1

Examine address 000,000, and single step five times. The Minidisk Drive should now be enabled with the motor on and the head loaded. Failure to enable the Drive at this point could be the result of defective Disk Board #1 addressing circuitry, the Disk Enable circuitry on Minidisk Board #2, interconnect cable or the Minidisk Drive itself.

Test #2

After enabling the Minidisk Drive in Test 1, single step two more times. The Altair 8800 front panel Data lights should display the Sector Position Register as follows:

DØ - ON all the time

D1 - ON all the time (flashing very fast)

D2 - Flashing very fast

D3 - Flashing fast

D4 - Flashing slowest

D5 - OFF all the time

D6 - ON all the time

D7 - ON all the time

Improper display of lights indicates problems on Disk Board #1 in the Index/Sector circuit. If all the lights stay on, the trouble is either in the Disk Board #1 Addressing circuit or in the Minidisk Drive.

Test #3

With the Minidisk Drive still enabled, single step the program three times. The Minidisk System Status should now appear on the Altair 8800 Data lights as follows:

DØ - ON (ENWD = Indicates Write Circuit is Not Requesting Data)

D1 - OFF (MH = OK To Step The Head)

D2 - OFF (HS = Head Properly Loaded)

D3 - OFF = No Function

D4 - OFF = No Function

D5 - ON if "INTE" On Front Panel Off

D6 - Indicates Track Ø = OFF if at TRK Ø

D7 - ON Flickering (NRDA Indicates Read Circuit is Detecting Data)

If the lights do not appear normal, the circuit associated with the questionable light may be defective. If all lights are on, the trouble is probably in the Address Circuit on Disk Board #1.

3-2. ALTAIR MINIDISK CONTROLLER TIMING TEST POINTS

The Minidisk Controller PC cards are equipped with test points on the key timing circuits. Below are listed the test points, their associated circuit function and the positive pulse width for normal operation. These test points may be observed when running the Disk Read/Write Test Program (see Paragraph 3-4).

MINIDISK BOARD #1

TP-1 (CI A1-13)	Read Clock Mask - 1.6 to 2.4µs. Occurs every 8µs when Drive enabled and not writing. Used to separate Read Clock from Read Data.
TP-2 (IC A1-5)	Read Data Window - 5.9 to 6.3µs. Occurs every 8µs when Drive enabled and not writing. The most critical time constant, nominally 6.1µs. Used to separate Read Clock from Read Data.
TP-3 (IC E1-5)	Index Pulse Window - 8.0 - 11.2ms. Occurs every 12.5ms when Drive is enabled. Used to separate Index pulses from Sector pulses.
TP-4 (IC E1-13)	Sector Pulse Mask - 150 - 600µs. Occurs every 12.5ms when Drive is enabled. Used to separate Index pulses from Sector pulses.
TP-5 (IC F1-13)	Read Clear - 400 - 600µs. Occurs every 12.5ms when Drive is enabled. Used to clear Read Circuit at beginning of Sector.
TP-6 (IC F1-5)	Index Pulse Verification - 8.0 - 11.2ms. Occurs every 200 ms when Drive is enabled. Used to insure proper detection of Index pulse when Drive first enabled.
TP-7 (IC F4-13)	Sector True - 20 - 40 s. Occurs every 12.5ms when Drive is enabled. Used to indicate beginning of Sector.
TP-8 (IC F4-5)	Write Data Enable - 900 - 1200µs. Occurs every 12.5ms when Drive is enabled. Used to keep Write Registers cleared during start of Write operation so that zeros are written during first portion of Sector (preamble).

MINIDISK BOARD #2

TP-1 (ICB3-13)	Disk Enable Timer - 1.5 - 4.5µs. Occurs when Disk is enabled. Used to insure proper enabling of Drive.
TP-2 (IC B3-5)	Disk Reset - 1.5 - 4.5µs. Occurs when Disk is disabled. Used to insure proper reset of Controller.
TP-3 (IC A1-13)	Step Out Direction - 1.5 - 4.5µs. Occurs when step out movement desired. Used to clear Step Direction Flip-Flop

TP-4 (IC A1-5) Step Pulse - 150 - 450µs. Occurs when step in or out command is issued. Used to step Minidisk Drive. A minimum of 45ms between step pulses. Drive stepping occurs on trailing edge of step pulse.

TP-5 (IC B1-5) Head Settle Delay - 45 - 75ms. Occurs when step command is issued. Used to indicate MH and HS status to prevent stepping of Disk head or Read/Write functions after a step command.

TP-6 (IC B1-13) Drive Motor on Delay - .9 - 1.5 sec. Occurs when Drives are selected. Used to prevent Disk operations during the time that the Drive motor speed stabilizes.

3-3. ALTAIR MINIDISK TEST PROGRAMS

The following Altair Disk Test programs check out all the normal functions of the Disk Drive. The programs require a minimum of 1K of memory using no wait states, addressed at Ø. These programs are also available on the DWRT PROM.

A. Disk Read/Write Test Program

Program 3-I writes data on Sector 0 of the track it is positioned on, then reads the data back, stores it in memory and outputs it to an I/O device. It is used for testing all Read/Write functions.

WRITE: The number of write data bytes (maximum of 220_8) is set by the position of the sense switches. Write Data consists of:

1st byte = 377_8 (D7 = 1 - sync bit)
2nd byte = data on sense switch
3rd byte = 2nd - 1
4th byte = 2nd - 2
"n"th byte = 001
last byte = 000

If sense switches are set to 000, program will stop.

READ: The Read Data is stored in memory, starting at address $001,236_8$ and consists of the data written by the Write Program.

OUTPUT: After the Read Program, the data is output to a terminal (Teletype, CRT, etc.). The output program is set to output on Channel 1. To obtain a useful output pattern, change the sense switches until a desirable pattern is printed. The characters printed will consist of all printable ASCII characters in reversed order (as in 987654321 and ZYXWVU . . .). This pattern repeats itself and is easily observed for errors.

Program 5-I. Minidisk Read/Write/Output Test Program

TAG	MNEMONIC	ADDRESS	OCTAL CODE	EXPLANATION
	MVI(A)	000,000	076	
		1	000	Disk drive address
	OUT	2	323	
		3	010	Disk controller enable channel
LDHD	MVI(A)	4	076	
		5	004	Reset Timer Bit
	OUT	6	323	
		7	011	Disk function control channel
WRTLP	IN	10	333	Input # of bytes to be written
		11	377	Sense switch
	MOV(C)←(A)	12	117	Store in "C" reg.
	MVI(D)	13	026	Store in "D" reg.
		14	377	First write byte
	MVI(B)	15	006	Store in "B" reg.
		16	001	"ENWD" status mask
WSECT	IN	17	333	Write sector test
		20	011	Sector position channel
	CPI	21	376	
		22	300	Ø sector
	JNZ	23	302	Jump if not start of Ø sect.
		24	017	to "WSECT"
		25	000	
	MVI(A)	26	076	
		27	200	Write enable bit
		30	323	
		31	011	Disk function control channel
FBYT		32	333	First byte test
		33	010	Disk status channel
	ANA(A)/(B)	34	240	Test for "ENWD" status
	JNZ	35	302	Jump if "ENWD" false (=1)
		36	032	to "FBYT"
		37	000	
	MOV(A)(D)	40	172	Move 377 into accum.
	OUT	41	323	Output first byte
		42	012	Disk data channel
INDAT	IN	43	333	Start of write data sequence
		44	010	Disk status channel
	ANA	45	240	Test for "ENWD" status
	JNZ	46	302	Jump if "ENWD" false (=1)
		47	043	to "WDAT"
		50	000	
	MOV(A)←(C)	51	171	Move "DATA" byte to accum.
	OUT	52	323	
		53	012	Disk data channel
	DCR(C)	54	015	Decrement "DATA" byte
	JNZ	55	302	Jump if data byte = Ø
		56	043	to "WDAT", write another byte
		57	000	
W7T	IN	60	333	Start of zero byte

TAG	MNEMONIC	ADDRESS	OCTAL CODE	EXPLANATION
		61	010	Output sequence
	ANA(A)←(B)	62	240	Test "ENWD" (last byte written)
	JNZ	63	302	Jump if "ENWD" false
		64	060	To WZT
		65	000	
	XRA(A)(A)	66	257	Zeros accumulator
	OUT	67	323	Output zero byte
		70	012	Disk data channel (end of write, start of read)
	LXI	71	041	Load H+L reg. with:
		72	236	Starting addr. to store read data
		73	001	
	MVI(B)	74	006	Store in "B" reg.
		75	200	"NRDA" mask
	NOP	76	000	
	NOP	77	000	
RSECT	IN	100	333	Read sector test
		101	011	Sector position channel
	CPI	102	376	
		103	300	Ø sector
	JNZ	104	302	Jump if not start of Ø sect.
		105	100	to "RSECT"
		106	000	
RDTST	IN	107	333	Start of "NRDA" test
		110	010	Disk status channel
	ANA(A)/(B)	111	240	Test for "NRDA" status
	JNZ	112	302	Jump if "NRDA" false (=1)
		113	107	to "RDTST"
		114	000	
	IN	115	333	Input read data
		116	012	Disk data channel
	MOV(M)←(A)	117	167	Store data in memory (H+L)
	INR(L)	120	054	Increment L reg. (mem addr)
	JNZ	121	302	Jump if L reg. ≠ 0
		122	107	to RDTST
		123	000	
	MOV(A)←(D)	124	172	Move 377 byte to accum.
	OUT	125	323	Disenable disk by output logic 1 on
		126	010	D7 to disk enable chan. (end of read, start of output)
	LXI(H+L)	127	041	Load H+L with:
		130	236	Starting addr of data stored by read program
		131	001	

TAG	MNEMONIC	ADDRESS	OCTAL CODE	EXPLANATION
*INIT	MVI(A)	000,132	076	
		133	003	
	OUT	134	323	
		135	020	Initialize 2SIO Port 20/21
	MVI(A)	136	076	
		137	021	
	OUT	140	323	
		141	020	
OTST	IN	142	333	Test Output Channel for Busy
		143	020	Status Channel
	ANI	144	346	And immediate
		145	002	Mask for bit D1
	JZ	146	312	Jump if D1 = 0 (busy)
		147	142	
		150	000	To "OTST"
	MOV(A)←(M)	151	176	Move data PROM mem to Accum
	OUT	152	323	Output data
		153	021	To I/O port
	INR(L)	154	054	Increment L register
	JNZ	155	302	If L ≠ 0, output another byte, jump
		156	142	
		157	000	To "OTST"
	MVI(A)	160	076	
		161	000	Enable Disk
		162	323	
		163	010	
		164	303	Jump
		** 165	004	
		**000,166	000	To "LDHD"

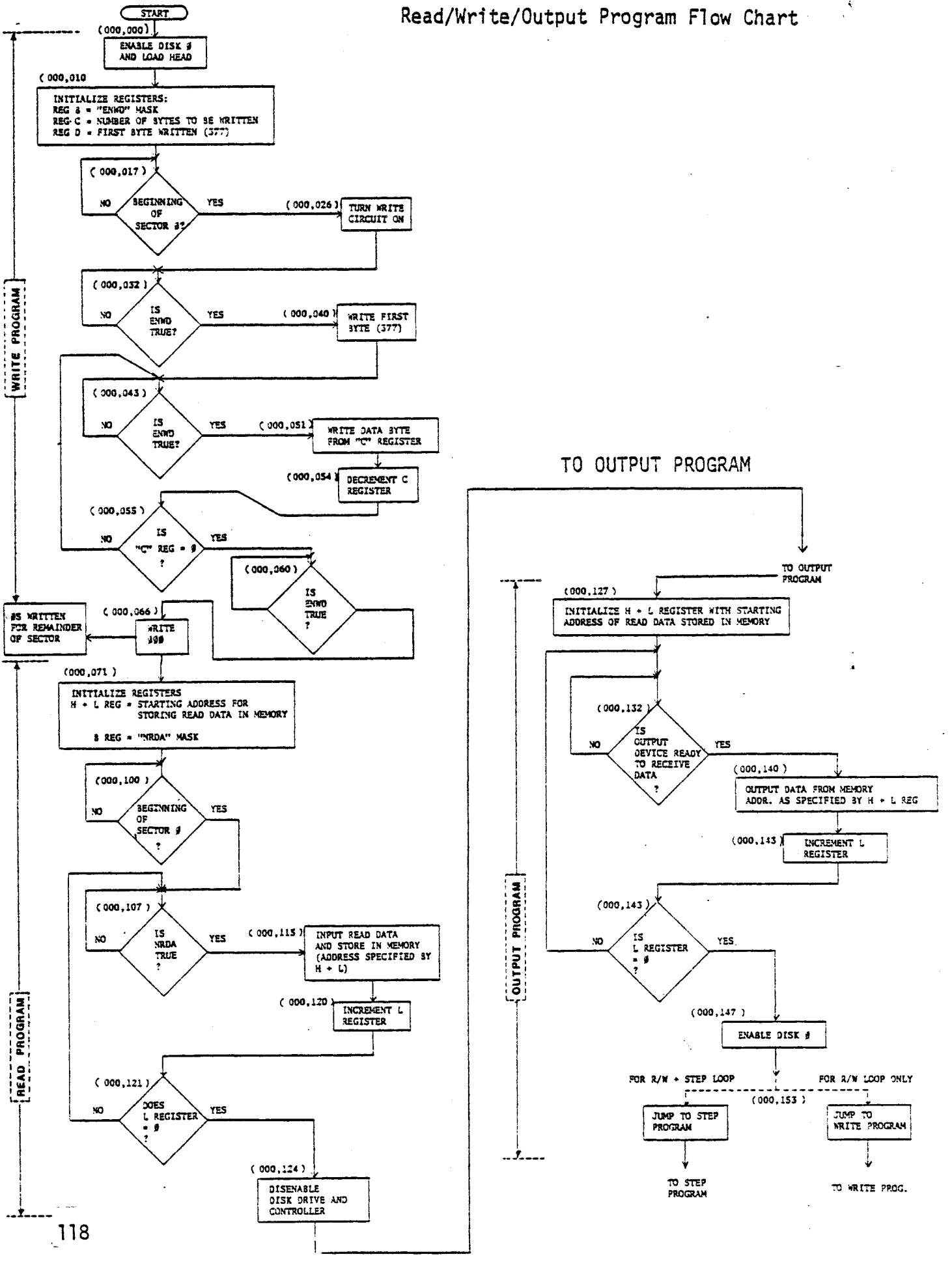
*If using the old SIOA board, replace instructions from 000,132 with the following program.

**For R/W-step loop, change Data at (000,165) to 037; Data at (000,166) to 001.

TAG	MNEMONIC	ADDRESS	OCTAL CODE	EXPLANATION
OTST	IN	132	333	Test output device for busy
		133	000	Status chan. of terminal
	RLC	134	007	Test bit Ø. rotate into carry
	JC	135	332	Jump if carry (bit Ø = 1)
		136	132	to "OTST"
		137	000	
	MOV(A)←(M)	140	176	Move data from mcm(H+L)
	OUT	141	323	Output data
		142	001	Data channel for term
	INR(L)	143	054	Increment L register
	JNZ	144	302	Jump if L reg ≠ 0, output another byte
		145	132	to "OTST"
		146	000	
	MVI(A)	147	076	
		150	000	
	OUT	151	323	Enable disk
		152	010	
	JMP	153	303	
NOTE		†154	004	To "LDHD"
		†155	000	
		156		
		157		

†For R/W-step loop, change Data at 000,154 to 037; Data at 000,155 to 001.

Read/Write/Output Program Flow Chart



248067A

B. Stepping Program

This program steps the Disk head out 34 times to TRACK Ø and then in 34 times to track 34, continuously repeating with the computer in the Run mode. This program is useful for testing the Disk Enable, MH status, TRACK Ø status, and stepping functions of the Disk. To loop with the Read/Write Program, see next section.

Drive Address

For Stepping Program, Disk Drive address of 000 is used. To change Disk Drive tested, the address is contained in location 001,001. For the Read/Write Test, the Drive address is in location 000,001 and 000,150 .

C. Looping With Stepping Program

To check the Read/Write and step functions simultaneously, the two programs may be run together by changing the following:

1) Data in locations 000,154 and 000,155 to 037,001 as indicated
2) Data in location 001,034 to 303 as indicated

Begin the program at 001,000, the start of the Stepping Program. The Disk head will step out to Track 0.

The head will then load and a Write/Read will occur. The head will then unload and output will take place. After output, the head will step in once, starting the Write/Read sequence again. After this repeats 34 times, the head is stepped out to TRACK Ø, and it begins again.**

NOTE**: 1) For Read/Write program, Disk Drive address of 000 is used. To change Disk Drive tested, the address is contained in location 000,001 and 000,150.
2) Output device addresses are in locations 000,133 status and 000,141 data.

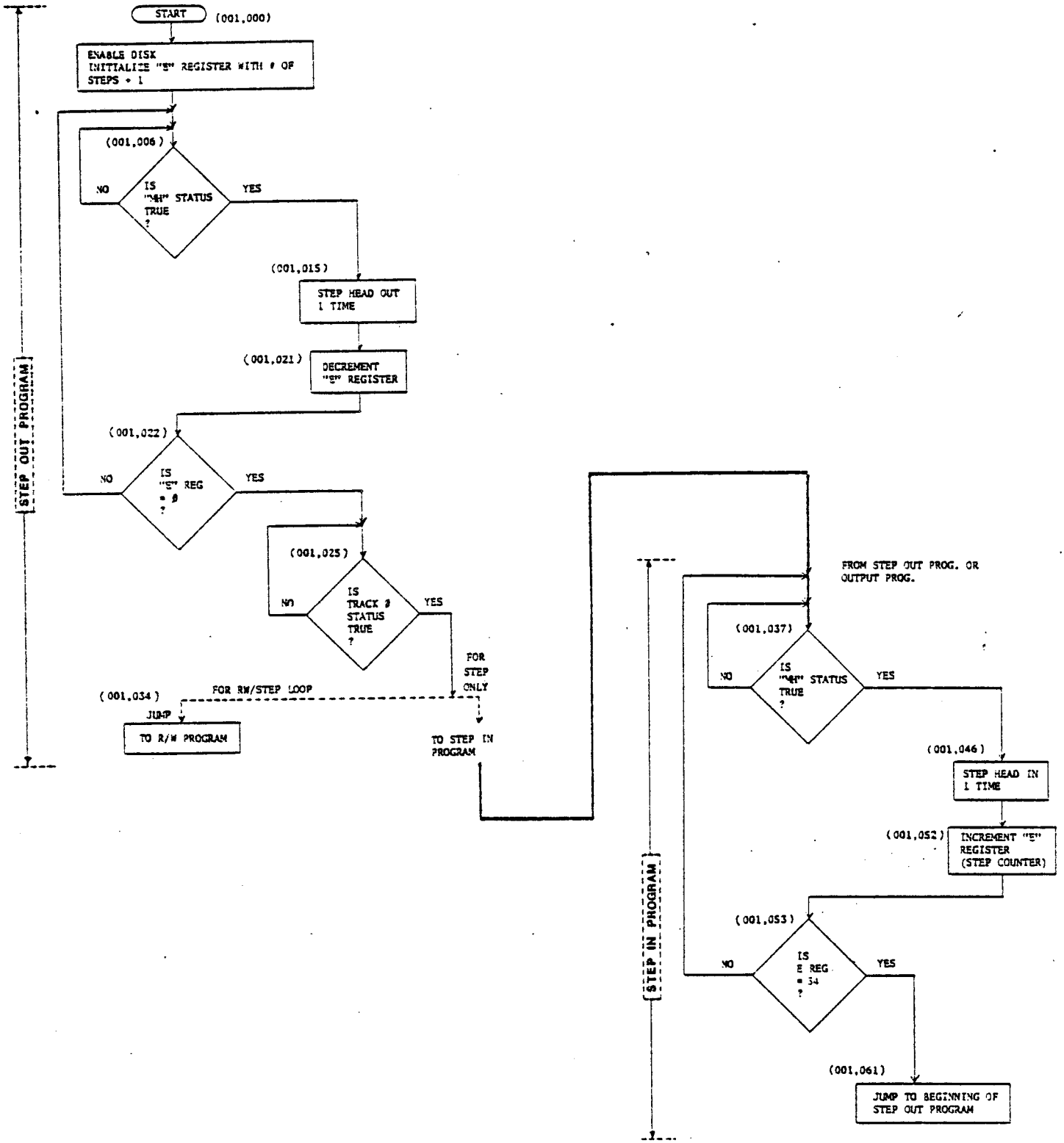
Program 3-II. Minidisk Stepping Program

TAG	MNEMONIC	ADDRESS	OCTAL CODE	EXPLANATION
STEP	MVI(A)	001,000	076	
		1	000	Disk drive addr Ø
	OUT	2	323	Output (data-ØØØ) to
		3	010	Disk CTRL enable channel
NOS	MVI(E)	4	036	Initialize E register
		5	043	=35 (number of steps + 1)
SOUT	IN	6	333	Test "MH" status bit (move head)
		7	010	Disk status channel
	ANI	10	346	Test
		11	002	D1 mask
	JNZ	12	302	Jump if "MH" false (D1=1)
		13	006	To "SOUT"
		14	001	
	MVI(A)	15	076	
		16	002	Bit D1=1 (step out)
	OUT	17	323	Output (data 002) to
		20	011	Disk function control channel
	DCR(E)	21	035	Decrement step counter (E. reg.)
	JNZ	22	302	Jump if E reg ≠ 0
		23	006	to "SOUT"
		24	001	
TZ	IN	25	333	Test for track Ø status
		26	010	Disk status channel
	ANI	27	346	Test
		30	100	D6 mask
	JNZ	31	302	Jump if track Ø false (D6=1)
		32	025	to "TZ"
		33	001	
LOOP	NOP	*34	000	
	NOP	35	000	
	NOP	36	000	
SIN	IN	37	333	Test "MH" status bit (move head)
		40	010	Disk status channel
	ANI	41	346	Test
		42	002	D1 mask
	JNZ	43	302	Jump if "MH" false (D1=1)
		44	037	to "SIN"
		45	001	
	MVI(A)	46	076	
		47	001	Bit DØ = 1
	OUT	50	323	Output (Data 001) to
		51	011	Disk function control channel

TAG	MNEMONIC	ADDRESS	OCTAL CODE	EXPLANATION
	INR(E)	52	034	Add 1 to "E" register
	MVI(A)	53	076	
		54	042	34 steps
	CMP(A)/(E)	55	273	Compare "E" reg. to 34
	JNZ	56	302	Jump if "E" reg. ≠ 34
		57	034	To "Loop"
		60	001	to "Loop"
	JMP	61	303	Jump if "E" reg. = 34
		62	004	to "NOS"
		63	001	
		64		
		65		
		66		
		67		

*--Change to 303 for Step + R/W loop

MINIDISK STEPPING PROGRAM FLOWCHART



APPENDICES

APPENDIX A

ALTAIR 8800b BUS ASSIGNMENTS

The Altair 8800b system bus has 100 lines. These are arranged 50 on each side of the plug-in boards. The following general rules apply to the Altair 8800b bus.

SYMBOLS a "P" prefix denotes a processor command/control signal. "S" denotes a processor status signal.

LOADING All inputs to a card are loaded with a maximum of one TTL low power load except for the Turnkey Module.

LEVEL All bus signals except those for the power supply are TTL compatible. Signals whose names are barred (DO DSBL, for example) are active low (0 volts). All others are active high (+5 volts).

In the listing below, those signal names accompanied by * are ineffective or not used in the Altair 8800b Turnkey computer.

Number	Symbol	Name	Function
1	+8V	+8 volts	Unregulated input to 5 volt regulators
2	+18V	+18 volts	Positive unregulated voltage
3	XRDY	External Ready	For special applications: pulling this line low causes the processor to enter a wait state and allows the status of the normal ready line (PRDY) to be examined.
4	VI 0	Vectored Interrupt	Line 0
5	VI 1	Vectored Interrupt	Line 1
6	VI 2	Vectored Interrupt	Line 2
7	VI 3	Vectored Interrupt	Line 3
8	VI 4	Vectored Interrupt	Line 4
9	VI 5	Vectored Interrupt	Line 5
10	VI 6	Vectored Interrupt	Line 6
11	VI 7	Vectored Interrupt	Line 7
12	XRDY2	Extra Ready line	For special applications.
13 to 17		To be assigned	

18	$\overline{\text{STA DSB}}$	$\overline{\text{STATUS DISABLE}}$	Puts buffers for the 8 status lines in their high-impetance tri-state. In this state, no information can be transferred.
19	C/C DSB	$\overline{\text{COMMAND/CONTROL DISABLE}}$	Puts the buffers for the 6 command/ control lines in their high-impedance tri-state.
*20	UNPROT	UNPROTECT	Input to the memory protect flip-flop.
*21	SS	SINGLE STEP	Indicates that the computer is in the process of performing a single step.
22	$\overline{\text{ADD DSB}}$	$\overline{\text{ADDRESS DISABLE}}$	Puts the buffers for the 16 address lines in their high-impedance tri-state.
23	$\overline{\text{DO DSBL}}$	$\overline{\text{DATA OUT DISABLE}}$	Puts the buffers for the 8 data out lines in their high-impedance tri-state.
24	Ø2	Phase 2 clock	
25	Ø1	Phase 1 clock	
26	PHLDA	Hold Acknowledge	Processor output signal which appears in response to the HOLD signal indicates that the data and address buffers will go to the high-impedance tri-state.
27	PWAIT	WAIT	Processor output indicates that the processor is in the WAIT state.
28	PINTE	Interrupt Enable	Indicates interrupts are enabled; displays contents of the CPU interrupt flip-flop. This flip-flop may be set or reset by the EI or DI instructions. When reset, it prevents the CPU from acknowledging interrupt requests.
29	A 5	Address Line 5	
3Ø	A 4	Address Line 4	
31	A3	Address Line 3	
32	A 15	Address Line 15	

33	A 12	Address Line 12	
34	A 9	Address Line 9	
35	DO 1	Data Out Line 1	
36	DO Ø	Data Out Line Ø	
37	A 1Ø	Address Line 1Ø	
38	DO 4	Data Out Line 4	
39	DO 4	Data Out Line 5	
4Ø	DO 6	Data Out Line 6	
41	DI 2	Data In Line 2	
42	DI 3	Data In Line 3	
43	DI 7	Data In Line 7	
44	SM1	M1	Status output that indicates that the processor is in the fetch cycle for the first byte of an instruction.
45	SOUT	OUT	Indicates that the address bus contains the address of an output device and the data bus will contain the output data when PWR is active.
46	SINP	INP	Indicates that the address bus contains the address of an input device
47	SMEMR	MEMR	Indicates that the data bus will carry memory read data.
48	SHLTA	HLTA	Acknowledges a HALT instruction.
49	$\overline{\text{CLOCK}}$	$\overline{\text{Clock}}$	Inverted output of the 2MHz oscillator that drives the clock.
5Ø	GND	Ground	
51	+8V	+8 volts	
52	-18V	-18 volts	
*53	$\overline{\text{SSW DSB}}$	$\overline{\text{SENSE SWITCH DISABLE}}$	Disables the data input buffers so that the inputs from the sense switches may be strobed onto the bidirectional data bus at the processor.
54	$\overline{\text{EXT CLR}}$	$\overline{\text{EXTERNAL CLEAR}}$	Clear signal for I/O devices.
55	RTC	Real Time Clock	
56	$\overline{\text{STSTB}}$	$\overline{\text{STATUS STROBE}}$	See section 2-2.

*57	DIG1	DATA INPUT GATA #1	Front panel control line.
*58	FRDY	Front Panel READY	
59 to 67		To be assigned	
68	MWRT	MEMORY WRITE	Indicates that the current data on the Data-Out bus is to be written into the memory location currently on the address bus.
69	$\overline{PS}$	$\overline{PROTECT\ STATUS}$	Indicates the status of the memory protect flip-flop on the memory board currently being addressed.
*70	PROT	PROTECT	Input to the memory protect flip-flop on memory board currently being addressed.
*71	RUN	RUN	Indicates that the RUN/STOP flip-flop is reset.
72	PRDY	READY	Input that controls the run state of the processor. If the line is pulled low the processor will enter a WAIT state until it is released.
73	$\overline{PINT}$	$\overline{INTERRUPT\ REQUEST}$	The processor recognizes a request on this line at the end of the current instruction or while halted. If the processor is in the HOLD state or the Interrupt Enable flip-flop is reset it will not honor the request.
74	$\overline{PHOLD}$	$\overline{HOLD}$	Requests the processor to enter the HOLD state. This allows an external device to gain control of the bus as soon as the processor has completed its current machine cycle.
75	$\overline{PRESET}$	$\overline{RESET}$	While activated, the contents of the program counter are cleared and the instruction register is set to 0.

2. ASSEMBLY CODE TO READ AND WRITE A SECTOR

Program 2-II is provided to help users write assembly language subroutines to read and write data on the Minidisk. It is assumed that the Disk being used has already been enabled and positioned to the correct track.

Program 2-II. Assembly Code To Read And Write A Sector

```
; CALL WITH NUMBER OF DATA BYTES TO WRITE IN [A]
; AND POINTER TO DATA BUFFER IN [H,L]
; ALL REGS DESTROYED.
DSKO:  MOV    C,A              ; SAVE # OF BYTES IN C
       MVI    A,136            ; CALCULATE NUMBER OF ZEROS TO WRITE
       SUB    C                ; SUBTRACT THE NUMBER OF DATA BYTES
       MOV    B,A              ; NUMBER OF ZEROS+1
       CALL   SECGET           ; LATENCY
       MVI    A,128            ; ENABLE WRITE WITHOUT SPECIAL CURRENT
       OUT    9
;
; CALL WITH [B]=NUMBER OF ZEROS [C]=NUMBER OF DATA BYTES
; AND [H,L] POINTING AT OUTPUT DATA
;
OHLDSK: MVI   D,1              ; SETUP A MASK (READY TO WRITE)
        MVI   A,128            ; HIGH BIT (D7) ALWAYS ON IN FIRST BYTE
        ORA   M                ; OR ON DATA BYTE
        MOV   E,A              ; SAVE FOR LATER
        INX   H                ; INCREMENT BUFFER POINTER
NOTYTD: IN    8                ; GET WRITE DATA READY STATUS
        ANA   D                ; TEST STATUS BIT
        JNZ   NOTYTD           ; NOT READY TO WRITE, WAIT
        ADD   E                ; ADD BYTE WE WANT TO SEND TO ZERO
        OUT   1Ø               : SEND THE BYTE
```

```
        MOV   E,M               ; GET NEXT DATA BYTE
        INX   H                 ; MOVE BUFFER POINTER AHEAD AGAIN
        DCR   C                 ; DECREMENT COUNT OF CHARS TO SEND
        JNZ   NOTYTD            ; STILL MORE CHARS, DO THEM.
ZRLOP:  IN    8                 ; GET READY TO WRITE
        ANA   D                 ; IS IT READY
        JNZ   ZRLOP             ; IF NOT, LOOP
        OUT   1Ø                ; KEEP SENDING FINAL BYTE
        DCR   B                 ; DECREMENT COUNT OF BYTES TO SEND
        JNZ   ZRLOP             ; KEEP WAITING
        EI                      ; RE-ENABLE INTERRUPTS
        MVI   A,8               ; UNLOAD HEAD
        OUT   9                 ; SEND COMMAND
        RET                     ; DONE
; DISK INPUT ROUTINE.  ENTER WITH POINTER
; OF 137 BYTE BUFFER IN [H,L].  ALL REGS DESTROYED.
DSKI:   CALL  SECGET            ; POINT TO RIGHT SECTOR
        MVI   C,137             ; GET # OF CHARS TO READ
READOK: IN    8                 ; GET DISK STATUS
        ORA   A                 ; READY TO READ BYTE
        JM    READOK
        IN    1Ø                ; READ THE STUFF
        MOV   M,A               ; SAVE IN BUFFER
        INX   H                 ; BUMP DESTINATION POINTER
        DCR   C                 ; LESS CHARS
        JNZ   READOK            ; IF CHARS STILL LEFT, LOOP BACK
```

```
RETDO:  EI                      ; RE-ENABLE INTERRUPTS
        MVI   A,8               ; UNLOAD HEAD
        OUT   9                 ; SEND COMMAND
        RET
SECGET: DI                      ; DISABLE INTERRUPTS
SECLP2: IN    9                 ; GET SECTOR INFO
        RAR                     ; FIX UP SECTOR #
        JC    SECLP2            ; IF NOT, KEEP WAITING
        ANI   15                ; GET SECTOR #
        CMP   E                 ; IS IT THE ONE WE WANTED
        JNZ   SECLP2            ; TRY TO FIND IT
        RET
```

3 MACHINE LANGUAGE OPERATION

Controller I/O Requirements

To communicate with the 88-MDS Controller at the machine language level, the following I/O information is provided. The Minidisk Controller uses three I/O Channels in the Altair computer. Three 8-bit Channels go into the Controller for controlling and writing of data, and three 8-bit Channels for reading the Controller Status, the Sector Count (rotational position of the Minidiskette) and the Read Data. The following is a listing of the Channels and a description of their functions.

A. I/O Address for the Minidisk Controller

Octal Address	Mode	Description
ØlØ	Output from CPU	Enables one of four Drives
ØlØ	Input to CPU	Indicates status of Drives and Controller
Ø11	Output from CPU	Controls Drive operation
Ø11	Input to CPU	Indicates Sector position of Diskette
Ø12	Output from CPU	Write Data
Ø12	Input to CPU	Read Data

B. Definitions of I/O Functions as listed above.

1) Output from CPU to Minidisk Controller address 010:

Bit	Function
DØ D1	Enables one of four Minidisk Drives. The Read/Write Head is loaded when the Drive is enabled.
D2-D6	Not used
D7	Set to zero if enabling Drives. When set to 1, Minidisk system is turned off.

NOTES

a) When changing from one Drive address to another, turn the system off (output a 377 to Channel Ø1Ø), and then enable the desired Drive

b) Never issue a Head Step command prior to changing Drive addresses or turning off a Drive. If you must step the head, check the MH status bit for a logic Ø before changing or turning off the Drive.

c) If the Drive selected is not connected or its power is off, the Controller will automatically turn off.

d) Drive addresses are selected as follows:

Drive Address	DØ	D1
0	0	0
1	1	0
2	0	1
3	1	1

2) An input to CPU from Minidisk Controller Address Ø1Ø gives the Disk System status when a Drive is enabled.
When a bit is True, it is a logic Ø, when False, the bit is a logic 1. Also, all status bits are logic 1 when there is not a Minidiskette in the Drive. The status bits are described as follows:

DØ = $\overline{\text{ENWD}}$ - Enter New Write Data when True, requests that a byte of data be output to the Write Data Channel (Ø12). Occurs during the Write mode every 64μs. $\overline{\text{ENWD}}$ is reset upon receipt of the output data byte.

D1 = $\overline{\text{MH}}$ - Move Head when True, indicates that head stepping is allowed. Goes False for 50ms. after the step command, indicating the head may not be stepped. Also False during Write mode.

D2 = $\overline{HS}$ - Head Status when True, indicates the head is properly loaded and motor speed is stable. Goes True one second after Disk Enable, goes False for 50ms following a command. When False, it prevents the Sector information from being read. This bit is not normally used since Read/Write software tests the Sector Channel just before Reading or Writing. Note that the head is always loaded when the Drive is enabled.

D3 - Not used, always = 0 when Drive is enabled.

D4 - Not used, always = 0 when Drive is enabled.

D5 - $\overline{INTE}$, reflects the Interrupt Enable status of the CPU. True when equal to 0, indicating CPU interrupts are enabled.

D6 - $\overline{TRACK\ Ø}$, when True, indicates that the Drive R/W head is positioned at the outermost track. This status bit should be used for zeroing the software track counter.

D7 - $\overline{NRDA}$, New Read Data Available when True indicates the Read Circuit has a byte of data ready to be input from the Read Data Channel (Ø12). $\overline{NRDA}$ occurs every 64µs. when reading data and is reset each time a byte of Read Data is input from Channel Ø12.

3) An output from the CPU to Minidisk Controller Address Ø11 controls the Minidisk Drive functions.
A logic 1 represents a True signal and controls the Drive functions as follows:

DØ = STEP IN - steps the Drive R/W head in one position to a higher numbered track. The $\overline{MH}$ status should be checked before issuing a step command. STEP IN also resets the 6.4 second Disk Disable Timer and causes $\overline{MH}$ and Sector information to go False for 50ms. Software is responsible for keeping the track position.

D1 = STEP OUT - Steps the Drive R/W head out one position to a lower numbered track. The MH status should be checked before issuing a step command. STEP OUT also resets the 6.4 second Disk Disable Timer and causes $\overline{MH}$ and Sector information to go False for 50ms. Software is responsible for keeping the track position.

D2 = TIMER RESET - Resets the 6.4 second Disk Disable Timer. This command should be issued before every Read or Write operation to insure that the 88-MDS continues to be enabled.

D3 = Not used.

D4 = INTERRUPT ENABLE - Enables interrupts to occur at the beginning of each Sector. Stays enabled until turned off by Interrupt Disable or the Controller turned off (see section 3-9 for more information).

D5 = INTERRUPT DISABLE - Disables the Controllers interrupt circuit. Interrupts are also disabled when the Controller is turned off.

D6 = Not used.

D7 = WRITE ENABLE - turns the Controller and Drive Write Circuits on. WRITE ENABLE is reset at the end of each Sector. The WRITE ENABLE sequence should be performed as follows:

a. Minidisk Drive selected with head positioned at desired track.
b. Desired Sector is searched for (see next section, part d, for Sector information).
c. Desired Sector is found and WRITE ENABLE command is issued.
d. Zeros are automatically written for the first 1ms of the Sector.
e. 1ms after beginning of Sector, $\overline{ENWD}$ goes True, requesting first byte of Write Data.

f. Most significant bit (D7) of first byte written must be a logic 1 (sync bit). The sync bit is used for Read synchronization. The MSB (D7) is written first. The first byte is referred to as the sync byte.

g. $\overline{\text{ENWD}}$ goes True every 64µs and is reset after a Write Data byte is output to Channel Ø12.

h. The maximum number of bytes that are written is 137, including the sync byte.

i. The last or 138th byte written must be all zeros (000). This pattern will be written to the end of the Sector. $\overline{\text{ENWD}}$ may be ignored from this point on.

j. At the end of the Sector the Write Circuit automatically turns off.

The WRITE ENABLE sequence is now completed. For more information on the software required for reading and writing data, see the Read/Write Test program in section 5-4 (Program 5-I).

4) Sector Position

An Input to the CPU from Minidisk Controller address Ø11 gives the Sector position of the Minidiskette in the selected Minidisk Drive.

Sector position is determined by the rotational position of the Minidiskette. The 88-MDS uses a 16 Sector Minidiskette which has 16 Sector holes and one Index hole. These holes are sensed optically and cause pulses to be sent to the Minidisk Controller. The Controller has a counter that is cleared when the Index hole is detected and then counts the Sectors 0 through 15. Reading and writing of data must start at the beginning of the Sector to insure there is no loss of data. To be certain the Read/Write operations start at the beginning of a Sector, the first Sector position bit goes True only during the first 30µs of a Sector. The next four Sector position bits give the actual Sector count. Table 3-B describes the Sector position bits.

DØ = $\overline{ST}$ - Sector True = Ø when True. It is True during the first 30µs of a Sector. When reading or writing data, this is the only time the Sector position may be checked against the desired Sector position.

The following bits reflect the actual Sector count:

Table 3-B. Sector Position Bits

	Sector Count															
	0	1	2	3	4	.	.	.	.	13	14	15				
D1	0	1	0	1	0					1	0	1				
D2	0	0	1	1	0					0	1	1				
D3	0	0	0	0	1					1	1	1				
D4	0	0	0	0	0					1	1	1				
D5 = Always Ø																
D6 = Not used = 1																
D7 = Not used = 1																

NOTE

The Sector position channel will be disabled (all "1"s) for 1 second after the Drive is enabled, and 50 ms after a step command is issued.

When reading a Sector, the Read Circuit is disabled during the first 500µs to insure valid detection of the sync byte. When writing a Sector, the Write Circuit should be enabled as near to the Sector True detection as possible. When enabled, the Write Circuit will automatically write zeros for the first 1ms of the Sector.

5) Write Data

An output from the CPU to Minidisk Controller address Ø12 writes data to the Controller Write Circuit.

Write Data should be output to the Controller only after detection of the $\overline{ENWD}$ status bit going True. $\overline{ENWD}$ is reset upon the Controllers receipt of the output data byte.

Write Data is written on the Minidiskette most significant bit first in MFM format.

6) Read Data

An input to the CPU from Minidisk Controller Address Ø12 reads data from the Controller Read Circuit.

When the Minidisk Drive is enabled, the Controller is normally in the Read mode unless the Write Circuit is enabled. Data bytes may be read upon detection of the $\overline{\text{NRDA}}$ status bit going True. $\overline{\text{NRDA}}$ is reset when the byte of data is read on Channel Ø12.

Read Data is read from the Minidisk Drive most significant bit first in MFM format.

4. USING INTERRUPTS ON THE ALTAIR MINIDISK SYSTEM

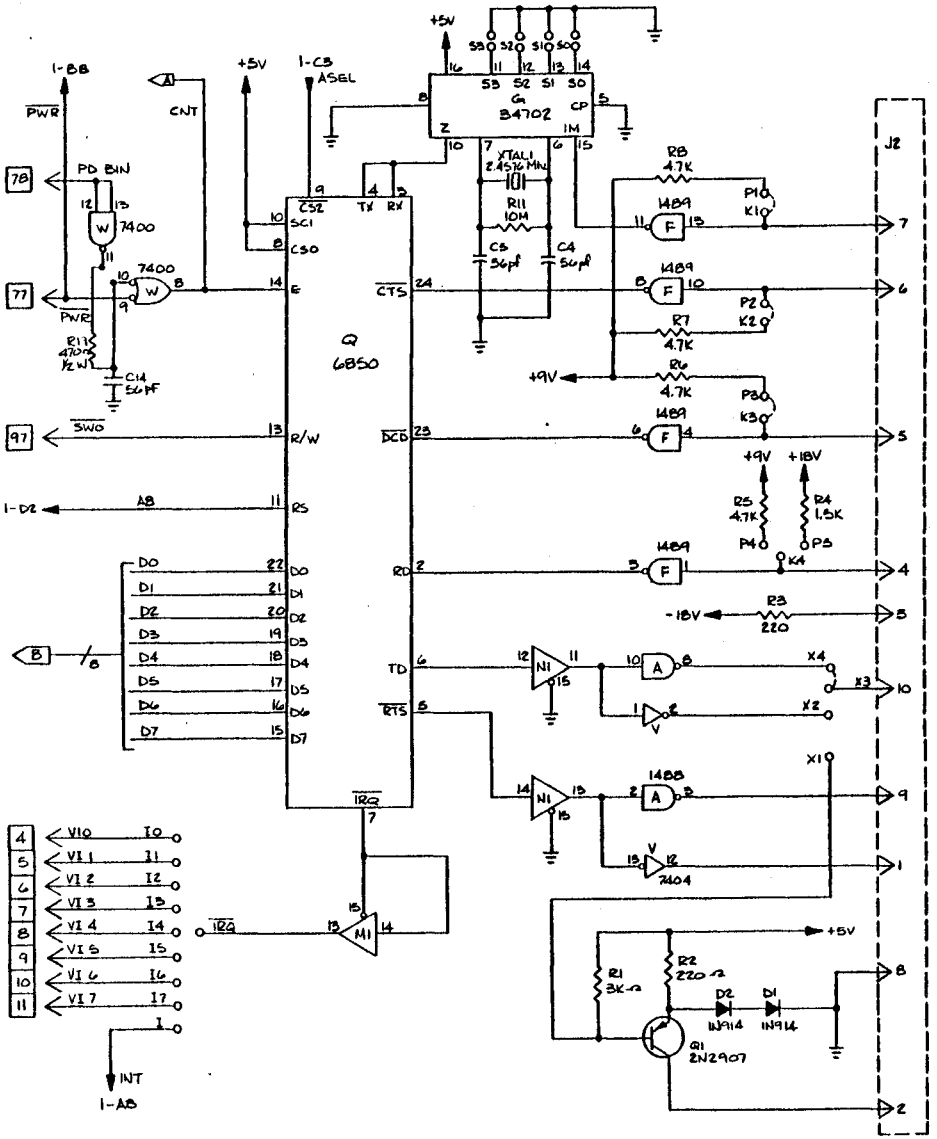
Although the Interrupt Circuit of the Minidisk Controller is an extremely useful feature, not many users take advantage of it since it is not utilized in Altair Minidisk BASIC. The primary functions of the interrupt procedures are to save CPU time in systems that are supporting Minidisks and other operations simultaneously. Minidisk interrupts are caused by detection of a Sector pulse when interrupts are enabled.

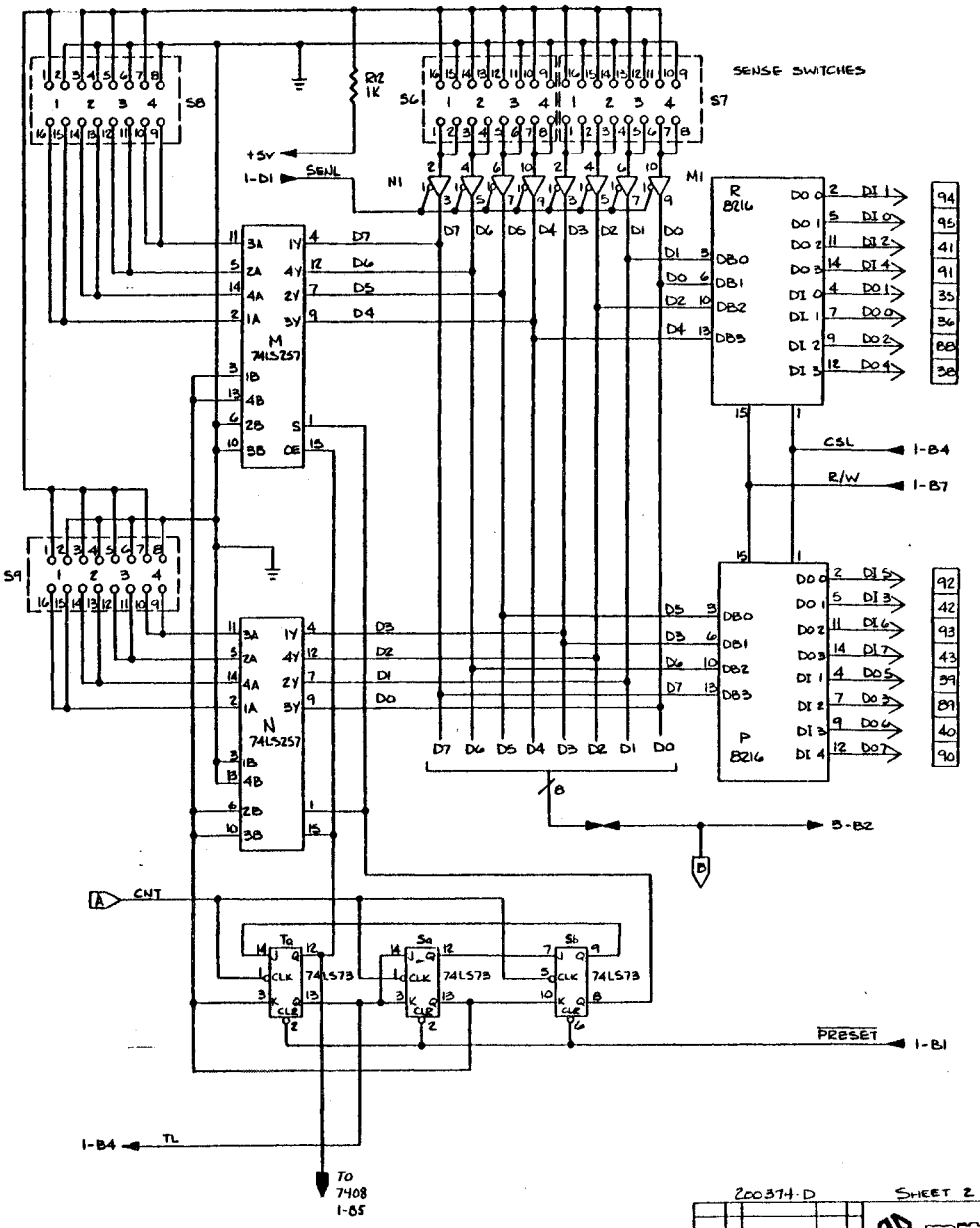
The most obvious use of the Sector interrupts would be performing a Sector search for Disk I/O. The Minidisk Controller would interrupt the Altair computer at the beginning of every Sector, or every 12.5ms. Only a few microseconds would be used in identifying the Sector count, and the Altair computer could be performing other tasks until the required Sector was found.

Another use for the interrupts is for Disk system timing. Instead of checking Move Head status every time the Disk head is stepped, the timing can be controlled by Sector interrupts. This is done by enabling interrupts and issuing the desired step command after the first interrupt is received. Since interrupts occur every 12.5ms , four interrupts are counted (50ms) and the next step command is issued. This process may be used to step the Disk head any number of tracks. Check for TRACK Ø status before issuing the step command.

To utilize Sector interrupts, on Minidisk Controller Board 1, the SR1 jumper must be connected to the desired interrupt pad. If single level interrupts are implemented, use the INT (or PINT) pad. If Vectored Interrupts are implemented, use the highest level priority, VIØ.

To enable interrupts, the 8080 CPU must have its interrupts enabled. Also if Vectored Interrupts are utilized, consult the 88-VI/RTC manual. Then, the Minidisk Controller must have its interrupts enabled. CPU Interrupts must be re-enabled after every interrupt is serviced if more interrupts are required.





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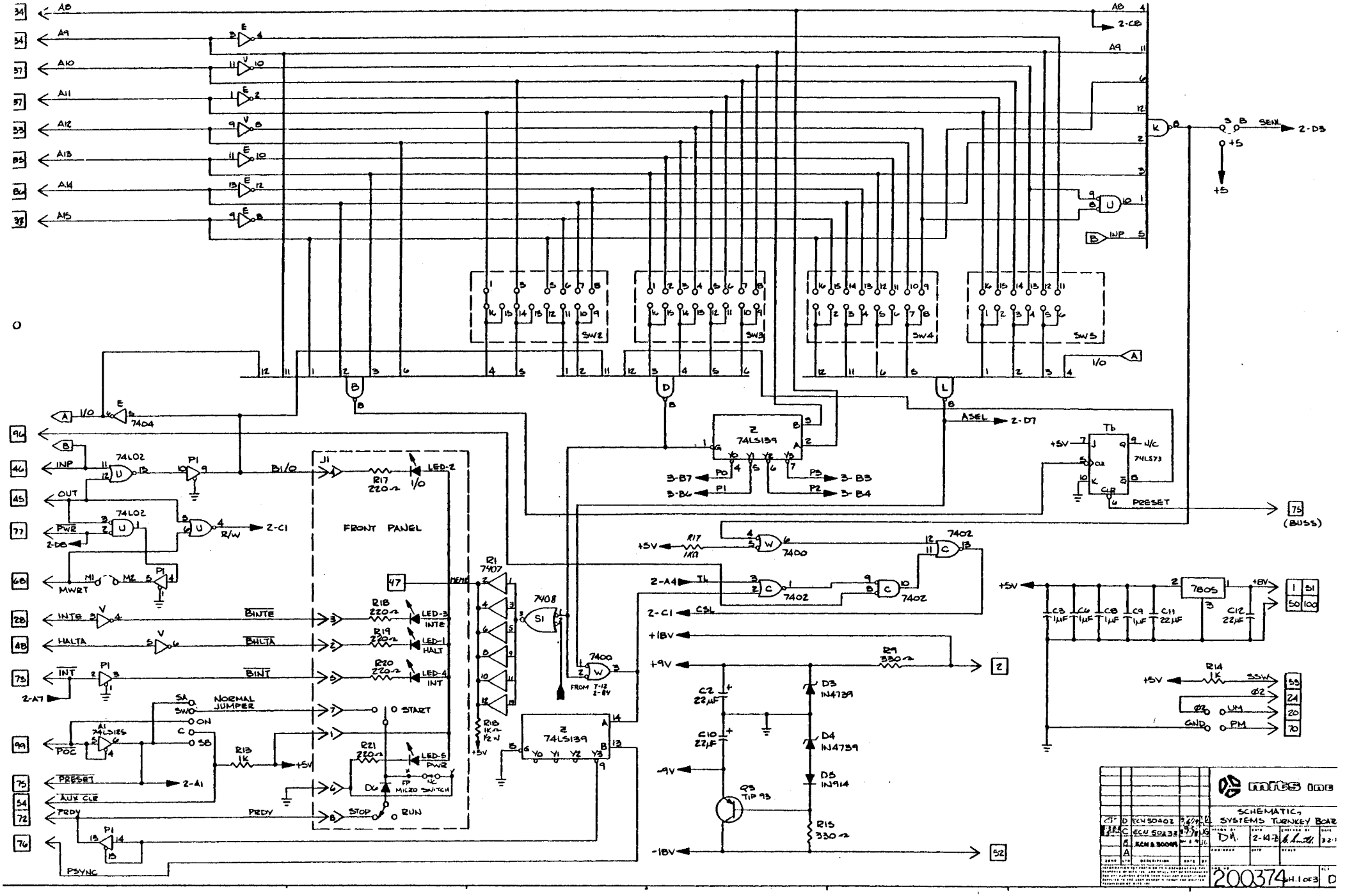
mits inc

SCHEMATIC, SYSTEMS TURNKEY BOARD

D	ECN 50802	9/27/76			
C	ECN 50232	8/17/76	DM	2-16-76	
B	ECN 50044	2/11/76			
A					



C	ECN 50402	9/6/77	LC	SCHEMATIC, SYSTEMS TURNKEY BOARD
B	ECN 50238	8/19/77	DH	2-14-78
A	RCN B 30099	8/16/77		

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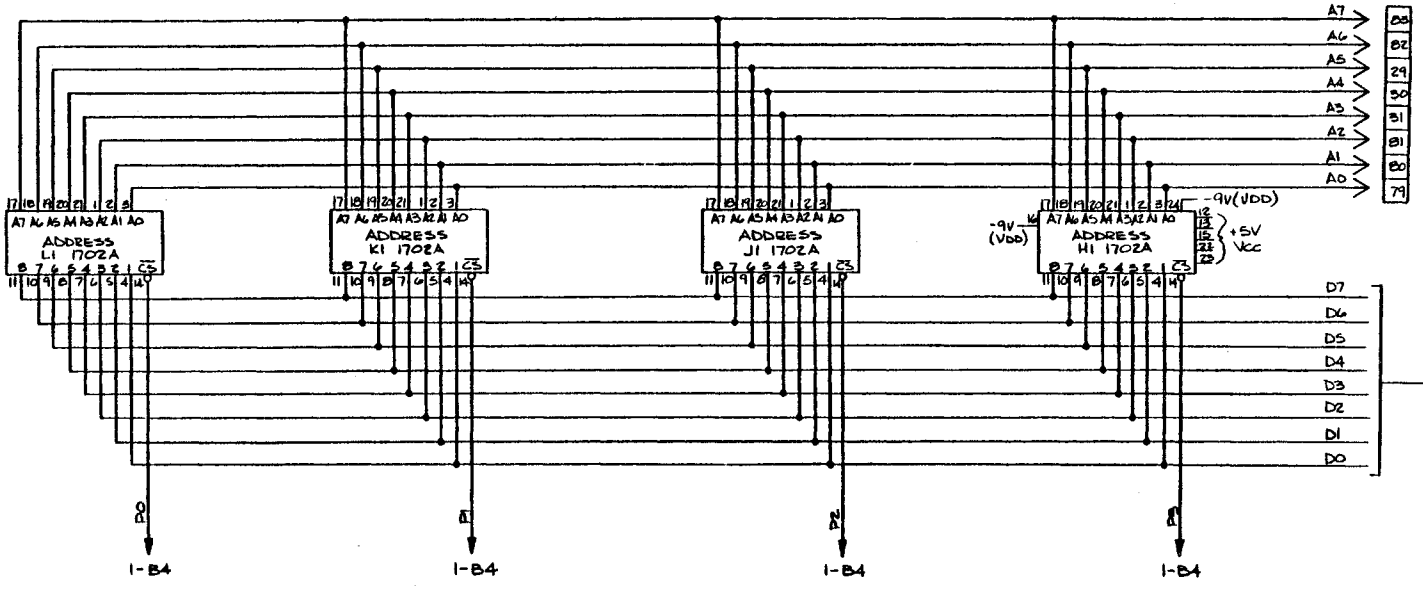

PROM

POWER CONNECTIONS				
REF DES	PART #	GND PIN	Vcc PIN	# OF PINS
L1,K1,J1,H1	1702A	——	12,22,23	24
B,V	7404	7	14	14
U,C	7402	7	14	14
A1	74LS125	7	14	14
Z	74LS139	8	16	16
W	7400	7	14	14
R1	7407	7	14	14
T,S	74LS75	11	4	14
B.B,L.K	74LS30	7	14	14
P1,N1,H1	74367	8	16	16
F	1489	7	14	14
Q	6850	1	12	24
M,N	74LS257	8	16	16
R,P	8216	8	16	16
S1	7408	7	14	14
A	1488	7	14	14

D	ECN 50402	4/5/76	D.M.	
C	ECN 50232	2/17/76	D.M.	
B	ECN 50099	1/5/76	D.M.	
A				

mits inc

SCHEMATIC, SYSTEMS TURNKEY BOARD

DRAWN D.M. 2-15-76 CHECKED [illegible] 3-2-76

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