New Style Altair 8800bt Turnkey Board

P/N 200372-01

Pages from 8800bt Manual

4 THEORY OF OPERATION - THE COMPUTER

4-4 TURNKEY BOARD

The Turnkey Board includes miscellaneous circuitry controlling the operations of PROM, I/O Channel, Sense Switches, Front Panel and Auto-Start logic.

The System Turnkey Board consists of:

- Sense Switches
- Prom Memory
- Serial I/O Channel
- Front Panel Logic
- Auto-Start Circuit
- Miscellaneous Signals

Detailed information on logic and operation of each is shown on the following pages and corresponding board schematics.

All power required comes from the +8V and ±18V lines on the Motherboard, and regulated down to +5V and ±9V.

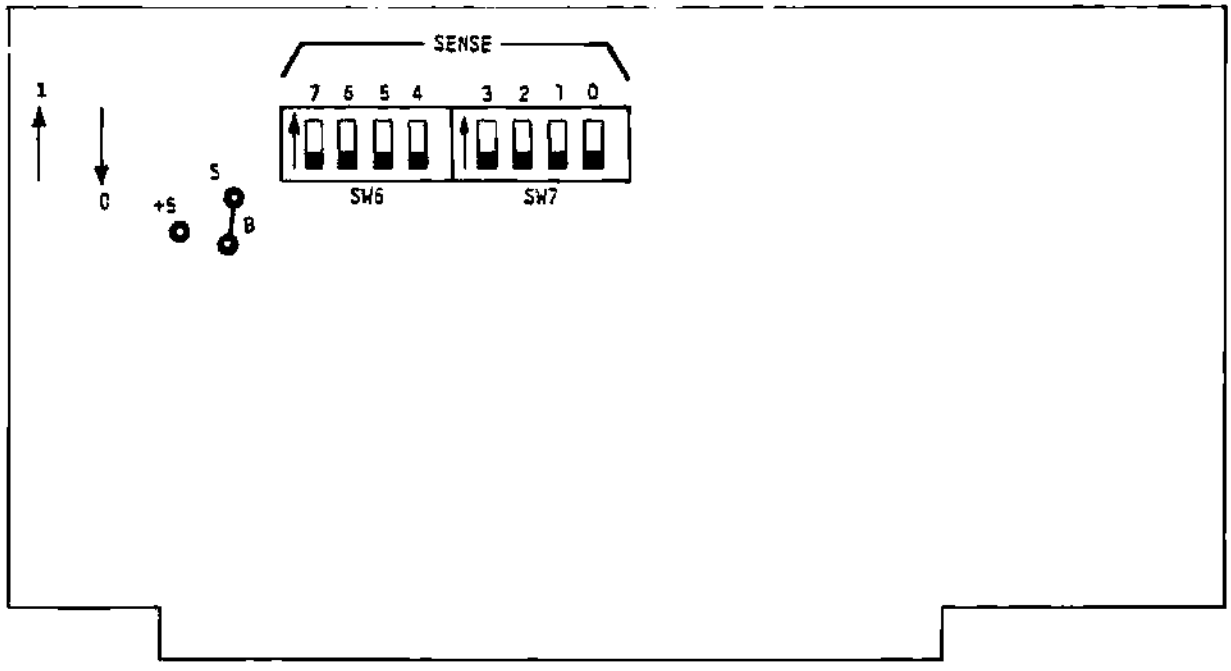
4-4 TURNKEY BOARD

4-4a SENSE SWITCHES

The sense switches determine the arrangement of data-input entry to perform a required operation. There are eight switches on the Turnkey Board representing one byte of data. This byte may be read by program instructions and used as data or to select options in the program.

Moving the sense switches in the direction of the silkscreened arrow on the Turnkey Board represents a one on the bidirectional data bus, and if the switch is moved in the opposite direction represents a zero on the bi-directional data bus.

In the schematic, IC K detects I/O port address, which is reserved for the sense switches. The output, active LOW, enables the tri-state buffers connected to the sense switches to place the bits represented by the switch positions on the bidirectional bus. IC K also enables the bus interface, so that the sense switch bits are placed on the Data-In system bus. The sense switches are used by the system software (refer to the appropriate software manual for actual use).



4-4b PROM MEMORY

The Turnkey Board includes programmable read only memory (PROM) to permanently store programs.

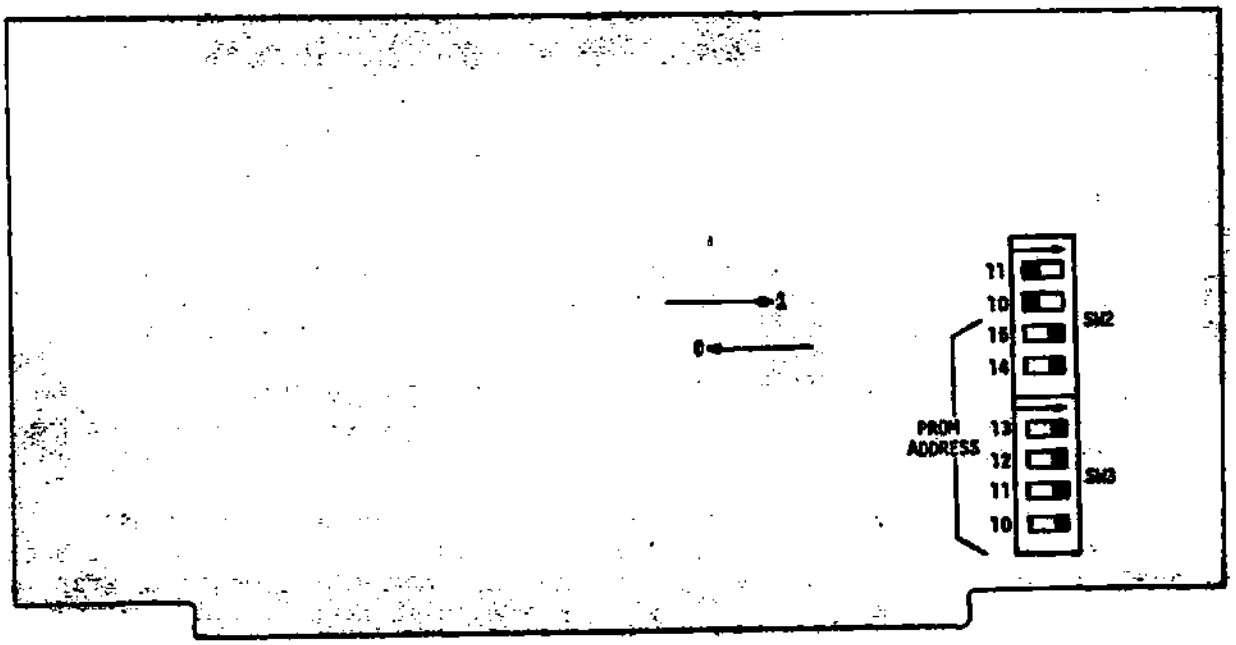
The Turnkey Board contains 1024 bytes of PROM. The starting address is selected by 6 switches on the Turnkey Board. The most significant 6 bits of the incoming address are compared with the switch settings. If they match, the remaining 10 bits are decoded to select the proper byte in that block.

The phantom circuit on the Turnkey Board allows PROM addresses to overlap RAM addresses. To set PROM address switches, select the starting address for each block and convert them to binary. The starting addresses must be integral multiples of 1024, so the low-order (rightmost) 10 bits of the PROM addresses must be zeros.

One starting bit address switch corresponds to each of the 6 high order bits of the starting address. (The most significant bit is bit 15.) If the bit is one, the corresponding switch is moved in the direction of the silk-screened arrow on the board. If the bit is zero, the switch is moved in the opposite direction of the arrow. This is shown on the facing page.

The incoming PROM address is compared with the starting PROM address by the NAND gate IC D. If the incoming address is in the 1K block selected for PROM, and an I/O cycle is not in progress, the output of IC D, active LOW, enables the PROM address decoder, IC Za, which selects one of the PROM ICs. Up to four PROM chips may be installed. The output of IC D is combined with the output of the I/O address detector in a NOR gate, the output of which causes the CPU to execute a Wait state and enables the data bus interface, IC's P and R. The low output from IC D is also fed to IC's S1 and R to hold MEMR LOW on the bus and prevents data from being read from System RAM. The selected PROM drives the bidirectional data bus, the interfaces, P and R, and puts the selected data on the Data-In system bus.

A memory read cycle to an address containing PROM and RAM will read PROM data; thus all 64K of address space can be utilized by RAM. An I/O cycle to port 377_8 (lines A8 - A15 HIGH) causes IC B, pin 8 to go LOW, clocking IC T, pin 8 LOW and permanently disabling IC D and the PROM select logic. The PROMS are disabled until a system reset clears IC T.


1
0
11
10
15
14
SW2
PROM ADDRESS
13
12
11
10
SW3

4-4 TURNKEY BOARD

4-4c SERIAL INPUT/OUTPUT (SIO) CHANNEL

The Turnkey Board uses a 6850 Asynchronous Communication Interface Adaptor (ACIA) to convert data characters from the CPU (in parallel format) into a continuous serial data stream for transmission. Simultaneously, it receives a serial data stream and converts it into a set of parallel data characters for the CPU.

The Input/Output (I/O) ports contain circuitry to communicate with devices existing outside the CPU or memory array.

In any computer system, the CPU must be able to communicate with peripheral devices (e.g., keyboard, floppy disks, printer, video display terminals) and other control structures that exist outside its normal memory array.

Input and Output operations are similar to memory read and write operation with the exception that a peripheral I/O device is addressed instead of a memory location.

Data can be input/output in either parallel/serial form via an I/O PORT. All data within the computer is represented in binary coded form. A binary data word consists of a group of bits, each bit is either a one or zero.

Parallel I/O consists of transferring all bits of a word at the same time, one bit per data line. Serial I/O consists of transferring one bit at a time time on a single line.

The CPU has special instructions devoted to manage read/write transfers and to isolate memory and I/O arrays. This assures that the memory address space is not effected by the I/O structure and makes it simpler to transfer data to and from the Accumulator with an addressed port.

The heart of the Serial Input/Output (SIO) circuitry is the ACIA (ICQ) which contains:

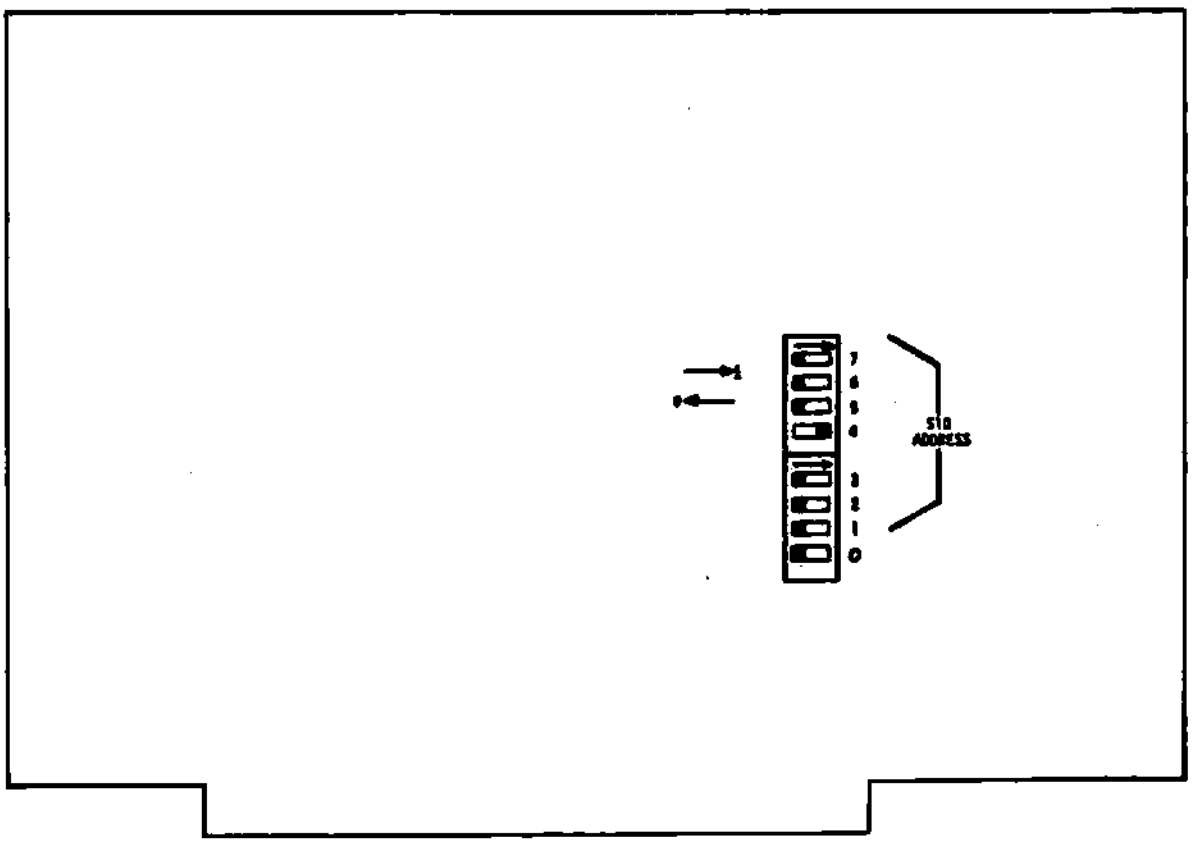
- Status Reg ster
- Control Re ister
- Interrupts
- Bit Rate S lection

These functions are described on the following pages.

The Turnkey Board SIO channel appears to the CPU as two of the 256 possible I/O ports. One port is used for data transfer and the other for channel status and control information. The high-order seven bits of the I/O address are compared with the SIO address switch settings. If they match, the channel is enabled. The least significant bit selects the Data (bit zero +1) or Status/Control (bit zero + 0) port.

To set the switches, convert the desired address to binary. Move each switch in the direction of the silkscreened arrow to represent a binary one and in the opposite direction for binary zero. Switch 7 represents the most significant bit.

The SIO address switches are shown below. The schematic at rear of manual shows serial I/O circuit.



i THE STATUS REGISTER

The Status Register contains status information on the data bus issued by the CPU at the beginning of each machine cycle. The status information tells what action will take place during that machine cycle.

When the Status/Control port is read during an input operation, the Status register contains information on the status of the Transmit Data register, the Receive Data register, the error logic, and peripheral or optional modem status inputs. The function of each bit of the Status register is:

Bit 0 Receive Data Register Full (RDRF . Receive Data Register Full indicates that received data has been transferred to the Receive Data register. RDRF is cleared after the CPU reads the Receive Data register or by a master reset. The cleared or empty state indicates that the contents of the Receive Data register are not current. RDRF also indicates empty if Data Carrier Detect is LOW.

1 Transmit Data Register Empty (TDRE). The Transmit Data Register Empty bit set to 1 indicates that the Transmit Data register contents have been transferred and that new data may be entered. A zero indicates that the register is full and that transmission of a new character has not begun since the last write data command.

Bit 2 Data Carrier Detect ($\overline{DCD}$). When the DCD input from a modem goes LOW to indicate that a carrier is not present, the Data Carrier Detect bit is set to 1. This setting causes an interrupt request to be generated if the Receive Interrupt Enable bit is set. After the DCD input returns HIGH, $\overline{DCD}$ remains one until it is reset, either by reading first the Status register and then the Data register, or by a master reset. If the DCD input remains LOW after the Status and Data registers have been read or a master reset occurs, the $\overline{DCD}$ bit remains the inverse of the DCD input.

Bit 3 Clear-to-Send ($\overline{CTS}$). The Clear-to-Send bit is the inverse of the Clear-to-Send input from a modem. Thus, zero in $\overline{CTS}$ indicates that there is a Clear-to-Send from the modem. When the Clear-to-Send signal is LOW, the Transmit Data Register Empty bit is inhibited and the $\overline{CTS}$ status bit is set to one. Master reset does not affect the $\overline{CTS}$ bit.

Bit 4 Framing Error (FE). A framing error occurs when the received character is improperly framed by a start and a stop bit. It is detected by the absence of the first stop bit. This indicates a synchronization error, faulty transmission, or a break condition. The Framing Error flag, FE, is set during the receive data transfer time. Therefore, the error indicator is present throughout the time that the associated character is available.

Bit 5 Receiver Overrun (OVRN). OVRN is an error flag that indicates that one or more characters in the data stream were lost, that is, a character or a number of characters were received but not read from the Receive Data register (RDR) before subsequent characters were received. The overrun condition begins at the midpoint of the last bit of the second character received without the RDR having been read. The OVRN bit is not set in the Status register until the valid character prior to the overrun has been read. The RDRF bit remains set until OVRN is reset. The OVRN bit is reset when data is read from the Receive Data register or by the master reset. Character synchronization is maintained during the overrun condition.

Bit 6 Parity Error (PE). The Parity Error flag indicates that the number of ones in the character does not agree with the preselected parity. Odd parity is defined as the condition in which the total number of ones in the character is odd. Even parity means the number of ones is even. The parity error indication is present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

Bit 7 Interrupt Request (IRQ). IRQ indicates the state of the IRQ signal. Any interrupt condition, with its applicable enable, is indicated in this status bit. Anytime the IRQ signal is LOW, the IRQ bit is set to indicate the interrupt or service request status.

ii THE CONTROL REGISTER

The Control Register contains status information on the current instruction governing the operation of the CPU for each machine cycle.

When the Status/Control port is loaded during an output operation, the control register contains information which controls the functions of the receiver and transmitter, interrupt enables, and the Request-to-Send peripheral/modem control input. The Control register bits and their functions are:

Bit 0 and 1 — Counter Divide Select

The Counter Divide Select bits determine the clock divide ratios used in both the transmitter and receiver sections of the SIO. Additionally, these bits are used to provide a master reset for SIO which clears the Status register (except for external conditions on the CTS and DCD lines) and initializes both the receiver and transmitter. Master reset does not affect other Control register bits. Note that after power-on or a power failure/restart, these bits must be set HIGH to reset the SIO. After reset, the clock divide ratio may be selected. The counter select bits provide for the following clock divide ratios:

CR1	CR0	RATIO
0	0	1 (synchronized)
0	1	16 (normal)
1	0	64 (slow)
1	1	master reset

The section 4-4c,iv describes the use of these bits to select the baud rate.

Bits 2, 3 and 4 — Word Select

The Word Select bits are used to specify word length, parity, and the number of stop bits in each character. Word length, parity select, and stop bit changes are not buffered and therefore, become effective immediately. The encoding format is as follows:

CR4	CR3	CR2	FUNCTION
0	0	0	7 bits, even parity, two stop bits
0	0	1	7 bits, odd parity, two stop bits
0	1	0	7 bits, even parity, one stop bits
0	1	1	7 bits, odd parity, one stop bits
1	0	0	8 bits, two stop bits
1	0	1	8 bits, one stop bit
1	1	0	8 bits, even parity, one stop bit
1	1	1	8 bits, odd parity, one stop bit

Bits 5 and 6 — Transmitter Control.

Two ransmitter Control bits provide for control of the interrupt from the Transmit Data Register Empty condition, the Request-to-Send output, and the transmission of a break level (space). The setup of interrupt jumpers are shown in Section 4-4c,iii. The following coding is used:

CR6	CR5	FUNCTION
0	0	RTS = HIGH, Transmitting Interrupt disabled
0	1	RTS = HIGH, Transmitting Interrupt enabled
1	0	RTS = LOW, Transmitting Interrupt disabled
1	1	RTS = HIGH, transmits a break level on the transmit data output, Transmitting disabled

Bit 7 — Receive Interrupt Enable

Receive Data Register Full, Overrun and Data Carrier Detect interrupt requests are enabled by a 1 in the Receive Interrupt Enable bit.

iii INTERRUPT HANDLING

Interrupts are requests to the CPU to either initiate or terminate the normal operation cycle.

The SIO generates an interrupt signal that may be connected to an interrupt line on the bus by means of jumpers. The jumper pads are shown on the facing page. The peripheral input lines also set the interrupt of the Control Register.

No jumper is installed if the SIO is not required to interrupt the CPU. Software can detect Status register bits in this case and direct I/O operations without interrupts.

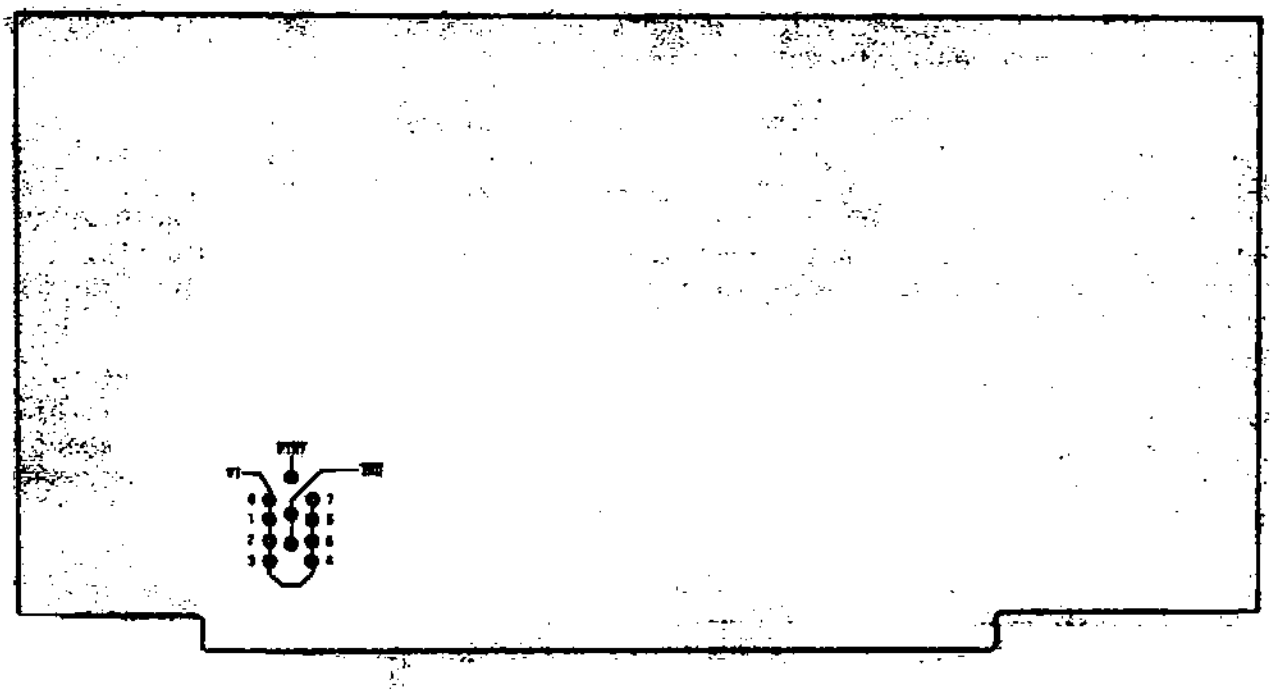
In systems not using the Vector Interrupt board, the signal IRQ may be connected to the $\overline{\text{PINT}}$ line. Then, if an SIO interrupt occurs, $\overline{\text{PINT}}$ will be pulled LOW until the condition that caused the interrupt no longer exists. If the Interrupt Enable bit in the CPU is set, then a RST 7 instruction is forced into the instruction sequence. Interrupt signals from other I/O circuits may also be connected to the $\overline{\text{PINT}}$ line if their outputs are effectively driven by open collector drivers. All MITS 300 I/O boards currently manufactured and supported have open collector interrupt signal drivers.

In systems using the Vector Interrupt board, IRQ may be connected through a jumper to any pad marked VI0 through VI7. These represent the 8 interrupt priority levels. Interrupt signals from different boards may be connected to the same priority level if they are all driven by open collector drivers.

The $\overline{\text{IRQA}}$ signal is brough out to jumper pad KA in the lower lefthand corner of the board. It is connected to the bus by installing one of the following jumpers:

If the Vector Interrupt board is in use, install the jumper from KA to one of the pads marked VI0 to 7, depending upon the priority level at which printer interrupts are to occur. See the VI/RTC board manual for further information.

If the Vector Interrupt board is not used, install the jumper between KA and $\overline{\text{PINT}}$. The jumper pads are shown on the facing page.



iv BIT RATE SELECTION

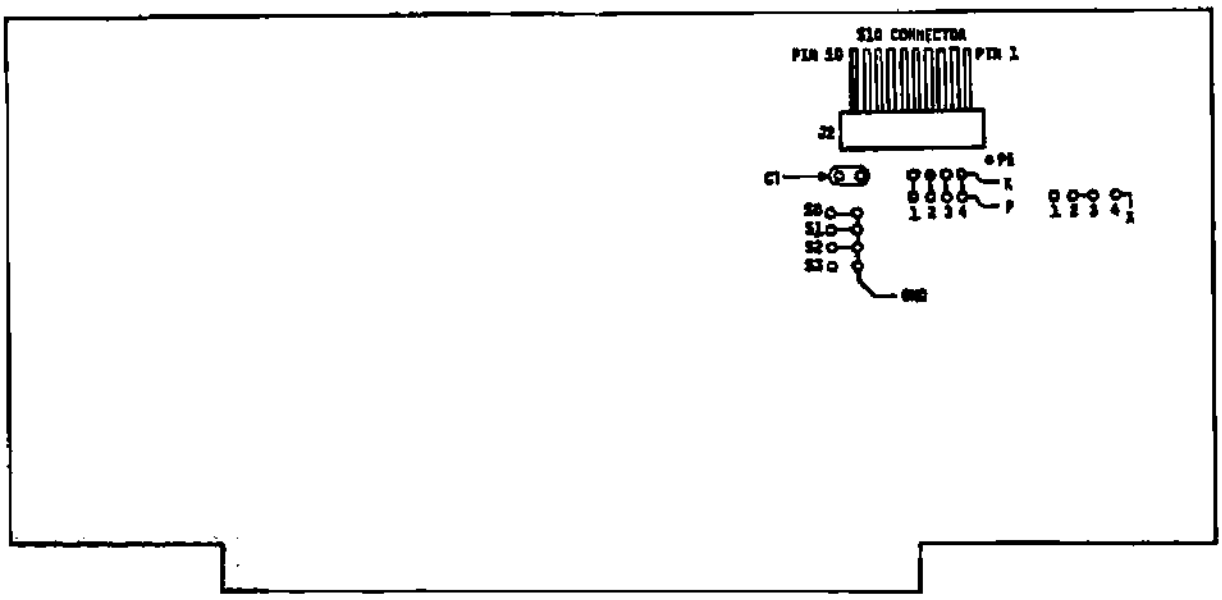
The rate at which binary digits or pulses representing them pass a given point on a communications device or channel in a second is called Bit Rate.

The bit rate is defined as the maximum rate of level changes on the data signal line. Since the SIO is an asynchronous device, the bit rate determines the rate at which the bits within each character are received or sent, but not in general, the average rate at which characters are handled.

The bit rate is generated by IC G which uses 2.4576 MHz crystal. The required Baud rate is obtained by selecting jumpers.

The bit rate is selected by jumpers and by Control register bits 1 and 0. The resultant bit rate for every usable combination of jumpers and control bits is shown on the facing page. If CR0 and CR1 are both zero and the external rate is not selected, then the SIO may only be used for transmission. Otherwise, the SIO may be used for both receiving and transmitting at the selected rate. If a rate above 300 bits per second is selected, capacitor C1 should be removed.

If the external clock and the 1 counter are selected, then the data must be synchronized with the clock. The transmitted data line changes levels within one microsecond of the LOW to HIGH clock transition. Output jitter is about 500 nanoseconds. The SIO will sample the receive data line within 1 microsecond after the HIGH to LOW clock transition.



Data Transmission Rates						
Jumpers (X means installed)				CR0 = 1 CR1 = 0 (normal; 16 counter selected)	CR0 = 0 CR1 = 1 (slow; 64 counter selected)	CR0 = 0 CR1 = 0 (sychronous data; 1 counter selected)
S3	S2	S1	S0			
-	-	-	-	110	27.5	1760
-	-	-	X	150	37.5	2400
-	-	X	-	300	75	4800
-	-	X	X	2400	600	38400
-	X	-	-	1200	300	19200
-	X	-	X	1800	450	28800
-	X	X	-	4800	1200	76800
-	X	X	X	9600	2400	153600
X	-	-	-	2400	600	38400
X	-	-	X	600	150	9600
X	-	X	-	200	50	3200
X	-	X	X	134.5	33.375	2152
X	X	-	-	75	18.75	1200
X	X	-	X	50	12.5	800
X	X	X	-	External 16 rate	External 64 rate	External rate
X	X	X	X	(36,000 max)	(9000 max)	(400,000 max)

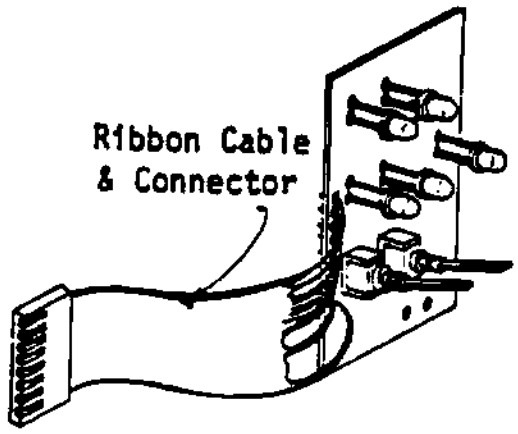
4-4d FRONT PANEL LOGIC

The front panel logic is contained on the Turnkey Board. The indicators and switches on the front panel are connected to the Turnkey Board by a cable.

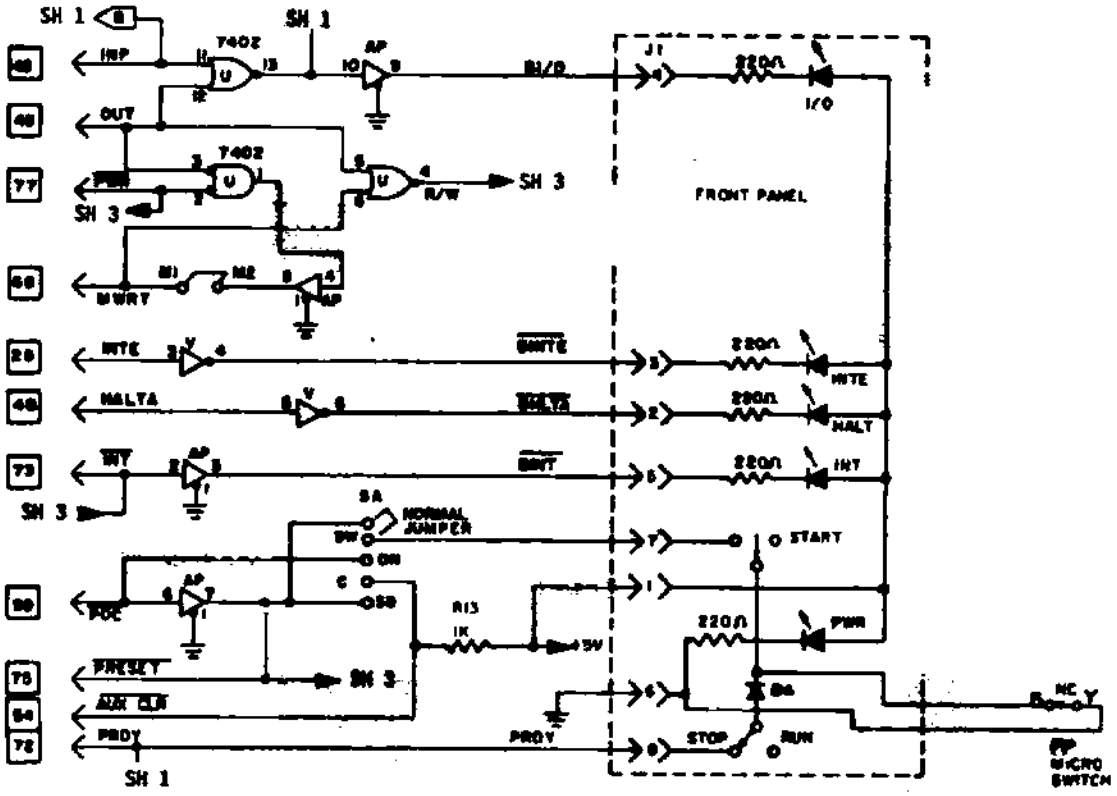
The bus signals PHLTA, PINTE, and $\overline{\text{PINT}}$ are buffered to drive the indicators HALT, INTE, and INT, respectively. The I/O indicator is driven by the logical sum (OR) of the INP and OUT signals. The POWER indicator monitors the output of the +5V regulator on the Turnkey Board.

The bus signal PRDY is grounded when the RUN/STOP switch is in the STOP position. PRESET is grounded momentarily by the START switch which, in turn, initiates the Auto-Start sequence.

The circuit diagram and ribbon cable orientation are shown on the facing page.



Ribbon Cable Orientation



Circuit Diagram

4-4 TURNKEY BOARD

4-4e AUTO-START CIRCUIT

The Turnkey Board provides an Auto-Start program in PROM which allows program loading to be done automatically from a Front Panel switch. The address of Auto-Start is the first location of a routine in PROM.

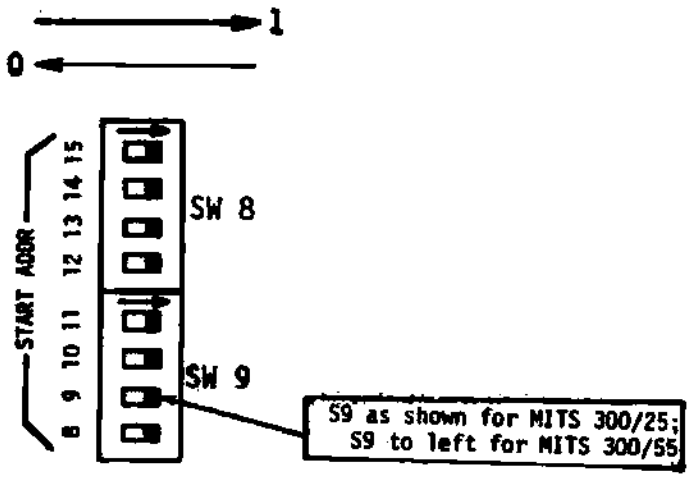
When power is turned on, or when the Start switch is released, the start sequence logic forces the CPU to jump to the Auto-Start address and to begin executing instructions. The address is selected by a set of Auto-Start switches (SW8 and SW9) on the Turnkey Board.

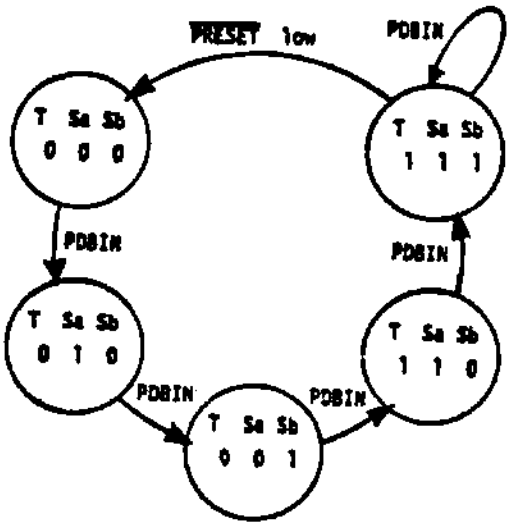
The Auto-Start switches are set in the same manner as PROM address switches previously described. The Auto-Start address is the address of the first location of a routine in PROM or Turnkey monitor. The address must be an integral multiple of 256, so the low-order eight bits must be zeros. The eight Auto-Start switches correspond to the high-order eight bits of the Auto-Start address. Bit 8 is the least significant bit. The switches are shown on the facing page.

The switches represent the variable byte in a JMP instruction. The JMP instruction is generated by a multiplexer, ICs M and N, which is controlled by flip-flops T, Sa and Sb. The flip-flops are cleared by PRESET, a bus signal derived from POC or generated by the Start switch on the front panel. Subsequent PDBIN pulses cause the flip-flops to change from one state to the next as shown in the sequence diagram on the facing page. The pulses generated by the flip-flops cause the multiplexer to choose the byte designated by the Auto-Start switches.

These bytes are placed on the bidirectional data bus in sequence and become the Auto-Start JMP instruction. The sequence of events in the Auto-Start procedure is shown on the facing page.

During the three bytes of the JMP instruction, the LOW Q output of flip-flop Ta, pin 12 is fed through IC's S1 and R1 to hold MEMR low and keep memory data off the bus. Once the JMP instruction is complete, Q goes HIGH and memory instructions can again be fetched.





Auto-Start Logic Control State Diagram

Auto-Start Sequence

Signal In	Control State	Function
PRESET	000	Mux. outputs enabled, Bus interface enabled, 303 octal put on bus.
PDBIN	010	000 put on bus.
PDBIN	001	Byte in Address switches put on the bus.
PDBIN	110	First byte of PROM program
PDBIN	111	Next byte of PROM program
.	.	.
.	.	.
.	.	.

4-4 TURNKEY BOARD

4-4f MISCELLANEOUS SIGNALS

The SIO can be configured to interface with peripheral equipment using 20 mA current loop, RS-232, and TTL signals. These signal options are selected by jumpers and internal cable connections.

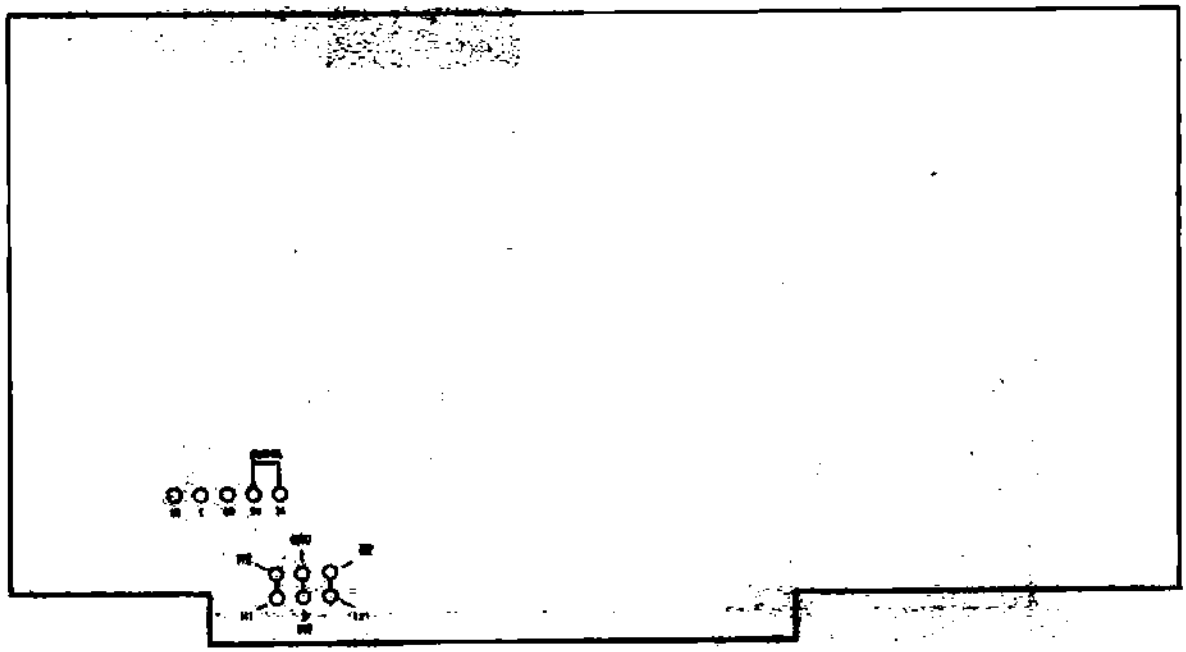
The SIO cable runs from the I/O connector on the Turnkey Board to the rear panel. The rear panel connector is the industry standard 25-pin data communications connector. The diagrams on the facing page depict setting-up the SIO for modem, teletype and RS-232 type operation.

Several miscellaneous signals are handled by the rest of the circuitry on the Turnkey Board. Some are optional and may be selected by jumpers.

MWRT is generated if the jumper from M1 to M2 is installed. It is used by memory boards for write functions, and installed on all MITS 300 Systems.

PROT and UNPROT are used for memory protect and unprotect functions. As supplied, the Turnkey Board grounds PROT and pulses UNPROT with phase 2 of the clock to unprotect all memory as it is accessed. This feature may be disabled by removing the jumpers from 02 to UM and from GND to PM.

AUX CLR is normally pulled HIGH by a resistor on the Turnkey Board, but insertion of optional jumpers allows the signal to be used.



Internal Cable Connections

From Molex		To 25 Pin Connector		
Pin Number	Function	Female TTY Cable	Male RS232 Cable	Female TTL Cable
1	TTL RTS	6		4
2	TTY XMIT	3		
3	TTY REC	4		
4	All REC	5	2	2
5	DCD		8	8
6	CTS		5	5
7	XTERNAL CLOCK		15	15
8	GND	2	7	7
9	RS232 RTS		4	
10	RS232 + TTL XMIT		3	3

Input/Output Signal Types

Signal Type	From	To	Notes
TTY Compatible	X1	X2	
	X4	P5	
	X3	P3	
	X2	P2	
RS232 Compatible	X3	X4	
	X3	P3	Put in only if DCD signal is not used.
	X2	P2	Put in only if CTS signal is not used
TTL Compatible (3.2 mA max load 16 mA min drive)	X2	X3	
	X4	P4	
	X3	P3	
	X2	P2	
	X1	P1	Not needed if external clock is not used.

Note: TTL inputs are two unit loads; input is actually "TTL compatible."