altair™ 88-16MCD

PRELIMINARY DOCUMENTATION

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a subsidiary of **Pertec Computer Corporation**

altair 88-16MCD

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INTRODUCTION

1-1. SCOPE AND ARRANGEMENT

The Altair 16K Dynamic Memory Board (88-16MCD) Documentation provides a general description of the printed circuit board and detailed theory of its operation. The manual contains four sections as follows:

1. Section I is a general description of the Altair 16K Dynamic Memory board.
2. Section II includes a detailed theory explanation of the 88-16MCD circuit operation.
3. Included in Section IV is a troubleshooting guide for the 88-16MCD board.
4. Assembly instructions for the 88-16MCD are found in Section V.

1-2. DESCRIPTION

The 16K Dynamic Memory board (88-16MCD) provides 16,384 bytes of random access memory for the Altair 8800 series computers. It uses thirty-two dynamic memory ICs (4K x 1 bits each) which have a maximum access time of 350 nanoseconds. The board requires a total of only three watts of power for all thirty-two ICs.

The 88-16MCD provides continuous operation at maximum speed by eliminating time-consuming wait states. All logic timing is crystal-controlled for greater accuracy. The board occupies one slot and plugs directly into the computer.

Address selection is done by an 8-pin dip switch, and one jumper selects either 8800b or 8800b Turnkey operation.

88-16MCD
SECTION II
THEORY OF OPERATION

2-1. ADDRESSING

The 88-16MCD can store a total of 16,384 bytes of data which are arranged in four blocks of 4,096 bytes each. Address lines A14 and A15 are decoded to select one of the four 16K memory boards which are directly accessed by the CPU. After the board has been selected, address lines A12 and A13 are decoded to select one of four 4K blocks on the board; AØ through A11 are decoded to select one byte within the 4K block.

The address select switch on each board determines the board's location within the 64K memory area as shown in Table 2-A.

Table 2-A. Address Switch Setting

	Switch (SW-1)			
	1	2	3	4
0 - 16K	Closed	Open	Open	Open
16 - 32K	Open	Closed	Open	Open
32 - 48K	Open	Open	Closed	Open
48 - 64K	Open	Open	Open	Closed

For example, assume that switch 1 is closed, and the address on the bus indicates that both A14 and A15 (Figure 2-1, Zone D2) are LOW. Inverter V presents HIGHs to input pins 13 and 14 of IC R (Zone D2) a dual 2-line input to 4-line decoder. Half of IC R contains input pins 13 and 14 and output pins 9, 10, 11 and 12. It is permanently enabled by the LOW on pin 15 (Zone D3). With pins 13 and 14 HIGH, pin 9 (Zone D2) goes LOW. Since switch 1 is closed, the LOW is passed to IC R pin 1 (Zone D2) which becomes the enable signal for the remaining input pins 2 and 3 (Zone D3) and output pins 4, 5, 6 and 7. At the same time, the LOW is present at IC Z pin 1 (Zone B2) in order to partially condition it for any subsequent read cycles from the selected memory board. The LOW from IC R pin 9 (Zone D2) is also inverted through IC X (Zone C2) and applied to IC M pins 4 (Zone D7) and 13 (Zone C7) as the Address Enable signal. With the first half of IC R enabled, it passes the decoded state of A12 and A13 through IC K to IC F (Zone C3).

The final address selection is made with a multiplexing scheme under the control of IC A (Zone D5), a Parallel Out Shift Register which is clocked by the crystal controlled oscillator circuit composed of XTAL #1 (Zone D7), IC B, R2, R3 and C6. IC A (Zone D5) is enabled by a HIGH on pin 9. This is accomplished by clocking IC C pin 5 (Zone C6) to a HIGH level. T1 is the first clock period of machine cycle 1. At the beginning of T1, IC M pins 2 and 4 (Zone D7) are LOW, forcing a LOW on IC C pin 3. During the latter stage of T1, SYNC, Ø2 and the Address Enable signal from IC X pin 2 go HIGH (Zone D7). However, the Ø2 inversion through IC Y (Zone B8) to IC M pin 3 (Zone D7) maintains a LOW on IC C pin 3 (Zone C6). When Ø2 transitions from HIGH to LOW during the latter part of T1, all HIGHs are present on IC M pins 1, 2, 3 and 4 (Zone D7). This reverses the level on IC C pin 3 from LOW to HIGH, clocking a HIGH on pin 5 (Zone C6), enabling IC A (Zone D5).

After IC A is enabled, the first 50 nsec. clock into IC A pin 8 drives IC A pin 3 HIGH. This signal is inverted through IC H (Zone D5) and becomes the $\overline{RAS}$ (Row Address Select), the enabling signal to each gate of IC F (Zone C3). At this time, IC A pins 5, 6 and 13 (Zone D5) and IC E pin 5 (Zone B6) are LOW. Thus, IC I pin 6 (Zone B5) is also LOW, enabling the tri-state buffer IC S (Zone A5). This allows the row address on AØ through A5 (Zone A4) to be latched into the appropriate 4K block of memory by the active $\overline{RAS}$ signal (Zone C3) which is selected through IC F by the decoded input of A12 and A13 (Zone D3).

$\overline{RAS}$ selects the 4K blocks as shown in Table 2-B.

Table 2-B. $\overline{RAS}$ Selection

Address Lines	Signal	Row
$\overline{A12}$, $\overline{A13}$	$\overline{RAS}$ Ø	AØ-A7
A12, $\overline{A13}$	$\overline{RAS}$ 1	BØ-B7
$\overline{A12}$, A13	$\overline{RAS}$ 2	CØ-C7
A12, A13	$\overline{RAS}$ 3	DØ-D7

Two clock periods after IC A pin 3 (Zone D5) has gone HIGH (100 nsec), IC A pin 5 goes HIGH, reversing the levels on IC I pins 6 and 8 (Zone B5). IC W (Zone A5) is now enabled, IC S (Zone A4) is disabled, and the column address on A6 through A11 (Zones A5 and A4) is presented to the selected 4K memory block. IC A pin 6 (Zone D5) goes HIGH one clock period after IC A pin 5 has gone HIGH. The signal from IC A pin 6 is inverted at IC H (Zone B5) and applied to each RAM IC as $\overline{CAS}$, Column Address Select (Zone B3). $\overline{CAS}$ causes the column address on A6 through A11 and $\overline{CS}$ to be latched into the selected 4K memory board. The RAMs' internal address circuitry in the selected 4K block decodes the combined input of AØ through A11 in order to select one address out of the possible 4096. The selected address is now written into or read from. Four clock periods after IC A pin 6 goes HIGH (200 nsec), following the completion of the write or read cycle, IC A pin 13 (Zone D) goes HIGH. This signal is inverted through IC H (Zone C6) to clear IC C pin 5 and disable IC E (Zone C3). The resulting LOW at IC A pin 9 (Zone D5) drives all outputs of IC A LOW and prepares it for another addressing cycle.

2-2. WRITE CYCLE

For a memory write cycle, the MWRITE line goes HIGH (Zone C8) and is inverted through ICs Y, X (Zone C8) and D (Zone B4). This signal appears on each of the 32 RAM ICs pin 3 as LOW and coincides with the active $\overline{RAS}$ signal (Zone C3) on each of the 8 RAMs pin 4 in the selected 4K block. The next falling edge of $\overline{CAS}$ now latches the data present on the DOØ through DO7 (Zone C1) lines from the CPU into pin 2, DI (Zone C2), of each of the 8 selected RAMs.

2-3. READ CYCLE

For a memory read cycle, a LOW is held on the MWRITE line, placing a HIGH on pin 3 of each RAM while $\overline{CAS}$ is active. This causes the internal data buffer of each of the 8 RAMs, as selected by $\overline{RAS}$ and $\overline{CS}$, to present their stored data to pin 14, DO (Zone B2) of each selected RAM and to the inputs of IC Z (Zone B2). MEMR and PDBIN (Zone A2) are both HIGH, indicating a read from memory. IC Z pins 13 and 11 (Zone B2) are also HIGH, conditioning IC Z to pass data from the RAMs to the CPU, lines DIØ through DI7 (Zone B1).

2-4. REFRESH CYCLE

Due to the dynamic nature of the RAM ICs used on the 88-16MCD, the storage cell matrix within each RAM must be accessed (refreshed) at least once during each 1 millisecond time interval to prevent loss of stored data.

The on-board refresh circuitry insures that a pulse is provided to each of the 64 row addresses within each 4K block once each millisecond. Refresh timing is controlled by the free running timer, IC P (Zone B6) whose output is a 15 microsecond clock into IC E pin 11. Pin 9 of IC E (Zone B6) provides a D input for the first half of IC E (Zone C6). The output pins 5 and 6 of IC E (Zone C6) then become the refresh control signals.

The operation of the refresh circuitry is explained for two conditions, Run and Stop. For example, assume that the system is in the Run mode. IC E pin 3 (Zone B6) is clocked by the gated combination of SM1, Ø2 and $\overline{\text{PDBIN}}$ through IC U pin 12 (Zone C7). If the board is not being addressed, IC R (Zone D3) is inactive, and all outputs are HIGH. The negative pulse from IC E pin 6 (Zone B6) accomplishes the following:

1. enables IC A (Zone D5) by driving IC C pin 5 (Zone C6) HIGH. IC A carries out its shift sequence as described in the addressing section (Paragraph 2-1).
2. enables all outputs of IC K (Zone C3) into IC F where they are gated with the output from IC A pin 3 (Zone D5) and applied to pin 4 of all 32 RAMs as $\overline{\text{RAS}}$ Ø through $\overline{\text{RAS}}$ 3.
3. clears IC E pin 9 (Zone B6) so that it is conditioned to toggle on the next clock from IC P (Zone B6).
4. triggers IC J pin 4 (Zone C4) which applies a LOW to IC Z pin 11 (Zone B2), latching the output data before the refresh cycle.
5. enables IC L (Zone A3), allowing one of the 0 through 63 counts produced by IC G (Zone A3) to be presented as the RAM refresh address. IC G is a 7-bit ripple counter, but only 6 bits are used.

At the same time, the positive pulse on IC E pin 5 (Zone C6) accomplishes the following:

1. disables $\overline{CS}$ (Zone B3) to each RAM.
2. disables buffers IC W and IC S (Zone A5).
3. conditions IC G (Zone A3) so that its count will be advanced by one on the falling edge of the pulse from IC E pin 5.

This sequence is repeated once each refresh cycle. The count of IC G advances by one to a maximum of 63 and then returns to 0. Thus, all 64 row addresses in each RAM are pulsed with all $\overline{RAS}$ signals active. This process accomplishes the refresh of the memory cell matrix. (Note that 15 microseconds multiplied by 64 counts equals .96 milliseconds, which is within the required 1 millisecond time interval).

The second refresh condition is the system in the Stop mode. Refresh action is similar to the previous condition but is different in several ways. Upon entering the Stop mode, the RUN line (Zone B8) goes LOW, causing the clear inputs to be removed from IC C pin 13 (Zone C8), IC N pins 14 and 15 (Zone B7), and IC J pin 11 (Zone D4). After RUN has gone LOW, IC C pin 8 (Zone C8) is clocked LOW on the first rising edge of the pulse from IC E pin 5 (Zone C6), holding a LOW on IC I pin 13 (Zone C6). IC N pin 9 (Zone B7), clocked HIGH by Ø2, now provides clocks to IC E pin 3 (Zone B6) for the duration of the Stop mode. IC C pin 9 (Zone C7) partially conditions IC M, and the final conditioning of IC M is accomplished by IC J pin 12 (Zone D4). This produces a short negative pulse at the end of each refresh cycle, causing IC M pin 8 (Zone C7) tc toggle. This allows a normal memory access in order to deposit and examine from the front panel while in the Stop mode.

When a HALT instruction is executed, the HLTA signal going HIGH at IC T pin 1 (Zone B8) simulates the Stop mode by forcing a HIGH at IC X pin 10 (Zone B8), allowing refresh to occur as previously stated.

2-5. SYSTEM OPTIONS

When the 88-16MCD is implemented with a full front panel system, the WAIT line is not used on the board, leaving IC Y pin 6 (Zone B8) open. However, if the 88-16MCD is used with a turnkey system (which does not have an interface board), Y pin 6 and T pin 11 (Zone B8) must be connected. This connection is made in order to substitute the WAIT line for the RUN line, since the RUN line is not used in the turnkey system. Jumpers are located according to the following diagram:

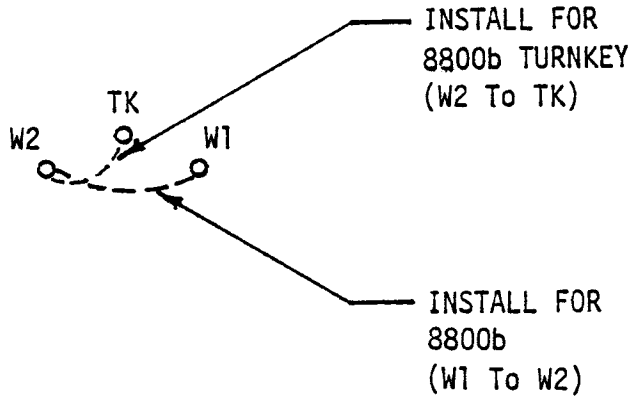


Figure 2-3. Jumpering Options

POWER CONNECTIONS				
IC	TYPE	VCC	GND	OTHER
A	74LS164	14	7	
B	74S04	14	7	
C	74LS74	14	7	
D	74LS20	14	7	
E	74LS74	14	7	
F	74LS32	14	7	
G	4024	14	7	
H	7404	14	7	
I	74LS32	14	7	
J	74LS123	16	8	
K	74LS08	14	7	
L	8797	16	8	
M	74LS55	14	7	
N	74LS112	16	8	
P	LM355	8	1	
R	74LS189	16	8	
S,W	8797	16	8	
T	74L04	14	7	
U	74LS27	14	7	
V	74L04	14	7	
X	74LS04	14	7	
Y	74L04	14	7	
Z	82/12	24	12	

For details see Sheet 2 of 2

16K x 8
MK 4096-15
32 DEVICES

NOTE:
1) RESISTORS ARE 1/4 WATT VALUE IN OHMS.
2) I.C. POWER CONNECTIONS PER CHART.
3) FOR EPROM (MK 4096-15) CONNECTION DETAILS SEE DWG-8800-123 (SH 2)

Figure 2-1. 88-16MCD Schematic (Sheet 1 of 2)

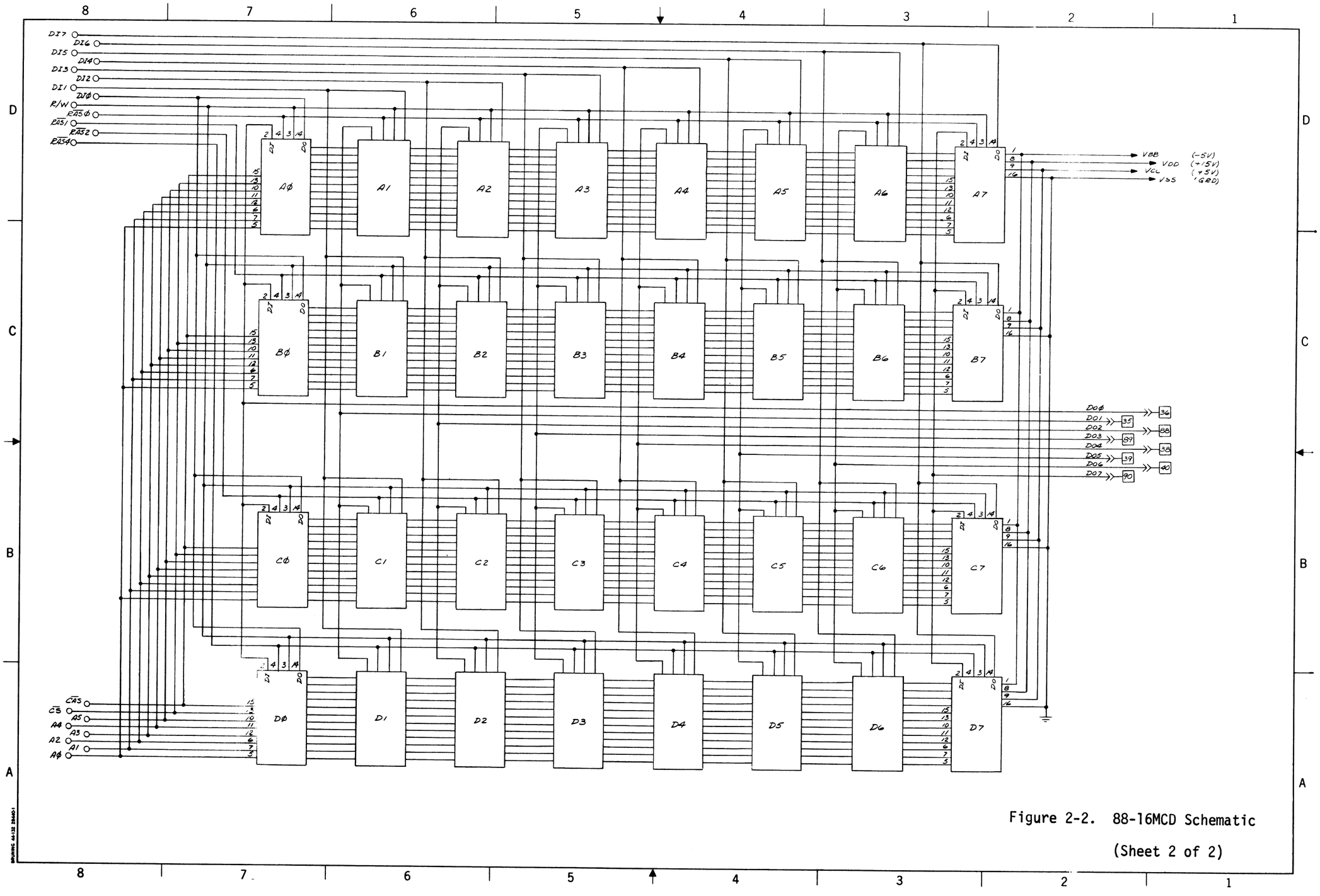


Figure 2-2. 88-16MCD Schematic

(Sheet 2 of 2)

88-16MCD
SECTION III
TROUBLESHOOTING

3-1. GENERAL

This troubleshooting guide is designed for use with the 8800b front panel to diagnose failure on the 88-16MCD memory board. Although no reference is made in this guide to specific diagnostic programs, any memory test program run on other types of Altair 8800b compatible memory boards can also be used on the 88-16MCD board.

The most difficult part of memory troubleshooting is identifying the type of failure (i.e. addressing, data, refresh, etc.). Different failures can cause similar indications on the front panel. Thus, the major areas of memory function are grouped according to failure symptoms.

First, eliminate the possibility of mechanical failure by checking for broken etches, open feed-throughs, solder bridges, pins not in holes, etc., before assuming that a component is defective.

Except where otherwise specified, the system should remain in the Stop mode, with necessary data and address line switching done from the front panel.

3-2. Voltage Check

Always check the three voltages used by the 88-16MCD memory board as a first step in troubleshooting.

Referring to Figure 2-1(88-16MCD Schematic, sheet 1 of 2), insure that the regulated output voltages are +15V (±5% tolerance) from the output of VR2, +5V(±5%) from the output of VR1 and -5V(±5%) at the anode of D1. Unregulated bus voltages (+8V, +18V and -18V) not within the ±5% tolerance range, can also cause random, intermittent memory failures.

Under no circumstances should the 88-16MCD board be powered up without -5V supplied to pin 1 of each RAM IC. Operating without -5V for more than five seconds can affect the long-term reliability of the RAMs.

3-3. Addressing

A. Failure Symptom #1

1) 88-16MCD board cannot be selected
2) cannot deposit or examine any address on board
3) all data LED's are On

Possible Failure Area #1

1) Check for jumper inserted between pads W1 and W2.
2) Check decoding of address lines A14 and A15 through IC V, IC R and SW-1.
3) When board is selected, IC X pin 1 will be LOW. Check $\overline{CAS}$ at IC H pin 12 for double negative going pulses when board is selected (Figure 3-1).
4) Unselected board will have single negative going pulse (Figure 3-2).
5) Check TP-3 for 80 to 90ns pulse (Figure 3-3).

B. Failure Symptom #2

1) 88-16MCD board can be selected.
2) One or more 4K blocks within the board cannot be selected.

Possible Failure Area #2

1) Check decoding of address lines A12 and A13 through IC V, IC R, IC K and IC F.
2) Pin 4 ($\overline{RAS}$) of all 8 RAMs in any 4K block will have double negative going pulses when that block is selected (Figure 3-4).
3) Unselected blocks will have a single negative going pulse (Figure 3-5).
4) Only one block should be selected for any given state of A12 and A13.

C. Failure Symptom #3

1) All blocks can be selected.
2) Certain addresses within each block cannot be selected.

Possible Failure Area #3

1) Check IC S and IC W, pins 1 and 15, for enabling pulses (Figures 3-6 through 3-11).
2) Check the outputs of IC S. They should toggle from LOW to HIGH when the corresponding address switch (AØ-A5) is raised and examined.
3) Follow the same procedure (2) with IC W and address switches A6-A11. Note that the output of IC W does not change levels but adds pulses as the address switches are raised and examined.

3-4. Write Circuitry Check

To check the Write circuitry, compare the signal at pin 3 of any RAM with the MWRITE signal at IC Y pin 3. MWRITE should appear as a positive going pulse approximately 120µs in duration each time the deposit switch is toggled. The pulse at RAM pin 3 should be the exact inverse of the MWRITE pulse. This pulse is difficult to capture on most non-storage scopes, so be persistent. Do not attempt to sync it; just verify that it is getting through to the RAMs.

Also verify that any data bits deposited from the front panel appear at pin 2 of its respective RAM.

3-5. Read Circuitry Check

Check the Read circuitry by looking at PDBIN at IC Y pin 9 with the machine in the Run mode. A command or program does not have to be entered. The signal at IC U pin 8 should appear identical to PDBIN aside from minor amplitude variations (Figure 3-12). The signal at IC U pin 12 should also appear similar to PDBIN, except that each positive pulse is less than half the duration of each positive PDBIN pulse (Figure 3-13). This occurs since Ø2 is gated into pin 1.

The final portion of the Read circuitry, consisting of IC Z, can be checked only if the Address and Refresh logic is functioning properly. Stop/Reset the machine and examine the first address on the board. The signal at TP-5 should appear at IC Z pin 11 (Figure 3-14). IC Z pin 13 should be HIGH and pin 1 should be LOW. Each RAM D1 line (pin 2), DØ line (pin 14) and the output lines of IC Z should follow their respective data switch setting each time the deposit switch is toggled. This check will also indicate bad RAM's.

Faulty RAM's can also be detected on the front panel, appearing as a constant HIGH in one bit position of one 4K block when all 0's are deposited. If all 1's are deposited, a constant LOW will appear. Always verify that all pins of a suspect RAM are receiving proper signals before assuming the RAM is bad.

3-6. Refresh Circuitry Check

A. The first possible Refresh failure can affect all addresses on the board and is easily detected on the front panel by depositing 0's to any address on the board. A few seconds after depositing the 0's, random data bits will appear on the front panel data display. Pin 14 of the RAMs, whose data bits are HIGH on the front panel, will be at a tri-state level of approximately +2V (Figures 3-15 through 3-17). This is interpreted as a HIGH by IC Z and passed to the system data in bus, causing the front panel data LED's to illuminate.

Check TP-6 (Figures 3-18 and 3-19), TP-7 (Figures 3-20 and 3-21), TP-9 (Figure 3-22) and TP-10 (Figure 3-23). If the failure is solid, the problem can be detected at one of these points. Note that TP-9 will have a signal only in the Stop mode. It should be a steady LOW when the machine is running. TP-10 will typically have a leading edge to leading edge pulse period of 14 to 15μs and should never be greater than 16μs. Any discrepancies can be caused by timing components R7, R8 or C9 out of tolerance or a defective IC P.

While switching the machine back and forth between Stop and Run several times in succession, look at TP-6. The pulse period at TP-6 will vary from 10 to 12μs in the Run mode and 14 to 15μs in the Stop mode. Any complete loss of the pulses while switching is usually caused by problems in the string of gates feeding IC E pin 3.

B. The second type of Refresh failure only affects certain addresses in a repetitive pattern. This type is usually caused by problems with IC G or IC L.

IC G pin 12 should be a symmetrical square wave with a typical period of 28 to 30μs or one half the frequency of the pulse period at TP-6. Pin 11 should be one half the frequency of pin 12, pin 9 one half the frequency of pin 11, and so on through all six outputs.

To check the operation of IC L, Stop/Reset the machine and examine the first address on the board. IC L pins 1 and 15 should be receiving enable pulses, the inverse of TP-6 (Figure 3-24). With one channel of the scope, sync on IC L pin 10, and with the second channel look at pin 9. For every positive pulse on pin 10, there should be one positive pulse on pin 9 (Figure 3-25).

Check the remainder of the IC L gates in the same manner. Pin 11 will have two positive pulses for each positive pulse on pin 12. Pin 13 will have four pulses for each one on pin 14 (Figure 3-26). Pin 3 will have eight pulses, pin 5 will have sixteen pulses, and pin 7 will have thirty-two pulses (Figure 3-27).

$\overline{CAS}$ - TP-8 Board Selected
2v/Div. Vertical
.1μs/Div. Horizontal

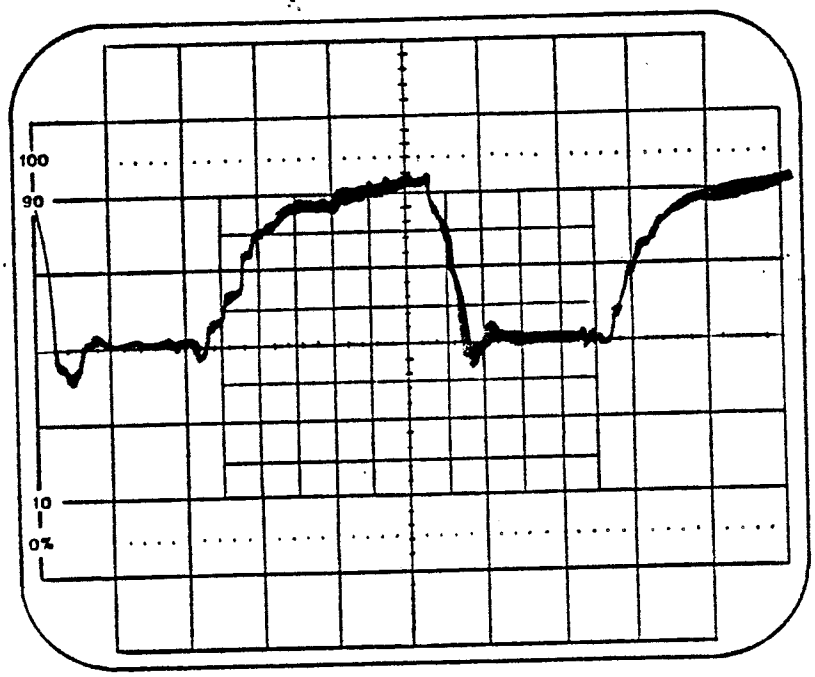


Figure 3-1

$\overline{CAS}$ - TP-8 Board Unselected
2v/Div. Vertical
.1μs/Div. Horizontal

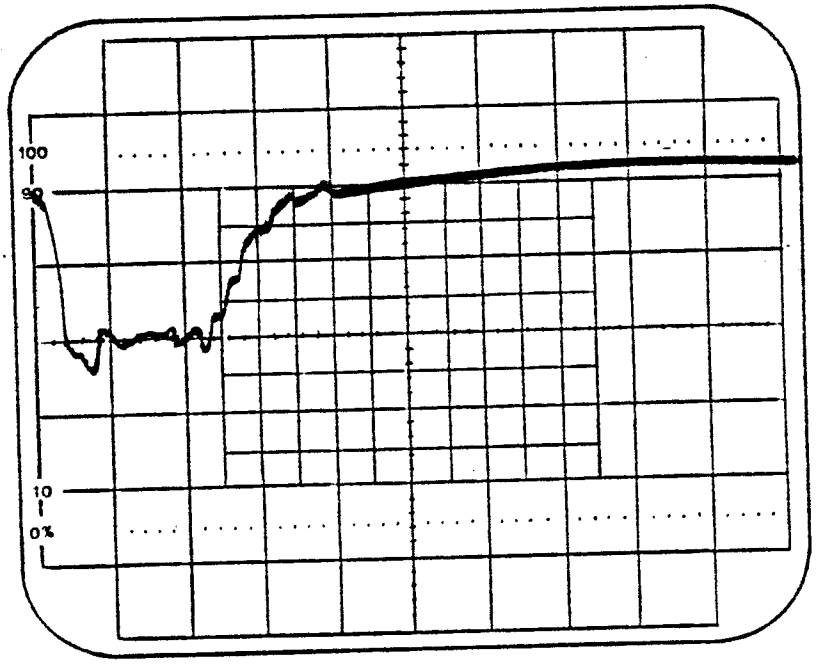


Figure 3-2

TP-3 Stop Mode Only
Board Selected or Unselected
2v/Div. Vertical
.1μs/Div. Horizontal

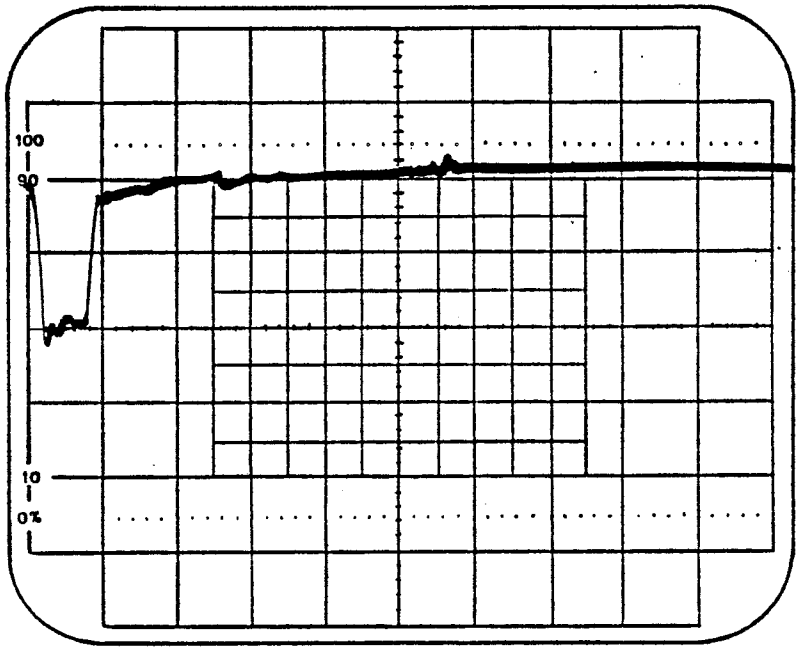


Figure 3-3

$\overline{RAS}$ - TP-4 Block Selected
2v/Div. Vertical
.1μs/Div. Horizontal

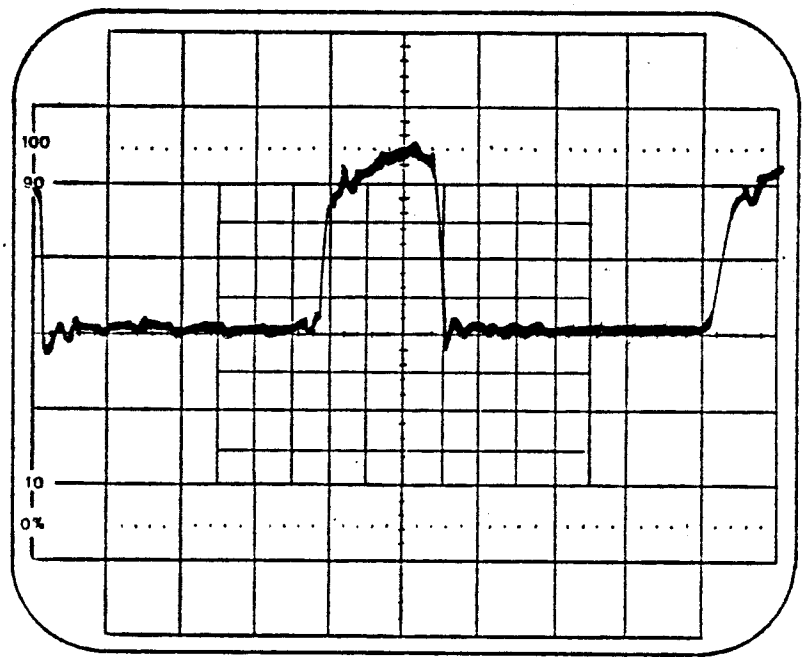


Figure 3-4

$\overline{RAS}$ - TP-4 Block Unselected
2v/Div. Vertical
.1μs/Div. Horizontal

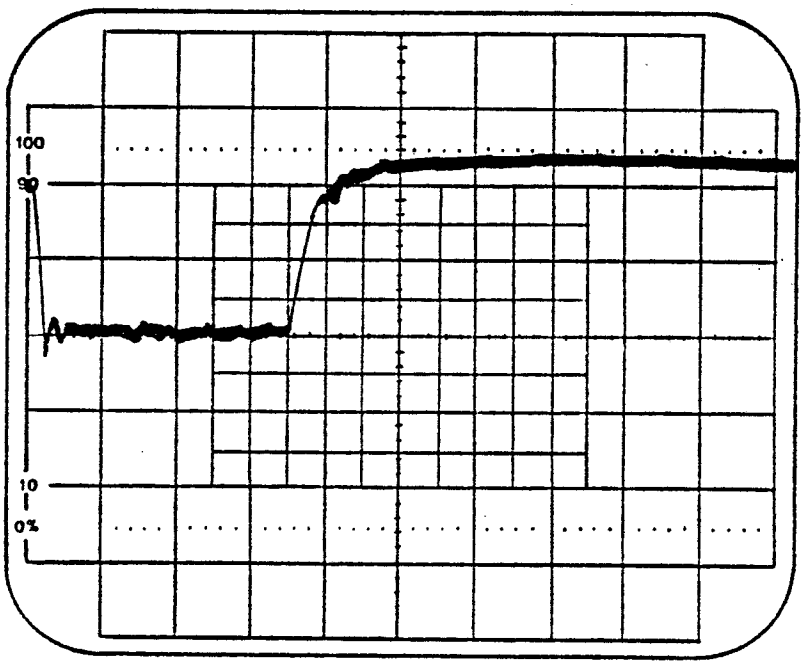


Figure 3-5

A-8 TP-1 Address Select Clock
A-3 TP-2 RAS Enable
2v/Div. Vertical
.1μs/Div. Horizontal

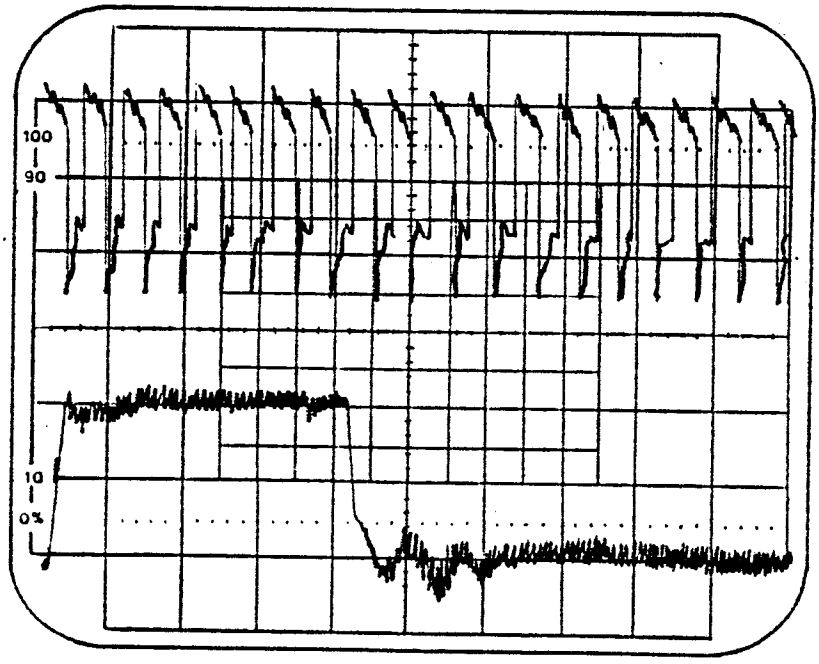


Figure 3-6

IC-W Pins 1 + 15
IC-S Pins 1 + 15
2v/Div. Vertical
.1µs/Div. Horizontal

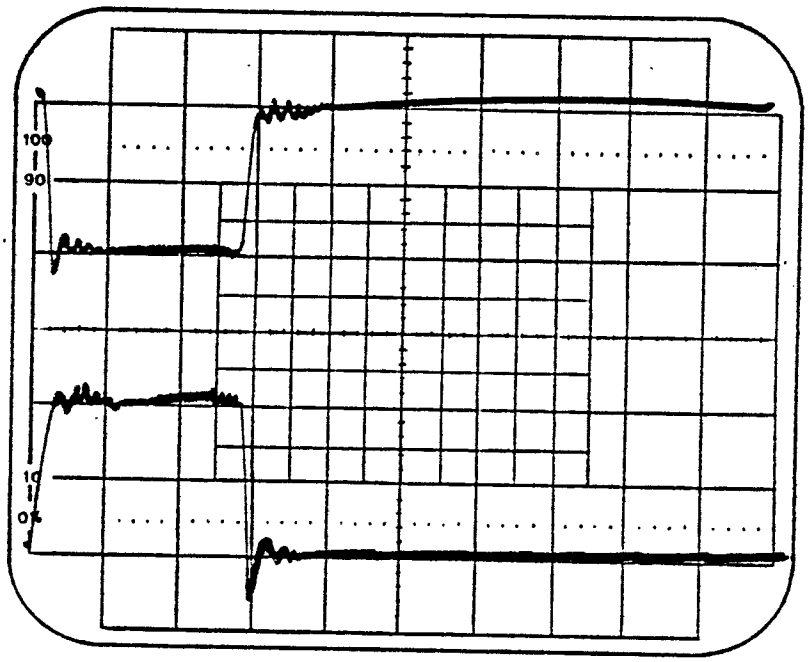


Figure 3-7

IC-S Pin 3
Address Line AØ LOW
2v/Div. Vertical
5µs/Div. Horizontal

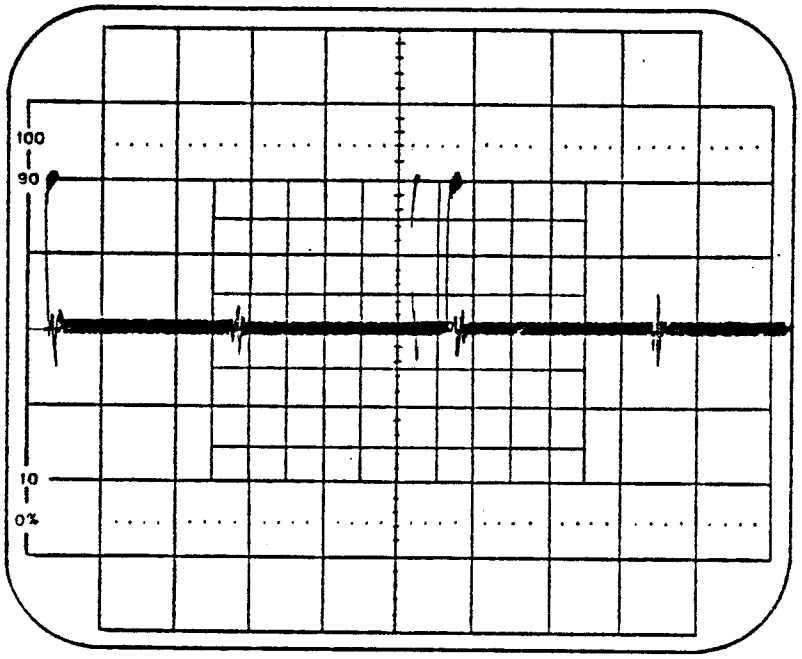


Figure 3-8

IC-S Pin 3
Address Line AØ HIGH
2v/Div. Vertical
5µs/Div. Horizontal

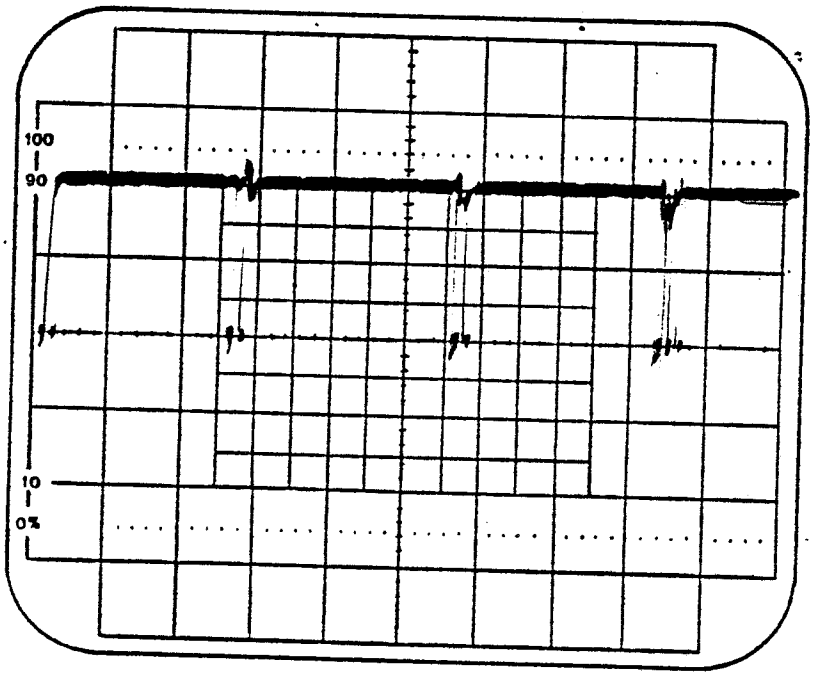


Figure 3-9

IC-W Pin 3
Address Line A6 LOW
2v/Div Vertical
5µs/Div. Horizontal

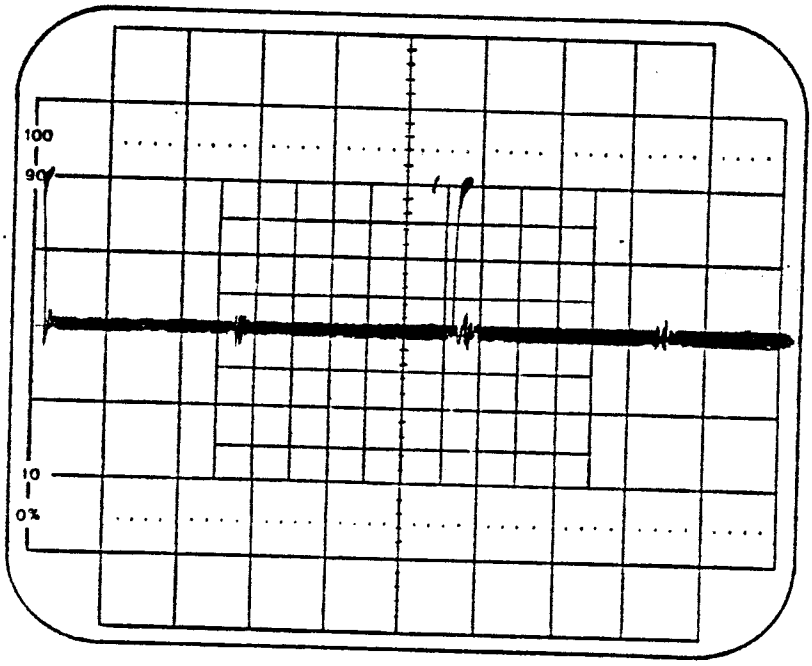


Figure 3-10

IC-W Pin 3
Address Line A6 HIGH
2v/Div. Vertical
5µs/Div. Horizontal

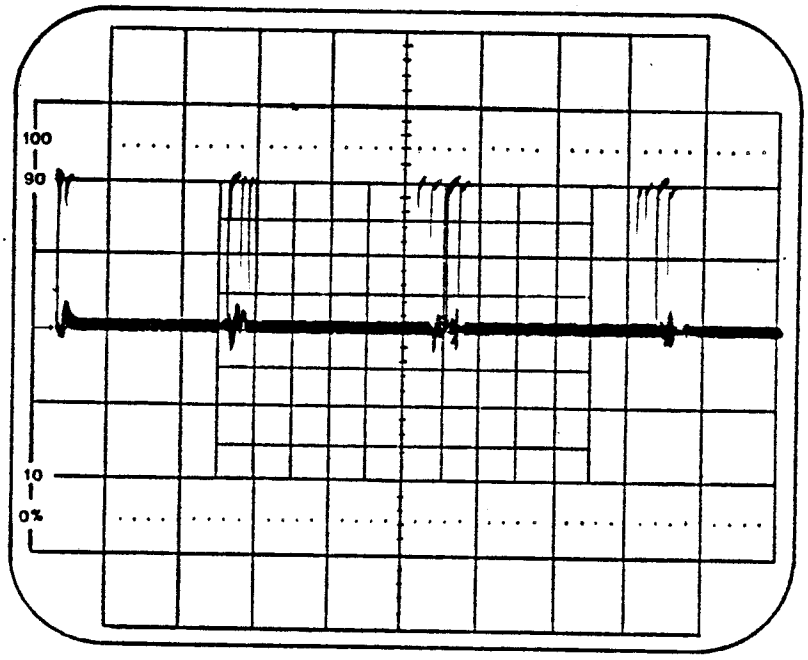


Figure 3-11

IC-Y Pin 9 PDBIN Run Mode
IC-U Pin 8
2v/Div. Vertical
.5µs/Div. Horizontal

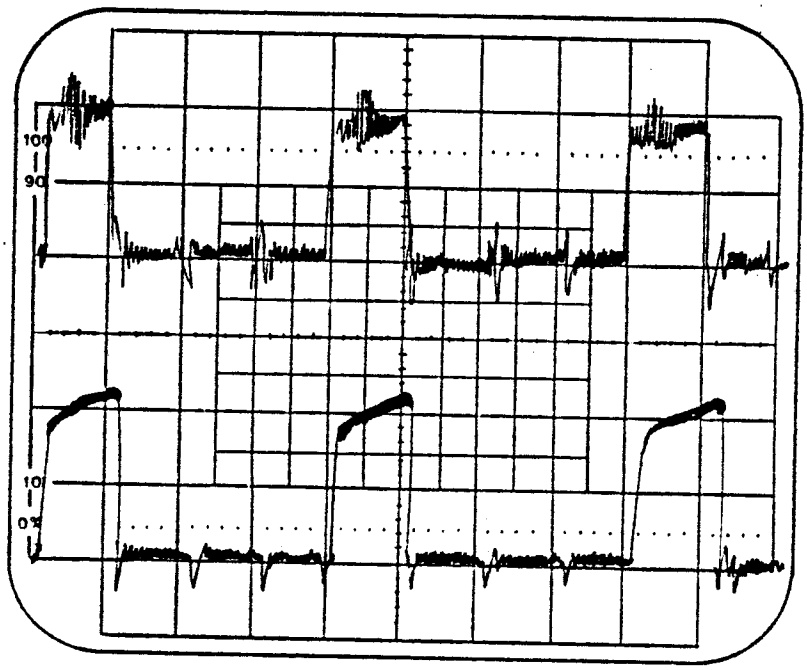


Figure 3-12

IC-Y Pin 9 PDBIN Run Mode
IC-U Pin 12
2v/Div. Vertical
.5us/Div. Horizontal

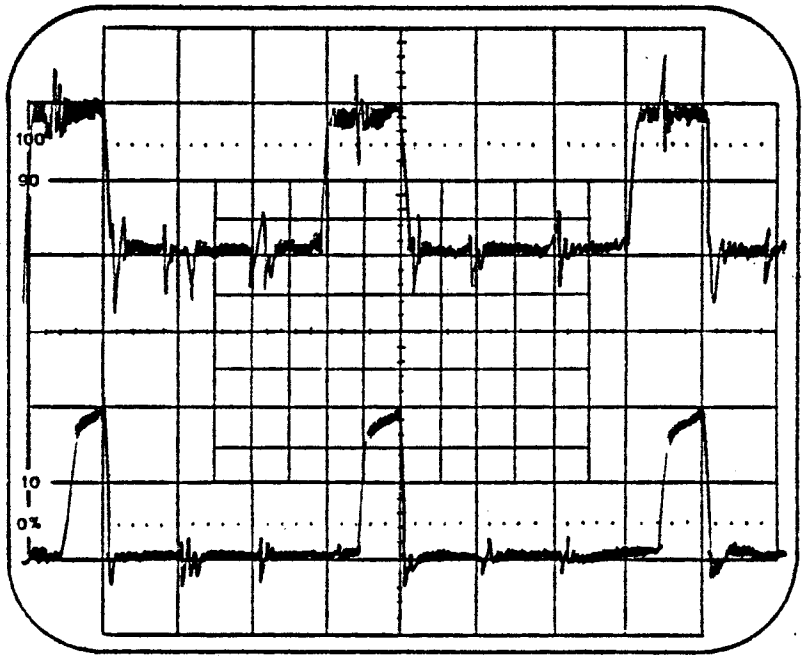


Figure 3-13

TP-5, IC-Z Pin 11 Stop Mode
2v/Div. Vertical
.5us/Div. Horizontal

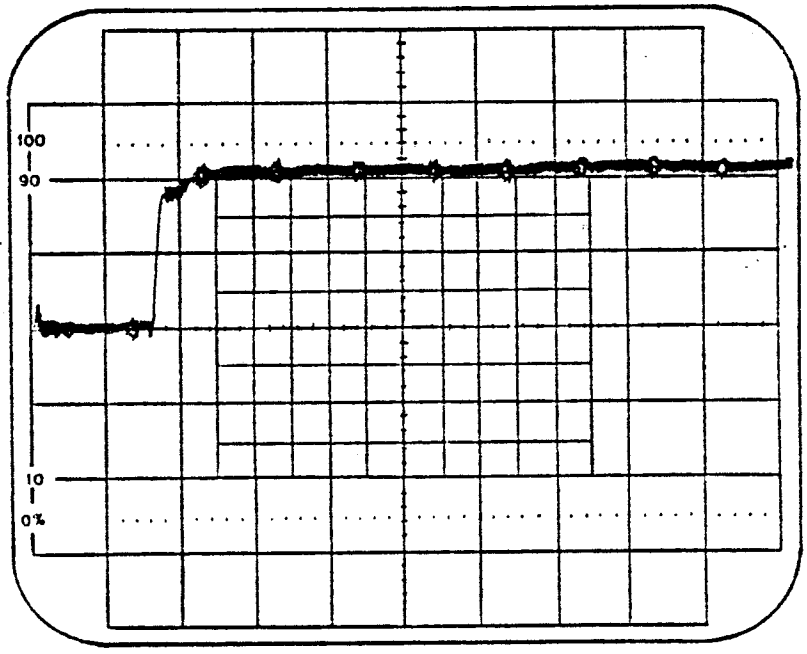


Figure 3-14

Pin 14 of any selected RAM IC
Data bits equal zero
0 volts
2v/Div. Vertical
5µs/Div. Horizontal

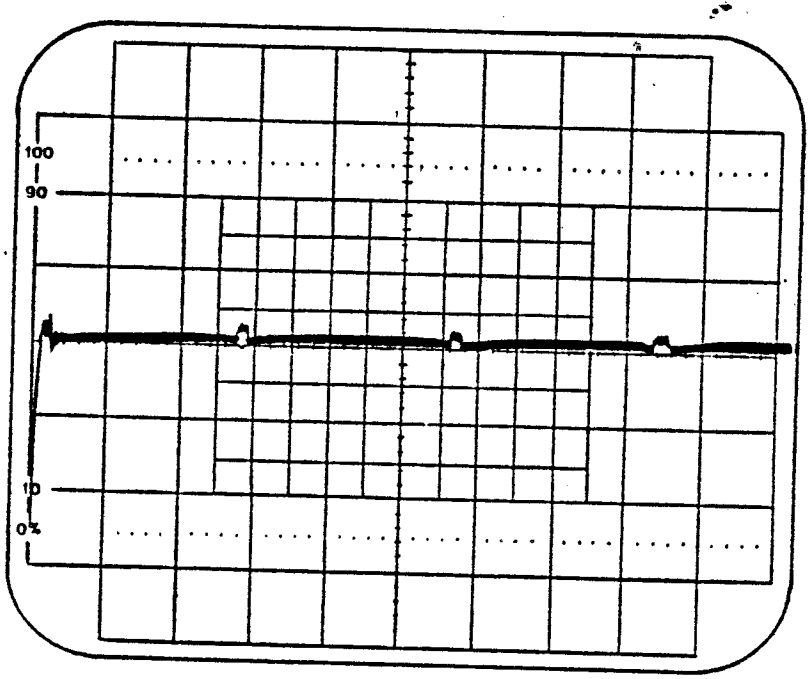


Figure 3-15

Pin 14 of any selected RAM IC
Data bits equal one
5 volts
2v/Div. Vertical
5µs/Div. Horizontal

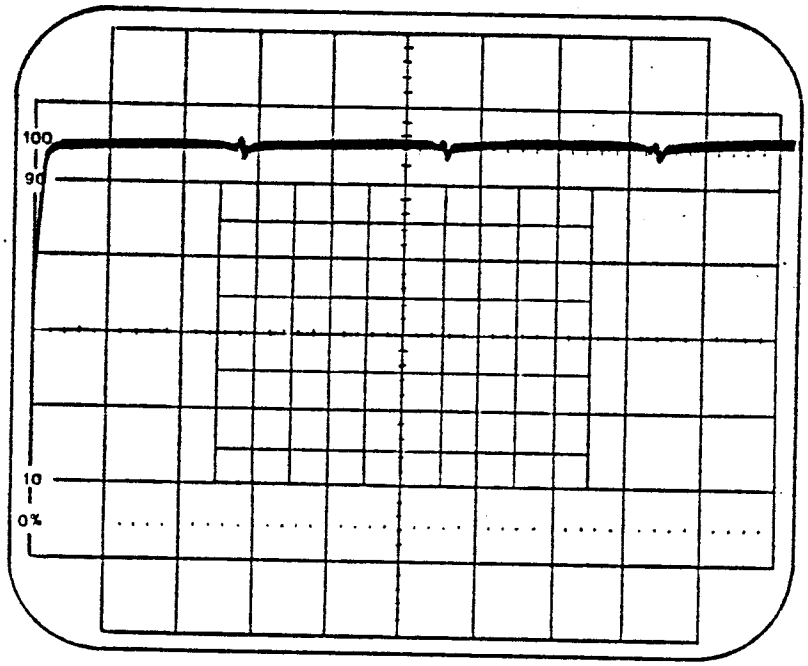


Figure 3-16

Pin 14 of RAM unselected; or
selected but refresh inoperative.
2 volts
2v/Div. Vertical
5μs/Div. Horizontal

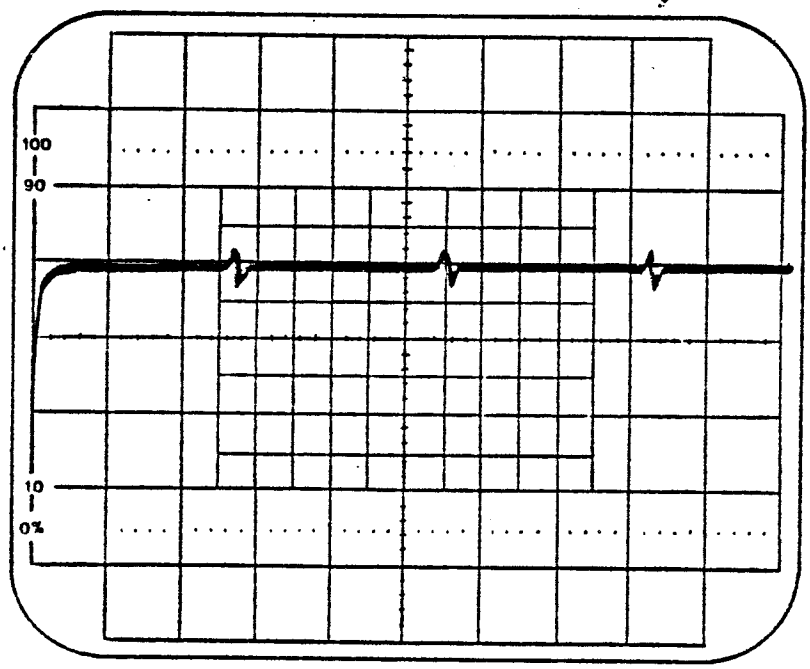


Figure 3-17

TP-6 Stop Mode
2v/Div. Vertical
2μs/Div. Horizontal

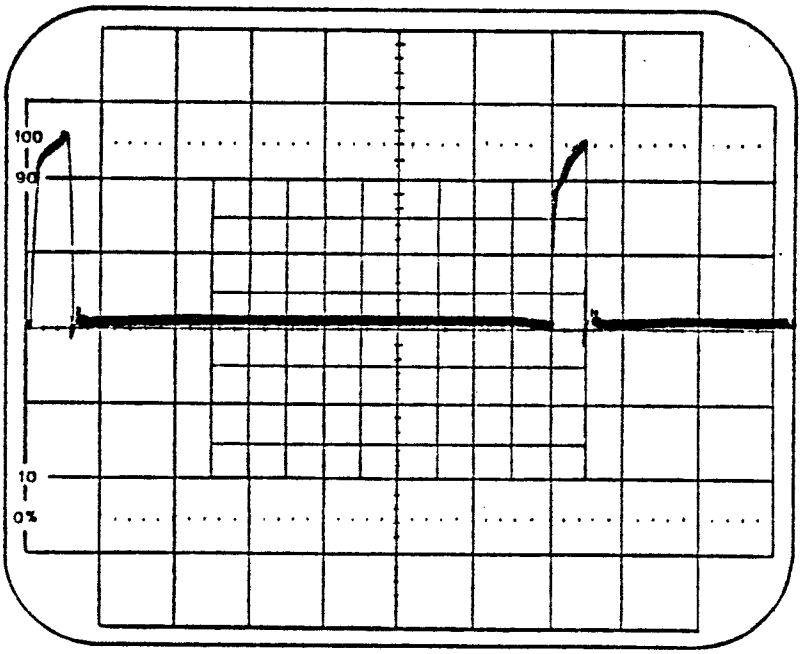


Figure 3-18

TP-6 Run Mode
2v/Div. Vertical
2μs/Div. Horizontal

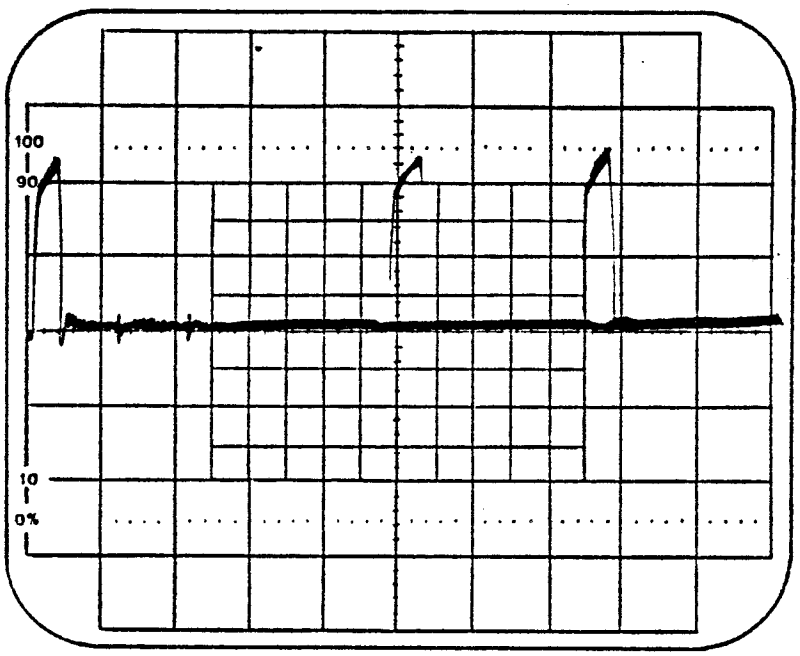


Figure 3-19

E-3 TP-7
Refresh control clock
Stop Mode
2v/Div. Vertical
1μs/Div. Horizontal

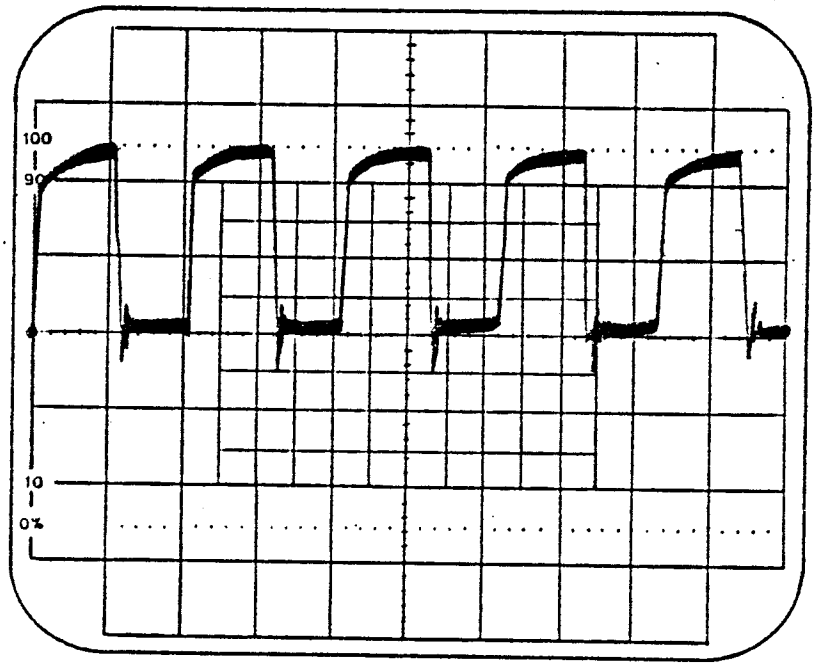


Figure 3-20

E-3 TP-7
Refresh control clock
Run Mode
2v/Div. Vertical
1μs/Div. Horizontal

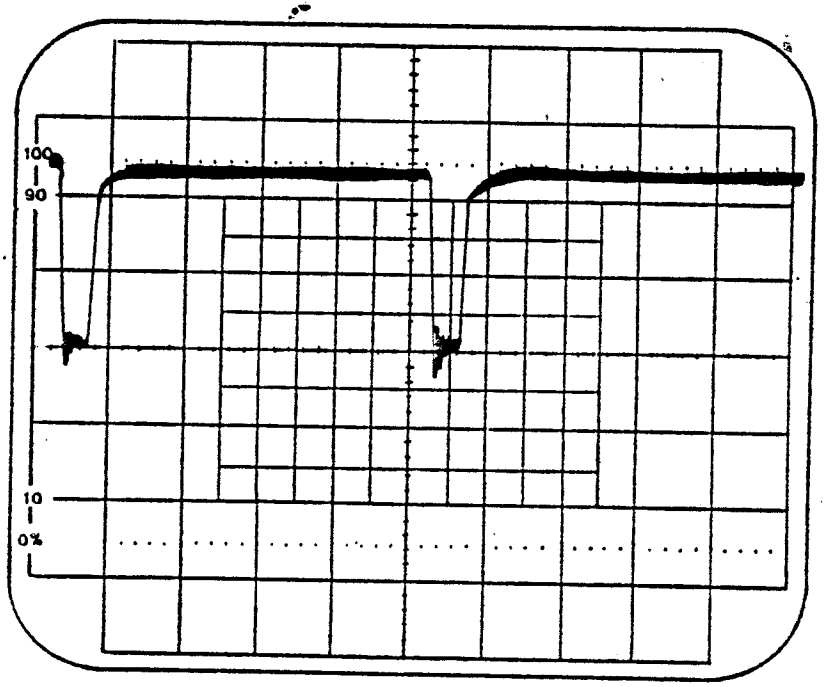


Figure 3-21

TP-9
Stopped Mode
2v/Div. Vertical
.5μs/Div. Horizontal

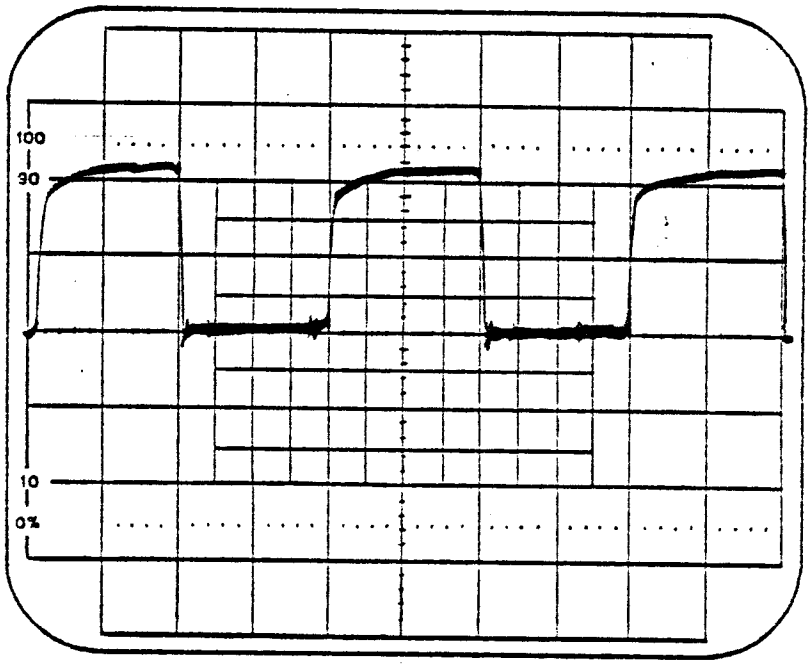


Figure 3-22

P-3 TP-10
Refresh master clock
2v/Div. Vertical
5μs/Div. Horizontal

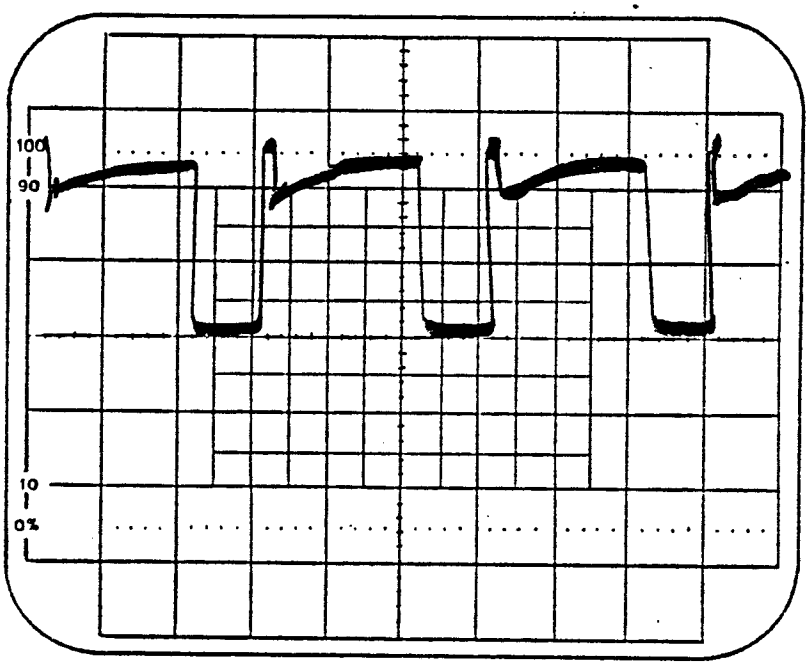


Figure 3-23

IC L pins 1 and 15
Stop Mode

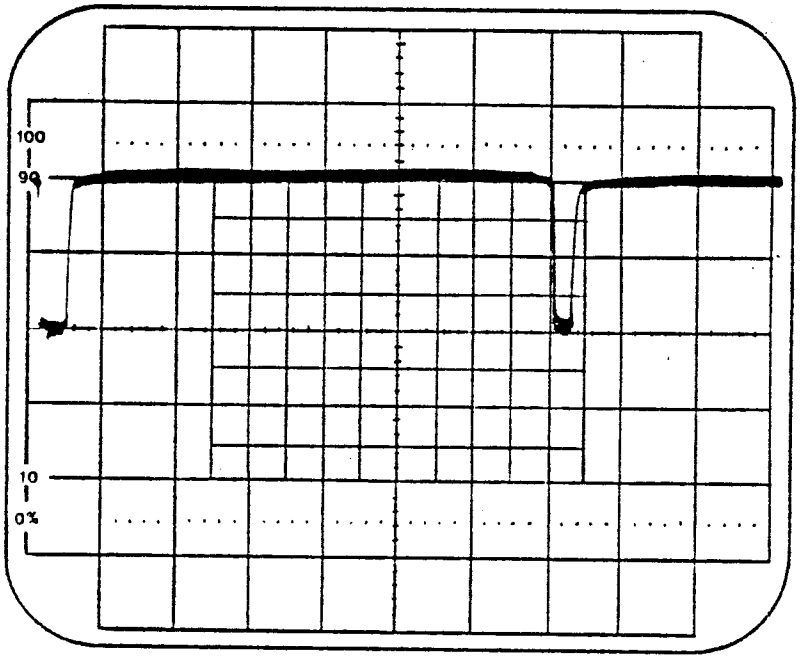


Figure 3-24

IC-L Pin 10
IC-L Pin 9
2v/Div. Vertical
5µs/Div. Horizontal

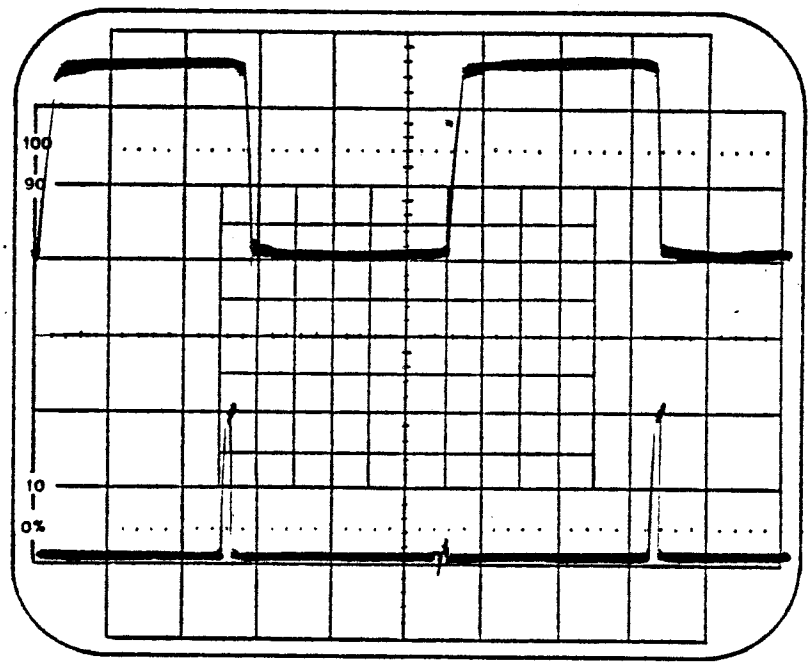


Figure 3-25

IC-L Pin 14
IC-L Pin 13
2v/Div. Vertical
20µs/Div. Horizontal

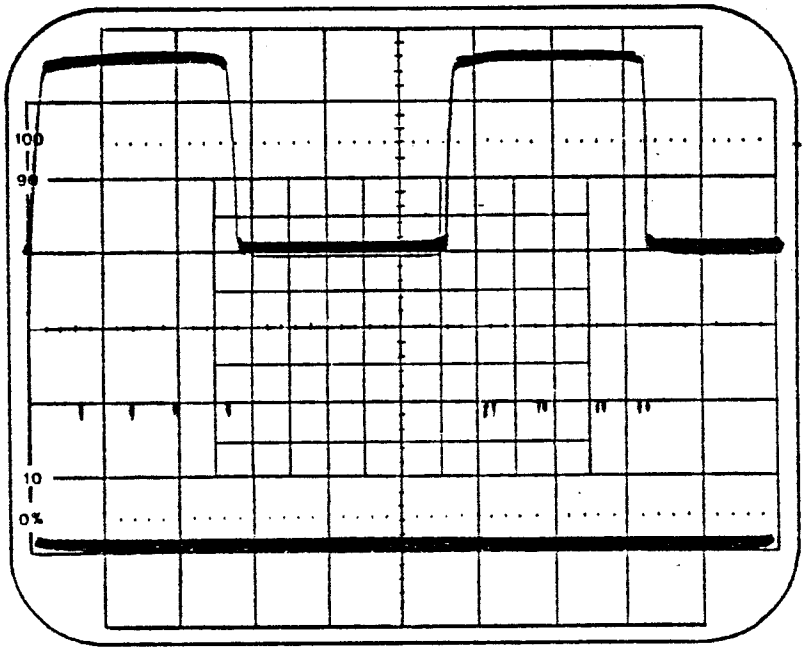


Figure 3-26

IC-L Pin 6
IC-L Pin 7
2v/Div. Vertical
100µs/Div. Horizontal

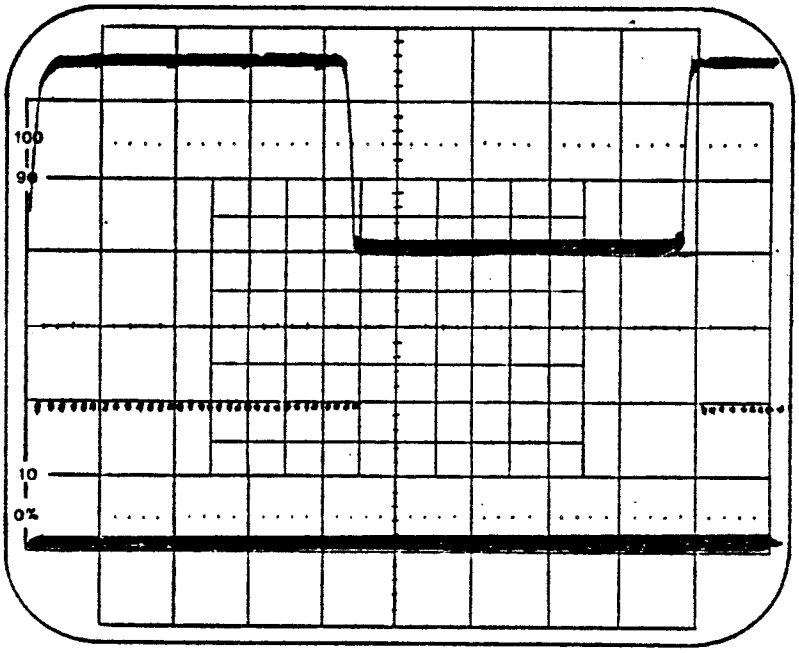


Figure 3-27

88-16MCD
SECTION IV
ASSEMBLY

4-1. INTRODUCTION

Section IV contains step-by-step instructions for component installation of the 88-16MCD 16K Dynamic Memory board.

Before beginning the assembly procedure, carefully read the enclosed "MITS Kits Assembly Hints booklet. It contains helpful suggestions and several important warnings. Failure to heed these warnings could cause you to void the warranty.

Check the contents of the kit using the parts list (Appendix A) to make sure all of the required components are enclosed. As you assemble the board, read each step carefully and follow the instructions in the order in which they are presented. Always complete each step before going on to the next. Under no circumstances should you proceed with an assembly step without fully understanding the procedures involved. A little patience at this stage will save a great deal of time and potential "headaches" later.

4-2. VISUAL INSPECTION

It is recommended that a visual inspection of the board be made before beginning the assembly procedures. A thorough inspection of this kind will eliminate one possibility for errors should the board fail to operate properly after it is assembled. Troubleshooting efforts may then be concentrated elsewhere.

Look for etching "bridges" or "opens" in the printed circuit lands, as shown ir Figure 4-1 below.

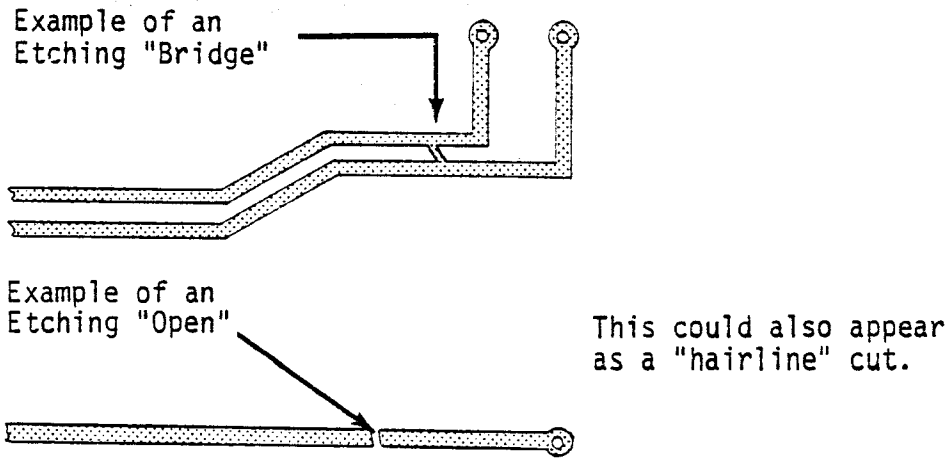


Figure 4-1. Visual Inspection

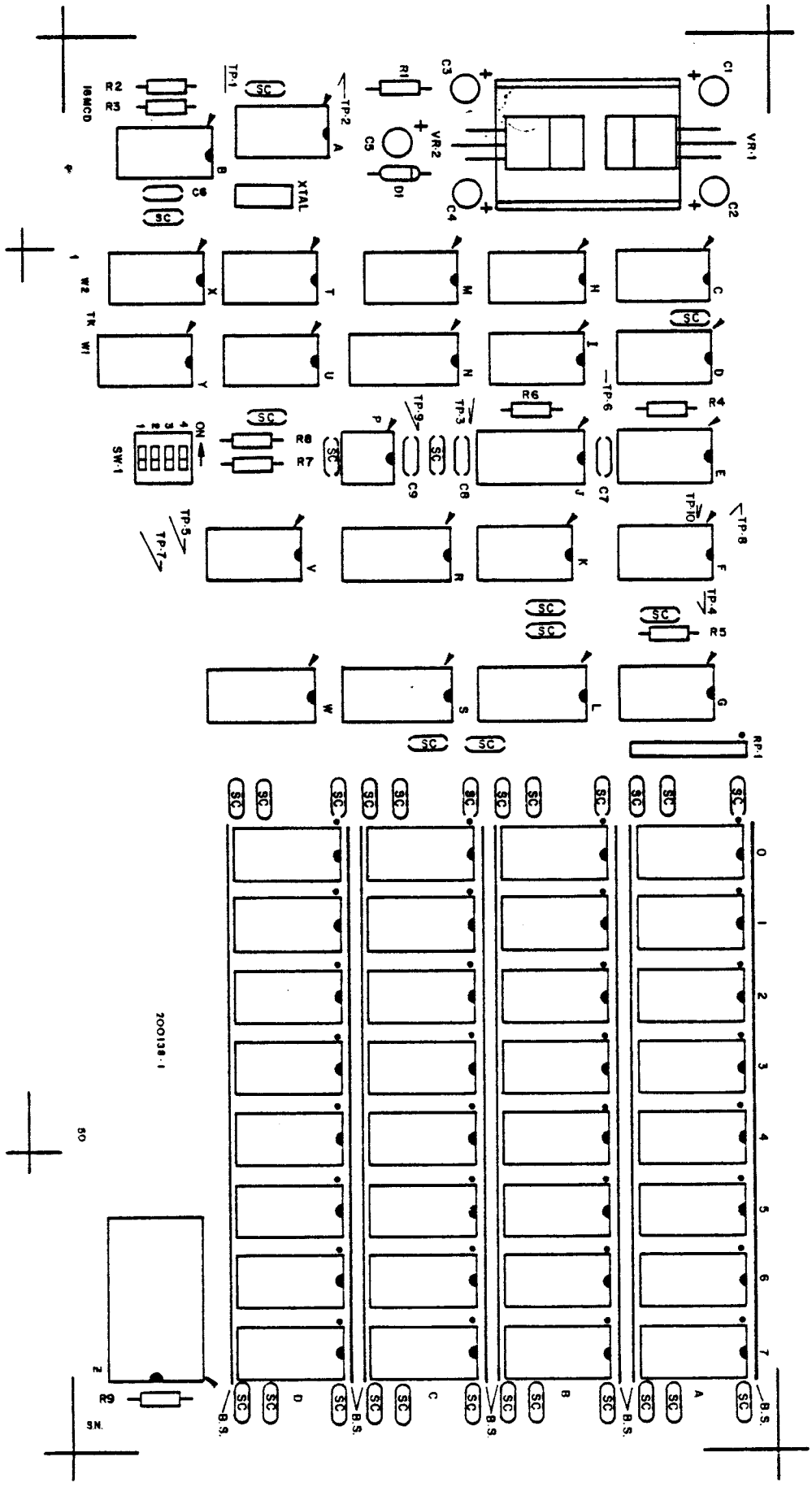


Figure 4-2. 88-16MCD Silkscreen

4-3. COMPONENT INSTALLATION INSTRUCTIONS

The following paragraphs describe the proper procedures for installing various types of components on the board. Read these instructions carefully, and refer to Figure 4-2, the 88-16MCD silkscreen when necessary. Failure to properly install components may cause permanent damage to the component or the rest of the unit; it will definitely void the warranty.

4-4. Diode Installation

Diodes are marked with a band on the cathode end. Each diode must be installed so that the cathode end is oriented towards the band printed on the PC board. Failure to correctly orient the diodes may result in permanent damage to the unit.

Use the following procedure to install diode D1 (Bag 4) onto the board. Refer to the list of diode part numbers included in the specific assembly instructions to make sure the correct diode is installed each time.

1. Bend the leads of the diode at right angles to match their respective holes on the board.
2. Make sure the cathode end is properly oriented, and insert the diode into the correct holes on the silkscreen. Secure the diode in place with masking tape.
3. Solder the the two leads to the foil pattern on the back of the board, and clip off any excess lead lengths.

Diode	Part Number
( ) D1	IN4733

4-5. Resistor Installation (Figure 4-3)

Resistors have four, or possibly five, color-coded bands as represented in Table 4-A. The fourth band is gold or silver in color and indicates the tolerance. When assembling MITS kits, you need only be concerned with the three bands of color to one side of the gold or silver (tolerance) band. These three bands denote the resistor's value in ohms. The first two bands correspond to the first two digits of the resistor's value and the third band represents a multiplier.

For example, a resistor with red, violet, yellow and silver bands has a value of 270,000 ohms and a tolerance of 10%. Refer to Table 4-A. Red denotes a value of 2 and violet, a value of 7. Multiply 27 by the yellow multiplier band (10,000) to arrive at a total value of 270,000 ohms (270K). The silver band denotes the 10% tolerance. Use this process to choose the correct resistor called for in the specific instructions.

Table 4-A. Resistor Color Codes

Color	Bands 1 & 2	3rd Band (Multiplier)
Black	0	1
Brown	1	10
Red	2	10^2
Orange	3	10^3
Yellow	4	10^4
Green	5	10^5
Blue	6	10^6
Violet	7	10^7
Gray	8	10^8
White	9	10^9

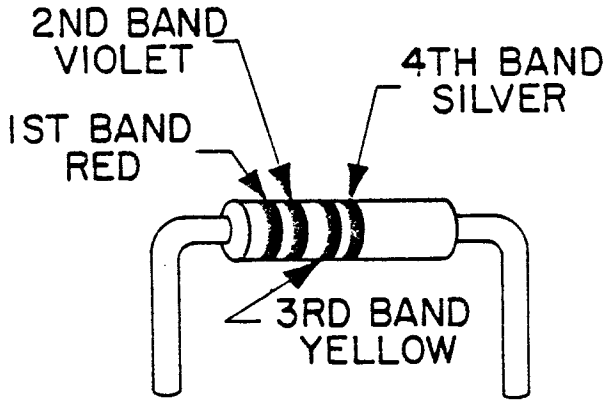


Figure 4-3. Resistor Color Codes

Make sure the colored bands on each resistor match the colors called for in the list of resistor values and color codes given below. When the correct value resistor has been selected, install the nine (R1 through R9, Bag 4) according to the following instructions:

1. Using needle-nose pliers, bend the leads of the resistor at right angles to match their respective holes on the board.
2. Install the resistor into its correct holes on the silk-screened side of the board, and secure in place with masking tape.
3. Solder the leads to the foil pattern on the back of the board, and clip off any excess lead lengths.

To install the resistor pack (RP-1, Bag 4), follow the instructions below:

1. The resistor pack has a small dot at one end. The two leads farthest from this dot should be clipped off.
2. The dot on the resistor pack corresponds to a small dot on the board. Align these dots and insert RP-1 into the silk-screened side of the board.
3. Solder each pin to the foil (bottom) side of the board. Be careful not to leave any solder bridges and clip off any excess lead lengths.

Resistor	Value	
( ) R1	1.3K ohm, 1/2W	(Brown, Orange, Red)
( ) R2, R3	330 ohm, 1/2W	(Orange, Orange, Brown)
( ) R4, R7	10K ohm, 1/2W	(Brown, Black, Orange)
( ) R5, R6	5.1K ohm, 1/2W	(Breen, Brown, Red)
( ) R8	5.6K ohm, 1/2W	(Green, Blue, Red)
( ) R9	1K ohm, 1/2W	(Brown, Black, Red)
( ) RP-1	1K ohm, 1/2W	

4-6. Capacitor Installation

There are 44 capacitors to be installed on the 88-16MCD board. C1 through C5 (Bag 5) are tantalum capacitors, and C6 through C10 (Bag 5) are ceramic disk capacitors. The remaining 34 capacitors (Bag 6), used for noise suppression, are epoxy dipped.

A. Polarity must be noted on tantalum capacitors before they are installed.

Tantalum capacitors are marked with "+" signs on the positive side as shown in Figure 4-4.

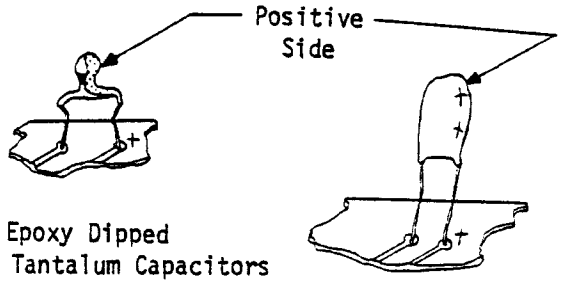


Figure 4-4. Epoxy Dipped Tantalum Capacitors

Install the 5 tantalum capacitors (Bag 5) according to the following instructions.

1. Bend the two leads of the capacitor at right angles to conform to their respective holes on the board.
2. Insert the capacitor into the holes on the silk-screened side of the board, aligning the positive side with the "+" signs printed on the board. Secure the capacitor in place with masking tape.
3. Solder the leads to the foil pattern on the back of the board. Clip off any excess lead lengths.

Capacitor	Value
( ) C2, C4, C5*	22µf, 16V, tantalum
( ) C1, C3	22µf, 35V, tantalum

*C5 is not labelled on the board. It is located between R1 and D1.

B. Ceramic Disk and Epoxy Dipped Ceramic Capacitors

Ceramic disk and epoxy dipped capacitors are non-polarized and are shown in Figure 4-5.

Figure 4-5. Ceramic Disk and Epoxy Dipped Ceramic Capacitors

Install the 5 ceramic disk (Bag 5) and 34 epoxy dipped (Bag 6) capacitors according to the following procedure.

1. Bend the two capacitor leads to conform to their respective holes on the board.
2. Insert the capacitor into the correct holes from the silk-screened side of the board, and secure with masking tape.
3. Solder the leads to the foil (bottom) side of the board. Clip off any excess lead lengths.

Capacitors	Value
( ) C6	180 pf, 1KV, ceramic disk
( ) C7	200 pf, 1KV, ceramic disk
( ) C8	10 pf, 16V, ceramic disk
( ) C9	820 pf, 1KV, ceramic disk
( ) C10*	.01 µf, 16V-20V, ceramic disk

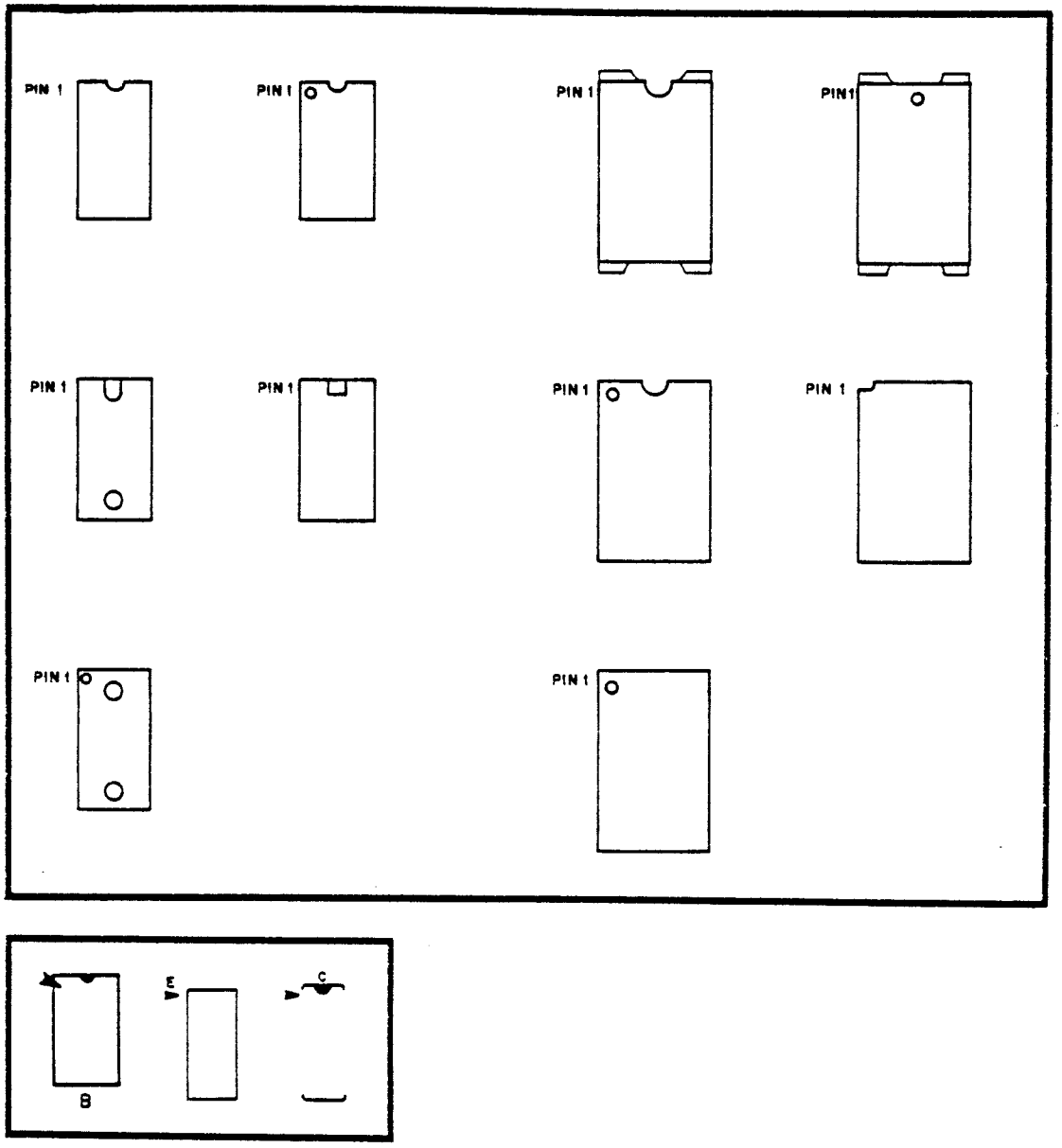
*C10 is not labelled on the board. It is located directly below IC P and is labelled "SC."

( ) 34 suppressor capacitors µf, 50V, epoxy dipped labelled "SC"

4-7. IC Identification

Integrated circuits may have any one, or a combination of, several different markings which are used to determine correct orientation when the ICs are placed on the printed circuit board. Refer to Figure 4-6 to locate pin 1 of the ICs.

Figure 4-6a indicates the various methods used to show the position of ICs on the printed circuit board. These outlines are silk-screened directly on the board. The arrowhead indicates the pin 1 position.



Figures 4-6 and 4-6a. IC Identification Chart

4-8. IC and Socket Installation

There are 24 ICs (Bag 1) to be installed on the 88-16MCD board. All ICs must be oriented so that pin 1 corresponds with the pad marked with an arrowhead. Refer to the IC identification chart in Paragraph 4-7 to identify pin 1. All ICs are easily damaged and should be handled carefully. Always try to hold the IC by the ends and avoid touching the pins as often as possible. When removing the IC from its holder, carefully straighten any bent pins using needle-nose pliers. All pins should be evenly spaced and should be aligned perpendicular to the body of the IC itself.

A. Installing ICs without sockets

1. Orient the IC so that pin 1 coincides with the arrowhead on the PC board.
2. Align the pins on one side of the IC so that just the tips are inserted into their holes on the board.
3. Lower the other side of the IC into place. If the pins do not go into their holes right away, rock the IC back, exert a little inward pressure, and try again. Be patient. The tip of a small screwdriver may be used to help guide the pins into place. When the tips of all of the pins have been started into their holes, push the IC into the board the rest of the way. Tape the IC to the board with masking tape.
4. Solder each pin to the foil pattern on the back of the board. Be careful not to leave any solder bridges. Clip off any excess lead lengths, and remove the masking tape.

IC	Part Number
( ) A	74LS164
( ) B	74S04
( ) C,E	74LS74
( ) D	74LS20
( ) F,I	74LS32

( ) G	C04024 (MC14024 or CD14024)
( ) H	7404
( ) J	74LS123
( ) K	74LS08
( ) L,S,W	8t97
( ) M	74LS55
( ) N	74LS112
( ) R	74LS139
( ) T,Y,V	74L04
( ) U	74LS27
( ) X	74LS04

B. Installing ICs with sockets

ICs P and Z (Bag 1) are installed with sockets (Bag 3) according to the following instructions.

1. Refer to the drawing below, and orient the socket so that pin 1 coincides with the arrowhead on the board. Set the socket into its holes, and secure with masking tape.

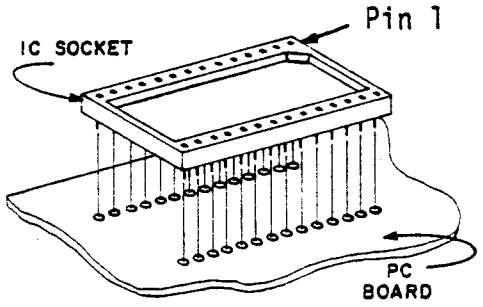


Figure 4-7. Installing ICs With Sockets

2. Solder each pin to the foil pattern on the back of the board. Be careful not to leave any solder bridges. Clip off any excess lead lengths, and remove the masking tape.
3. Orient the IC over the socket so that pin 1 coincides with pin 1 on the socket.
4. Align the pins on one side of the socket so that just the tips are inserted into the holes.
5. Lower the other side of the IC into place. If the pins don't go into their holes right away, rock IC back, exert a little inward pressure, and try again. Be patient. When the tips of all of the pins have been started into their holes, push the IC into the socket the rest of the way.

IC	Part Number	Socket Size
( ) P	555	8-Pin
( ) Z	8212	24-Pin

4-9. MOS IC Installation

There are 32 MOS ICs (Bag 2) with sockets (Bag 3) to be installed on the 88-16MCD board. MOS ICs are extremely sensitive to static electricity and transient voltages. In order to prevent damaging these components, read the following precautions and adhere to them as closely as possible. Failure to do so may result in permanent damage to the IC.

1. All equipment (soldering iron, tools, solder, etc.) should be at the same potential as the PC board, the assembler, the work surface, the IC itself and its container. This can be accomplished by continuous physical contact with the work surface, the components and everything else involved in the operation.
2. When handling the IC, develop the habit of first touching the conductive container in which it is stored before touching the IC itself. If the IC has to be moved from one container to another, touch both containers before doing so.
3. Do not wear clothing that will build up static charges. Cotton is preferable to wool or synthetic fibers.
4. Always touch the PC board before touching the IC to it. Try to maintain this contact as often as possible when installing the IC.
5. Handle the IC by the edges. Avoid touching the pins themselves.
6. Dry air moving over plastic can build up considerable static charges. Avoid placing the IC near any such area or object.

Install the 32 MOS ICs with sockets according to the instructions in Paragraph 4-8, Section B.

IC	Socket Size
( ) 32 MOS IC	16-Pin

4-10. Switch Installation

Install the 8-pin dip switch (SW-1, Bag 3) according to the following instructions.

1. Remove the switch from its holder, and straighten any bent pins with needle nose pliers.
2. Orient the switch so that the numbers 1,2,3,4 are towards IC Y on the board.
3. Start the pins on one side of the switch into their respective holes on the silk-screened side of the board. Do not push the pins in all the way. If it is difficult to insert the pins into their holes, guide them with the tip of a small screwdriver.
4. Start the pins on the other side of the switch into their holes in the same manner. When all 8 pins have been started, push the switch into place by gently rocking it back and forth until it rests as close as possible to the board. Secure the switch in place with masking tape.
5. Solder each pin to the foil pattern on the back of the board. Be careful not to leave any solder bridges. Clip off any excess lead lengths.

Switch	Part Number
( ) SW-1	76-B04

6. Refer to Paragraph 2-1 in the 88-16MCD Theory of Operation Section for addressing information.

4-11. Crystal Installation

There is one 20 MHz crystal (XTAL, Bag 7) to be installed on the 88-16MCD board.

1. Set the crystal in place on the silk-screened side of the baord, aligning the two leads with their respective holes.
2. Insert the leads so that the crystal is resting flat on the board.
3. Solder the two leads to the foil (bottom) side of the board. Be sure not to leave any solder bridges.
4. Clip off any excess lead lengths.

Silkscreen Designation
( ) XTAL

4-12. Voltage Regulator Installation

Install two voltage regulators (VR1 and VR2, Bag 1) with large heat sink (Bag 7) according to the following instructions.

1. Set the regulators in place on the silk-screened side of the board, aligning the leads with their designated holes.
2. Use needle-nose pliers to bend each of the three leads at a right angle to conform to its proper hole on the board.

NOTE
Use heat sink grease when installing this component. Apply the grease to all metal surfaces that come into contact with each other.

3. Set both regulators and heat sink in place on the silk-screened side of the board. Secure them each in place with a #6-32 x 3/8 inch screw, a #6-32 nut and a #6 lockwasher (Bag 7).
4. Solder the leads to the foil pattern on the back of the board. Be sure not to leave any solder bridges.
5. Clip off any excess lead lengths.

Voltage Regulator	Part Number
( ) VR1	7805
( ) VR2	7815

4-13. Buss Strip Installation

There are 8 buss strips (Bag 7) to be installed on the 88-16MCD board. The buss strips are to be inserted on each side and in between the MOS ICs. They are denoted by long lines on the silk-screen side of the board.

1. Insert the 16 leads of the buss strip into the silk-screen side of the board. Solder each pin to the foil (bottom) side.
2. Be careful not to leave any solder bridges and clip off any excess lead lengths.

( ) 8 buss strips

4-14. Terminal Test Point Installation

Install 10 test points (TP1 through TP10, Bag 7) on the 88-16MCD board according to the following instructions.

1. Insert the pin through the silk-screened side of the board, and solder in place on the silk-screened side.
2. Turn the board over and solder the pin on the foil (bottom) side of the board.
3. Return the board to the silk-screened (top) side. Straighten the pin if necessary, and resolder.

NOTE
Do not clip off the portion of the test point that protrudes from the bottom of the board; it can be used during testing and troubleshooting.

Silkscreen Designation

( ) TP1-TP10

4-15. INSTALLATION OF BOARD INTO MAINFRAME

1. Before installing the 88-16MCD board, check the board for solder shorts, open lands and missing components.
2. Remove the four #6-32 x 3/8" screws (two on each side) from the computer case, and slide the case bottom forward so that the bottom of the motherboard is exposed.
3. Insert the 100-pin edge connector (Bag 7) into the motherboard so that pin 1 is in the lower right position (looking at the front of the computer).
4. Solder each pin to the bottom of the motherboard. Be careful not to leave any solder bridges. Clip off any excess lead lengths.
5. Slide the 88-16MCD board down through the card guides (Bag 7), and insert the card stab connector into the edge connector so that the silk-screened side is towards the right side of the computer.
6. Slide the case bottom back into place and replace the four #6-32 x 3/8" screws.

4-16. BURN-IN PROCEDURE

When assembly of the 88-16MCD board has been completed, we recommend that a "burn-in" procedure be performed to uncover possible malfunctions that may occur at this time. After the board has been installed, turn the unit on, and set the cover in place. Leave the computer on for a period of 48 to 100 hours. If problems are encountered, refer to the troubleshooting section of the manual.

appendix A
parts list

Bag #	Quantity	Component	MITS Part #
1	1	7805 voltage regulator	101074
	1	7815 voltage regulator	101048
	1	7404 integrated circuit	101022
	1	8212 integrated circuit	101071
	1	555 8-pin integrated circuit	101414
	1	74LS04 integrated circuit	101042
	3	74L04 integrated circuit	101073
	2	74LS74 integrated circuit	101088
	1	74LS27 integrated circuit	101103
	1	74LS20 integrated circuit	101134
	1	C04024, MC14024 or CD14024 integrated circuit	101183
	1	74LS08 integrated circuit	101186
	1	74LS164 integrated circuit	101187
	1	74S04 integrated circuit	101188
	1	74LS55 integrated circuit	101189
	2	74LS32 integrated circuit	101191
	1	74LS139 integrated circuit	101181
	3	8T97 integrated circuit	101420
	1	74LS123 integrated circuit	101185
	1	74LS112 integrated circuit	101190
2	32	4096-15 MOS integrated circuit	101406
3	32	16-pin socket	102103
	1	24-pin socket	102105
	1	8-pin socket	102101
	1	74 B04 switch	102348
4	1	IN4733 diode	100721
	2	330 ohm, 1/2W, 5% resistor	101926
	2	5.1K ohm, 1/2W, 5% resistor	101944
	1	5.6K ohm, 1/2W, 5% resistor	102091
	1	1K ohm, 1/2W, 5% resistor	101928
	1	1K ohm resistor pack	102074
	2	10K ohm, 1/2W, 5% resistor	101932
	1	1.3K ohm, 1/2W, 5% resistor	102216

Bag #	Quantity	Component	MITS Part #
5	1	10pf, 16v ceramic disk capacitor	100301
	1	180pf, 1Kv ceramic disk capacitor	100399
	1	200pf, 1Kv ceramic disk capacitor	100367
	1	820pf, 1Kv ceramic disk capacitor	100397
	1	.01mf, 16-20v ceramic disk capacitor	100321
	3	22mf, 16v tantalum capacitor	100395
	2	22mf, 35v tantalum capacitor	100393
6	34	.1mf, 50v epoxy dipped tantalum capacitor	100380
7	1	100-pin connector	101864
	2	card guide	101714
	4	#6-32 x 1/2" screw	100918
	1	large heat sink	101870
	2	#6-32 x 3/8" screw	100925
	2	#6 lockwasher	100942
	2	#6 nut	100933
	1	20MHz crystal	102513
	8	buss strips	101620
	10	terminal test points	101663
Misc.	1	88-16MCD Board	100226
	1	88-16MCD Manual	102706